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P1

Given

- Unit cost = $150
- Overall budget = $4,000,000
- Component cost = 50% of unit cost

1. How many processors can you produce within the budget?
2. If an engineers salary is $95,000, how many engineers can be hired using the fixed cost budget?

Answer

1. $\frac{\text{budget}}{\text{unit cost}} = \left\lfloor \frac{4000000}{150} \right\rfloor = 26666$
2. $K_v = 0.5 \cdot 150 = \$75$

   $K_f = \frac{C - K_v n}{1 + 0.1\sqrt[3]{n}} = \frac{4 \cdot 10^6 - 75 \cdot 26666}{1 + 0.1 \cdot \sqrt[3]{26666}} = \$501{,}570.09$

   $\text{Engineers} = \left\lfloor \frac{K_f}{95000} \right\rfloor = 5$

P2

Solve for n, $K_f = 1.2M, K_v = 60, C = 4M$

Answer

After inserting and reordering into a cubic equation, $n = 7506$

P3

A chip of 2.5 cm² is to be fabricated in a 28 nm process on 30 cm diameter wafers costing $1800 each. The defect density is 0.5 defects/cm². Each wafer has an 85% utilization rate. You plan to sell 2 million chips at $25 per unit and the total project budget is $35M.

1. What is the yield per chip?
2. How many good chips per wafer?
3. What is the maximum acceptable fixed cost (engineering budget)?

Answer

1. yield (assuming simplified model) $y = \frac{1}{(\text{AD})^2} = 0.64$
2. $\text{wafer size W} = \frac{\pi \cdot 30^2}{4} = 706.86\ \text{cm}^2$

   $\text{chips per wafer N} = \left\lfloor \frac{W \cdot 0.85}{2.5\text{cm}^2} \right\rfloor = 150$

   $\text{good chips per wafer} = N \cdot y = 96$
3. $\text{cost per chip} = \frac{1800}{96} = \$18.75$

   $\text{component cost} = \frac{18.75}{25} = 0.75 = \$13.125$

   $K_f = \frac{C - K_v n}{1 + 0.1\sqrt[3]{n}} = \$643{,}419.70$

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P4

Given

- $n = 20000 \text{ units}$
- $K_f = \$800{,}000$
- $K_v = \$45$

Calculate the target budget for the given volume.

Answer

$C = K_f + \left(0.1 \cdot K_f\right) \sqrt[3]{n} + K_v n = \$3{,}871{,}534.09$

P5

Given

- $\text{unit sale price} = \$120$
- $K_f = \$1{,}000{,}000$
- $K_v = \$55$

Solve for the break-even unit volume n.

Answer

$120n = 1000000 + 0.1 \cdot 1000000 \cdot \sqrt[3]{n} + 55n$

$n = 82306$

P6

Given

- defect density = 0.2/cm^2
- target yield = 0.8
- net dia area = 88 mm^2
- f = 0.13 µm

Estimate the available SRAM in bits in kB.

Answer

$\text{rbe} = 675 \cdot f^2$

$\text{A}_{\text{rbe}} = \frac{0.088 \mu m^2}{675 \cdot f^2} = 7{,}714{,}223.10$

$\text{SRAM bits } (0.6 \text{ rbe}) = \frac{A_{\text{rbe}}}{0.6} = 12{,}857{,}038 \text{ bits} = 1569.46 \text{ kB}$

P7

SoC includes 4 RISC-V cores (16kB cache, 32kB memory each), 2 DSPs (64kB cache, 128kB memory each). Net area = 3500 A; interconnect = 600 A; rbe = 0.6 (Bitcell efficiency (rbe) = 0.6 Each bit = 0.6 rbe); 1 kB = 1481 bits.

1. Compute total SRAM area used.

2. How many A-units are left for logic?
3. If one DSP is removed, how many RISC-V cores can be added?
4. With ARM Cortex-M (24kB cache, 64kB memory), what is total SRAM?

Answer

1. $4 \cdot 48 + 2 \cdot 192 = 576\ \text{kB}$
2. $3500 - 600 - 576 * 8 * 1024 * \frac{0.6}{1481} = 988.35\text{A}$
3. This is not possible to answer without further information on how much area a RISC-V core or DSP occupies. While their respective SRAM will probably dominate, we would need to know what kind of RISC-V core and DSP we are talking about (fp units? vector extension? what DSP? …)
4. The same applies as for 3., we would need information on what Cortex-M we are talking about (M0, M4+, M55, FPU?, Helium SIMD?, …)

P8

Given

- Wafer size = 150 cm²
- Defect density = 0.8 defects/cm²
- Die area = 75 mm²
- Yield model: $Y = e^{-A \cdot D}$, with A in cm²
- Wafer cost = $2000
- Component cost = $300

1. Calculate the number of total dies per wafer.
2. Estimate the yield.
3. Determine the number of functional (good) dies per wafer.
4. Calculate the manufacturing cost per working die.

Answer

1. $N = \frac{150\text{cm}^2}{75\text{mm}^2} = 200$
2. $Y = 0.55$
3. $\text{good dies} = \lfloor N \cdot Y \rfloor = 109$
4. $\text{cost per die} = \frac{2000}{N} = \$18.35$

P9

Given

- Process node: 130 nm → f = 0.13 µm
- Net die area: 80 mm² (after guard band)
- Normalized area A = 80 / (10^6 × (0.13×10^-3)^2) ≈ 4730 A-units
- Core logic + control area = 2200 A-units
- RBE (bitcell efficiency) = 0.6
- rbbe = 1481 bits/A-unit

Estimate available SRAM in bits and kB

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Answer

Available area $= 4730 - 2200 = 2530\text{A}$

$\text{SRAM} = \frac{2530 \cdot 1481}{0.6} = 6{,}244{,}883.33 \text{ bits} = 762.31 \text{ kB}$

P10

A CPU runs at 2 GHz, its prototype on FPGA runs at 200 MHz. You are designing:

- 1-way cache = 1 cycle
- 2-way cache = 1.5× 1-way latency
- 4-way = 2× latency

1. What are access latencies for 2-way and 4-way caches (in cycles)?
2. What is the largest cache size if you want access latency ≤ 2 CPU cycles?

Answer

????

P11

You need 20 GB/s bandwidth with DDR4 @ 3200 MT/s. Each I/O transfers 1 bit per cycle.

How many I/O pins are needed?

Answer

20 GB/s $= 171{,}798{,}691{,}840 \text{ bits/s } \left(\cdot 8 \cdot 2^{30}\right) = 8 \cdot n \cdot 3200 \cdot 10^6, n = 7$