SoC Architecture & Design: Homework #2

P1: Given:
- Unit cost = $150
- Overall budget = $4,000,000
- Component cost = 50% of unit cost

Tasks:
1. How many processors can you produce within the budget?
2. If an engineer's salary is $95,000, how many engineers can be hired using the fixed cost budget?

P2: Given:
$C = Kf + 0.1 \times Kf \times \sqrt[3]{n} + Kv \times n$

Task:
1. If Kf = $1.2M, Kv = $60, C = $4M, solve for n.

P3: A chip of 2.5 cm^2 is to be fabricated in a 28nm process on 30 cm diameter wafers costing $1800 each.
The defect density is 0.5 defects/cm^2. Each wafer has an 85% utilization rate.
You plan to sell 2 million chips at $25 per unit and the total project budget is $35M.

Tasks:
1. What is the yield per chip?
2. How many good chips per wafer?
3. What is the maximum acceptable fixed cost (engineering budget)?

P4: Given:
- n = 20,000 units
- Kf = $800,000
- Kv = $45

Task:

1. calculate the target budget for the given volume

P5: Given:
- Unit sale price = $120
- Kf = $1,000,000
- Kv = $55

Task:

1. solve for break-even unit volume n

P6: Given:
- Defect density = $0.2/cm^2$
- Target yield = 80%
- Net die area = 88 mm^2 = 0.88 cm^2
- f = 0.13 µm

Task:

1. Estimate available SRAM in bits and kB.

P7: SoC includes 4 RISC-V cores (16kB cache, 32kB memory each), 2 DSPs (64kB cache, 128kB memory each).
Net area = 3500 A; interconnect = 600 A; rbe = 0.6 (Bitcell efficiency (rbe) = 0.6
Each bit = 0.6 rbe); 1 kB = 1481 bits.

Tasks:
1. Compute total SRAM area used.
2. How many A-units are left for logic?
3. If one DSP is removed, how many RISC-V cores can be added?
4. With ARM Cortex-M (24kB cache, 64kB memory), what is total SRAM?

P8: Given:
- Wafer size = 150 cm^2
- Defect density = 0.8 defects/cm^2
- Die area = 75 mm^2
- Yield model: Y = e^(-A · D), with A in cm^2
- Wafer cost = $2000
- Component cost = $300

Tasks:
1. Calculate the number of total dies per wafer.
2. Estimate the yield.
3. Determine the number of functional (good) dies per wafer.

4. Calculate the manufacturing cost per working die.

P9: Given:
- Process node: 130 nm → f = 0.13 μm
- Net die area: 80 mm^2 (after guard band)
- Normalized area A = 80 / (10^6 × (0.13×10^-3)^2) ≈ 4730 A-units
- Core logic + control area = 2200 A-units
- RBE (bitcell efficiency) = 0.6
- rbbe = 1481 bits/A-unit

Task:
1. Estimate available SRAM in bits and kB.

P10: A CPU runs at **2 GHz**, its prototype on FPGA runs at **200 MHz**. You are designing:

- 1-way cache = 1 cycle
- 2-way cache = 1.5× 1-way latency
- 4-way = 2× latency

Tasks:
1. What are access latencies for 2-way and 4-way caches (in cycles)?
2. What is the largest cache size if you want access latency ≤ 2 CPU cycles?

P11: You need 20 GB/s bandwidth with DDR4 @ 3200 MT/s. Each I/O transfers 1 bit per cycle.

Task:
1. How many I/O pins are needed?