

Traffic Light

[raised by Tianjin Zhao, contact eda2018_uestc@126.com if any question.]

Background:

Traffic lights are three-color lights consisting of red, yellow, and green (green to blue-green) to signal traffic.



Figure 1 traffic light in T road

- S1 controls the left turn state of R1
- S2L controls the left turn state of R2
- S2S controls the straight state of R2
- S3 controls the straight state of R3

TASK:

1. design a traffic_light unit to control the traffic light

Specification:

Please look at figure 2 and table 1.

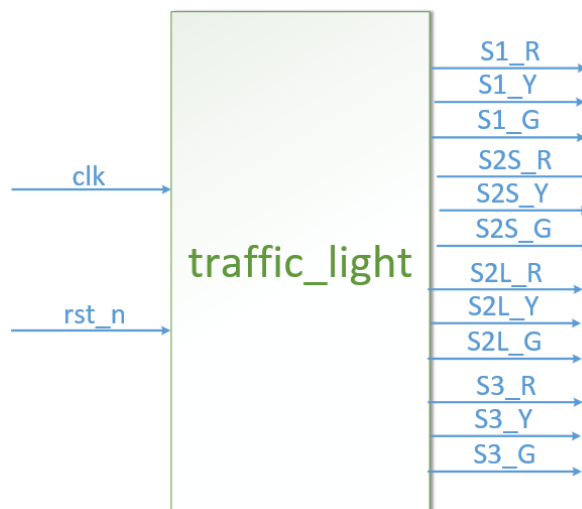


Figure 2 traffic_light

Table 1 specification of traffic_light

Port	Number of bits	Direction	Function
clk	1	In	clock
rst_n	1	In	Synchronous reset,active low
S1_R	1	Out	State of red light at S1,active high
S1_Y	1	Out	State of yellow light at S1,active high
S1_G	1	Out	State of green light at S1,active high
S2L_R	1	Out	State of red light at S2L,active high
S2L_Y	1	Out	State of yellow light at S2L,active high
S2L_G	1	Out	State of green light at S2L,active high
S2S_R	1	Out	State of red light at S2S,active high
S2S_Y	1	Out	State of yellow light at S2S,active high
S2S_G	1	Out	State of green light at S2S,active high
S3_R	1	Out	State of red light at S3,active high
S3_Y	1	Out	State of yellow light at S3,active high
S3_G	1	Out	State of green light at S3,active high

There are three state of traffic:

- R1 turn left and R2、 R3 stop
- R2、 R3 go straight and R1 stop and R2 can't turn left
- R2 turn left and R1、 R2 stop

notice:

- ***In any state, if the rst_n is active, the initial state(all lights turns to RED) will be entered immediately in the next posedge clk.***
- ***Red and green light holds on 40 clock cycles.***
- ***Yellow light holds on 10 clock cycles.***

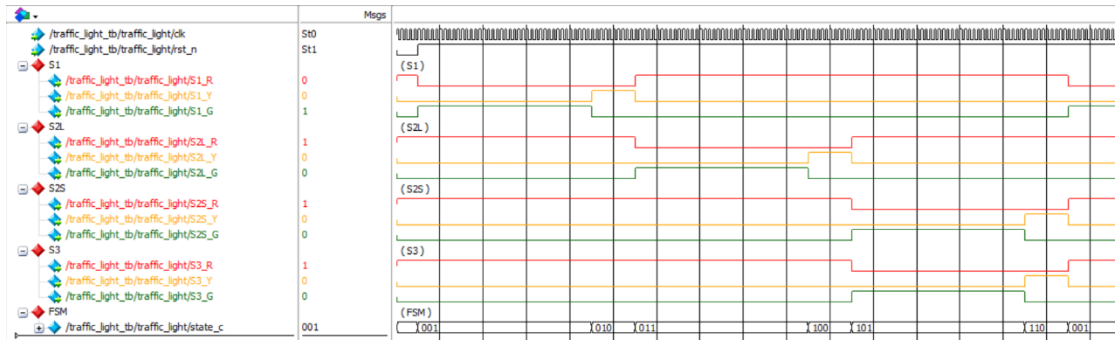


Figure 3 timing diagram

Requirements:

1. The port name must be kept strictly the same as the description table.
2. The file name must be "traffic_ligh.vhd".
3. The entity name must be "traffic_light".
4. Coding in VHDL.
5. This job should be synthesizable.
6. Upload your code and synthesize report to eda2018_uestc@126.com.