Programming Assignment #3

TDF Simulator

Introduction:

As the leading academic EDA tool provider, we provide our customers with a PODEM-based *NTU ATPG* (automatic test pattern generator) for single stuck-at faults. This ATPG system has two major functions: test pattern generation and fault simulation. However, our customers hope that we can support *transition delay fault* (TDF) simulation.

Our customers wrap their *CUT* (circuit under test) by flip-flops, which are stitched in a scan chain. Therefore, we need to chain the original primary inputs (PI) and primary outputs (PO) so that we can do the TDF simulation by using *launch-on-shift* (LOS) technique. In this PA, we first show you how to run *tdfsim* mode. Then, you are asked to build the whole TDF simulator.

Tutorial:

First, please enter the bin directory, and run the golden binary to see results of ATPG mode. Notice that you should run these commands on *Linux* platforms with *GCC* version 4.8 or newer. In case you see any compilation error, please check if your platform supports *C++11*. If not, you can update your OS or GCC version. The code can be compiled correctly on edaU1 of edaunion. Simply type the following commands.

```
cd bin
./golden_tdfsim –ndet 1 -tdfsim ../tdf_patterns/c17.pat ../sample_circuits/c17.ckt
```

Then you will see results generated by *tdfsim* on the screen. Note that *–ndet 1* means the number of detection is one; *i.e.* a fault will be dropped as soon as they are detected once. In this programming assignment, you can assume that *-ndet* is always one. This feature will be used later in the final project.

Second, please enter the *src* directory, then compile the source code by typing

```
cd src
make
```

If compilation is successful, an executable file '`atpg`' is generated. In the same directory, you can run this software in *tdfsim* mode by typing the following command.

```
./atpg –tdfsim ../tdf_patterns/c17.pat ../sample_circuits/c17.ckt
```

Notice that you will see nothing happened because we are not build the simulator yet. Your job is to use what you have learned in the testing class to build the whole TDF simulator. Our customers expect to see the following information shown on the screen.

```
#Circuit Summary:
#---------------
#number of inputs = 5
#number of outputs = 2
#number of gates = 6
#number of wires = 11
#atpg: cputime for reading in circuit ../sample_circuits/c17.ckt: 0.0s 0.0s
#atpg: cputime for levelling circuit ../sample_circuits/c17.ckt: 0.0s 0.0s
#atpg: cputime for rearranging gate inputs ../sample_circuits/c17.ckt: 0.0s 0.0s
#atpg: cputime for creating dummy nodes ../sample_circuits/c17.ckt: 0.0s 0.0s
#atpg: cputime for generating fault list ../sample_circuits/c17.ckt: 0.0s 0.0s
vector[7] detects 3 faults (3)
vector[6] detects 5 faults (8)
vector[5] detects 3 faults (11)
```

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```
vector[4] detects 1 faults (12)
vector[3] detects 3 faults (15)
vector[2] detects 0 faults (15)
vector[1] detects 4 faults (19)
vector[0] detects 4 faults (23)

# Result:
-----------------------
# total transition delay faults: 34
# total detected faults: 23
# fault coverage: 67.647059 %
#atpg: cputime for test pattern generation ../sample_circuits/c17.ckt: 0.0s 0.0s
```

I/O Files:

We explain the I/O information using the following circuit, *c17*. Please note that our customer wrap the circuit so PIs and POs are stitched into a scan chain. The entrance of the chain is the first PI (*e.g.* PI_1), and the exit of the chain is the last PO (*e.g.* PO_2).

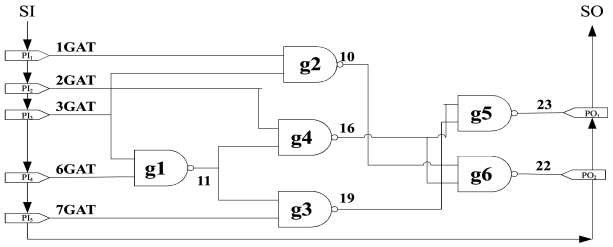

Figure 1. *c17* circuit

Notice that we chain the PIs and POs according to the order they appear in the file. For example, in C17, we chain the PIs and POs from *1GAT(0)* to *23GAT(9)*.

```
name C17.iscas
i 1GAT(0)
i 2GAT(1)
i 3GAT(2)
i 6GAT(3)
i 7GAT(4)

o 22GAT(10)
o 23GAT(9)

g1 nand 6GAT(3) 3GAT(2) ; 11GAT(5)
g2 nand 3GAT(2) 1GAT(0) ; 10GAT(6)
g3 nand 7GAT(4) 11GAT(5) ; 19GAT(7)
g4 nand 11GAT(5) 2GAT(1) ; 16GAT(8)
g5 nand 19GAT(7) 16GAT(8) ; 23GAT(9)
g6 nand 16GAT(8) 10GAT(6) ; 22GAT(10)
```

Figure 2. *c17* circuit file

The following file is our test pattern (*c17.pat*). The circuit information is shown at the beginning. Then, all test vectors are shown after the keyword "T", which composed of two parts. The two parts are separated by a space. First part is for our scan inputs (V_1), and the second part is one additional bit for V_2 scan input in the LOS. Take the first pattern T'00110 1' as example, the first pattern will be '00110'. That means, PPI1=0, PPI2=0, PPI3=1, PPI4=1, PPI5=0. After we shift in the scan chain with V_1, we then apply one more bit to scan in a '1'

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for V_2. So PPI1=1, PPI2=0, PPI3=0, PPI4=1, PPI5=1. Then we apply one capture clock to capture the response of CUT. Then we shift out the captured responses of the first pattern and shift in the second pattern '10011'. That means, PPI1=1, PPI2=0, PPI3=0, PPI4=1, PPI5=1. The same process will repeat for eight LOS test patterns.

```
#Circuit Summary:
#---------------
#number of inputs = 5
#number of outputs = 2
#number of gates = 6
#number of wires = 11
T'00110 1'
T'10111 0'
T'10001 1'
T'01000 0'
T'11011 1'
T'01100 0'
T'10000 1'
T'01111 0'
```

Figure 3. *c17* pattern file

Assignments:

Enter *src* directory and edit the file *tdfsim.cpp*. You can also modify other files, but you should clearly write down it in the report.

We give you a simple hint.

Step 1: Assign V_1 pattern and run a good simulation to check which faults are activated.

Step 2: Shift in a bit and obtain V_2 pattern

Step 3: Do a single stuck-at fault simulation to check which faults (from step 1) are detected.

Step 4: Drop the faults that have been detected and continue to the next pattern

Notice:

In previous programming assignment, we generate stuck-at fault in function, *generate_fault_list()*. This function will collapse equivalent fault into one fault. However, we can't collapse these TDF, so you don't need to do any fault collapsing in this assignment. Please answer why we can't collapse transition delay faults and implement a new fault generation function.

1) Please fill in the following table in your report.

circuit number	number of gates	number of total TDFs	number of detected faults	number of undetected faults	transition delay fault coverage
C17	6	34	23	11	67.64%
C432					
C499					
C880					
C1355					
C2670					
C3540					
C6288					
C7552					

2) Please show the critical parts of your code and explain it in your report.

3) Please show how you generate the transition delay fault list and why we cannot collapse TDF in your report.

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Grading:
80% correctness
20% report

Submission:
Make a directory <*student_id*>*_pa3*
Please copy 3 items /*src*, *report*, *readme* into directory. Then submit a single **.tgz* file to CEIBA system. Please submit your code on *ceiba*. Include everything so that your code can be easily compiled using 'make'. Please use the following command to compress a whole directory: `tar -zcvf <filename>.tgz <dir>`

Copying source code results in zero grade for both students!
