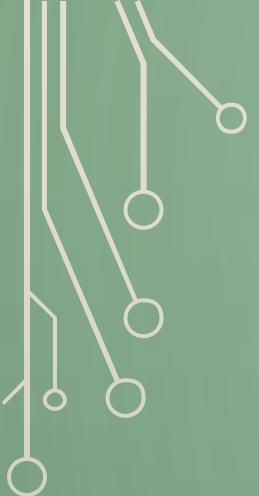
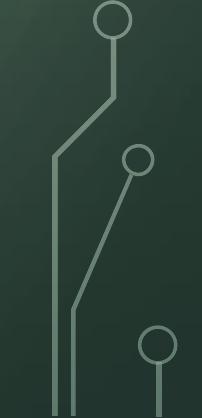


Introduction to Altera DE2-115

Course : ITI 1100C
Term: Winter 2016
Professor : Dr. Ahmed Karmouch



There are only 10 types of people

- One who understands binary
 - The other who don't.
- 
- 

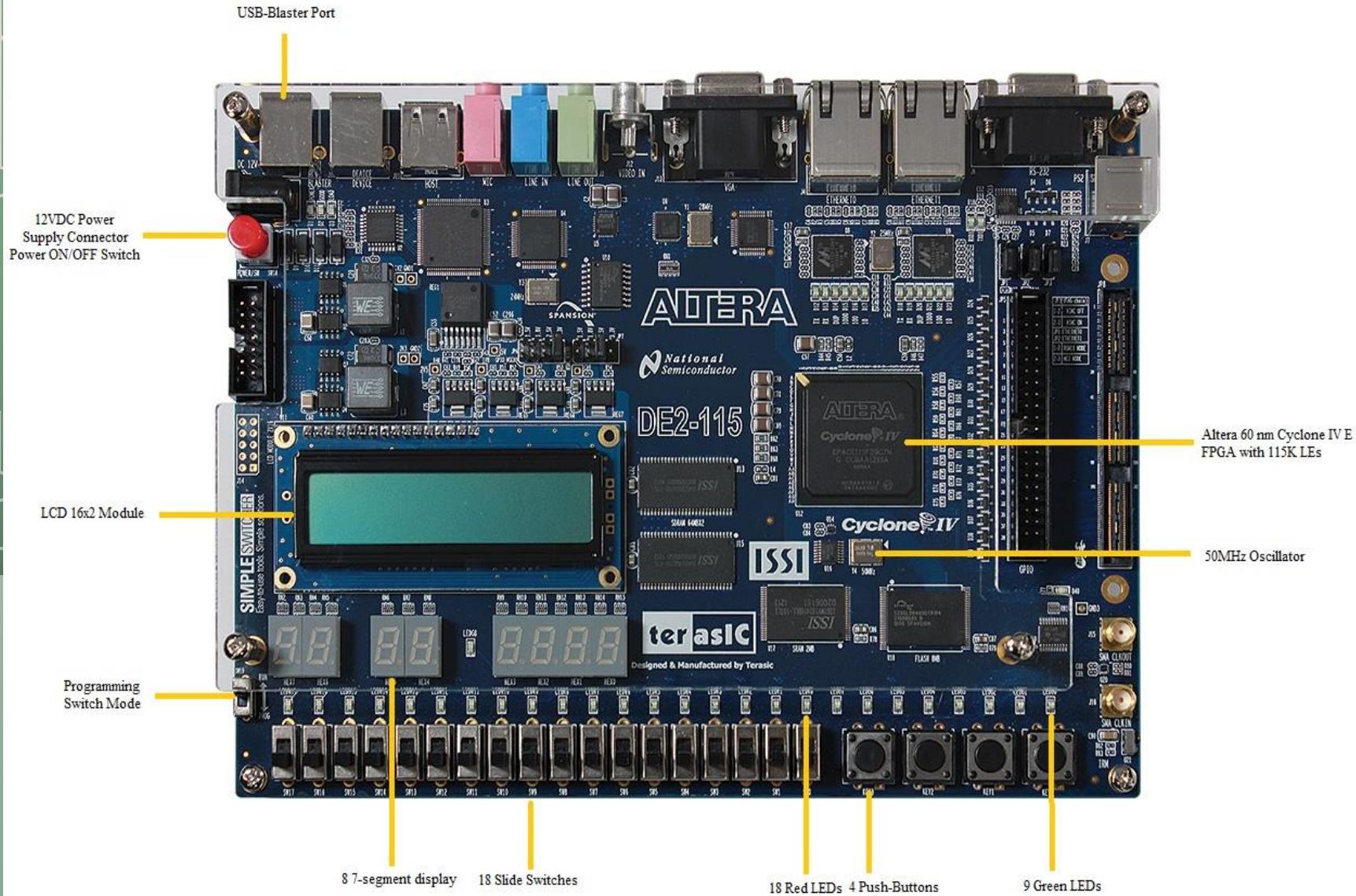
AGENDA

- Getting Started
 - Introduction to *Altera FPGA*
 - Introduction to *Quartus II 13.0*
 - The fundamental parts of *New Altera and Quartus*
- Detailed example through the software
- What to do during your lab
- Marks distribution
- Lab Report Formats.

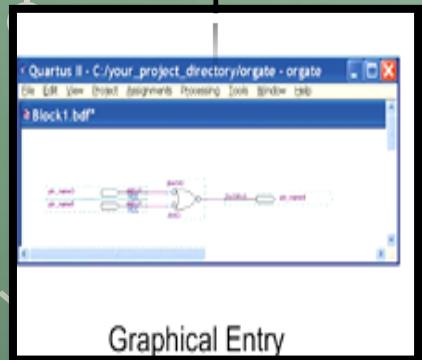
ALTERA FPGA DE2-115

- A Field Programmable Gate Array (FPGA) is a Programmable Logic Device (PLD) with higher densities and capable of implementing different logic functions in a short period of time.

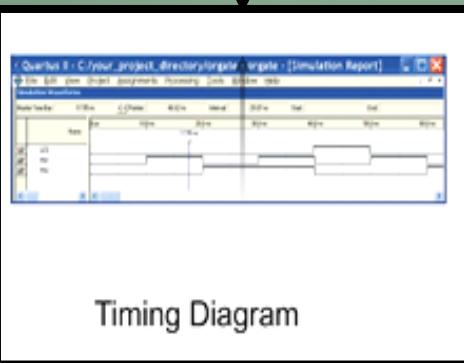
Altera DE2-115



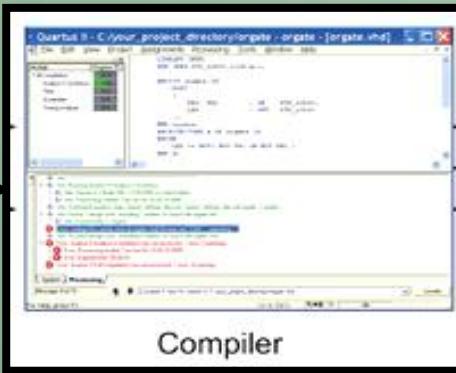
DESIGN PROCESS FOR A SCHEMATIC



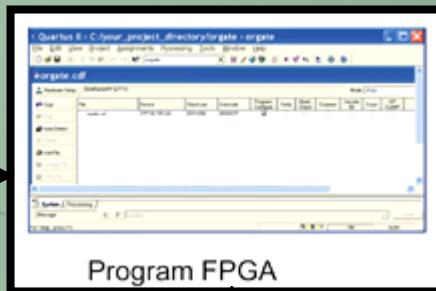
Design



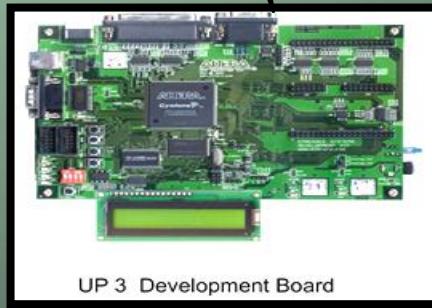
Simulation



Compilation



Verification



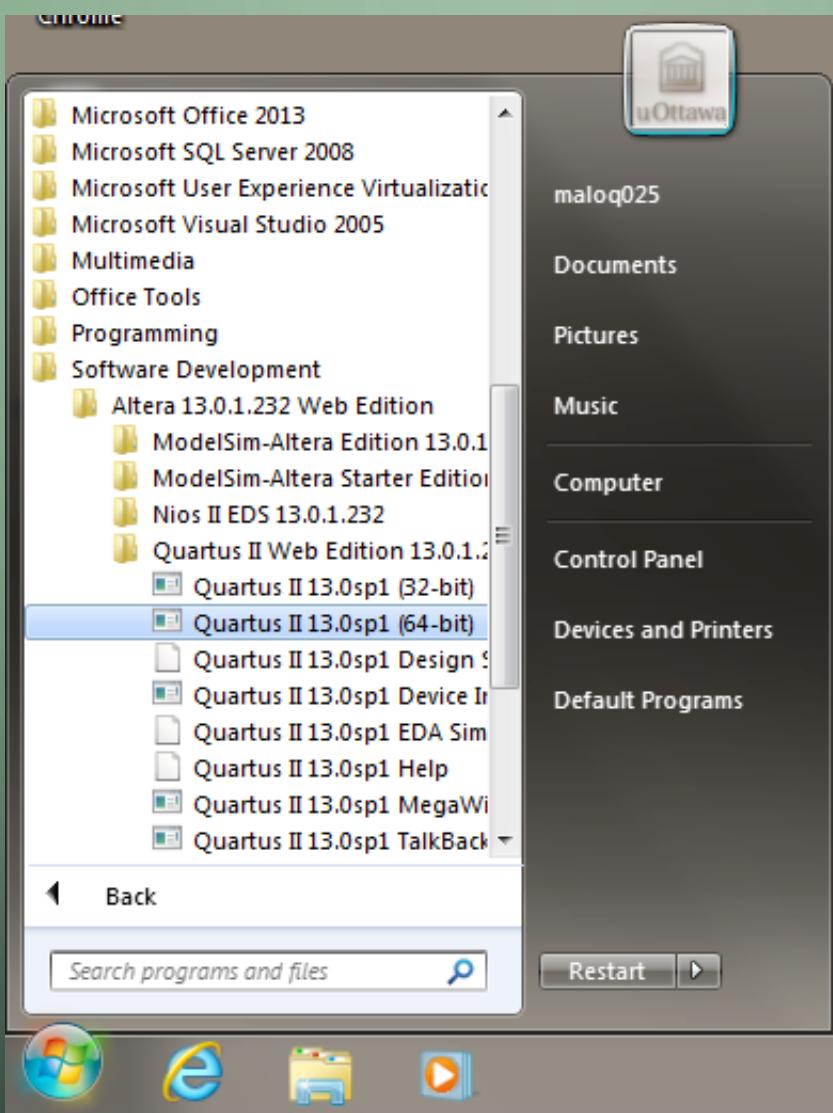
UP 3 Development Board

INTRODUCTION TO QUARTUS II 13.0

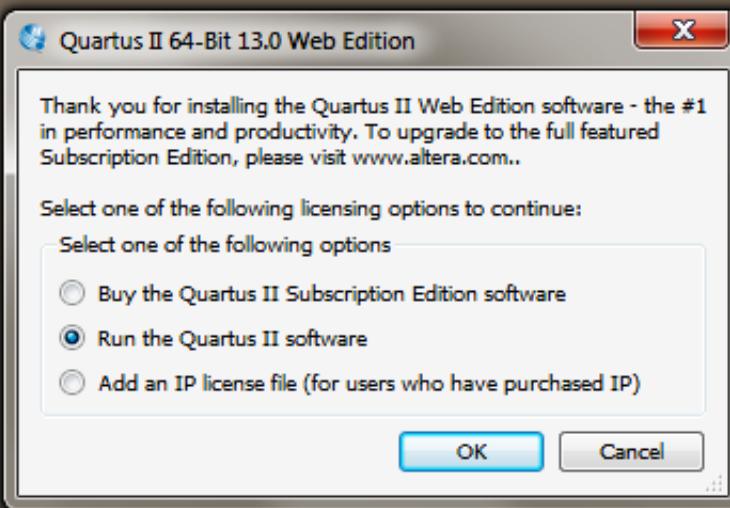
- **Quartus Version 13.0 web edition** can be downloaded from the Internet

- <http://dl.altera.com/13.0/?edition=web>
- DO NOT try to download different versions.
- **Version 9.0** is NO longer available or used at uOttawa labs. It will not be compatible with the University versions.

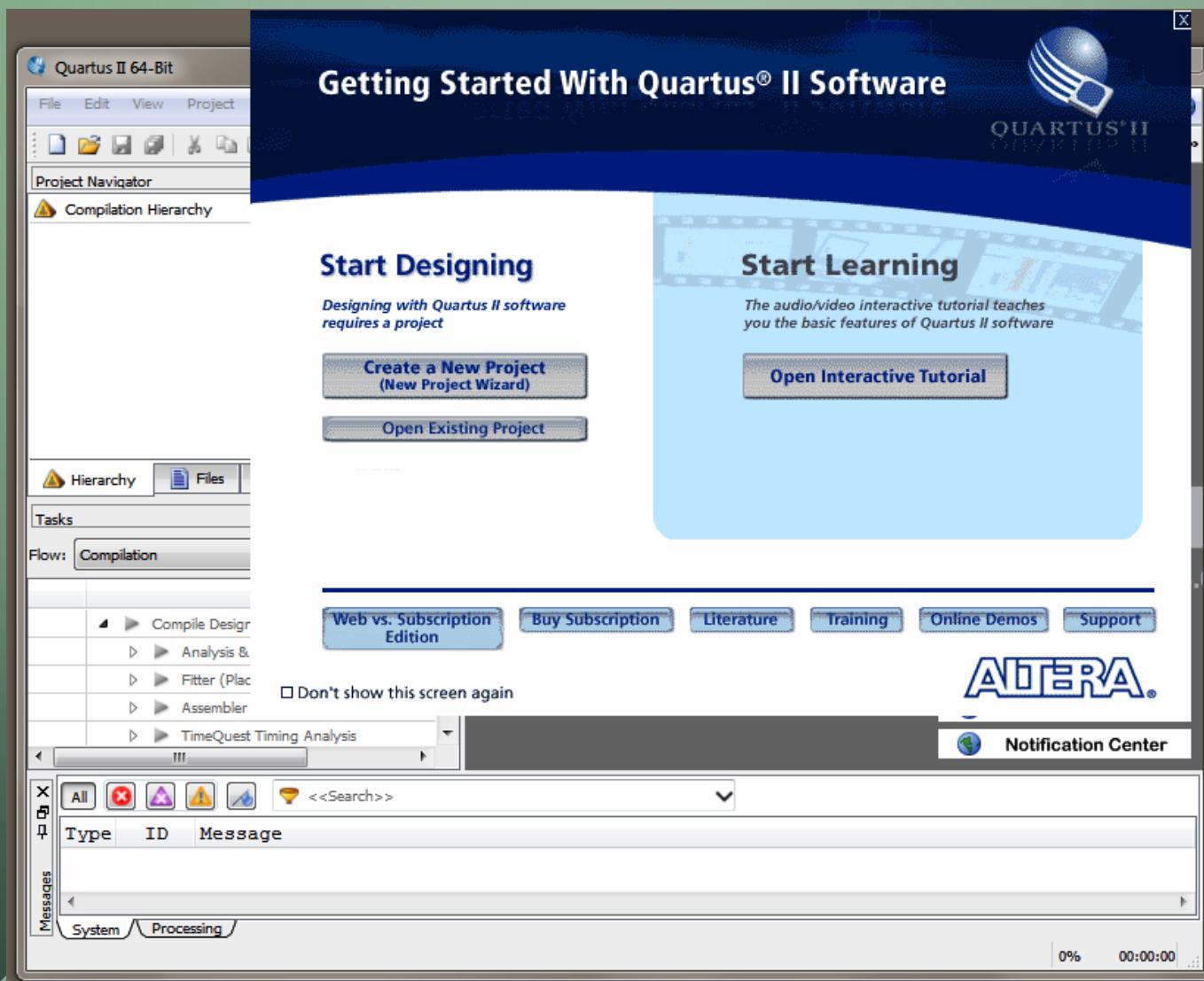
Altera Quartus II 13.0



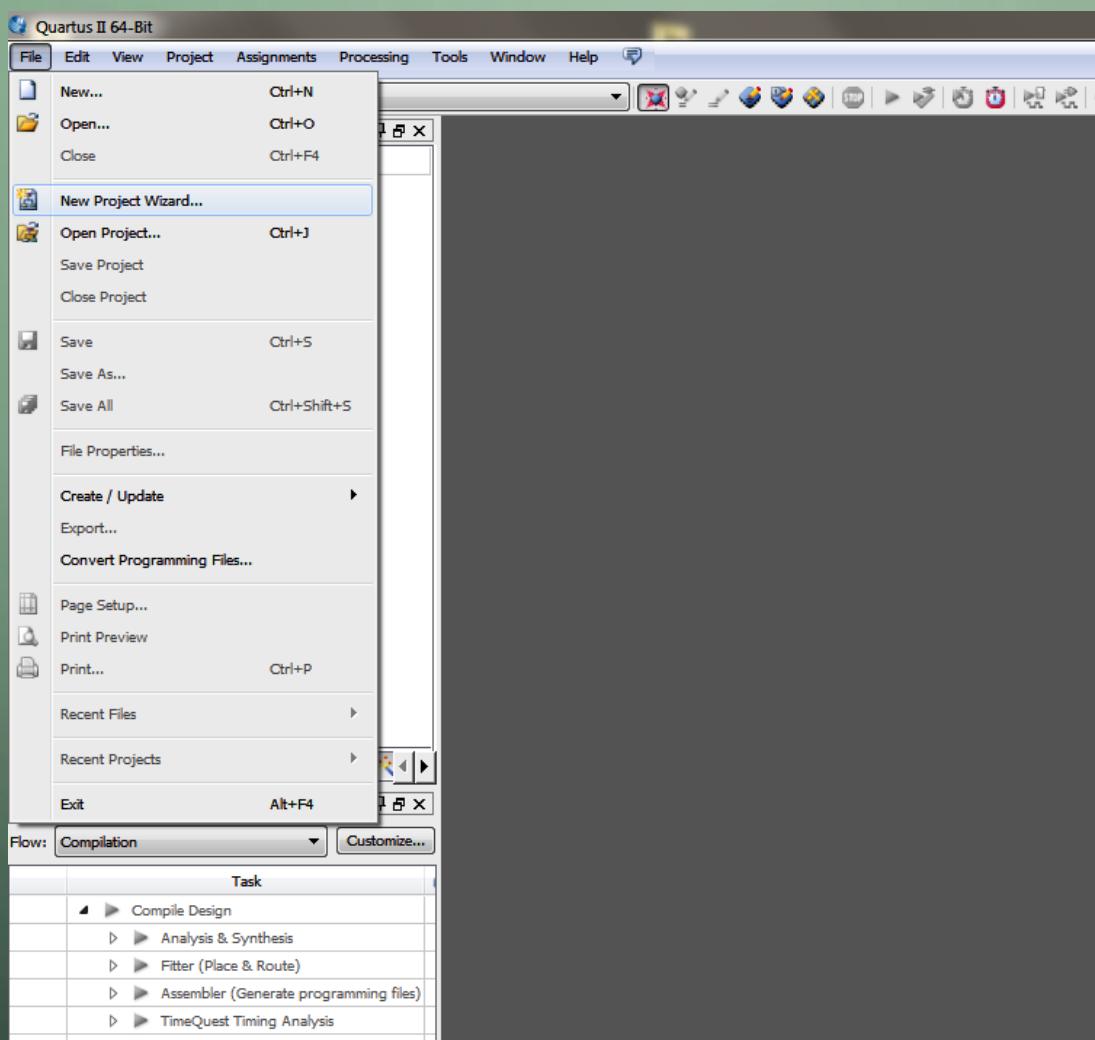
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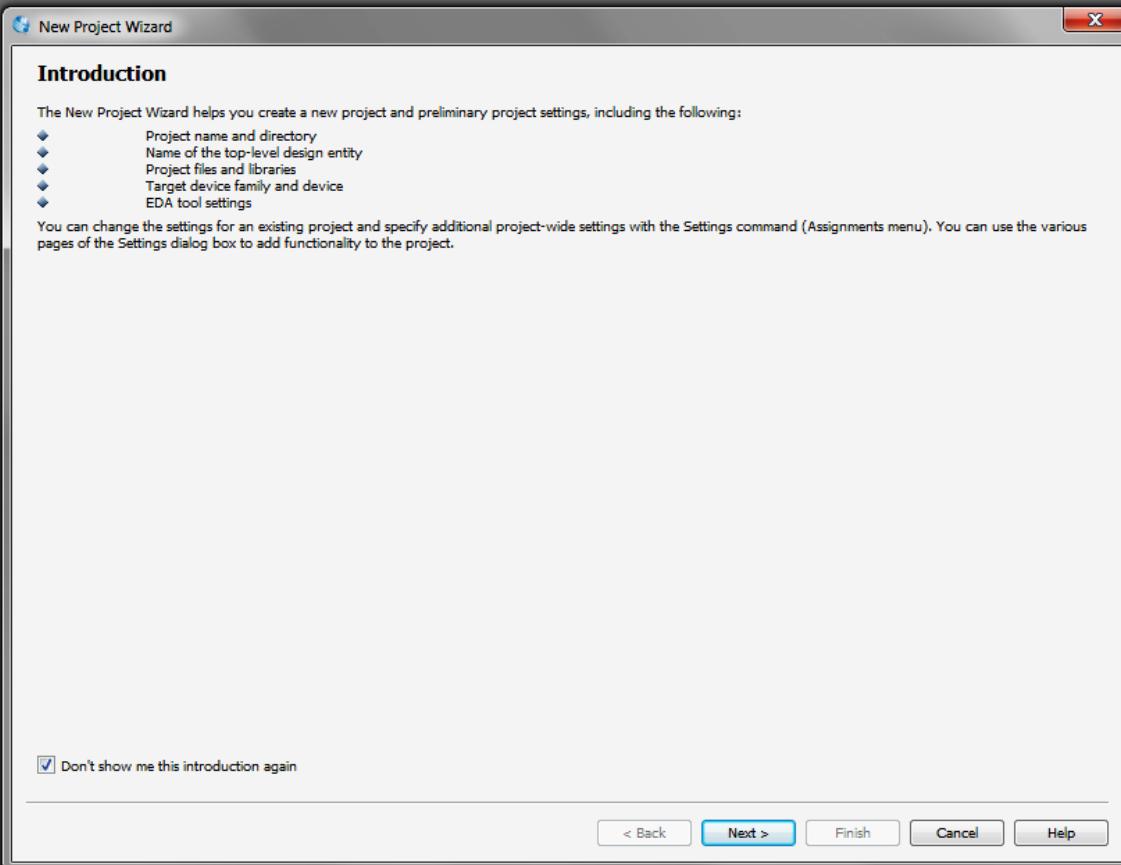
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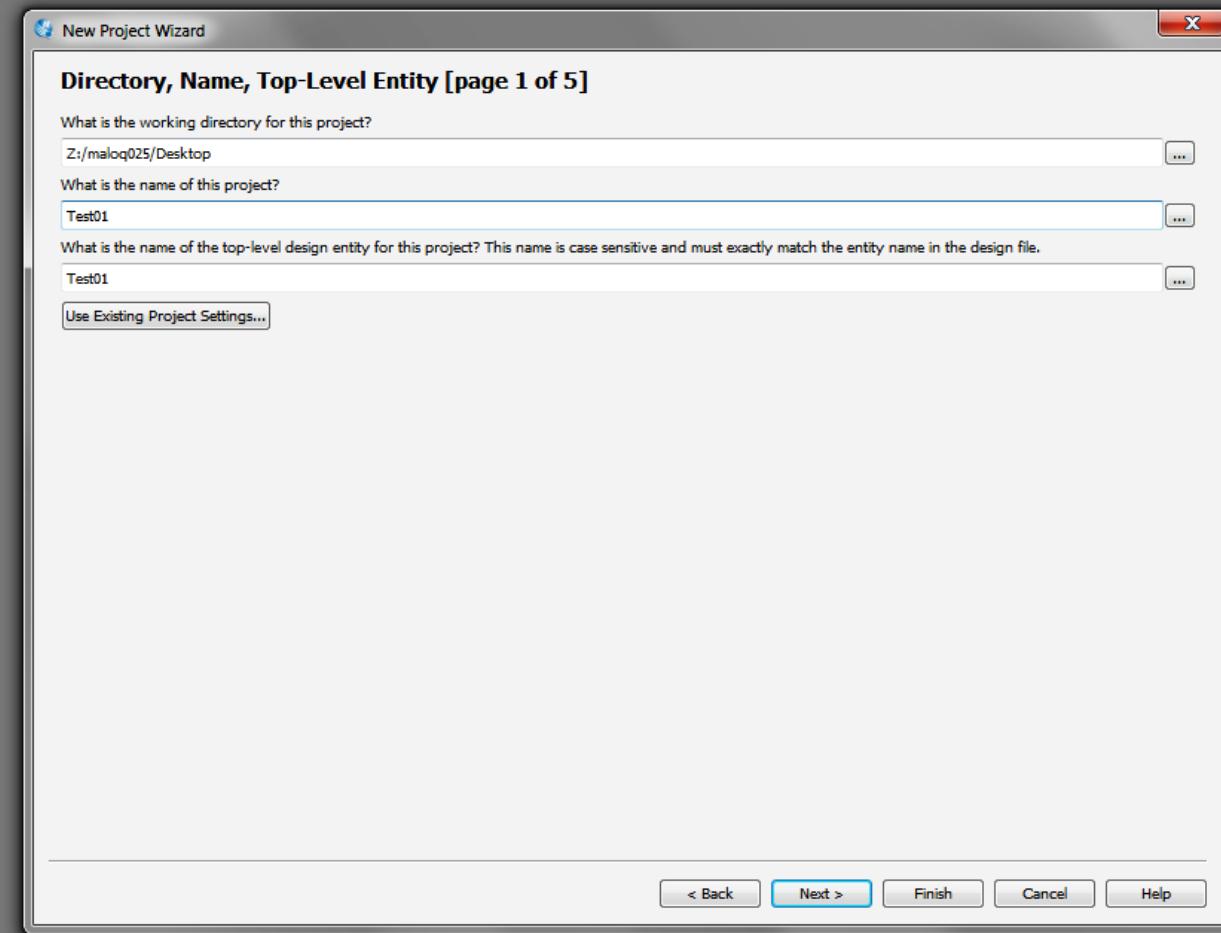
Altera Quartus II 13.0



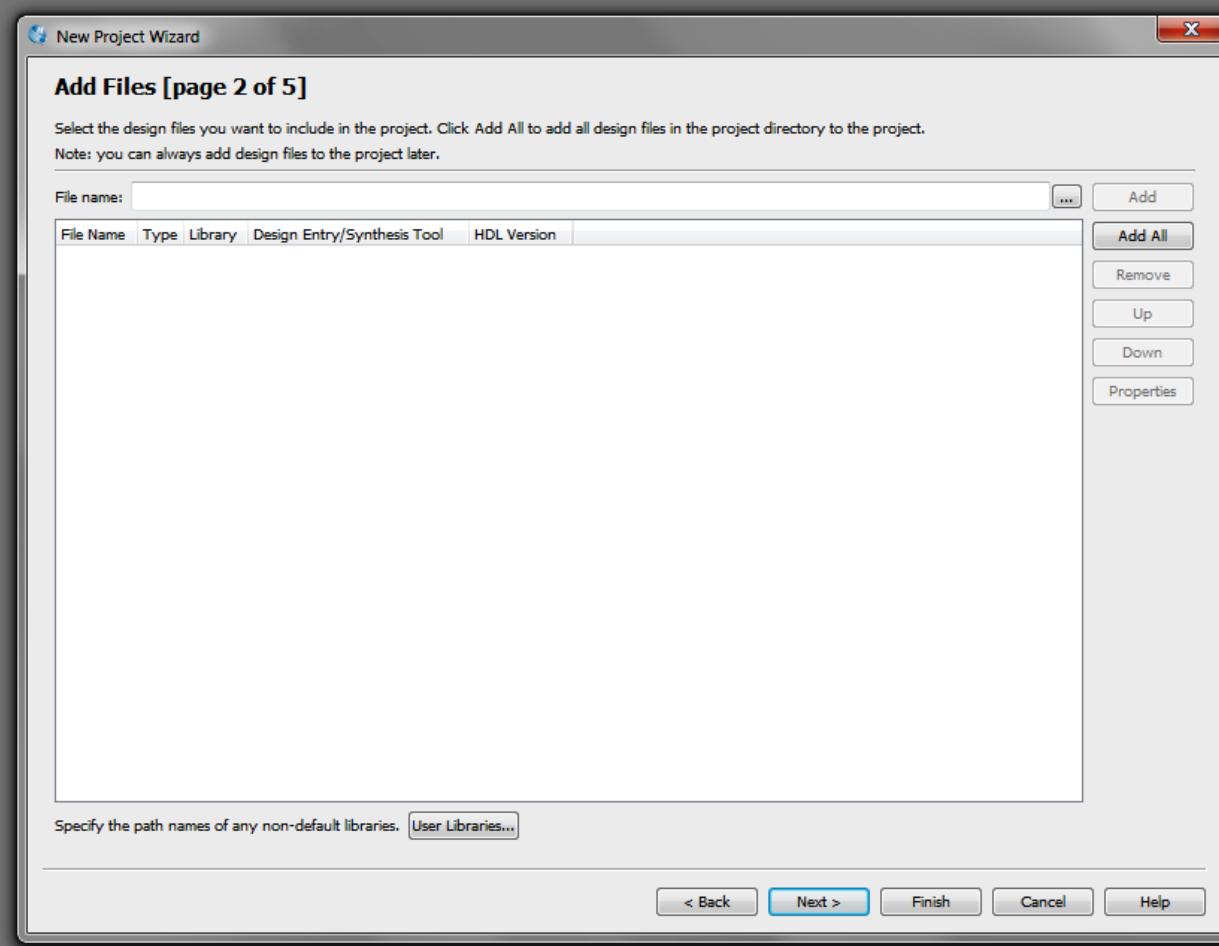
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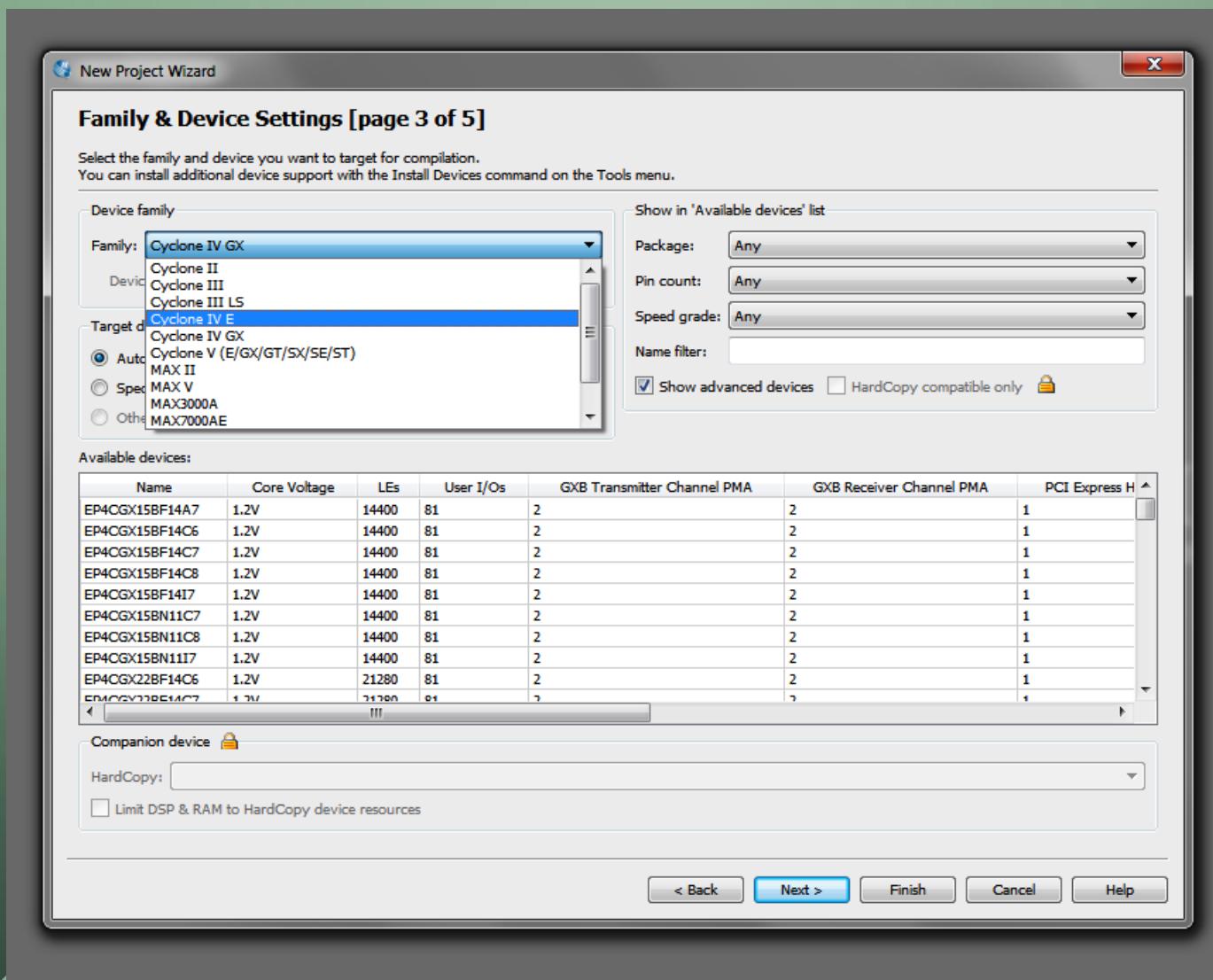
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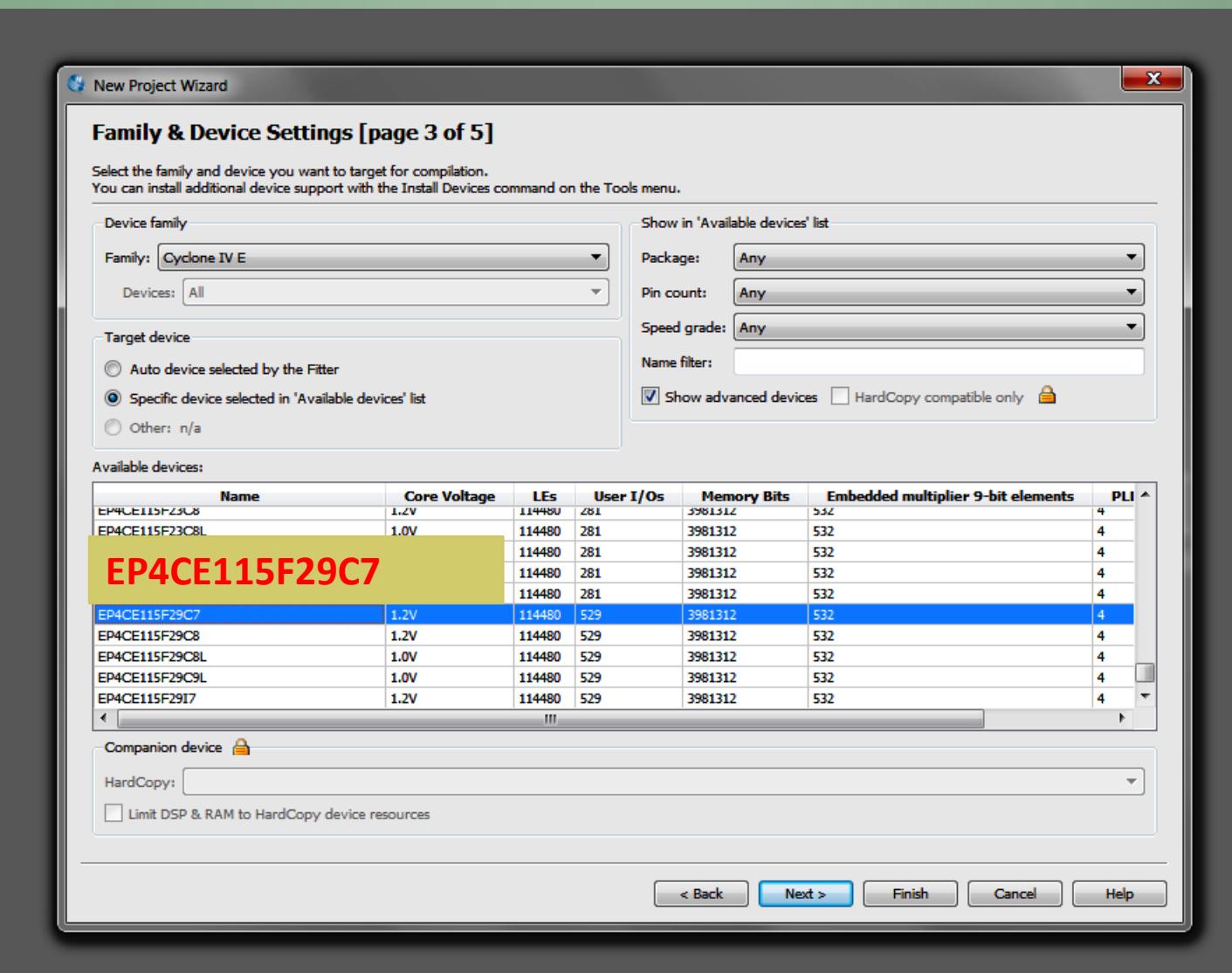
Altera Quartus II 13.0



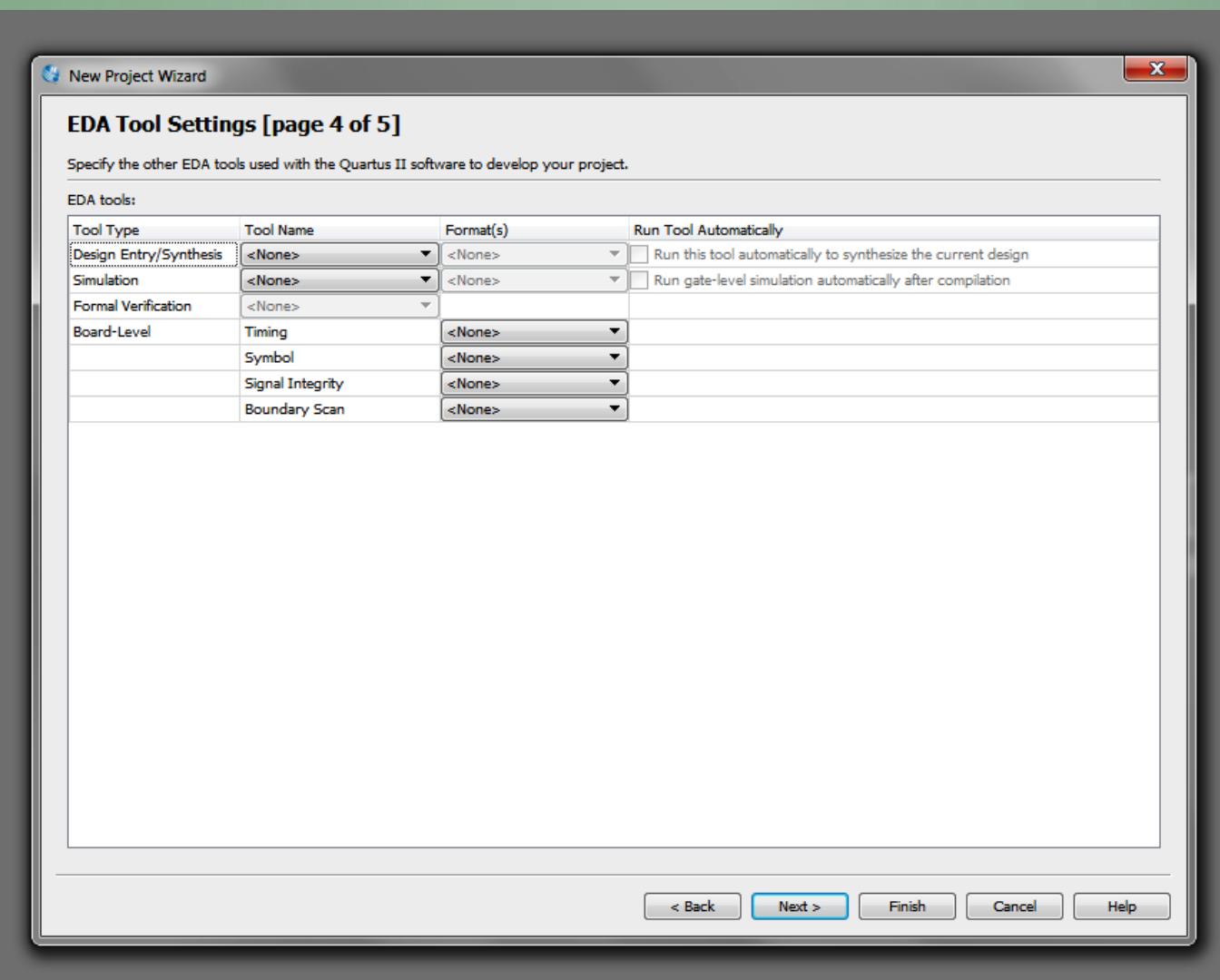
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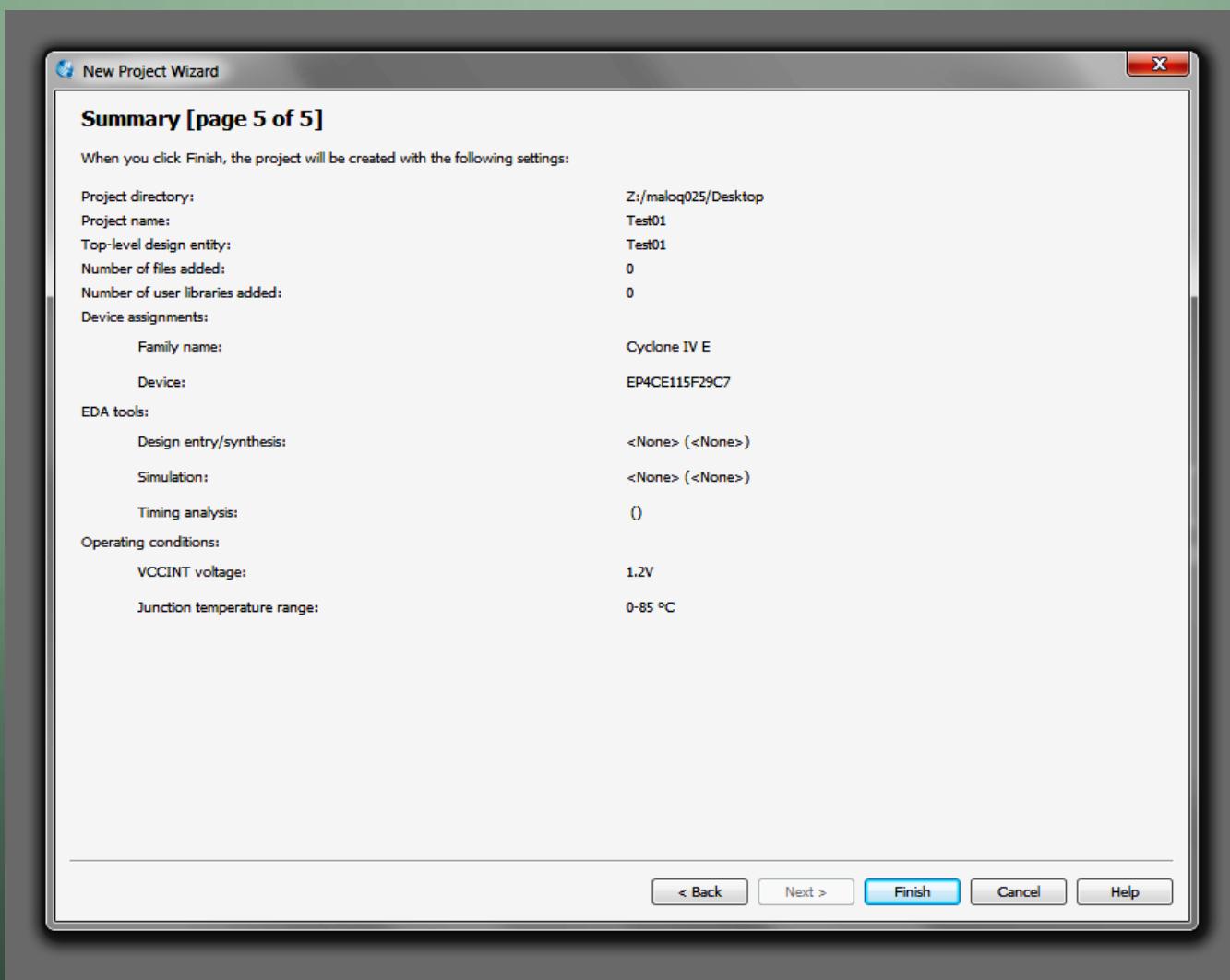
Altera Quartus II 13.0



Altera Quartus II 13.0



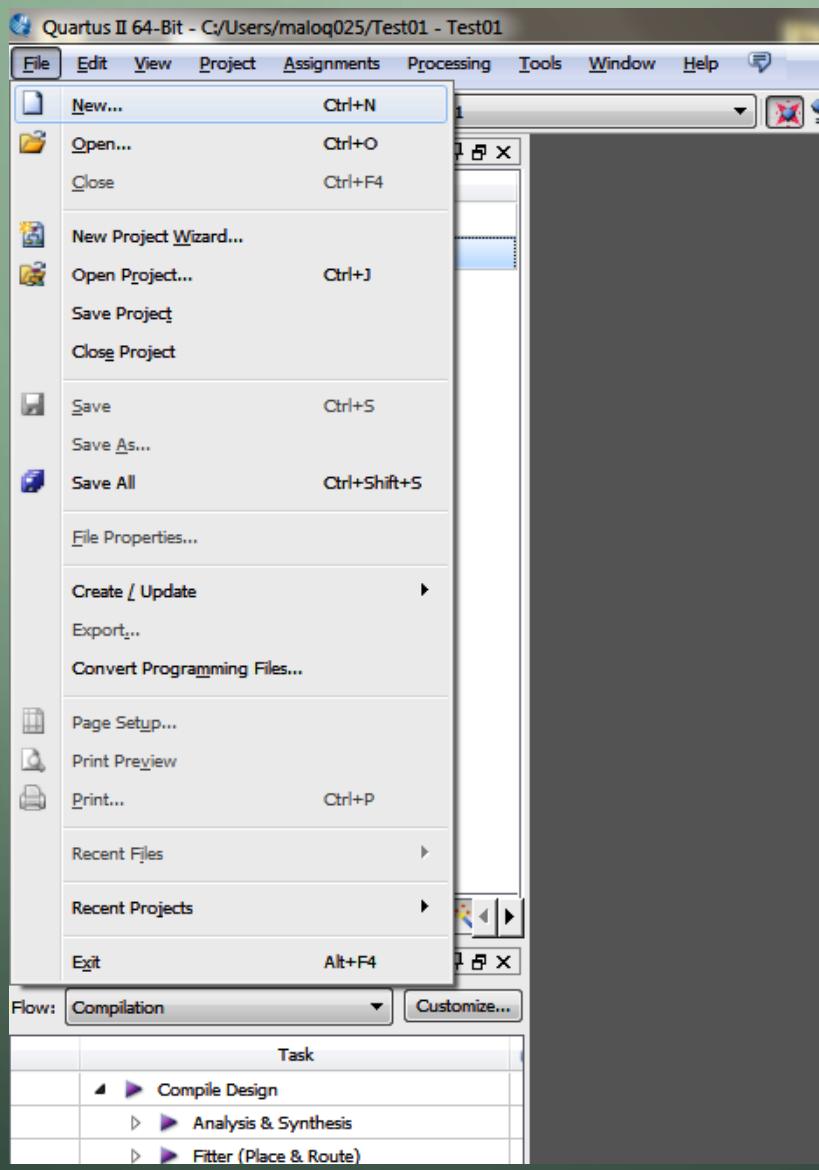
Altera Quartus II 13.0



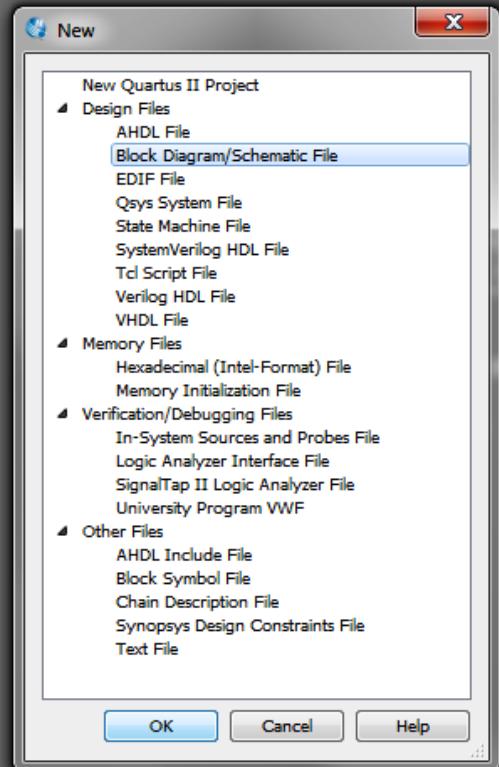
Altera Quartus II 13.0



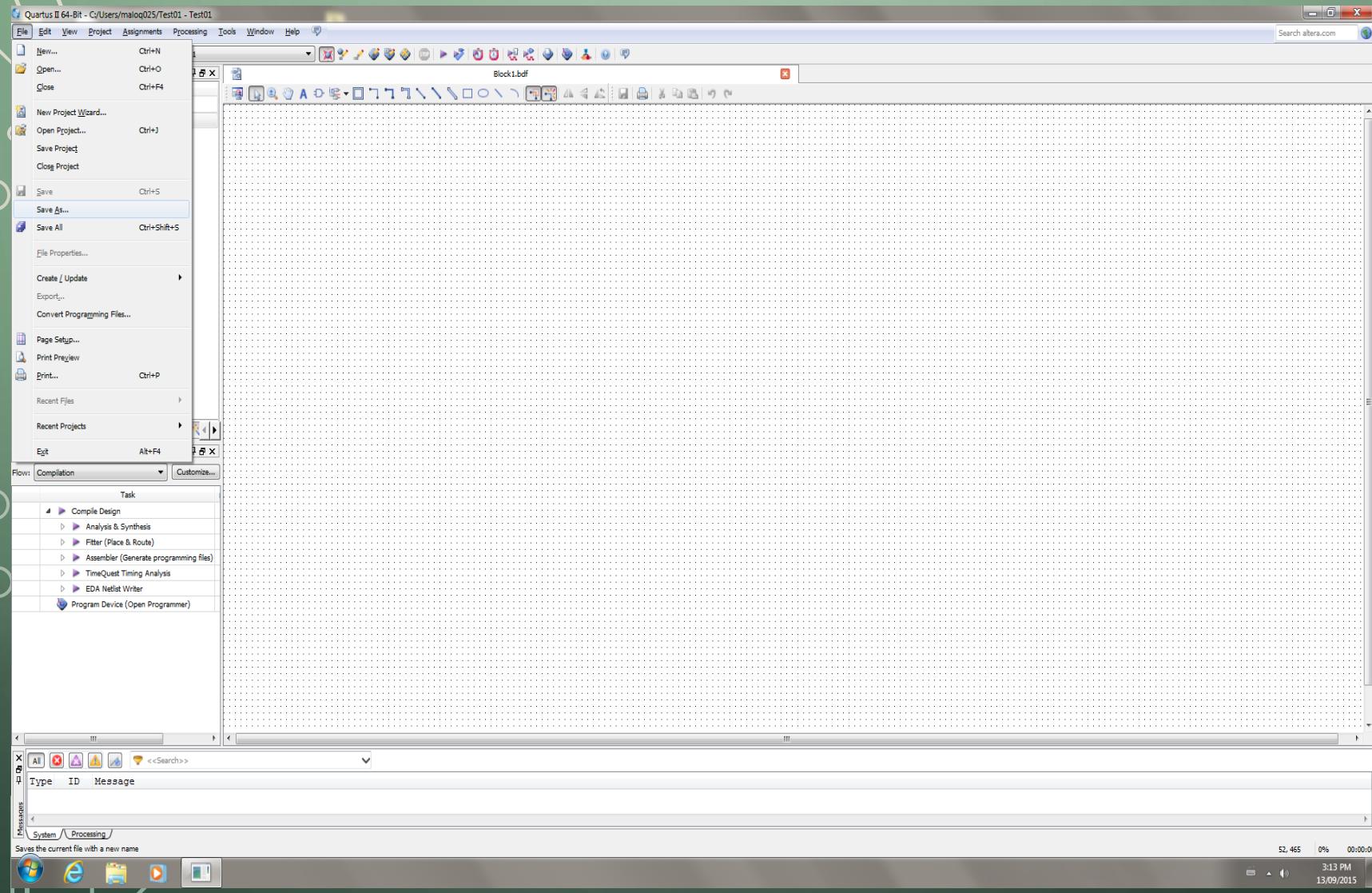
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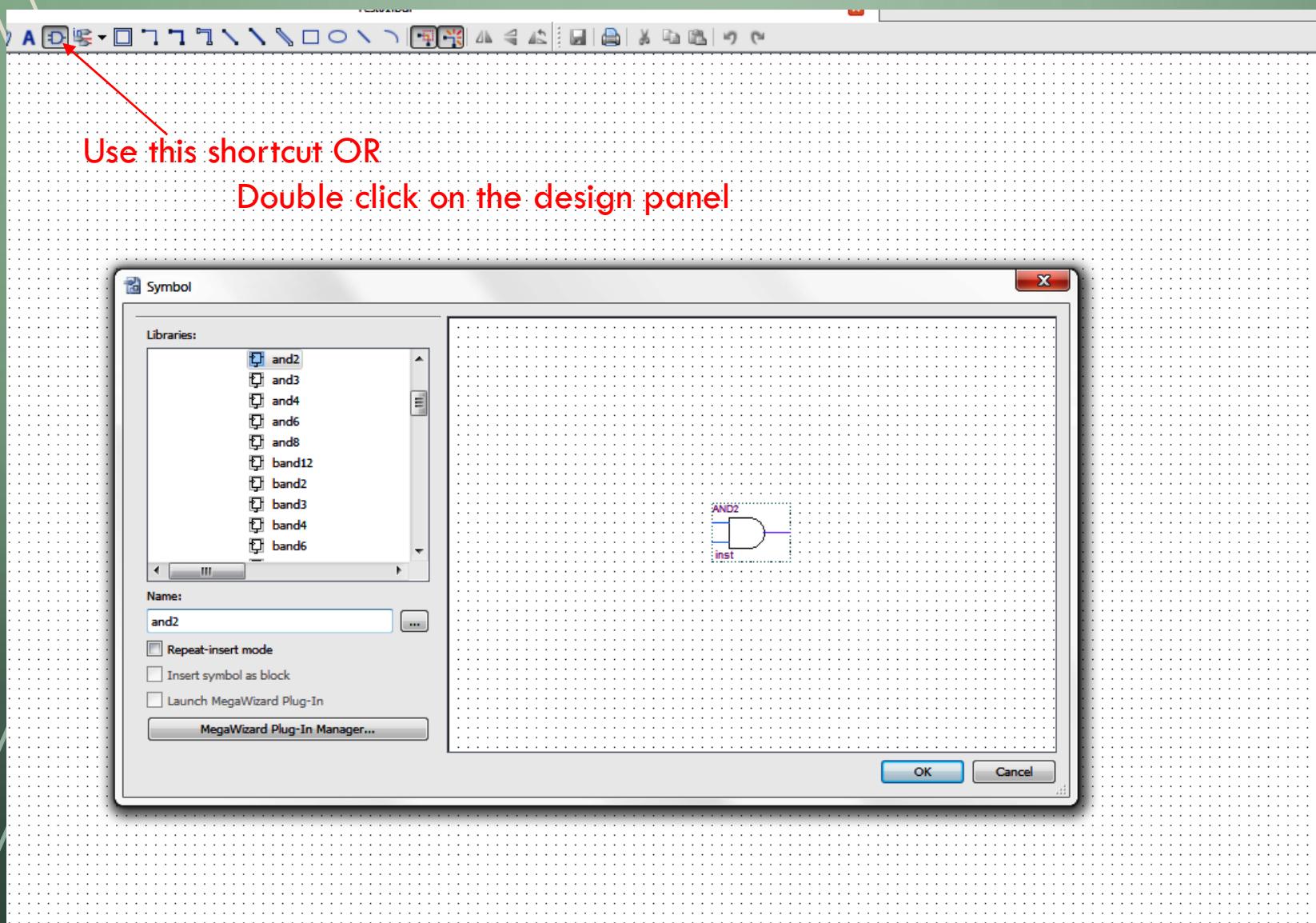
Altera Quartus II 13.0



Altera Quartus II 13.0



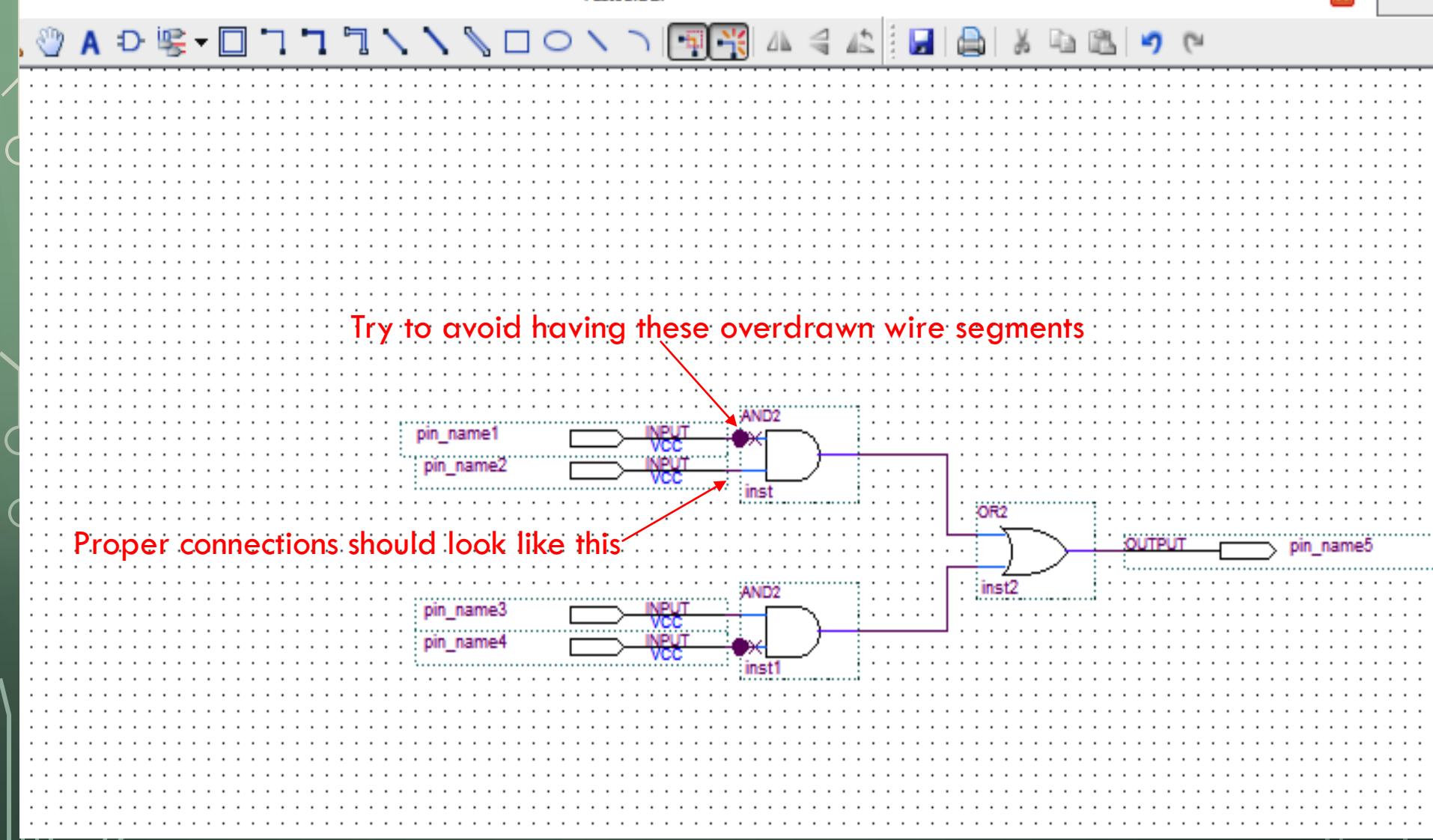
Altera Quartus II 13.0



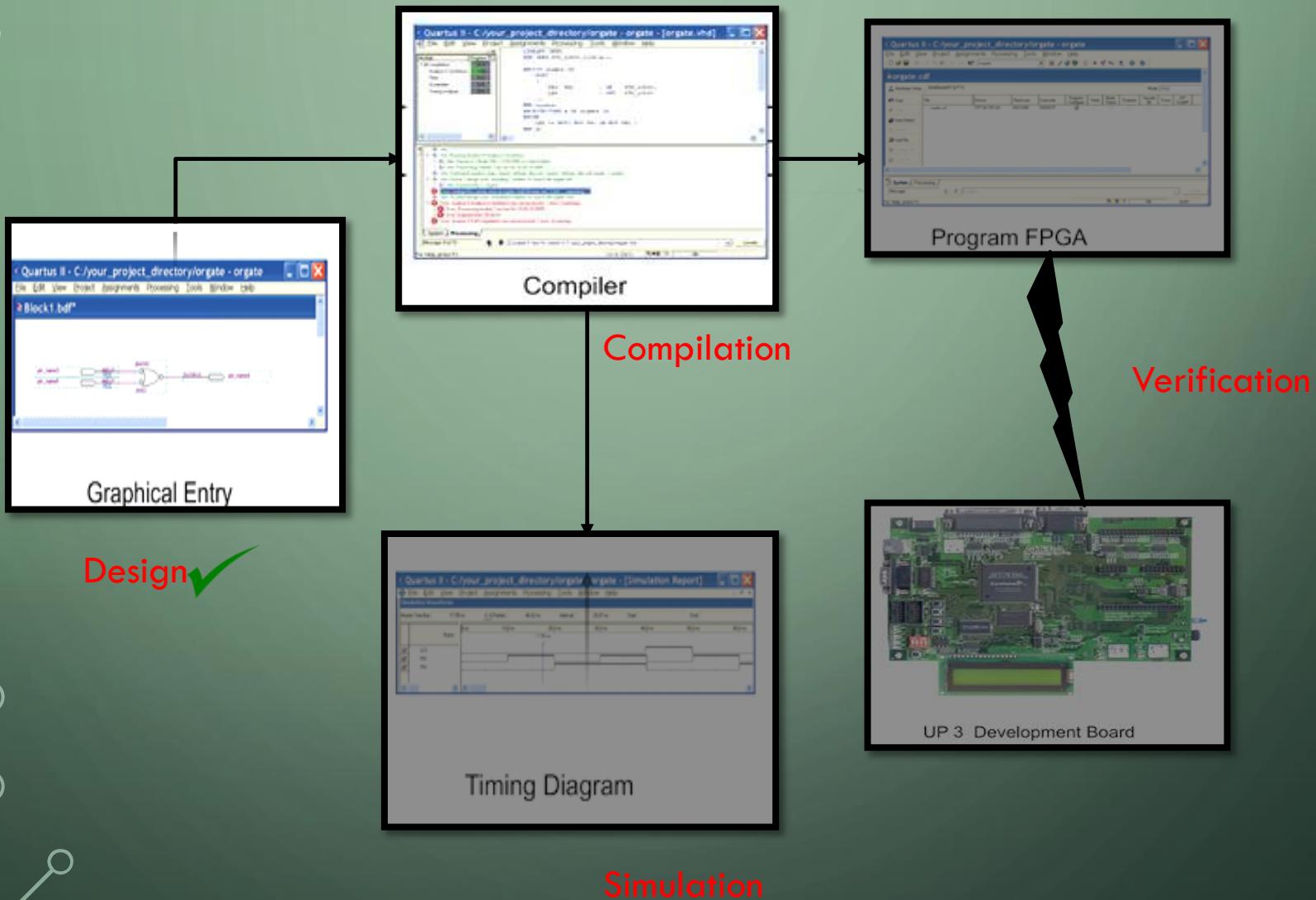
Use this shortcut OR
Double click on the design panel

Altera Quartus II 13.0

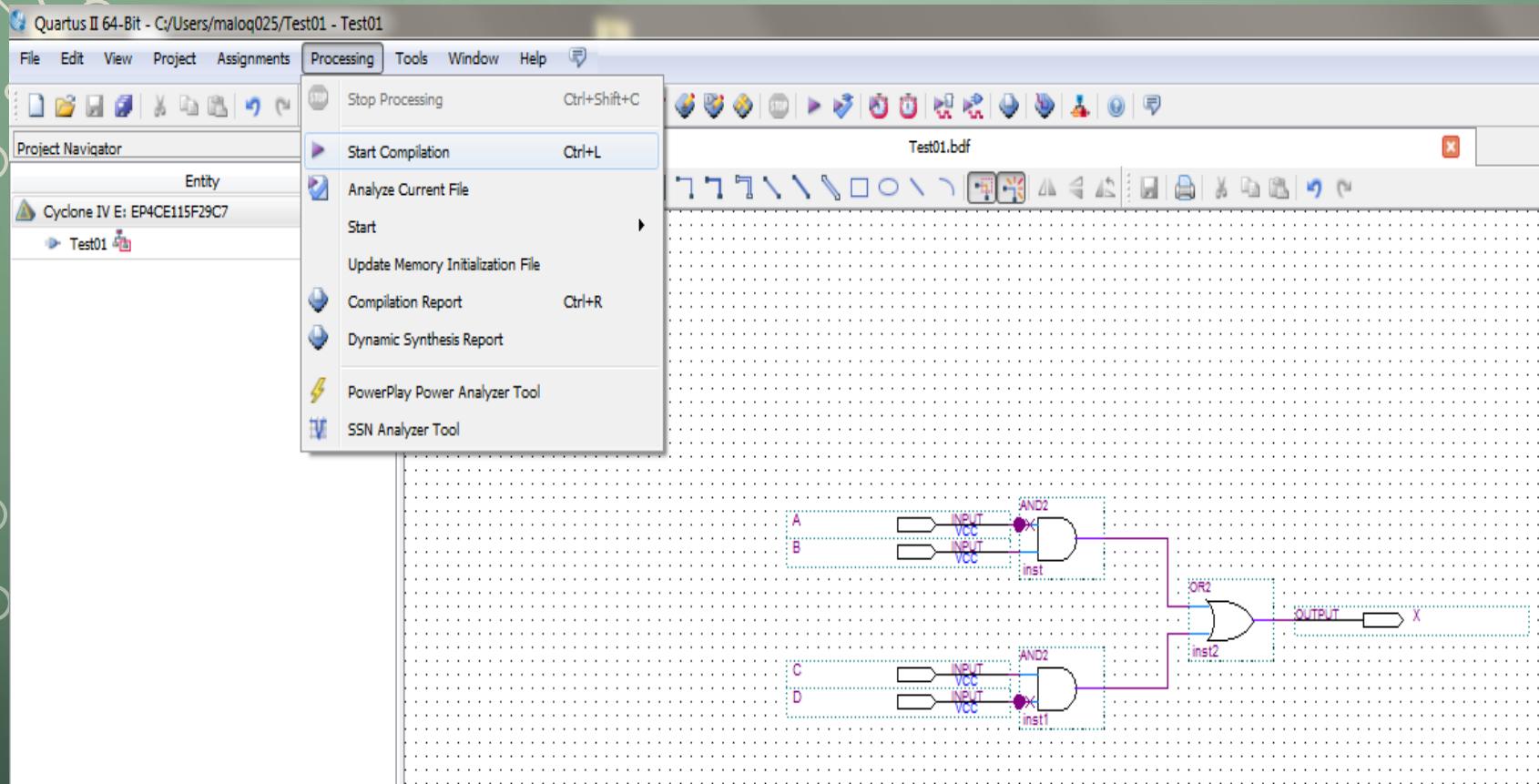
Test01.bdf*



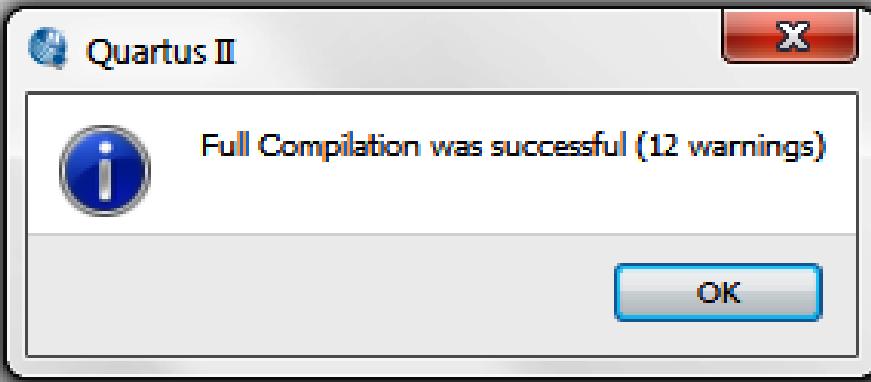
DESIGN PROCESS FOR A SCHEMATIC



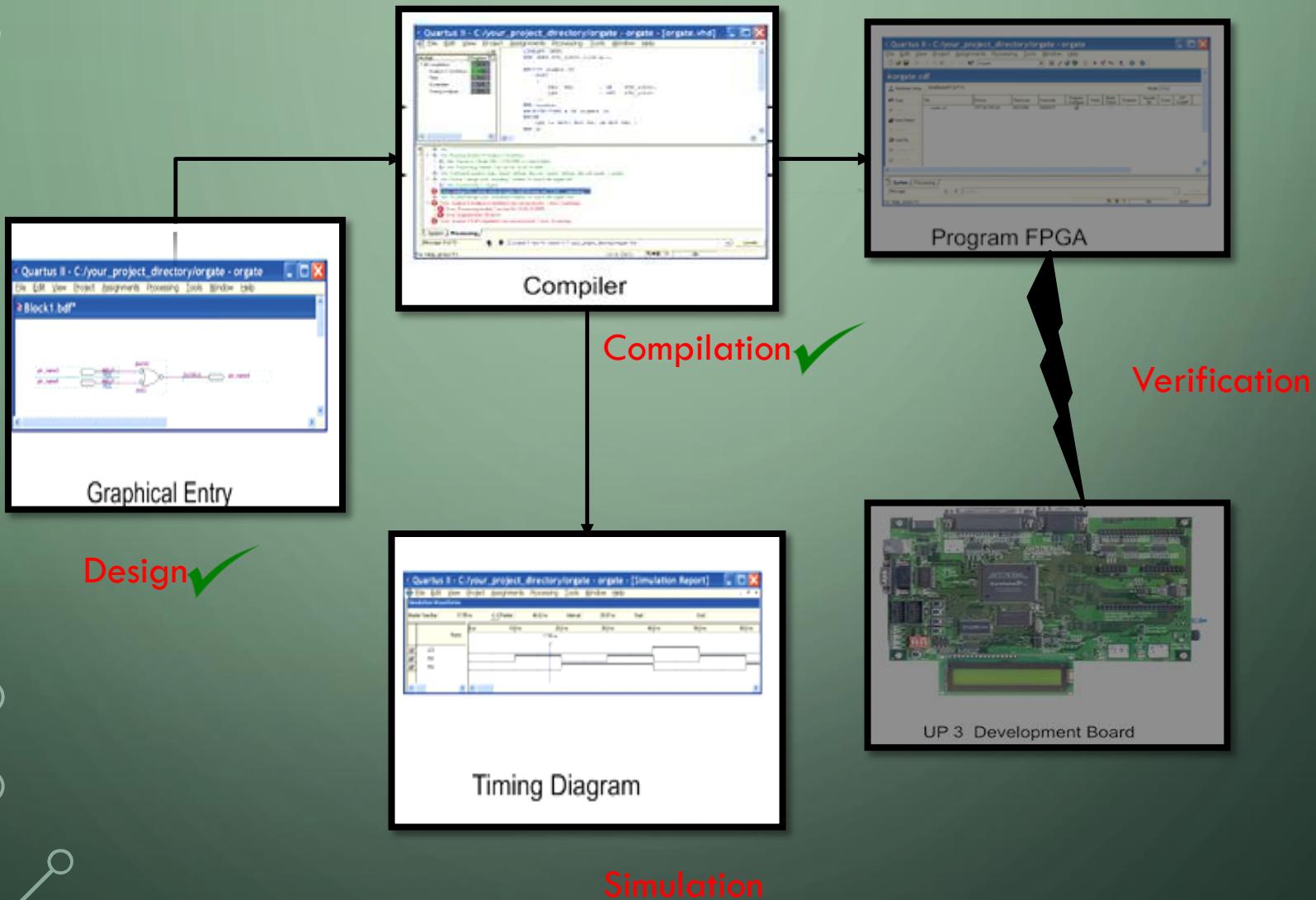
Altera Quartus II 13.0



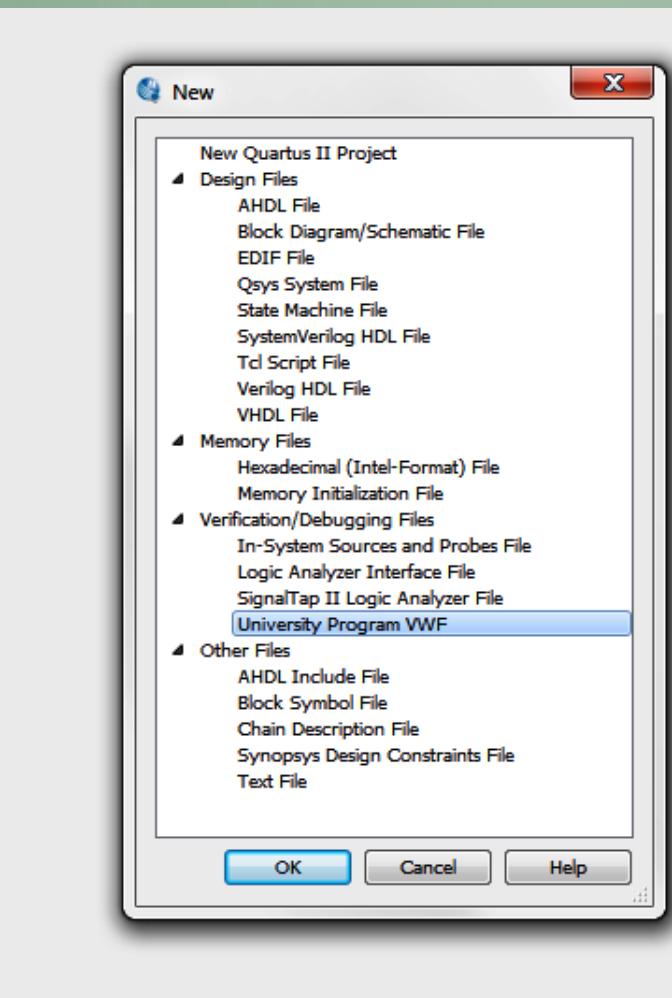
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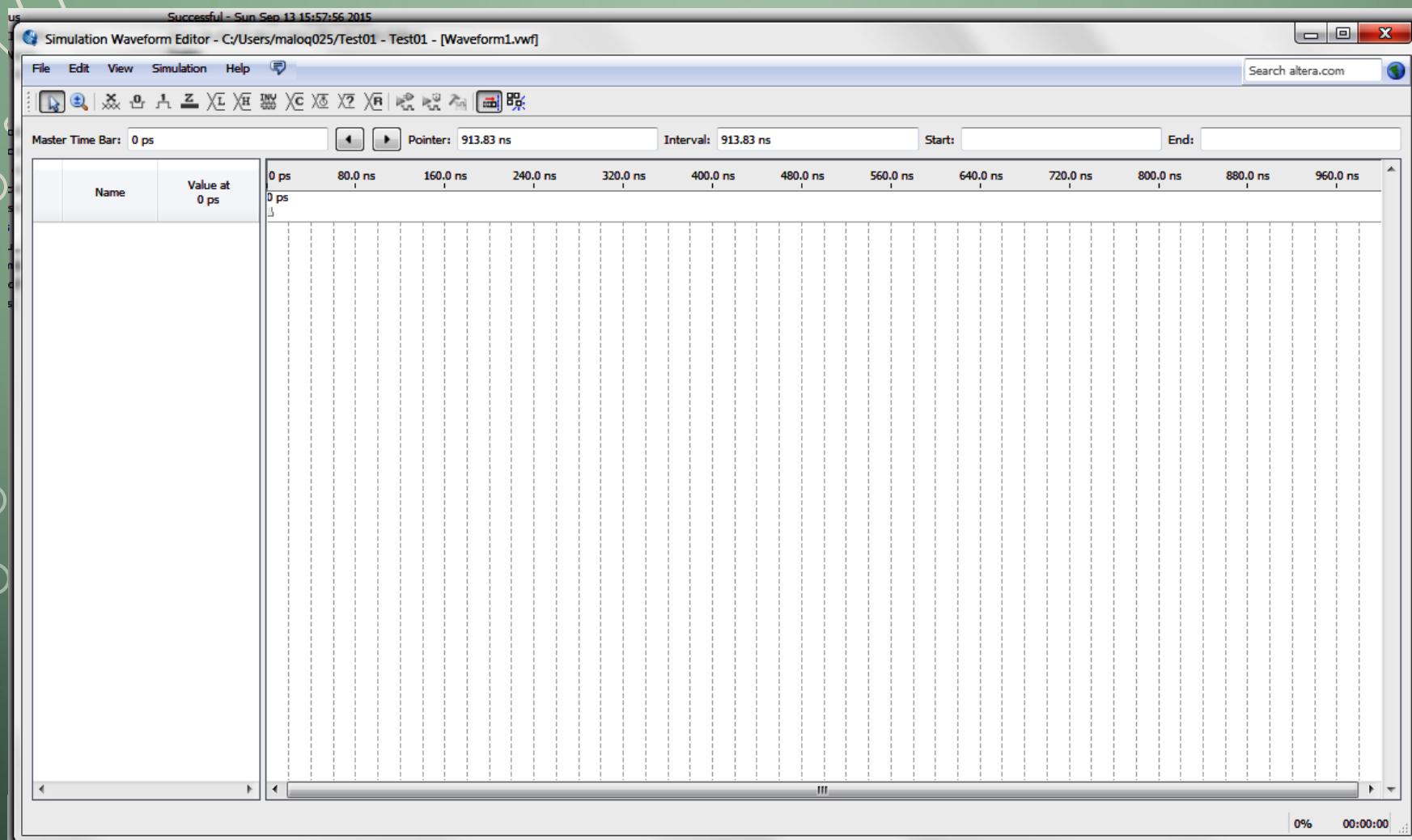
DESIGN PROCESS FOR A SCHEMATIC



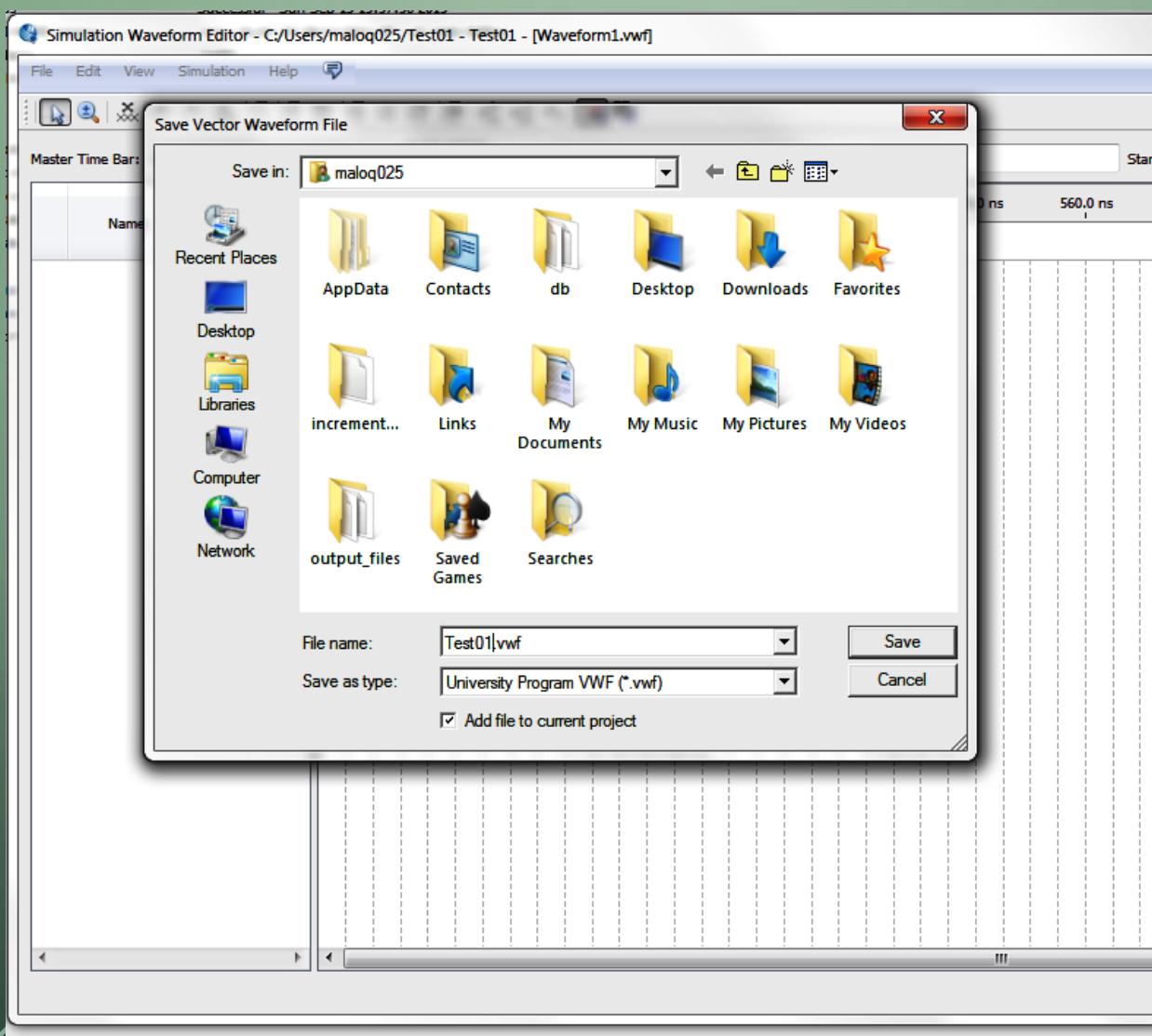
Altera Quartus II 13.0



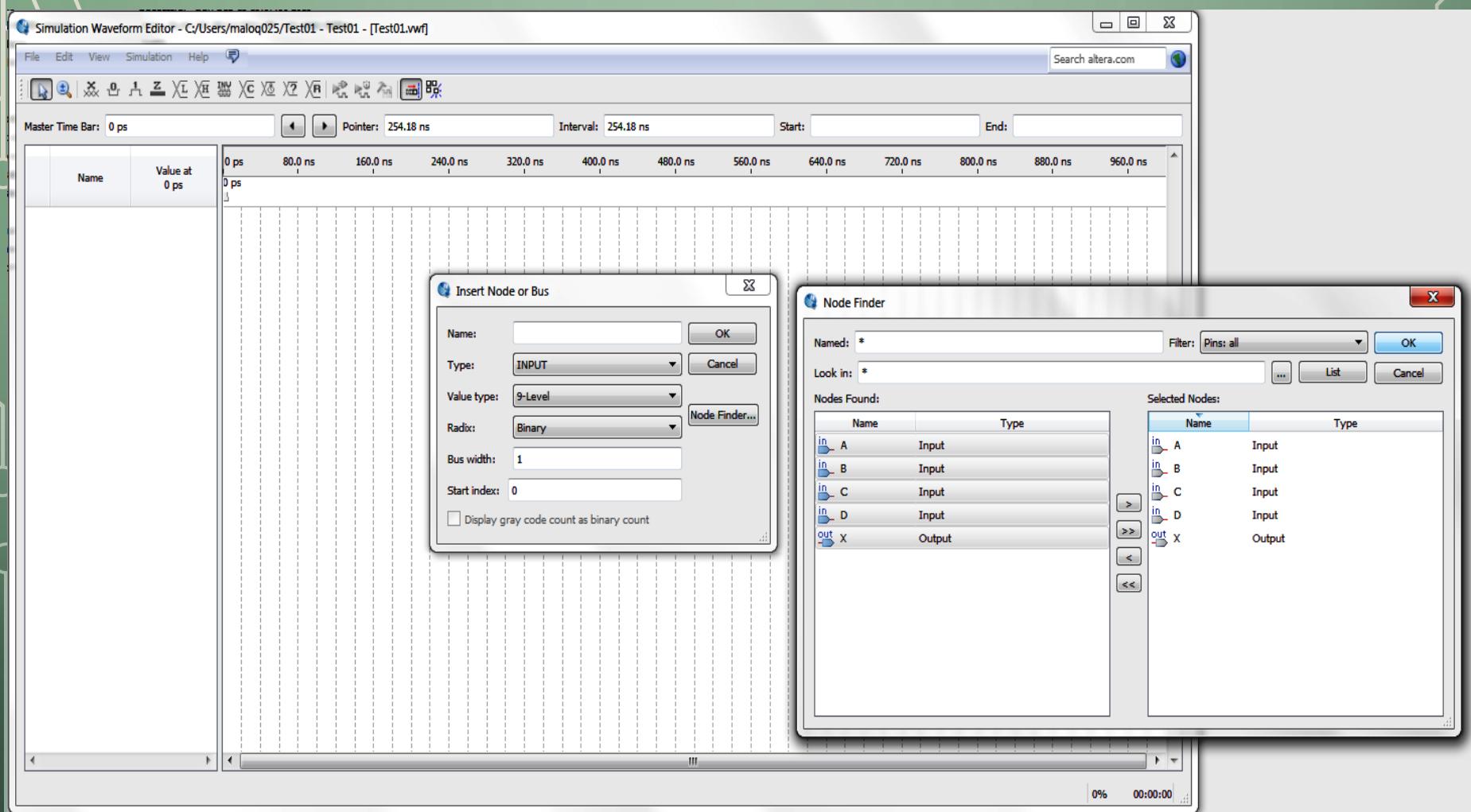
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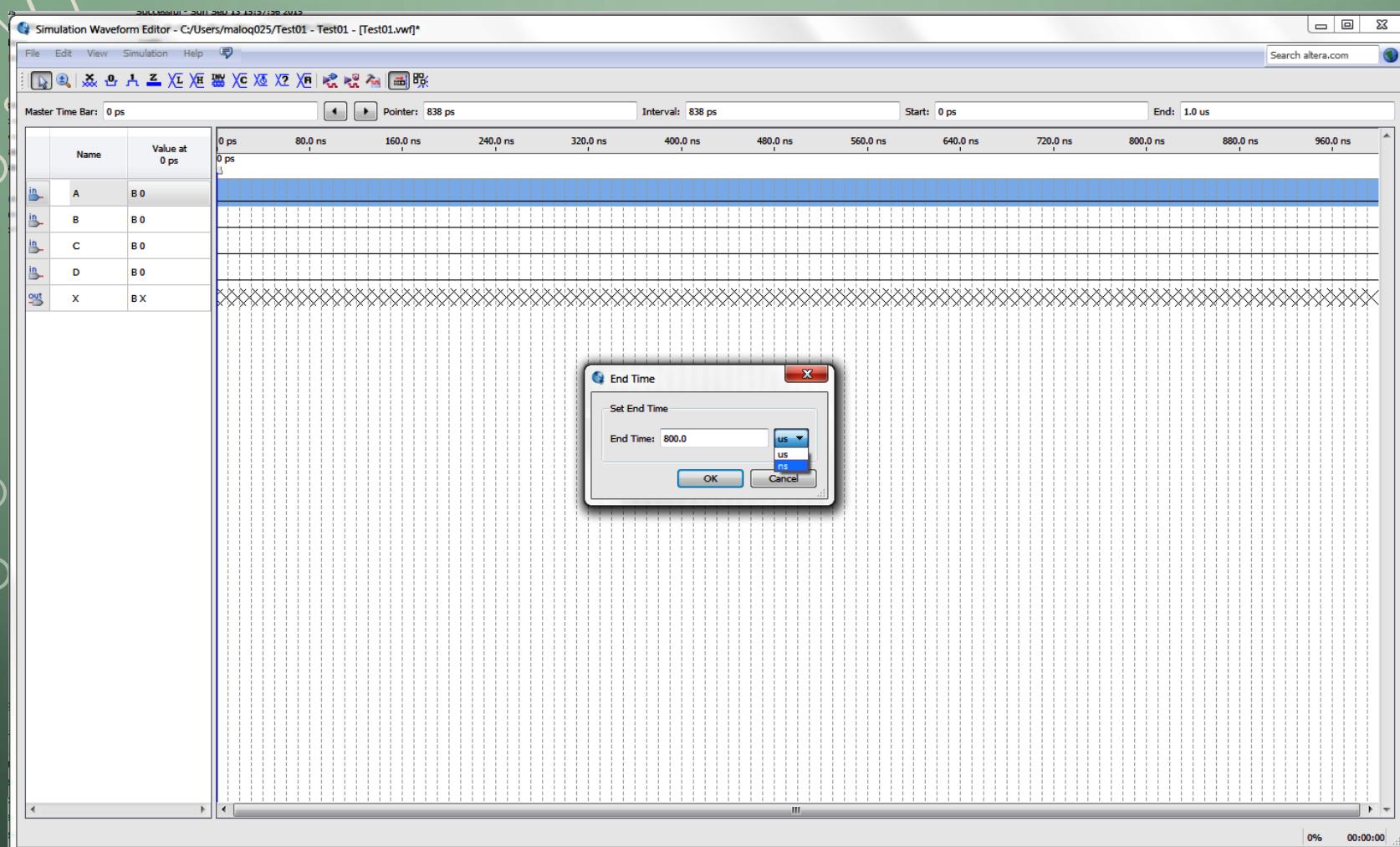
Altera Quartus II 13.0



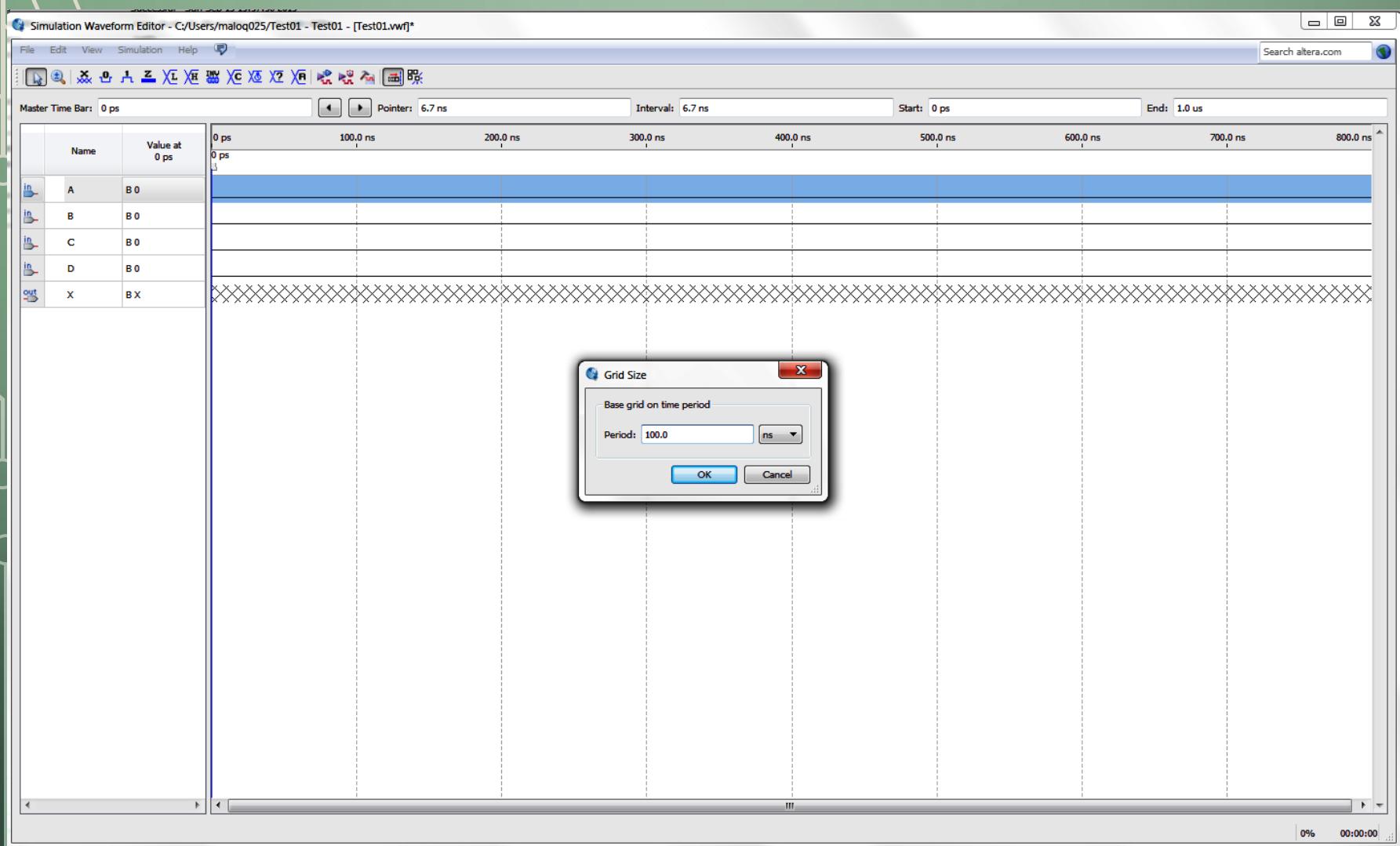
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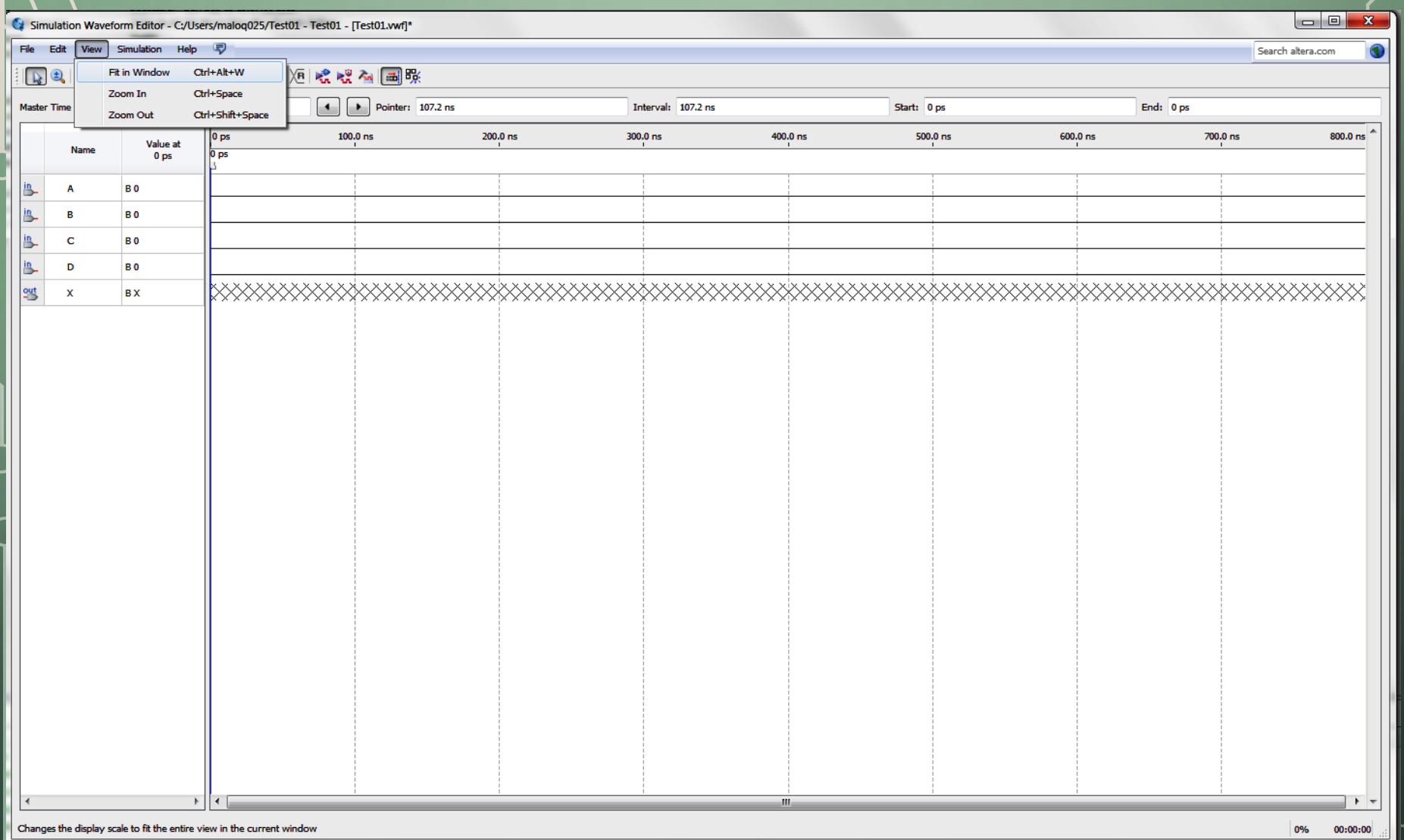
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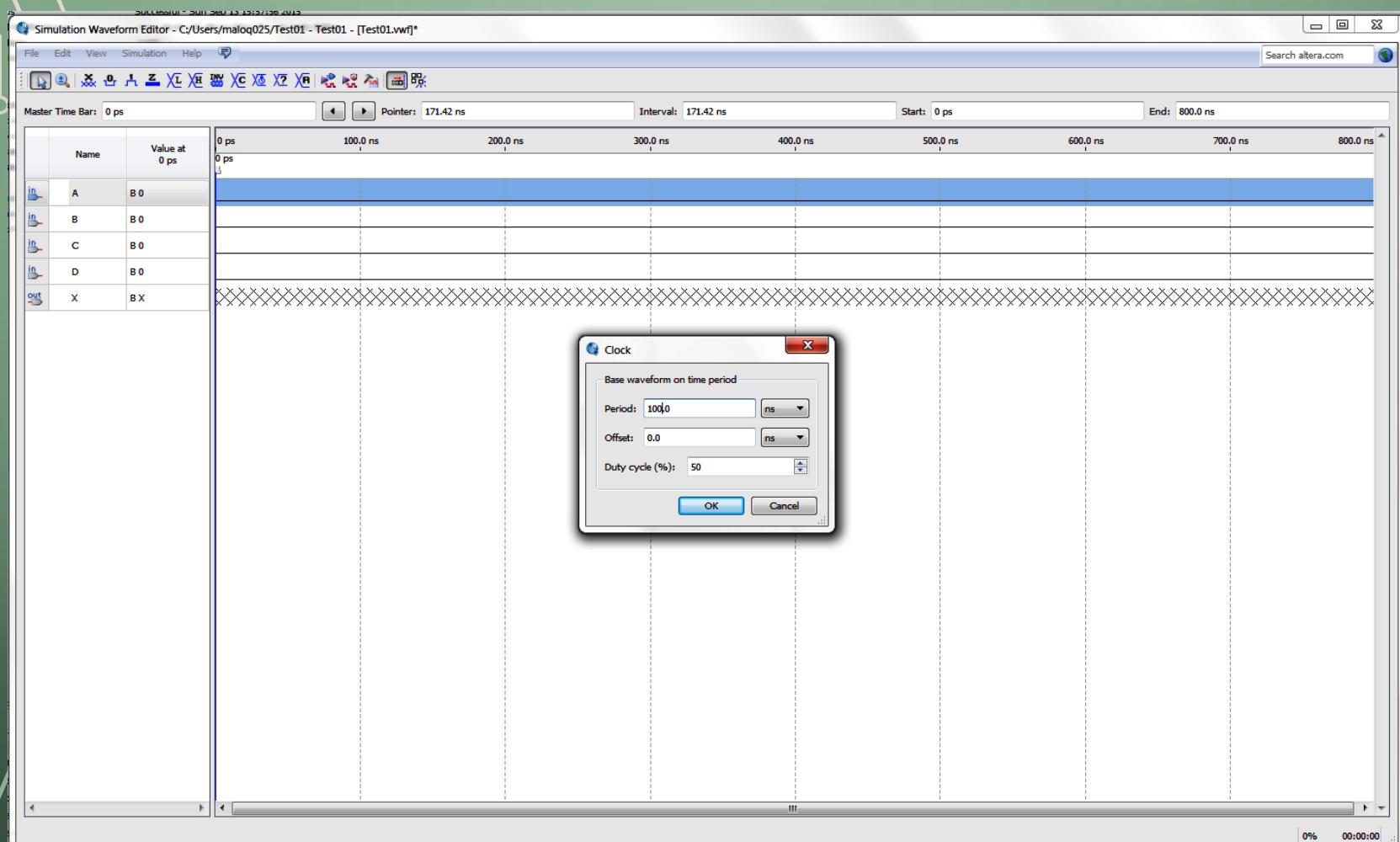
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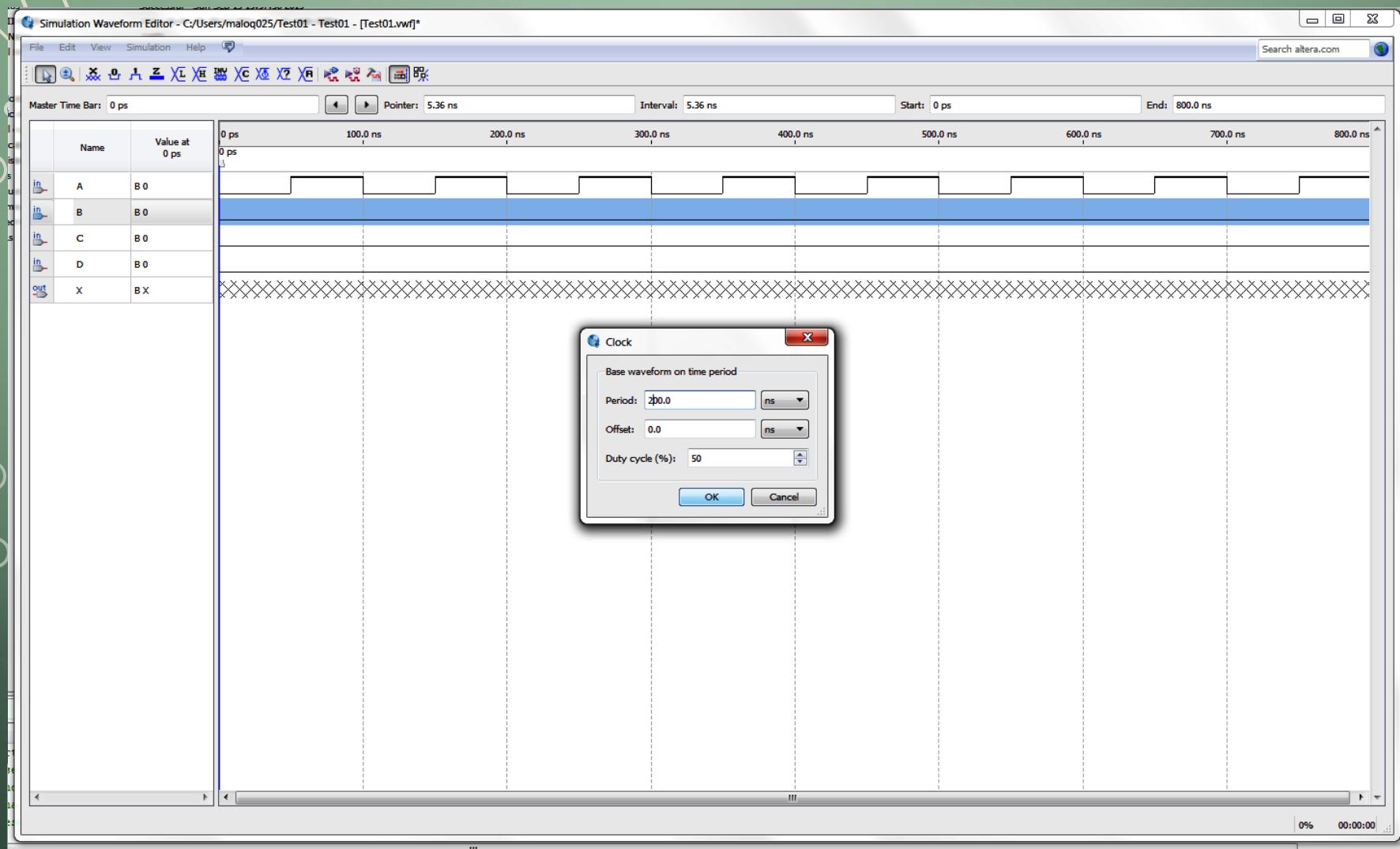
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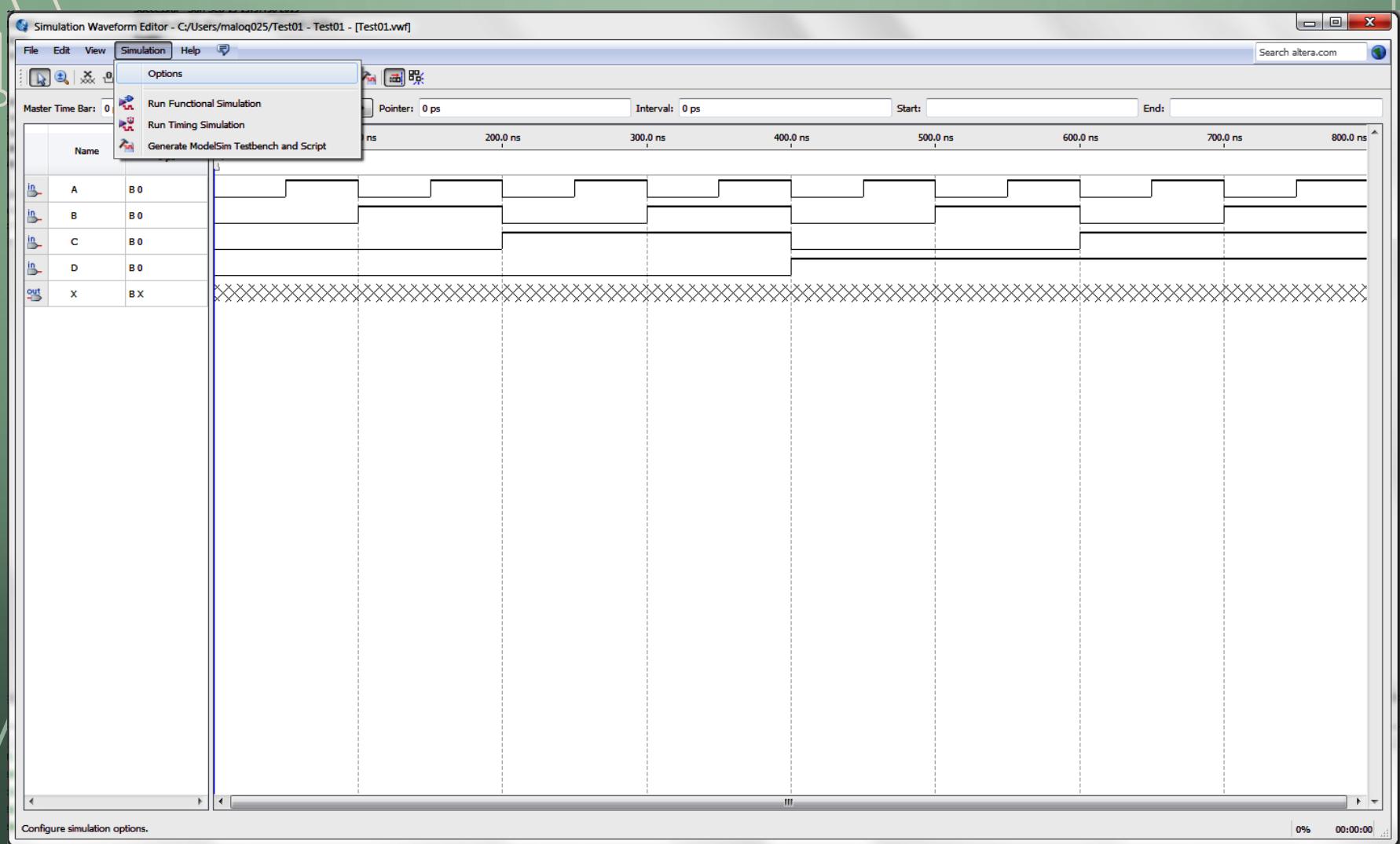
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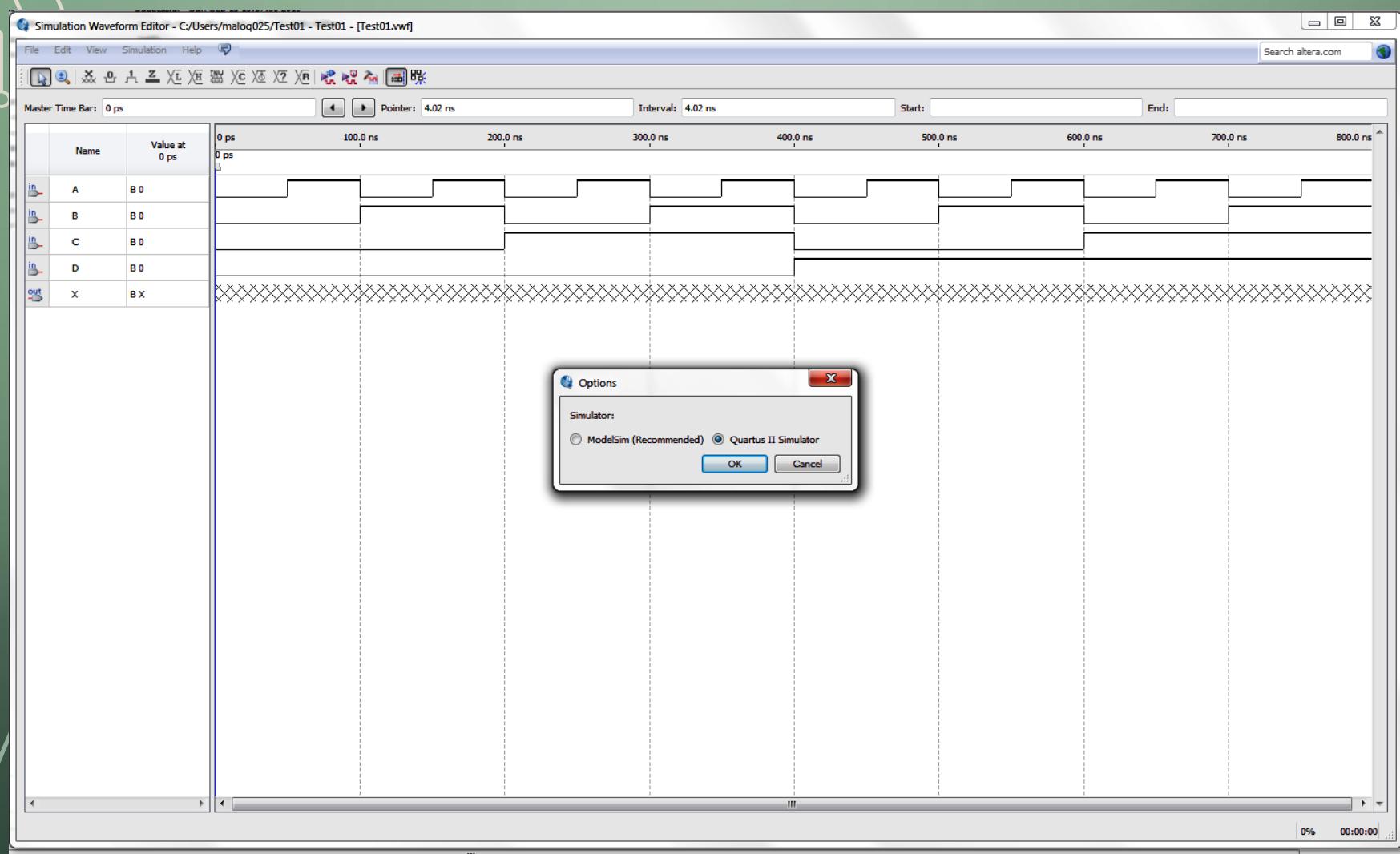
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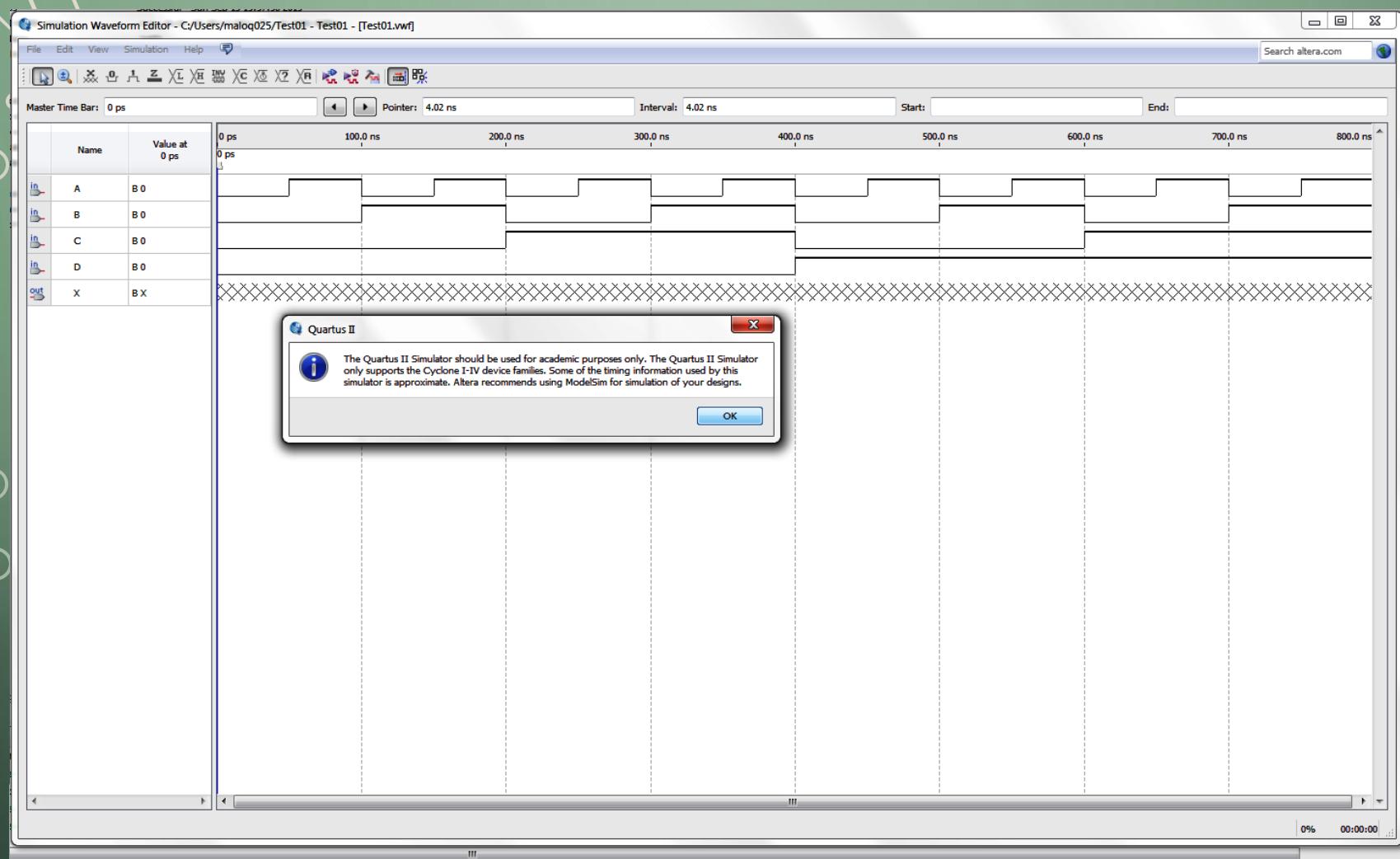
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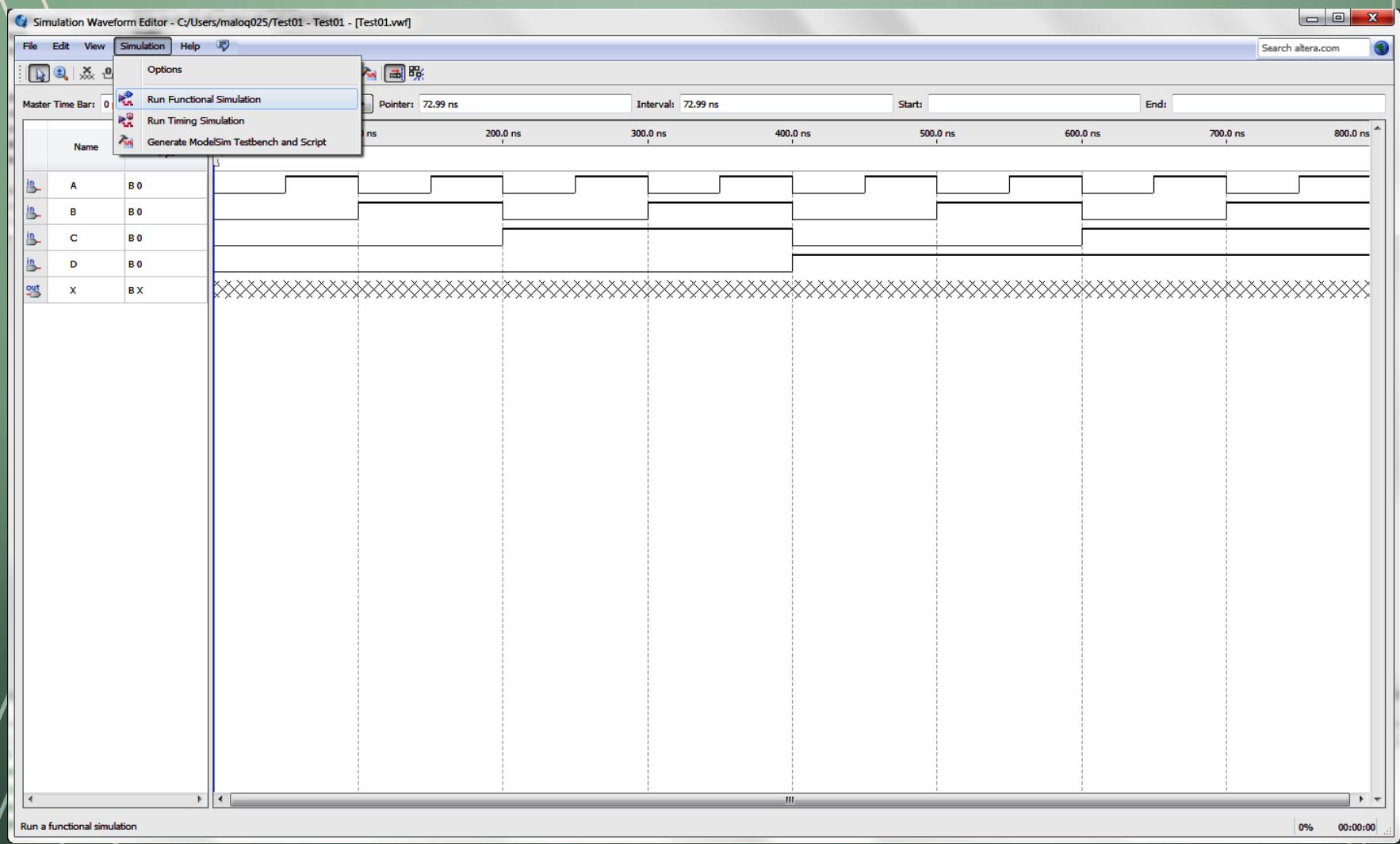
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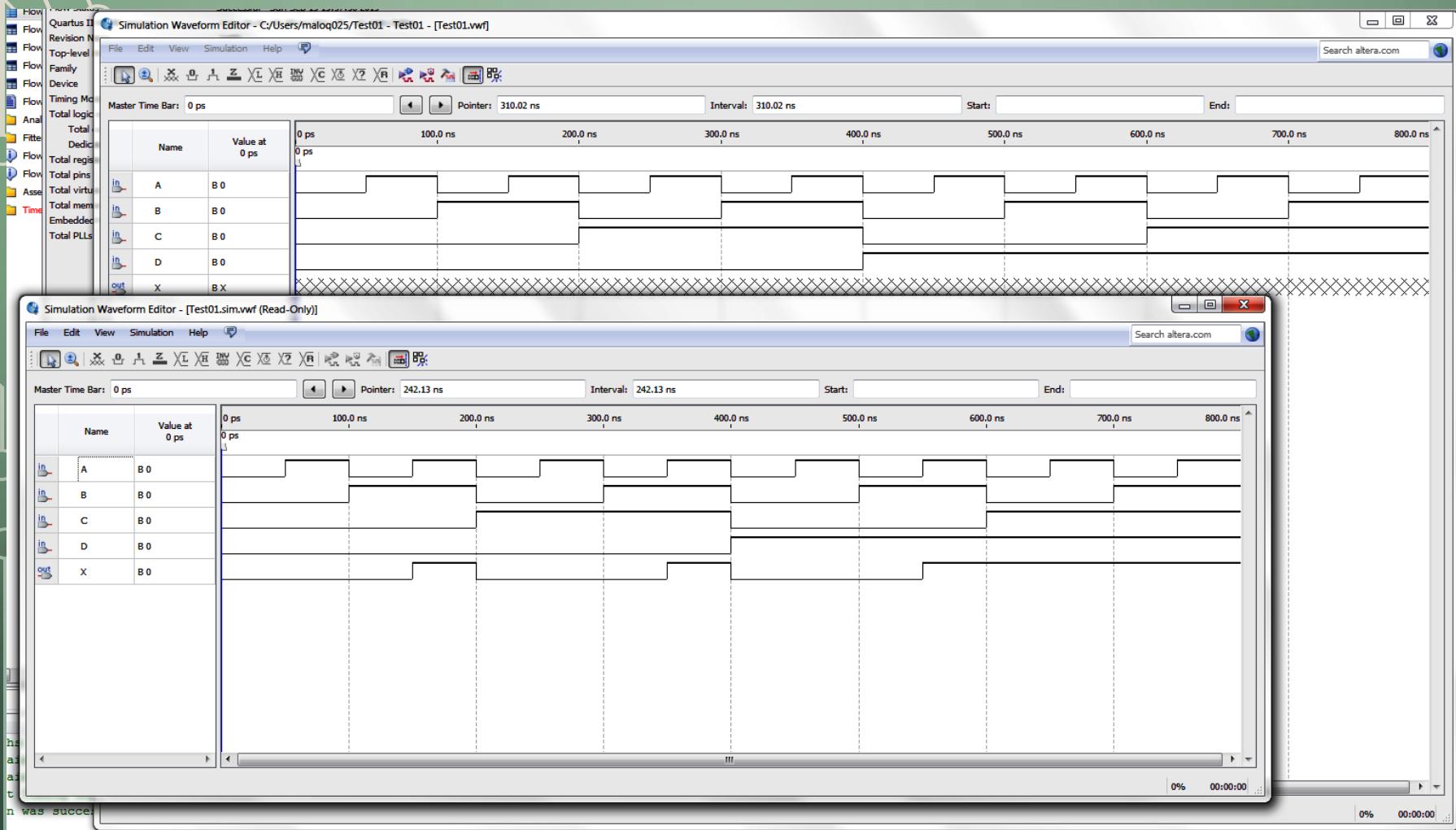
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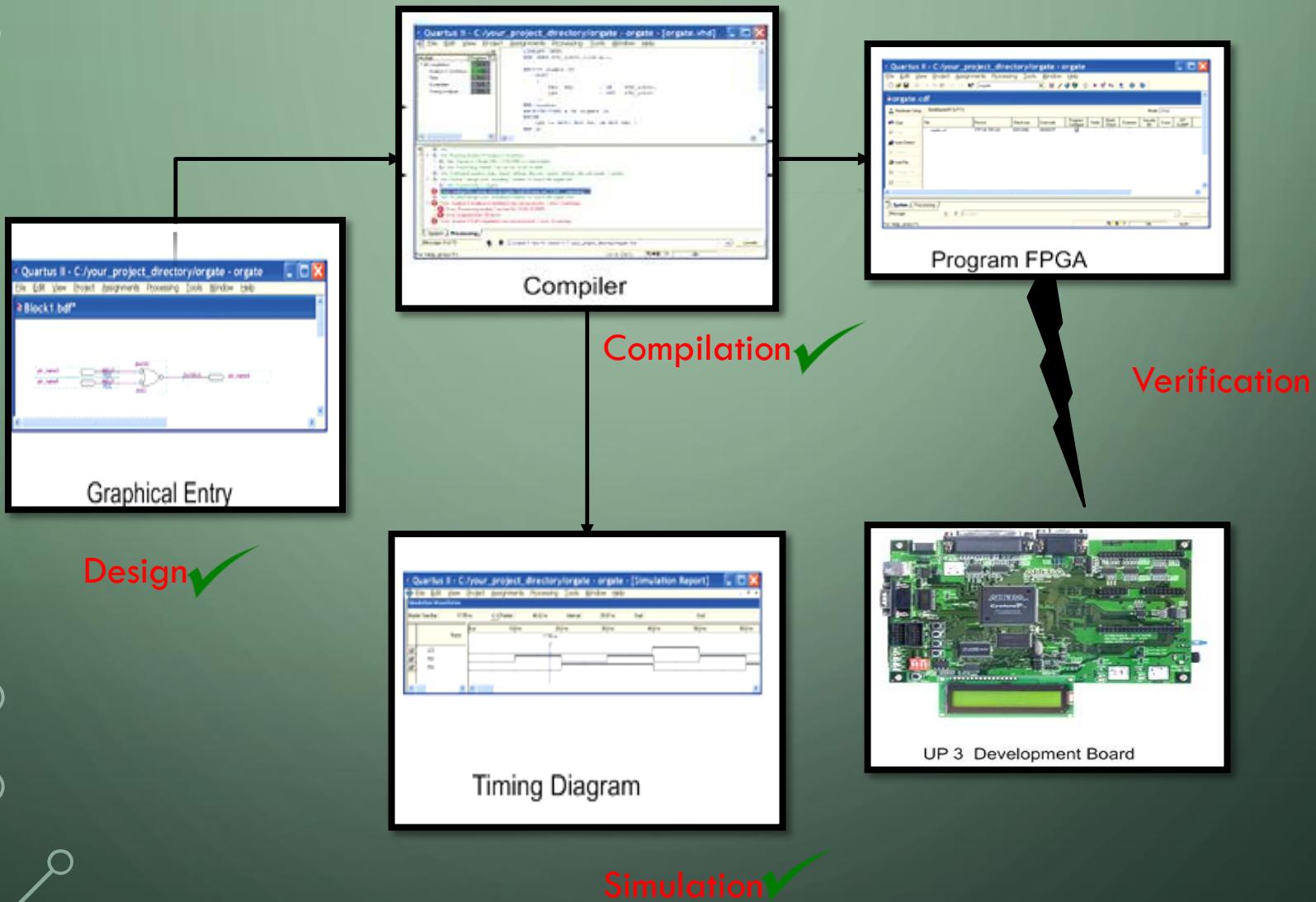
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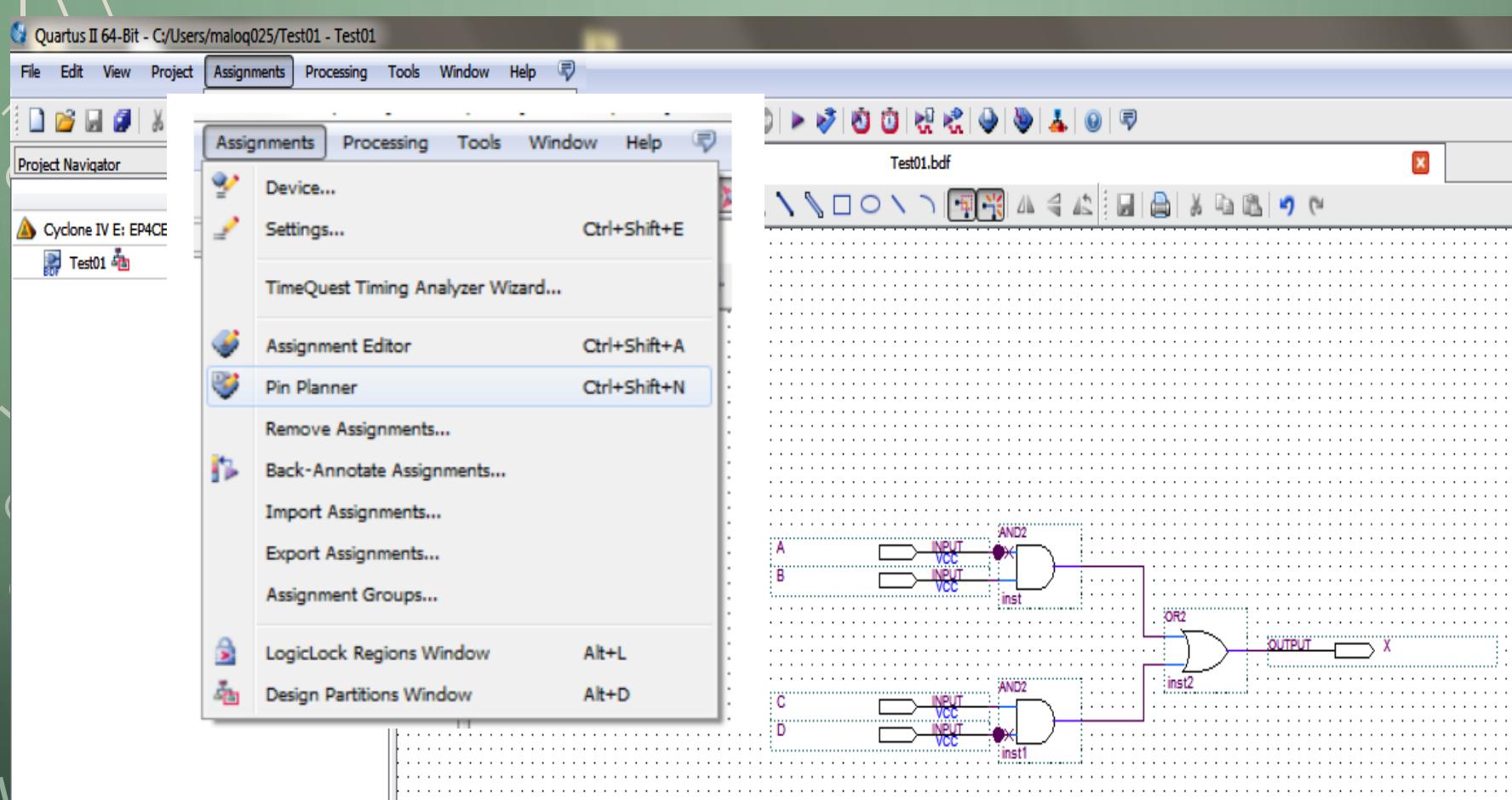
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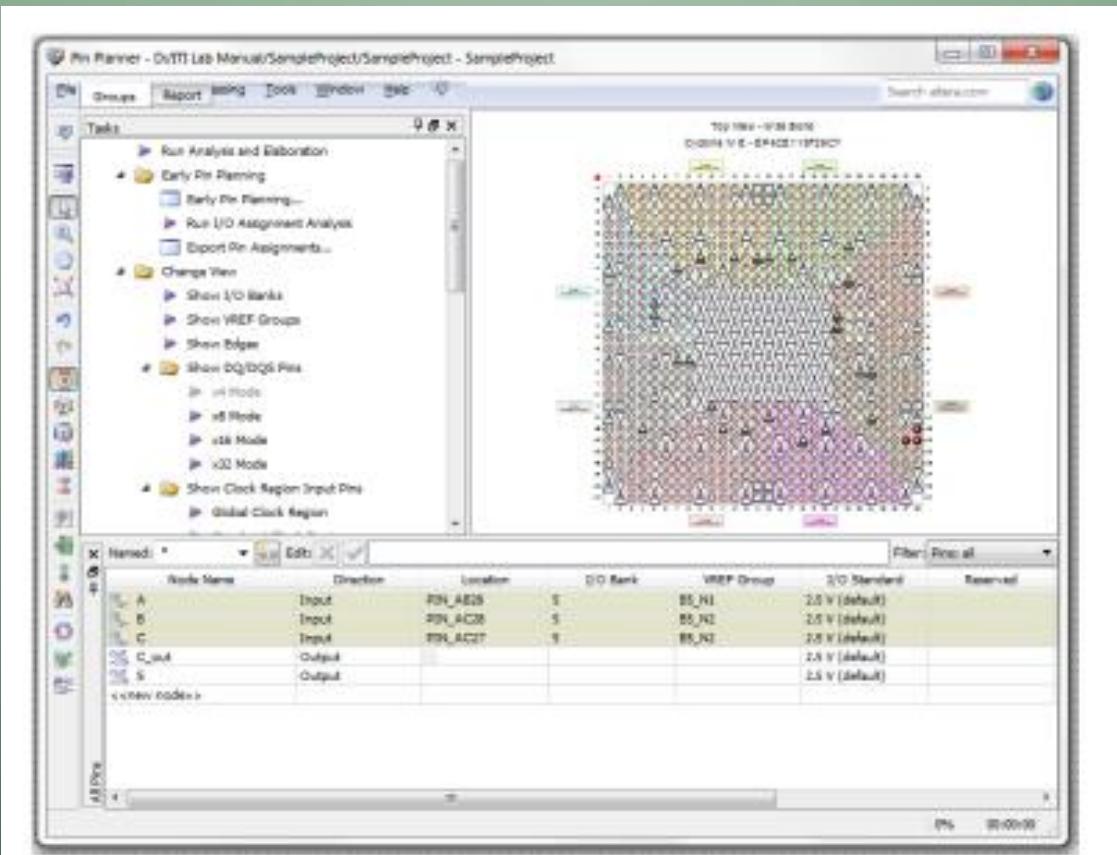
DESIGN PROCESS FOR A SCHEMATIC



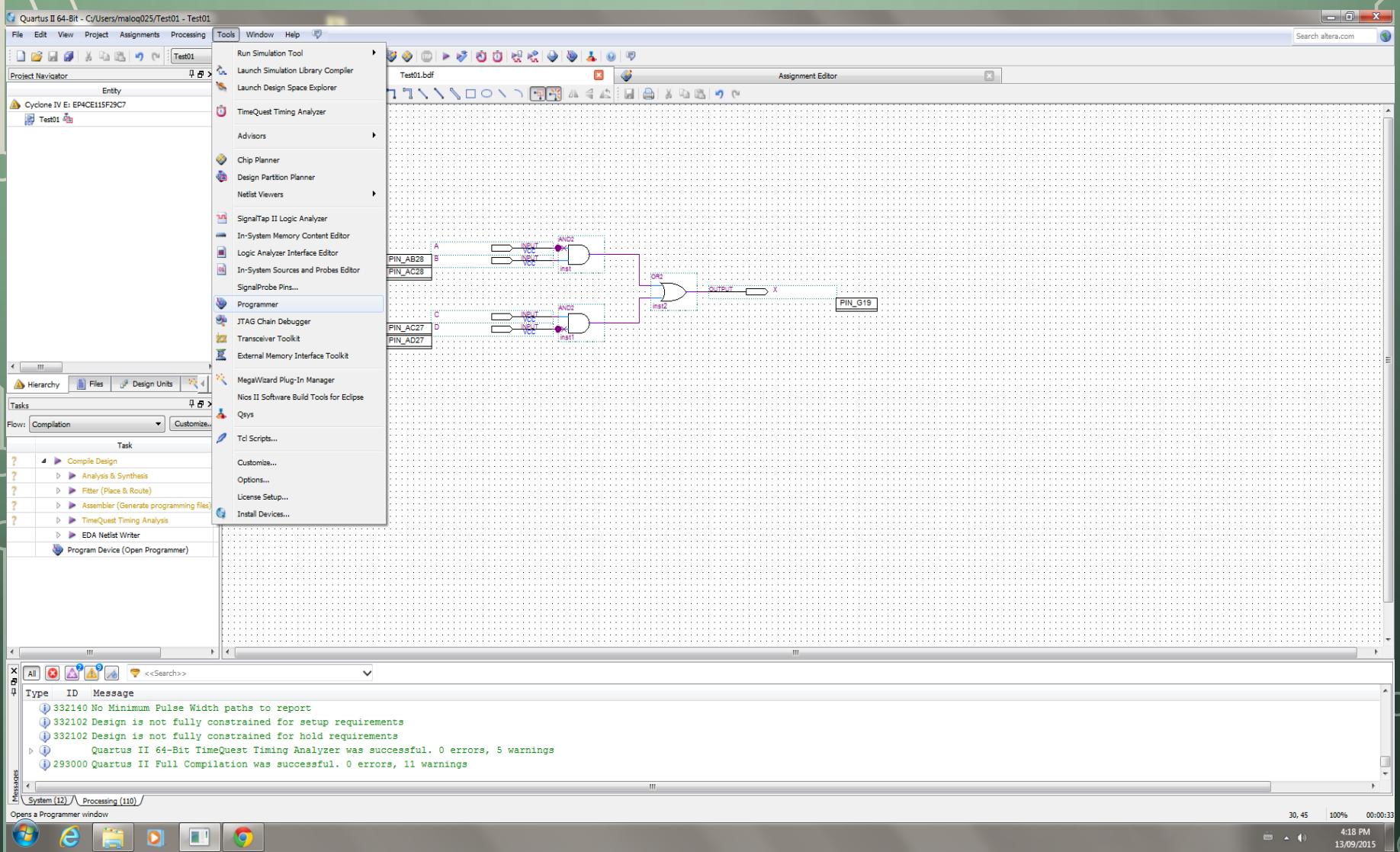
Altera Quartus II 13.0



Altera Quartus II 13.0



Altera Quartus II 13.0



Altera Quartus II 13.0

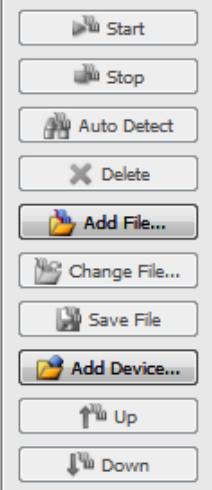
Programmer - C:/Users/maloq025/Test01 - Test01 - [output_files/Test01.cdf]

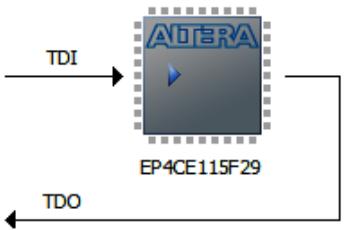
File Edit View Processing Tools Window Help  Search altera.com

Hardware Setup... No Hardware Mode: JTAG Progress:

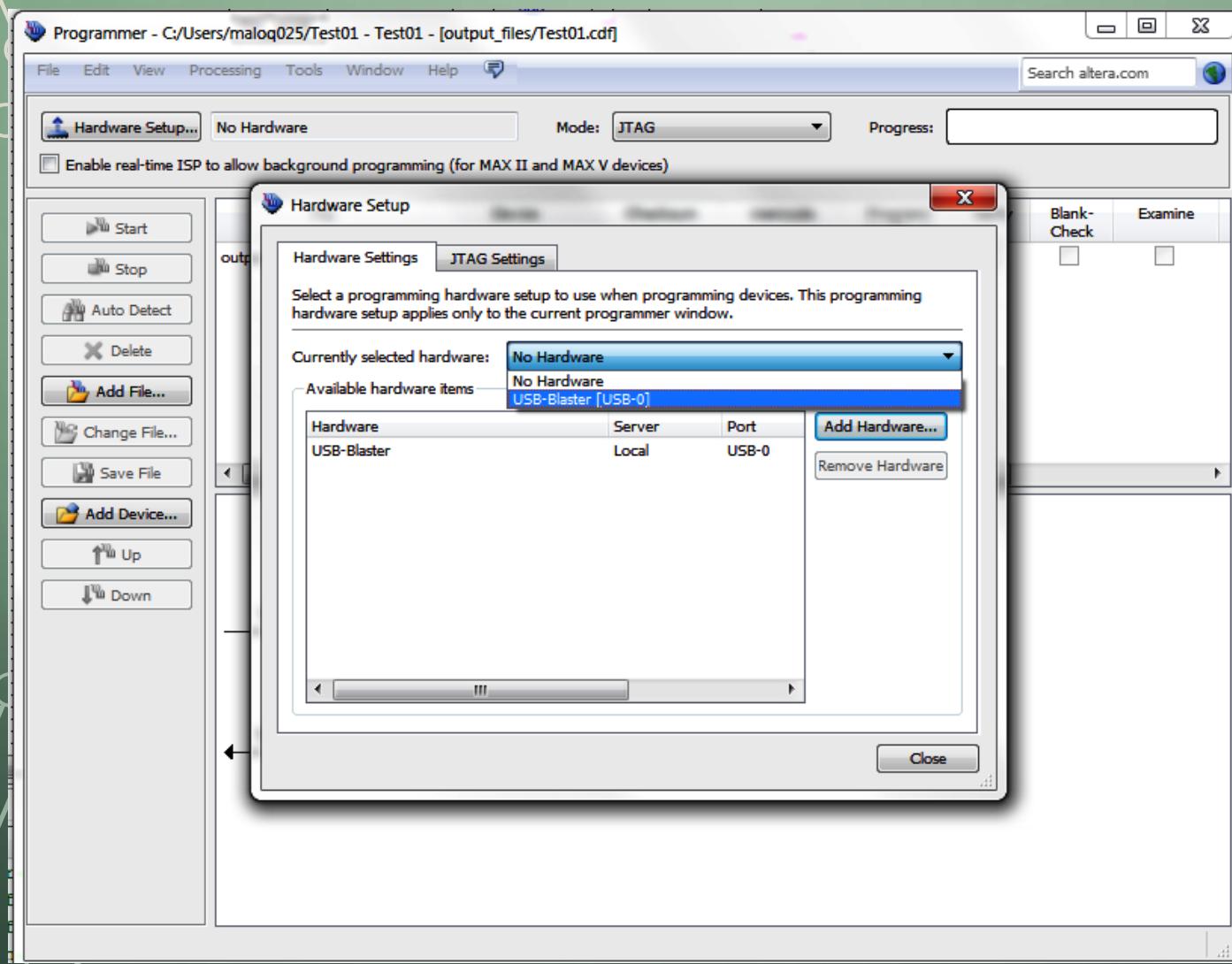
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine
output_files/Test01.sof	EP4CE115F29	005634BF	005634BF	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

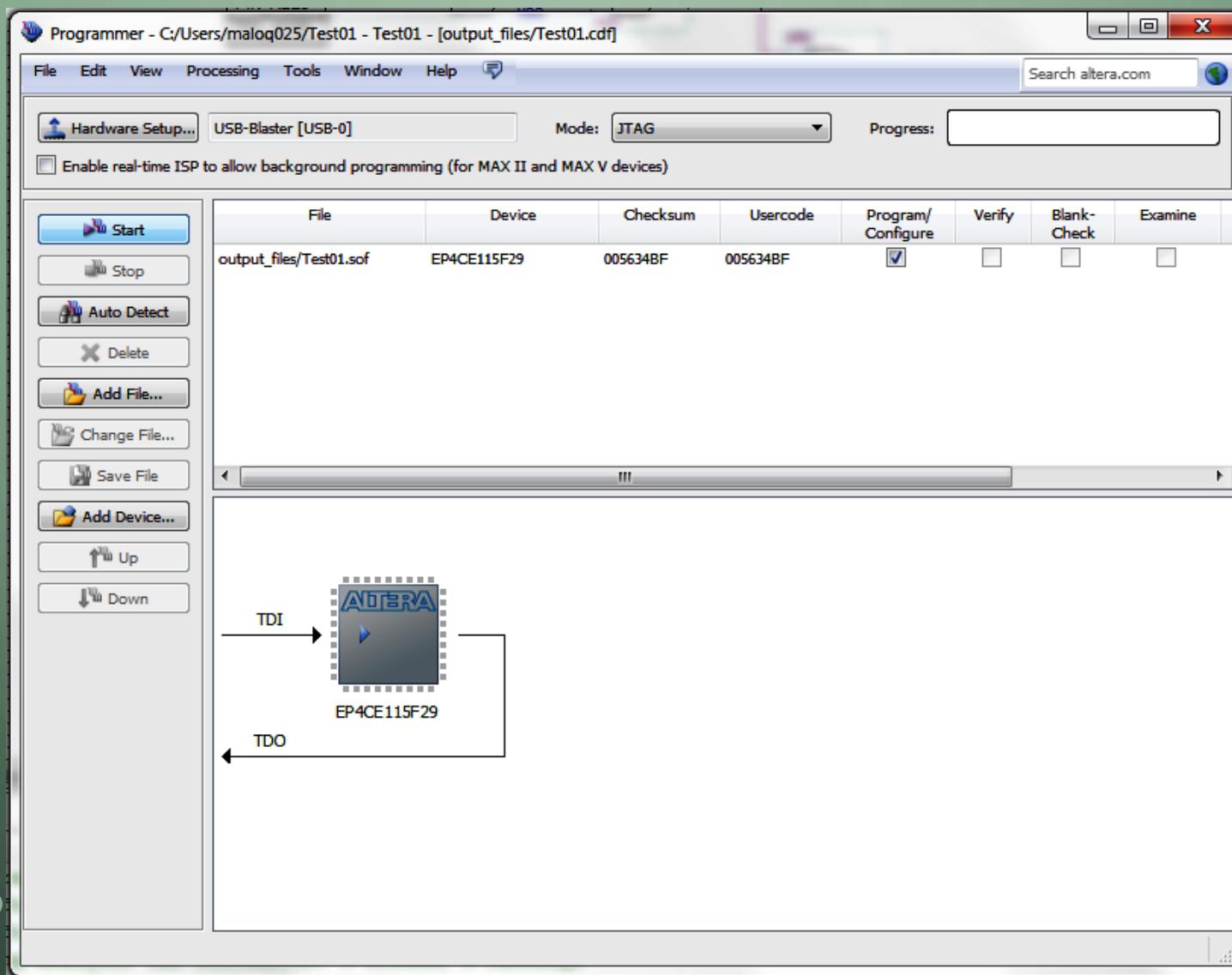




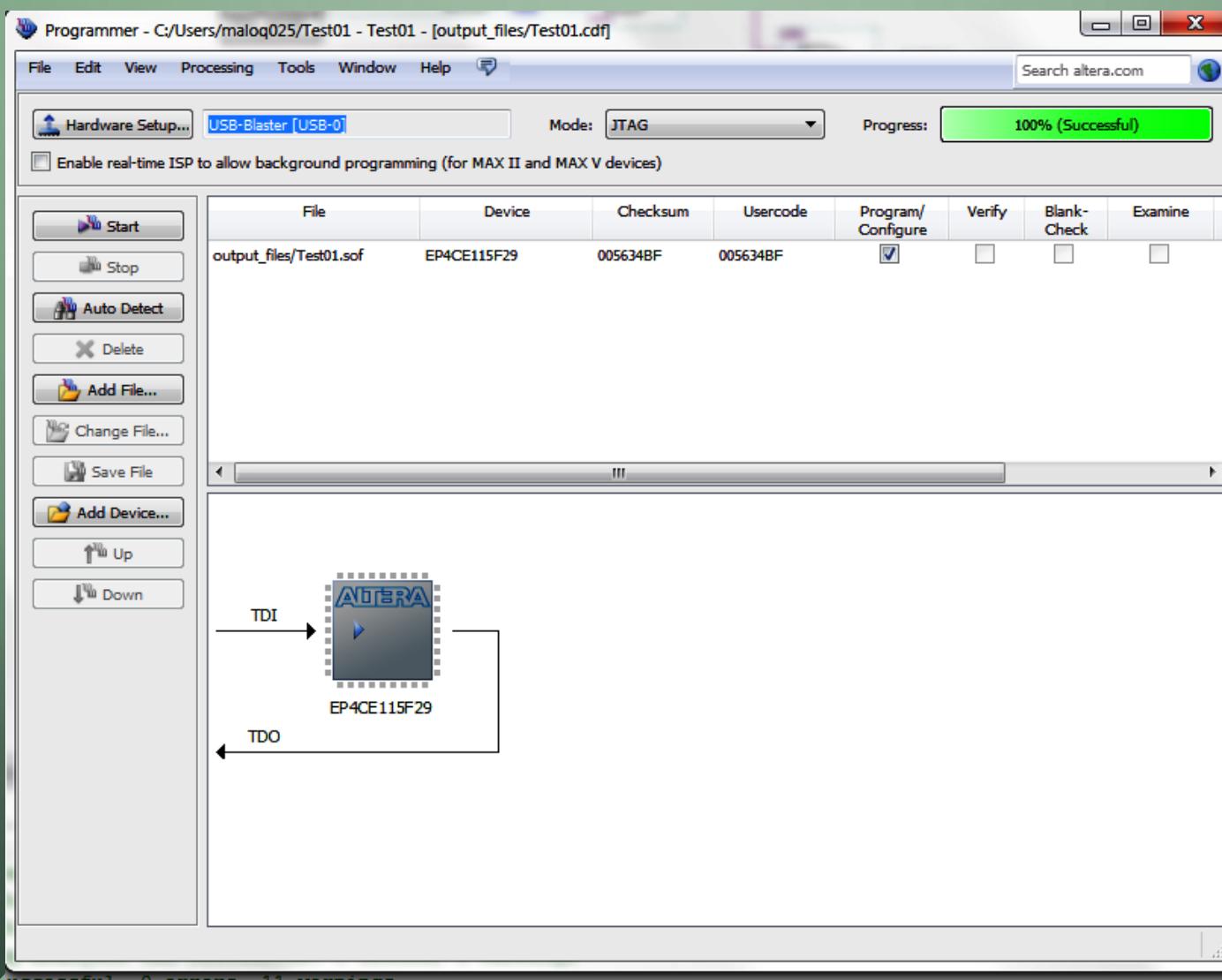
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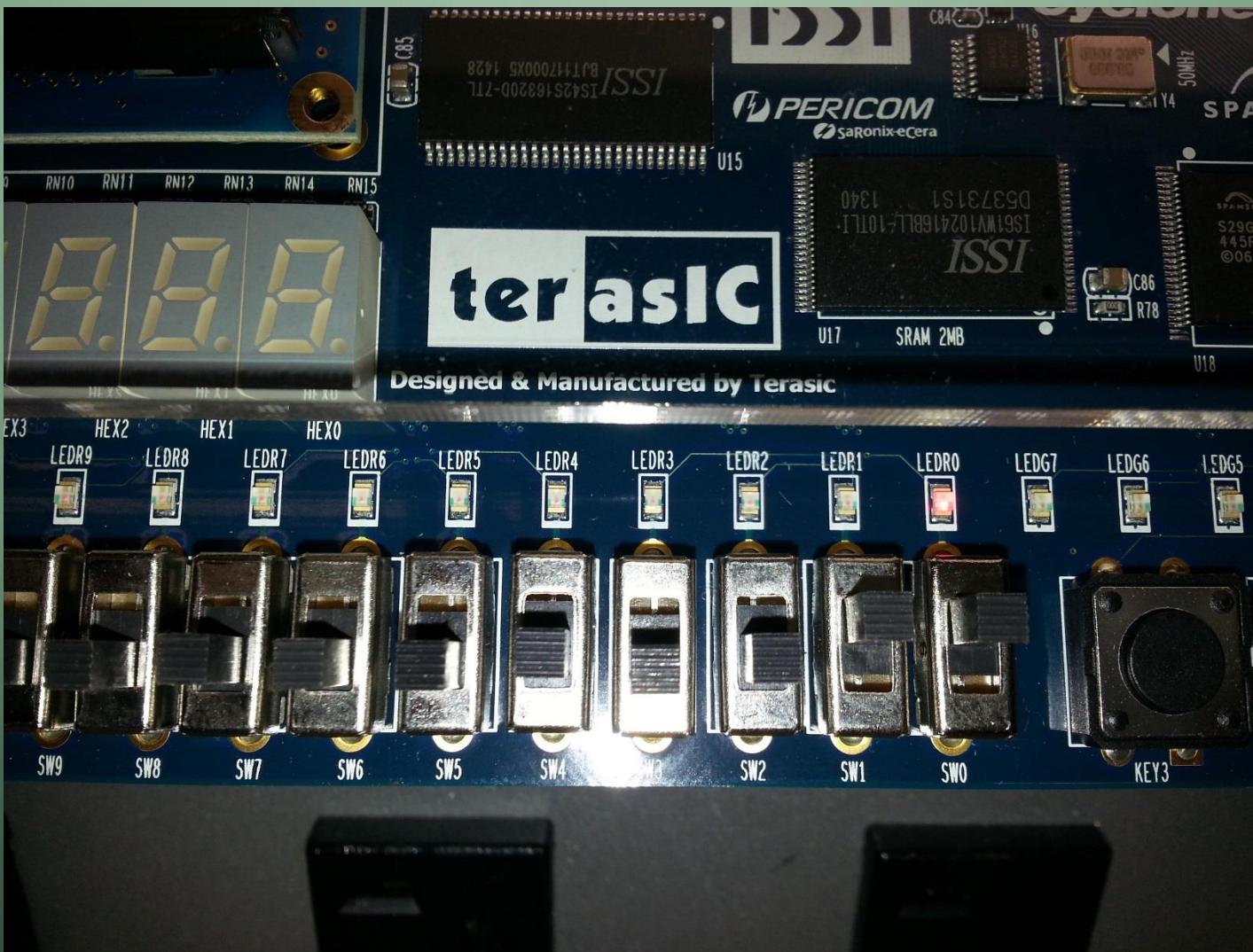
Altera Quartus II 13.0



Altera Quartus II 13.0



Altera Quartus II 13.0



HOW WE EVALUATE YOU ?

MODULES AND MARKS DISTRIBUTION

Lab Grading

Presence, Pre-lab, Design, Simulation and Demonstration

Complete Lab report

50 marks assigned for lab reports can be roughly divided as follows;

Objectives	= 4%
Equipment & Components	= 4%
Circuit Diagrams	= 16%
Experimental Results (Simulation)	= 22%
Comparison of theoretical and experimental	= 30%
Discussion/Conclusion	= 20%
Pre-lab, Completeness and Clarity	= 4%
Total (50 marks)	= 100%

Experiment

= 50 marks

= 50 marks

Report

EXPERIMENT

1 Prelab

Pre-lab preparation consist of:

Answering **ALL** questions of **ALL** preparation sections from **ALL *parts**

Example:

Lab 1 Has two parts

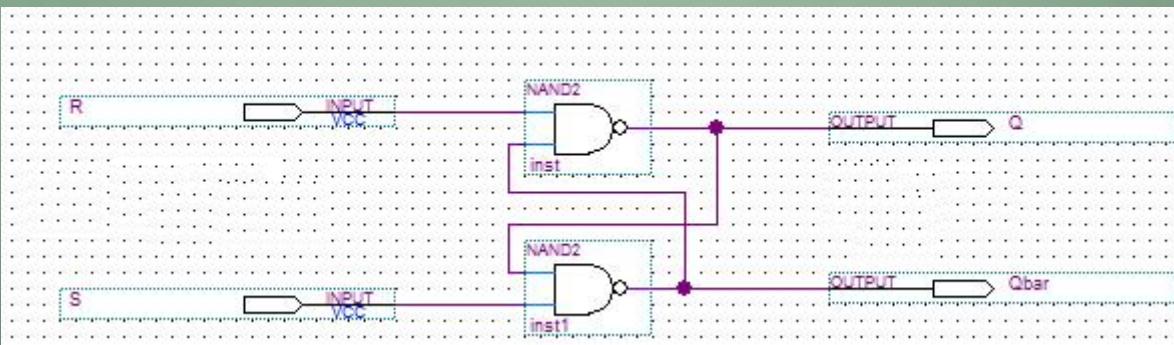
Part I : Two Preparation questions ← 6 points

Part II: Two Preparation questions ← 8 points

*unless TAs mention to do only specific ones.

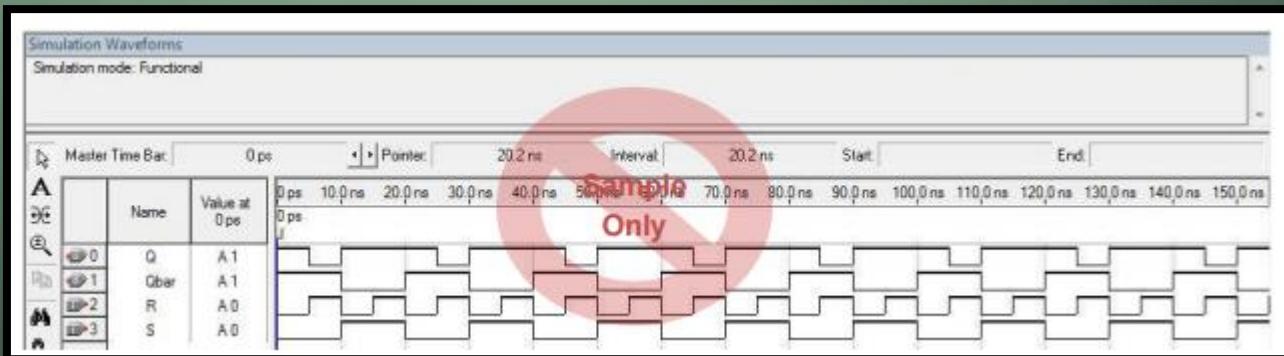
2. Design

Take a screen-shots of your design to include in your lab report.



3. Simulation

- Simulations for all circuits is compulsory unless excluded by TAs
- Make sure you save the simulation results into an accessible location (e.g. T drive).
- Also, take the **screen-shots** of the simulation result, to be include in the lab report.



A sample simulation result waveform

4. Demonstration and Verification

- Once circuit designs are simulated to verify their accuracy, students can load them into DE2 board to demonstrate
- Check that the circuit generate expected results by comparing with theoretical results
- All group members must be capable of explaining results to TAs to get full marks

Note: No explanation → less marks

- Make sure a TA check your work and enter experiment marks 15 mins before the end of the lab

DIVISION OF EXPERIMENT MARKS

- TA's MARKS SHEET

LABORATORY REPORT FORMAT

LABORATORY REPORT FORMAT

Lab #: Lab Title

ITI 1100 A/D - Digital Systems

Fall 2016

**School of Electrical Engineering and Computer Science
University of Ottawa**

Course Coordinator: Dr. Ahmed Karmouch

Teaching Assistants: TA 1 Name
TA 2 Name

Group #

Student Name and number #
Student Name and number #

Experiment Date:
Submission Date:

LABORATORY REPORT FORMAT

Objectives (2 marks*)

- Use point form with bullets
- State main objectives and sub objectives
- State laws/theorems verified if any

Equipment & Components (2 marks*)

- List all main instruments, tools, software and other components used
- Include their model/type
- Quartus II Student Edition Software
- Altera UP-1 circuit board
- Wire strippers etc...

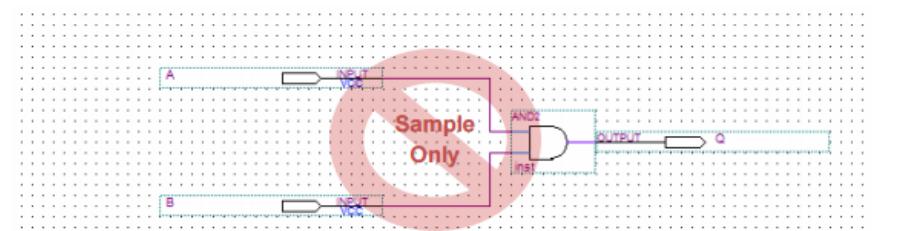
Circuit Diagrams (2 ~ 8 marks*)

- Include screen-shots of schematic design diagrams which shows all gates and other components with pin names clearly
- Clearly specify to which part or section the figure is belong to, by following same title/sub-title structure used in lab manual.
- Clearly Name and number Circuit Diagrams

Example:

Part I – Combinational Logic Circuits Construction

One Chip Logic Circuit



LABORATORY REPORT FORMAT

Experimental Data and Data Processing (4 ~ 10 marks*)

- Include Screen-shots of simulation **outputs**. If you only include screen-shots of input waveform diagrams without simulation output, marks will not be given
- Tabulate observed experimental results
- Perform calculations using observed/measured data to obtain comparable results if necessary.
i.e. some observed results might need further processing before comparing with theoretical results.
- Specify to which part or section screen-shots, calculations and tables are belong to) by following same title/sub-title structure used in lab manual.
- Present experimental data in the same order as the procedure

Part I – Combinational Logic Circuits Construction

One Chip Logic Circuit

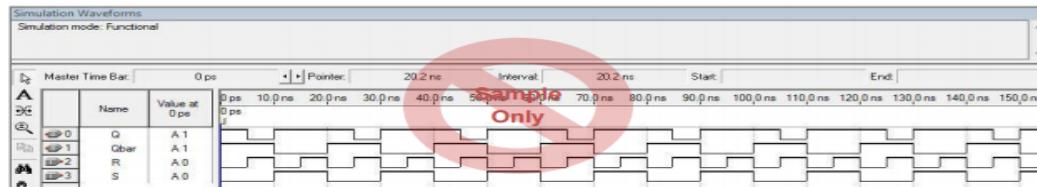


Table 1 : Experimental data observed from MAX 7000 circuit board**

Input given from dip switches		Observed Output from LED's
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

LABORATORY REPORT FORMAT

Comparison of Theoretical Data and Experimental Data

(12 ~ 20 marks*)

- Perform a side-by-side comparison of expected and experimental data in tables
- Highlight important observations (if any), used in result analysis and comparison.
- Highlight major deviations of observed results (if any) from theoretical
- Include calculations used for result analysis and comparison if necessary
- Explain briefly about compared and analyzed results

Part I – Combinational Logic Circuits Construction

One Chip Logic Circuit

Table 2 : Comparison of Theoretical and Experimental results for one chip logic circuit**

Inputs		Expected Results	Actual Results
A	B	Q	Q
0	0	0	0
0	1	1 Sample Only	0
1	0	0	0
1	1	1	1

The results observed experimentally for one chip circuit from MAX 7000 FGPA were identical to results obtained theoretically as expected.

LABORATORY REPORT FORMAT

Discussion & Conclusions (10 marks)

- Discuss objectives and experiment methodology in brief
- Discuss matching of expected and experimental data in general and state what laws have been verified, what sub-objectives have been met
- Try to give logical explanation for major deviations of results (if any) and discuss problems you faced and solutions used to overcome them.

Appendix (Pre-Lab) (2 marks)

- Attach clearly written pre-lab with correct order of pages

THE STUDENTS DUTIES

- Students are expected to work on their tasks during the labs in a group of two.
- Attendance shall be taken for all Labs.
- Students shall be prepared upon arrival at the lab sessions. Pre-lab of each section will be taken per-group.
 - If a group member is not shown, a ZERO mark will count.
 - Students need to know the logic/theory behind the pre-lab questions.
- Students shall submit one lab report per team.



Thank You

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