



1. Description

1.1. Project

Project Name	blinky
Board Name	custom
Generated with:	STM32CubeMX 6.10.0
Date	01/08/2024

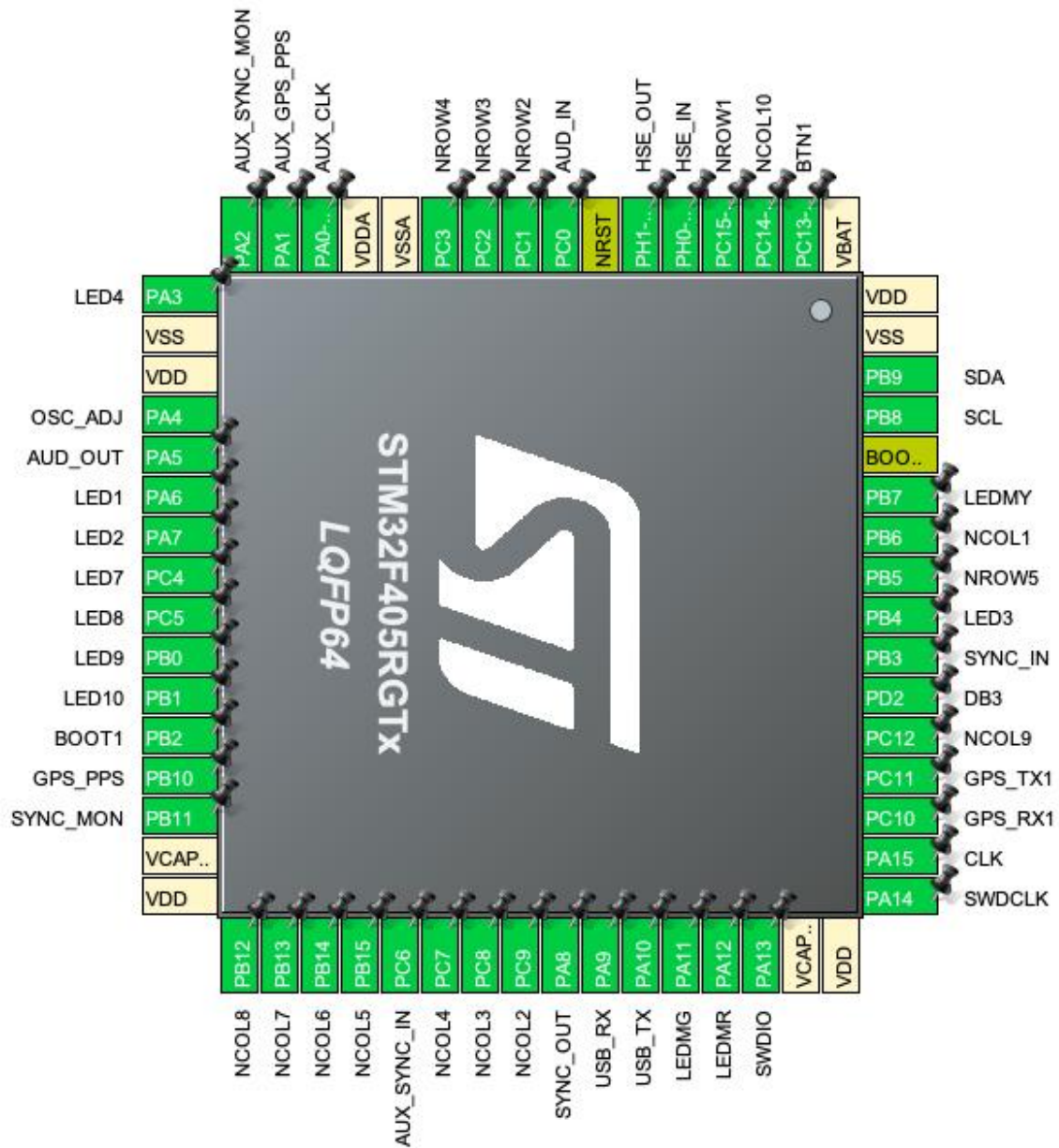
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F405/415
MCU name	STM32F405RGTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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2. Pinout Configuration



(Rotated +90°)

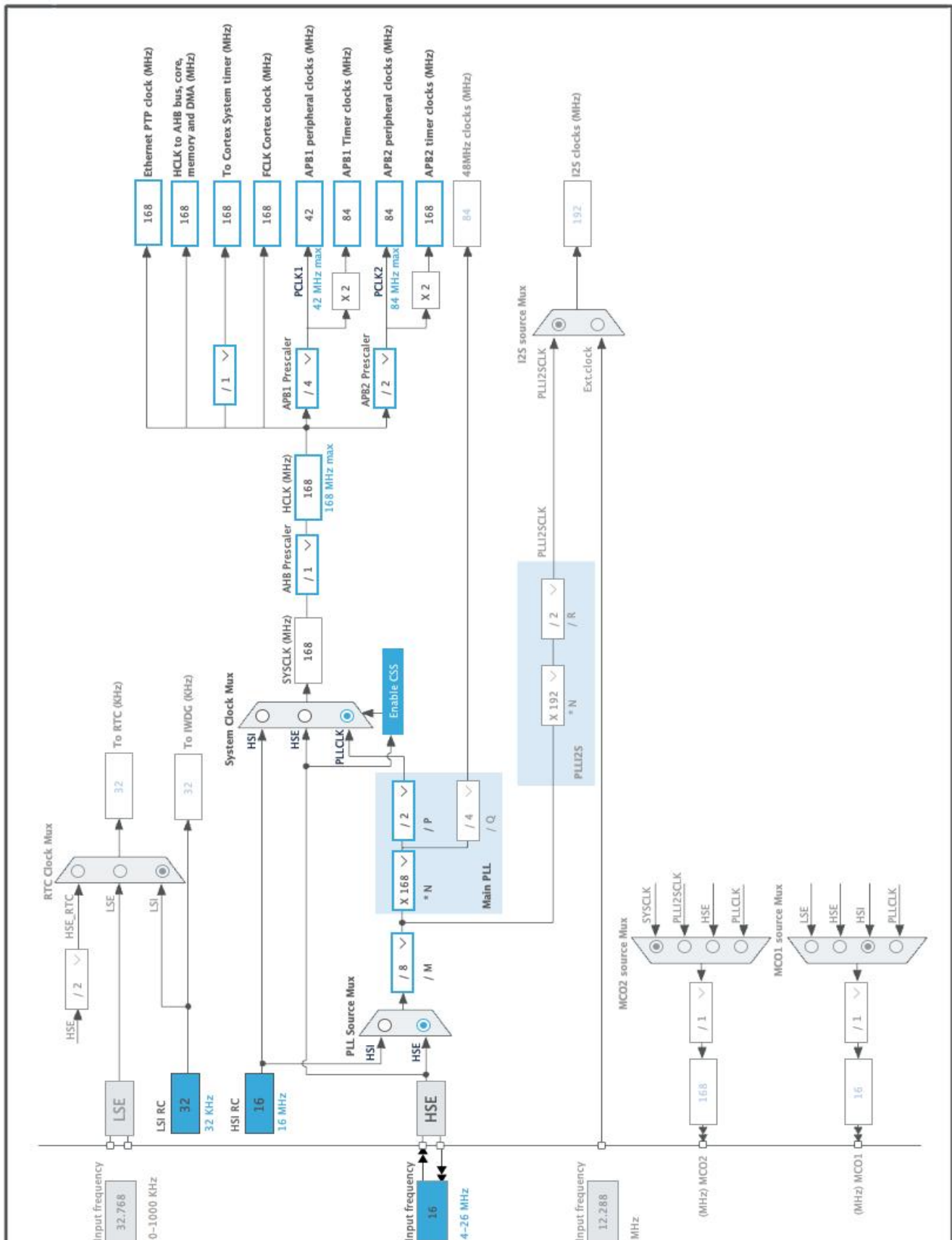
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-ANTI_TAMP *	I/O	GPIO_Input	BTN1
3	PC14-OSC32_IN *	I/O	GPIO_Output	NCOL10
4	PC15-OSC32_OUT *	I/O	GPIO_Output	NROW1
5	PH0-OSC_IN	I/O	RCC_OSC_IN	HSE_IN
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	HSE_OUT
7	NRST	Reset		
8	PC0	I/O	ADC1_IN10	AUD_IN
9	PC1 *	I/O	GPIO_Output	NROW2
10	PC2 *	I/O	GPIO_Output	NROW3
11	PC3 *	I/O	GPIO_Output	NROW4
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	TIM5_CH1	AUX_CLK
15	PA1	I/O	TIM5_CH2	AUX_GPS_PPS
16	PA2	I/O	TIM5_CH3	AUX_SYNC_MON
17	PA3 *	I/O	GPIO_Output	LED4
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	DAC_OUT1	OSC_ADJ
21	PA5	I/O	DAC_OUT2	AUD_OUT
22	PA6 *	I/O	GPIO_Output	LED1
23	PA7 *	I/O	GPIO_Output	LED2
24	PC4 *	I/O	GPIO_Output	LED7
25	PC5 *	I/O	GPIO_Output	LED8
26	PB0 *	I/O	GPIO_Output	LED9
27	PB1 *	I/O	GPIO_Output	LED10
28	PB2 *	I/O	GPIO_Input	BOOT1
29	PB10	I/O	TIM2_CH3	GPS_PPS
30	PB11	I/O	TIM2_CH4	SYNC_MON
31	VCAP_1	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	NCOL8
34	PB13 *	I/O	GPIO_Output	NCOL7
35	PB14 *	I/O	GPIO_Output	NCOL6
36	PB15 *	I/O	GPIO_Output	NCOL5

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
37	PC6	I/O	TIM8_CH1	AUX_SYNC_IN
38	PC7 *	I/O	GPIO_Output	NCOL4
39	PC8 *	I/O	GPIO_Output	NCOL3
40	PC9 *	I/O	GPIO_Output	NCOL2
41	PA8	I/O	TIM1_CH1	SYNC_OUT
42	PA9	I/O	USART1_TX	USB_RX
43	PA10	I/O	USART1_RX	USB_TX
44	PA11 *	I/O	GPIO_Output	LEDMG
45	PA12 *	I/O	GPIO_Output	LEDMR
46	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
47	VCAP_2	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	SWDCLK
50	PA15	I/O	TIM2_ETR	CLK
51	PC10	I/O	USART3_TX	GPS_RX1
52	PC11	I/O	USART3_RX	GPS_TX1
53	PC12 *	I/O	GPIO_Output	NCOL9
54	PD2 *	I/O	GPIO_Output	DB3
55	PB3	I/O	TIM2_CH2	SYNC_IN
56	PB4 *	I/O	GPIO_Output	LED3
57	PB5 *	I/O	GPIO_Output	NROW5
58	PB6 *	I/O	GPIO_Output	NCOL1
59	PB7 *	I/O	GPIO_Output	LEDMY
60	BOOT0	Boot		
61	PB8	I/O	I2C1_SCL	SCL
62	PB9	I/O	I2C1_SDA	SDA
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	blinky
Project Folder	/Users/fluffy/src/blinky
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.27.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	Yes

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_TIM8_Init	TIM8
5	MX_DAC_Init	DAC
6	MX_I2C1_Init	I2C1
7	MX_USART1_UART_Init	USART1
8	MX_ADC1_Init	ADC1
9	MX_TIM5_Init	TIM5
10	MX_TIM1_Init	TIM1
11	MX_TIM4_Init	TIM4

Rank	Function Name	Peripheral Instance Name
12	MX_TIM2_Init	TIM2
13	MX_TIM6_Init	TIM6
14	MX_TIM3_Init	TIM3
15	MX_USART3_UART_Init	USART3

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F405/415
MCU	STM32F405RGTx
Datasheet	DS8626_Rev8

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

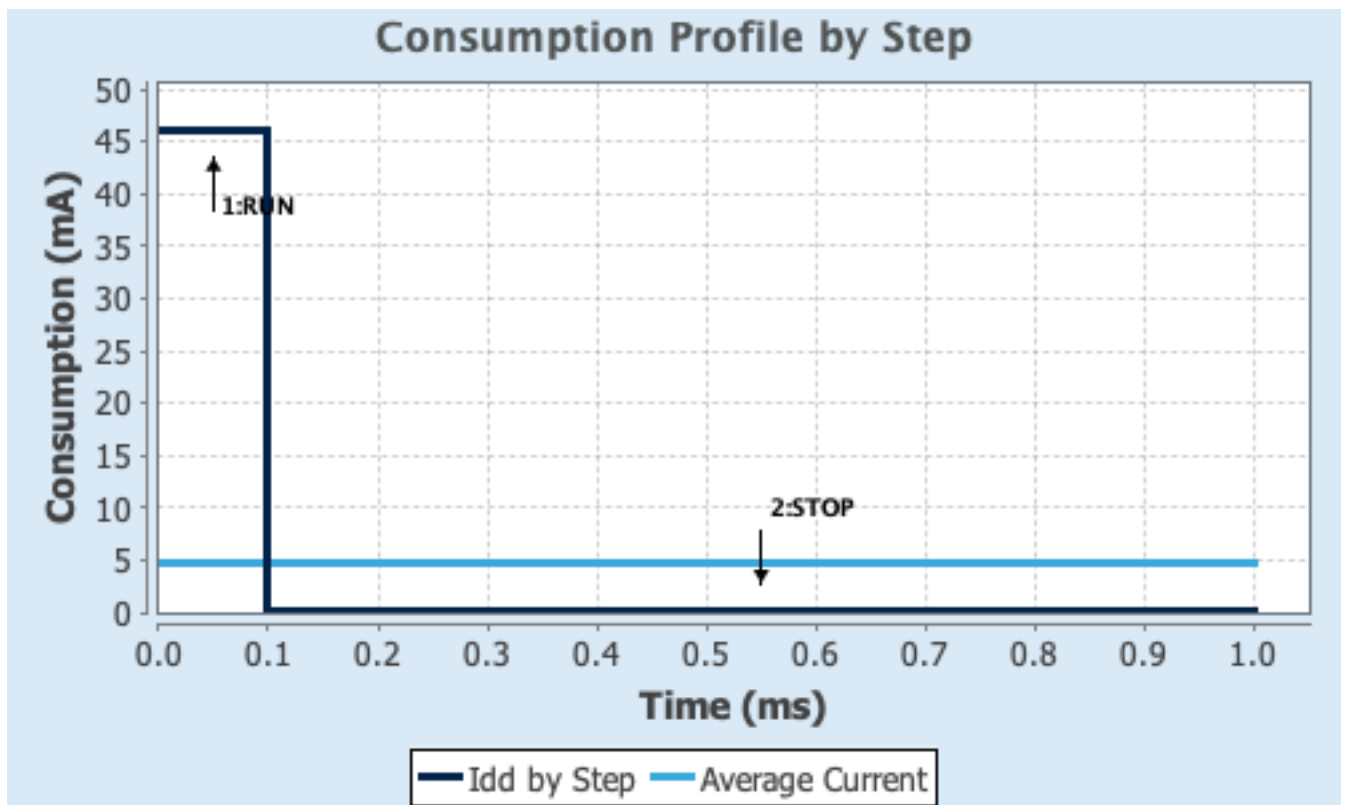
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	168 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	280 μ A
Duration	0.1 ms	0.9 ms
DMIPS	210.0	0.0
Ta Max	98.02	104.96
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

1.6. Chart



2. Peripherals and Middlewares Configuration

2.1. ADC1

mode: IN10

2.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests **Enabled ***

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source **Timer 3 Trigger Out event ***

External Trigger Conversion Edge Trigger detection on the rising edge

Rank 1

Channel Channel 10

Sampling Time 3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

2.2. DAC

mode: OUT1 Configuration

mode: OUT2 Configuration

2.2.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer Enable

Trigger None

DAC Out2 Settings:

Output Buffer	Enable
Trigger	Timer 6 Trigger Out event *
Wave generation mode	Disabled

2.3. I2C1

I2C: I2C

2.3.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

2.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

2.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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2.5. SYS

Debug: Serial Wire

Timebase Source: SysTick

2.6. TIM1

Slave Mode: Reset Mode

Trigger Source: ITR1

Clock Source : Internal Clock

Channel1: Output Compare CH1

2.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	3360-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	55000-1 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable
Slave Mode Controller	Reset Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Output Compare Channel 1:

Mode	Toggle on match *
Pulse (16 bits value)	1000 *
Output compare preload	Disable
CH Polarity	High
CH Idle State	Reset

2.7. TIM2

Clock Source : ETR2

Channel2: Input Capture direct mode

Channel3: Input Capture direct mode

Channel4: Input Capture direct mode

2.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	2048000-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Update Event *

Clock:

Clock Filter (4 bits value)	0
Clock Polarity	non inverted
Clock Prescaler	Prescaler not used

Input Capture Channel 2:

Polarity Selection	Falling Edge *
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 3:

Polarity Selection	Falling Edge *
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 4:

Polarity Selection	Falling Edge *
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

2.8. TIM3

Clock Source : Internal Clock

2.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	84-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	114-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Update Event *

2.9. TIM4

Slave Mode: Reset Mode

Trigger Source: ITR1

mode: Clock Source

2.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	84-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1000-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Slave Mode Controller	Reset Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

2.10. TIM5

Slave Mode: External Clock Mode 1

Trigger Source: TI1_ED

Channel2: Input Capture direct mode

Channel3: Input Capture direct mode

2.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	1 *
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	10000000-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Slave Mode Controller	ETR mode 1

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Trigger:

Trigger Filter (4 bits value)	0
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Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

2.11. TIM6

mode: Activated

2.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	84-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	114-1 *
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Update Event *
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2.12. TIM8

Clock Source : Internal Clock

Channel1: Input Capture direct mode

2.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	3360-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	55000-1 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Both Edges *
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

2.13. USART1

Mode: Asynchronous

2.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

2.14. USART3

Mode: Asynchronous

2.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	4800 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

* User modified value

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	AUD_IN
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	OSC_ADJ
	PA5	DAC_OUT2	Analog mode	No pull-up and no pull-down	n/a	AUD_OUT
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	SCL
	PB9	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	SDA
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	HSE_IN
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	HSE_OUT
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWDCLK
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	SYNC_OUT
TIM2	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	GPS_PPS
	PB11	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	SYNC_MON
	PA15	TIM2_ETR	Alternate Function Push Pull	No pull-up and no pull-down	Low	CLK
	PB3	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	SYNC_IN
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	AUX_CLK
	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	AUX_GPS_PPS
	PA2	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	AUX_SYNC_MON
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	AUX_SYNC_IN
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	High *	USB_RX
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	High *	USB_TX
USART3	PC10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	High *	GPS_RX1
	PC11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	High *	GPS_TX1
GPIO	PC13-ANTI_TAMP	GPIO_Input	Input mode	Pull-up *	n/a	BTN1
	PC14-OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NCOL10
	PC15-OSC32_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NROW1
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NROW2
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NROW3

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NROW4
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED4
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED7
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED8
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED9
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED10
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BOOT1
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NCOL8
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NCOL7
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NCOL6
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NCOL5
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NCOL4
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NCOL3
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NCOL2
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDMG
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDMR
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NCOL9
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	DB3
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NROW5
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NCOL1
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDMY

3.2. DMA configuration

DMA request	Stream	Direction	Priority
DAC2	DMA1_Stream6	Memory To Peripheral	Low
ADC1	DMA2_Stream0	Peripheral To Memory	Low

DAC2: DMA1_Stream6 DMA request Settings:

Mode: **Circular ***
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: **Word ***
Memory Data Width: **Word ***

ADC1: DMA2_Stream0 DMA request Settings:

Mode: **Circular ***
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: **Word ***
Memory Data Width: **Word ***

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA1 stream6 global interrupt	true	0	0
ADC1, ADC2 and ADC3 global interrupts	true	0	0
TIM1 capture compare interrupt	true	0	0
TIM2 global interrupt	true	2	0
TIM3 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
USART3 global interrupt	true	0	0
TIM8 trigger and commutation interrupts and TIM14 global interrupt	true	15	0
TIM8 capture compare interrupt	true	3	0
TIM5 global interrupt	true	0	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
USART1 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
FPU global interrupt	unused		

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream6 global interrupt	false	true	true
ADC1, ADC2 and ADC3 global interrupts	false	true	true
TIM1 capture compare interrupt	false	true	true
TIM2 global interrupt	false	true	true
TIM3 global interrupt	false	true	true
TIM4 global interrupt	false	true	true
USART3 global interrupt	false	true	true
TIM8 trigger and commutation interrupts and TIM14 global interrupt	false	true	true
TIM8 capture compare interrupt	false	true	true
TIM5 global interrupt	false	true	true
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	false	true	true
DMA2 stream0 global interrupt	false	true	true

* User modified value

4. System Views

4.1. Category view

4.1.1. Current

Middleware						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA ✓	ADC1 ✓	TIM1 ✓	I2C1 ✓			
GPIO ✓	DAC ✓	TIM2 ✓	USART1 ✓			
NVIC ✓		TIM3 ✓	USART3 ✓			
RCC ✓		TIM4 ✓				
SYS ✓		TIM5 ✓				
		TIM6 ✓				
		TIM8 ✓				

5. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32f405-415_407-417_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32f405-415_407-417_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32f4_svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstmcsuite.pdf
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