

1. Description

1.1. Project

Project Name	blinky
Board Name	custom
Generated with:	STM32CubeMX 6.8.0
Date	07/07/2023

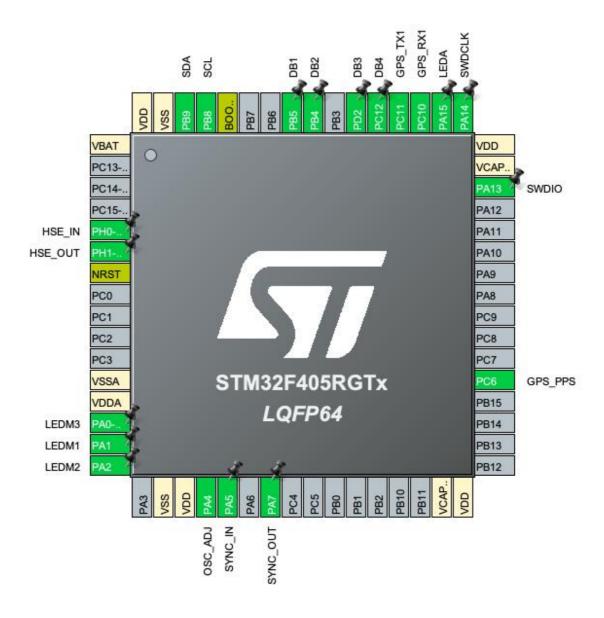
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F405/415
MCU name	STM32F405RGTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4	

2. Pinout Configuration

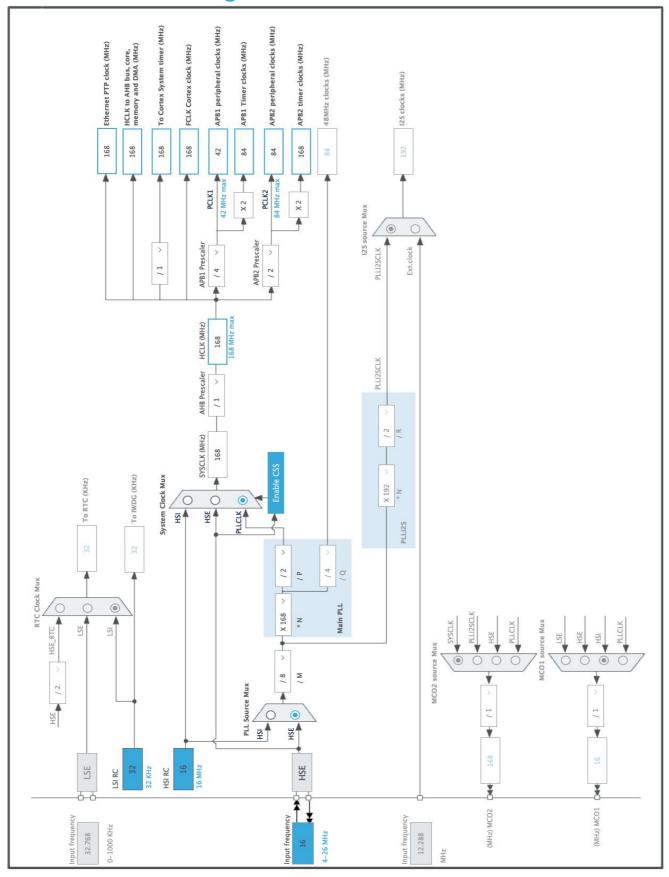


3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP64	(function after	,	Function(s)	_5.00.
LQIIOT			r driction(3)	
	reset)	_		
1	VBAT	Power	D00 000 W	
5	PH0-OSC_IN	I/O	RCC_OSC_IN	HSE_IN
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	HSE_OUT
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP *	I/O	GPIO_Output	LEDM3
15	PA1 *	I/O	GPIO_Output	LEDM1
16	PA2 *	I/O	GPIO_Output	LEDM2
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	DAC_OUT1	OSC_ADJ
21	PA5	I/O	TIM2_CH1	SYNC_IN
23	PA7	I/O	TIM3_CH2	SYNC_OUT
31	VCAP_1	Power		
32	VDD	Power		
37	PC6	I/O	TIM8_CH1	GPS_PPS
46	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
47	VCAP_2	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	SWDCLK
50	PA15 *	I/O	GPIO_Output	LEDA
51	PC10	I/O	USART3_TX	GPS_RX1
52	PC11	I/O	USART3_RX	GPS_TX1
53	PC12 *	I/O	GPIO_Output	DB4
54	PD2 *	I/O	GPIO_Output	DB3
56	PB4 *	I/O	GPIO_Input	DB2
57	PB5 *	I/O	GPIO_Input	DB1
60	воото	Boot		
61	PB8	I/O	I2C1_SCL	SCL
62	PB9	I/O	I2C1_SDA	SDA
63	VSS	Power		
64	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value
Project Name	blinky
Project Folder	/Users/fluffy/src/blinky
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F4 V1.27.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_TIM2_Init	TIM2
4	MX_TIM7_Init	TIM7
5	MX_TIM8_Init	TIM8
6	MX_DAC_Init	DAC
7	MX_I2C1_Init	I2C1
8	MX_TIM3_Init	TIM3
9	MX_USART3_UART_Init	USART3

blinky Project
Configuration Report

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4	
Line	STM32F405/415	
мси	STM32F405RGTx	
Datasheet	DS8626_Rev8	

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

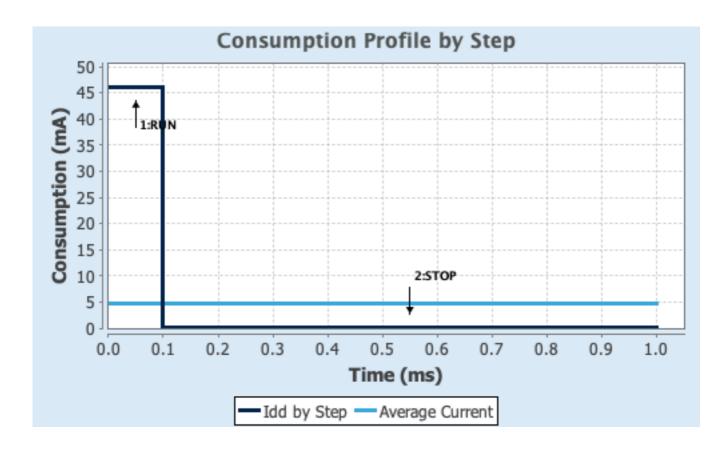
6.4. Sequence

	T	
Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	168 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	280 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	210.0	0.0
Ta Max	98.02	104.96
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. DAC

mode: OUT1 Configuration7.1.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer Enable
Trigger None

7.2. I2C1 I2C: I2C

7.2.1. Parameter Settings:

Master Features:

I2C Speed Mode Standard Mode

I2C Clock Speed (Hz) 100000

Slave Features:

Clock No Stretch Mode Disabled

Primary Address Length selection 7-bit

Dual Address Acknowledged Disabled

Primary slave address 0

General Call address detection Disabled

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.5. TIM2

Clock Source : Internal Clock

Channel1: Input Capture direct mode

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 84 *

Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) 1000000 *

Internal Clock Division (CKD) No Division auto-reload preload Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection Both Edges *

IC Selection Direct
Prescaler Division Ratio No division

Input Filter (4 bits value) 0

7.6. TIM3

Channel2: Output Compare CH2

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 65535

Internal Clock Division (CKD)

No Division

auto-reload preload

Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Output Compare Channel 2:

Mode Frozen (used for Timing base)

Pulse (16 bits value) 0

Output compare preload Disable

CH Polarity High

7.7. TIM7

mode: Activated

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 84 *

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 1000 *

auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection Reset (UG bit from TIMx_EGR)

7.8. TIM8

Clock Source: Internal Clock

Channel1: Input Capture direct mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 65535

Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0

auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection Rising Edge
IC Selection Direct
Prescaler Division Ratio No division

Input Filter (4 bits value) 0

7.9. **USART3**

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	OSC_ADJ
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	SCL
	PB9	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High	SDA
RCC	PH0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	HSE_IN
	PH1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	HSE_OUT
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	SWDCLK
TIM2	PA5	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	SYNC_IN
TIM3	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	SYNC_OUT
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	GPS_PPS
USART3	PC10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	GPS_RX1
	PC11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	GPS_TX1
GPIO	PA0-WKUP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDM3
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDM1
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDM2
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDA
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DB4
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DB3
	PB4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB2
	PB5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB1

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority		
Non maskable interrupt	true	0	0		
Hard fault interrupt	true	0	0		
Memory management fault	true	0	0		
Pre-fetch fault, memory access fault	true	0	0		
Undefined instruction or illegal state	true	0	0		
System service call via SWI instruction	true	0	0		
Debug monitor	true	0	0		
Pendable request for system service	true	0	0		
System tick timer	true	15	0		
TIM2 global interrupt	true	3	0		
TIM7 global interrupt	true	2	0		
PVD interrupt through EXTI line 16	unused				
Flash global interrupt	unused				
RCC global interrupt	unused				
TIM3 global interrupt	unused				
I2C1 event interrupt	unused				
I2C1 error interrupt	unused				
USART3 global interrupt	unused				
TIM8 break interrupt and TIM12 global interrupt	unused				
TIM8 update interrupt and TIM13 global interrupt	unused				
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused				
TIM8 capture compare interrupt	unused				
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused				
FPU global interrupt	unused				

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM2 global interrupt	false	true	true
TIM7 global interrupt	false	true	true

^{*} User modified value

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

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BSDL files https://www.st.com/resource/en/bsdl_model/stm32f405-415_407-

417_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32f405-415_407-

417_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f4_svd.zip

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