

1. Description

1.1. Project

Project Name	blinky
Board Name	custom
Generated with:	STM32CubeMX 6.7.0
Date	03/13/2023

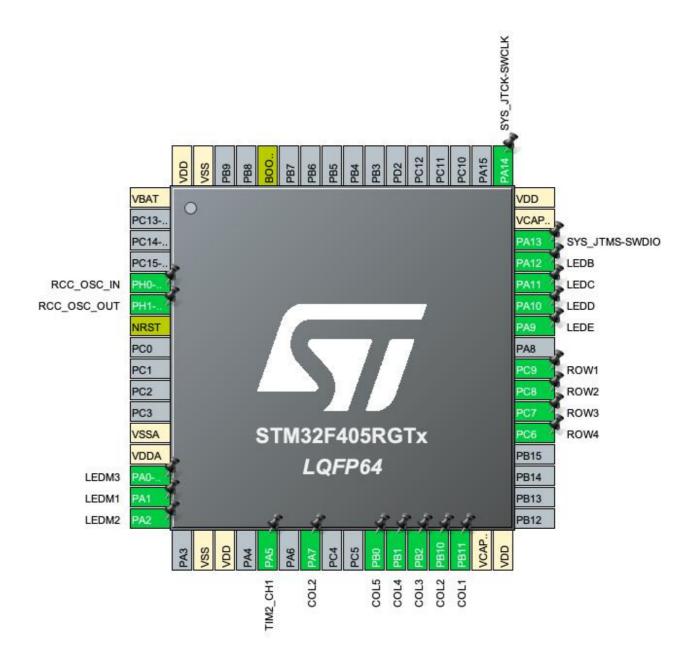
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F405/415
MCU name	STM32F405RGTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration

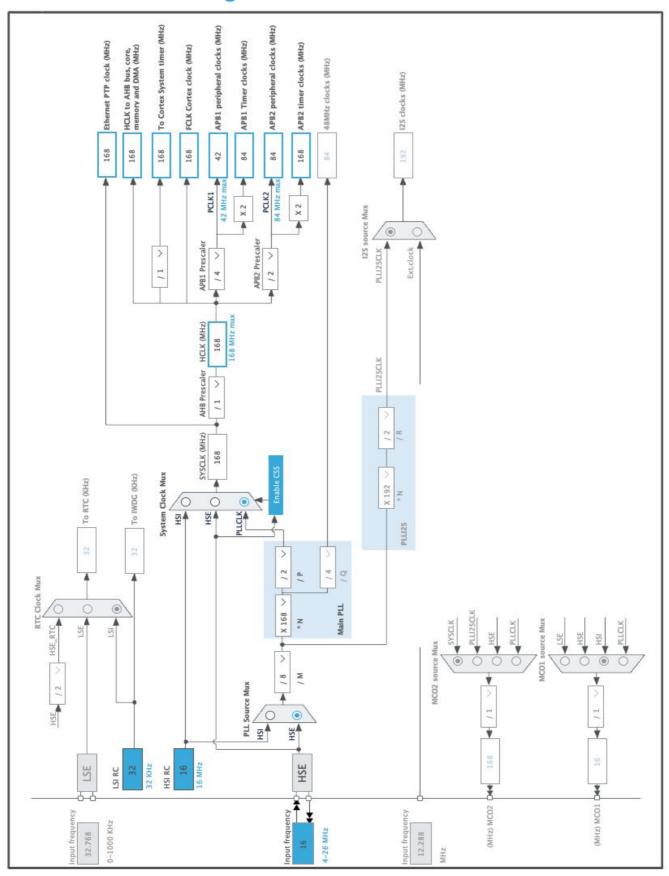


3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP64	(function after		Function(s)	
	reset)			
1	VBAT	Power		
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP *	I/O	GPIO_Output	LEDM3
15	PA1 *	I/O	GPIO_Output	LEDM1
16	PA2 *	I/O	GPIO_Output	LEDM2
18	VSS	Power		
19	VDD	Power		
21	PA5	I/O	TIM2_CH1	
23	PA7 *	I/O	GPIO_Output	COL2
26	PB0 *	I/O	GPIO_Output	COL5
27	PB1 *	I/O	GPIO_Output	COL4
28	PB2 *	I/O	GPIO_Output	COL3
29	PB10 *	I/O	GPIO_Output	COL2
30	PB11 *	I/O	GPIO_Output	COL1
31	VCAP_1	Power		
32	VDD	Power		
37	PC6 *	I/O	GPIO_Output	ROW4
38	PC7 *	I/O	GPIO_Output	ROW3
39	PC8 *	I/O	GPIO_Output	ROW2
40	PC9 *	I/O	GPIO_Output	ROW1
42	PA9 *	I/O	GPIO_Output	LEDE
43	PA10 *	I/O	GPIO_Output	LEDD
44	PA11 *	I/O	GPIO_Output	LEDC
45	PA12 *	I/O	GPIO_Output	LEDB
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VCAP_2	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	blinky
Project Folder	/Users/fluffy/src/blinky
Toolchain / IDE	EWARM V8.50
Firmware Package Name and Version	STM32Cube FW_F4 V1.27.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_TIM2_Init	TIM2
4	MX_TIM7_Init	TIM7
5	MX_TIM8_Init	TIM8

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4	
Line	STM32F405/415	
мси	STM32F405RGTx	
Datasheet	DS8626_Rev8	

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

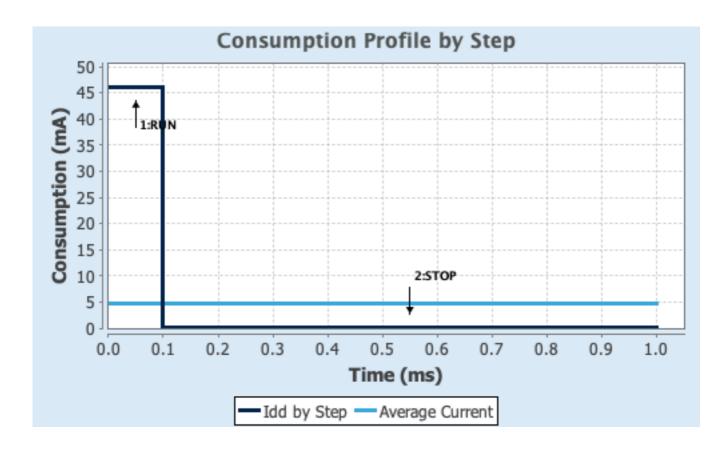
6.4. Sequence

	T	
Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	168 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	280 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	210.0	0.0
Ta Max	98.02	104.96
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.2. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.3. TIM2

Clock Source : Internal Clock

Channel1: Input Capture direct mode

7.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 168 *
Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) 1000000 *

Internal Clock Division (CKD) No Division auto-reload preload Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection Rising Edge
IC Selection Direct
Prescaler Division Ratio No division

Input Filter (4 bits value) 0

7.4. TIM7

mode: Activated

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 168 *

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 1000 *

auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection Reset (UG bit from TIMx_EGR)

7.5. TIM8

Clock Source: Internal Clock

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division
Repetition Counter (RCR - 8 bits value) 0

auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PH0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
TIM2	PA5	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PA0-WKUP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDM3
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDM1
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDM2
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	COL2
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	COL5
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	COL4
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	COL3
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	COL2
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	COL1
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ROW4
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ROW3
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ROW2
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ROW1
	PA9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDE
	PA10 GPIO_Ou		Output Push Pull	No pull-up and no pull-down	Low	LEDD
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDC
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDB

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority		
Non maskable interrupt	true	0	0		
Hard fault interrupt	true	0	0		
Memory management fault	true	0	0		
Pre-fetch fault, memory access fault	true	0	0		
Undefined instruction or illegal state	true	0	0		
System service call via SWI instruction	true	0	0		
Debug monitor	true	0	0		
Pendable request for system service	true	0	0		
System tick timer	true	15	0		
TIM2 global interrupt	true	3	0		
TIM7 global interrupt	true	2	0		
PVD interrupt through EXTI line 16	unused				
Flash global interrupt		unused			
RCC global interrupt	unused				
TIM8 break interrupt and TIM12 global interrupt	pt unused				
TIM8 update interrupt and TIM13 global interrupt	unused				
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused				
TIM8 capture compare interrupt	unused				
FPU global interrupt	unused				

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler	
Non maskable interrupt	false	true	false	
Hard fault interrupt	false true		false	
Memory management fault	false true		false	
Pre-fetch fault, memory access fault	false	true	false	
Undefined instruction or illegal state	false	true	false	
System service call via SWI instruction	false	true	false	
Debug monitor	false	true	false	
Pendable request for system service	false	true	false	
System tick timer	false	true	true	
TIM2 global interrupt	false	true	true	
TIM7 global interrupt	false	true	true	

blinky Project
Configuration Report

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

			Middleware			
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA		TIM2 🤡				
GPIO ♥		ТІМ7 ♥				
NVIC 🔮		TIM8 ♥				
RCC ⊘						
SYS 🔮						

10. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f405-415_407-

417_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32f405-415_407-

417_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f4_svd.zip

Description

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f405-415_407-

417_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32f405-415_407-

417_ibis.zip

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stm8_embedded_software_solutions.pdf

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