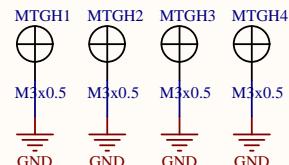
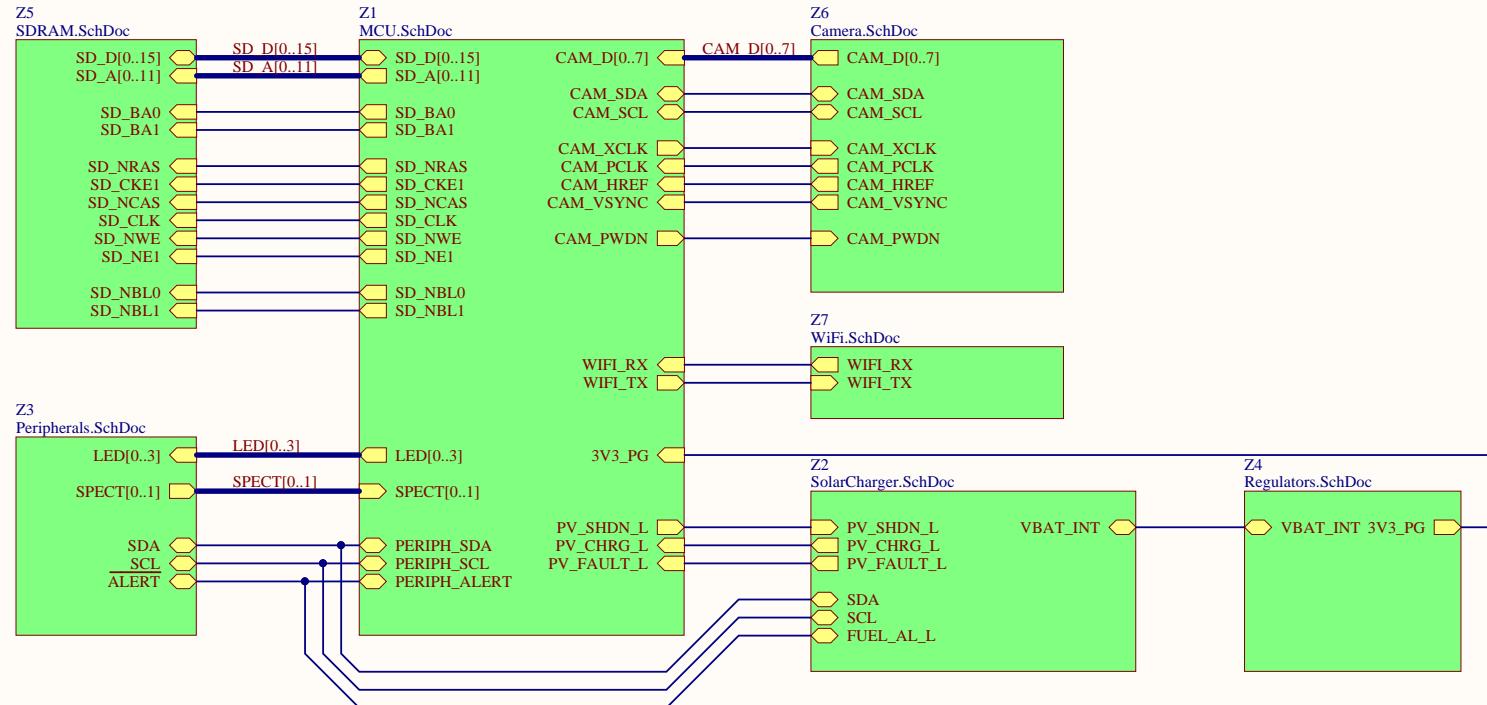


A

A



Title

Solens Camera Subsystem
ERC_WARN, FOOTPRINT_N/A

Size

Number

Revision

Date:

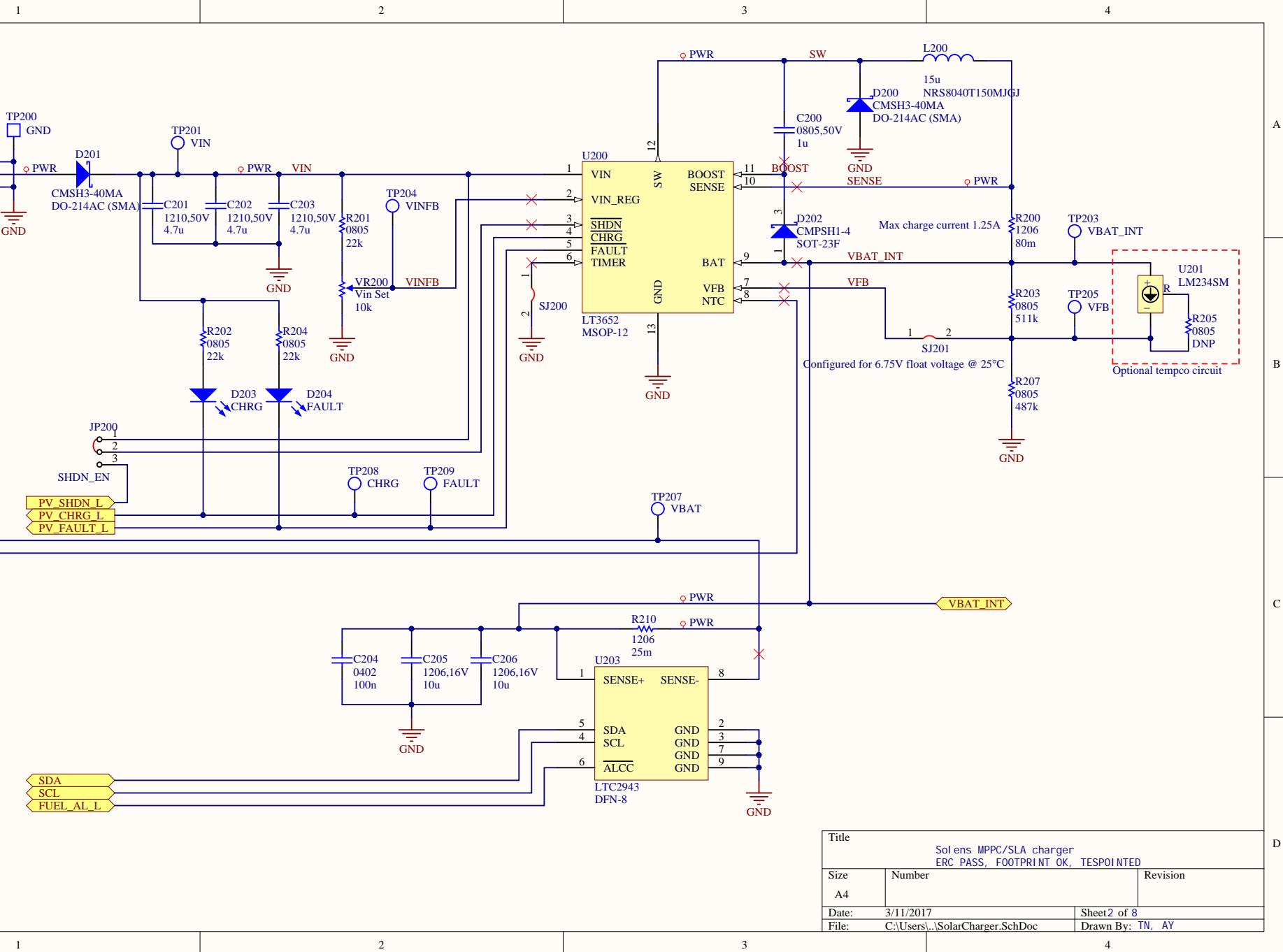
3/11/2017

Sheet 1 of 8

File:

C:\Users\..\Solens.SchDoc

Drawn By: JL, AY



A

A

B

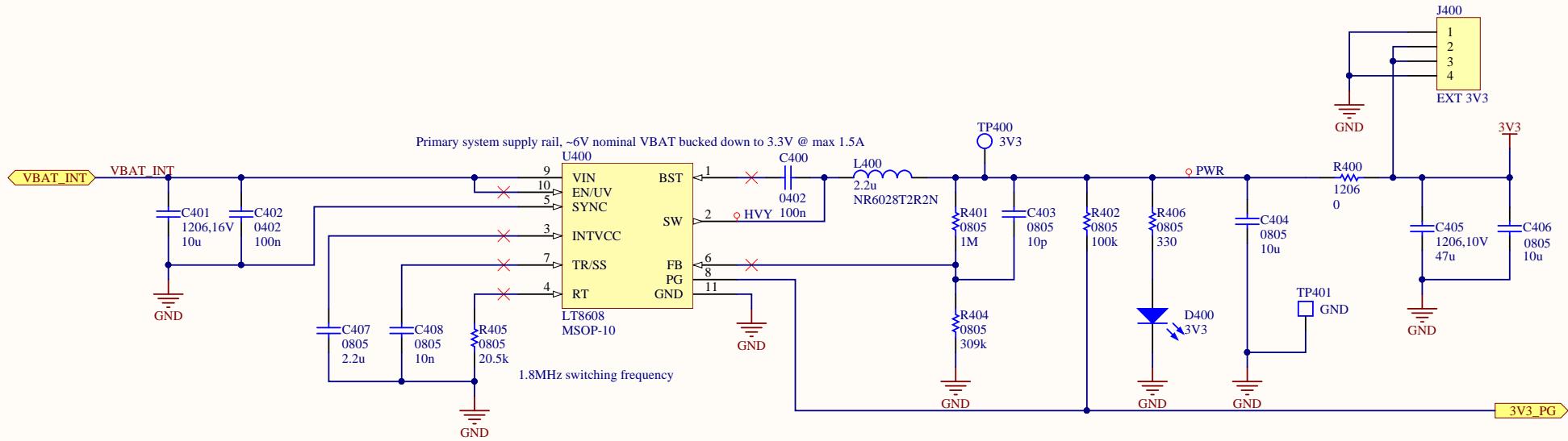
B

C

C

D

D



Title		
Solens Voltage Regulators		ERC PASS, FOOTPRINT OK, TESPOINTED
Size		Revision
A4		
Date:	3/11/2017	Sheet 3 of 8
File:	C:\Users...\Regulators.SchDoc	Drawn By: TN, AY

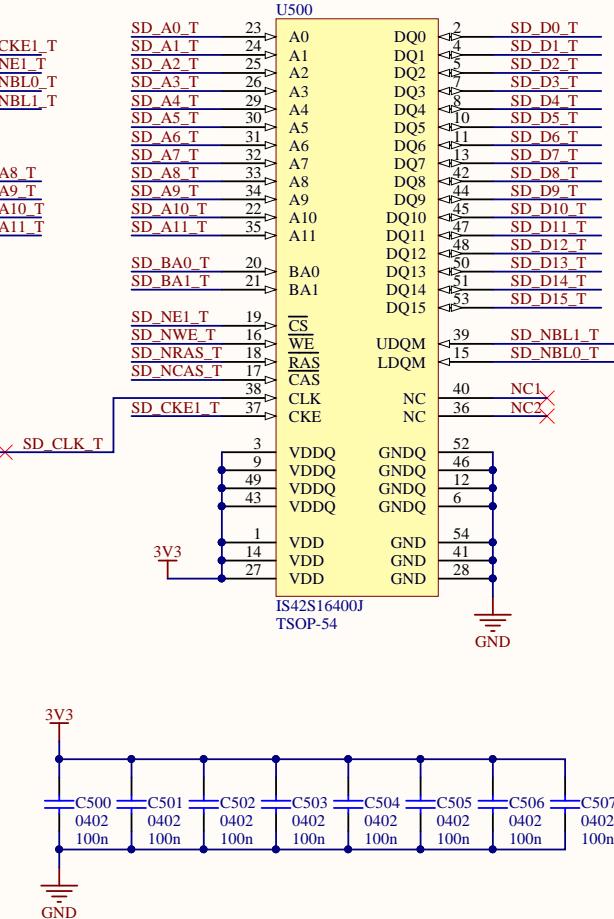
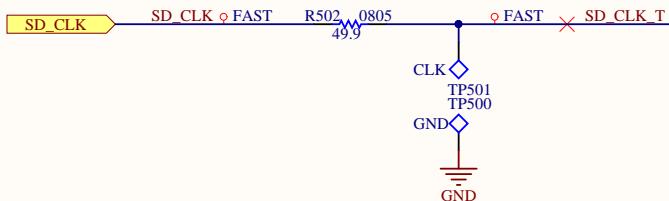
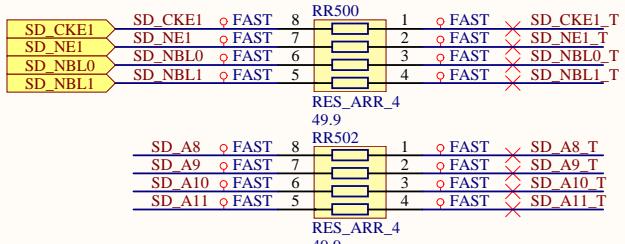
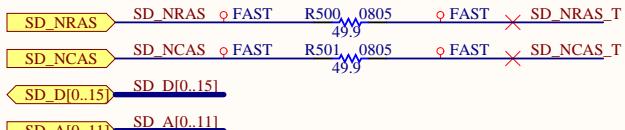
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2

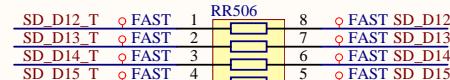
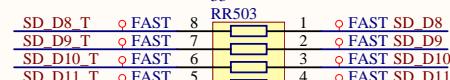
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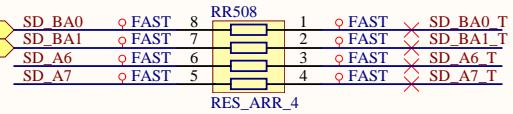
A



DATA termination to be placed halfway between MCU and RAM



ADDR and CLK termination to be placed at MCU



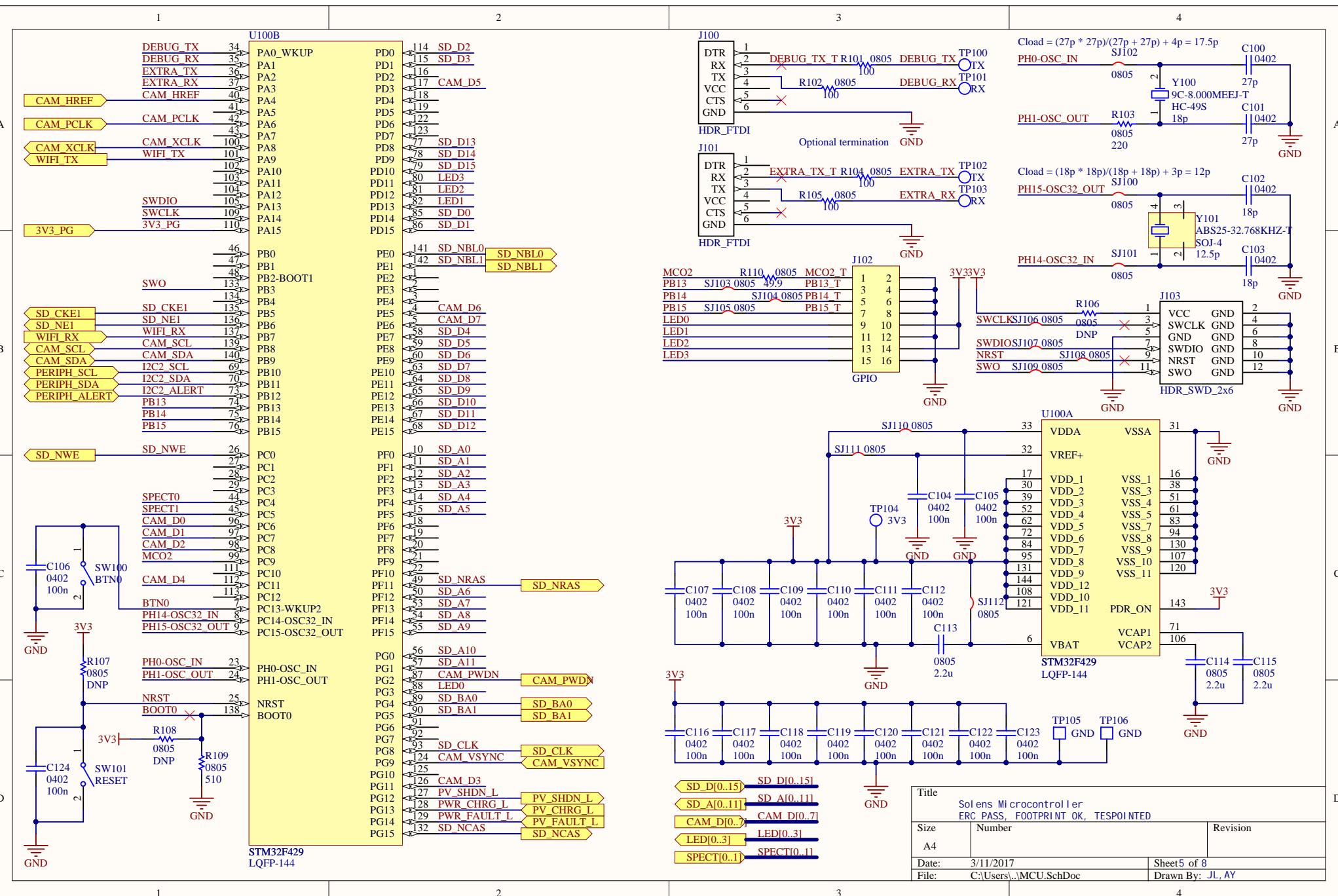
Title		
Solens_SDRAM		
Size	Number	Revision
A4		
Date:	3/11/2017	Sheet 4 of 8
File:	C:\Users\...\SDRAM.SchDoc	Drawn By: JL, AY

1

2

3

4



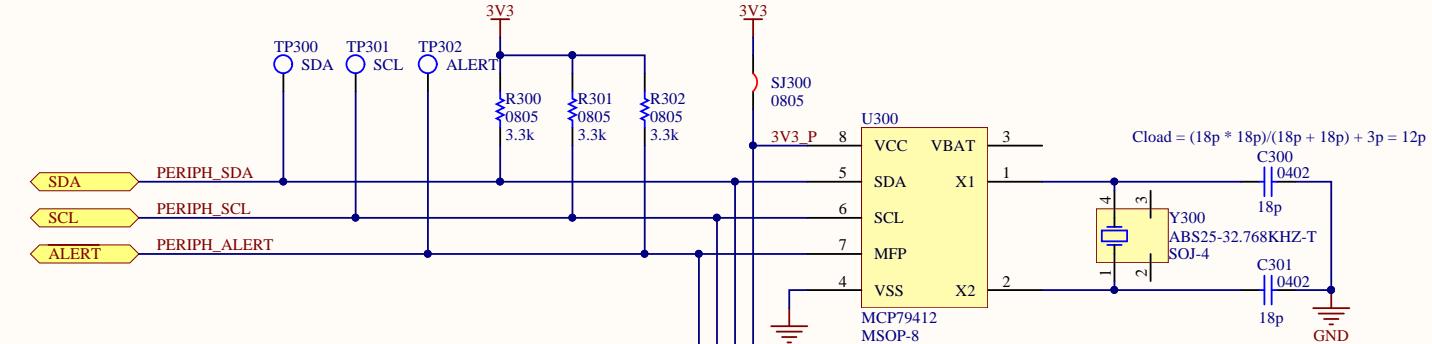
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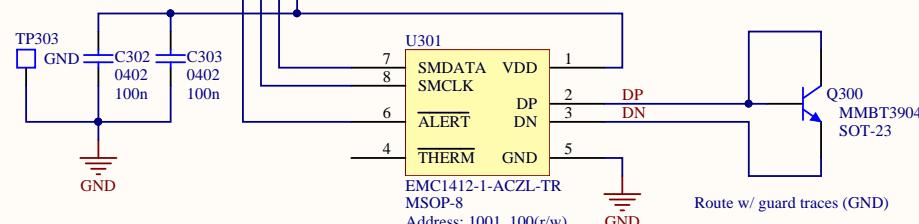
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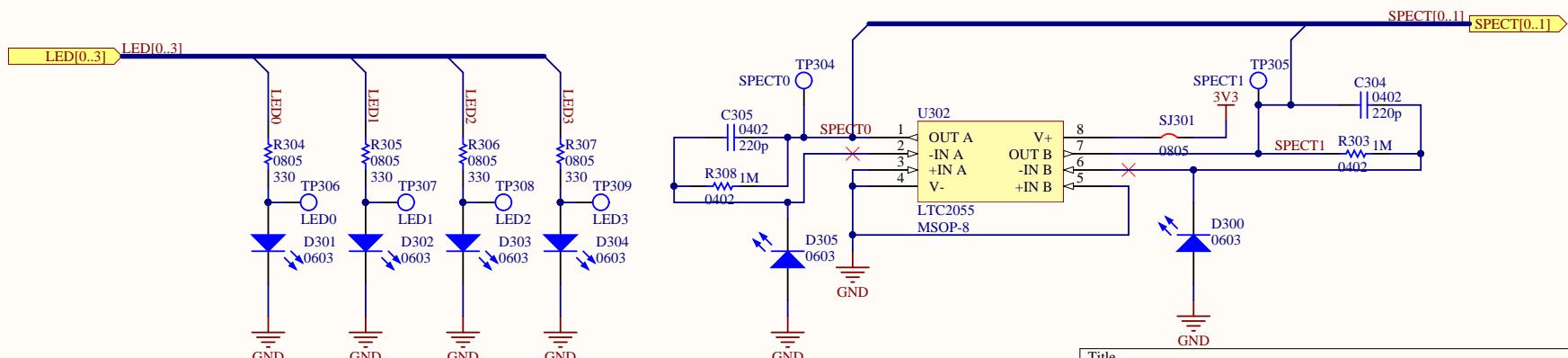
A



B



C



D

Title		
Solens Peripherals ERC PASS, FOOTPRINT OK, TESPOINTED		
Size	Number	Revision
A4		
Date:	3/11/2017	Sheet 6 of 8
File:	C:\Users...\Peripherals.SchDoc	Drawn By: AY

1

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3

4

A

A

B

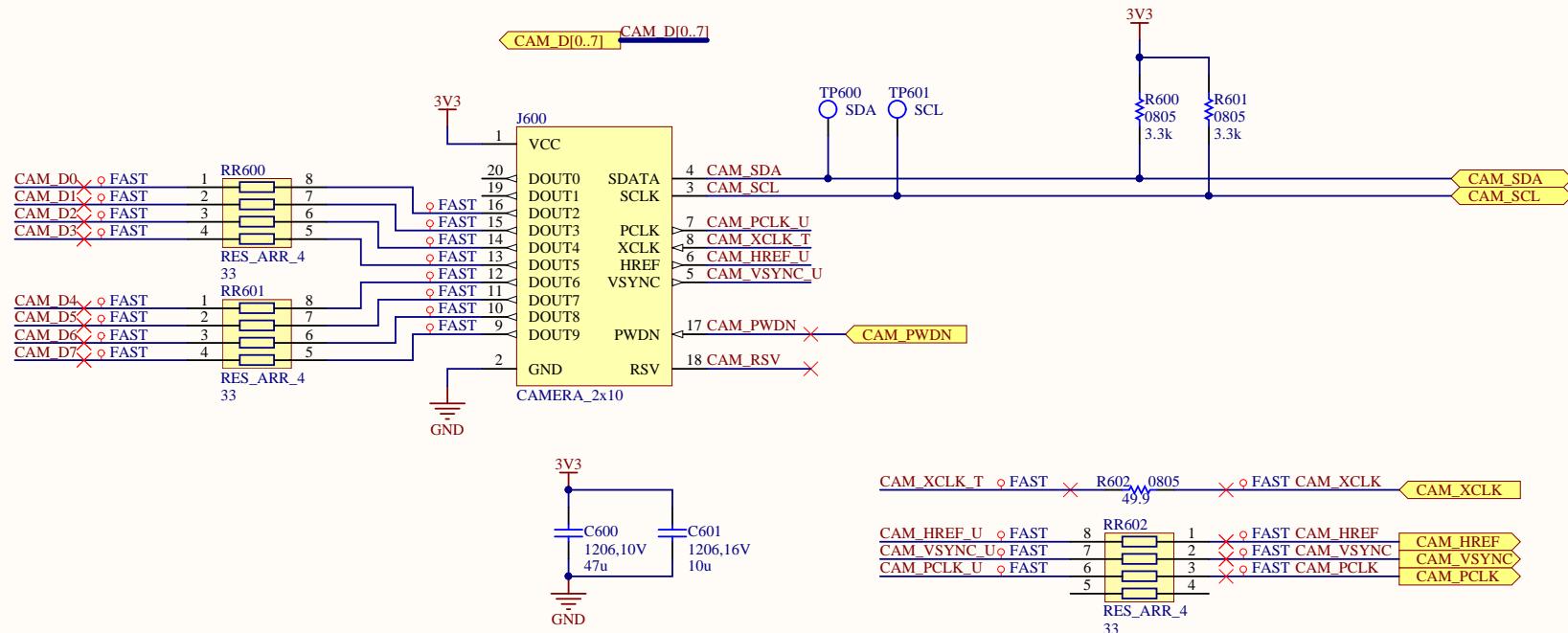
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C

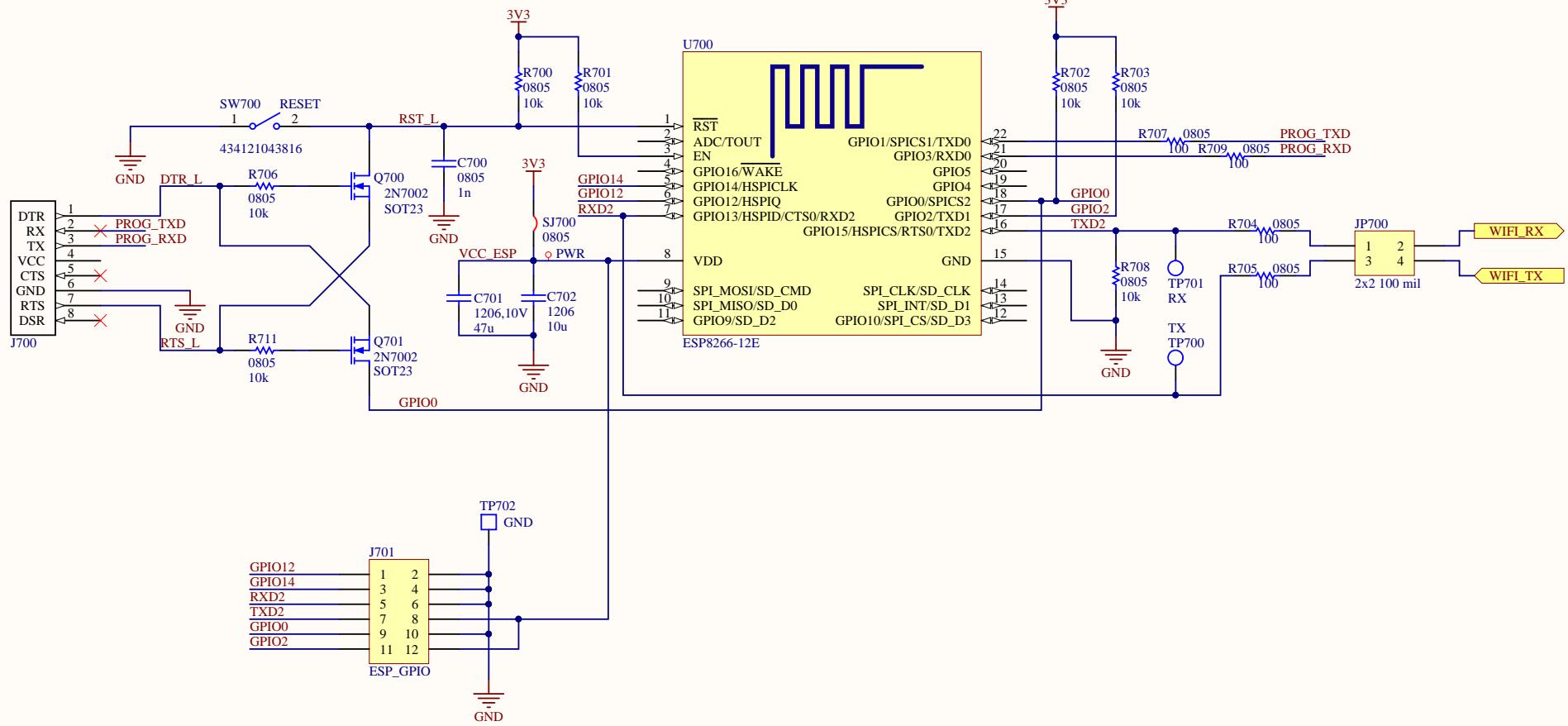
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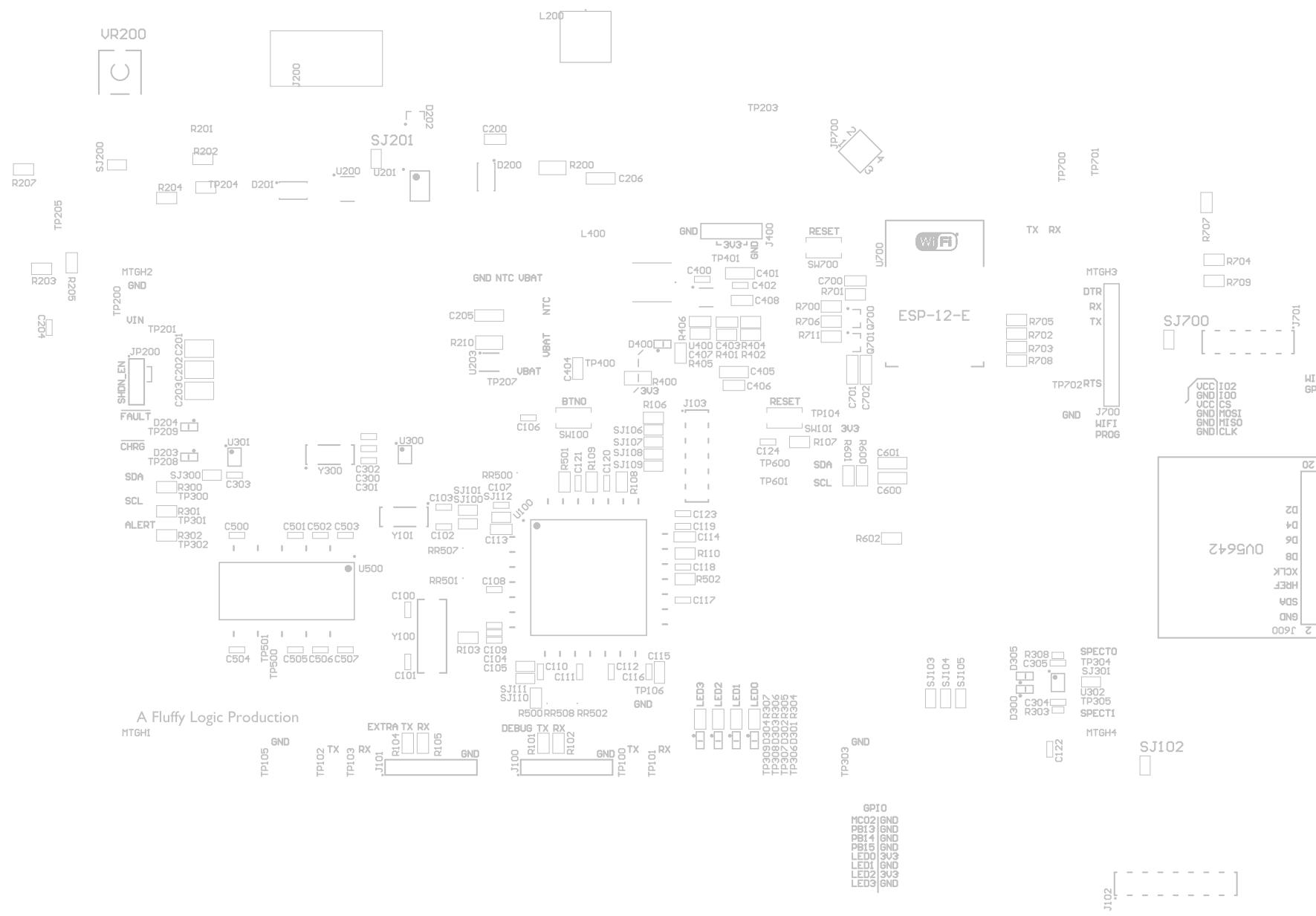
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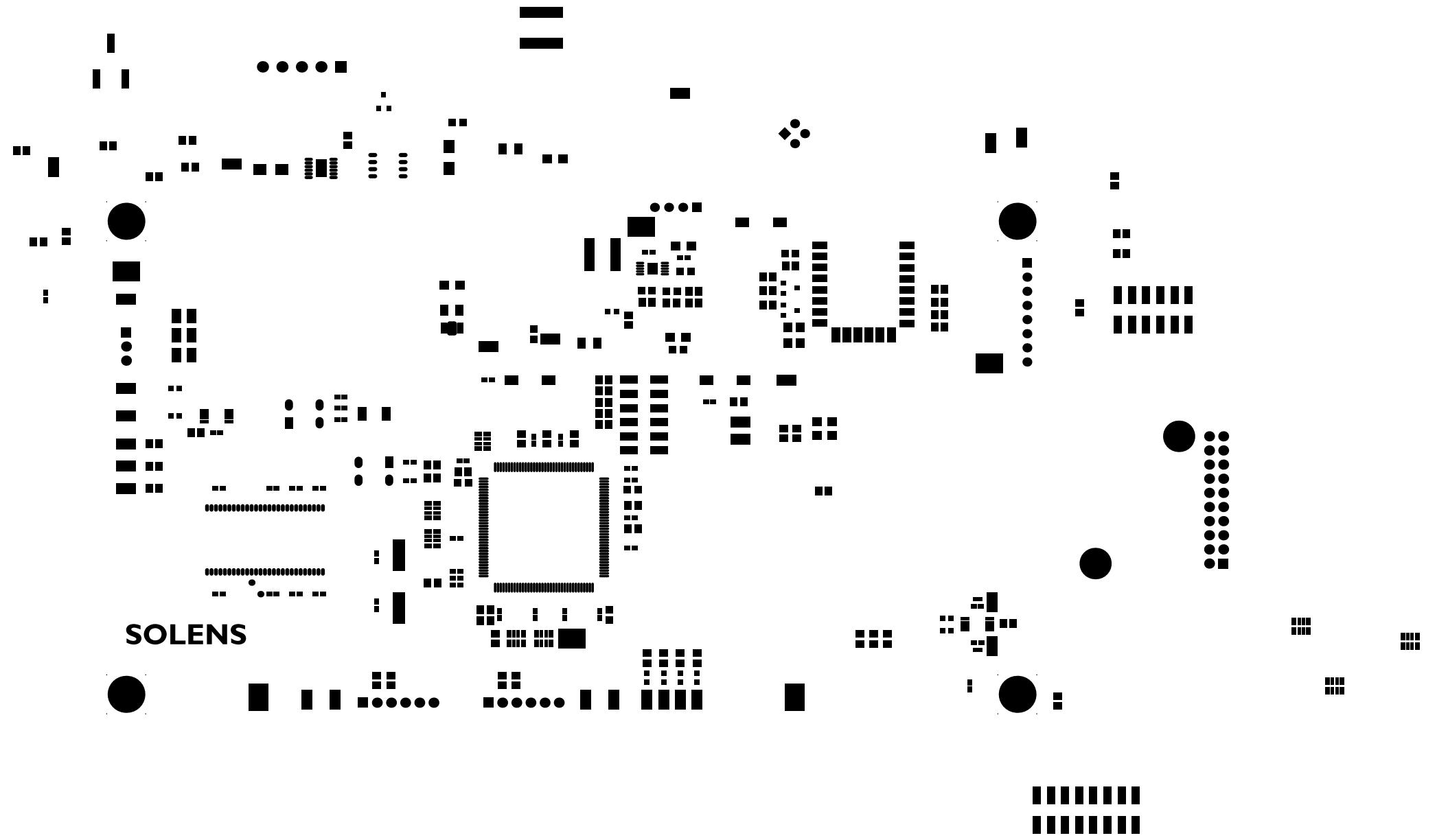
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Size A4	Number	Revision
Date: 3/11/2017	Sheet 7 of 8	
File: C:\Users...\Camera.SchDoc		Drawn By: JL, AY



Title		
Solens WiFi Subsystem ERC PASS, FOOTPRINT OK, TESTPOINTED		
Size		Number
A4		Revision
Date:	3/11/2017	Sheet 8 of 8
File:	C:\Users\...\WiFi.SchDoc	Drawn By: JL, AY



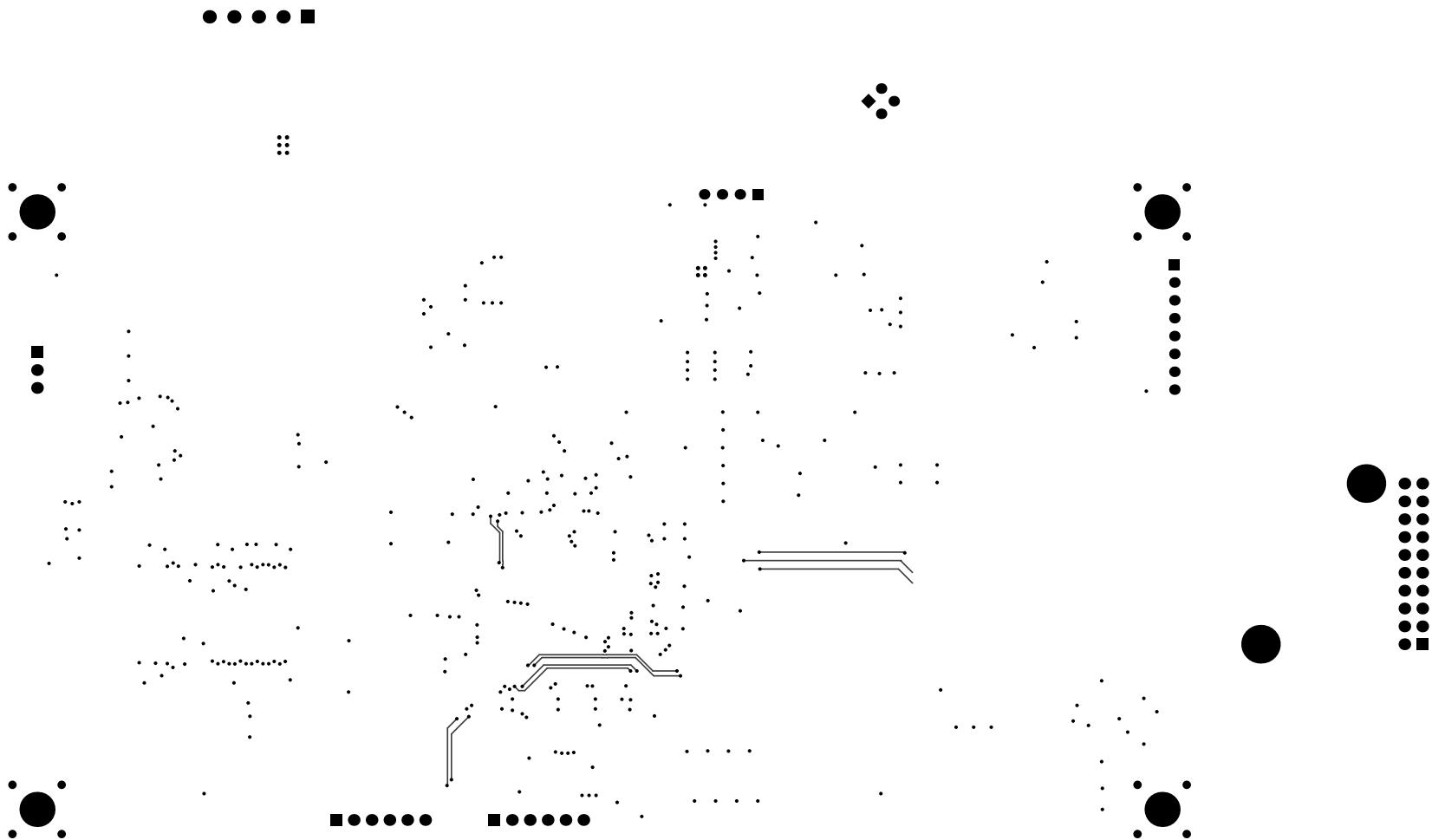
SOLENS

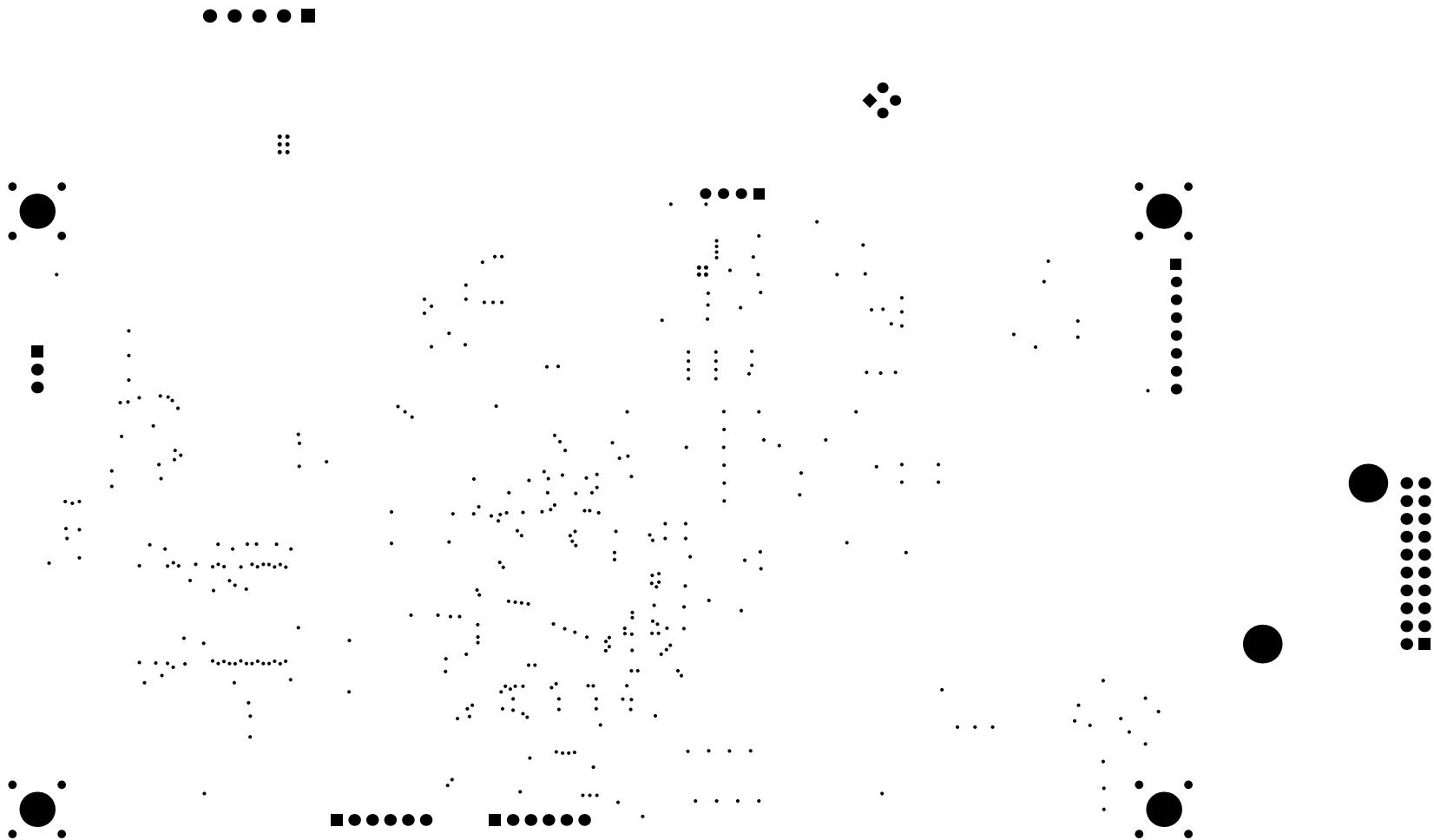


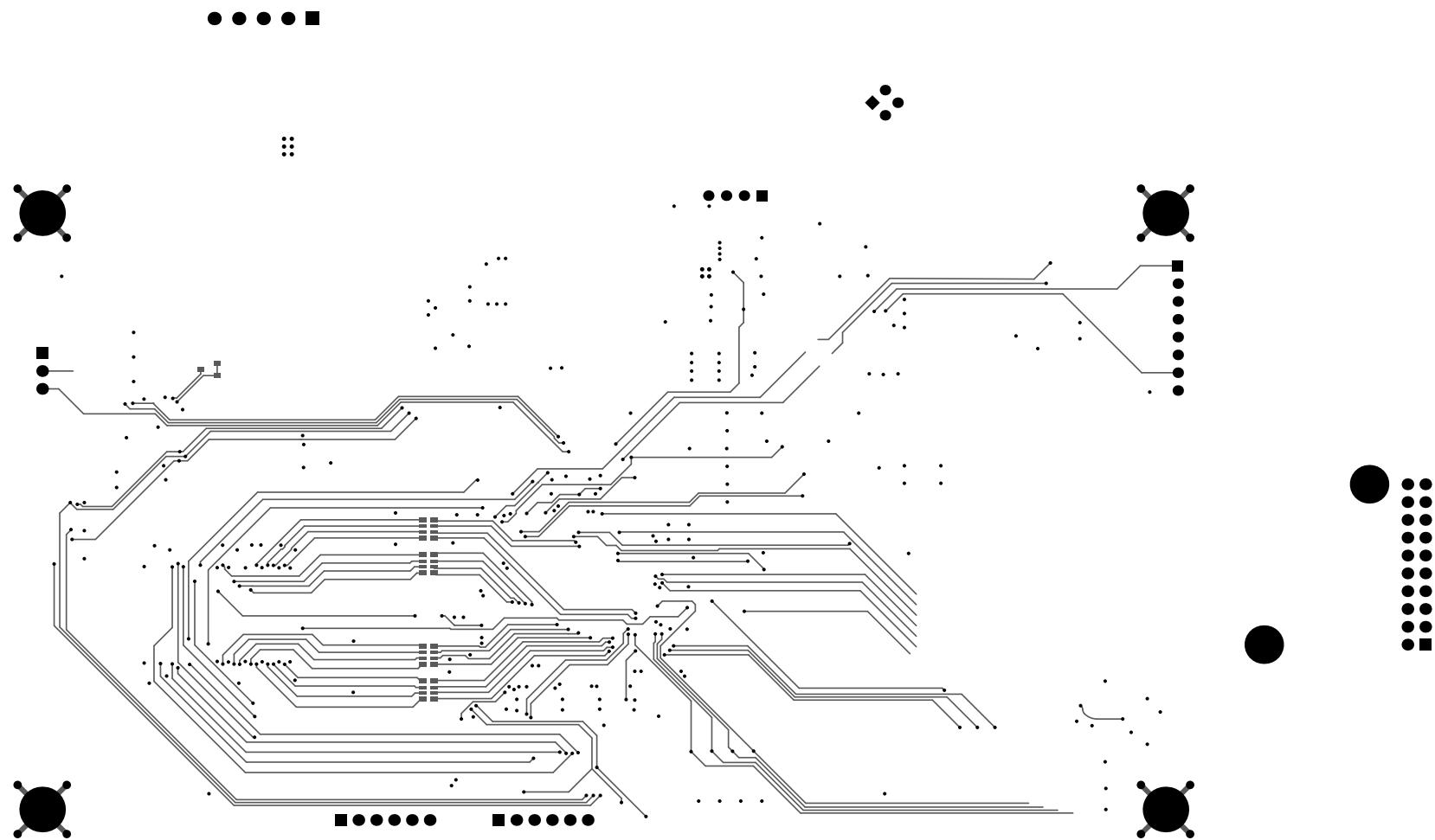


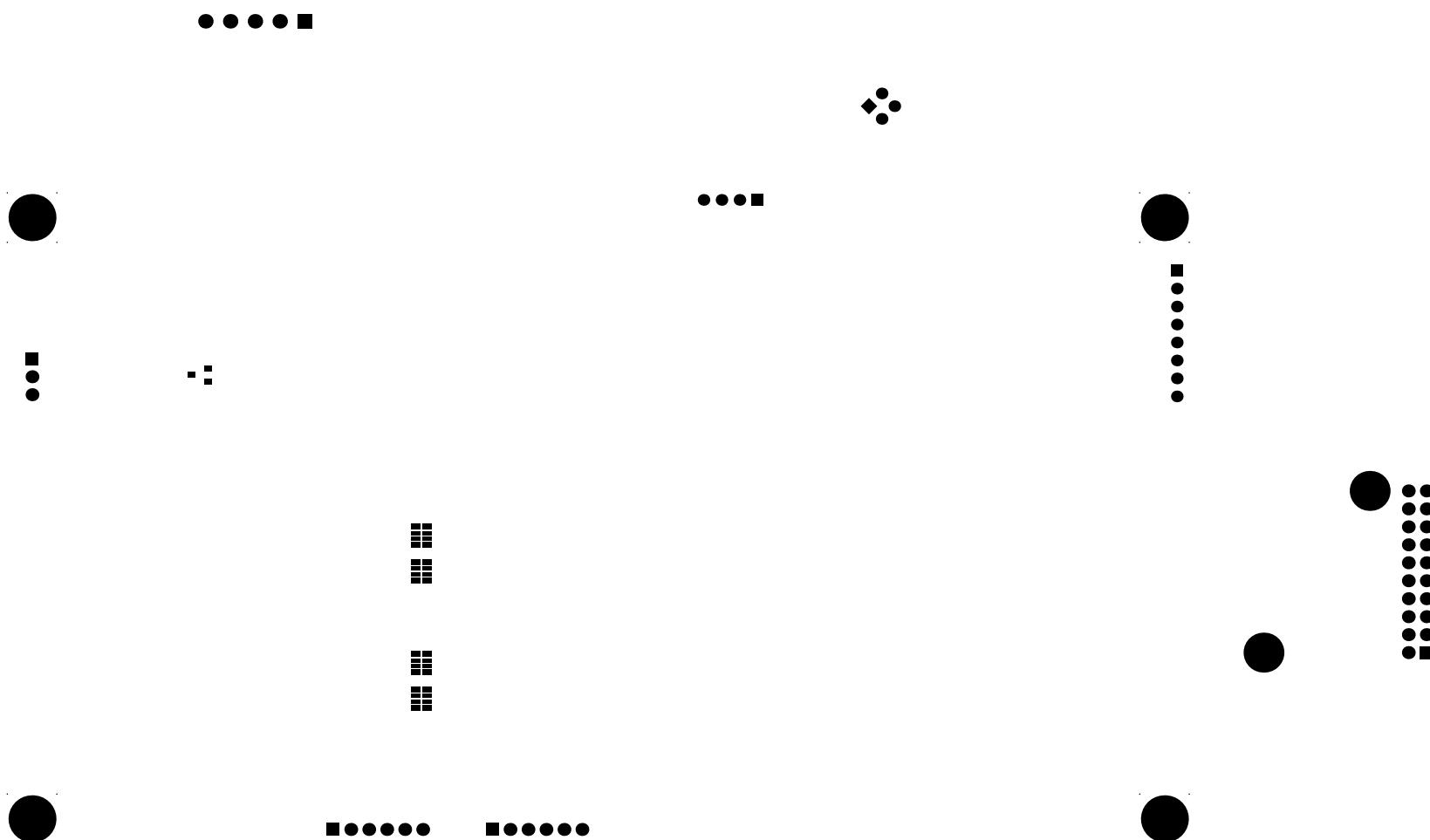
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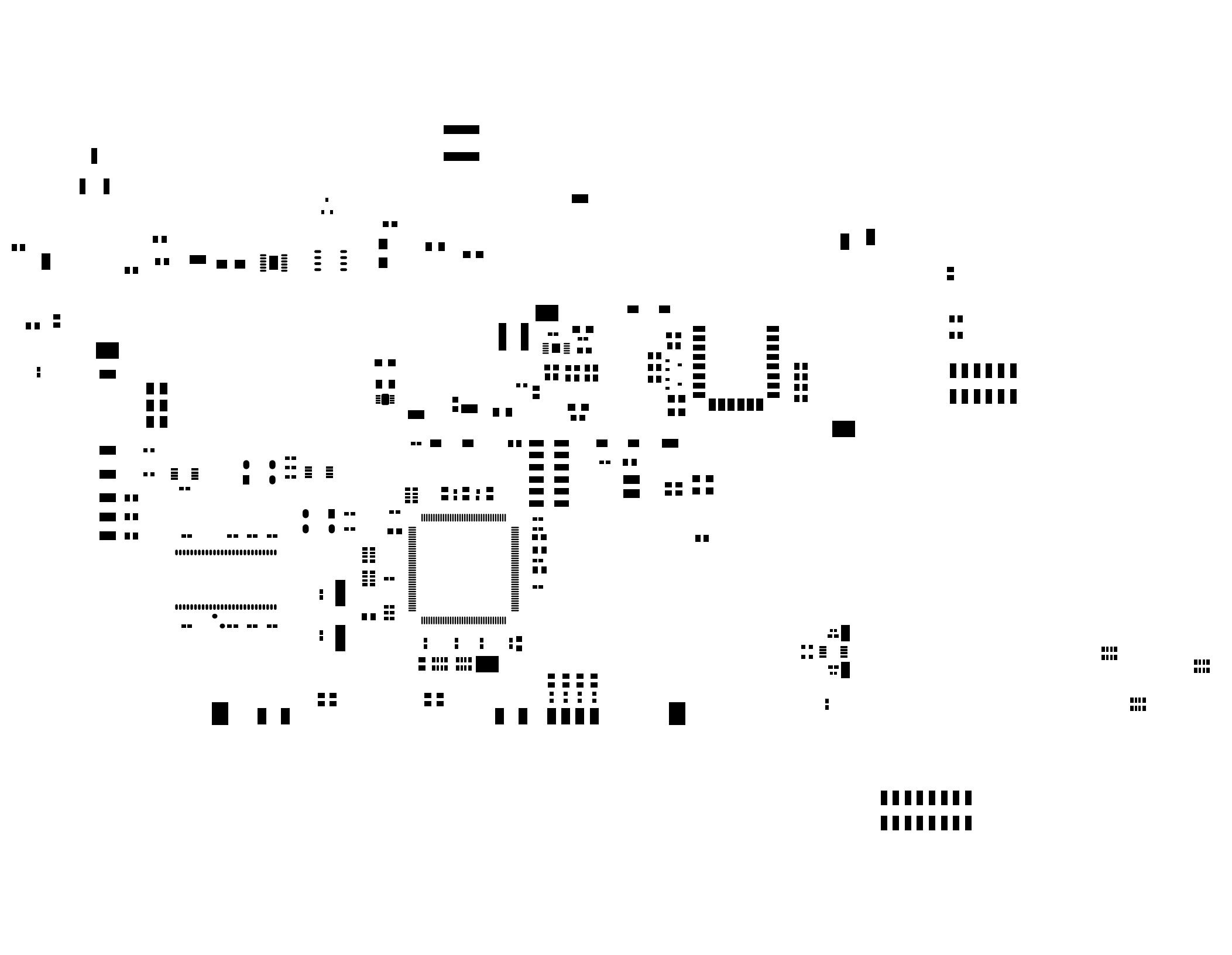
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0300

RR508
RR504

RR503
RR506

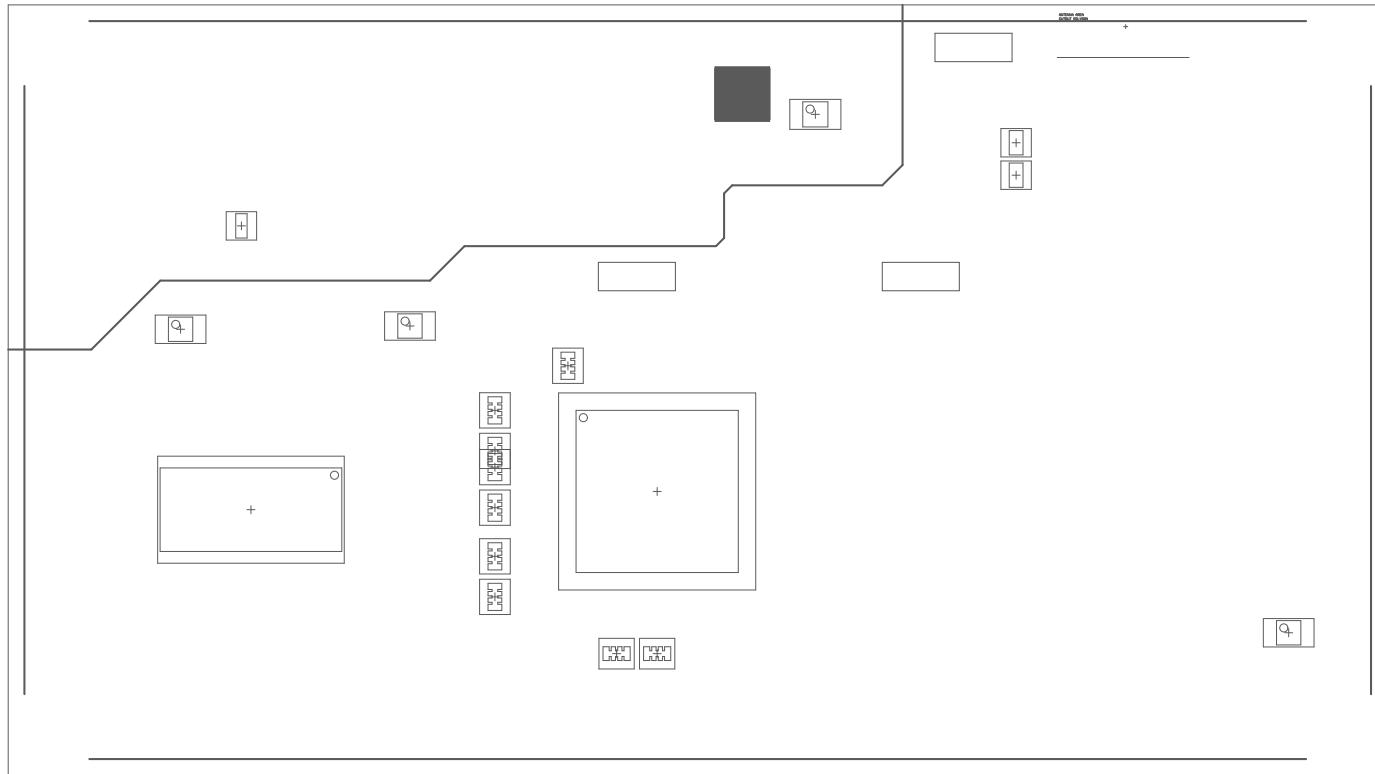
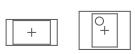
AKIRA YOUNGERLOOD
JEREMY Rapp
TAYLOR Neuyen
JEFFERY Tim
Ben HEBREIN



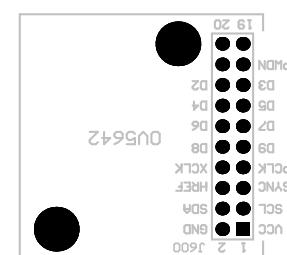
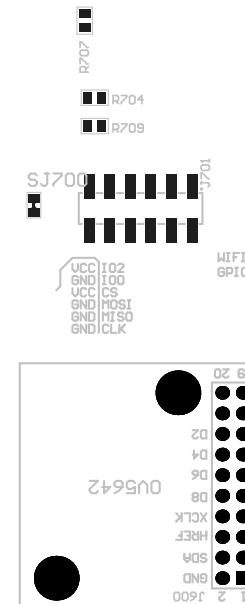
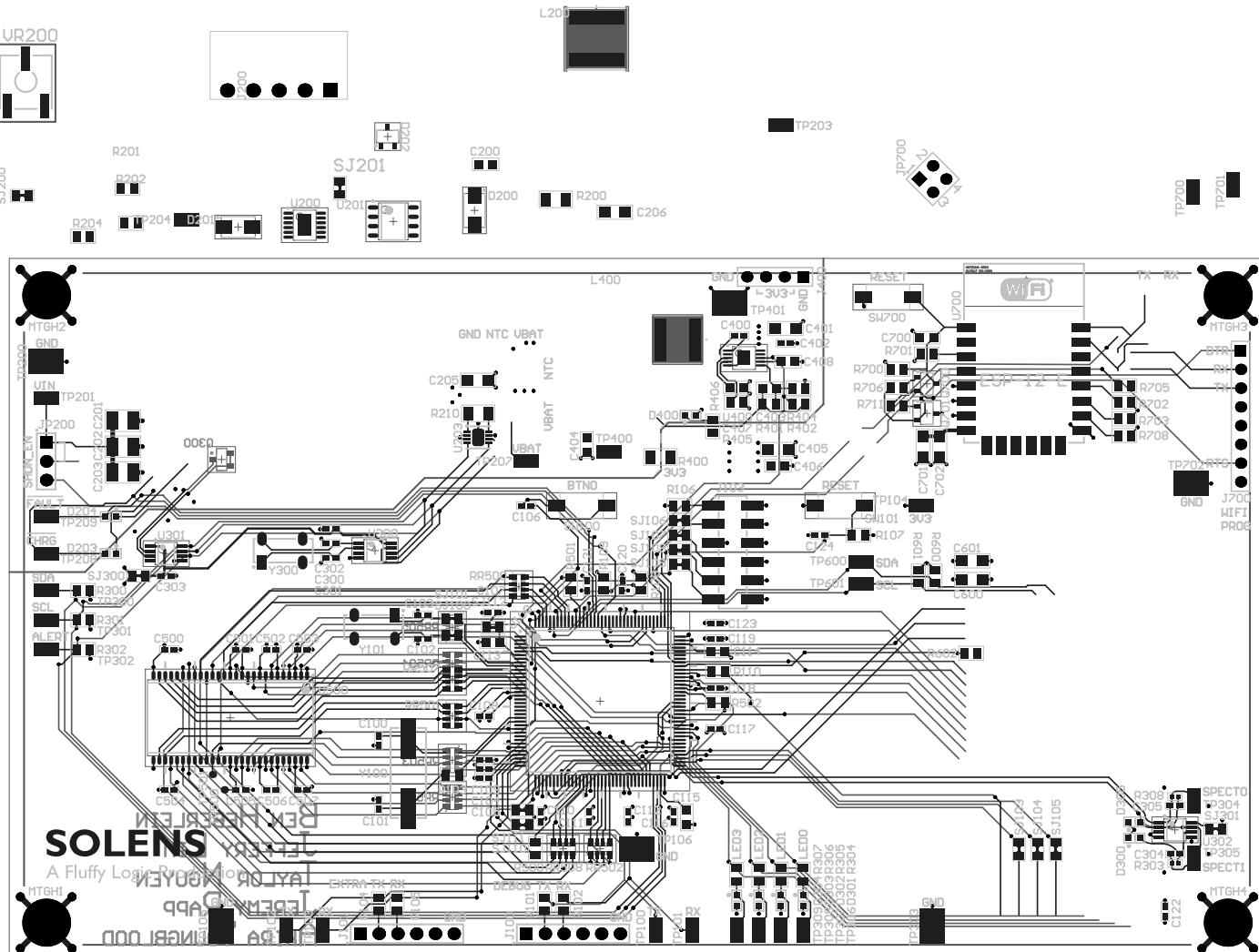


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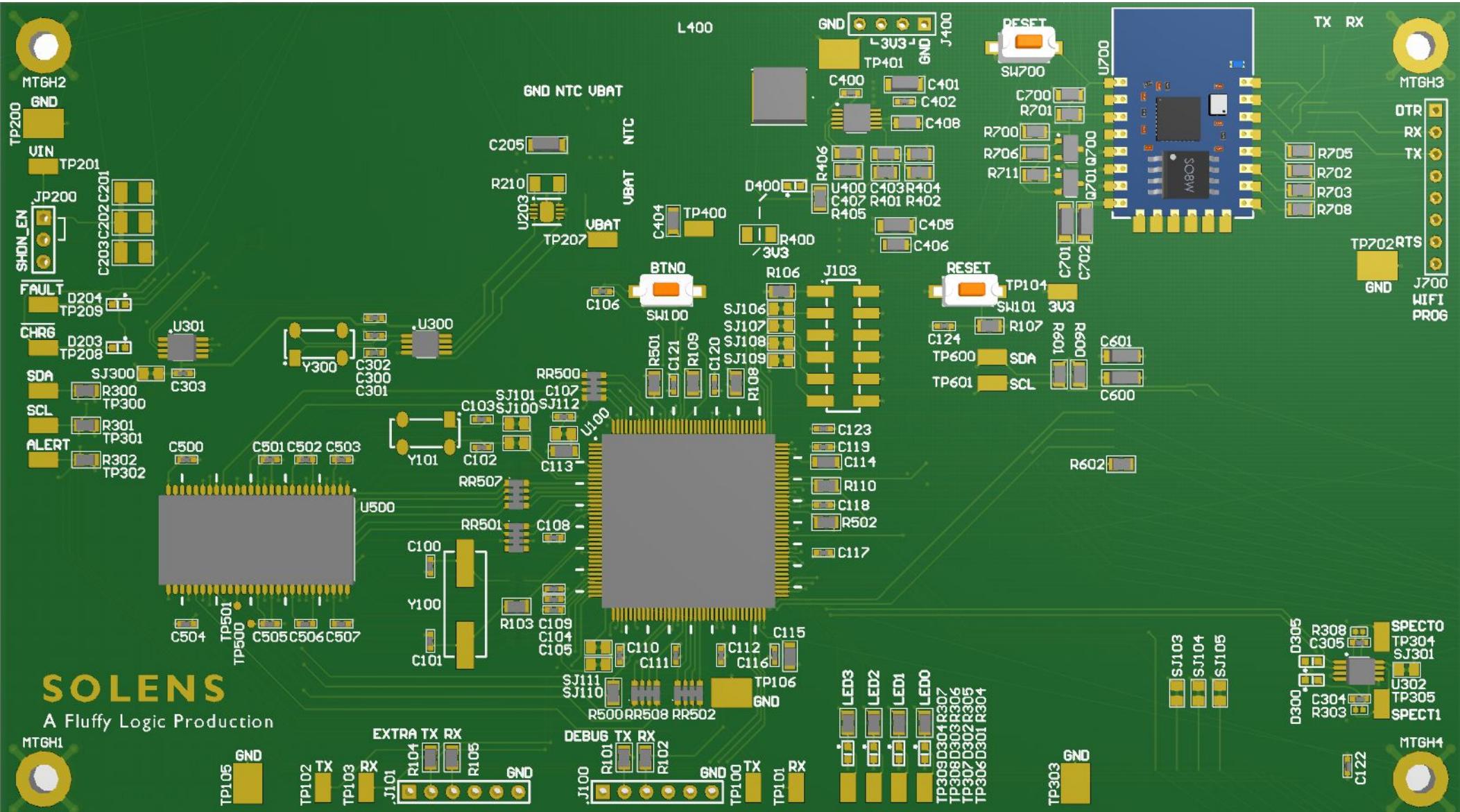


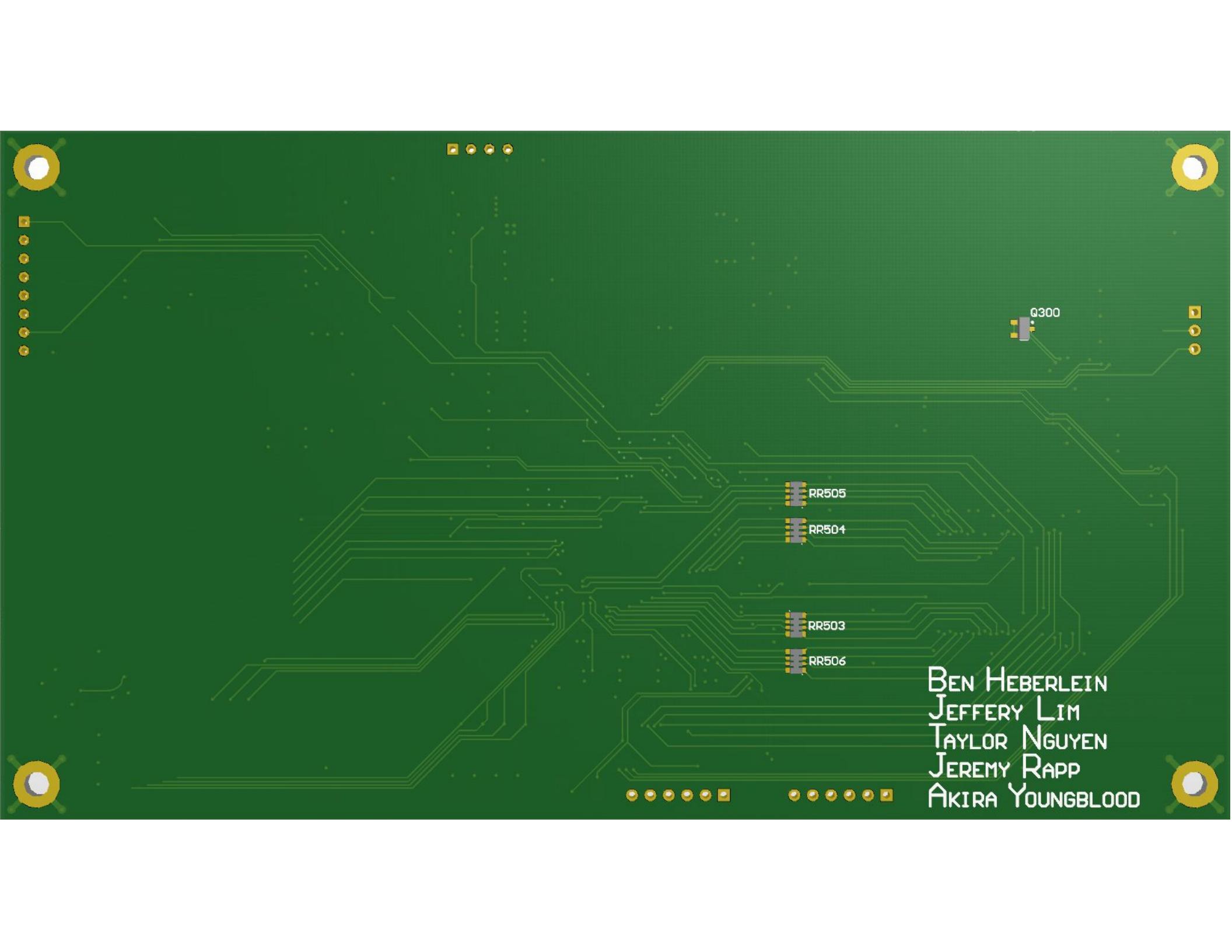






GPIO	
MC02	GND
PB13	GND
PB14	GND
PB15	GND
LEDO	3V3
LED1	GND
LED2	3V3
LED3	GND





BEN HEBERLEIN
JEFFERY LIM
TAYLOR NGUYEN
JEREMY RAPP
AKIRA YOUNGBLOOD

RR505

RR504

RR503

RR506

Q300