Electrical Rules Check Report

Class	Document	Message
Warning	Solens.SchDoc	Nets Wire I2C2_ALERT has multiple names (Net Label I2C2_ALERT,Net Label PERIPH_ALERT,Sheet Entry Z1-PERIPH_ALERT(I/O),Sheet Entry Z2-FUEL_AL_L(I/O),Sheet Entry Z3-A\L\E\R\T\(I/O))
Warning	Solens.SchDoc	Nets Wire I2C2_SCL has multiple names (Net Label I2C2_SCL,Net Label PERIPH_SCL,Sheet Entry Z1-PERIPH_SCL(I/O),Sheet Entry Z2-SCL(I/O),Sheet Entry Z3-SCL(I/O))
Warning	Solens.SchDoc	Nets Wire I2C2_SDA has multiple names (Net Label I2C2_SDA,Net Label PERIPH_SDA,Sheet Entry Z1-PERIPH_SDA(I/O),Sheet Entry Z2-SDA(I/O),Sheet Entry Z3-SDA(I/O))
Warning	Solens.SchDoc	Nets Wire PERIPH_ALERT has multiple names (Sheet Entry Z1-PERIPH_ALERT(I/O),Sheet Entry Z2-FUEL_AL_L(I/O),Sheet Entry Z3-A\L\E\R\T\(I/O))
Warning	Solens.SchDoc	Nets Wire PERIPH_SCL has multiple names (Sheet Entry Z1-PERIPH_SCL(I/O),Sheet Entry Z2-SCL(I/O),Sheet Entry Z3-SCL(I/O))
Warning	Solens.SchDoc	Nets Wire PERIPH_SDA has multiple names (Sheet Entry Z1-PERIPH_SDA(I/O),Sheet Entry Z2-SDA(I/O),Sheet Entry Z3-SDA(I/O))
Warning	Solens.SchDoc	Nets Wire PWR_CHRG_L has multiple names (Net Label PWR_CHRG_L,Sheet Entry Z1-PV_CHRG_L(Input),Sheet Entry Z2-PV_CHRG_L(Output))
Warning	Solens.SchDoc	Nets Wire PWR_FAULT_L has multiple names (Net Label PWR_FAULT_L,Sheet Entry Z1-PV_FAULT_L(Input),Sheet Entry Z2-PV_FAULT_L(Output))

Design Rules Verification Report

Filename : C:\Users\qux\projects\solenshardware\Altium\Solens\Solens.PcbDoc

Warnings 4
Rule Violations 31

Warnings	
Unplated multi-layer pad(s) detected	4
Total	4

Rule Violations	
Room Z6 (Bounding Region = (6533.072mil, 6040.945mil, 7911.024mil, 7306.299mil)	0
Width Constraint (Min=8mil) (Max=120mil) (Preferred=8mil) (InComponent('MTGH*'))	0
Short-Circuit Constraint (Allowed=Yes) (InComponent('MTGH*') And (IsFill Or IsPad Or IsTrack)),(InComponent('MTG*')	0
Short-Circuit Constraint (Allowed=Yes) (InComponent('SJ*') And (IsFill Or IsPad Or IsTrack)),(InComponent('SJ*') And	0
Clearance Constraint (Gap=0mil) (InComponent('SJ*') And (IsFill Or IsPad Or IsTrack)),(InComponent('SJ*') And (IsFill	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Net Antennae (Tolerance=0mil) (All)	2
Silk to Silk (Clearance=5mil) (All),(All)	20
Silk To Solder Mask (Clearance=2mil) (IsPad),(All)	2
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Hole Size Constraint (Min=8mil) (Max=250mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Component Clearance Constraint (Horizontal Gap = 1mil, Vertical Gap = 10mil) (All),(All)	0
Width Constraint (Min=7mil) (Max=12mil) (Preferred=8mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Clearance Constraint (Gap=8mil) (All),(All)	0
Un-Routed Net Constraint ((All))	7
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Width Constraint (Min=8mil) (Max=64mil) (Preferred=8mil) (InNetClass('PWR'))	0
Width Constraint (Min=8mil) (Max=64mil) (Preferred=8mil) (InNetClass('HVY'))	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil)	0
Room Z7 (Bounding Region = (5794.882mil, 7369.685mil, 7911.024mil, 8698.424mil)	0
Room Z1 (Bounding Region = (2300.787mil, 7664.961mil, 4416.929mil, 8698.425mil)	0
Room Z2 (Bounding Region = (4416.929mil, 8058.661mil, 5794.882mil, 8698.424mil)	0
Total	31

Unplated multi-layer pad(s) detected
Pad MTGH4-1(3937.008mil,196.85mil) on Multi-Layer on Net GND
Pad MTGH3-1(5314.961mil,2559.055mil) on Multi-Layer on Net GND
Pad MTGH2-1(196.85mil,2559.055mil) on Multi-Layer on Net GND
Pad MTGH1-1(196.85mil,196.85mil) on Multi-Layer on Net GND

Net Antennae (Tolerance=0mil) (All)
Net Antennae: Track (1235.236mil,1125.984mil)(1373.032mil,988.189mil) on Bottom Layer
Net Antennae: Track (5046.071mil,1512.606mil)(5190.01mil,1512.606mil) on Top Layer

Silk to Silk (Clearance=5mil) (All),(All)
Silk To Silk Clearance Constraint: (4.912mil < 5mil) Between Text "C700" (3618.11mil,2358.268mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (3.833mil < 5mil) Between Text "C700" (3618.11mil,2358.268mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (4.896mil < 5mil) Between Text "C121" (2956.693mil,1614.173mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (4.896mil < 5mil) Between Text "C121" (2956.693mil,1614.173mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (4.529mil < 5mil) Between Text "C116" (3298.228mil,431.102mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (4.529mil < 5mil) Between Text "C116" (3298.228mil,431.102mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (4.563mil < 5mil) Between Text "C407" (2295.276mil,2192.913mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.592mil < 5mil) Between Text "C402" (2791.339mil,2314.961mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (4.529mil < 5mil) Between Text "C401" (2795.276mil,2263.754mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.592mil < 5mil) Between Text "C402" (2791.339mil,2314.961mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (4.832mil < 5mil) Between Text "ALERT" (88.583mil,1082.677mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 5mil) Between Text "C116" (3298.228mil,431.102mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (3.998mil < 5mil) Between Text "C112" (3169.29mil,425.198mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (3.378mil < 5mil) Between Text "PWDN" (4979.331mil,1049.961mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (4.073mil < 5mil) Between Text "D3" (5049.331mil,949.961mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (3.771mil < 5mil) Between Text "D5" (5049.331mil,844.961mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (3.889mil < 5mil) Between Text "140 MM" (2885.827mil,665.354mil) on Bottom Overlay And Track
Silk To Silk Clearance Constraint: (4.821mil < 5mil) Between Text "VFB" (1202.464mil,2067.311mil) on Bottom Overlay And Track
Silk To Silk Clearance Constraint: (4.821mil < 5mil) Between Text "RF3" (1202.464mil,2000.126mil) on Bottom Overlay And Track
Silk To Silk Clearance Constraint: (2.561mil < 5mil) Between Text "C402" (2791.339mil,2314.961mil) on Top Overlay And Text "C401"

Silk To Solder Mask (Clearance=2mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (Collision < 2mil) Between Track (3937.008mil,2411.417mil)(4724.409mil,2411.417mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 2mil) Between Track (3937.008mil,2411.417mil)(4724.409mil,2411.417mil) on Top Overlay And Pad

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Net GND Between Pad U302-4(3891.732mil,1375mil) on Top Layer And Pad U302-5(4064.961mil,1375mil) on Top Layer
Un-Routed Net Constraint: Unplated Pad MTGH1-1(196.85mil,196.85mil) on Multi-Layer
Un-Routed Net Constraint: Unplated Pad MTGH2-1(196.85mil,2559.055mil) on Multi-Layer
Un-Routed Net Constraint: Unplated Pad MTGH3-1(5314.961mil,2559.055mil) on Multi-Layer
Un-Routed Net Constraint: Unplated Pad MTGH4-1(3937.008mil,196.85mil) on Multi-Layer
Un-Routed Net Constraint: Net SD_NWE_T Between Track (1235.236mil,1125.984mil)(1373.032mil,988.189mil) on Bottom Layer And Via
Un-Routed Net Constraint: Net VBAT_INT Between Track (1093.504mil,2233.268mil)(1093.504mil,2265.748mil) on Signal Layer 2 And Pad