

Electrical Rules Check Report

Class	Document	Message
Warning	Solens.SchDoc	Nets Wire FUEL_AL_L has multiple names (Sheet Entry Z1-FUEL_AL_L(I/O),Sheet Entry Z4-PERIPH_ALERT(I/O),Sheet Entry Z5-ALIVE\RTV(I/O))
Warning	Solens.SchDoc	Nets Wire I2C2_ALERT has multiple names (Net Label I2C2_ALERT,Net Label PERIPH_ALERT,Sheet Entry Z1-FUEL_AL_L(I/O),Sheet Entry Z4-PERIPH_ALERT(I/O),Sheet Entry Z5-ALIVE\RTV(I/O))
Warning	Solens.SchDoc	Nets Wire I2C2_SCL has multiple names (Net Label I2C2_SCL,Net Label PERIPH_SCL,Sheet Entry Z1-SCL(I/O),Sheet Entry Z4-PERIPH_SCL(I/O),Sheet Entry Z5-SCL(I/O))
Warning	Solens.SchDoc	Nets Wire I2C2_SDA has multiple names (Net Label I2C2_SDA,Net Label PERIPH_SDA,Sheet Entry Z1-SDA(I/O),Sheet Entry Z4-PERIPH_SDA(I/O),Sheet Entry Z5-SDA(I/O))
Warning	Solens.SchDoc	Nets Wire PWR_CHRG_L has multiple names (Net Label PWR_CHRG_L,Sheet Entry Z1-PV_CHRG_L(Output),Sheet Entry Z4-PV_CHRG_L(Input))
Warning	Solens.SchDoc	Nets Wire PWR_FAULT_L has multiple names (Net Label PWR_FAULT_L,Sheet Entry Z1-PV_FAULT_L(Output),Sheet Entry Z4-PV_FAULT_L(Input))
Warning	Solens.SchDoc	Nets Wire SCL has multiple names (Sheet Entry Z1-SCL(I/O),Sheet Entry Z4-PERIPH_SCL(I/O),Sheet Entry Z5-SCL(I/O))
Warning	Solens.SchDoc	Nets Wire SDA has multiple names (Sheet Entry Z1-SDA(I/O),Sheet Entry Z4-PERIPH_SDA(I/O),Sheet Entry Z5-SDA(I/O))

Design Rules Verification Report

Filename : C:\Users\qux\projects\solenshardware\Altium\Solens\Solens.PcbDoc

Warnings 6
Rule Violations 500

Warnings	
Your board contains 2 shelved polygons - copper connectivity will not be reported correctly. Unshelve polygons and	2
Unplated multi-layer pad(s) detected	4
Total	6

Rule Violations	
Width Constraint (Min=8mil) (Max=120mil) (Preferred=8mil) (InComponent("MTGH**"))	0
Short-Circuit Constraint (Allowed=Yes) (InComponent("MTGH**") And (IsFill Or IsPad Or IsTrack)),(InComponent("MTG**"))	0
Room Z6 (Bounding Region = (6641.339mil, 5696.457mil, 7468.11mil, 7035.039mil) (InComponentClass("Z6"))	0
Short-Circuit Constraint (Allowed=Yes) (InComponent("SJ**") And (IsFill Or IsPad Or IsTrack)),(InComponent("SJ**") And	0
Clearance Constraint (Gap=0mil) (InComponent("SJ**") And (IsFill Or IsPad Or IsTrack)),(InComponent("SJ**") And (IsFill	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Net Antennae (Tolerance=0mil) (All)	0
Silk to Silk (Clearance=8mil) (All),(All)	1
Silk To Solder Mask (Clearance=8mil) (IsPad),(All)	417
Minimum Solder Mask Sliver (Gap=6mil) (All),(All)	82
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Hole Size Constraint (Min=12mil) (Max=250mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Width Constraint (Min=7mil) (Max=12mil) (Preferred=8mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Clearance Constraint (Gap=8mil) (All),(All)	0
Un-Routed Net Constraint (All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Room Z2 (Bounding Region = (5302.756mil, 7468.11mil, 6680.709mil, 8688.583mil) (InComponentClass("Z2"))	0
Width Constraint (Min=8mil) (Max=64mil) (Preferred=8mil) (InNetClass("PWR"))	0
Width Constraint (Min=8mil) (Max=64mil) (Preferred=8mil) (InNetClass("HVV"))	0
Room Z1 (Bounding Region = (2350mil, 6975.984mil, 5224.016mil, 8688.583mil) (InComponentClass("Z1"))	0
Room Z7 (Bounding Region = (6779.134mil, 7172.835mil, 9042.913mil, 8688.583mil) (InComponentClass("Z7"))	0
Total	500

Your board contains 2 shelved polygons - copper connectivity will not be reported correctly. Unshelve polygons and re	
Polygon named: 3V3 Plane 1 In net 3V3 On Signal Layer 2	
Polygon named: GND Plane In net GND On Signal Layer 1	

Unplated multi-layer pad(s) detected	
Pad MTGH3-1(6496.063mil,3543.307mil) on Multi-Layer on Net GND	
Pad MTGH2-1(196.85mil,3543.307mil) on Multi-Layer on Net GND	
Pad MTGH1-1(196.85mil,196.85mil) on Multi-Layer on Net GND	
Pad MTGH4-1(6496.063mil,196.85mil) on Multi-Layer on Net GND	

Silk to Silk (Clearance=8mil) (All),(All)	
Silk To Silk Clearance Constraint: (5.151mil < 8mil) Between Text "C304" (4481.299mil,387.795mil) on Top Overlay And Arc (4476.378mil,455.709mil) on	

[illegible]

Silk To Solder Mask (Clearance=8mil) (IsPad),(All)

[illegible]

[illegible]

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Silk To Solder Mask (Clearance=8mil) (IsPad),(All)

[illegible]

Silk To Solder Mask (Clearance=8mil) (IsPad),(All)

[illegible]

[illegible]

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[illegible]

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Silk To Solder Mask (Clearance=8mil) (IsPad), (All)

Silk To Solder Mask Clearance Constraint: (Collision < 8mil) Between Text "U100" (2696.85mil, 1771.654mil) on Top Overlay And Pad

Minimum Solder Mask Sliver (Gap=6mil) (All),(All)
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-123(3218.504mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-122(3238.189mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-121(3257.874mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-120(3277.559mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-119(3297.244mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-118(3316.929mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-117(3336.614mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-116(3356.299mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-115(3375.984mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-114(3395.669mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-113(3415.354mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-112(3435.039mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-111(3454.724mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-110(3474.41mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-109(3494.095mil, 1804.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-107(3575.787mil, 1702.756mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-106(3575.787mil, 1683.071mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-105(3575.787mil, 1663.386mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-104(3575.787mil, 1643.701mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-103(3575.787mil, 1624.016mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-102(3575.787mil, 1604.331mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-101(3575.787mil, 1584.646mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-100(3575.787mil, 1564.961mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-99(3575.787mil, 1545.276mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-98(3575.787mil, 1525.591mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-97(3575.787mil, 1505.906mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-96(3575.787mil, 1486.22mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-95(3575.787mil, 1466.535mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-94(3575.787mil, 1446.85mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.071mil < 6mil) Between Pad U100-93(3575.787mil, 1427.165mil) on Top Layer And Pad