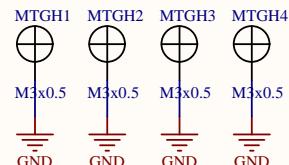
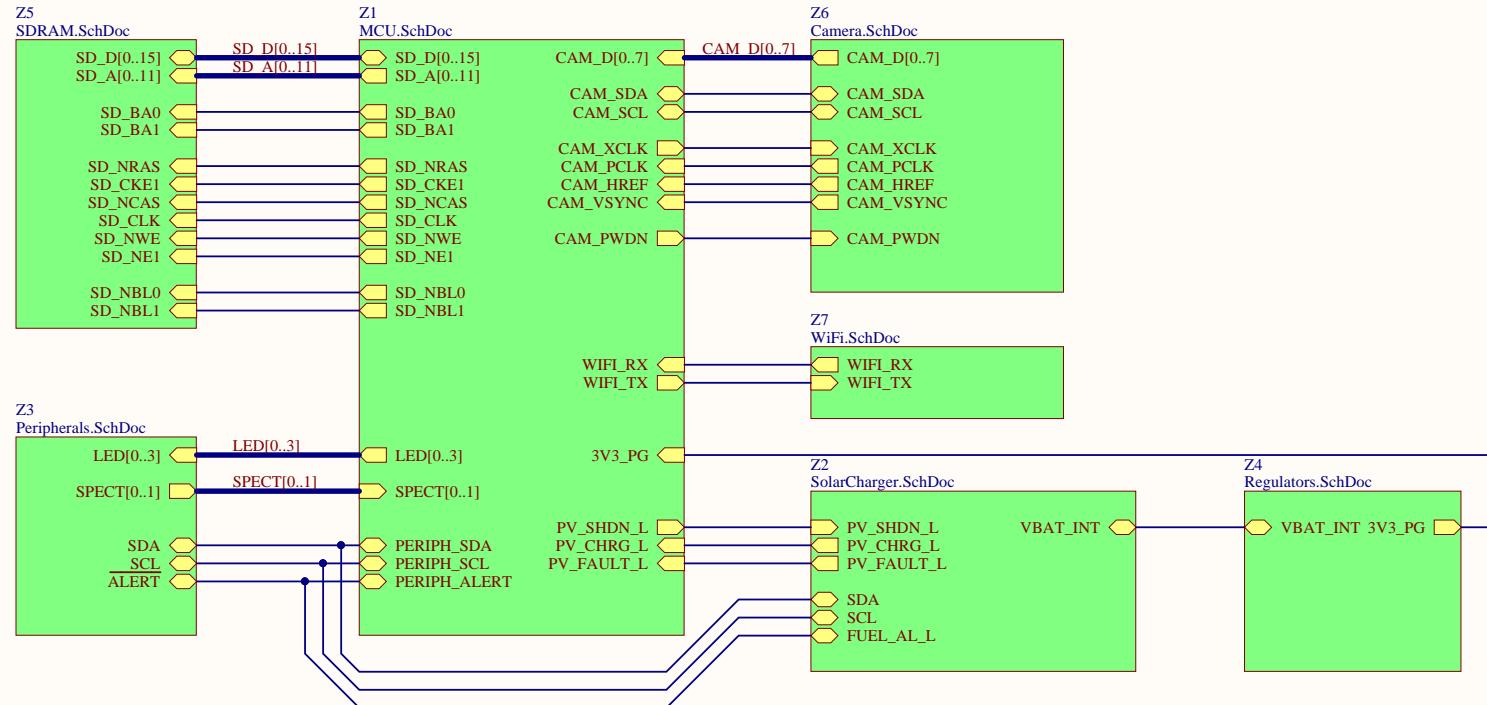


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Title

Solens Camera Subsystem
ERC_WARN, FOOTPRINT_N/A

Size

A4

Number

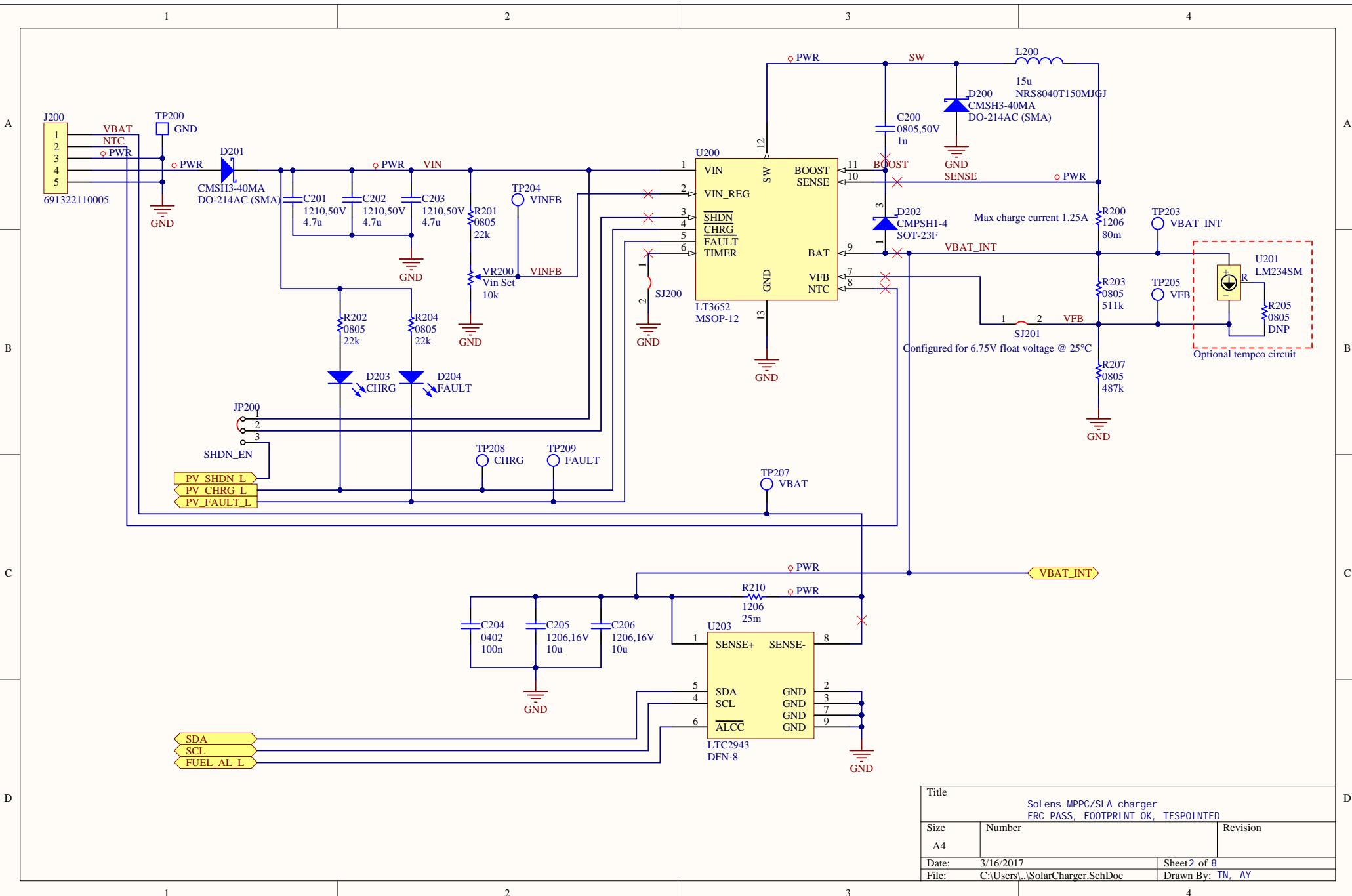
Revision

Date: 3/16/2017

Sheet 1 of 8

File: C:\Users\..\Solens.SchDoc

Drawn By: JL, AY



A

A

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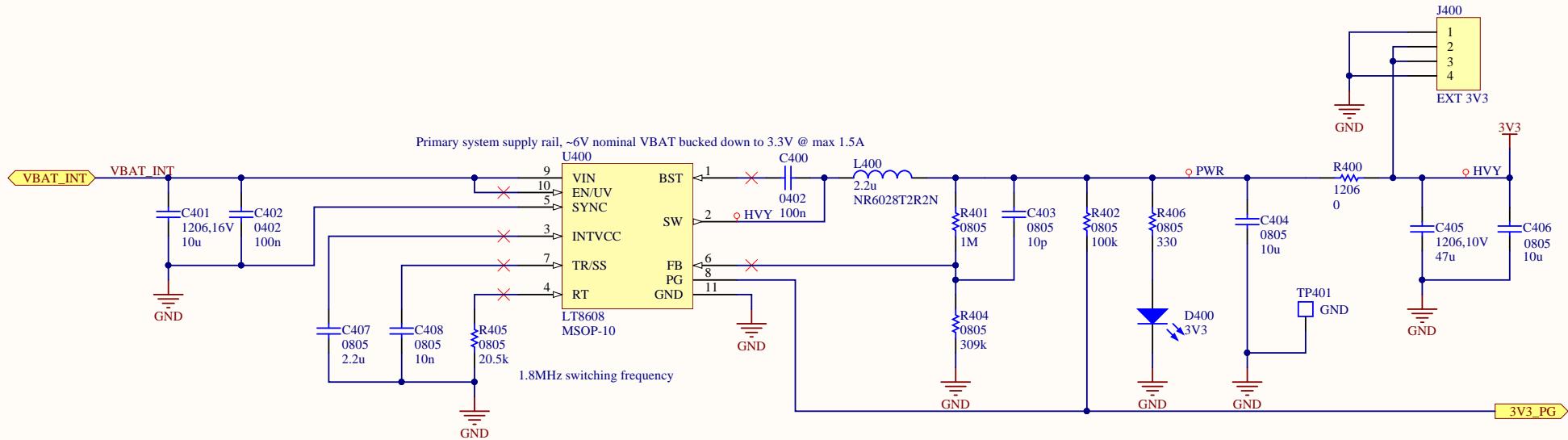
B

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D



Title		
Solens Voltage Regulators		ERC PASS, FOOTPRINT OK, TESPOINTED
Size		Revision
A4		
Date:	3/16/2017	Sheet 3 of 8
File:	C:\Users...\Regulators.SchDoc	Drawn By: TN, AY

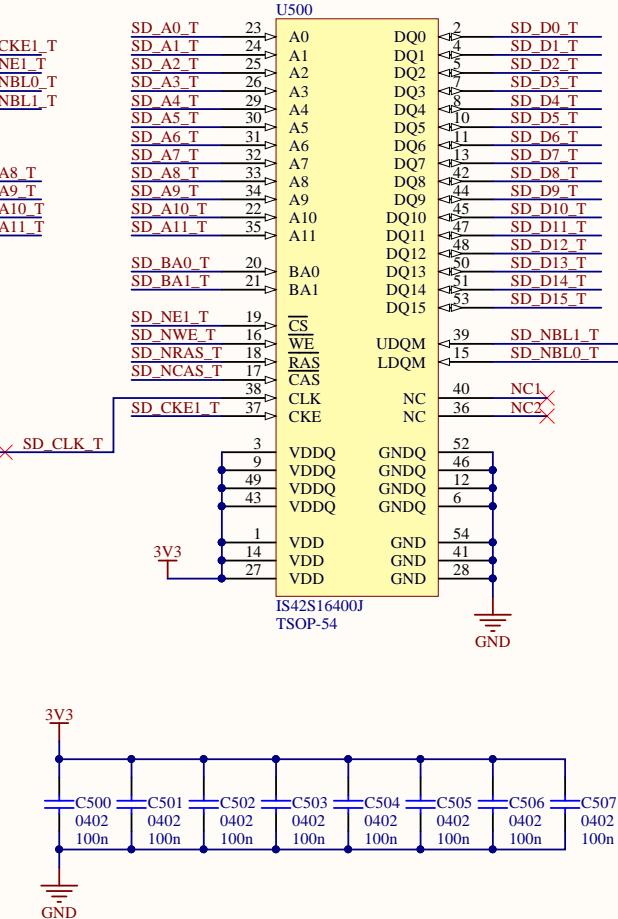
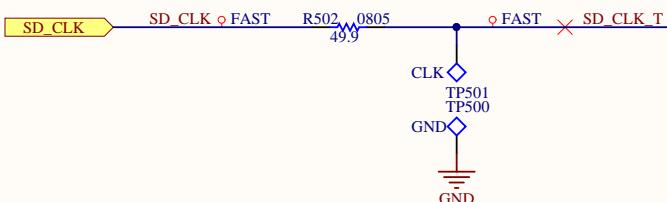
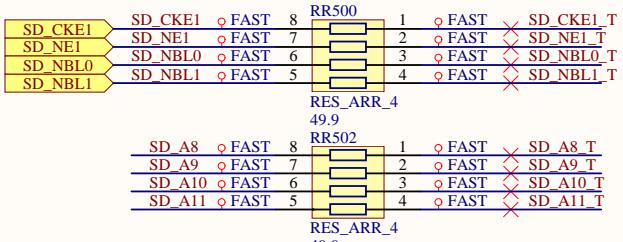
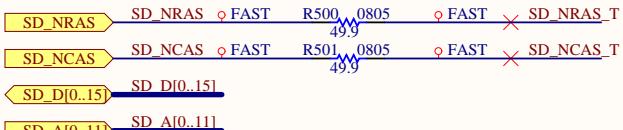
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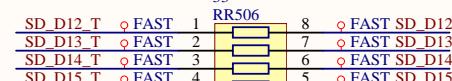
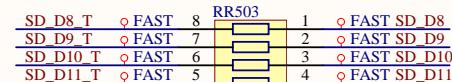
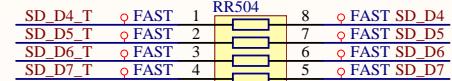
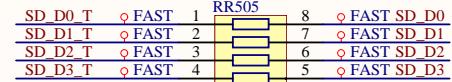
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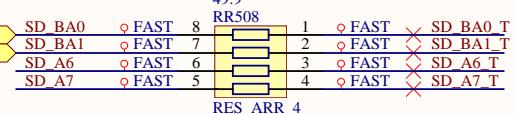
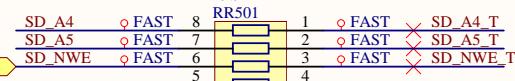
A



DATA termination to be placed halfway between MCU and RAM



ADDR and CLK termination to be placed at MCU



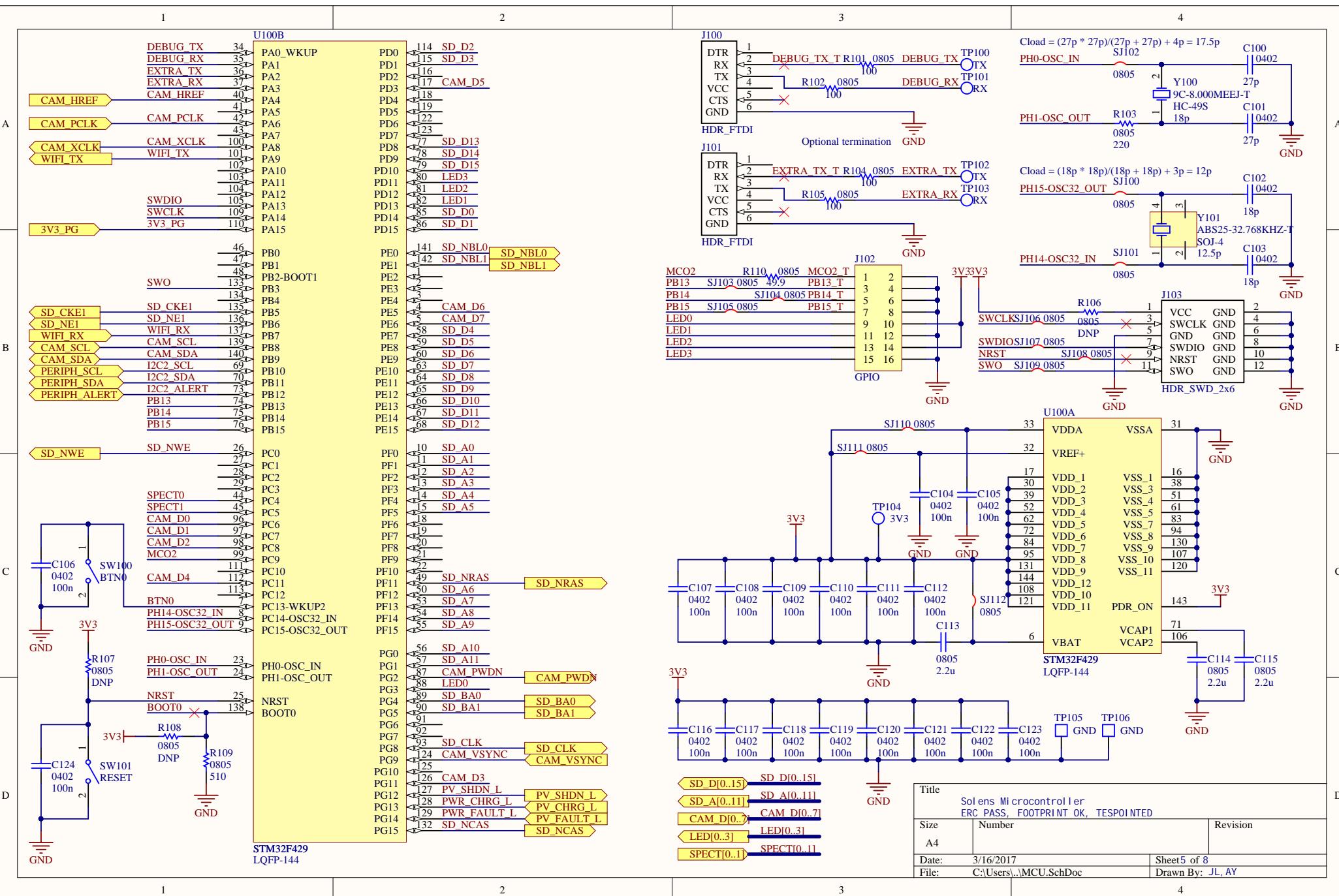
Title		
Solens_SDRAM		
Size	Number	Revision
A4		
Date:	3/16/2017	Sheet 4 of 8
File:	C:\Users\...\SDRAM.SchDoc	Drawn By: JL, AY

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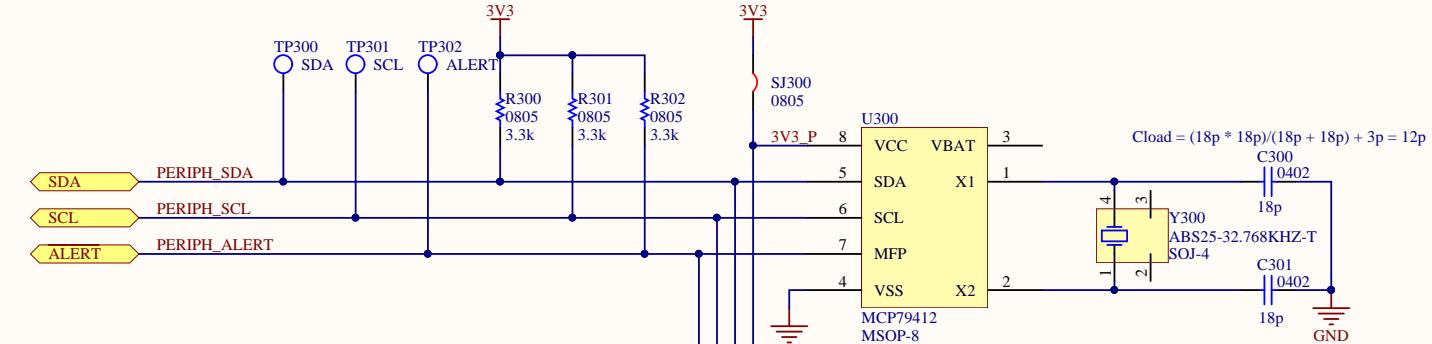
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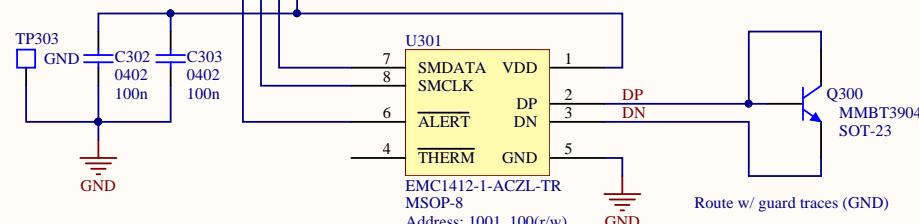
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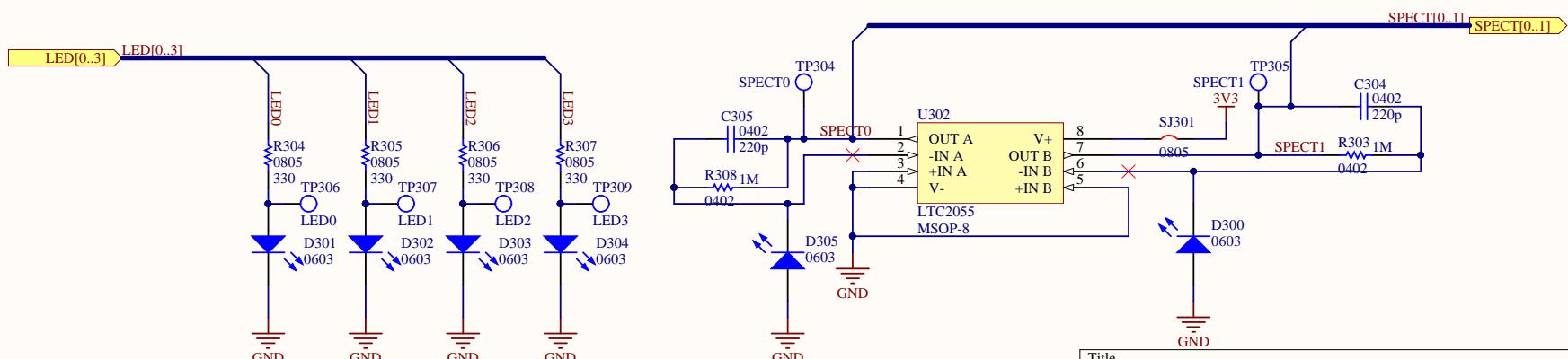
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Title		
Solens Peripherals ERC PASS, FOOTPRINT OK, TESPOINTED		
Size	Number	Revision
A4		
Date: 3/16/2017	Sheet 6 of 8	
File: C:\Users...\Peripherals.SchDoc		Drawn By: AY

1

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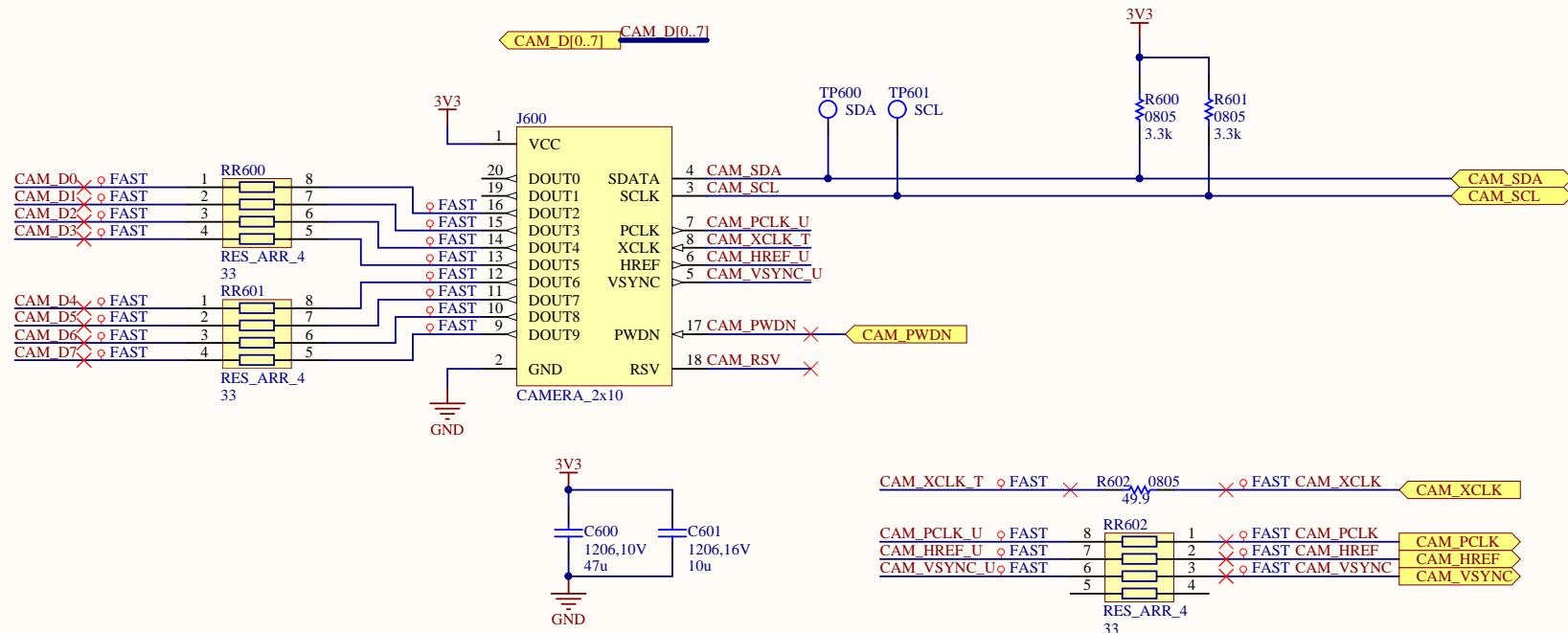
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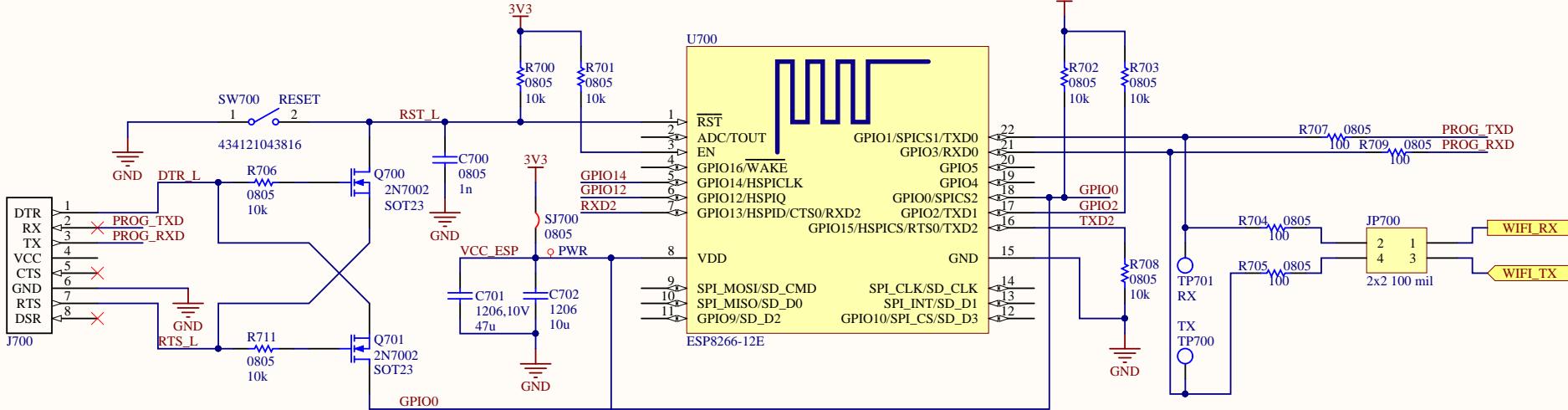
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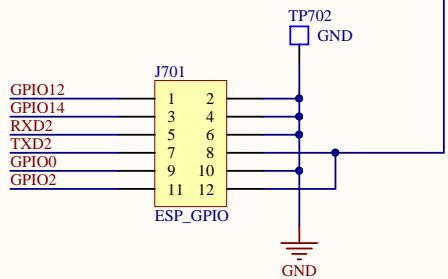


Title		
Solens Camera Subsystem ERC PASS, FOOTPRINT OK, TESTPOINTED		
Size	Number	Revision
A4		
Date:	3/16/2017	Sheet 7 of 8
File:	C:\Users\...\Camera.SchDoc	Drawn By: JL, AY

A

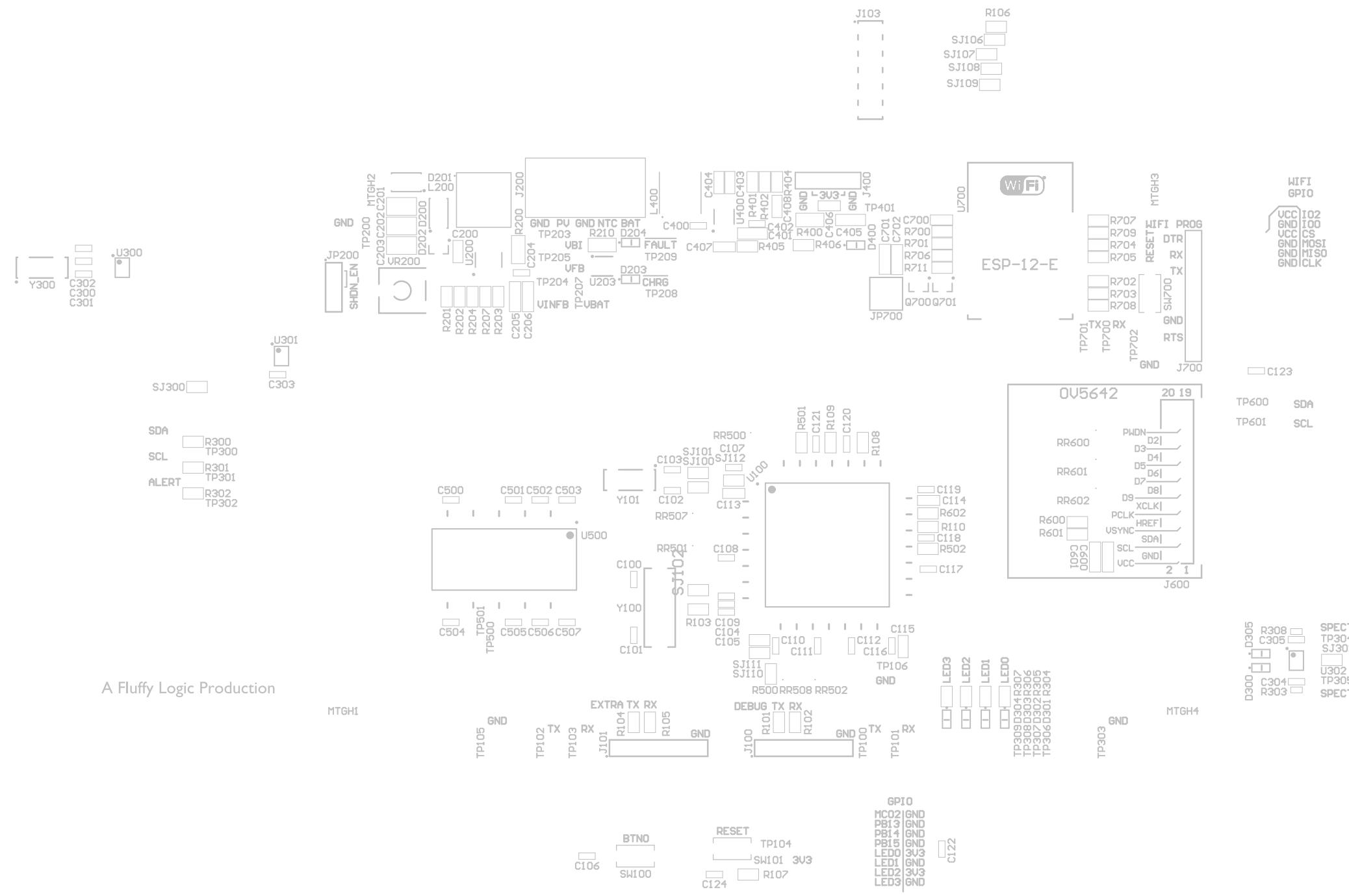


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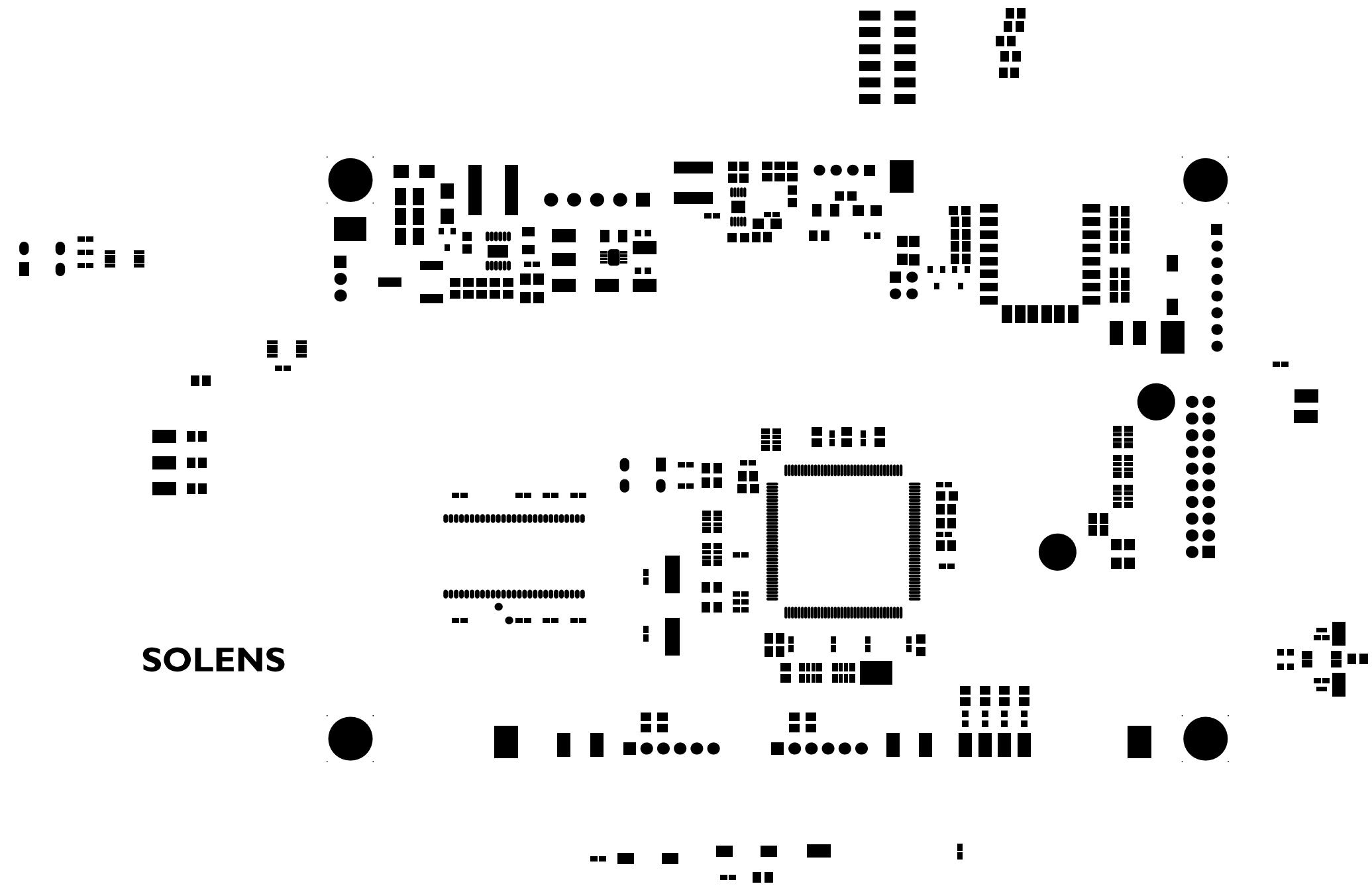


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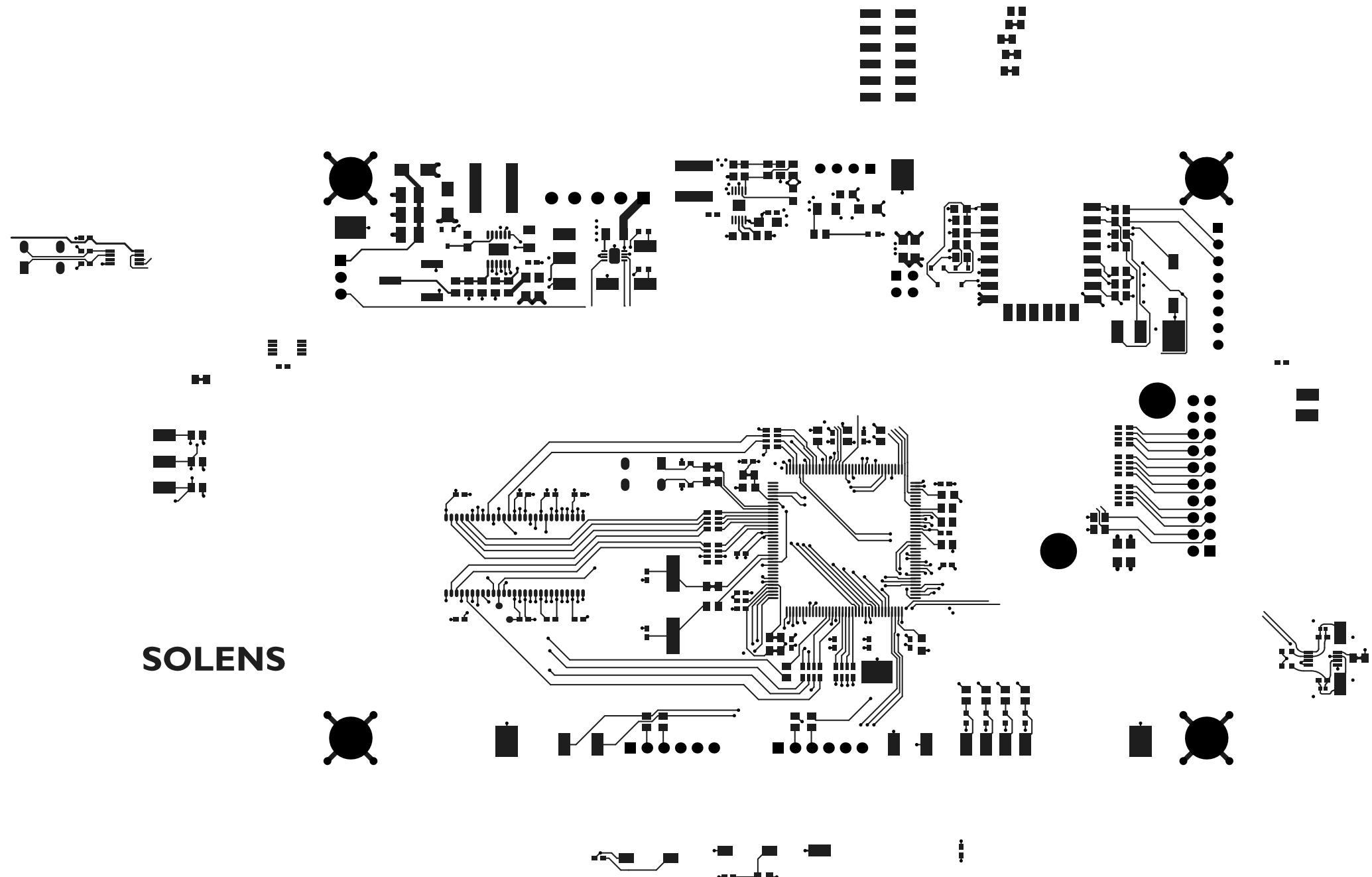
Title		
Solens WiFi Subsystem ERC PASS, FOOTPRINT OK, TESTPOINTED		Revision
Size	Number	
A4		
Date:	3/16/2017	Sheet 8 of 8
File:	C:\Users\...\WiFi.SchDoc	Drawn By: JL, AY

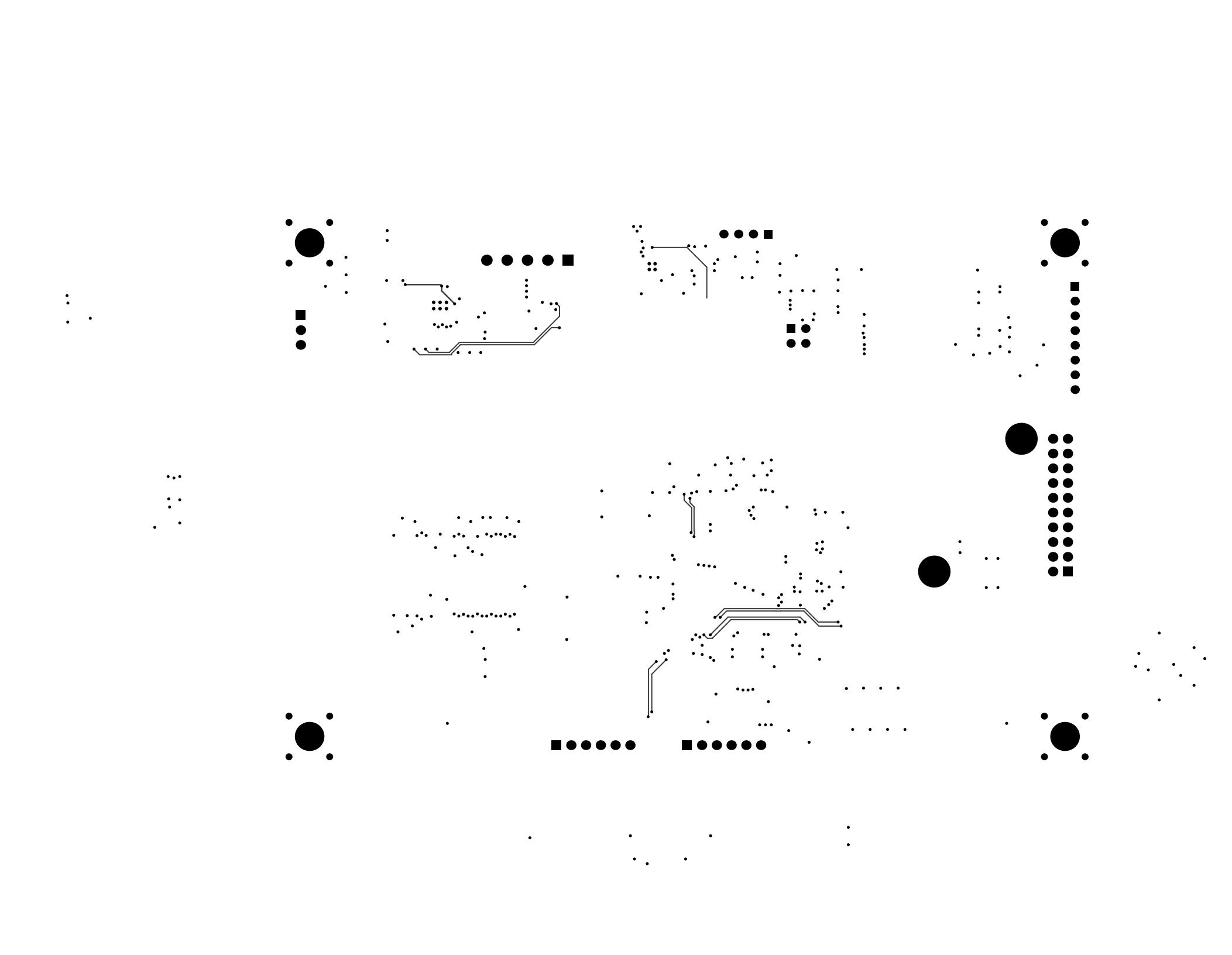


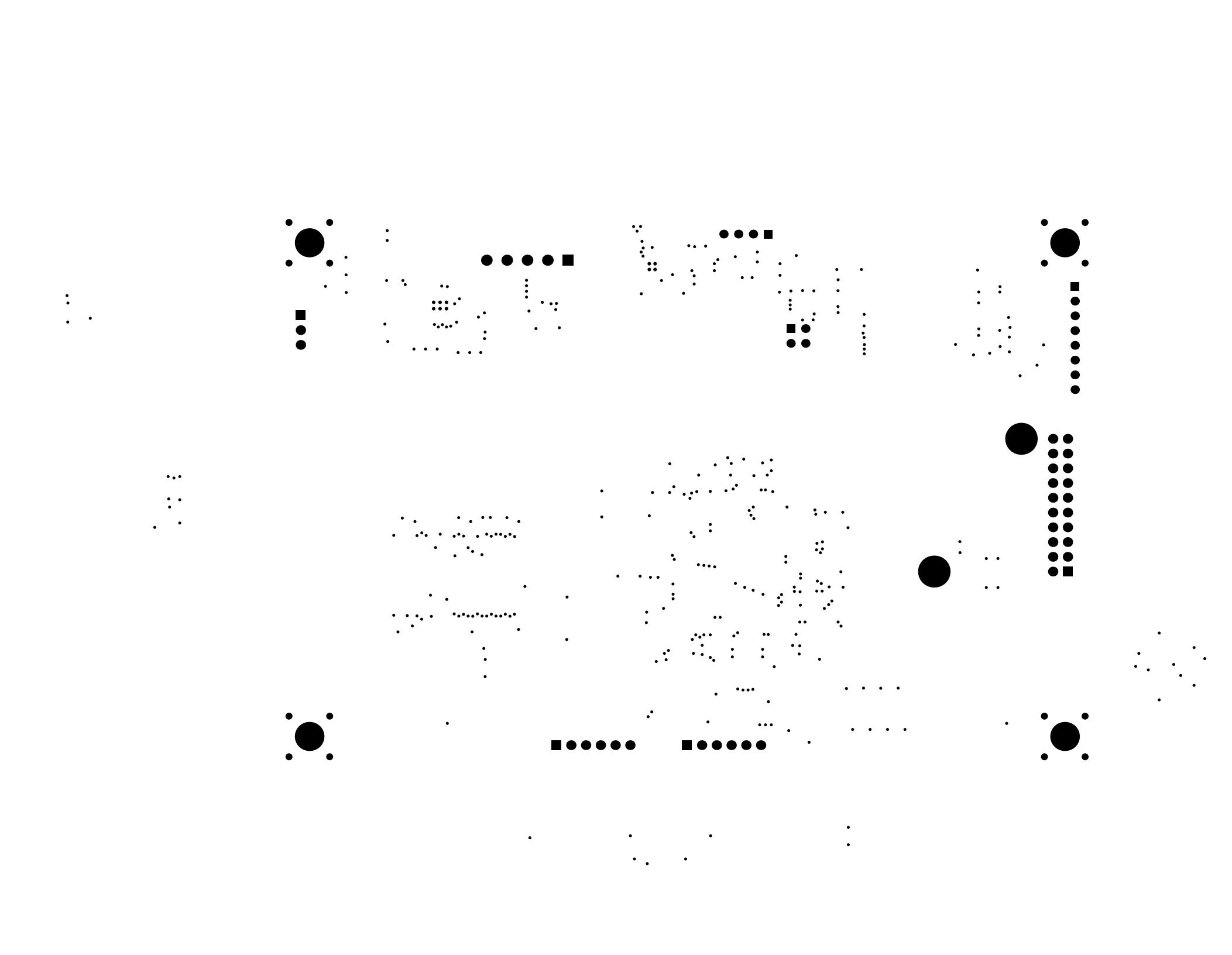
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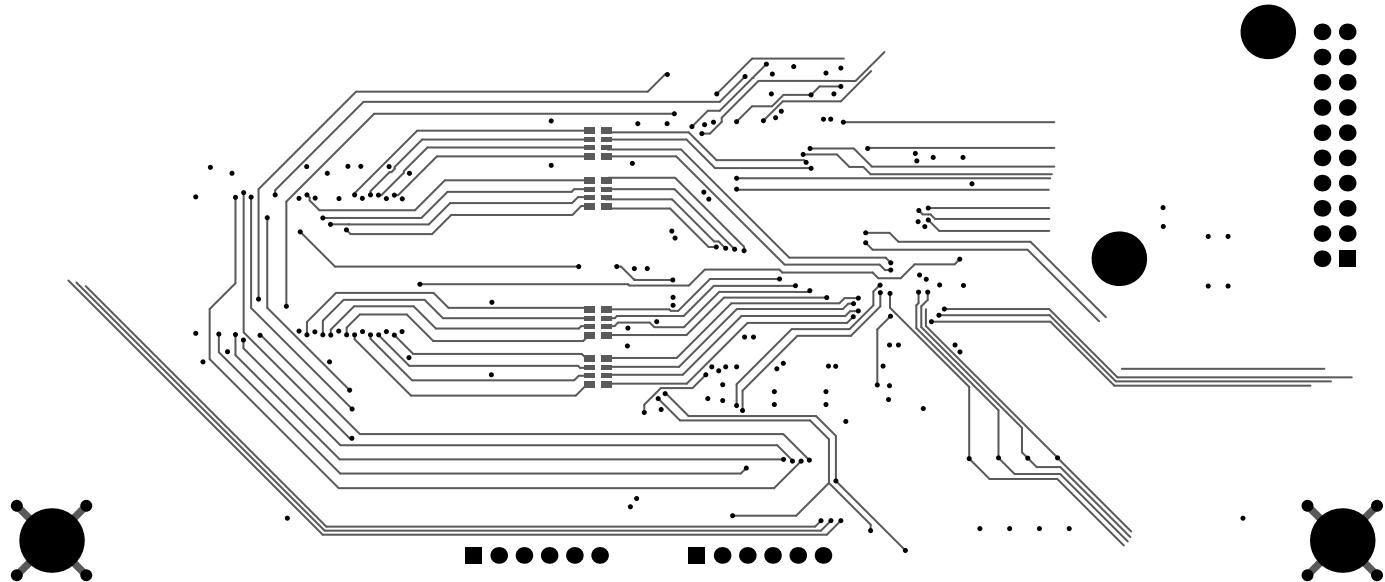
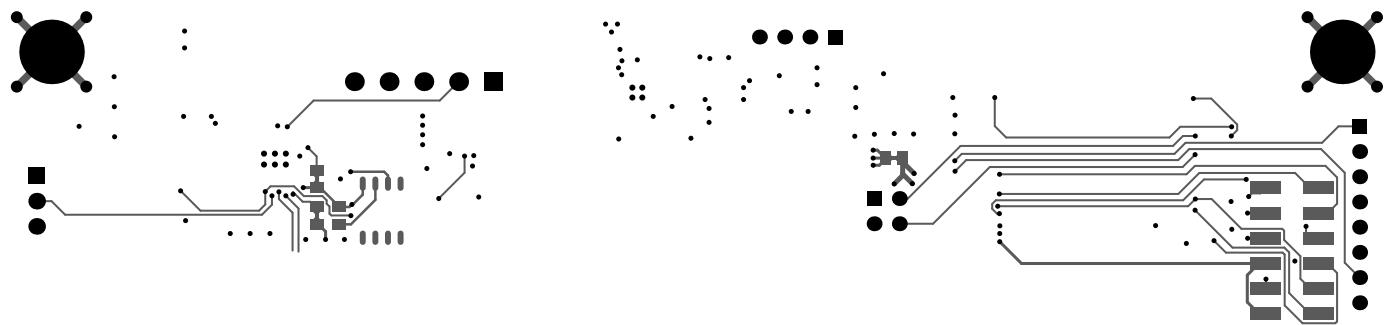


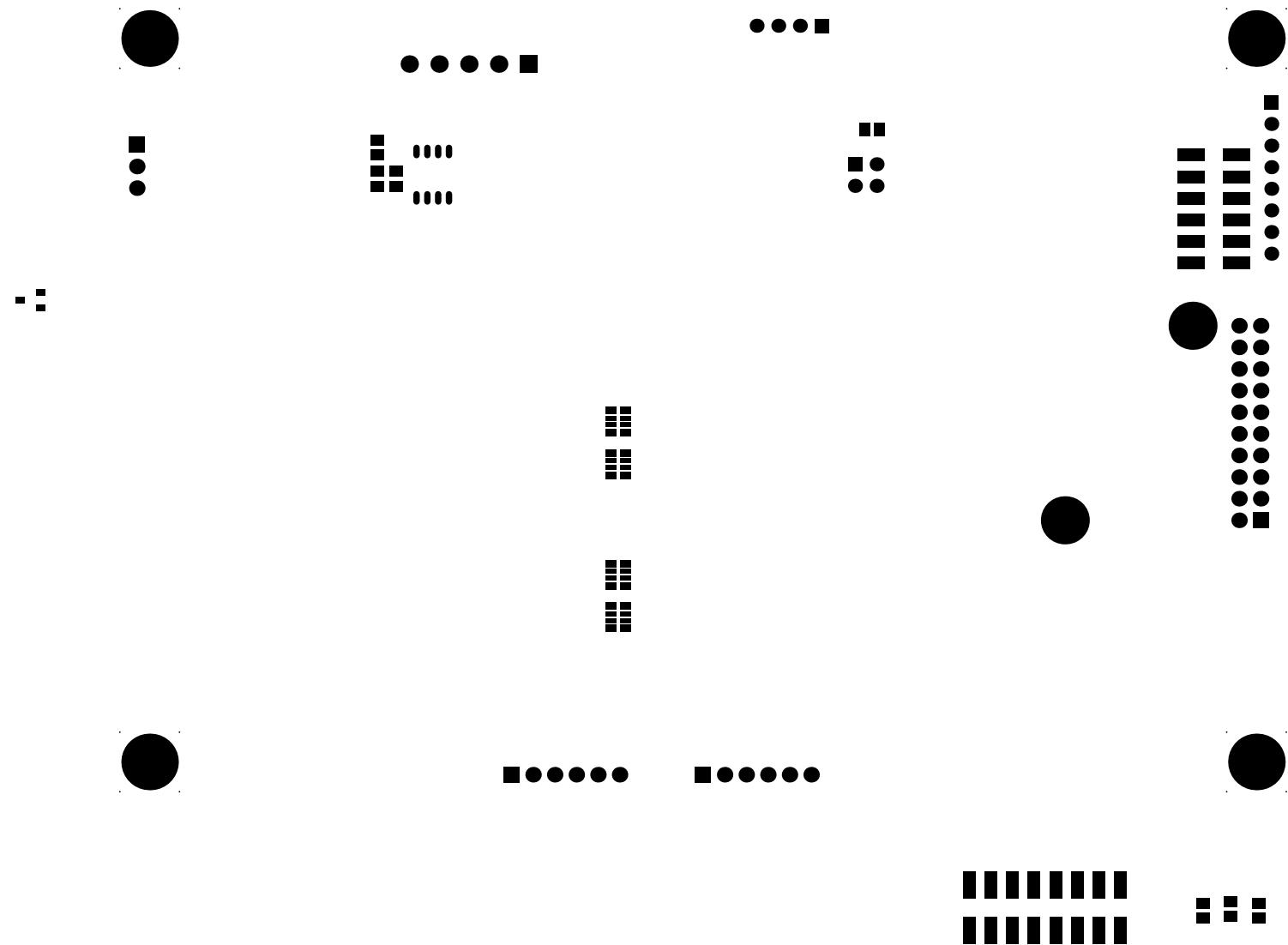
SOLENS











BEN HEBERLEIN
JEFFERY LIM
TAYLOR Neuhen
JEREMY Rab
AKIRA Youngblood

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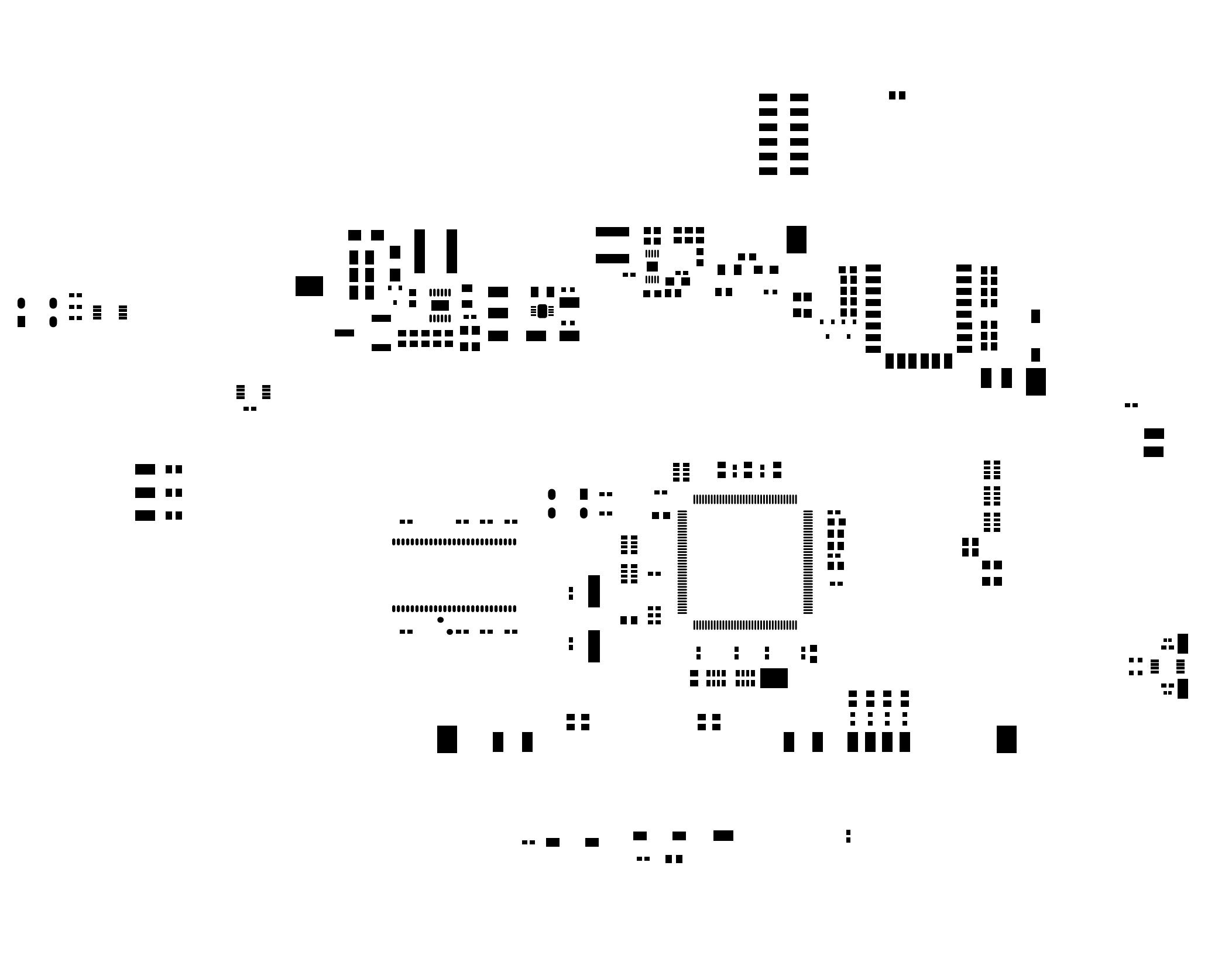
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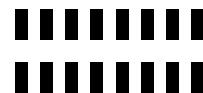
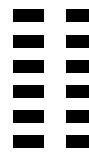
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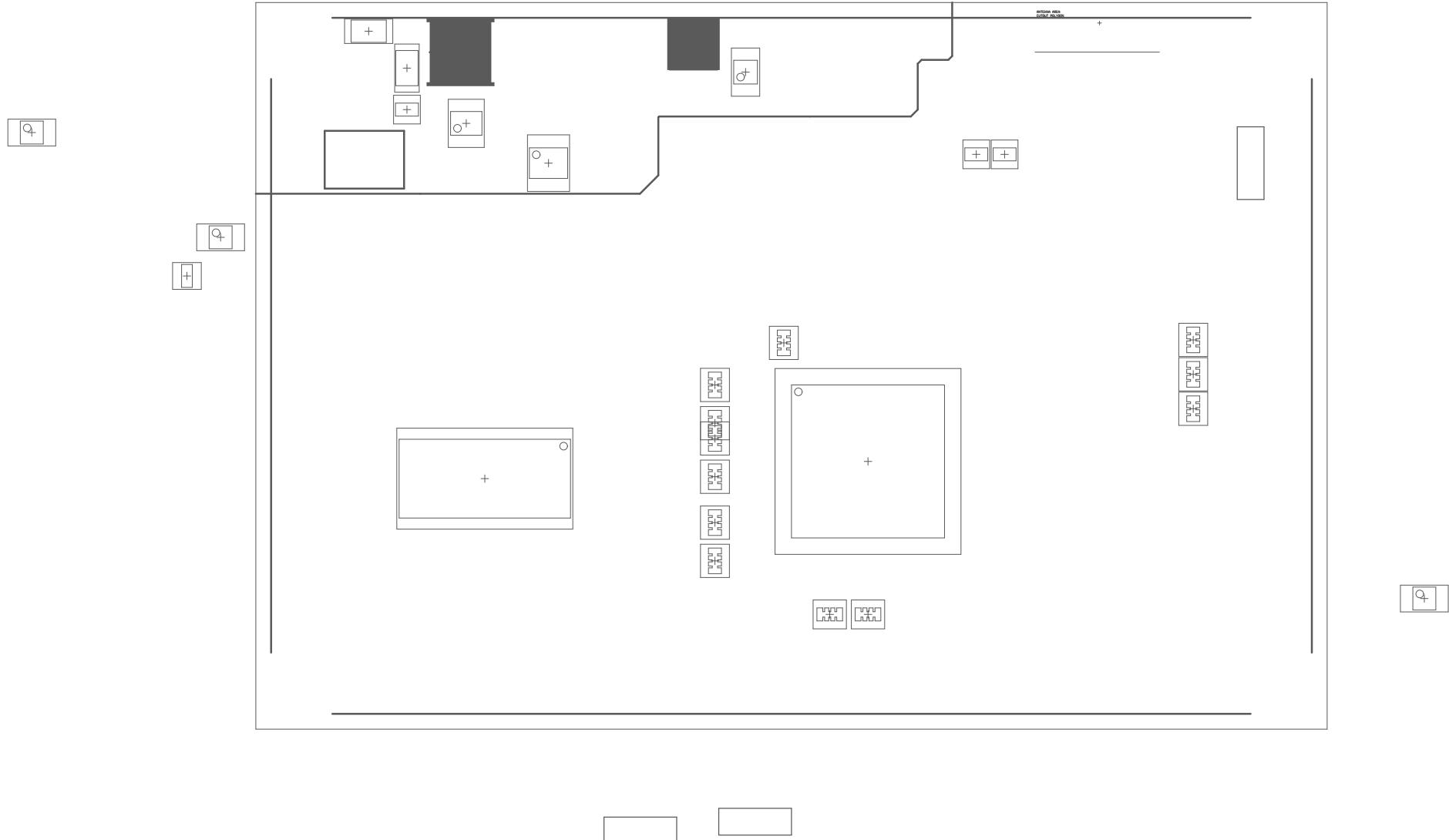
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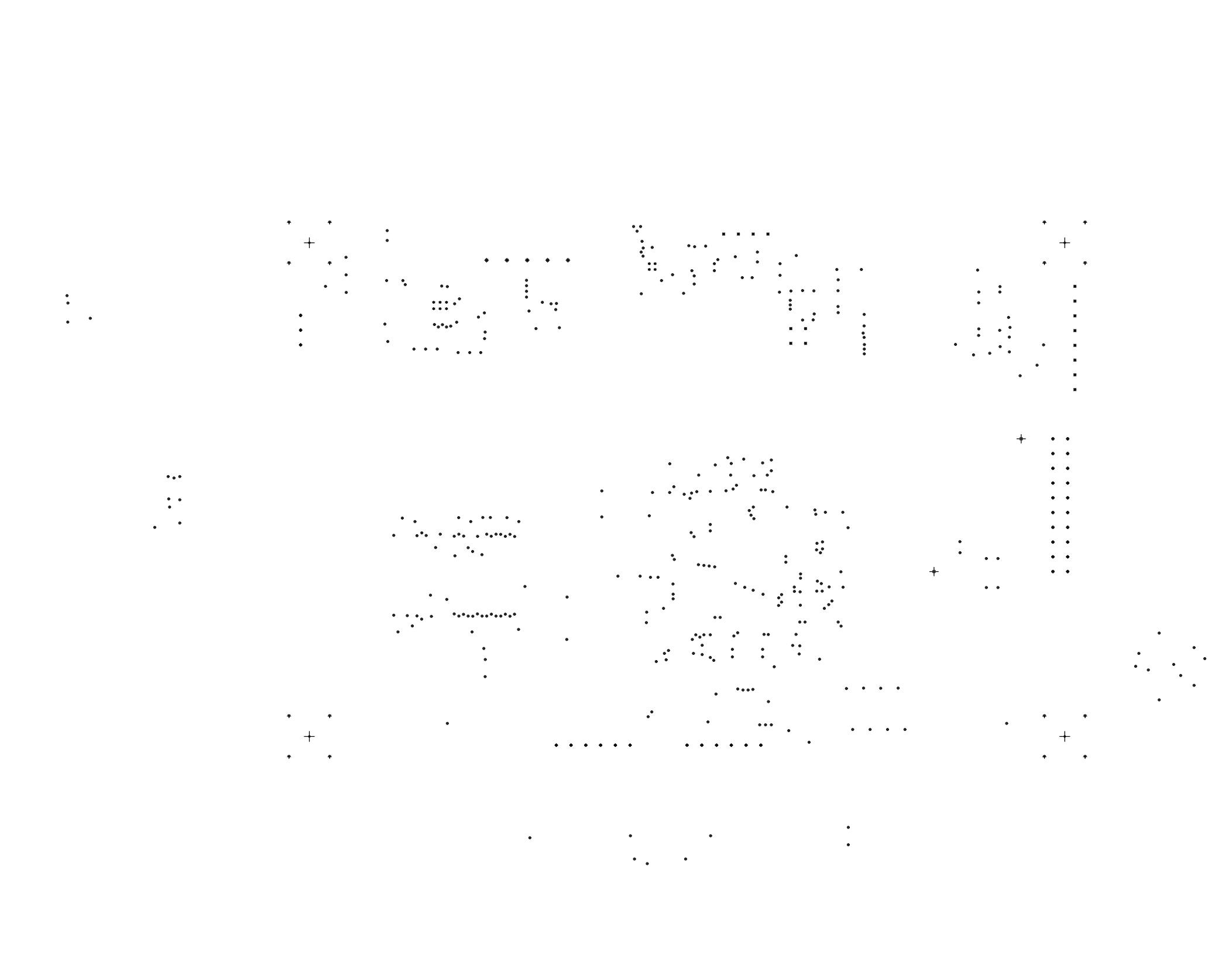




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SOLENS
A Fluffy Logic Production

AKIRA Youngblood
JEREMY Rapp
TAYLOR Neuhren
JEFFERY LIm
BEN HEBERlein

