## **Electrical Rules Check Report**

| Class   | Document      | Message  |
|---------|---------------|--|
| Warning | Solens.SchDoc | Nets Wire I2C2_ALERT has multiple names (Net Label I2C2_ALERT,Net Label              |
|         |               | PERIPH_ALERT, Sheet Entry Z1-PERIPH_ALERT(I/O), Sheet Entry                          |
|         |               | 72-FUEL AL L(I/O), Sheet Entry 73-A\L\E\R\T\(I/O))                                   |
| Warning | Solens.SchDoc | Nets Wire 12C2 SCL has multiple names (Net Label 12C2 SCL, Net Label                 |
|         |               | PERIPH_SCL,Sheet Entry Z1-PERIPH_SCL(I/O),Sheet Entry Z2-SCL(I/O),Sheet Entry        |
|         |               | Z3-SCL(I/O))   |
| Warning | Solens.SchDoc | Nets Wire 12C2_SDA has multiple names (Net Label 12C2_SDA,Net Label                  |
|         |               | PERIPH_SDA,Sheet Entry Z1-PERIPH_SDA(I/O),Sheet Entry Z2-SDA(I/O),Sheet Entry        |
|         |               | 73-SDA(I/O))   |
| Warning | Solens.SchDoc | Nets Wire PERIPH_ALERT has multiple names (Sheet Entry Z1-PERIPH_ALERT(I/O), Sheet   |
|         |               | Entry Z2-FUEL AL L(I/O), Sheet Entry Z3-A\L\E\R\T\(I/O))                             |
| Warning | Solens.SchDoc | Nets Wire PERIPH_SCL has multiple names (Sheet Entry Z1-PERIPH_SCL(I/O), Sheet Entry |
|         |               | Z2-SCL(I/O), Sheet Entry Z3-SCL(I/O))  |
| Warning | Solens.SchDoc | Nets Wire PERIPH_SDA has multiple names (Sheet Entry Z1-PERIPH_SDA(I/O), Sheet Entry |
|         |               | Z2-SDA(I/O), Sheet Entry Z3-SDA(I/O))  |
| Warning | Solens.SchDoc | Nets Wire PWR_CHRG_L has multiple names (Net Label PWR_CHRG_L,Sheet Entry            |
|         |               | Z1-PV_CHRG_L(Input), Sheet Entry_Z2-PV_CHRG_L(Output))                               |
| Warning | Solens.SchDoc | Nets Wire PWR_FAULT_L has multiple names (Net Label PWR_FAULT_L, Sheet Entry         |
|         |               | Z1-PV FAULT L(Input), Sheet Entry Z2-PV FAULT L(Output))                             |

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**Design Rules Verification Report**Filename : C:\Users\qux\projects\solenshardware\Altium\Solens\Solens.PcbDoc

Warnings 4 Rule Violations 4

| Warnings                             |   |
|--------------------------------------|---|
| Unplated multi-layer pad(s) detected | 4 |
| Total                                | 4 |

| Rule Violations  |   |
|--|---|
| Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil )  | 0 |
| Room Z1 (Bounding Region = (2350mil, 6975.984mil, 5224.016mil, 8688.583mil) (Disabled)(InComponentClass('Z1'))         | 0 |
| Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil )  | 0 |
| Room Z6 (Bounding Region = (6798.819mil, 5853.937mil, 9003.543mil, 7113.779mil)  | 0 |
| Room Z7 (Bounding Region = (6779.134mil, 7172.835mil, 9042.913mil, 8688.583mil)  | 0 |
| Width Constraint (Min=8mil) (Max=64mil) (Preferred=8mil) (InNetClass('HVY'))   | 0 |
| Width Constraint (Min=8mil) (Max=64mil) (Preferred=8mil) (InNetClass('PWR'))   | 0 |
| Room Z2 (Bounding Region = (5302.756mil, 7468.11mil, 6680.709mil, 8688.583mil)   | 0 |
| Short-Circuit Constraint (Allowed=No) (All),(All)  | 0 |
| Un-Routed Net Constraint ( (All) )   | 4 |
| Clearance Constraint (Gap=8mil) (All),(All)  | 0 |
| Power Plane Connect Rule(Relief Connect )(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)         | 0 |
| Width Constraint (Min=7mil) (Max=12mil) (Preferred=8mil) (All)   | 0 |
| Component Clearance Constraint ( Horizontal Gap = 1mil, Vertical Gap = 10mil ) (All),(All)                             | 0 |
| Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)   | 0 |
| Hole Size Constraint (Min=8mil) (Max=250mil) (All)   | 0 |
| Hole To Hole Clearance (Gap=10mil) (All),(All)   | 0 |
| Silk To Solder Mask (Clearance=2mil) (IsPad),(All)   | 0 |
| Silk to Silk (Clearance=5mil) (All),(All)  | 0 |
| Net Antennae (Tolerance=0mil) (All)  | 0 |
| Modified Polygon (Allow modified: No), (Allow shelved: No)   | 0 |
| Clearance Constraint (Gap=0mil) (InComponent('SJ*') And (IsFill Or IsPad Or IsTrack)), (InComponent('SJ*') And (IsFill | 0 |
| Short-Circuit Constraint (Allowed=Yes) (InComponent('SJ*') And (IsFill Or IsPad Or IsTrack)),(InComponent('SJ*') And   | 0 |
| Short-Circuit Constraint (Allowed=Yes) (InComponent('MTGH*') And (IsFill Or IsPad Or IsTrack)),(InComponent('MTG*')    | 0 |
| Width Constraint (Min=8mil) (Max=120mil) (Preferred=8mil) (InComponent('MTGH*'))                                       | 0 |
| Total  | 4 |
|  |   |

| Unplated multi-layer pad(s) detected                           |  |  |
|--|--|--|
| Pad MTGH1-1(196.85mil, 196.85mil) on Multi-Layer on Net GND    |  |  |
| Pad MTGH2-1(196.85mil,3543.307mil) on Multi-Layer on Net GND   |  |  |
| Pad MTGH3-1(6496.063mil,3543.307mil) on Multi-Layer on Net GND |  |  |
| Pad MTGH4-1(6496.063mil, 196.85mil) on Multi-Layer on Net GND  |  |  |

| Un-Routed Net Constraint ( (AII) )   |
|--|
| Un-Routed Net Constraint: Unplated Pad MTGH1-1(196.85mil, 196.85mil) on Multi-Layer    |
| Un-Routed Net Constraint: Unplated Pad MTGH2-1(196.85mil,3543.307mil) on Multi-Layer   |
| Un-Routed Net Constraint: Unplated Pad MTGH4-1(6496.063mil,196.85mil) on Multi-Layer   |
| Un-Routed Net Constraint: Unplated Pad MTGH3-1(6496.063mil,3543.307mil) on Multi-Layer |

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