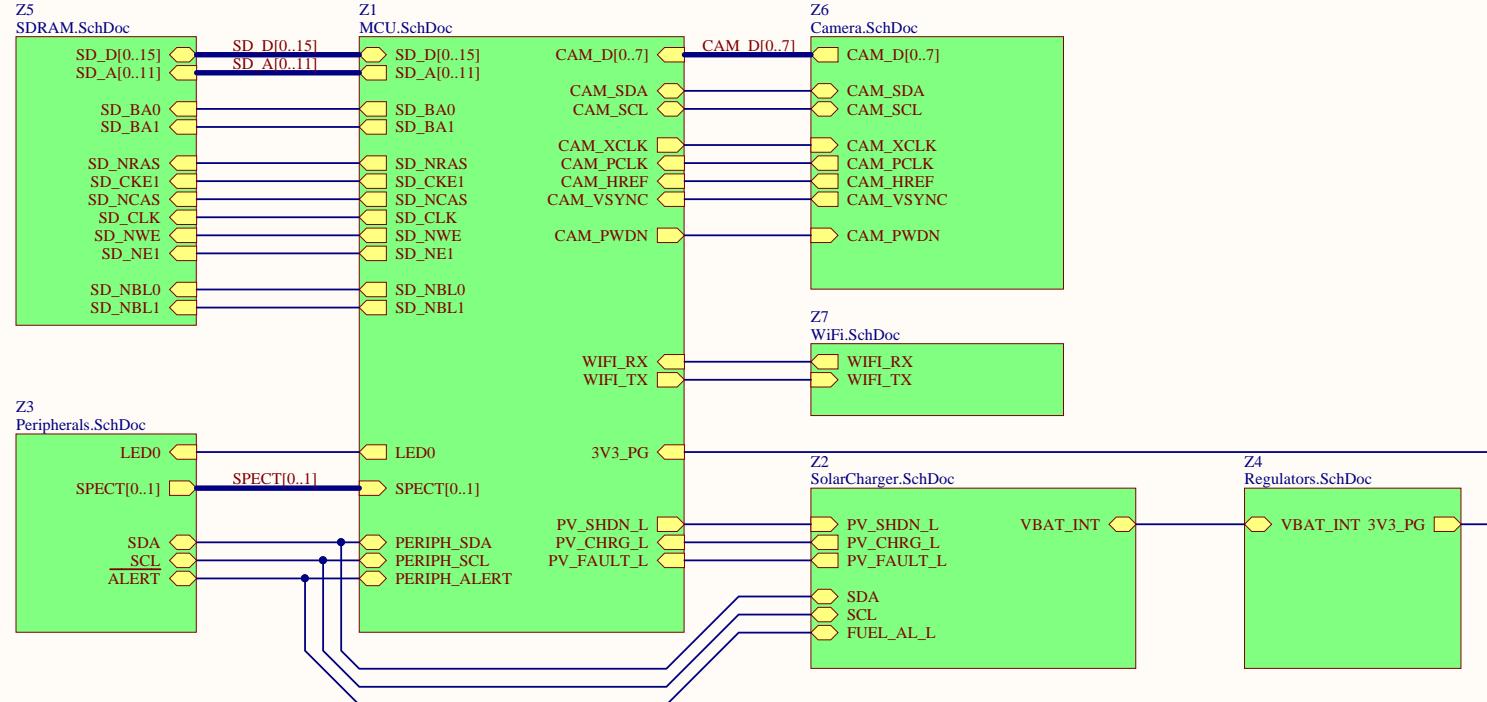


A

A



B

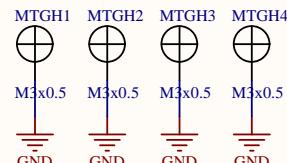
B

C

C

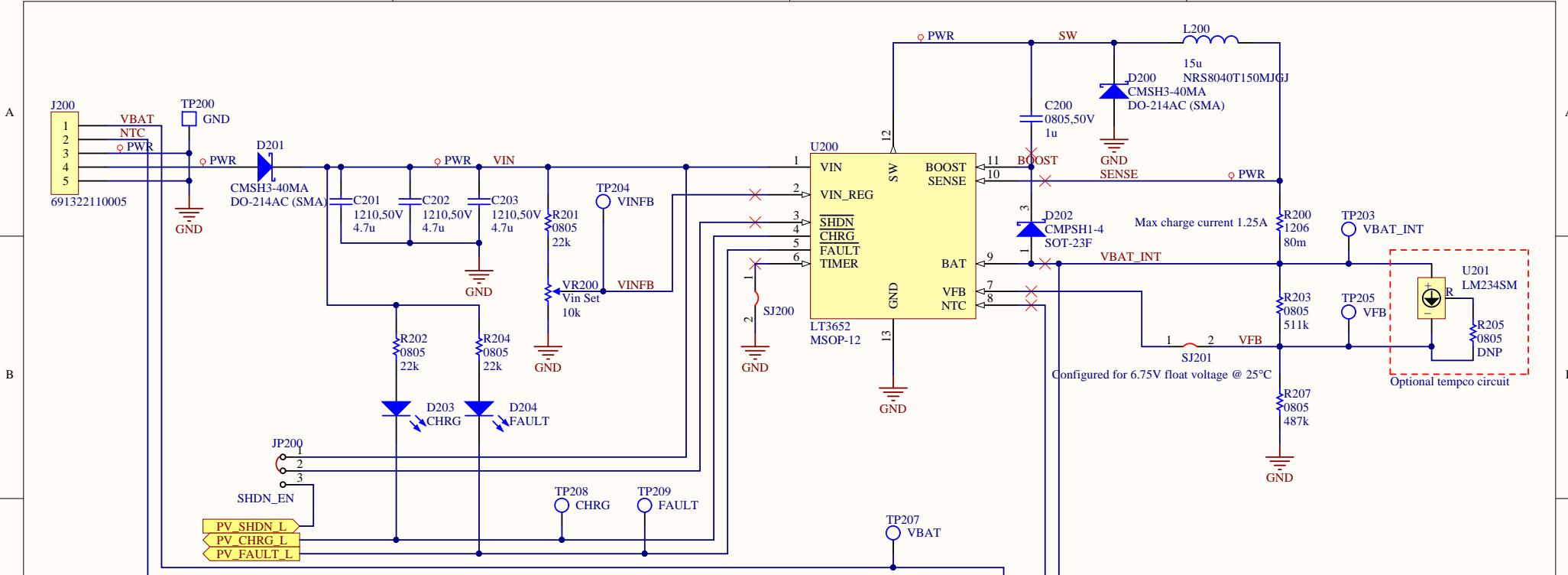
D

D



Title		
Solens Camera Subsystem		ERC_WARN, FOOTPRINT_N/A
Size		Number
A4		
Date:	3/18/2017	Sheet 1 of 8
File:	C:\Users\..\Solens.SchDoc	Drawn By: JL, AY

1 2 3 4



Title		
Solens MPPC/SLA charger ERC PASS, FOOTPRINT OK, TESPOINTED		
Size	Number	Revision
A4		
Date:	3/18/2017	Sheet 2 of 8
File:	C:\Users..\SolarCharger.SchDoc	Drawn By: TN, AY

1 2 3 4

A

A

B

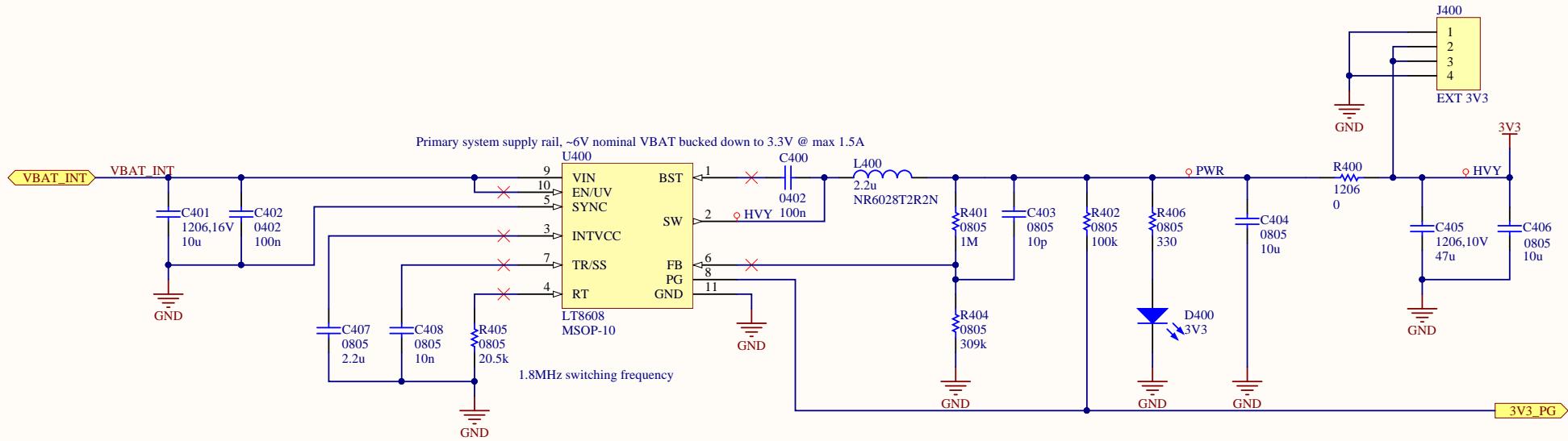
B

C

C

D

D



Title		
Solens Voltage Regulators		ERC PASS, FOOTPRINT OK, TESPOINTED
Size		Revision
A4		
Date:	3/18/2017	Sheet 3 of 8
File:	C:\Users...\Regulators.SchDoc	Drawn By: TN, AY

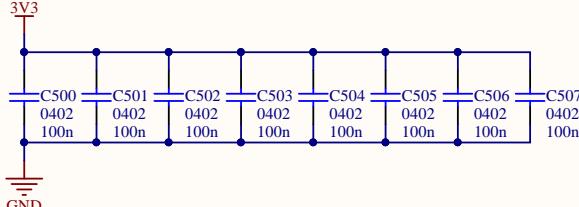
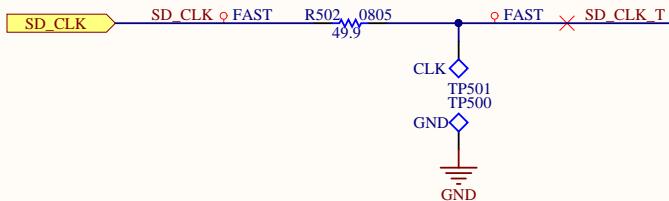
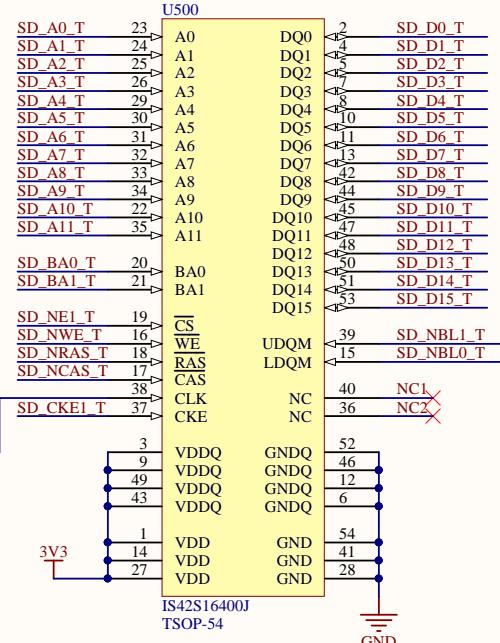
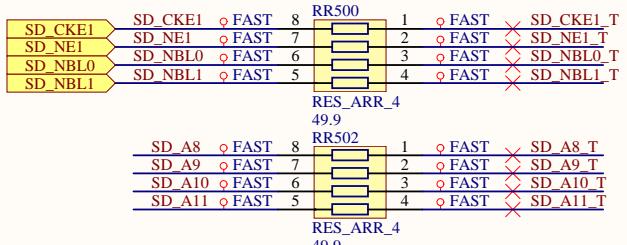
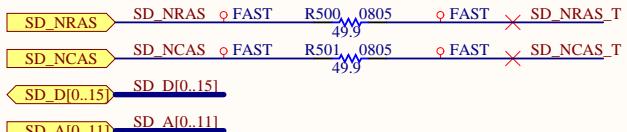
1

2

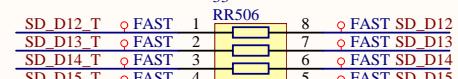
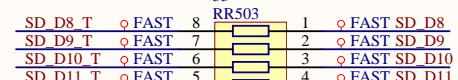
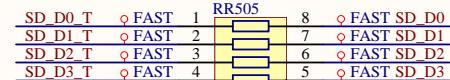
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4

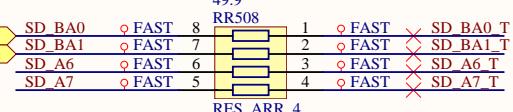
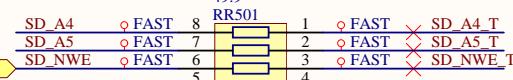
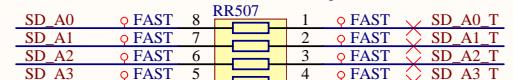
A



DATA termination to be placed halfway between MCU and RAM



ADDR and CLK termination to be placed at MCU



Title: Solens_SDRAM
ERC PASS, FOOTPRINT OK, TESPOINTED

Size	Number	Revision
A4		

Date:	Sheet 4 of 8
3/18/2017	

File:	Drawn By:
C:\Users\...\SDRAM.SchDoc	JL, AY

1

2

3

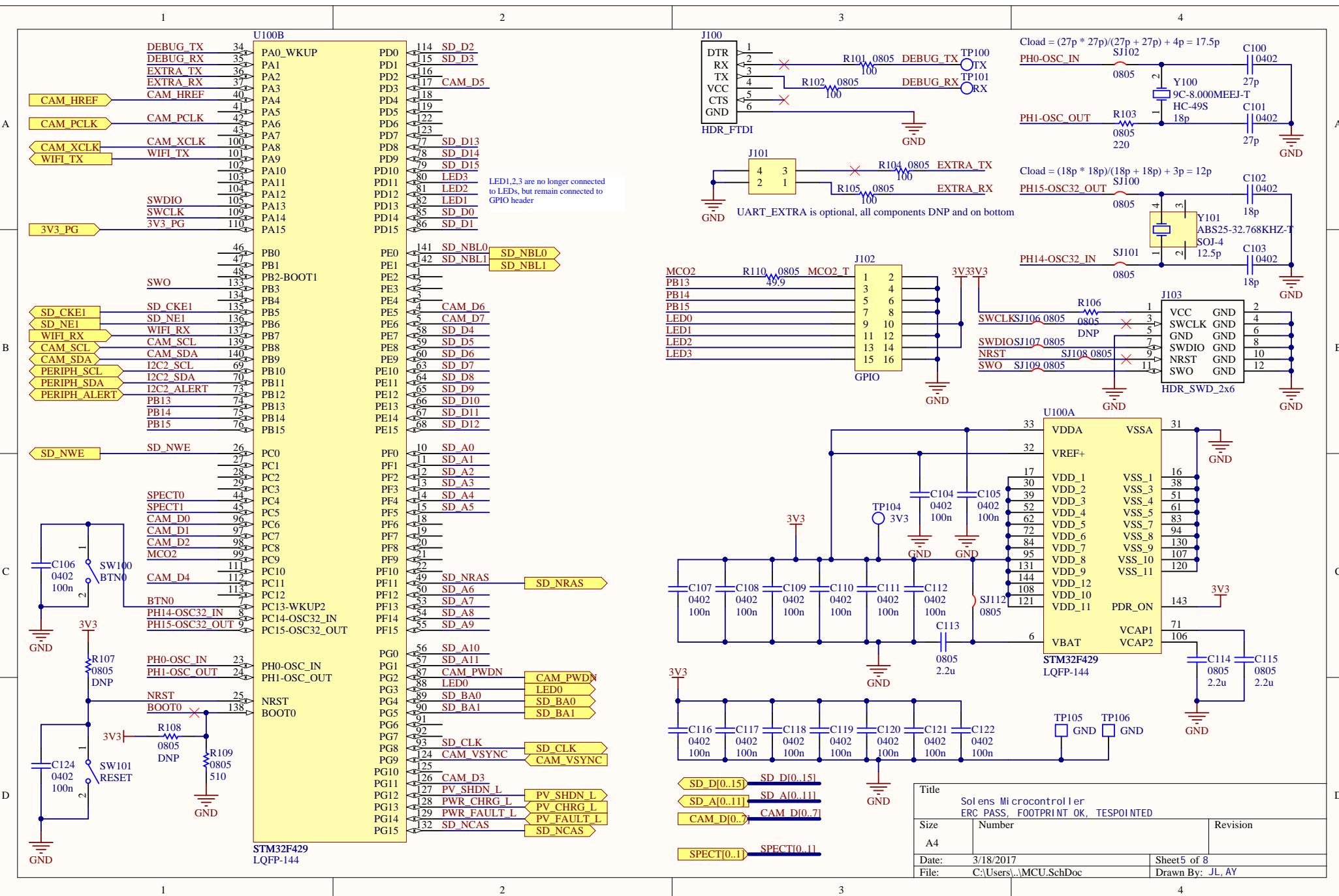
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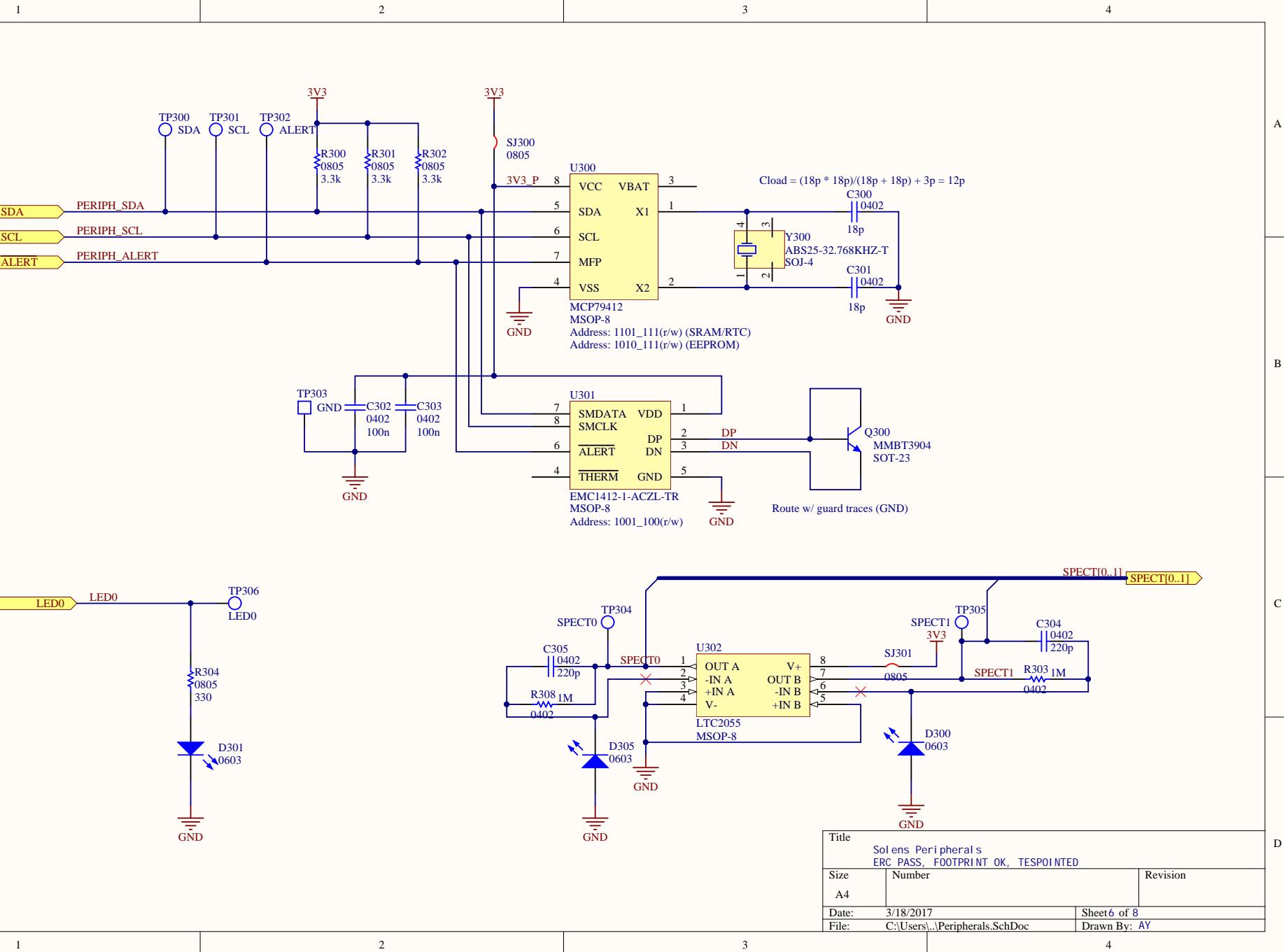
A

B

C

D





A

A

B

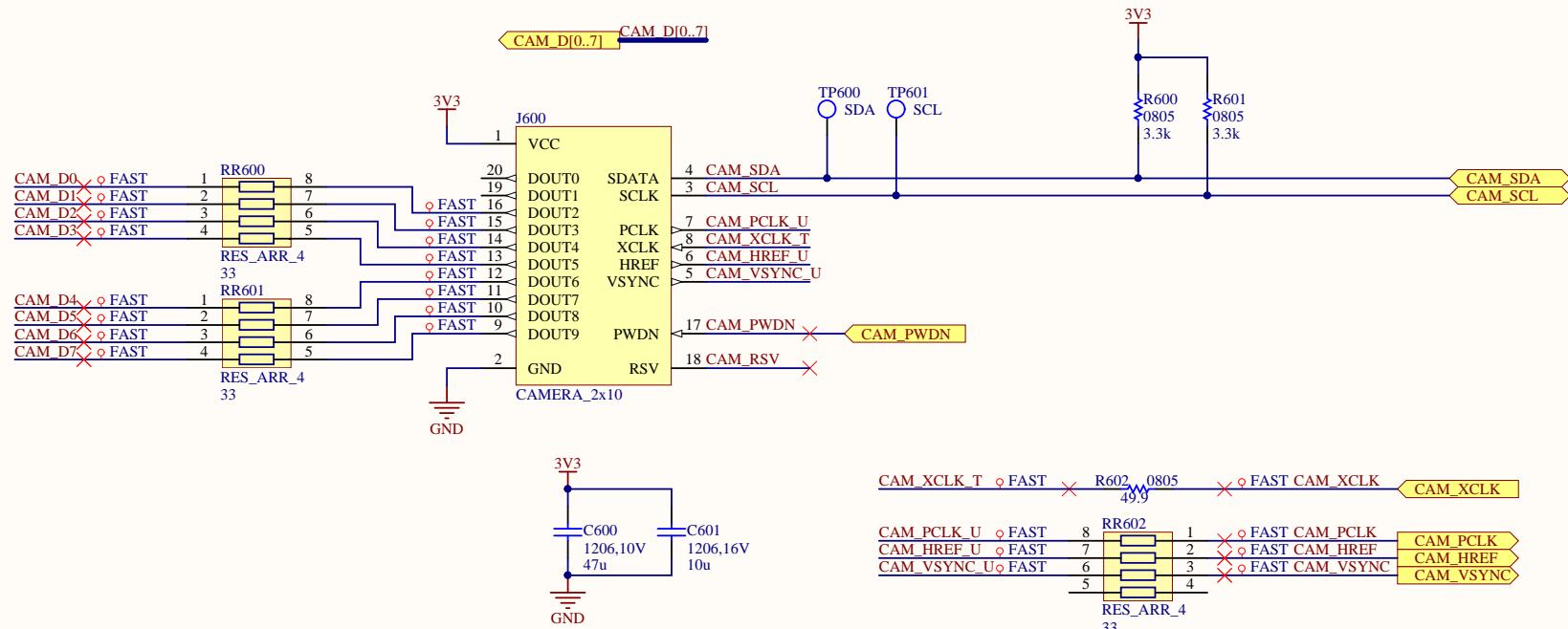
B

C

C

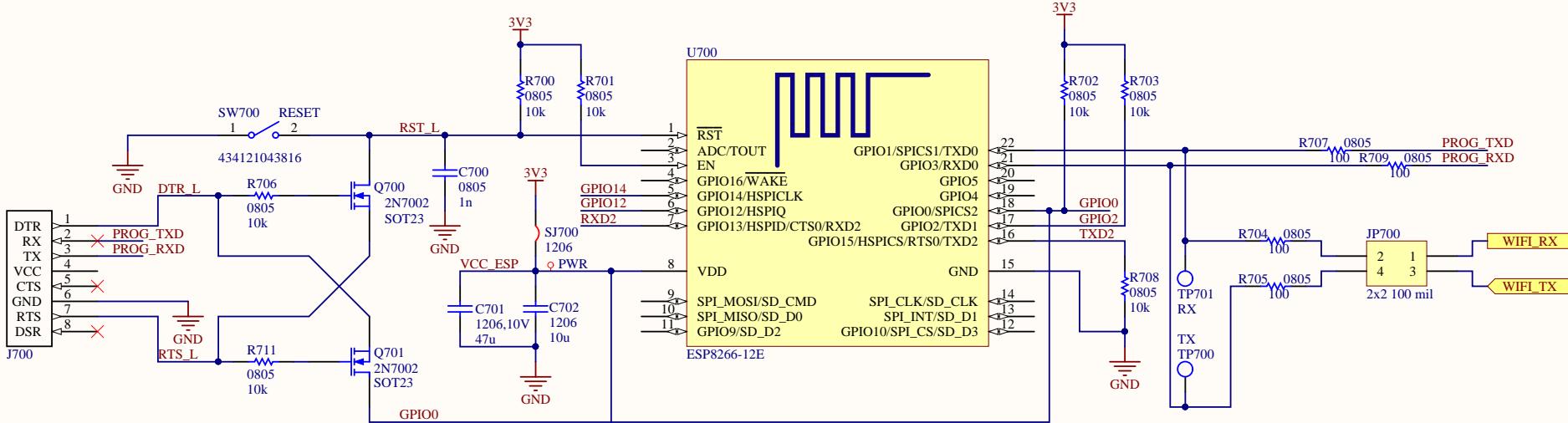
D

D

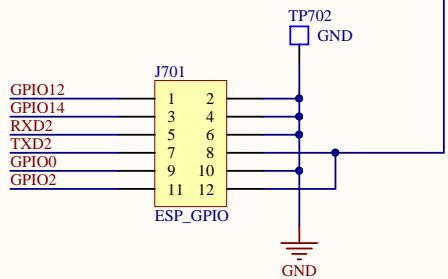


Title		
Solens Camera Subsystem ERC PASS, FOOTPRINT OK, TESTPOINTED		
Size	Number	Revision
A4		
Date:	3/18/2017	Sheet 7 of 8
File:	C:\Users\...\Camera.SchDoc	Drawn By: JL, AY

A

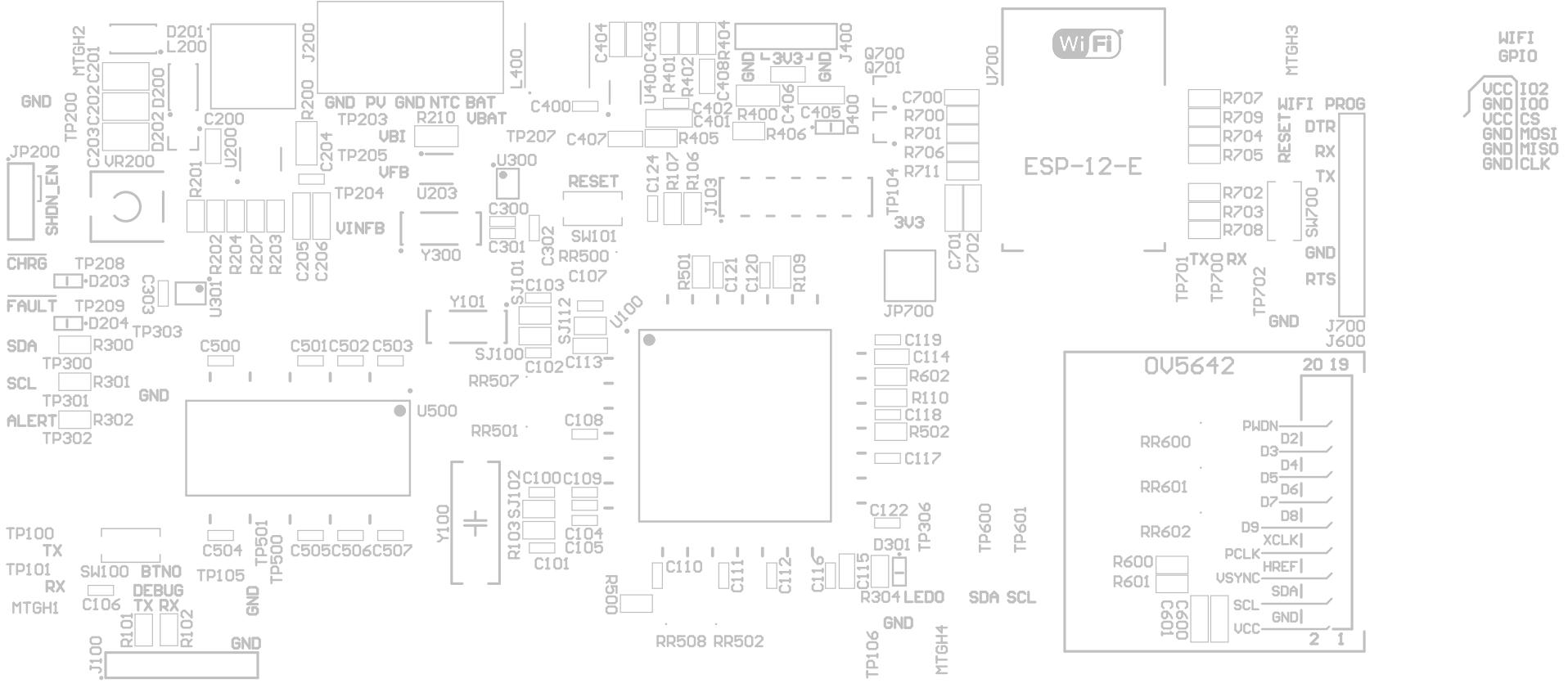


B

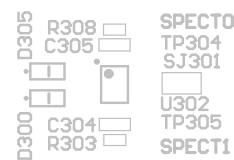


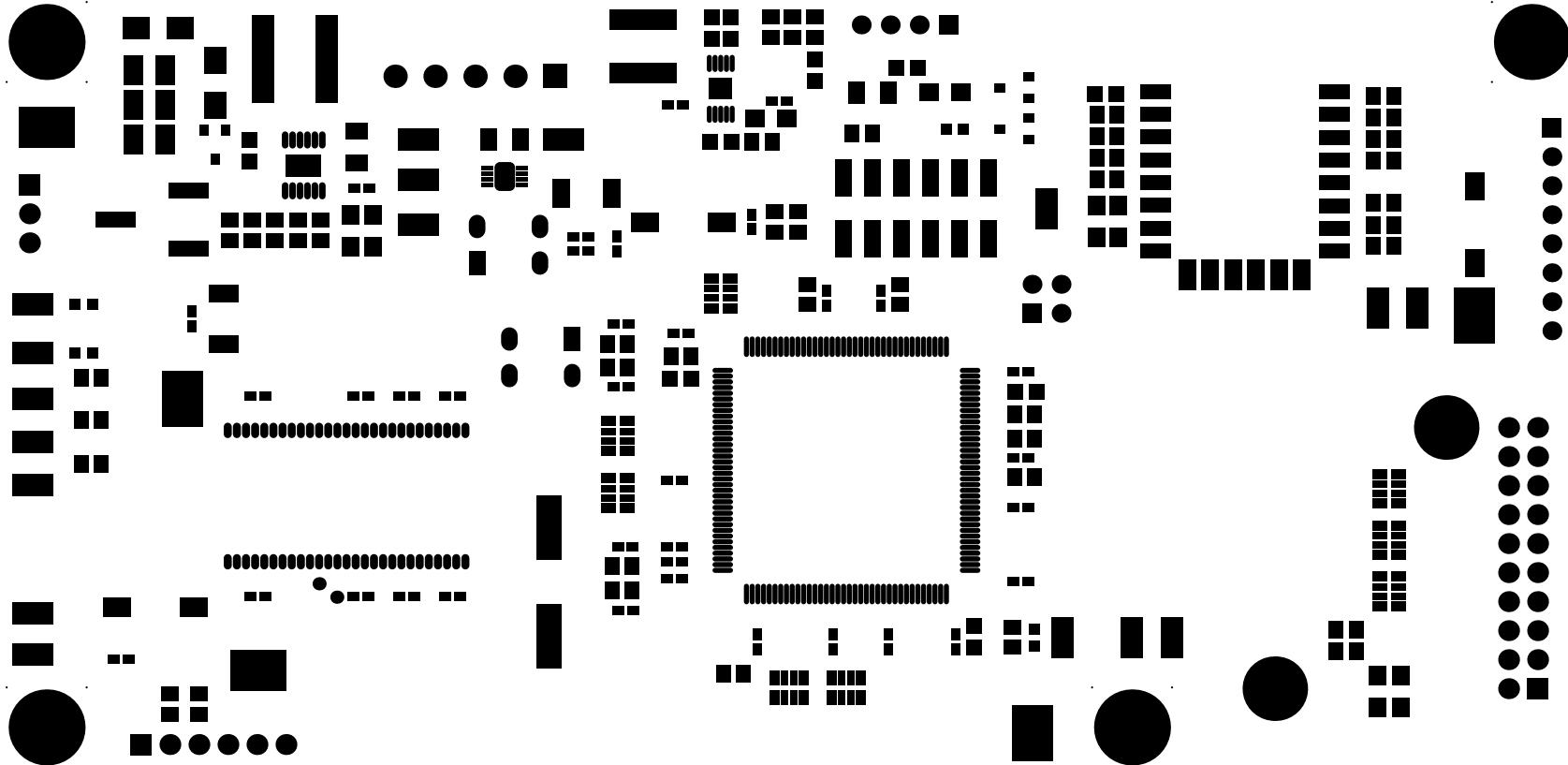
C

Title		
Solens WiFi Subsystem ERC PASS, FOOTPRINT OK, TESTPOINTED		
Size	Number	Revision
A4		
Date:	3/18/2017	Sheet 8 of 8
File:	C:\Users\...\WiFi.SchDoc	Drawn By: JL, AY

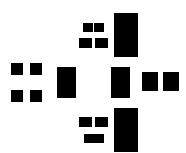


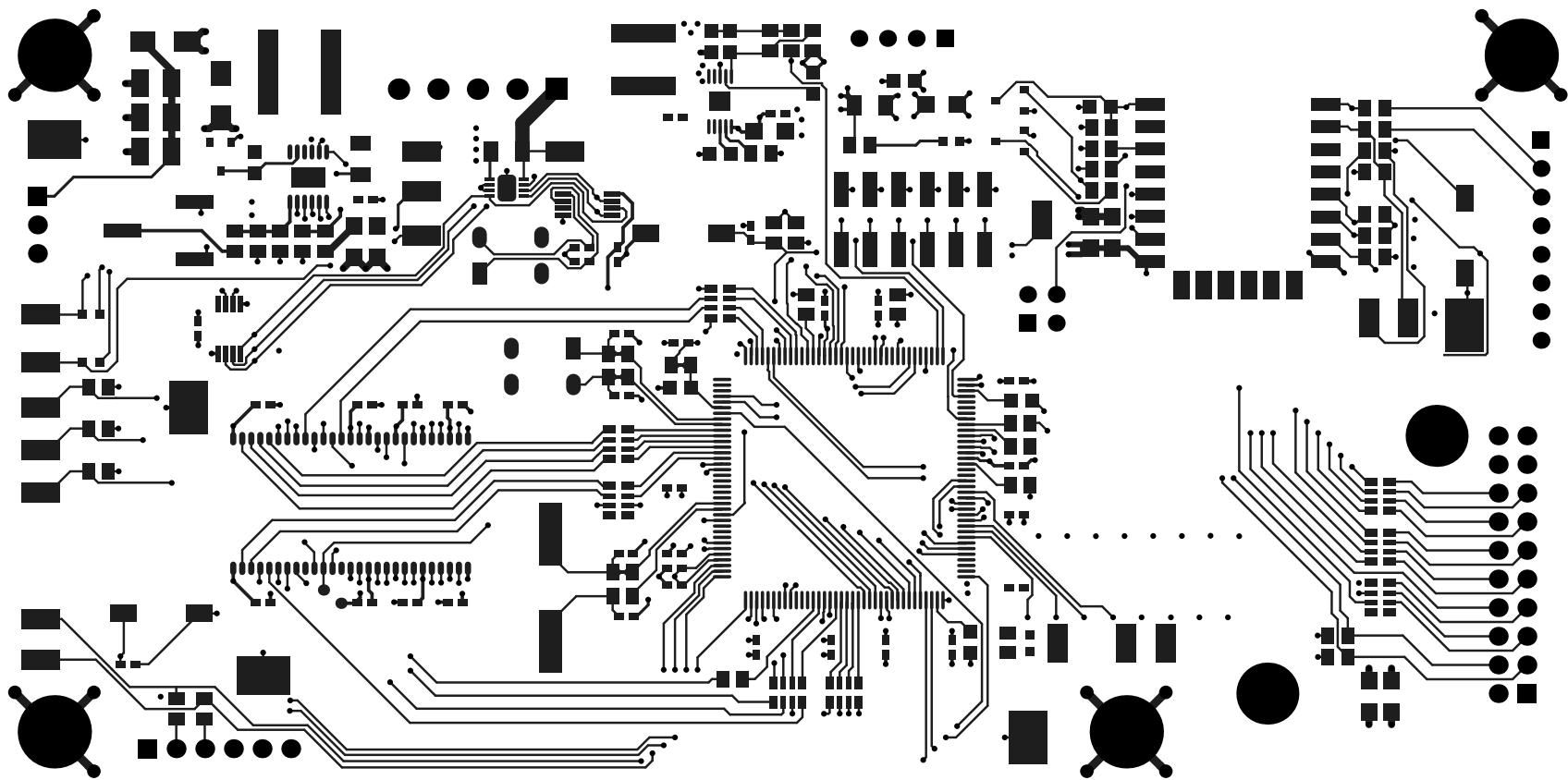
A Fluffy Logic Production



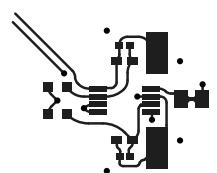


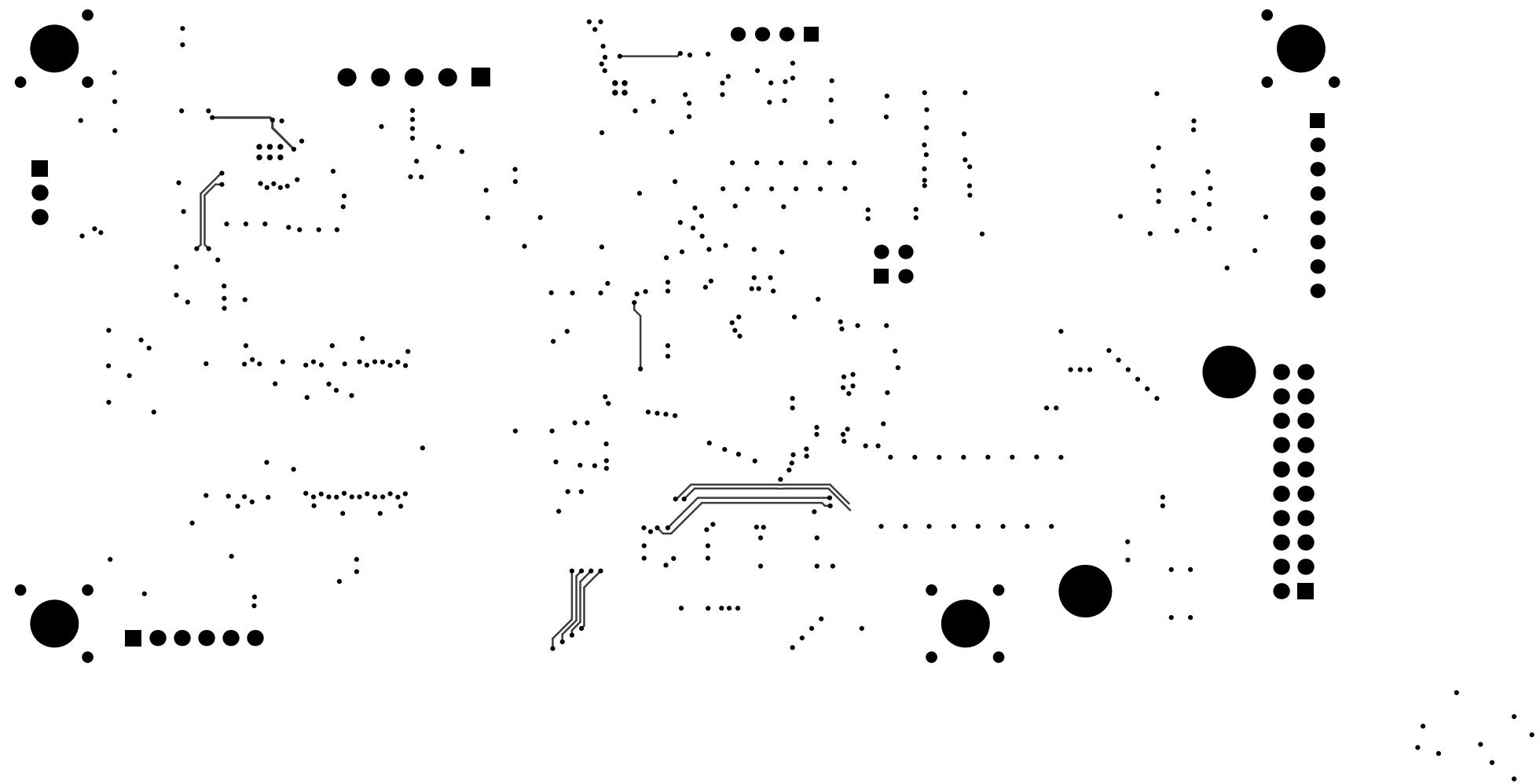
SOLENS

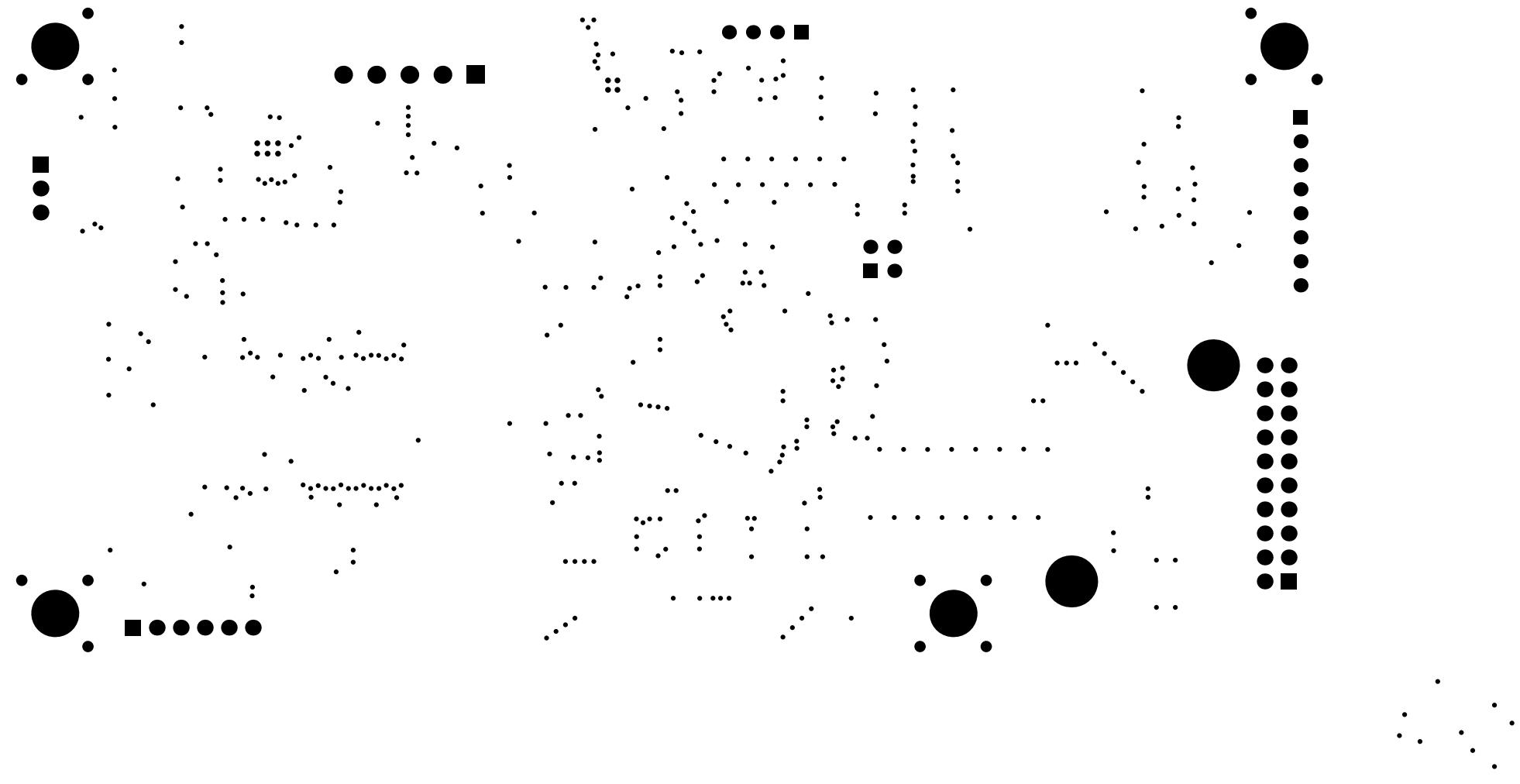


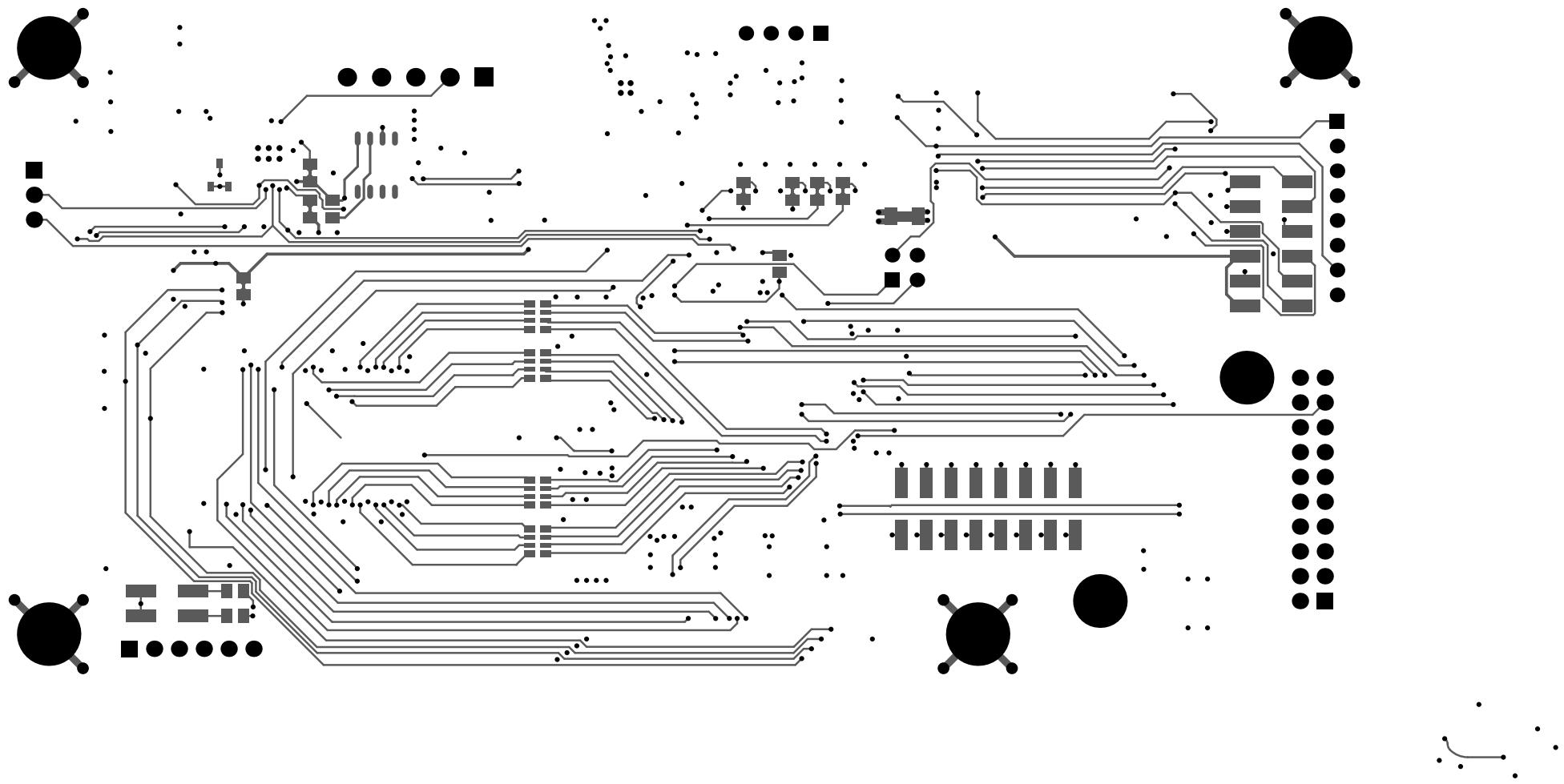


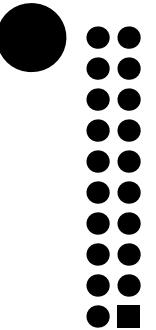
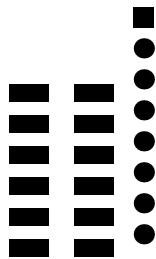
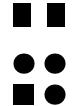
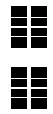
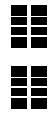
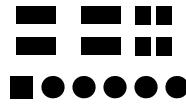
SOLENS



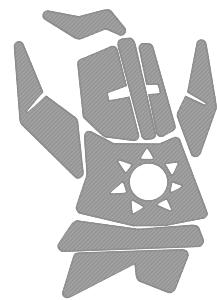








BEN HEBERLEIN
JEFFERY LIM
TAYLOR NGUYEN
JEREMY RAPP
AKIRA YOUNGBLOOD

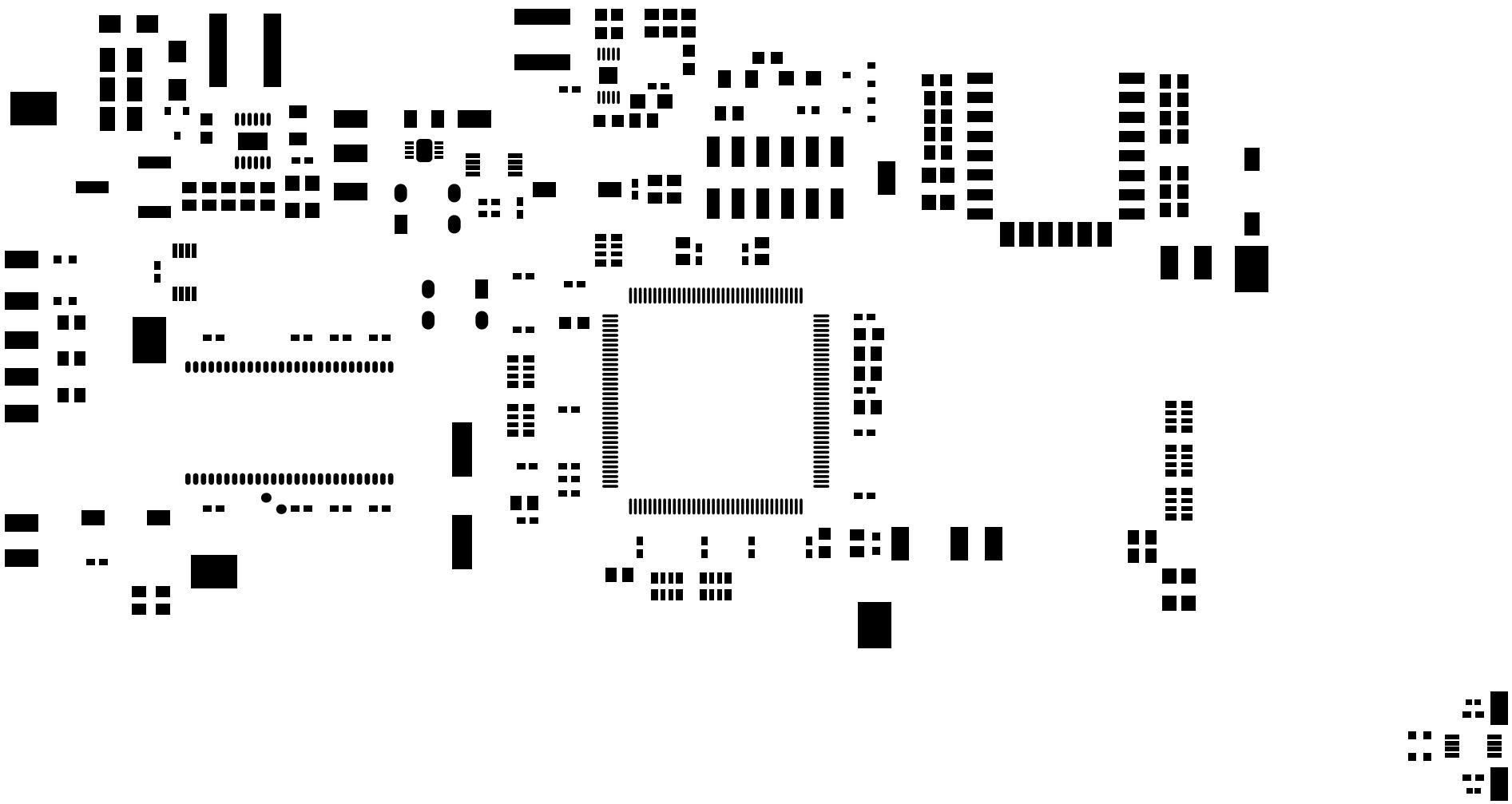


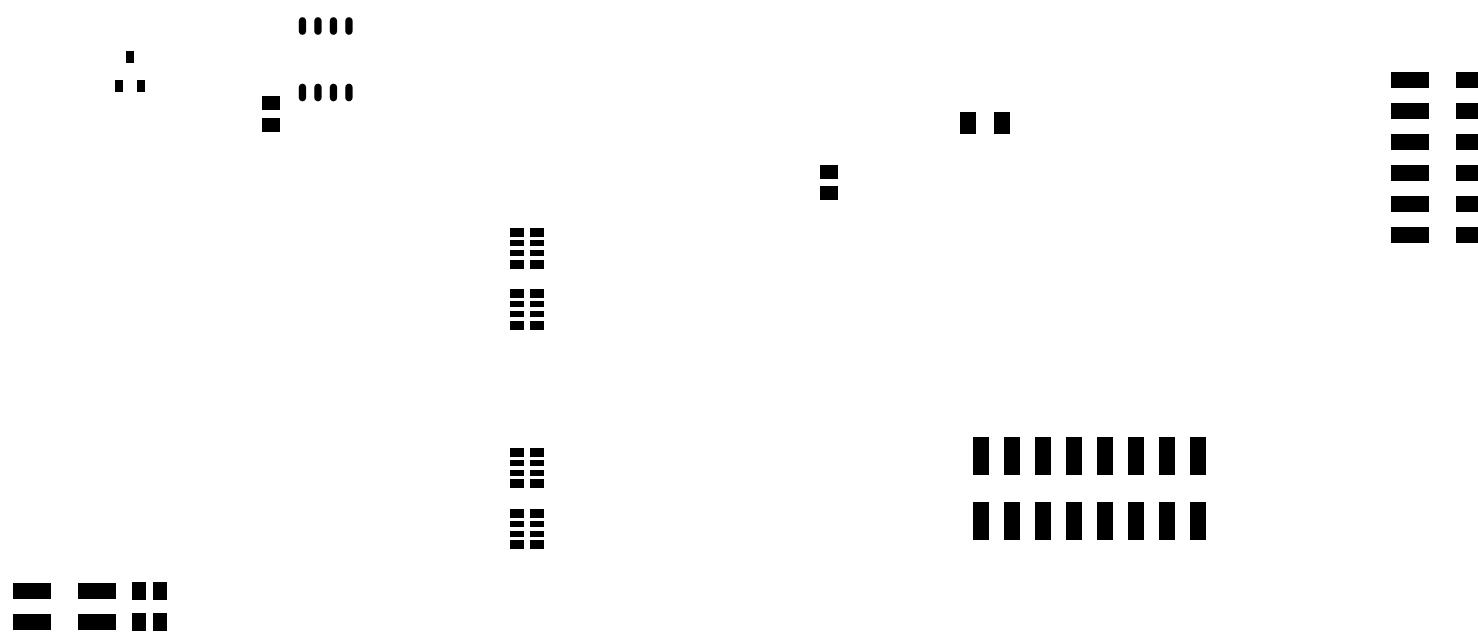
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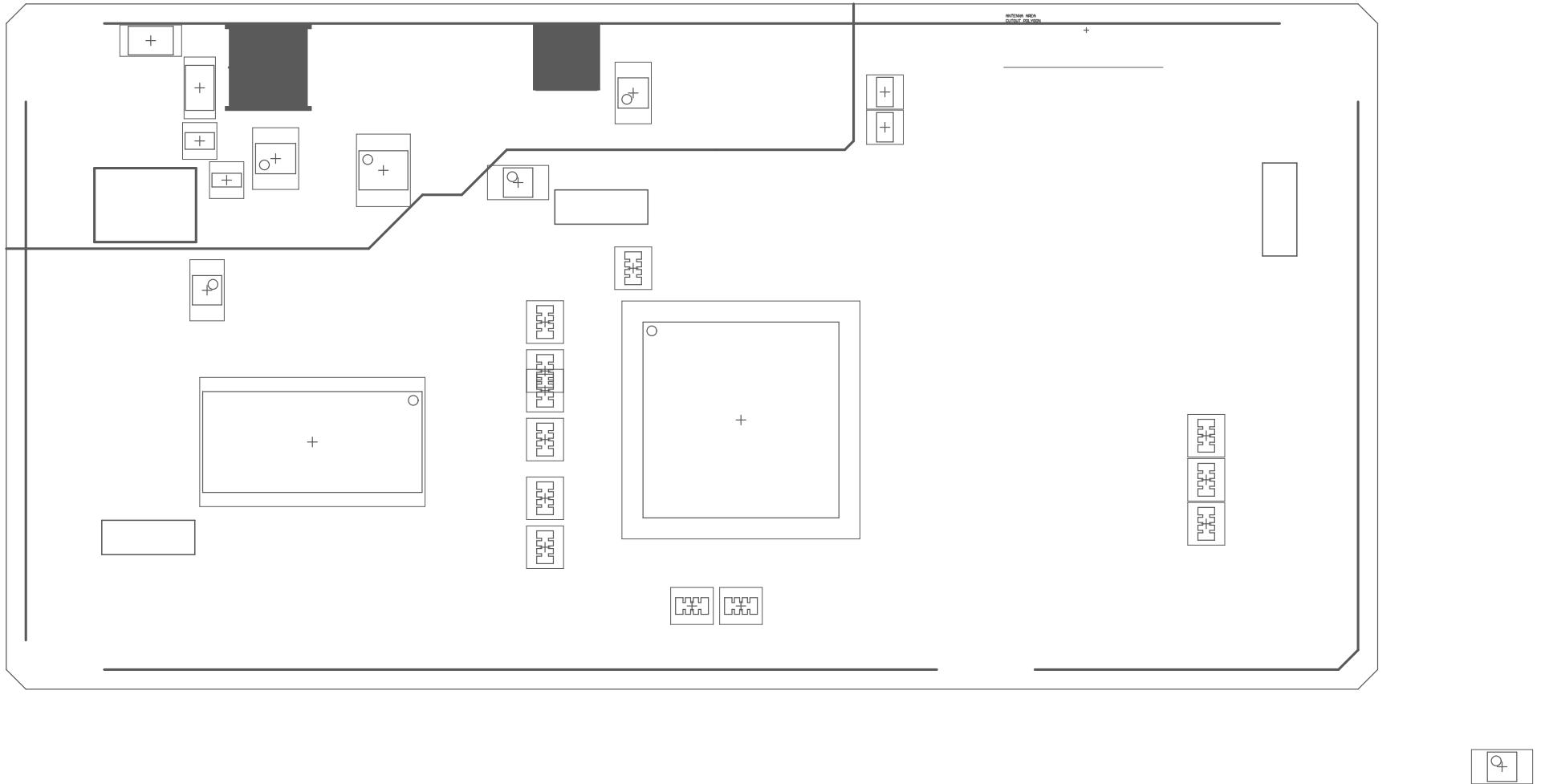
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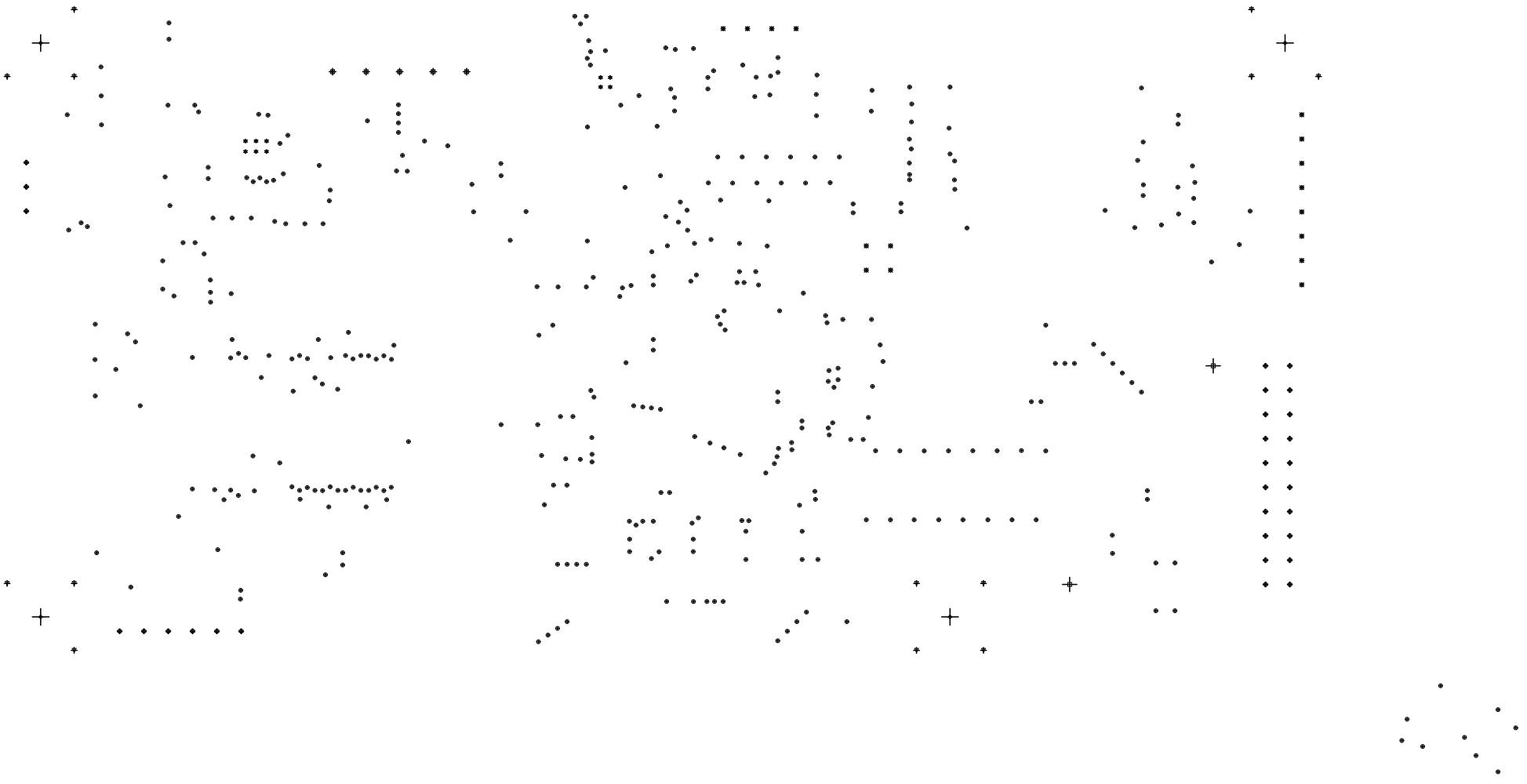
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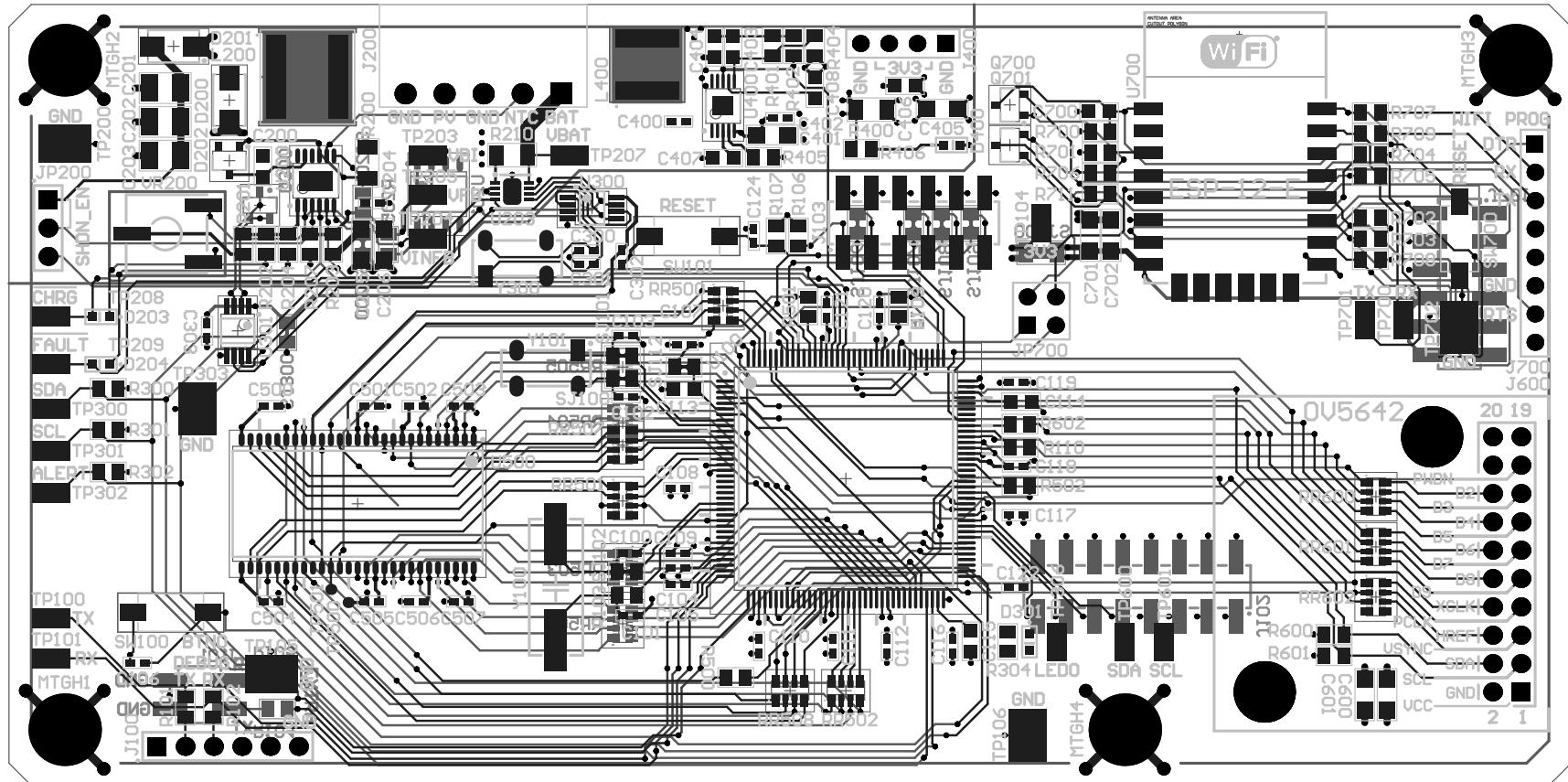
[]











SOLENS

A Fluffy Logic Production

BEN HEBERLEIN
EFFERY LIM
LAJOR Nguyen
JEREMY Rapp
AKIRA Youngblood

GPIO	
MCO2	GND
PB13	GND
PB14	GND
PB15	GND
LEDO	3U3
LED1	GND
LED2	3U3
LED3	GND

	I02
UCC	GND
GND	I00
VCC	CS
GND	MOSI
GND	MISO
GND	CLK

