Electrical Rules Check Report

Class	Document	Message
Warning	Solens.SchDoc	Nets Wire FUEL_AL_L has multiple names (Sheet Entry Z1-FUEL_AL_L(I/O),Sheet Entry Z4-PERIPH_ALERT(I/O),Sheet Entry Z5-A\L\E\R\T\(I/O))
Warning	Solens.SchDoc	Nets Wire I2C2_ALERT has multiple names (Net Label I2C2_ALERT,Net Label PERIPH_ALERT,Sheet Entry Z1-FUEL_AL_L(I/O),Sheet Entry Z4-PERIPH_ALERT(I/O),Sheet Entry Z5-A\L\E\R\T\(I/O))
Warning	Solens.SchDoc	Nets Wire I2C2_SCL has multiple names (Net Label I2C2_SCL,Net Label PERIPH_SCL,Sheet Entry Z1-SCL(I/O),Sheet Entry Z4-PERIPH_SCL(I/O),Sheet Entry Z5-SCL(I/O))
Warning	Solens.SchDoc	Nets Wire I2C2_SDA has multiple names (Net Label I2C2_SDA,Net Label PERIPH_SDA,Sheet Entry Z1-SDA(I/O),Sheet Entry Z4-PERIPH_SDA(I/O),Sheet Entry Z5-SDA(I/O))
Warning	Solens.SchDoc	Nets Wire PWR_CHRG_L has multiple names (Net Label PWR_CHRG_L,Sheet Entry Z1-PV_CHRG_L(Output),Sheet Entry Z4-PV_CHRG_L(Input))
Warning	Solens.SchDoc	Nets Wire PWR_FAULT_L has multiple names (Net Label PWR_FAULT_L,Sheet Entry Z1-PV_FAULT_L(Output),Sheet Entry Z4-PV_FAULT_L(Input))
Warning	Solens.SchDoc	Nets Wire SCL has multiple names (Sheet Entry Z1-SCL(I/O),Sheet Entry Z4-PERIPH_SCL(I/O),Sheet Entry Z5-SCL(I/O))
Warning	Solens.SchDoc	Nets Wire SDA has multiple names (Sheet Entry Z1-SDA(I/O),Sheet Entry Z4-PERIPH_SDA(I/O),Sheet Entry Z5-SDA(I/O))

Design Rules Verification Report

Filename : C:\Users\qux\projects\solenshardware\Altium\Solens\Solens.PcbDoc

Warnings 4
Rule Violations 6

Warnings	
Unplated multi-layer pad(s) detected	4
Total	4

Rule Violations	
Room Z1 (Bounding Region = (2350mil, 6975.984mil, 5224.016mil, 8688.583mil) (InComponentClass('Z1'))	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil)	0
Room Z6 (Bounding Region = (6798.819mil, 5853.937mil, 9003.543mil, 7113.779mil) (InComponentClass('Z6'))	0
Room Z7 (Bounding Region = (6779.134mil, 7172.835mil, 9042.913mil, 8688.583mil) (InComponentClass('Z7'))	0
Width Constraint (Min=8mil) (Max=64mil) (Preferred=8mil) (InNetClass('HVY'))	0
Width Constraint (Min=8mil) (Max=64mil) (Preferred=8mil) (InNetClass('PWR'))	0
Room Z2 (Bounding Region = (5302.756mil, 7468.11mil, 6680.709mil, 8688.583mil) (InComponentClass('Z2'))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	1
Un-Routed Net Constraint ((All))	4
Clearance Constraint (Gap=8mil) (All),(All)	1
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Width Constraint (Min=7mil) (Max=12mil) (Preferred=8mil) (All)	0
Component Clearance Constraint (Horizontal Gap = 1mil, Vertical Gap = 10mil) (All),(All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Hole Size Constraint (Min=8mil) (Max=250mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Silk To Solder Mask (Clearance=2mil) (IsPad),(All)	0
Silk to Silk (Clearance=5mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Clearance Constraint (Gap=0mil) (InComponent('SJ*') And (IsFill Or IsPad Or IsTrack)),(InComponent('SJ*') And (IsFill	0
Short-Circuit Constraint (Allowed=Yes) (InComponent('SJ*') And (IsFill Or IsPad Or IsTrack)),(InComponent('SJ*') And	0
Short-Circuit Constraint (Allowed=Yes) (InComponent('MTGH*') And (IsFill Or IsPad Or IsTrack)),(InComponent('MTG*')	0
Width Constraint (Min=8mil) (Max=120mil) (Preferred=8mil) (InComponent('MTGH*'))	0
Total	6

Unplated multi-layer pad(s) detected
Pad MTGH1-1(196.85mil,196.85mil) on Multi-Layer on Net GND
Pad MTGH2-1(196.85mil,3543.307mil) on Multi-Layer on Net GND
Pad MTGH3-1(6496.063mil,3543.307mil) on Multi-Layer on Net GND
Pad MTGH4-1(6496.063mil,196.85mil) on Multi-Layer on Net GND

Short-Circuit Constraint (Allowed=No) (All),(All)
Short-Circuit Constraint: Between Track (1303.147mil,3059.049mil)(2492.132mil,3059.049mil) on Bottom Layer And Via (2362.205mil,3051.181mil) from

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Unplated Pad MTGH1-1(196.85mil,196.85mil) on Multi-Layer
Un-Routed Net Constraint: Unplated Pad MTGH2-1(196.85mil,3543.307mil) on Multi-Layer
Un-Routed Net Constraint: Unplated Pad MTGH4-1(6496.063mil,196.85mil) on Multi-Layer
Un-Routed Net Constraint: Unplated Pad MTGH3-1(6496.063mil,3543.307mil) on Multi-Layer

Clearance Constraint (Gap=8mil) (All),(All)
Clearance Constraint: (Collision < 8mil) Between Track (1303.147mil,3059.049mil)(2492.132mil,3059.049mil) on Bottom Layer And Via