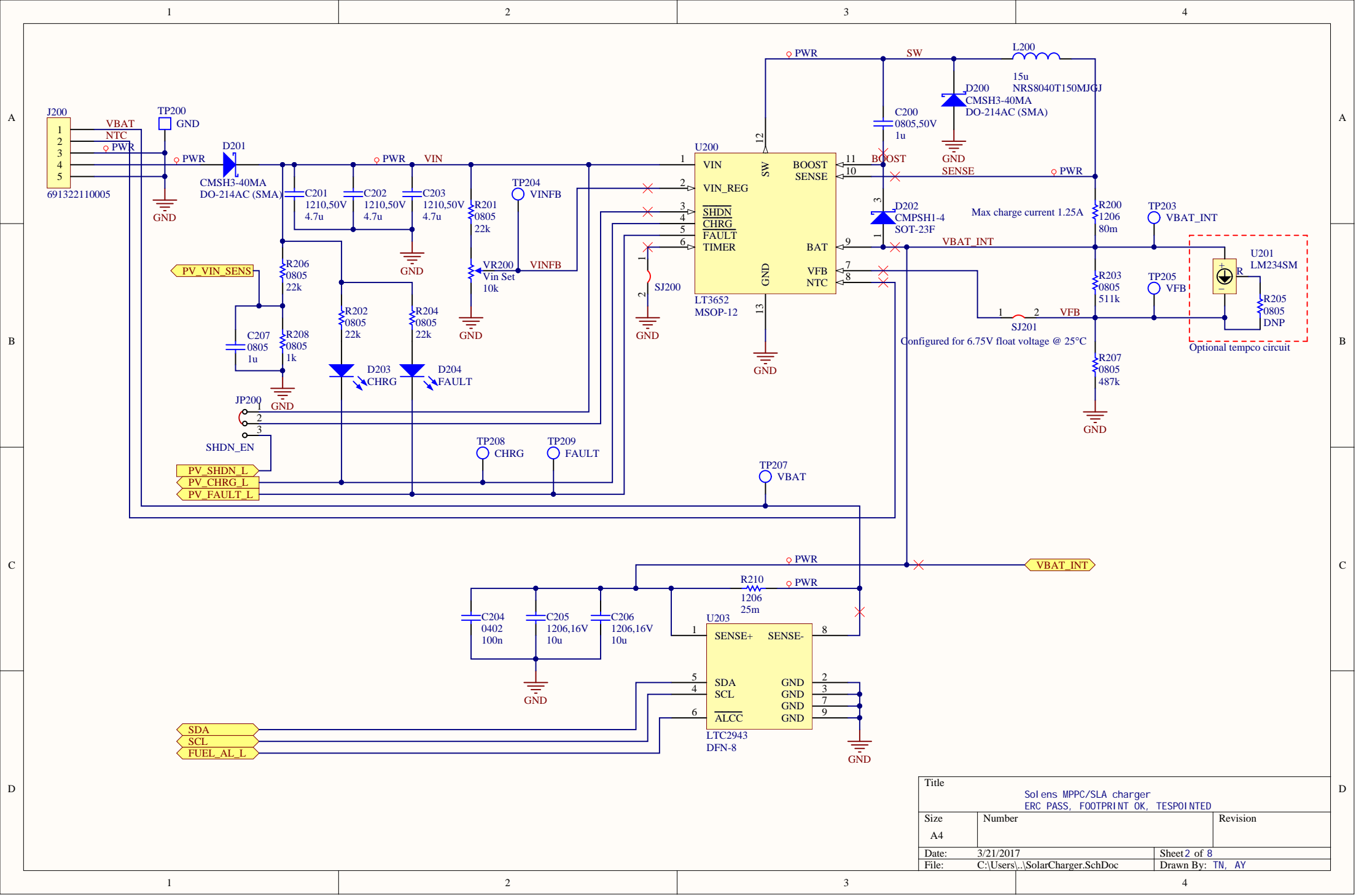
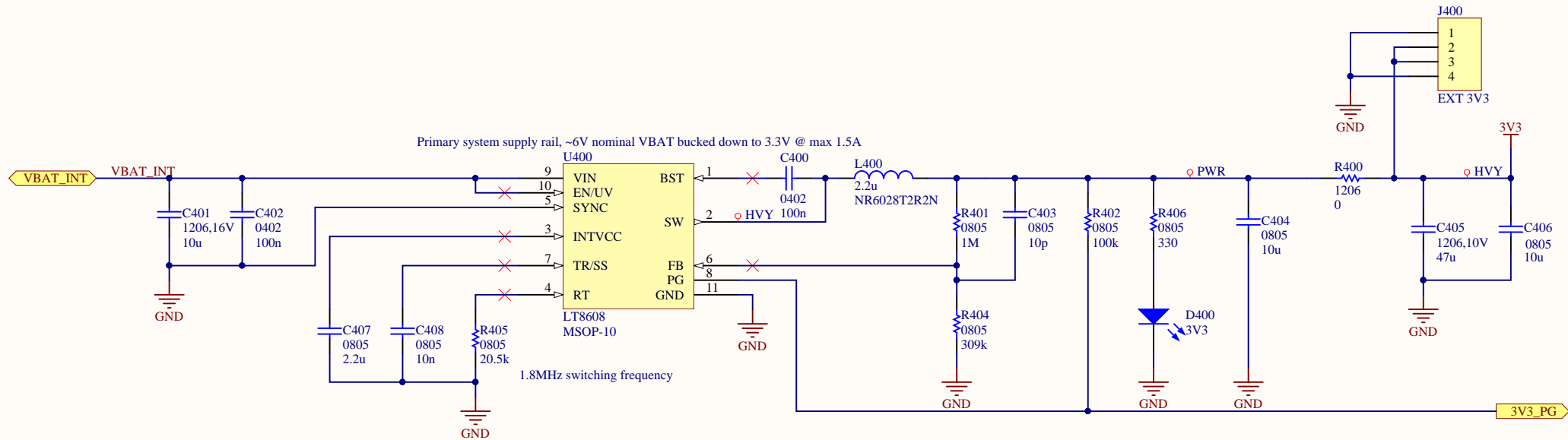


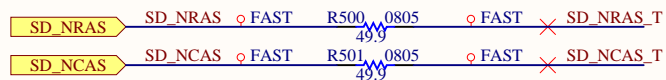
Title		
Solens Camera Subsystem		
ERC WARN, FOOTPRINT N/A		
Size	Number	Revision
A4		
Date:	3/21/2017	Sheet 1 of 8
File:	C:\Users\...\Solens.SchDoc	Drawn By: JL, AY





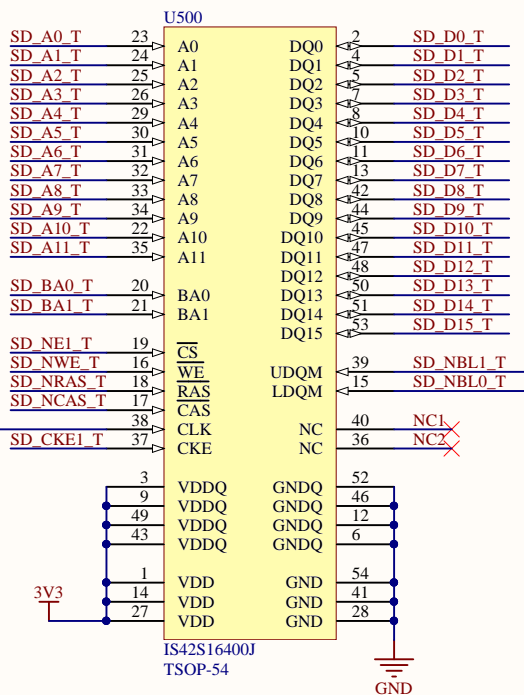
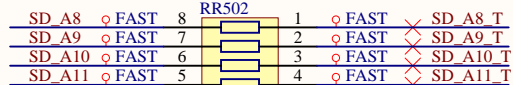
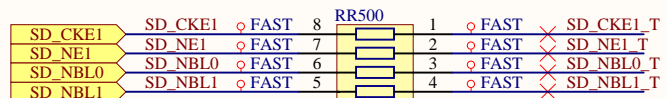
Title		
Solens Voltage Regulators		
ERC PASS, FOOTPRINT OK, TESPOINTED		
Size	Number	Revision
A4		
Date:	3/21/2017	Sheet 3 of 8
File:	C:\Users\...\Regulators.SchDoc	Drawn By: TN, AY

A

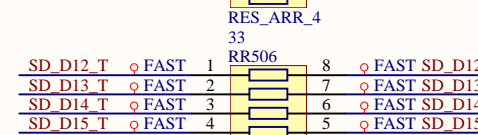
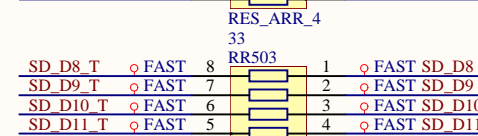
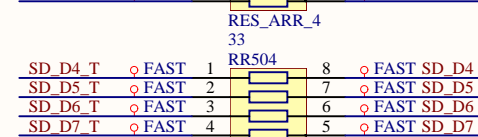
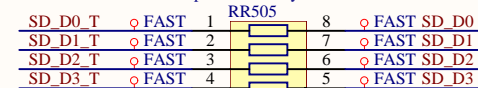


SD_D[0..15] SD_D[0..15]

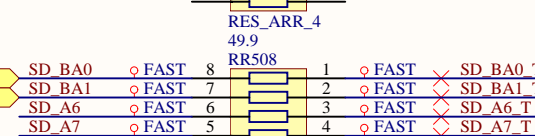
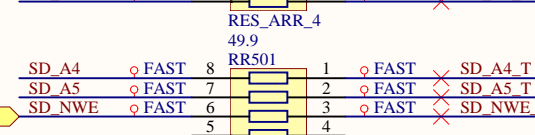
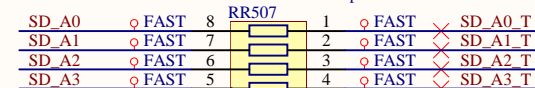
SD_A[0..11] SD_A[0..11]



DATA termination to be placed halfway between MCU and RAM



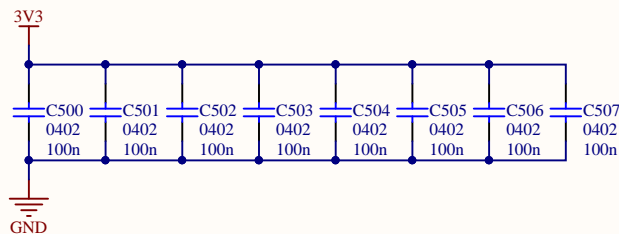
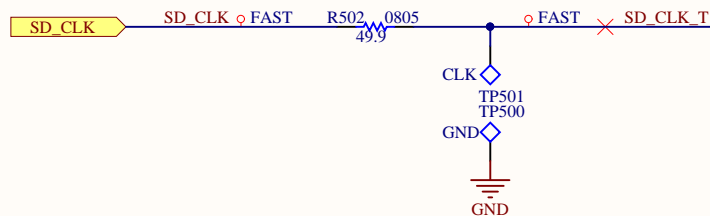
ADDR and CLK termination to be placed at MCU



B

C

D



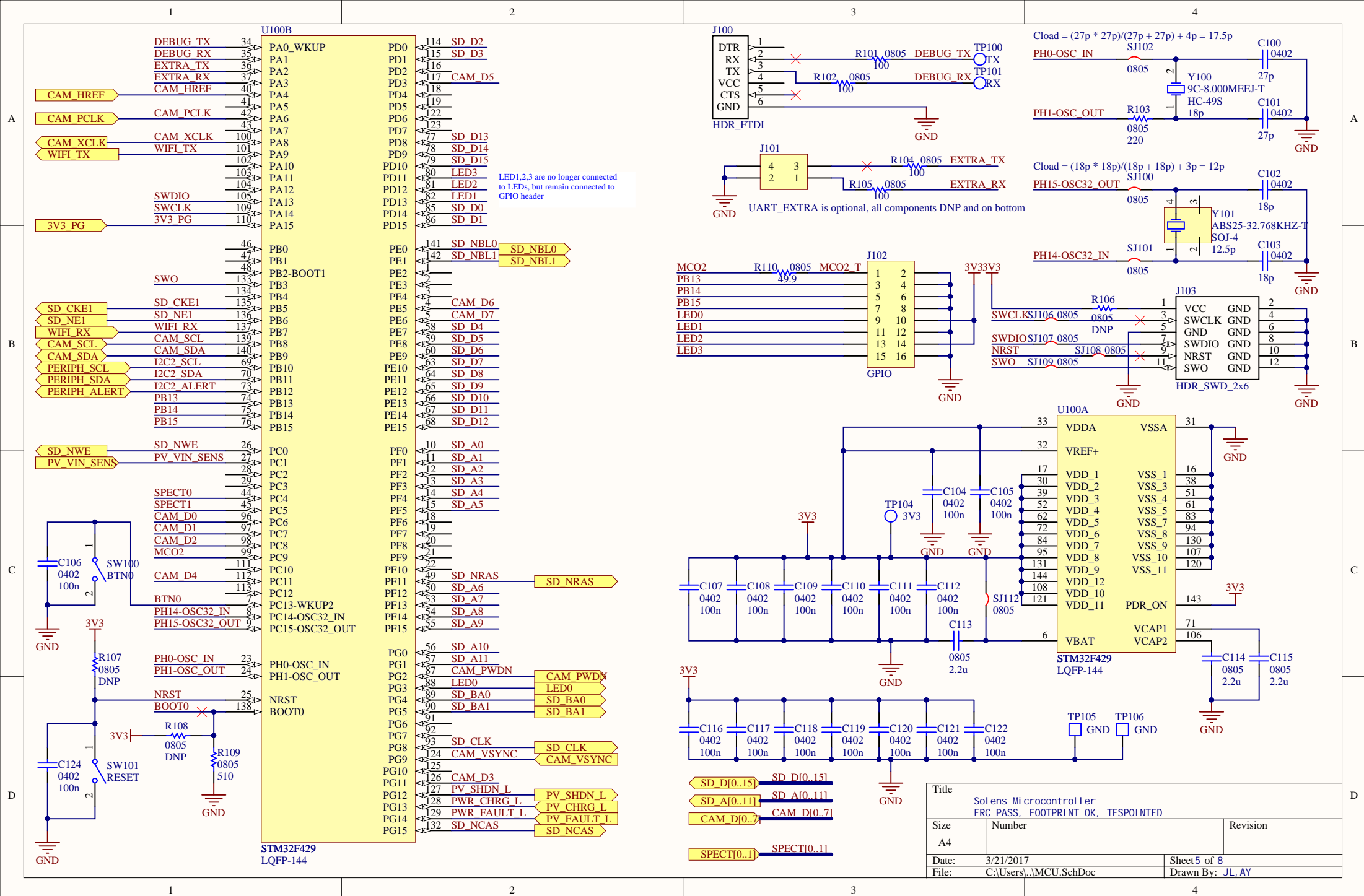
Title		
Solens SDRAM		
ERC PASS, FOOTPRINT OK, TESPOINTED		
Size	Number	Revision
A4		
Date:	3/21/2017	Sheet 4 of 8
File:	C:\Users\...\SDRAM.SchDoc	Drawn By: JL, AV

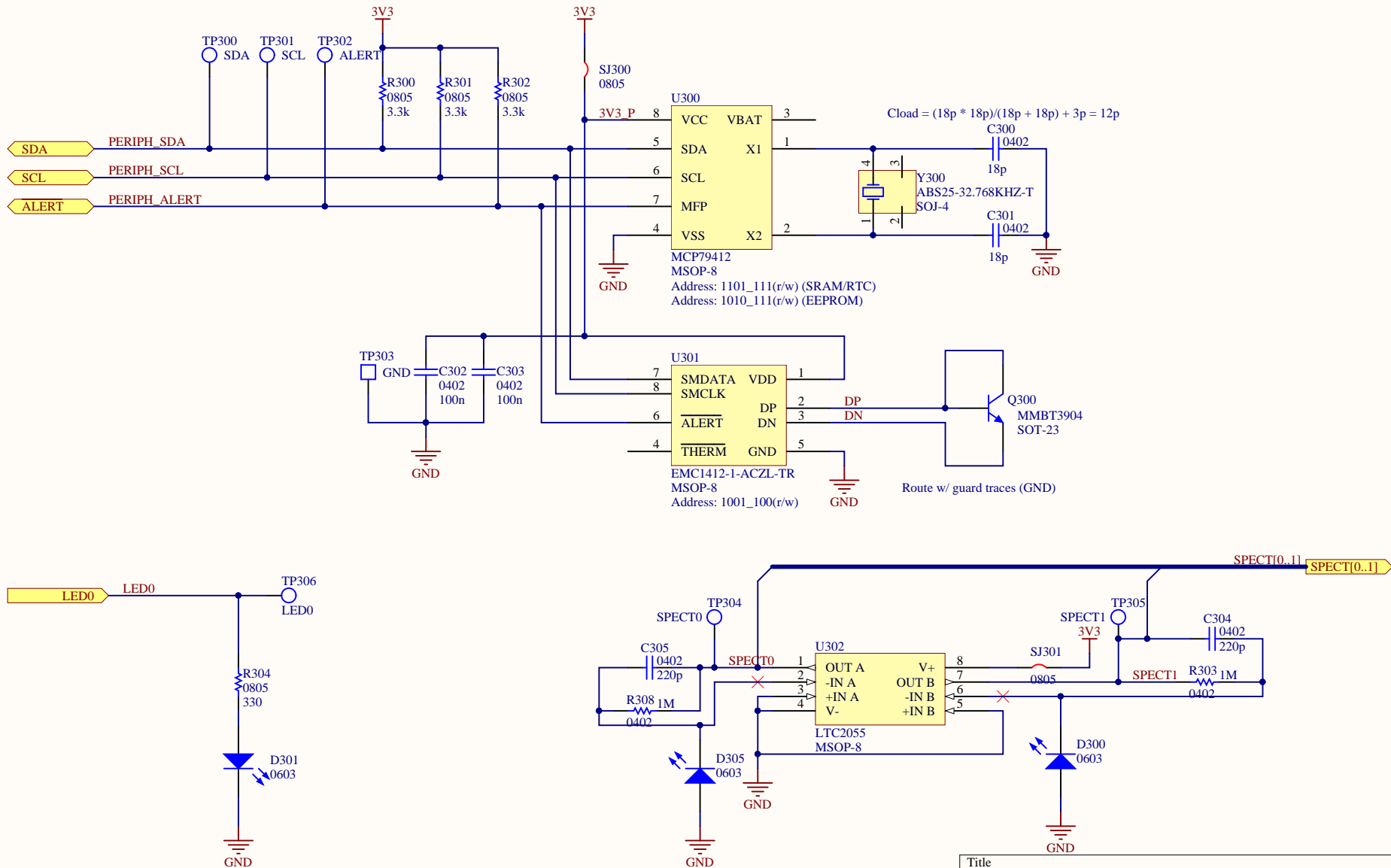
A

B

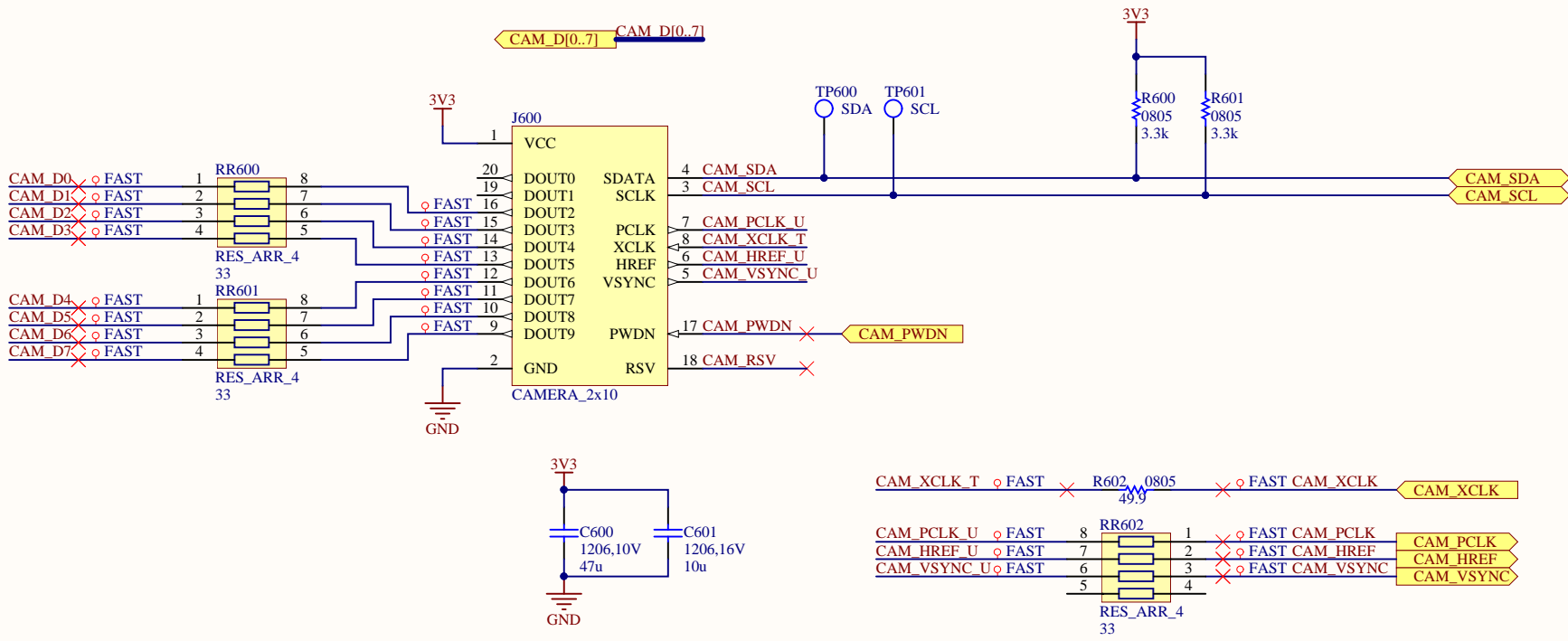
C

D

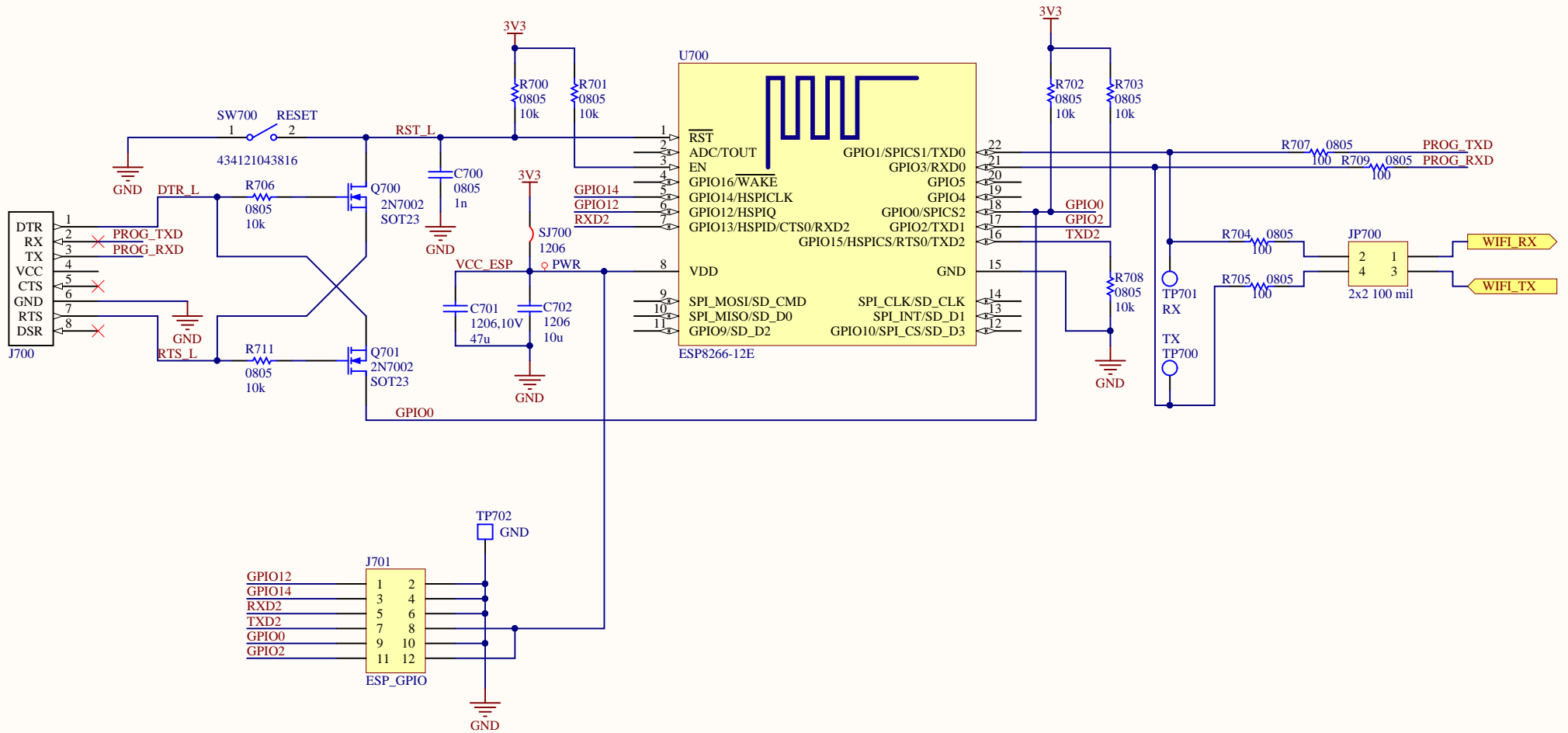




Title		
Solens Peripherals		
ERC PASS, FOOTPRINT OK, TESTPOINTED		
Size	Number	Revision
A4		
Date:	3/21/2017	Sheet 6 of 8
File:	C:\Users\...\Peripherals.SchDoc	Drawn By: AY



Title		
Solens Camera Subsystem		
ERC PASS, FOOTPRINT OK, TESTPOINTED		
Size	Number	Revision
A4		
Date:	3/21/2017	Sheet 7 of 8
File:	C:\Users\...\Camera.SchDoc	Drawn By: JL, AY



Title		
Solens WiFi Subsystem		
ERC PASS, FOOTPRINT OK, TESTPOINTED		
Size	Number	Revision
A4		
Date:	3/21/2017	Sheet 8 of 8
File:	C:\Users\...\WiFi.SchDoc	Drawn By: JL, AY