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4. Juni 2024

Download:

https://github.com/flufpuf/functional_verification_of_fpga_designs_presentation

What is testing? &
Why should we test?

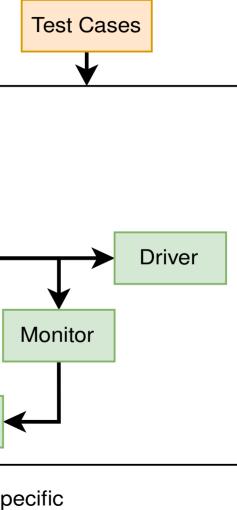


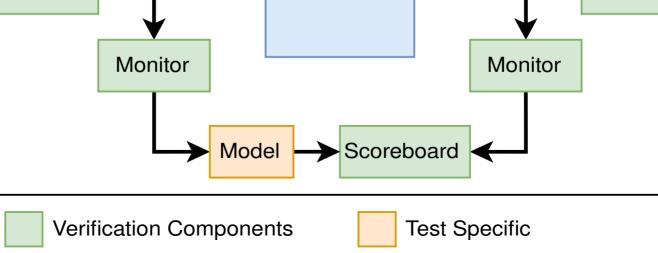
Universal Verification Methodology (UVM)

Testbench

Sequence

Driver



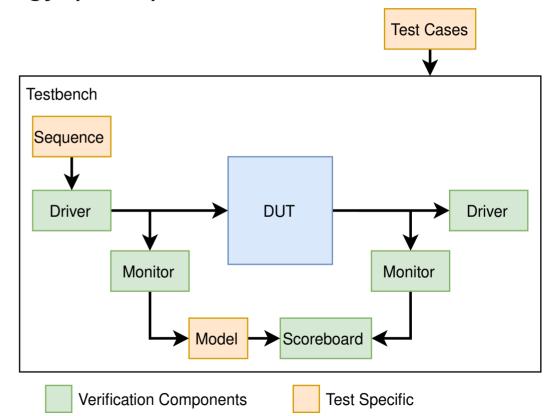


DUT

Universal Verification Methodology (UVM)

- Universal testbench architecture
- Collection of reusable VCs
- Transaction Level Modelling (TLM) as abstracted VC API

Requirement:
Design for Testability (DFT)
(makes live easier)



UVM Standard (Accellera):

https://www.accellera.org/downloads/standards/uvm

Some free and open source tools

OSVVM

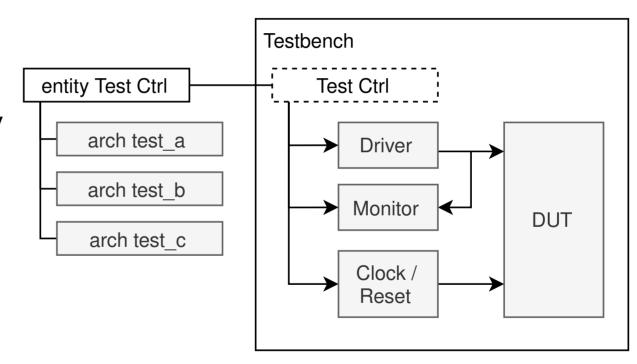
VUnit

Cocotb

- Simulation interface
- Test case management
- Test configuration
- Verification Components
- Transfer Level Modelling (TLM)

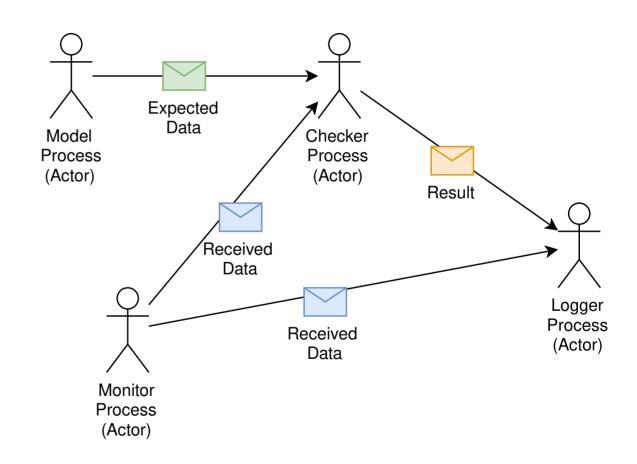
- Randomization
- Assertion checking
- Logging
- Report generation

- Jim Lewis (IEEE VHDL WG Chair)
- Classic VHDL
- Test cases are defined by VHDL configurations
- TCL framework for test management

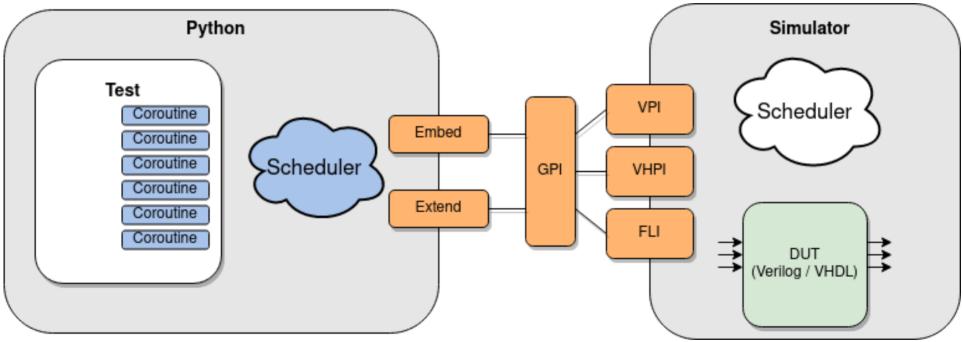


VUnit

- Python
- Simple and powerful
- Test management and configuration
- Actor Model
- Hacked "strong typing" of VHDL



CocoTB

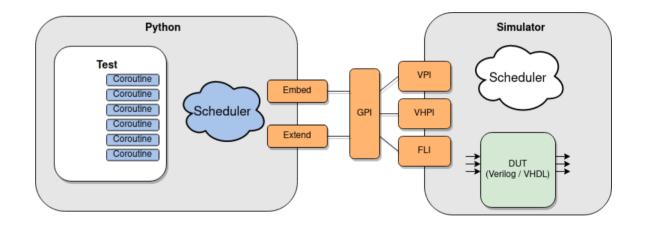


Source: docs.cocotb.org

Verilog Procedural Interface (VPI) VHDL Programming Language Interface (VHPI) Foreign Language Interface (FLI)

CocoTB

- DUT runs in Simulator
- Testbench runs in python
- Based on python coroutines (asyncio)
- All python features can be used



Source: docs.cocotb.org

Verilog Procedural Interface (VPI)
VHDL Programming Language Interface (VHPI)
Foreign Language Interface (FLI)

Appendix

Links

- UVM Standard (Accellera): https://www.accellera.org/downloads/standards/uvm
- OSVVM: https://osvvm.org/ and https://github.com/OSVVM
- Vunit: https://vunit.github.io/ and https://github.com/VUnit/vunit
- Cocotb: https://www.cocotb.org/ and https://github.com/cocotb/cocotb
- GHDL: https://github.com/ghdl/ghdl
- gtkwave: https://github.com/gtkwave/gtkwave
- NVC: https://github.com/nickg/nvc