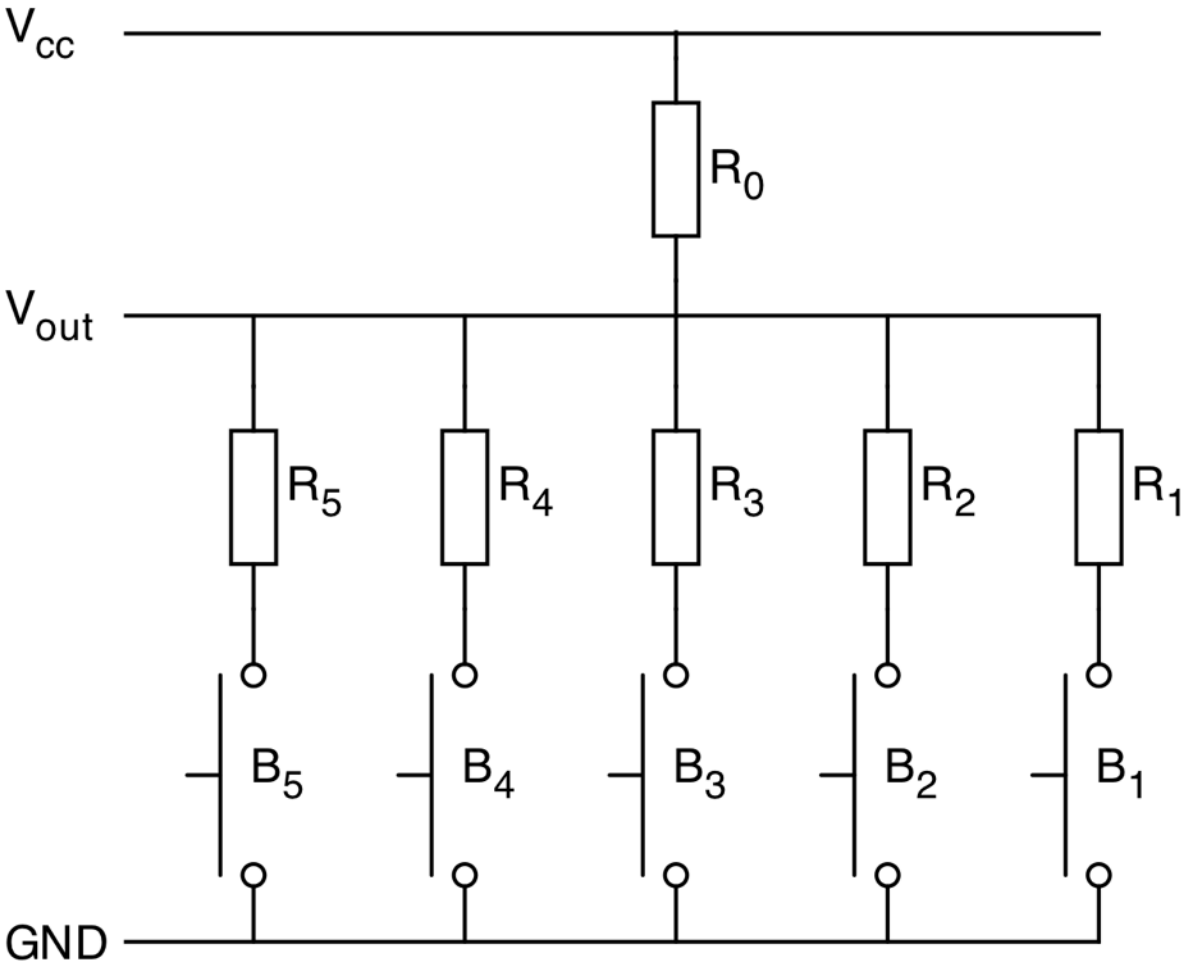
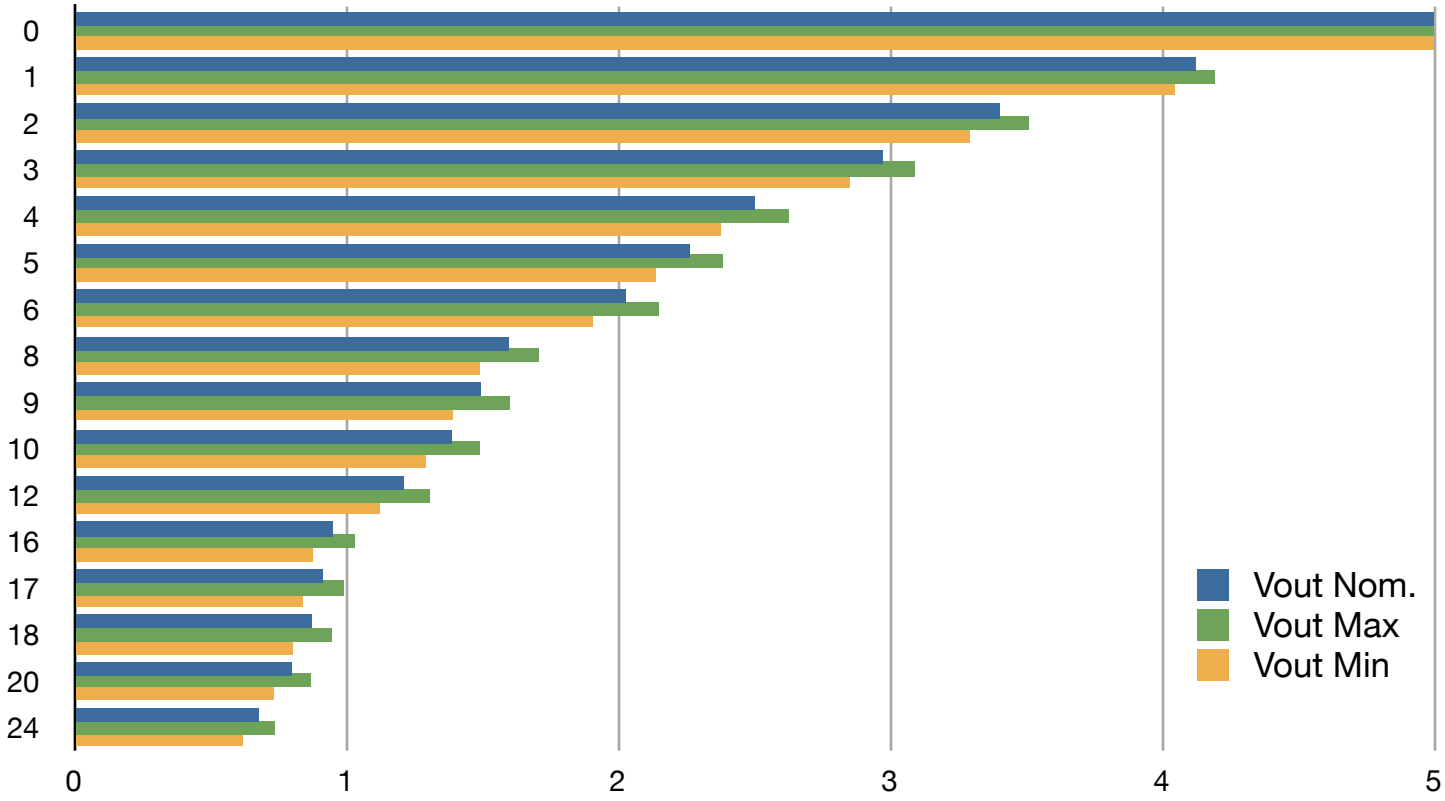
Resistor Ladder Analysis



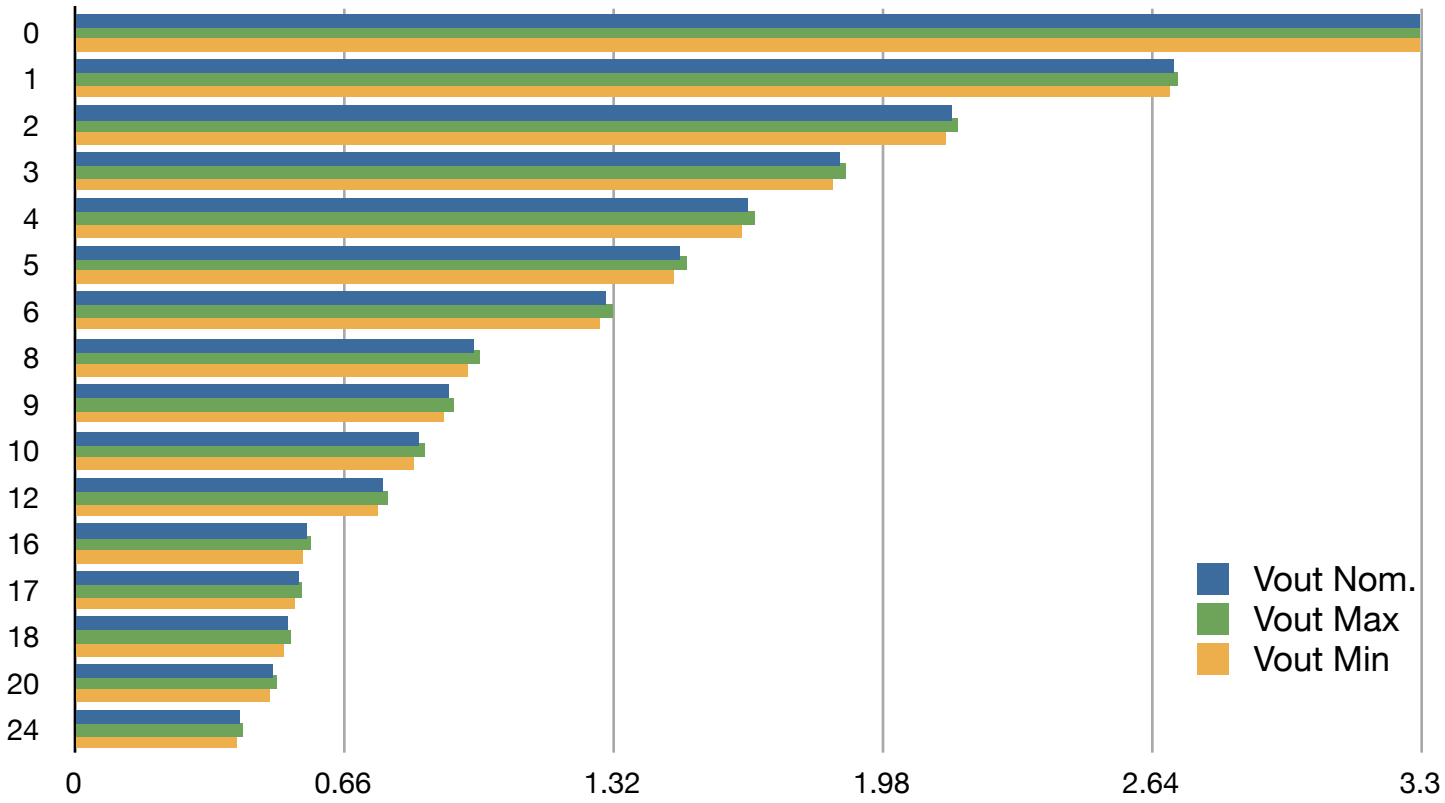
Configuration of the Resistor Ladder for the AnalogFiveButtons Arduino Library

The following graphs are showing examples of the resistor ladder Vout for the 16 combination of the switches states (1 and 2 switches down). The first graph is for Vcc=5V and a set of resistors at 5% tolerance. The second graph is for Vcc=3.3V and resistor at 1% tolerance.
The blue bars show Vout if the resistors were perfectly calibrated. The green and yellow bars show the maximum and minimum Vout for values of the resistors at the limits of their tolerances. The most de-favorable cases are $R_{0\text{-}min} + R_{1\text{-}min}\text{-}R_{5\text{-}min}$ and $R_{0\text{-}min} + R_{1\text{-}max}\text{-}R_{5\text{-}max}$.
The graphs illustrate how the voltage difference between successive switches states is decreasing as the resistor combination uses higher values. Depending the resistor combination chosen and the tolerance, it may not be possible to detect the right state. For example, for the 5% ladder, state 20 max is in fact greater than state 18 min! This is even exemplified if you take into account the limited accuracy of the analog to digital converter. The last column of the table show when the wrong state will be detected with a 8 bit ADC.
This means that you should either choose resistors with precise tolerance, or measure the actual values of the resistors on your specific board and uses them to configure the ladder.

Analog Input with 5% resitors - Max 2 buttons simultaneously



Analog Input with 1% resitors - Max 2 buttons simultaneously



Ladder 5% - 5V

	B5	B4	B3	B2	B1	Req	Vout Nom.	Req	Vout Max	Req	Vout Min	
						Log Ladder		*Log R-5%*		*Log R+5%*		*8bit ADC*
0	0	0	0	0	0	inf.	5.00	inf.	5	inf.	5	
1	0	0	0	0	1	22.00	4.12	23.10	4.19	20.90	4.04	OK
2	0	0	0	1	0	10.00	3.40	10.50	3.51	9.50	3.29	OK
3	0	0	0	1	1	6.88	2.97	7.22	3.09	6.53	2.85	OK
4	0	0	1	0	0	4.70	2.50	4.94	2.63	4.47	2.38	ERROR
5	0	0	1	0	1	3.87	2.26	4.07	2.38	3.68	2.14	ERROR
6	0	0	1	1	0	3.20	2.02	3.36	2.15	3.04	1.90	OK
7	0	0	1	1	1	2.79	1.86	2.93	1.98	2.65	1.75	
8	0	1	0	0	0	2.20	1.59	2.31	1.70	2.09	1.49	ERROR
9	0	1	0	0	1	2.00	1.49	2.10	1.60	1.90	1.39	ERROR
10	0	1	0	1	0	1.80	1.39	1.89	1.49	1.71	1.29	ERROR
11	0	1	0	1	1	1.67	1.31	1.75	1.41	1.58	1.21	
12	0	1	1	0	0	1.50	1.21	1.57	1.30	1.42	1.12	OK
13	0	1	1	0	1	1.40	1.15	1.47	1.24	1.33	1.06	
14	0	1	1	1	0	1.30	1.09	1.37	1.17	1.24	1.00	
15	0	1	1	1	1	1.23	1.04	1.29	1.12	1.17	0.96	
16	1	0	0	0	0	1.10	0.95	1.16	1.03	1.05	0.87	ERROR
17	1	0	0	0	1	1.05	0.91	1.10	0.99	1.00	0.84	ERROR
18	1	0	0	1	0	0.99	0.87	1.04	0.94	0.94	0.80	ERROR
19	1	0	0	1	1	0.95	0.84	1.00	0.91	0.90	0.77	
20	1	0	1	0	0	0.89	0.80	0.94	0.87	0.85	0.73	ERROR
21	1	0	1	0	1	0.86	0.77	0.90	0.84	0.81	0.71	
22	1	0	1	1	0	0.82	0.74	0.86	0.81	0.78	0.68	
23	1	0	1	1	1	0.79	0.72	0.83	0.78	0.75	0.66	
24	1	1	0	0	0	0.73	0.67	0.77	0.74	0.70	0.62	
25	1	1	0	0	1	0.71	0.66	0.75	0.72	0.67	0.60	
26	1	1	0	1	0	0.68	0.63	0.72	0.69	0.65	0.58	
27	1	1	0	1	1	0.66	0.62	0.70	0.67	0.63	0.57	
28	1	1	1	0	0	0.63	0.59	0.67	0.65	0.60	0.54	
29	1	1	1	0	1	0.62	0.58	0.65	0.63	0.59	0.53	
30	1	1	1	1	0	0.60	0.56	0.63	0.62	0.57	0.52	
31	1	1	1	1	1	0.58	0.55	0.61	0.60	0.55	0.50	
						4.7	*Rd*	4.465	*Rd*	4.935	*Rd*	
						1.1	*R5*	1.155	*R5*	1.045	*R5*	
						2.2	*R4*	2.31	*R4*	2.09	*R4*	
						4.7	*R3*	4.935	*R3*	4.465	*R3*	
						10	*R2*	10.5	*R2*	9.5	*R2*	
						22	*R1*	23.1	*R1*	20.9	*R1*	
						5	*Vcc*	5	*Vcc*	5	*Vcc*	

Ladder 1% - 3.3V

	B5	B4	B3	B2	B1	Req	Vout Nom.	Req	Vout Max	Req	Vout Min		
						Log Ladder		*Log R-1%*		*Log R+1%*		*8bit ADC*	
0	0	0	0	0	0	inf.	3.30	inf.	3.3	inf.	3.3	Nom. Step	
1	0	0	0	0	1	22.10	2.69	22.32	2.70	21.88	2.68	OK	0.544
2	0	0	0	1	0	9.31	2.15	9.40	2.16	9.22	2.13	OK	0.275
3	0	0	0	1	1	6.55	1.87	6.62	1.89	6.48	1.86	OK	0.223
4	0	0	1	0	0	4.99	1.65	5.04	1.67	4.94	1.63	OK	0.167
5	0	0	1	0	1	4.07	1.48	4.11	1.50	4.03	1.47	OK	0.181
6	0	0	1	1	0	3.25	1.30	3.28	1.32	3.22	1.29	OK	0.324
7	0	0	1	1	1	2.83	1.19	2.86	1.21	2.80	1.18		
8	0	1	0	0	0	2.10	0.98	2.12	0.99	2.08	0.96	OK	0.061
9	0	1	0	0	1	1.92	0.92	1.94	0.93	1.90	0.90	OK	0.073
10	0	1	0	1	0	1.71	0.84	1.73	0.86	1.70	0.83	OK	0.089
11	0	1	0	1	1	1.59	0.80	1.61	0.81	1.57	0.79		
12	0	1	1	0	0	1.48	0.75	1.49	0.77	1.46	0.74	OK	0.185
13	0	1	1	0	1	1.39	0.72	1.40	0.73	1.37	0.71		
14	0	1	1	1	0	1.28	0.67	1.29	0.68	1.26	0.66		
15	0	1	1	1	1	1.21	0.64	1.22	0.65	1.19	0.63		
16	1	0	0	0	0	1.04	0.57	1.05	0.58	1.03	0.56	OK	0.021
17	1	0	0	0	1	0.99	0.55	1.00	0.56	0.98	0.54	OK	0.027
18	1	0	0	1	0	0.93	0.52	0.94	0.53	0.93	0.51	OK	0.036
19	1	0	0	1	1	0.90	0.50	0.91	0.51	0.89	0.49		
20	1	0	1	0	0	0.86	0.49	0.87	0.49	0.85	0.48	OK	0.082
21	1	0	1	0	1	0.83	0.47	0.84	0.48	0.82	0.46		
22	1	0	1	1	0	0.79	0.45	0.80	0.46	0.78	0.44		
23	1	0	1	1	1	0.76	0.44	0.77	0.44	0.75	0.43		
24	1	1	0	0	0	0.70	0.40	0.70	0.41	0.69	0.40		
25	1	1	0	0	1	0.67	0.39	0.68	0.40	0.67	0.39		
26	1	1	0	1	0	0.65	0.38	0.65	0.39	0.64	0.37		
27	1	1	0	1	1	0.63	0.37	0.63	0.38	0.62	0.36		
28	1	1	1	0	0	0.61	0.36	0.62	0.37	0.60	0.35		
29	1	1	1	0	1	0.59	0.35	0.60	0.36	0.59	0.34		
30	1	1	1	1	0	0.57	0.34	0.58	0.35	0.57	0.33		
31	1	1	1	1	1	0.56	0.33	0.56	0.34	0.55	0.33		
						4.99	*Rd*	4.9401	*Rd*	5.0399	*Rd*	*1/512*	*0.0020*
						1.039	*R5*	1.04939	*R5*	1.02861	*R5*		
						2.1	*R4*	2.121	*R4*	2.079	*R4*		
						4.99	*R3*	5.0399	*R3*	4.9401	*R3*		
						9.31	*R2*	9.4031	*R2*	9.2169	*R2*		
						22.1	*R1*	22.321	*R1*	21.879	*R1*		
						3.3	*Vcc*	3.3	*Vcc*	3.3	*Vcc*		