

IARPA SuperTools Deliverable

# **ColdFlux Logic Cell Library for MIT-LL SFQ Process**

*Submitted by*

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Version 2.0

# Version History

- **Version 2.0:** This version updates the AQFP and RSFQ logic cell libraries for SuperTools phase 2, and combines both libraries in a single document.
- **Version 1.5:** Previous release of AQFP Logic cell library document.
- **Version 1.1:** Previous release of RSFQ Logic cell library document.

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# **Part I**

## **AQFP Logic**

# 1. Introduction and Setup

## 1.1 Introduction

With our proposed minimalist design methodology, standard cell libraries have been built for MIT 10 kA/cm<sup>2</sup> Nb/Al-AlO<sub>x</sub>/Nb tri-layer process. This cell library contains the basic logic cells, on-chip interfaces and off-chip interfaces as listed below. All cells are driven by 4-phase clock generated by 2 AC sources and a DC source [1].

All views of the cell library were developed using Xic from the XicTools suite [2]. Section 1.3 details our naming conventions used for this cell library and the full list of cells is shown in Section 1.4. The library files for circuit design are GDS files that can be opened in Xic. Each GDS file embeds the schematic, symbol, and physical layout for each logic cell. While the physical layout can be viewed by other GDS viewers, one should not overwrite the data outside of Xic or other data such as the schematic and symbol may be lost. Moving forward, we are considering the OpenAccess format to improve interoperability with other tools.

The components of each cell are listed as follows:

- **Symbol:** Symbol view of a cell is designed in Xic and provides a hierarchical way to build digital logic circuits. It is a simple symbol with terminal (I/O) definitions. It is embedded into the GDS file of the cell, usable only in Xic.
- **Schematic:** Schematic view of the cell designed in Xic. The circuit parameters have been extracted from the physical layout using InductEx [3]. It is embedded into the GDS file of the cell, usable only in Xic.
- **Layout:** The physical layout of the cell designed in Xic. It is embedded into the GDS file of the cell, and it is readable not just in Xic but potentially other GDS viewers.
- **Netlist:** An .elecnet format netlist exported by Xic for each logic cell.
- **Analog waveform:** Using the analog circuit testbenches included in the cell library, functionality was confirmed using WRspice.
- **Verilog model:** Behavior-level model of a cell with built-in timing specification block. It is written in hardware-description-language (HDL) Verilog and can be found as a separate file named ‘CellName.v’ under the **verilog** sub-directory. Each cell model has an embedded module named ‘biasDir\_b.v’ as an I/O interface to produce a normalized clock based on the relative directions the AC and DC current.

- **SDF:** Standard delay format file. Generated by the AQFP timing extraction tool AQFPTX [4].
- **Digital waveform:** Generated by the open source Verilog simulator Icvarus-Verilog [5] and viewed using the open source wave viewer GTKWave [6].
- **Switching energy:** Switching energies of each logic cell are simply calculated based on the energy table of four building blocks, buffer, inverter, constant 0 and constant 1 at present. Further investigations will be performed for more precise estimation of the complex logic cells. The energy tables are generated using the methodology described in [7]. Essentially, we can calculate the switching energy from analog simulation using the following formula:  $E_{\text{total}} = \int_0^{1/f} V_x(t)I_x(t)dt$ , where  $V_x(t)$  is the voltage across the excitation inductor of an AQFP cell,  $I_x(t)$  is the current going through the same excitation inductor, and  $f$  is the operating frequency.

## 1.2 Cell library structure

```
coldflux-aqfp-cell-library
|   README.md <--> readme file
|
|--- lib_jjmit <--> tech file, GDS cells (schematic, symbol, layout)
|   |   doc <--> PDF of current documentation of the library
|   |   verilog <--> Verilog models including global SDF
|
|--- legacy <--> old files and documentation for reference purposes.
|   |   cell-lib-doc-resources <--> contains .docx files for PDFs.
```

## 1.3 Conventions

The logic gates are named using the following convention:

`<gate><inputs>_<polarities>`

Table 1.1 describes in detail the different naming components and Table 1.2 shows some examples. Table 1.3 lists the pin naming conventions as well.

**Table 1.1:** Naming convention of AQFP logic cells.

Name Component	Description
<b>&lt;gate&gt;</b>	This is the shortened name of the gate. In the case where the gate has one or zero (e.g., constant cells) inputs, we simply use the <b>&lt;gate&gt;</b> .
<b>&lt;inputs&gt;</b>	This is the number of logic inputs, i.e., the number of inputs that directly produces the logic function. It doesn't include clocking inputs. In the case of fan-out circuits ( <b>sp12</b> , <b>sp13</b> ), the number indicates number of outputs/fan-out.
<b>&lt;polarities&gt;</b>	For each logic input $i$ ( $a, b, c, d\dots$ ), we designate its polarity as positive ( <b>p</b> ) or negative ( <b>n</b> ). The polarity mainly applies to Boolean logic gates like MAJ, OR, and AND. It is not used for splitter ( <b>sp12</b> or <b>sp13</b> ), for example. The ordering explicitly specifies exactly which input is which polarity. For example: <b>ppn</b> designates that input $a$ is positive, input $b$ is positive, and input $c$ is negative.

**Table 1.2:** Naming examples and explanations.

Name	Explanation
<b>maj3_ppn</b>	A 3-input majority gate. Input $a$ is positive, input $b$ is positive, and input $c$ is negative.
<b>or2_pp</b>	A 2-input OR gate. Both input $a$ and $b$ are positive inputs.
<b>sp13</b>	A 1-input to 3-output splitter/fan-out.

**Table 1.3:** Pin naming conventions.

Name	Convention
Input	$a, b, c, d\dots$
Output (single)	$q$
Output (multi)	$q0, q1, q2\dots$
AC excitation (single)	$xin / xout$
AC excitation (multi)	$xin1, xin2, xin3\dots / xout1, xout2, xout3\dots$
DC offset (single)	$dcin / dcout$
DC offset (multi)	$dcin1, dcin2, dcin3\dots / dcout1, dcout2, dcout3\dots$

## 1.4 Full List of AQFP Cells

Table 1.4 shows a full listing of our AQFP cells. The cell name, type of cell, number of Josephson junctions (JJs), height and width in  $\mu\text{m}$ , and the Boolean function for each cell is shown. Type is defined as follows: ‘S’ refers to sub-cells which are used only for building logic cells and are not normally used standalone; ‘C’ refers to normal logic cells which are used to build digital circuits; ‘B’ refers to structures that can be both ‘S’ and ‘C’; ‘M’ refers to macro-type cells which are composed of ‘B’ or ‘C’ type cells. ‘M’ type cells do not have a fixed area as its own placement is dependent on how other neighboring cells are also arranged. ‘I’ type cells are interface cells for communicating off-chip or on-chip between AQFP-SFQ logic families.

**Table 1.4:** Summary listing of all AQFP cells to date.

Cell Name	Type	JJs	Height ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Boolean Function
bfr	B	2	44	22	$q = a$
inv	B	2	44	22	$q = \bar{a}$
const0	B	2	44	22	$q = 0$
const1	B	2	44	22	$q = 1$
spl2	C	2	64	44	$q_0, q_1 = a$
spl3	C	2	64	66	$q_0, q_1, q_2 = a$
spl4	C	2	64	88	$q_0, q_1, q_2, q_3 = a$
maj3_ppp	C	6	64	66	$q = \text{MAJ}(a, b, c) = ab + ac + bc$
maj3_ppn	C	6	64	66	$q = \text{MAJ}(a, b, \bar{c}) = ab + a\bar{c} + b\bar{c}$
maj3_pnp	C	6	64	66	$q = \text{MAJ}(a, \bar{b}, c) = a\bar{b} + ac + \bar{b}c$
maj3_pnn	C	6	64	66	$q = \text{MAJ}(a, \bar{b}, \bar{c}) = a\bar{b} + a\bar{c} + \bar{b}\bar{c}$
maj3_npp	C	6	64	66	$q = \text{MAJ}(\bar{a}, b, c) = \bar{a}b + \bar{a}c + bc$
maj3_npn	C	6	64	66	$q = \text{MAJ}(\bar{a}, b, \bar{c}) = \bar{a}b + \bar{a}\bar{c} + b\bar{c}$
maj3_nn	C	6	64	66	$q = \text{MAJ}(\bar{a}, \bar{b}, c) = \bar{a}\bar{b} + \bar{a}c + \bar{b}c$
maj3_nnn	C	6	64	66	$q = \text{MAJ}(\bar{a}, \bar{b}, \bar{c}) = \bar{a}\bar{b} + \bar{a}\bar{c} + \bar{b}\bar{c} = \text{MIN}(a, b, c)$
maj5_ppppp	C	10	64	110	$q = \text{MAJ}(a, b, c, d, e) = abc + abd + abe + acd + ace + ade + bcd + bce + bde + cde$
and2_pp	C	6	64	66	$q = ab$

Continued on the next page...

**Table 1.4:** (Continued from previous page.)

Cell Name	Type	JJs	Height ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Boolean Function
and2_pn	C	6	64	66	$q = a\bar{b}$
and2_np	C	6	64	66	$q = \bar{a}b$
and2_nn	C	6	64	66	$q = \bar{a}\bar{b} = \overline{a + b}$
or2_pp	C	6	64	66	$q = a + b$
or2_pn	C	6	64	66	$q = a + \bar{b}$
or2_np	C	6	64	66	$q = \bar{a} + b$
or2_nn	C	6	64	66	$q = \bar{a} + \bar{b} = \overline{ab}$
qfp1	C	6	94	44	$q' = a(\overline{a \oplus b}) + q(a \oplus b)$
dff	M	26	N/A	N/A	$q' = de + q\bar{e}$
branch2	S	0	20	44	$q_0, q_1 = a$
branch3	S	0	20	66	$q_0, q_1, q_2 = a$
branch4	S	0	20	88	$q_0, q_1, q_2, q_3 = a$
branch5	S	0	20	110	$q_0, q_1, q_2, q_3, q_4 = a$
storage_gate	S	2	30	44	N/A
qdc	I	8	110	22	N/A
aqfp2rsfq	I	10	100	55	N/A
rsfq2aqfp	I	4	40	35	N/A

## 1.5 Roadmap

- **Timing checks (Phase 2B):** Currently, the timing checks are preliminary due to limited support in vanilla Icarus Verilog and due to tool lag with qVsim. We will ensure the timing checks are working under USC's SDF compatible Verilog simulator qVsim.
- **Implement new layout architecture (Phase 2B):** The current RSFQ cell library has been modified to use a new routing architecture as described in [8]. It is compatible with the general design principles for AQFP logic. The establishment of this track routing architecture is a key step towards converging into a universal library that supports both AQFP and RSFQ logic. This would be a substantial redesign of the AQFP logic cells, but would enable a more systematic and consistent approach towards satisfying various density requirements that the MIT LL SFQ5ee process has. It will also further improve interoperability between AQFP and RSFQ

circuits.

- **Cell library data format (Phase 2B):** During Phase 2A, we have been experimenting with OpenAccess (OA) data format with some success in Xic, and it is a possible candidate moving forward instead of using a collection of schematic/symbol-embedded GDS files or native Xic files.
- **Reconcile interfaces (Phase 3):** Currently, we designed our AQFP $\leftrightarrow$ RSFQ interfaces using generic RSFQ components, and not with the current RSFQ cell library available now (as it was under redesign). Related to the above plan, we will improve our interfaces so that they are using the same RSFQ structures that SU uses.
- **SPIRA-enabled layouts (Phase 3):** The basic AQFP cell (**bfr**) has been parameterized via SPIRA already but has not been modified to use the new routing architecture. After a re-design of the cells to use the new architecture, we plan to revisit layout parameterization again.

## 2. AQFP Cell Library

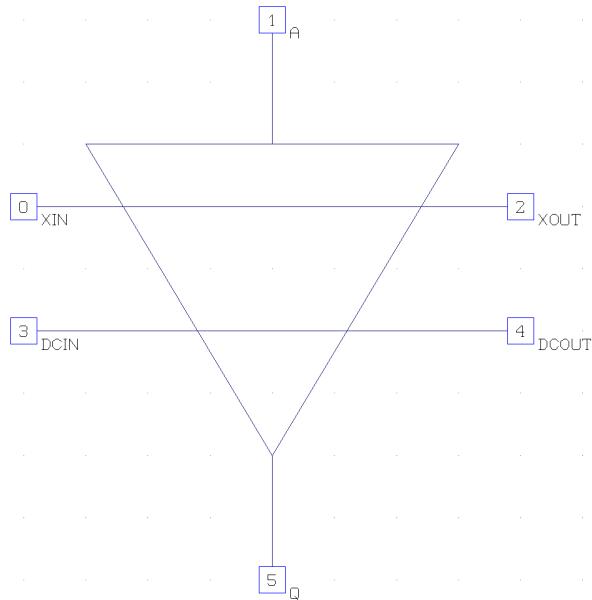
This section presents the schematic, netlist, physical layout, digital model, analog simulation, digital simulation, and switching energy of *representative* AQFP cells. We do not fully describe all variations because it is rather redundant. Instead, we show representative majority, AND, and OR cells. In the respective text, we list the variations of those cells that are also available. Table 1.4 is a complete listing of all of our AQFP cells.

### 2.1 Combinational Cells

#### 2.1.1 BFR

The buffer (`bfr`) is the basic logic structure of AQFP circuits consisting of a double-Josephson-junction SQUID.

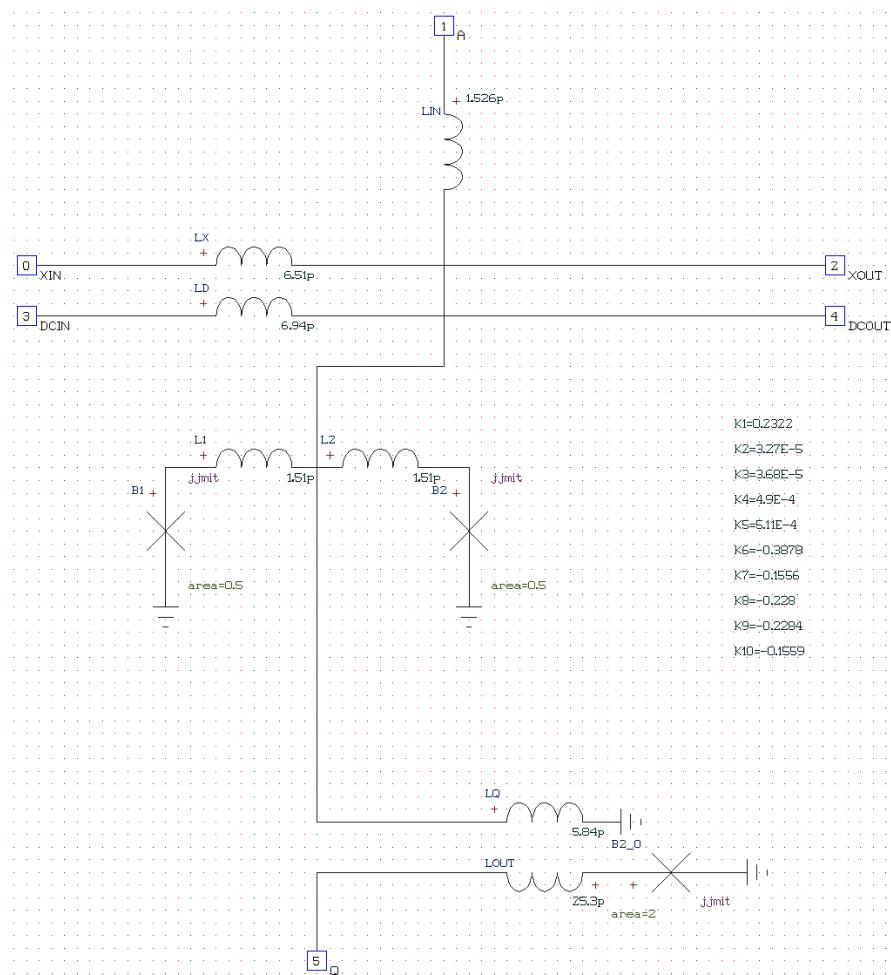
##### Symbol



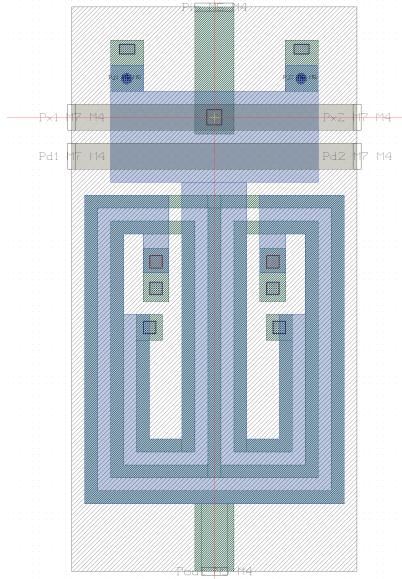
**Figure 2.1:** `bfr` symbol.

**Table 2.1:** bfr pin list.

Pin	Description
<b>A</b>	data input
<b>XIN</b>	serial clock input
<b>DCIN</b>	dc offset input
<b>Q</b>	data output
<b>XOUT</b>	serial clock output
<b>DCOUT</b>	dc offset output

**Schematic****Figure 2.2:** bfr schematic.

## Layout



**Figure 2.3:** bfr layout.

## Analog model

```

1 * Generated by Xic from cell bfr
2
3 .subckt bfr1 XIN A XOUT DCIN DCOUT Q
4 B1 8 0 11 jjmit area=0.5
5 B2 9 0 12 jjmit area=0.5
6 B2_0 10 0 13 jjmit area=2
7 K1 LX LD 0.2322
8 K2 LD LOUT 3.27E-5
9 K3 LX LOUT 3.68E-5
10 K4 LD LQ 4.9E-4
11 K5 LX LQ 5.11E-4
12 K6 LOUT LQ -0.3878
13 K7 L2 LD -0.1556
14 K8 L2 LX -0.228
15 K9 LX L1 -0.2284
16 K10 LD L1 -0.1559
17 L1 8 7 1.51p
18 L2 7 9 1.51p
19 LD DCIN DCOUT 6.94p
20 LIN A 7 1.526p
21 LOUT 10 Q 25.3p
22 LQ 7 0 5.84p
23 LX XIN XOUT 6.51p
24 .ends bfr
25 .model jjmit jj(rtype=1, vg=2.6m,
26 + icrit=0.1m, r0=144, rn=16, cap=0.07p)

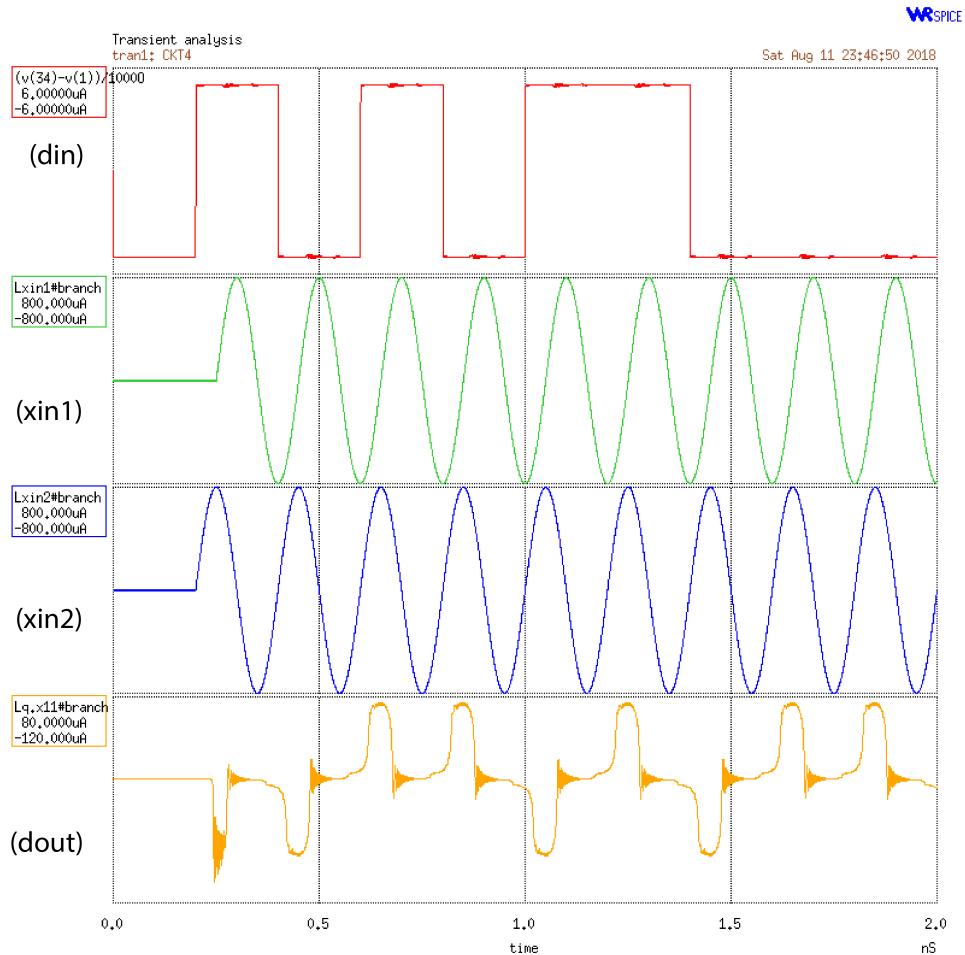
```

**Listing 2.1:** bfr netlist (.elecnet).

## Simulation result

Simulation waveform of a 12-stage AQFP buffer chain at 5 GHz. Signals from top to bottom: buffer chain input (input of the first buffer) as 101011, AC source 1 (generates phase 1 and 3), AC source 2 (generates phase 2 and 4), and the output of the final (12th)

buffer in the buffer chain as 001101011 with three random initial outputs 001. This is because of the meander structure of AQFP circuits. In a 12-stage AQFP circuit, it takes three clock cycles to propagate the data to the output. Input peak-to-peak amplitude is  $\pm 5 \mu\text{A}$ , AC amplitude is  $800 \mu\text{A}$ , and DC is set to  $1.2 \text{ mA}$ .



**Figure 2.4:** bfr analog waveform.

## Digital model

```

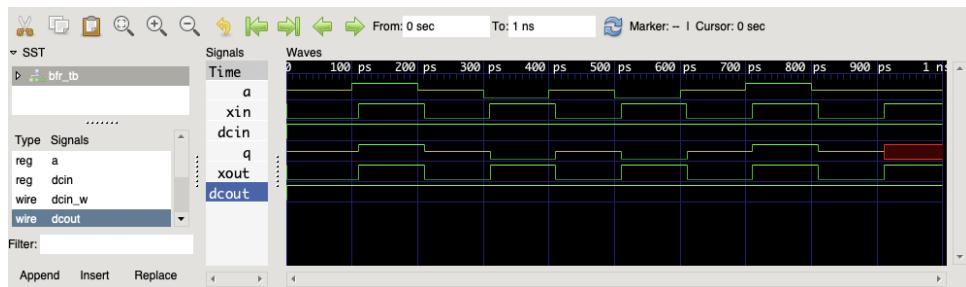
1 //-----
2 // Design Name : buffer
3 // File Name   : bfr.v
4 // Function    : buffer with built-in timing check
5 // Developer   : Olivia Chen (olivia.chen@ieee.org)
6 //-----
7 'timescale 1ps/10fs
8
9 module bfr(a, q, xin, xout, dcin, dc当地);
10   input a;
11   output q;
12   inout xin, xout, dcin, dc当地;
13   reg q;
14   parameter pul_wid = 100;
15   wire not_a;
16
17   assign not_a = !a;

```

```

18   biasDir_b I0(xin, xout, dcin, dcout, gatex);
19
20   initial begin
21
22     $timeformat(-12, 1, "_ps", 8); // time format
23
24     // output register initialization
25     q = 1'bz;
26
27   end // initialization
28
29   specify
30     specparam a_xin    = 5;
31     specparam xin_a   = 50;
32
33     $setup(posedge a && a, posedge gatex, a_xin);
34     $setup(negedge a && not_a, posedge gatex, a_xin);
35     $setup(posedge gatex, negedge a && a, xin_a);
36     $setup(posedge gatex, posedge a && not_a, xin_a);
37   endspecify
38
39   always @(posedge gatex)
40     begin
41       if (a == 1 || a == 0)
42         begin
43           q <= a;
44           q <= #pul_wid 1'bz;
45         end
46       else
47         begin
48           q <= 1'bx;
49           q <= #pul_wid 1'bz;
50         end
51     end
52
53 endmodule

```

**Listing 2.2:** bfr Verilog model code.**Figure 2.5:** bfr digital waveform. HDL '1': AQFP '1'; HDL '0': AQFP '0'; HDL 'z': inactive; HDL 'x': error.

### Switching energy

Different energy consumption results based on different data input patterns ( $a = 0$  and  $a = 1$ ) and clock frequencies.

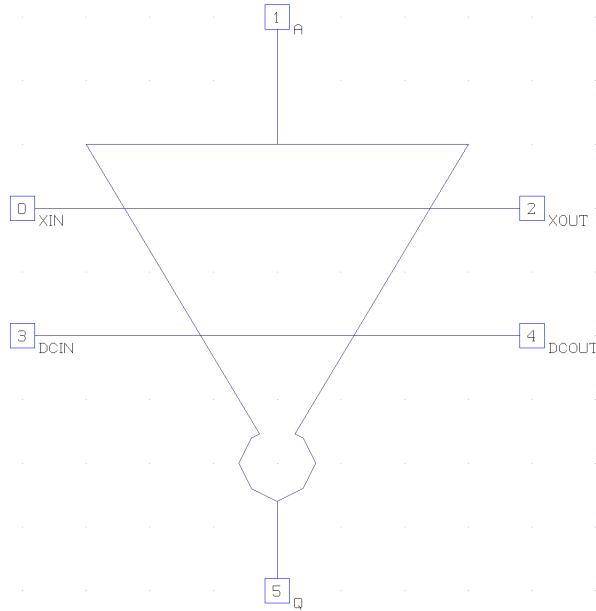
**Table 2.2:** bfr switching energy table.

Clock rate (GHz)	Logic ‘0’ (J)	Logic ‘1’ (J)
0.1	1.28E-23	1.30E-23
0.2	2.57E-23	2.61E-23
0.5	6.42E-23	6.51E-23
1	1.30E-22	1.32E-22
2	2.69E-22	2.76E-22
5	8.83E-22	9.72E-22
10	2.61E-21	3.41E-21

## 2.1.2 INV

The AQFP inverter (**inv**) is one variation of the buffer cell. The operational principle is to generate the opposite direction of the output current by changing the sign of the coupling coefficient of the output transformer (e.g. k6 of the schematic in 2.7).

### Symbol



**Figure 2.6:** inv symbol.

**Table 2.3:** inv pin list.

Pin	Description
<b>A</b>	data input
<b>XIN</b>	serial clock input
<b>DCIN</b>	dc offset input
<b>Q</b>	data output
<b>XOUT</b>	serial clock output
<b>DCOUT</b>	dc offset output

## Schematic

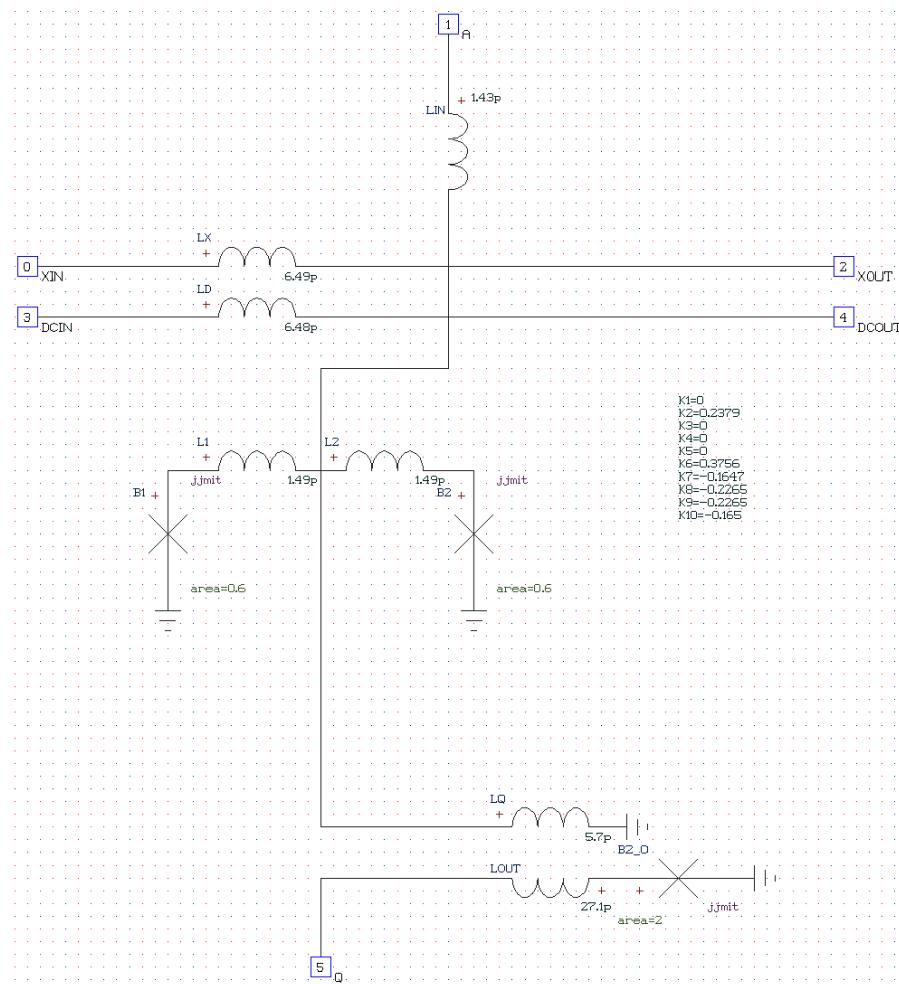
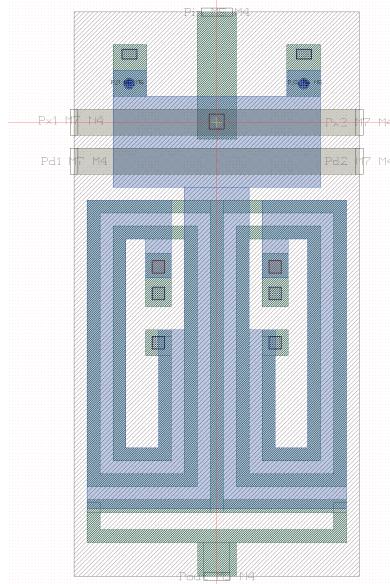


Figure 2.7: inv schematic.

## Layout



**Figure 2.8:** inv layout.

## Analog model

```

1 * Generated by Xic from cell inv
2
3 .subckt inv XIN A XOUT DCIN DCOUT
4 Q B1 8 0 11 jjmit area=0.6
5 B2 9 0 12 jjmit area=0.6
6 B2_0 10 0 13 jjmit area=2
7 K1 LQ LD 0
8 K2 LX LD 0.2379
9 K3 LD LOUT 0
10 K4 LX LOUT 0
11 K5 LX LQ 0
12 K6 LOUT LQ 0.3756
13 K7 L2 LD -0.1647
14 K8 L2 LX -0.2265
15 K9 LX L1 -0.2265
16 K10 LD L1 -0.165
17 L1 8 7 1.49p
18 L2 7 9 1.49p
19 LD DCIN DCOUT 6.48p
20 LIN A 7 1.43p
21 LOUT 10 Q 27.1p
22 LQ 7 0 5.7p
23 LX XIN XOUT 6.49p
24 .ends inv
25 .model jjmit jj(rtype=1, vg=2.6m,
26 + icrit=0.1m, r0=144, rn=16, cap=0.07p)

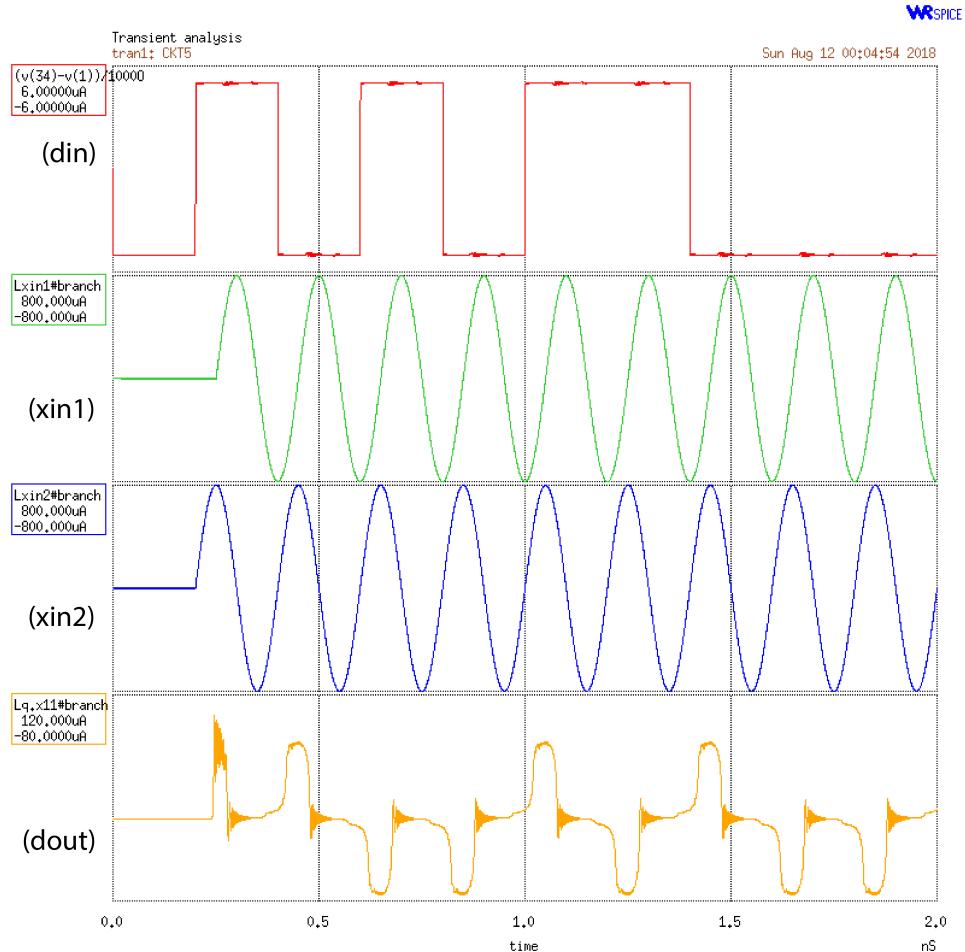
```

**Listing 2.3:** inv netlist (.elecnet).

## Simulation result

Simulation waveform of an INVERTER (inv) DUT (design under test) with 4-stage buffer before the input (a). Another 4-stage buffer is placed after the inverter's q output. Clock frequency is 5 GHz. Signals from top to bottom: buffer chain input a (input of the first

buffer) as 101011, AC source 1 (xin1) (generates phase 1 and 3), AC source 2 (xin2) (generates phase 2 and 4), and the output (dout) generated from the final stage of buffer as 110010100 with three random initial outputs 110. This is because of the meander structure of AQFP circuits. In a 12- stage AQFP circuit, it takes three clock cycles to propagate the data to the output. Input peak-to-peak amplitude is  $\pm 5 \mu\text{A}$ , AC amplitude is  $\pm 800 \mu\text{A}$ , and DC is set to 1.2 mA.



**Figure 2.9:** inv analog waveform.

## Digital model

```

1 //-----
2 // Design Name : inverter
3 // File Name   : inv.v
4 // Function    : inverter with built-in timing check
5 // Developer   : Olivia Chen (olivia.chen@ieee.org)
6 //-----
7
8 'timescale 1ps/10fs
9 'define idle 3'd0
10 'define stop 3'd1
11 'define error 3'd2
12 module inv(a, q, xin, xout, dcin, dc当地);
13   input a;
14   output q;

```

```

15  inout xin, xout, dcin, dcout;
16  reg q;
17  parameter pul_wid = 100;
18  wire not_a;
19
20  assign not_a = !a;
21
22  biasDir_b I0(xin, xout, dcin, dcout, gatex);
23
24  initial begin
25
26  $timeformat(-12, 1, "_ps", 8); // time format
27
28  // output register initialization
29  q = 1'bz;
30  end // initialization
31
32  specify
33    specparam a_xin    = 5;
34    specparam xin_a   = 50;
35
36    $setup(posedge a && a, posedge gatex, a_xin);
37    $setup(negedge a && not_a, posedge gatex, a_xin);
38    $setup(posedge gatex, negedge a && a, xin_a);
39    $setup(posedge gatex, posedge a && not_a, xin_a);
40  endspecify
41
42  always @(posedge gatex)
43  begin
44    if (a == 1 || a == 0)
45      begin
46        q <= !a;
47        q <= #pul_wid 1'bz;
48      end
49    else
50      begin
51        q <= 1'bx;
52        q <= #pul_wid 1'bz;
53      end
54  end
55
56 endmodule

```

Listing 2.4: inv Verilog model code.



Figure 2.10: inv digital waveform. HDL '1': AQFP '1'; HDL '0': AQFP '0'; HDL 'z': inactive; HDL 'x': error.

### Switching energy

Different energy consumption results based on different data input patterns ( $a = 0$  and  $a = 1$ ) and clock frequencies.

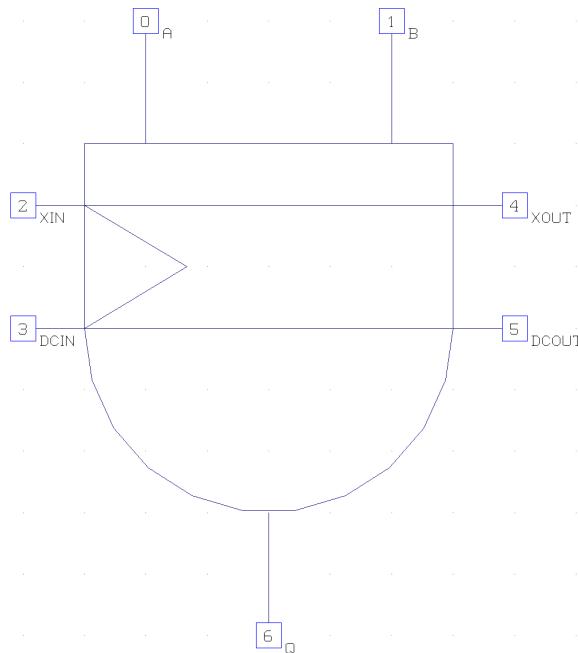
**Table 2.4:** `inv` switching energy table.

Clock rate (GHz)	Logic ‘0’ (J)	Logic ‘1’ (J)
0.1	3.91E-24	3.32E-23
0.2	2.03E-23	5.53E-23
0.5	7.23E-23	1.24E-23
1	2.04E-22	2.71E-22
2	6.86E-22	7.61E-22
5	2.81E-21	2.85E-21
10	6.85E-21	6.71E-21

### 2.1.3 AND2

The 2-input AQFP AND cell is built from buffer and constant 0 cells. The operational principle is to merge the output of two buffers and a constant 0 cell through a 3-to-1 branch. There are 4 types of AND gate with different inputs (positive and negative): `and2_pp`, `and2_pn`, `and2_np`, `and2_nn`. Here we present the AND gate with two positive inputs named `and2_pp`. The branch and constant 0 cells are introduced in sub-cells.

#### Symbol

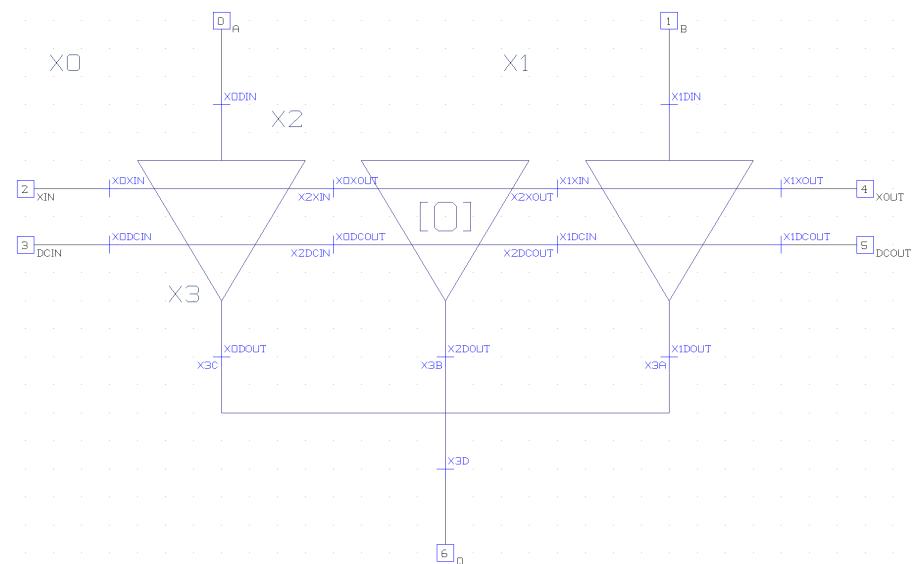


**Figure 2.11:** `and2_pp` symbol.

**Table 2.5:** `and2_pp` pin list.

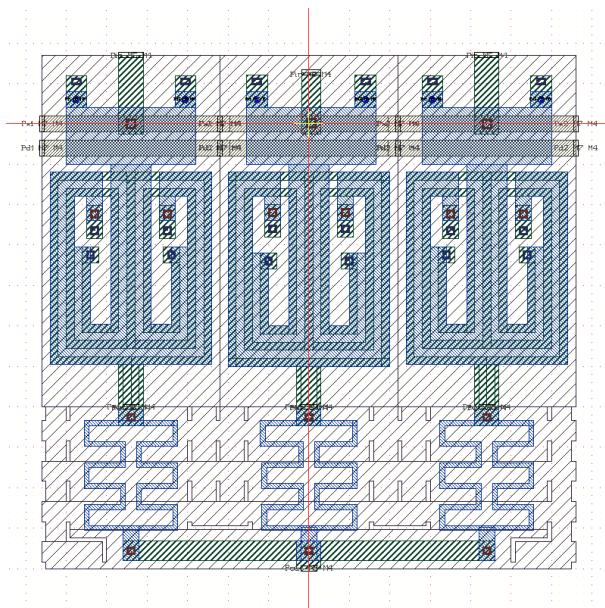
Pin	Description
<b>A</b>	data input
<b>B</b>	data input
<b>XIN</b>	serial clock input
<b>DCIN</b>	dc offset input
<b>Q</b>	data output
<b>XOUT</b>	serial clock output
<b>DCOUT</b>	dc offset output

## Schematic



**Figure 2.12:** and2\_pp schematic.

## Layout



**Figure 2.13:** and2\_pp layout.

## Analog model

```

1 | Generated by Xic from cell and2_pp
2 |
3 | .subckt and2_pp A B XIN DCIN XOUT DCOUT Q
4 | X0 XIN A 10 DCIN 9 8 bfr
5 | X1 13 B XOUT 12 DCOUT 11 bfr

```

```

6 | X2 10 13 9 12 14 const0
7 | X3 11 14 8 Q branch3
8 | .ends and2_pp
9 | .model jjmit jj(rtype=1, vg=2.6m,
10 | + icrit=0.1m, r0=144, rn=16, cap=0.07p)
11 |
12 | .subckt const0 XIN XOUT DCIN DCOUT Q
13 | B1 6 0 10 jjmit area=0.5
14 | B2 8 0 11 jjmit area=0.5
15 | BOUT 9 0 12 jjmit area=2
16 | K1 LX LOUT -2.1e-5
17 | K2 LOUT LD -0.000154
18 | K3 LQ LOUT -0.3959
19 | K4 L2 LD -0.1758
20 | K5 L2 LX -0.236
21 | K6 LD L1 -0.1618
22 | K7 L1 LX -0.226
23 | K8 LX LD 0.26
24 | L1 6 7 1.52p
25 | L2 7 8 1.57p
26 | LD DCIN DCOUT 6.89p
27 | LOUT 9 Q 25p
28 | LQ 7 0 5.9p
29 | LX XIN XOUT 6.5p
30 | .ends const0
31 |
32 | .subckt branch3 A B C D
33 | B0 5 6 8 jjmit area=2
34 | B1 7 6 9 jjmit area=2
35 | LIP 6 D 0.315p
36 | LP1 A 5 13.5p
37 | LP2 B 6 10.1p
38 | LP3 C 7 13.4p
39 | .ends branch3
40 |
41 | .subckt bfr XIN DIN XOUT DCIN DCOUT DOUT
42 | B1 8 0 11 jjmit area=0.5
43 | B2 9 0 12 jjmit area=0.5
44 | B2_0 10 0 13 jjmit area=2
45 | K1 LX LD 0.2322
46 | K2 LD LOUT 3.27E-5
47 | K3 LX LOUT 3.68E-5
48 | K4 LD LQ 4.9E-4
49 | K5 LX LQ 5.11E-4
50 | K6 LOUT LQ -0.3878
51 | K7 L2 LD -0.1556
52 | K8 L2 LX -0.228
53 | K9 LX L1 -0.2284
54 | K10 LD L1 -0.1559
55 | L1 8 7 1.51p
56 | L2 7 9 1.51p
57 | LD DCIN DCOUT 6.94p
58 | LIN DIN 7 1.526p
59 | LOUT 10 DOUT 25.3p
60 | LQ 7 0 5.84p
61 | LX XIN XOUT 6.51p
62 | .ends bfr

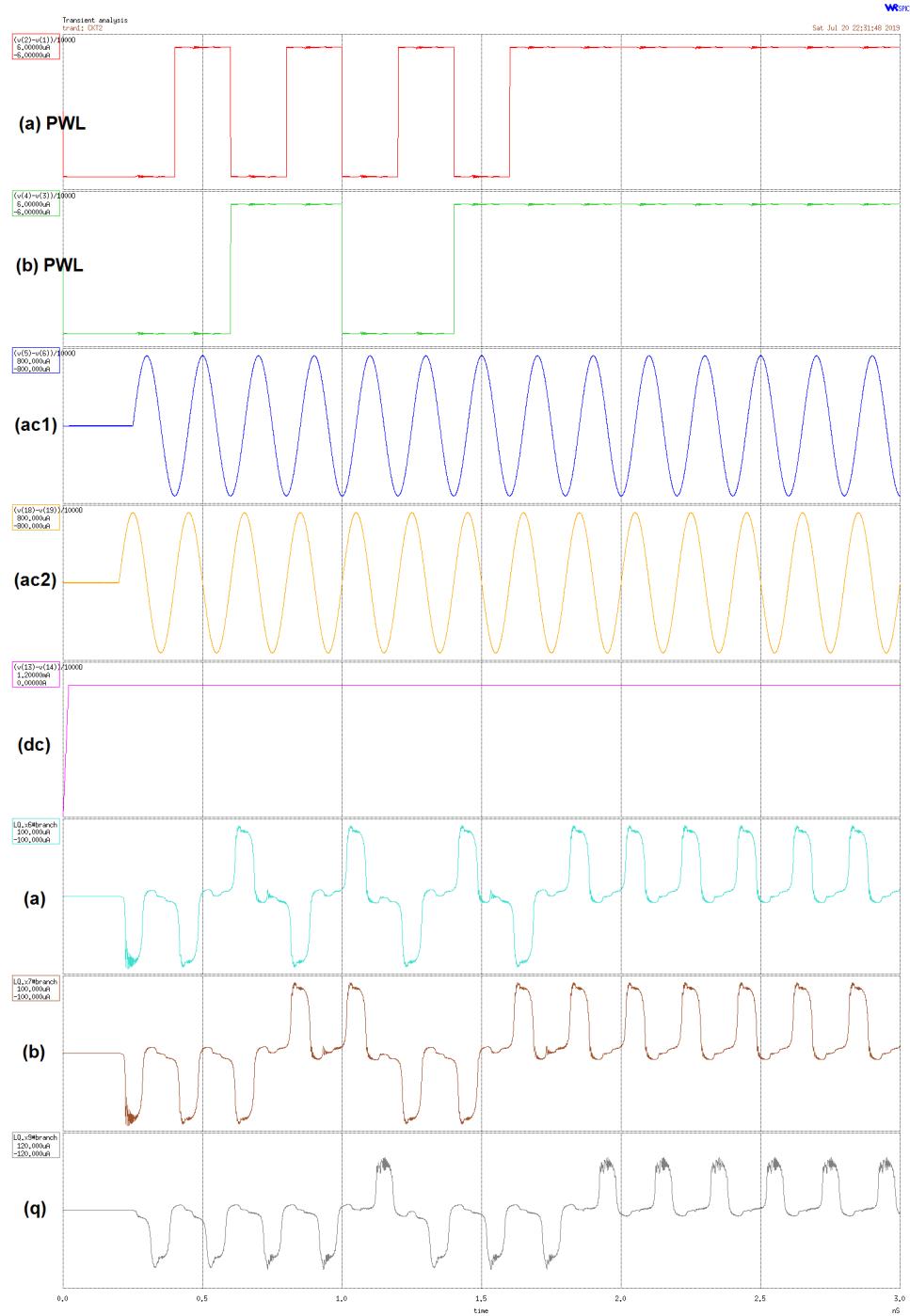
```

**Listing 2.5:** and2\_pp netlist (.elecnet).

## Simulation result

Simulation waveform of an AND (and2\_pp) DUT (design under test) with two 4-stage buffers before the input ‘a’ and ‘b’. Another 3-stage buffer is placed after the AND’s output ‘q’. Clock frequency is 5 GHz. Signals from top to bottom: buffer chain input (a) as 1010110 and (b) as 0110001 (inputs of the first stage buffers), AC source 1 (xin1) (generates phase 1 and 3), AC source 2 (xin2) (generates phase 2 and 4), and the output

generated from the final stage of buffer (q) as 100010000 with two random initial outputs 10. This is because of the meander structure of AQFP circuits. In an 8-stage AQFP circuit, it takes two clock cycles to propagate the data to the output. Input peak-to-peak amplitude is  $\pm 5 \mu\text{A}$ , AC amplitude is  $\pm 800 \mu\text{A}$ , and DC is set to 1.2 mA.



**Figure 2.14:** and2\_pp analog waveform.

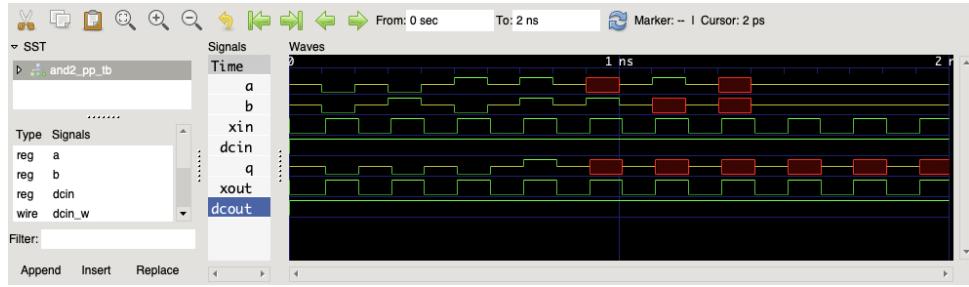
## Digital model

```

1 //-----
2 // Design Name : and_pp
3 // File Name   : and_pp.v
4 // Function    : normal and gate with built-in timing check
5 // Developer   : Olivia Chen (olivia.chen@ieee.org)
6 //-----
7 `timescale 1ps/10fs
8 `define idle 3'd0
9 `define stop 3'd1
10 `define error 3'd2
11 module and2_pp(a, b, q, xin, xout, dcin, dcout);
12   input a, b;
13   output q;
14   inout xin, xout, dcin, dcout;
15   reg q;
16   parameter pul_wid = 100;
17   wire not_a, not_b;
18
19   assign not_a = !a;
20   assign not_b = !b;
21
22
23   biasDir_b I0(xin, xout, dcin, dcout, gatex);
24
25   initial begin
26
27     $timeformat(-12, 1, "_ps", 8); // time format
28
29     // output register initialization
30     q = 1'bz;
31   end // initialization
32
33   specify
34     specparam a_xin    = 5;
35     specparam xin_a   = 50;
36
37     $setup(posedge a && a, posedge gatex, a_xin);
38     $setup(negedge a && not_a, posedge gatex, a_xin);
39     $setup(posedge gatex, negedge a && a, xin_a);
40     $setup(posedge gatex, posedge a && not_a, xin_a);
41     $setup(posedge b && b, posedge gatex, a_xin);
42     $setup(negedge b && not_b, posedge gatex, a_xin);
43     $setup(posedge gatex, negedge b && b, xin_a);
44     $setup(posedge gatex, posedge b && not_b, xin_a);
45   endspecify
46
47   always @(posedge gatex)
48     begin
49       if (a==1'bz && b!=1'bz && a!=1'bx && b==1'bx)
50         begin
51           q <= a && b;
52           q <= #pul_wid 1'bz;
53         end
54       else
55         begin
56           q <= 1'bx;
57           q <= #pul_wid 1'bz;
58         end
59     end
60   endmodule

```

**Listing 2.6:** and2\_pp Verilog model code.



**Figure 2.15:** and2\_pp digital waveform. HDL ‘1’: AQFP ‘1’; HDL ‘0’: AQFP ‘0’; HDL ‘z’: inactive; HDL ‘x’: error.

### Switching energy

Different energy consumption results based on different data input patterns ( $a = b = 0$  and  $a = b = 1$ ) and clock frequencies.

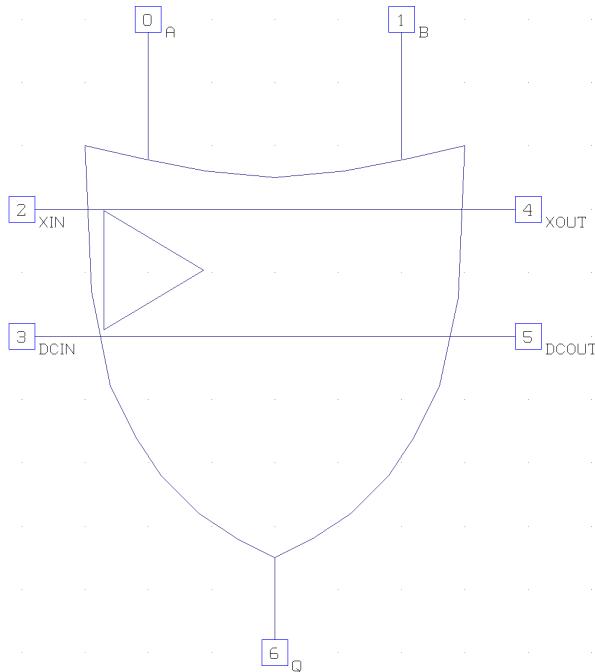
**Table 2.6:** and2\_pp switching energy table.

Clock rate (GHz)	Logic ‘0’ (J)	Logic ‘1’ (J)
0.1	4.23E-23	4.26E-23
0.2	8.47E-23	8.56E-23
0.5	2.17E-22	2.19E-22
1	4.88E-22	4.92E-22
2	1.21E-21	1.22E-21
5	4.53E-21	4.71E-21
10	1.22E-20	1.38E-20

### 2.1.4 OR2

The 2-input AQFP OR cell is built from buffer and constant 1 cells. The operational principle is to merge the output of two buffers and a constant 1 cell through a 3-to-1 branch. There are 4 types of OR gate with different inputs (positive and negative): `or_pp`, `or_pn`, `or_np`, `or_nn`. Here we only present the OR gate with two positive inputs named `or_pp` as an example. Others can be found in the deliverables. The branch and constant 1 cells are introduced in sub-cells.

#### Symbol

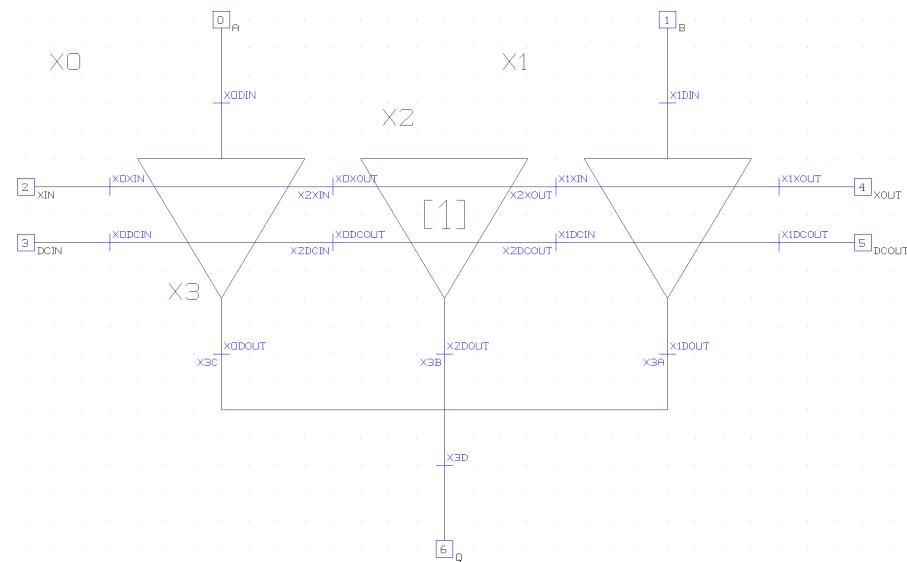


**Figure 2.16:** `or2_pp` symbol.

**Table 2.7:** `or2_pp` pin list.

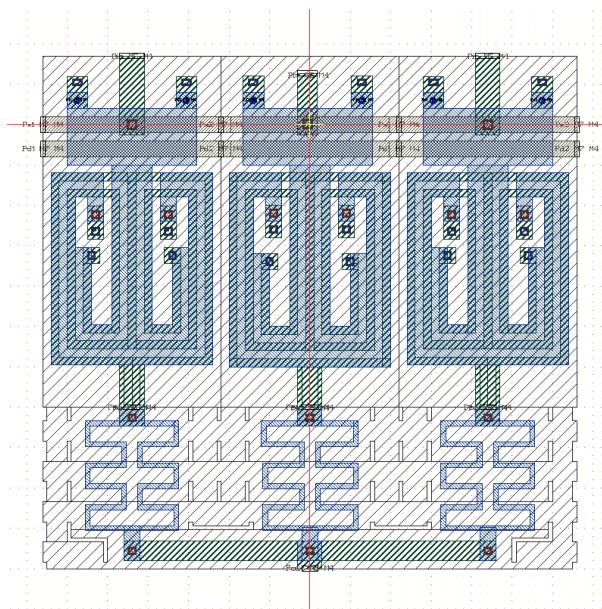
Pin	Description
A	data input
B	data input
XIN	serial clock input
DCIN	dc offset input
Q	data output
XOUT	serial clock output
DCOUT	dc offset output

## Schematic



**Figure 2.17:** or2\_pp schematic.

## Layout



**Figure 2.18:** or2\_pp layout.

## Analog model

```

1 * Generated by Xic from cell or2_pp
2 .subckt or2_pp A B XIN DCIN XOUT DCOUT Q
3 X0 XIN A 10 DCIN 9 8 bfr
4 X1 13 B XOUT 12 DCOUT 11 bfr
5 X2 13 10 12 9 14 const1

```

```

6 | X3 11 14 8 Q branch3
7 | .ends or2_pp
8 | .model jjmit jj(rtype=1, vg=2.6m,
9 | + icrit=0.1m, r0=144, rn=16, cap=0.07p)
10 |
11|.subckt const1 XOUT XIN DCOUT DCIN DOUT
12 X0 XOUT XIN DCOUT DCIN DOUT const0
13 .ends const1
14 |
15|.subckt const0 XIN XOUT DCIN DCOUT Q
16 B1 6 0 10 jjmit area=0.5
17 B2 8 0 11 jjmit area=0.5
18 BOUT 9 0 12 jjmit area=2
19 K1 LX LOUT -2.1e-5
20 K2 LOUT LD -0.000154
21 K3 LQ LOUT -0.3959
22 K4 L2 LD -0.1758
23 K5 L2 LX -0.236
24 K6 LD L1 -0.1618
25 K7 L1 LX -0.226
26 K8 LX LD 0.26
27 L1 6 7 1.52p
28 L2 7 8 1.57p
29 LD DCIN DCOUT 6.89p
30 LOUT 9 Q 25p
31 LQ 7 0 5.9p
32 LX XIN XOUT 6.5p
33 .ends const0
34 |
35|.subckt branch3 A B C D
36 B0 5 6 8 jjmit area=2
37 B1 7 6 9 jjmit area=2
38 LIP 6 D 0.315p
39 LP1 A 5 13.5p
40 LP2 B 6 10.1p
41 LP3 C 7 13.4p
42 .ends branch3
43 |
44|.subckt bfr XIN DIN XOUT DCIN DCOUT DOUT
45 B1 8 0 11 jjmit area=0.5
46 B2 9 0 12 jjmit area=0.5
47 B2_0 10 0 13 jjmit area=2
48 K1 LX LD 0.2322
49 K2 LD LOUT 3.27E-5
50 K3 LX LOUT 3.68E-5
51 K4 LD LQ 4.9E-4
52 K5 LX LQ 5.11E-4
53 K6 LOUT LQ -0.3878
54 K7 L2 LD -0.1556
55 K8 L2 LX -0.228
56 K9 LX L1 -0.2284
57 K10 LD L1 -0.1559
58 L1 8 7 1.51p
59 L2 7 9 1.51p
60 LD DCIN DCOUT 6.94p
61 LIN DIN 7 1.526p
62 LOUT 10 DOUT 25.3p
63 LQ 7 0 5.84p
64 LX XIN XOUT 6.51p
65 .ends bfr

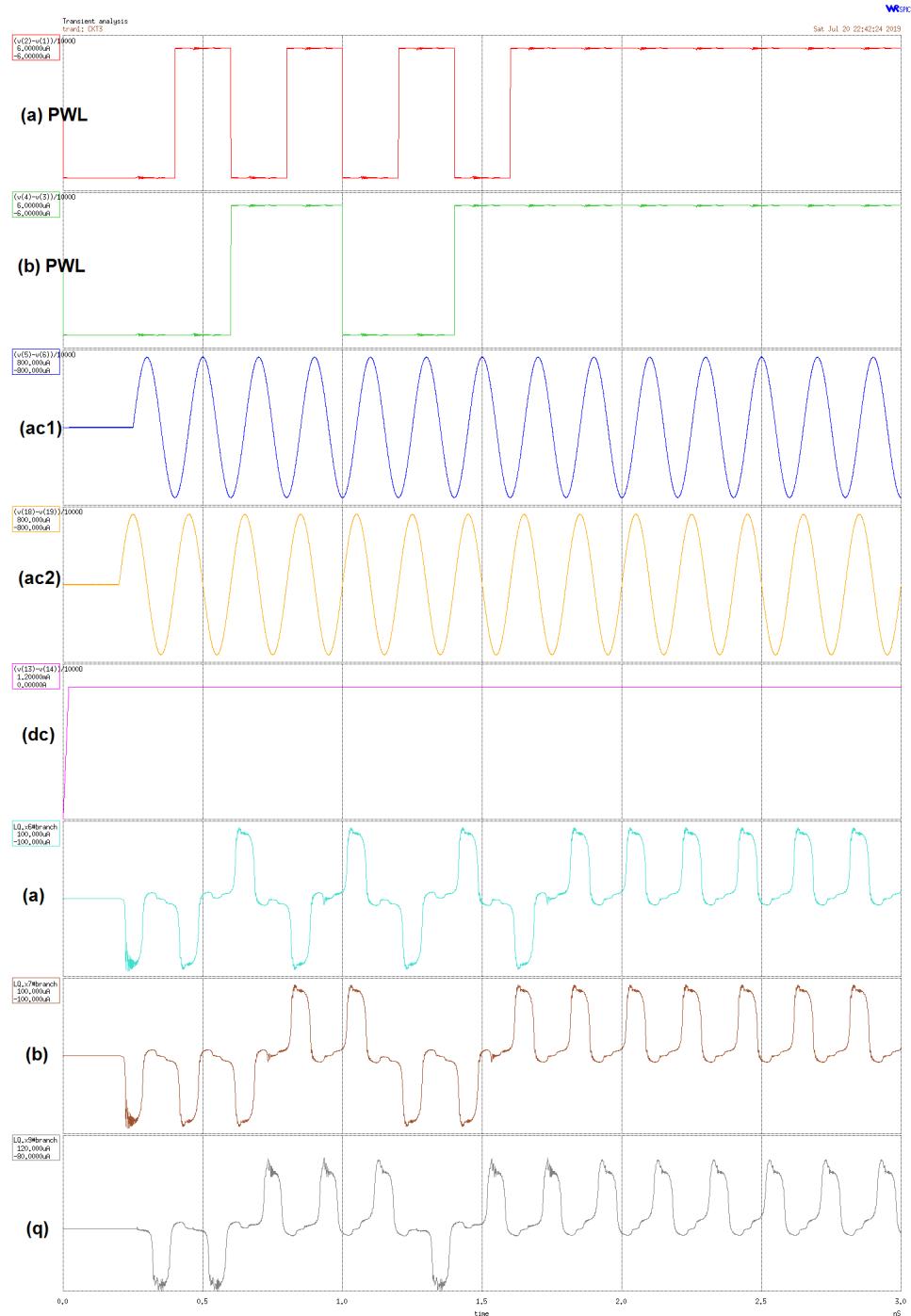
```

**Listing 2.7:** or2\_pp netlist (.elecnet).

## Simulation result

Simulation waveform of an 2-input OR (or2\_pp) DUT (design under test) with two 4-stage buffers before the input ‘a’ and ‘b’. Another 3-stage buffer is placed after the AND’s output ‘q’. Clock frequency is 5 GHz. Signals from top to bottom: buffer chain input

(a) as 1010110 and (b) as 0110001 (inputs of the first stage buffers), AC source 1 (xin1) (generates phase 1 and 3), AC source 2 (xin2) (generates phase 2 and 4), and the output generated from the final stage of buffer (q) as 011110111 with two random initial outputs 01. This is because of the meander structure of AQFP circuits. In an 8-stage AQFP circuit, it takes two clock cycles to propagate the data to the output. Input peak-to-peak amplitude is  $\pm 5 \mu\text{A}$ , AC amplitude is  $\pm 800 \mu\text{A}$ , and DC is set to 1.2 mA.



**Figure 2.19:** or2\_pp analog waveform.

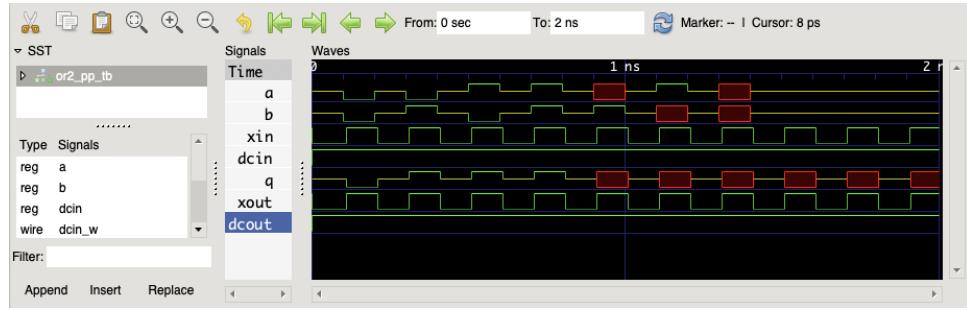
## Digital model

```

1 //-----
2 // Design Name : or_pp
3 // File Name   : or_pp.v
4 // Function    : normal OR gate with built-in timing check
5 // Developer   : Olivia Chen (olivia.chen@ieee.org)
6 //-----
7
8 `timescale 1ps/10fs
9 `define idle 3'd0
10 `define stop 3'd1
11 `define error 3'd2
12 module or2_pp(a, b, q, xin, xout, dcin, dcout);
13   input a, b;
14   output q;
15   inout xin, xout, dcin, dcout;
16   reg q;
17   parameter pul_wid = 100;
18   wire not_a, not_b;
19
20   assign not_a = !a;
21   assign not_b = !b;
22
23 biasDir_b I0(xin, xout, dcin, dcout, gatex);
24
25 initial begin
26
27 $timeformat(-12, 1, "_ps", 8); // time format
28
29 // output register initialization
30 q = 1'bz;
31 end // initialization
32
33 specify
34   specparam a_xin    = 5;
35   specparam xin_a    = 50;
36
37   $setup(posedge a && a, posedge gatex, a_xin);
38   $setup(negedge a && not_a, posedge gatex, a_xin);
39   $setup(posedge gatex, negedge a && a, xin_a);
40   $setup(posedge gatex, posedge a && not_a, xin_a);
41
42   $setup(posedge b && b, posedge gatex, a_xin);
43   $setup(negedge b && not_b, posedge gatex, a_xin);
44   $setup(posedge gatex, negedge b && b, xin_a);
45   $setup(posedge gatex, posedge b && not_b, xin_a);
46 endspecify
47
48 always @(posedge gatex)
49   begin
50     if (a==1'bz && b==1'bz && a!=1'bx && b!=1'bx)
51       begin
52         q <= a||b;
53         q <= #pul_wid 1'bz;
54       end
55     else
56       begin
57         q <= 1'bx;
58         q <= #pul_wid 1'bz;
59       end
60   end
61
62 endmodule

```

**Listing 2.8:** or2\_pp Verilog model code.



**Figure 2.20:** or2\_pp digital waveform. HDL ‘1’: AQFP ‘1’; HDL ‘0’: AQFP ‘0’; HDL ‘z’: inactive; HDL ‘x’: error.

### Switching energy

Different energy consumption results based on different data input patterns ( $a = b = 0$  and  $a = b = 1$ ) and clock frequencies.

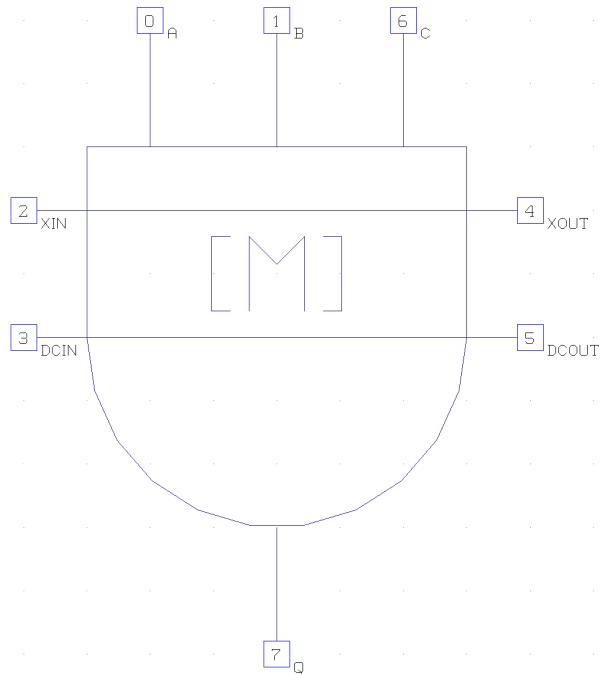
**Table 2.8:** or2\_pp switching energy table.

Clock rate (GHz)	Logic ‘0’ (J)	Logic ‘1’ (J)
0.1	4.25E-23	4.28E-23
0.2	8.52E-23	8.61E-23
0.5	2.19E-22	2.20E-22
1	4.91E-22	4.96E-22
2	1.21E-21	1.23E-21
5	4.56E-21	4.74E-21
10	1.29E-20	1.45E-20

## 2.1.5 MAJ3

AQFP majority cells are built from buffer cells. The operational principle of a 3-input majority gate is to merge the output of three buffers through a 3-to-1 branch. There are 8 types of 3-input majority gate with different inputs (positive and negative): `maj3_ppp`, `maj3_ppn`, `maj3_pnp`, `maj3_pnn`, `maj3_npp`, `maj3_npn`, `maj3_nnp`, `maj3_nnn`. Here we only present the 3-input majority gate with three positive inputs named `maj3_ppp`. Others can be found in the deliverables. The branch cells are introduced in the sub-cells.

### Symbol

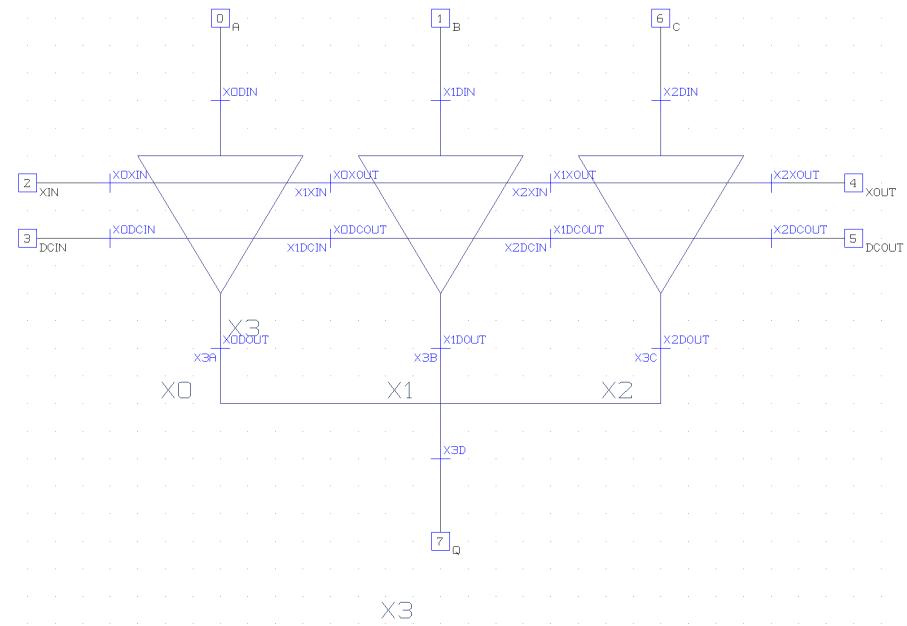


**Figure 2.21:** `maj3_ppp` symbol.

**Table 2.9:** `maj3_ppp` pin list.

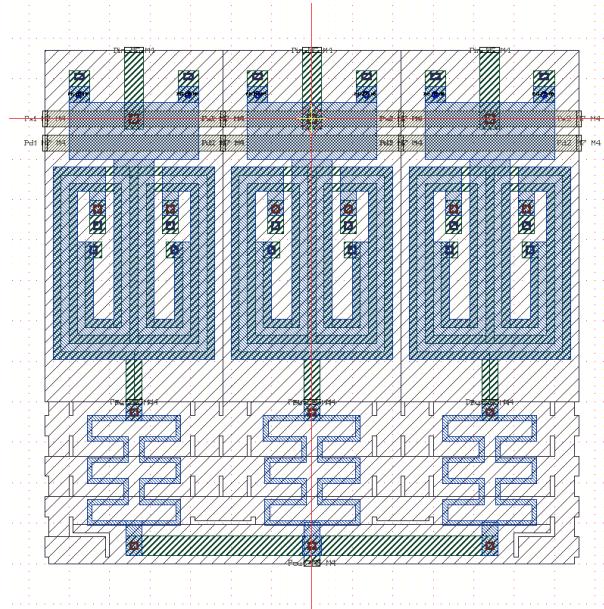
Pin	Description
<b>A</b>	data input
<b>B</b>	data input
<b>C</b>	data input
<b>XIN</b>	serial clock input
<b>DCIN</b>	dc offset input
<b>Q</b>	data output
<b>XOUT</b>	serial clock output
<b>DCOUT</b>	dc offset output

## Schematic



**Figure 2.22:** maj3\_ppp schematic.

## Layout



**Figure 2.23:** maj3\_ppp layout.

## Analog model

```
1 | * Generated by Xic from cell maj3_ppp
2 |
```

```

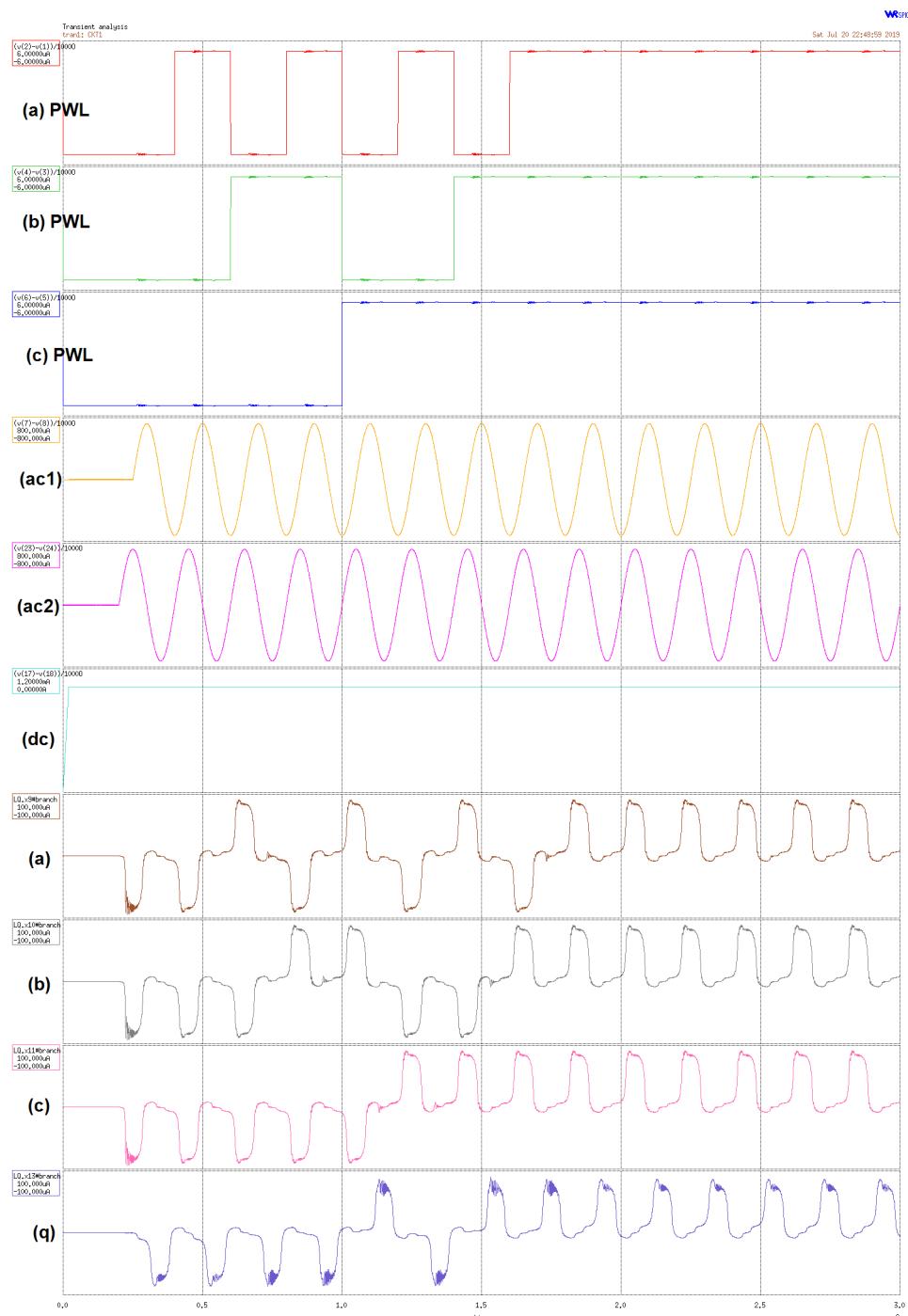
3 | .subckt maj3_ppp A B XIN DCIN XOUT DCOUT C Q
4 | X0 XIN A 11 DCIN 10 9 bfr
5 | X1 11 B 14 10 13 12 bfr
6 | X2 14 C XOUT 13 DCOUT 15 bfr
7 | X3 9 12 15 Q branch3
8 | .ends maj3_ppp
9 | .model jjmit jj(rtype=1, vg=2.6m,
10 | + icrit=0.1m, r0=144, rn=16, cap=0.07p)
11 |
12 | .subckt branch3 A B C D
13 | B0 5 6 8 jjmit area=2
14 | B1 7 6 9 jjmit area=2
15 | LIP 6 D 0.315p
16 | LP1 A 5 13.5p
17 | LP2 B 6 10.1p
18 | LP3 C 7 13.4p
19 | .ends branch3
20 |
21 | .subckt bfr XIN DIN XOUT DCIN DCOUT DOUT
22 | B1 8 0 11 jjmit area=0.5
23 | B2 9 0 12 jjmit area=0.5
24 | B2_0 10 0 13 jjmit area=2
25 | K1 LX LD 0.2322
26 | K2 LD LOUT 3.27E-5
27 | K3 LX LOUT 3.68E-5
28 | K4 LD LQ 4.9E-4
29 | K5 LX LQ 5.11E-4
30 | K6 LOUT LQ -0.3878
31 | K7 L2 LD -0.1556
32 | K8 L2 LX -0.228
33 | K9 LX L1 -0.2284
34 | K10 LD L1 -0.1559
35 | L1 8 7 1.51p
36 | L2 7 9 1.51p
37 | LD DCIN DCOUT 6.94p
38 | LIN DIN 7 1.526p
39 | LOUT 10 DOUT 25.3p
40 | LQ 7 0 5.84p
41 | LX XIN XOUT 6.51p
42 | .ends bfr

```

**Listing 2.9:** maj3\_ppp netlist (.elecnet).

## Simulation result

Simulation waveform of a 3-input MAJORITY (maj\_ppp) DUT (design under test) with three 4-stage buffers before the input ‘a’, ‘b’ and ‘c’. Another 3-stage buffer is placed after the MAJORITY’s output ‘q’. Clock frequency is 5 GHz. Signals from top to bottom: buffer chain input (a) as 1010110, (b) as 0110001 and (c) as 0110001(inputs of the first stage buffers), AC source 1 (xin1) (generates phase 1 and 3), AC source 2 (xin2) (generates phase 2 and 4), and the output generated from the final stage of buffer (d) as 100110001 with two random initial outputs 10. This is because of the meander structure of AQFP circuits. In an 8-stage AQFP circuit, it takes two clock cycles to propagate the data to the output. Input peak-to-peak amplitude is  $\pm 5 \mu\text{A}$ , AC amplitude is  $\pm 800 \mu\text{A}$ , and DC is set to 1.2 mA.



**Figure 2.24:** maj3\_ddd analog waveform.

## Digital model

```

1 //-----
2 // Design Name : maj_ppp
3 // File Name   : maj_ppp.v
4 // Function    : normal majority gate with built-in timing check
5 // Developer   : Olivia Chen (olivia.chen@ieee.org)
6 //-----
7 `timescale 1ps/10fs
  
```

```

8  `define idle 3'd0
9  `define stop 3'd1
10 `define error 3'd2
11 module maj3_ppp(a, b, c, q, xin, xout, dcin, dcout);
12   input a, b, c;
13   output q;
14   inout xin, xout, dcin, dcout;
15   reg q;
16   parameter pul_wid = 100;
17   wire not_a, not_b, not_c;
18   assign not_a = !a;
19   assign not_b = !b;
20   assign not_c = !c;
21   biasDir_b I0(xin, xout, dcin, dcout, gatex);
22   initial begin
23     $timeformat(-12, 1, "_ps", 8); // time format
24   // output register initialization
25   q = 1'bz;
26   end // initialization
27   specify
28     specparam a_xin    = 5;
29     specparam xin_a   = 50;
30     $setup(posedge a && a, posedge gatex, a_xin);
31     $setup(negedge a && not_a, posedge gatex, a_xin);
32     $setup(posedge gatex, negedge a && a, xin_a);
33     $setup(posedge gatex, posedge a && not_a, xin_a);
34     $setup(posedge b && b, posedge gatex, a_xin);
35     $setup(negedge b && not_b, posedge gatex, a_xin);
36     $setup(posedge gatex, negedge b && b, xin_a);
37     $setup(posedge gatex, posedge b && not_b, xin_a);
38     $setup(posedge c && c, posedge gatex, a_xin);
39     $setup(negedge c && not_c, posedge gatex, a_xin);
40     $setup(posedge gatex, negedge c && c, xin_a);
41     $setup(posedge gatex, posedge c && not_c, xin_a);
42   endspecify
43   always @(posedge gatex)
44   begin
45     if (a==1'bz && a!=1'bx && b==1'bz && b!=1'bx && c==1'bz && c!=1'bx)
46       begin
47         q <= (a&&b)||(b&&c)||(a&&c) ;
48         q <= #pul_wid 1'bz;
49       end
50     else
51       begin
52         q <= 1'bx;
53         q <= #pul_wid 1'bz;
54       end
55   end
56 endmodule

```

Listing 2.10: maj3\_ppp Verilog model code.

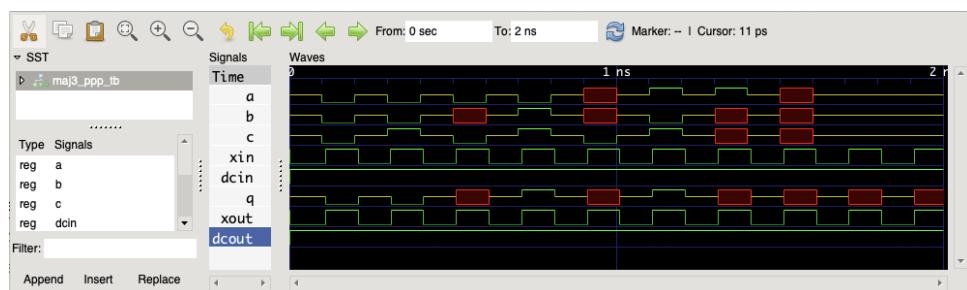


Figure 2.25: maj3\_ppp digital waveform. HDL '1': AQFP '1'; HDL '0': AQFP '0'; HDL 'z': inactive; HDL 'x': error.

## Switching energy

Different energy consumption results based on different data input patterns ( $a = b = 0$  and  $a = b = 1$ ) and clock frequencies.

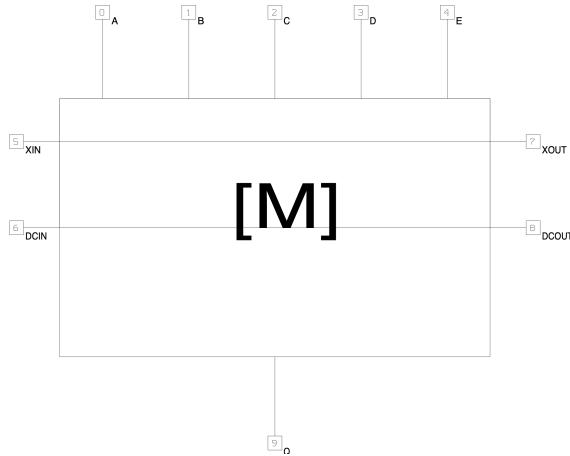
**Table 2.10:** maj3\_ppp switching energy table.

Clock rate (GHz)	Logic ‘0’ (J)	Logic ‘1’ (J)
0.1	4.23E-23	4.26E-23
0.2	8.47E-23	8.56E-23
0.5	2.17E-22	2.19E-22
1	4.88E-22	4.92E-22
2	1.21E-21	1.22E-21
5	4.53E-21	4.71E-21
10	1.22E-20	1.38E-20

## 2.1.6 MAJ5

AQFP majority cells are built from buffer cells. The operational principle of a 5-input majority gate is to merge the output of five buffers through a 5-to-1 branch. There are 32 possible types of 5-input majority gate with different inputs (positive and negative). Here we only present the 5-input majority gate with five positive inputs named `maj5_ppppp`. Others are under development. The branch cells are introduced in the sub-cells.

### Symbol

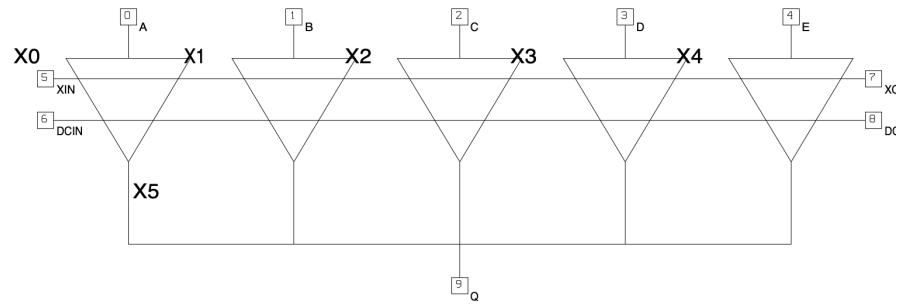


**Figure 2.26:** `maj5_ppppp` symbol.

**Table 2.11:** `maj5_ppppp` pin list.

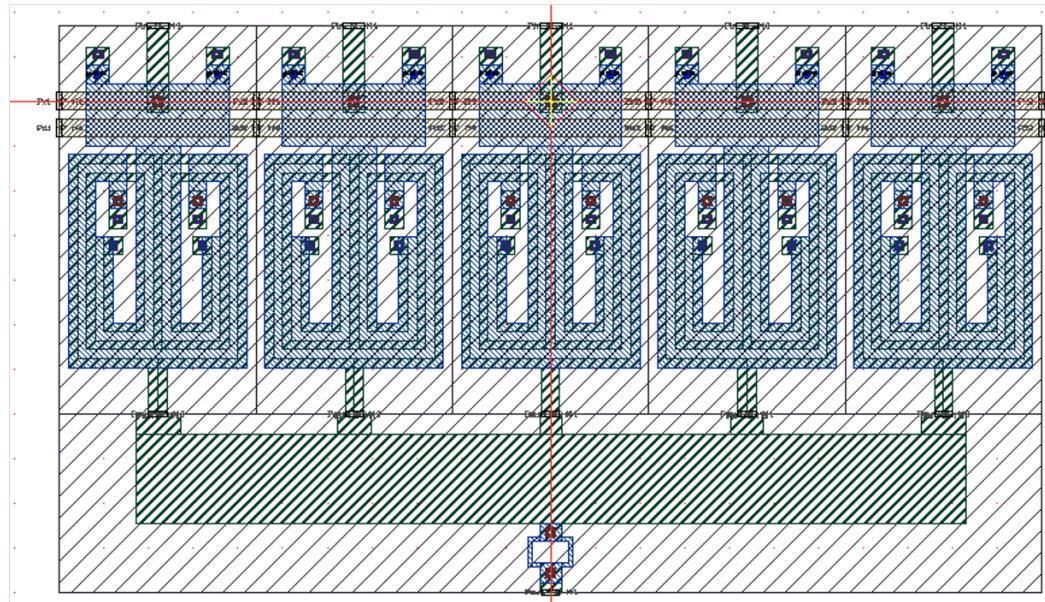
Pin	Description
<b>A</b>	data input
<b>B</b>	data input
<b>C</b>	data input
<b>D</b>	data input
<b>E</b>	data input
<b>XIN</b>	serial clock input
<b>DCIN</b>	dc offset input
<b>Q</b>	data output
<b>XOUT</b>	serial clock output
<b>DCOUT</b>	dc offset output

## Schematic



**Figure 2.27:** maj5\_ppppp schematic.

## Layout



**Figure 2.28:** maj5\_ppppp layout.

## Analog model

```

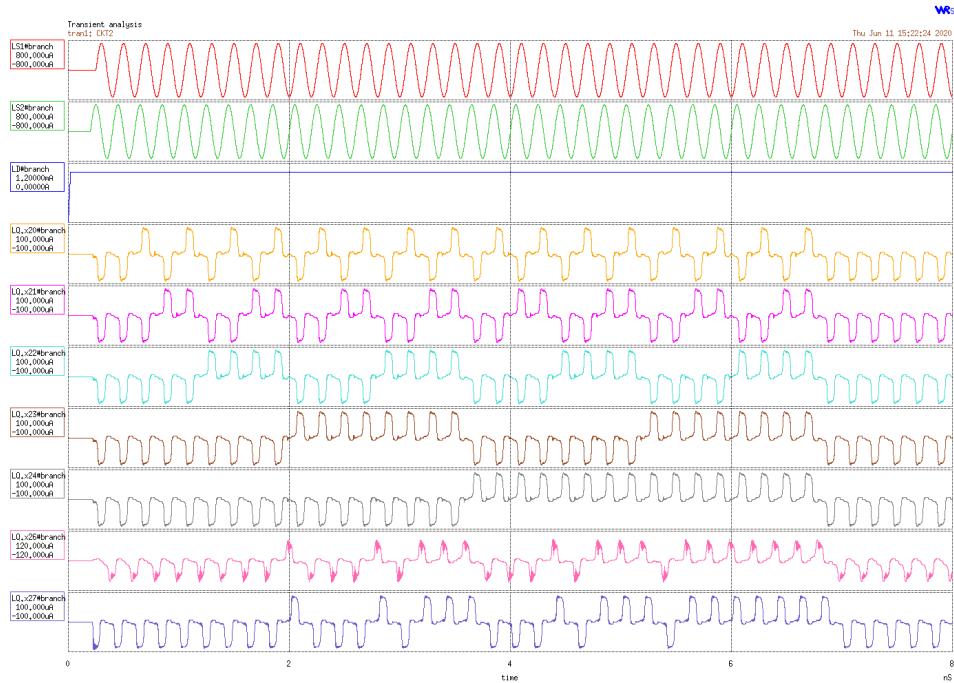
1 * Generated by Xic from cell maj5_ppppp
2 .subckt maj5_ppppp A B C D E XIN DCIN XOUT DCOUT Q
3 X5 11 12 13 14 15 Q branch5
4 .ends maj5_ppppp
5 .model jjmit jj(rtype=1, vg=2.6m,\ 
6 + icrit=0.1m, r0=144, rn=16, cap=0.07p)
7 .subckt branch5 A B C D E G\
8 B0 8 7 14 jjmit area=2
9 B1 7 12 15 jjmit area=2
10 B2 13 10 16 jjmit area=2
11 B3 11 10 17 jjmit area=2
12 L5 12 9 1.08p
13 L6 9 13 1.08p
14 LIP 9 G 2.59p
15 LP1 A 8 1.65p
16 LP2 B 7 0.559p
17 LP3 C 9 0.742p
18 LP4 D 10 0.559p
19 LP5 E 11 1.65p
20 .ends branch5
21 .subckt bfr PX1 PIN PX2 PD1 PD2 POUT
22 B1 8 0 11 jjmit area=0.5
23 B2 9 0 12 jjmit area=0.5
24 B3 10 0 13 jjmit area=2
25 K1 LX LD 0.2322
26 K2 LD LOUT 3.27E-5
27 K3 LX LOUT 3.68E-5
28 K4 LD LQ 4.9E-4
29 K5 LX LQ 5.11E-4
30 K6 LOUT LQ -0.3878
31 K7 L2 LD -0.1556
32 K8 L2 LX -0.228
33 K9 LX L1 -0.2284
34 K10 LD L1 -0.1559
35 L1 8 7 1.51p
36 L2 7 9 1.51p
37 LD PD1 PD2 6.94p
38 LIN PIN 7 1.526p
39 LOUT 10 POUT 25.3p
40 LQ 7 0 5.84p
41 LX PX1 PX2 6.51p
42 .ends bfr

```

**Listing 2.11:** maj5\_ppppp netlist (.elecnet).

## Simulation result

Simulation waveform of a 5-input MAJORITY (maj5\_ppppp) DUT (design under test) with three 4-stage buffers before the input ‘a’, ‘b’, ‘c’, ‘d’ and ‘e’. Another 3-stage buffer is placed after the MAJORITY’s output ‘q’. Clock frequency is 5 GHz. Signals from top to bottom: buffer chain input (a) as 010101010101010101010101, (b) as 001100110011001100110011, (c) as 000011100011110000111100001111, (d) as 000000011111110000000011111111, and (e) as 000000000000000011111111111111 (inputs of the first stage buffers), AC source 1 (xin1) (generates phase 1 and 3), AC source 2 (xin2) (generates phase 2 and 4), and the output generated from the final stage of buffer (q) as 0000001000101110001011101111111 with two random initial outputs 00. This is because of the meander structure of AQFP circuits. In an 8-stage AQFP circuit, it takes two clock cycles to propagate the data to the output. Input peak-to-peak amplitude is  $\pm 5 \mu\text{A}$ , AC amplitude is  $\pm 800 \mu\text{A}$ , and DC is set to 1.2 mA.



**Figure 2.29:** maj5\_ppppp analog waveform.

## Digital model

```

1 //-----
2 // Design Name : maj5_ppppp
3 // File Name   : maj5_ppppp.v
4 // Function    : 5-input majority gate with built-in timing check
5 // Developer   : Olivia Chen (olivia.chen@ieee.org)
6 //-----
7
8 'timescale 1ps/10fs
9 'define idle 3'd0
10 'define stop 3'd1
11 'define error 3'd2
12 module maj5_ppppp(a, b, c, d, e, q, xin, xout, dcin, dcout);
13   input a, b, c, d, e;
14   output q;
15   inout xin, xout, dcin, dcout;
16   reg q;
17   parameter pul_wid = 100;
18   wire not_a, not_b, not_c, not_d, not_e;
19
20   assign not_a = !a;
21   assign not_b = !b;
22   assign not_c = !c;
23   assign not_d = !d;
24   assign not_e = !e;
25
26   biasDir_b I0(xin, xout, dcin, dcout, gatex);
27
28   initial begin
29
30     $timeformat(-12, 1, "_ps", 8); // time format
31
32     // output register initialization
33     q = 1'bz;
34
35   end // initialization
36
37   specify

```

```

37   specparam a_xin    = 5;
38   specparam xin_a    = 50;
39
40   $setup(posedge a && a, posedge gatex, a_xin);
41   $setup(negedge a && not_a, posedge gatex, a_xin);
42   $setup(posedge gatex, negedge a && a, xin_a);
43   $setup(posedge gatex, posedge a && not_a, xin_a);
44
45   $setup(posedge b && b, posedge gatex, a_xin);
46   $setup(negedge b && not_b, posedge gatex, a_xin);
47   $setup(posedge gatex, negedge b && b, xin_a);
48   $setup(posedge gatex, posedge b && not_b, xin_a);
49
50   $setup(posedge c && c, posedge gatex, a_xin);
51   $setup(negedge c && not_c, posedge gatex, a_xin);
52   $setup(posedge gatex, negedge c && c, xin_a);
53   $setup(posedge gatex, posedge c && not_c, xin_a);
54
55   $setup(posedge d && d, posedge gatex, a_xin);
56   $setup(negedge d && not_d, posedge gatex, a_xin);
57   $setup(posedge gatex, negedge d && d, xin_a);
58   $setup(posedge gatex, posedge d && not_d, xin_a);
59
60   $setup(posedge e && e, posedge gatex, a_xin);
61   $setup(negedge e && not_e, posedge gatex, a_xin);
62   $setup(posedge gatex, negedge e && e, xin_a);
63   $setup(posedge gatex, posedge e && not_e, xin_a);
64 endspecify
65
66 always @(posedge gatex)
67 begin
68   if (a==1'bz && a!=1'bx && b==1'bz && b!=1'bx && c==1'bz && c!=1'bx && d==1'bz
69     && d!=1'bx && e==1'bz && e!=1'bx)
70     begin
71       q <= (a&b&c)|| (a&b&d)|| (a&b&e)|| (a&c&d)|| (a&c&e)|| (a&d&e)|| (b&c&d)
72         && ||(b&c&e)|| (b&d&e)|| (c&d&e);
73       q <= #pul_wid 1'bz;
74     end
75   else
76     begin
77       q <= 1'bx;
78       q <= #pul_wid 1'bz;
79     end
80   end
81 endmodule

```

Listing 2.12: maj5\_ppppp Verilog model code.

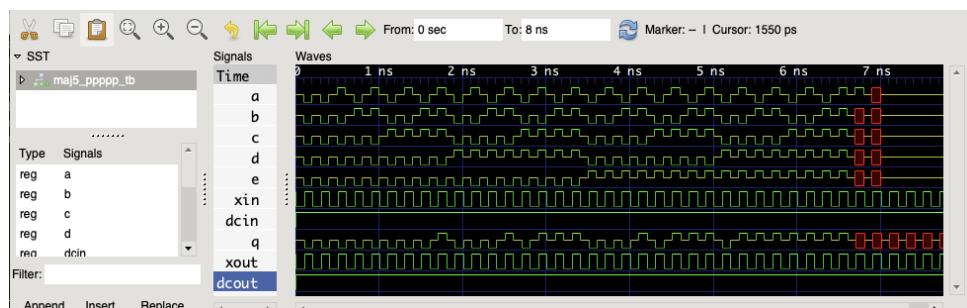


Figure 2.30: maj5\_ppppp digital waveform. HDL '1': AQFP '1'; HDL '0': AQFP '0'; HDL 'z': inactive; HDL 'x': error.

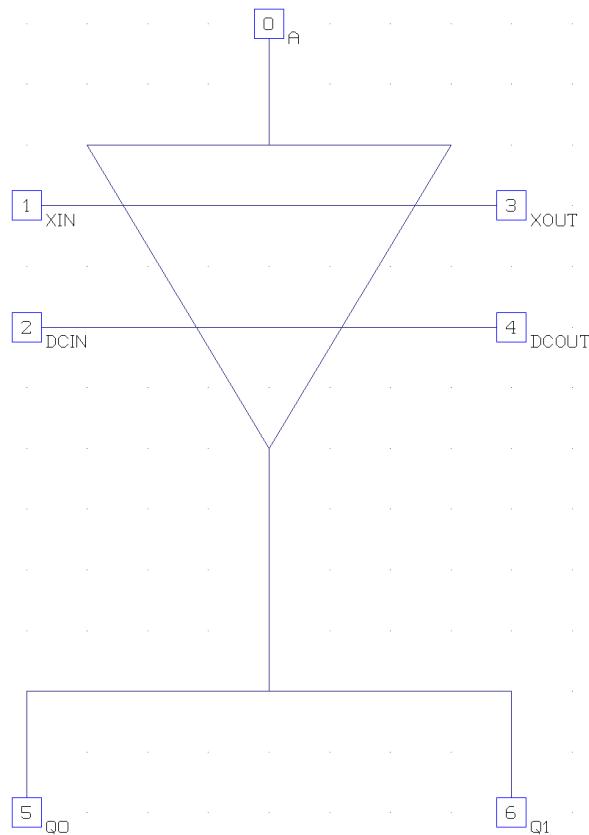
## Switching energy

To be investigated in the future.

## 2.1.7 SPL

Splitters are the splitting elements in AQFP logic to increase the fanout during data propagation. An AQFP splitter is built from buffer and 1-to-n branch cells. The operational principle is to split the output of a buffer through a 1-to-n branch. There are 2 types of splitter cells with different fanouts: splitter 1-to-2 (**spl2**) and 1-to-3 (**spl3**). Here we only present the **spl2** cell as an example. The other one can be found in the deliverables. The branch is introduced in sub-cells.

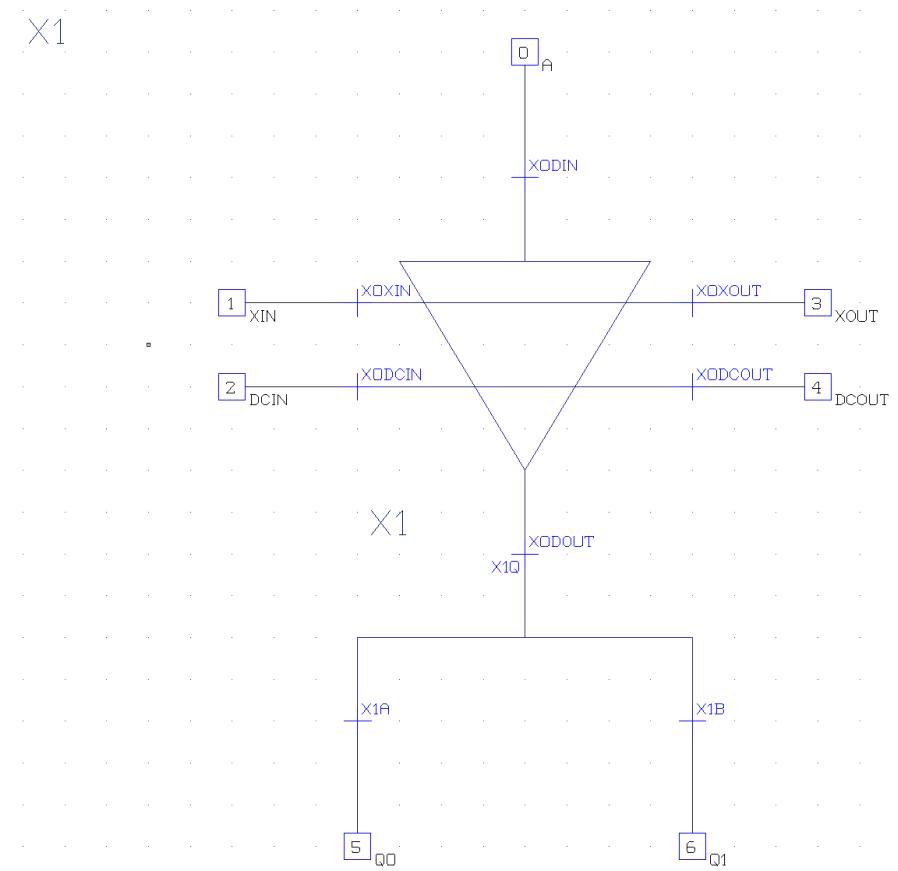
### Symbol



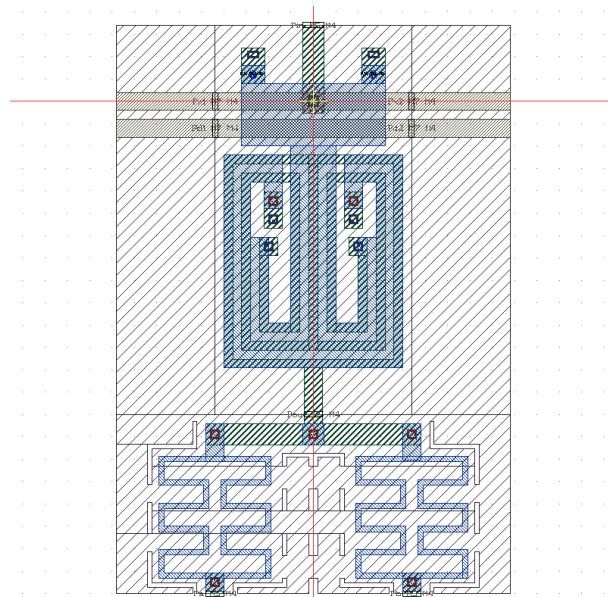
**Figure 2.31:** *spl2* symbol.

**Table 2.12:** *spl2* pin list.

Pin	Description
<b>A</b>	data input
<b>XIN</b>	serial clock input
<b>DCIN</b>	dc offset input
<b>Q0</b>	data output
<b>Q1</b>	data output
<b>XOUT</b>	serial clock output
<b>DCOUT</b>	dc offset output

**Schematic****Figure 2.32:** spl12 schematic.

## Layout



**Figure 2.33:** spl2 layout.

## Analog model

```

1 * Generated by Xic from cell spl2
2
3 .subckt spl2 A XIN DCIN XOUT DCOUT Q0 Q1
4 X0 XIN A XOUT DCIN DCOUT 8 bfr
5 X1 Q0 Q1 8 branch2
6 .ends spl2
7 .model jjmit jj(rtype=1, vg=2.6m,
8 + icrit=0.1m, r0=144, rn=16, cap=0.07p)
9
10 .subckt branch2 A B C
11 B0 5 4 7 jjmit area=2
12 B1 6 4 8 jjmit area=2
13 LIP 4 C 0.39p
14 LP1 A 5 12.4p
15 LP2 B 6 12.4p
16 .ends branch2
17
18 .subckt bfr XIN DIN XOUT DCIN DCOUT DOUT
19 B1 8 0 11 jjmit area=0.5
20 B2 9 0 12 jjmit area=0.5
21 B2_0 10 0 13 jjmit area=2
22 K1 LX LD 0.2322
23 K2 LD LOUT 3.27E-5
24 K3 LX LOUT 3.68E-5
25 K4 LD LQ 4.9E-4
26 K5 LX LQ 5.11E-4
27 K6 LOUT LQ -0.3878
28 K7 L2 LD -0.1556
29 K8 L2 LX -0.228
30 K9 LX L1 -0.2284
31 K10 LD L1 -0.1559
32 L1 8 7 1.51p
33 L2 7 9 1.51p
34 LD DCIN DCOUT 6.94p
35 LIN DIN 7 1.526p

```

```

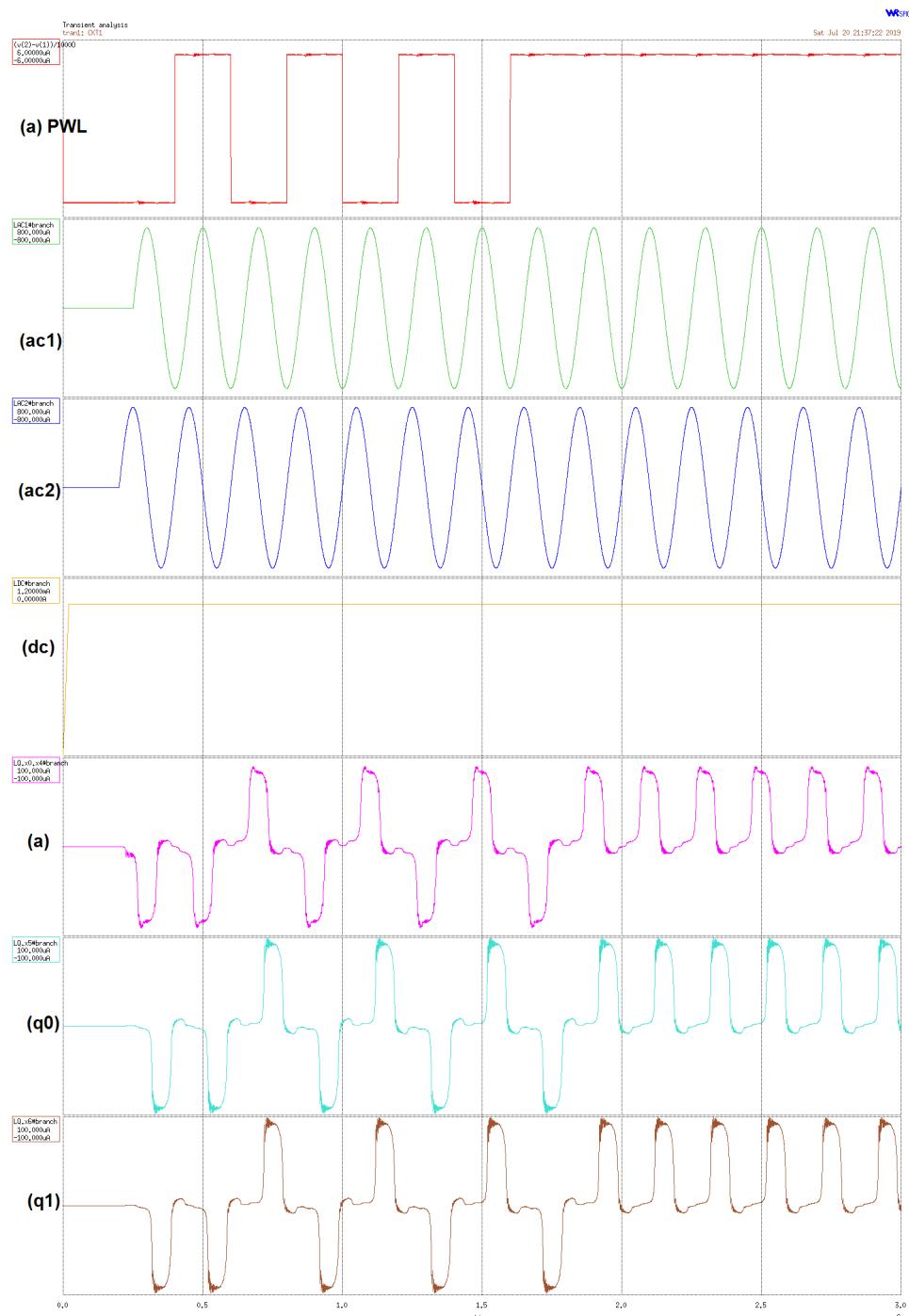
36 | LOUT 10 DOUT 25.3p
37 | LQ 7 0 5.84p
38 | LX XIN XOUT 6.51p
39 .ends bfr

```

**Listing 2.13:** spl2 netlist (.elecnet).

### Simulation result

Simulation waveform of a splitter 1-to-2 (spl2) DUT (design under test) with a 4-stage buffer before the input ‘a’. Another two 3-stage buffers are placed after the spl2’s output ‘b’ and ‘c’. Clock frequency is 5 GHz. Signals from top to bottom: buffer chain input (a) (input of the first stage buffers) as 1010110, AC source 1 (xin1) (generates phase 1 and 3), AC source 2 (xin2) (generates phase 2 and 4), and the outputs generated from the final stage of buffers (b and c) as 011010110 with two random initial outputs 01. This is because of the meander structure of AQFP circuits. In an 8-stage AQFP circuit, it takes two clock cycles to propagate the data to the output. Input peak-to-peak amplitude is  $\pm 5 \mu\text{A}$ , AC amplitude is  $\pm 800 \mu\text{A}$ , and DC is set to 1.2 mA.



**Figure 2.34:** spl2 analog waveform.

## Digital model

```

1 //-----
2 // Design Name : spl2
3 // File Name   : spl2.v
4 // Function    : 2-fanout splitter with built-in timing check
5 // Developer   : Olivia Chen (olivia.chen@ieee.org)
6 //-----
7 
```

```

8  `timescale 1ps/10fs
9  `define idle 3'd0
10 `define stop 3'd1
11 `define error 3'd2
12 module spl2(a, q0, q1, xin, xout, dcin, dcout);
13   input a;
14   output q0, q1;
15   inout xin, xout, dcin, dcout;
16   reg q0, q1;
17   parameter pul_wid = 100;
18   wire not_a;
19
20   assign not_a = !a;
21
22   biasDir_b I0(xin, xout, dcin, dcout, gatex);
23
24   initial begin
25
26     $timeformat(-12, 1, "_ps", 8); // time format
27
28     // output register initialization
29     q0 = 1'bz;
30     q1 = 1'bz;
31   end // initialization
32
33   specify
34     specparam a_xin    = 5;
35     specparam xin_a   = 50;
36
37     $setup(posedge a && a, posedge gatex, a_xin);
38     $setup(negedge a && not_a, posedge gatex, a_xin);
39     $setup(posedge gatex, negedge a && a, xin_a);
40     $setup(posedge gatex, posedge a && not_a, xin_a);
41
42   endspecify
43
44   always @(posedge gatex)
45     begin
46       if (a == 1 || a == 0)
47         begin
48           q0 <= a;
49           q0 <= #pul_wid 1'bz;
50           q1 <= a;
51           q1 <= #pul_wid 1'bz;
52         end
53       else
54         begin
55           q0 <= 1'bx;
56           q0 <= #pul_wid 1'bz;
57           q1 <= 1'bx;
58           q1 <= #pul_wid 1'bz;
59         end
60     end
61
62 endmodule

```

Listing 2.14: spl2 Verilog model code.



**Figure 2.35:** spl2 digital waveform. HDL ‘1’: AQFP ‘1’; HDL ‘0’: AQFP ‘0’; HDL ‘z’: inactive; HDL ‘x’: error.

### Switching energy

Different energy consumption results based on different data input patterns ( $a = 0$  and  $a = 1$ ) and clock frequencies.

**Table 2.13:** spl2 switching energy table.

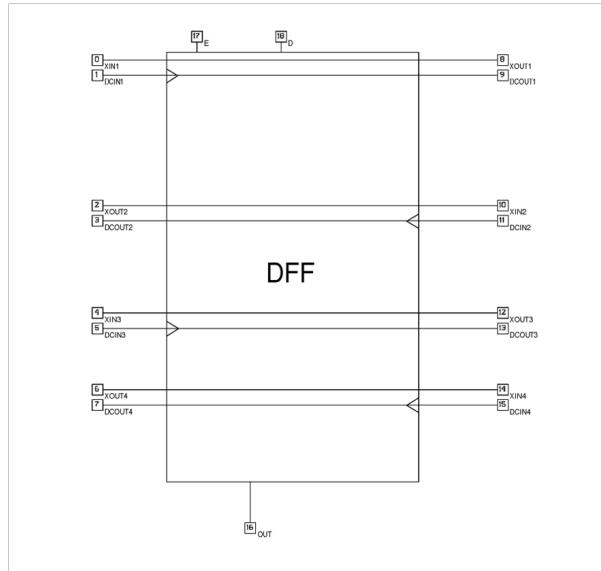
Clock rate (GHz)	Logic ‘0’ (J)	Logic ‘1’ (J)
0.1	1.28E-23	1.30E-23
0.2	2.57E-23	2.61E-23
0.5	6.42E-22	6.51E-22
1	1.30E-22	1.32E-22
2	2.69E-21	2.76E-21
5	8.83E-21	9.72E-21
10	2.61E-20	3.41E-20

## 2.2 Sequential Cells

### 2.2.1 DFF

D-Flip-Flop (DFF) is considered as a sequential logic element built from the developed AQFP logics cells. Here we present the symbol view, block diagram (schematic), netlist and simulation results from a test circuit.

#### Symbol

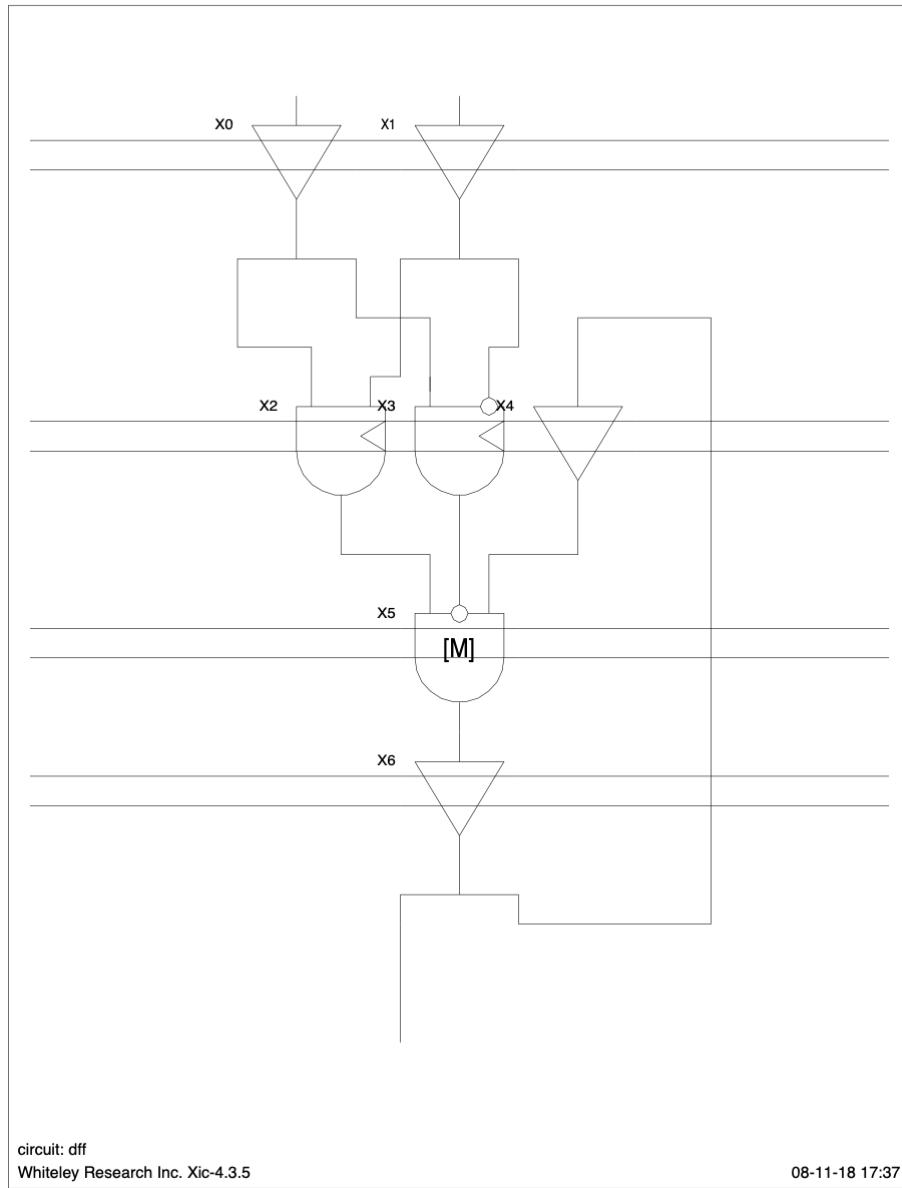


**Figure 2.36:** dff symbol.

**Table 2.14:** dff pin list.

Pin	Description
<b>E</b>	data input
<b>D</b>	data input
<b>XIN1</b>	serial clock input
<b>XIN2</b>	serial clock input
<b>XIN3</b>	serial clock input
<b>XIN4</b>	serial clock input
<b>DCIN1</b>	dc offset input
<b>DCIN2</b>	dc offset input
<b>DCIN3</b>	dc offset input
<b>DCIN4</b>	dc offset input
<b>Q</b>	data output
<b>XOUT1</b>	serial clock output
<b>XOUT2</b>	serial clock output
<b>XOUT3</b>	serial clock output
<b>XOUT4</b>	serial clock output
<b>DCOUT1</b>	dc offset output
<b>DCOUT2</b>	dc offset output
<b>DCOUT3</b>	dc offset output
<b>DCOUT4</b>	dc offset output

## Schematic



**Figure 2.37:** dff schematic.

## Layout

This is a multi-phase macro cell so we cannot fix the location of the excitation lines as it depends on how the DFF fits in a larger circuit design. Thus there is no fixed layout, as it should be placed dynamically on a case-by-case basis.

## Analog model

```

1 * Generated by Xic from cell dff
2 .subckt dff XIN1 DCIN1 XOUT2 DCOUT2 XIN3 DCIN3 XOUT4 DCOUT4 XOUT1 DCOUT1 XIN2
3 + DCIN2 XOUT3 DCOUT3 XIN4 DCIN4 OUT E D
4 X0 E XIN1 DCIN1 20 21 22 23 spl2
5 X1 D 20 21 XOUT1 DCOUT1 24 25 spl2
6 X2 24 22 31 30 XOUT2 DCOUT2 28 and_pp
7 X3 25 23 33 32 31 30 29 and_np
8 X4 33 26 XIN2 32 DCIN2 27 bfr
9 X5 28 29 XIN3 DCIN3 XOUT3 DCOUT3 27 34 maj_pnp
10 X6 34 XOUT4 DCOUT4 XIN4 DCIN4 OUT 26 spl2
11 .ends dff
12 .model jjmit jj(rtype=1, vg=2.6m,
13 + icrit=0.1m, r0=144, rn=16, cap=0.07p)
14
15 .subckt spl2 DIN XIN DCIN XOUT DCOUT A B
16 X0 XIN DIN XOUT DCIN DCOUT 8 bfr
17 X1 B A 8 branch2
18 .ends spl2
19
20 .subckt branch2 A B C
21 B0 5 4 7 jjmit area=2
22 B1 6 4 8 jjmit area=2
23 Lp 4 C 0.27p
24 Lp1 A 5 11.1p
25 Lp2 B 6 11.1p
26 .ends branch2
27
28 .subckt bfr XIN DIN XOUT DCIN DCOUT DOUT
29 B1 8 0 11 jjmit area=0.5
30 B2 9 0 12 jjmit area=0.5
31 B2_0 10 0 13 jjmit area=2
32 K1 Lx Ld 0.284
33 K2 Ld Lout 0
34 K3 Lx Lout 0
35 K4 Ld Lq 0
36 K5 Lx Lq 0
37 K6 Lout Lq -0.469
38 K7 L2 Ld -0.143
39 K8 L2 Lx -0.2
40 K9 Lx L1 -0.2
41 K10 Ld L1 -0.143
42 L1 8 7 1.4p
43 L2 7 9 1.4p
44 Ld DCIN DCOUT 6.09p
45 Lin DIN 7 0.804p
46 Lout 10 DOUT 27.6p
47 Lq 7 0 8.03p
48 Lx XIN XOUT 5.56p
49 .ends bfr
50
51 .subckt maj_pnp A B XIN DCIN XOUT DCOUT C D
52 X0 XIN A 11 DCIN 10 9 bfr
53 X1 11 B 14 10 13 12 inv
54 X2 14 C XOUT 13 DCOUT 15 bfr
55 X3 15 12 9 D branch3
56 .ends maj_pnp
57
58 .subckt inv XIN DIN XOUT DCIN DCOUT DOUT
59 B1 8 0 11 jjmit area=0.6
60 B2 9 0 12 jjmit area=0.6
61 B2_0 10 0 13 jjmit area=2
62 K1 Lq Ld 0
63 K2 Lx Ld 0.283
64 K3 Ld Lout 0
65 K4 Lx Lout 0
66 K5 Lx Lq 0
67 K6 Lout Lq 0.393
68 K7 L2 Ld -0.143
69 K8 L2 Lx -0.2
70 K9 Lx L1 -0.2

```

```

71 | K10 Ld L1 -0.143
72 | L1 8 7 1.4p
73 | L2 7 9 1.4p
74 | Ld DCIN DCOUT 6.08p
75 | Lin DIN 7 0.808p
76 | Lout 10 DOUT 27.6p
77 | Lq 7 0 6.75p
78 | Lx XIN XOUT 5.56p
79 | .ends inv
80
81 | .subckt branch3 A B C D
82 | B0 5 6 8 jjmit area=2
83 | B1 7 6 9 jjmit area=2
84 | Lip 6 D 0.315p
85 | Lp1 A 5 12p
86 | Lp2 B 6 10.4p
87 | Lp3 C 7 12p
88 | .ends branch3
89
90 | .subckt and_pp A B XIN DCIN XOUT DCOUT C
91 | X0 XIN A 10 DCIN 9 8 bfr
92 | X1 13 B XOUT 12 DCOUT 11 bfr
93 | X2 10 13 9 12 14 const0
94 | X3 11 14 8 C branch3
95 | .ends and_pp
96
97 | .subckt const0 XIN XOUT DCIN DCOUT DOUT
98 | B1 6 0 10 jjmit area=0.5
99 | B2 8 0 11 jjmit area=0.5
100 | Bout 9 0 12 jjmit area=2
101 | K1 Lq Ld -0.0046
102 | K2 Lx Ld 0.283
103 | K3 Ld Lout -0.000562
104 | K4 Lx Lout -0.000245
105 | K5 Lx Lq -0.00427
106 | K6 Lout Lq -0.474
107 | K7 L2 Ld -0.144
108 | K8 L2 Lx -0.201
109 | K9 Lx L1 -0.197
110 | K10 Ld L1 -0.138
111 | L1 6 7 1.4p
112 | L2 7 8 1.48p
113 | Ld DCIN DCOUT 6.13p
114 | Lout 9 DOUT 27.5p
115 | Lq 7 0 7.76p
116 | Lx XIN XOUT 5.62p
117 | .ends const0
118
119 | .subckt and_np A B XIN DCIN XOUT DCOUT C
120 | X0 XIN A 10 DCIN 9 8 inv
121 | X1 13 B XOUT 12 DCOUT 11 bfr
122 | X2 10 13 9 12 14 const0
123 | X3 11 14 8 C branch3
124 | .ends and_np

```

**Listing 2.15:** dff netlist (.elecnet).

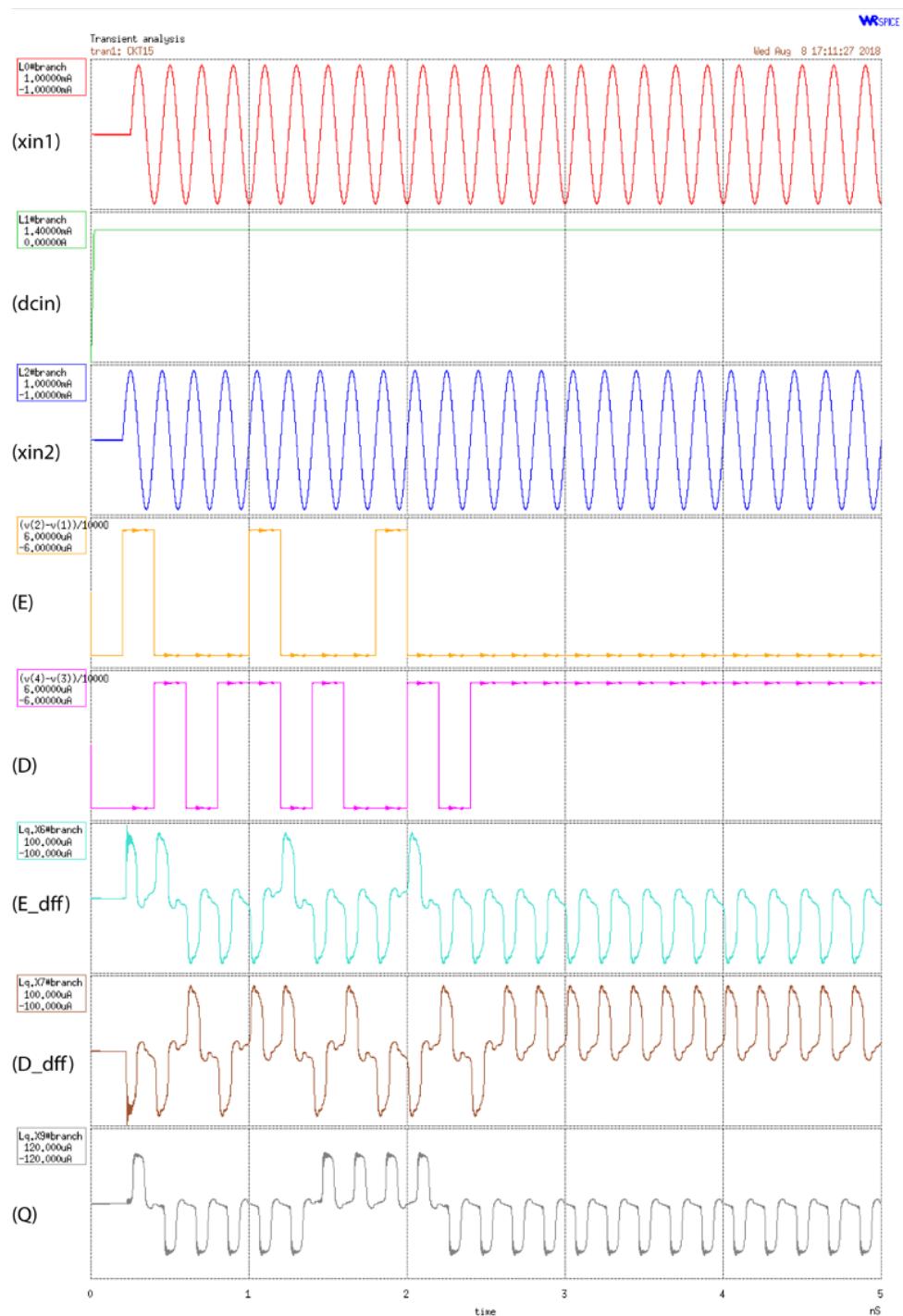
## Simulation result

Simulation waveform of a DFF DUT (design under test) with 4-stage buffer before the D input and before the E input. Another 4-stage buffer is placed after the DFF's Q output. Clock frequency is 5 GHz. Signals from top to bottom: buffer chain input (input of the first buffer), AC source 1 (generates phase 1 and 3), DC source, AC source 2 (generates phase 2 and 4), and the input E from generator going to test circuit, input D from generator going to test circuit, output E from buffer just before DFF, output D from buffer just before DFF and the output Q from buffer just after DFF. Input peak-to-peak

amplitude is  $\pm 5 \mu\text{A}$ , AC amplitude is  $\pm 800 \mu\text{A}$ , and DC is set to  $1.2 \text{ mA}$ .

When DFF is set to 0 ( $D = 1$ ), data is toggled while  $E=0$  to show data remains as 0, whereas when DFF is set to 1 ( $D=0$ ), data is toggled while  $E=0$  to show data remains as 1, when DFF is set to 0 again, data is toggled while  $E=0$  to show data remains as 0.

As shown in the waveform, where  $D = d_{\text{dff}} = (1)10001001000$  and  $E = e_{\text{dff}} = (0)010110100101$ , the output  $Q$  is  $(1)0000011110$ , correspondingly. The numbers marked in brackets represent the initial random outputs given by the meander structure of AQFP circuit, it takes one clock cycle to propagate data from the input buffer to the last-stage buffer.

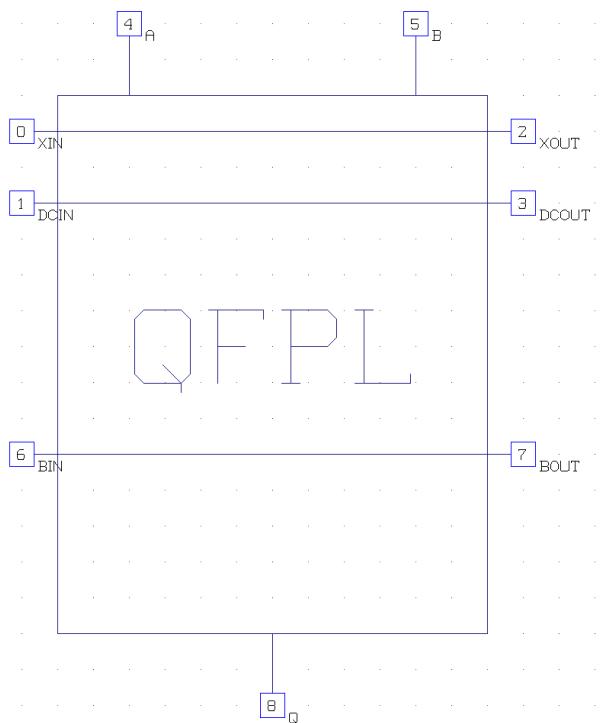


**Figure 2.38:** dff analog waveform.

## 2.2.2 QFPL

The quantum-flux-parametron latch (`qfpl`) is a native memory element in the AQFP library. It consists of two `qfpl` cells that serve as write gates and a single bi-stable storage gate that is based on the `bfr` core design with no ac excitation line but rather a single dc bias to indefinitely store the state of the `qfpl`.

### Symbol

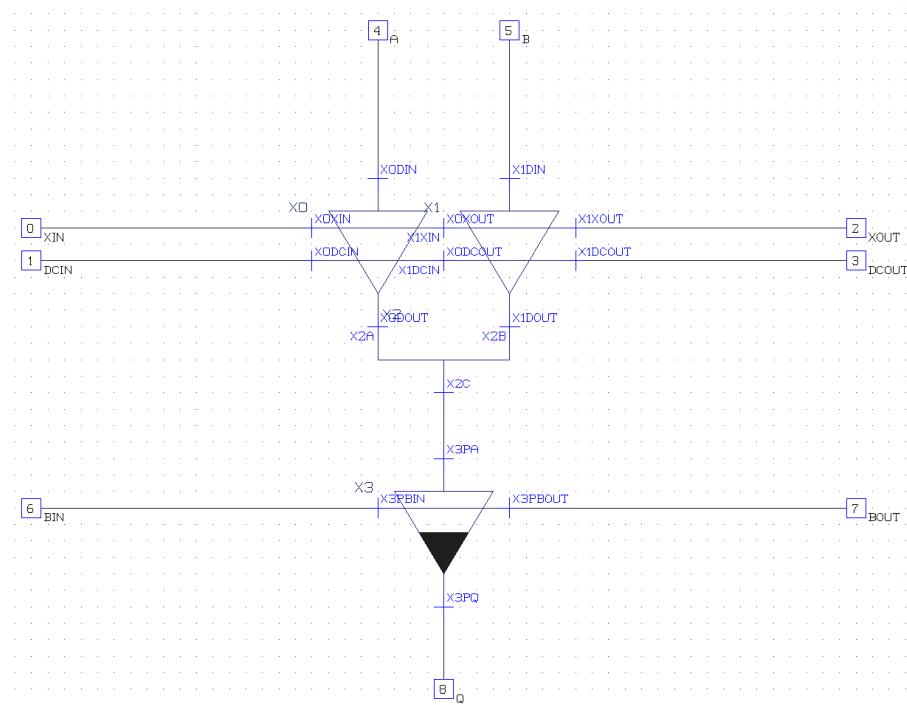


**Figure 2.39:** `qfpl` symbol.

**Table 2.15:** `qfpl` pin list.

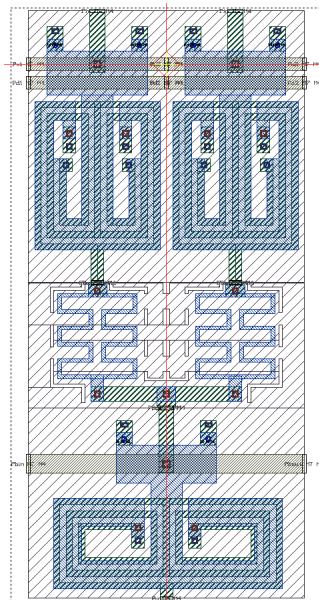
Pin	Description
<b>A</b>	data input
<b>B</b>	data input
<b>XIN</b>	serial clock input
<b>DCIN</b>	dc offset input
<b>BIN</b>	dc bias input for storage gate
<b>Q</b>	data output
<b>XOUT</b>	serial clock output
<b>DCOUT</b>	dc offset output
<b>BOUT</b>	dc bias input for storage gate

## Schematic



**Figure 2.40:** qfpl schematic.

## Layout



**Figure 2.41:** qfpl layout.

## Analog model

```

1  * Generated by Xic from cell qfpl
2
3  .subckt qfpl XIN DCIN XOUT DCOUT A B BIN BOUT Q
4  X0 XIN A 13 DCIN 12 11 bfr
5  X1 13 B XOUT 12 DCOUT 14 bfr
6  X2 11 14 10 branch2
7  X3 10 BIN BOUT Q storage_gate
8  .ends qfpl
9  .model jjmit jj(rtype=1, vg=2.6m,
10 + icrit=0.1m, r0=144, rn=16, cap=0.07p)
11
12 .subckt storage_gate PA PBIN PBOUT PQ
13 B1 6 0 9 jjmit area=0.5
14 B2 7 0 10 jjmit area=0.5
15 B2_0 8 0 11 jjmit area=2
16 K1 LD LOUT 0.000149
17 K2 LD LQ -0.000478
18 K3 LQ LOUT -0.493
19 K4 LD L2 0.167
20 K5 LD L1 0.167
21 L1 6 5 1.50p
22 L2 5 7 1.50p
23 LD PBIN PBOUT 11.5p
24 LIN PA 5 1.46p
25 LOUT 8 PQ 25.2p
26 LQ 5 0 5.04p
27 .ends storage_gate
28
29 .subckt branch2 A B C
30 B0 5 4 7 jjmit area=2
31 B1 6 4 8 jjmit area=2
32 LIP 4 C 0.39p
33 LP1 A 5 12.4p
34 LP2 B 6 12.4p
35 .ends branch2
36
37 .subckt bfr XIN DIN XOUT DCIN DCOUT DOUT
38 B1 8 0 11 jjmit area=0.5
39 B2 9 0 12 jjmit area=0.5
40 B2_0 10 0 13 jjmit area=2
41 K1 LX LD 0.2322
42 K2 LD LOUT 3.27E-5
43 K3 LX LOUT 3.68E-5
44 K4 LD LQ 4.9E-4
45 K5 LX LQ 5.11E-4
46 K6 LOUT LQ -0.3878
47 K7 L2 LD -0.1556
48 K8 L2 LX -0.228
49 K9 LX L1 -0.2284
50 K10 LD L1 -0.1559
51 L1 8 7 1.51p
52 L2 7 9 1.51p
53 LD DCIN DCOUT 6.94p
54 LIN DIN 7 1.526p
55 LOUT 10 DOUT 25.3p
56 LQ 7 0 5.84p
57 LX XIN XOUT 6.51p
58 .ends bfr

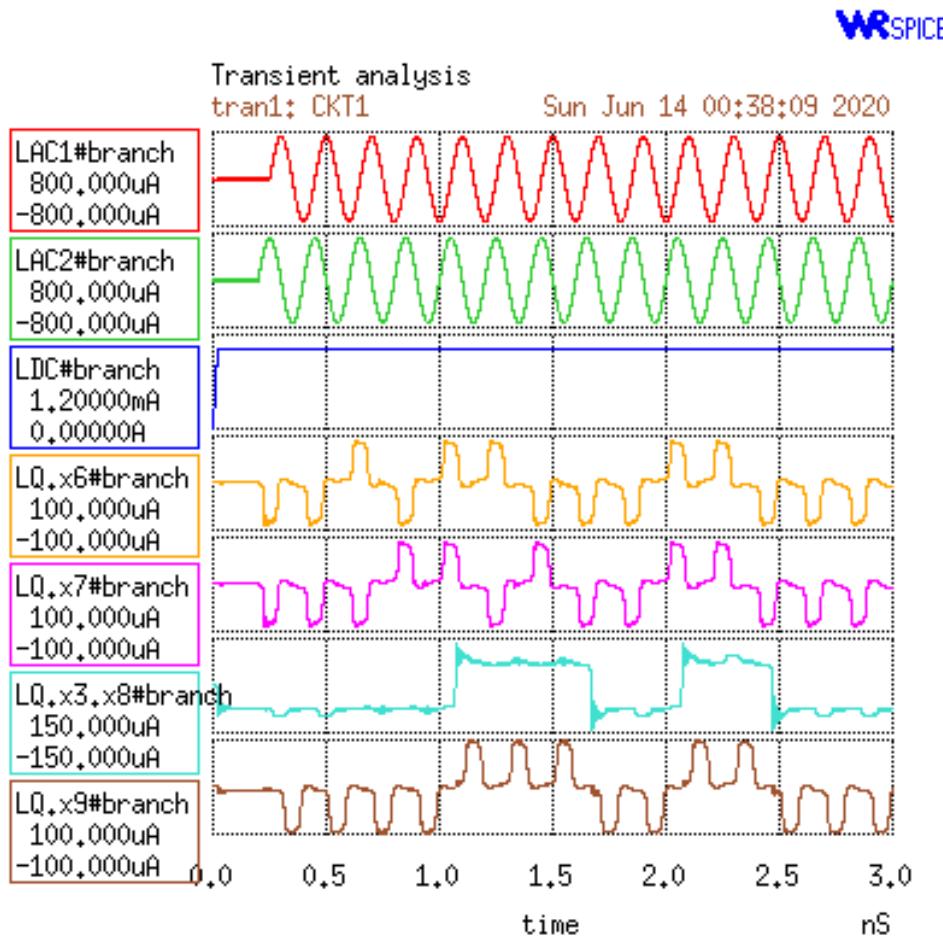
```

**Listing 2.16:** qfpl netlist (.elecnet).

## Simulation result

Simulation waveform of the **qfpl**. A 4-stage buffer chain is connected both input A and B. Each input is applied a test pattern with a peak-to-peak amplitude is  $\pm 5 \mu\text{A}$ . AC amplitude is  $800 \mu\text{A}$  at  $5 \text{GHz}$ , and DC is set to  $1.2 \text{mA}$ . Input A has a pattern of 010110001100 and B has a pattern of 001101001100. This results in an operation pattern of write ‘0’, hold, hold, write ‘1’, hold, hold, write ‘0’, write ‘0’, write ‘1’, write ‘1’, write ‘0’.

'0', write '0'. The resulting data output is 000111001100 as shown in the simulation waveform.



**Figure 2.42:** qfpl analog waveform.

## Digital model

```

1 //-----
2 // Design Name : qfpl
3 // File Name   : qfpl.v
4 // Function    : Model for qfpl
5 // Developer   : Christopher Ayala (chris.ayala@ieee.org)
6 //-----
7 `timescale 1ps/10fs
8
9 module qfpl(a, b, q, xin, xout, dcin, dc当地, bin, bout);
10
11   input a, b;
12   inout xin, xout, dcin, dc当地, bin, bout;
13   output q;
14
15   wire not_a, not_b;
16   reg q;
17
18   //use DC bias bidirection model for bin/bout
19   biasDC #(8) I1(bin, bout);
20   biasDir_b I2(xin, xout, dcin, dc当地, gate);
21 
```

```

22     assign not_a = !a;
23     assign not_b = !b;
24
25 initial begin
26     $timeformat(-12, 1, "_ps", 8); // time format
27     q = 1'bz;
28 end
29
30 specify
31     specparam a_xin    = 5;
32     specparam xin_a    = 50;
33     specparam b_xin    = 5;
34     specparam xin_b    = 50;
35
36     $setup(posedge a && a, posedge gatex, a_xin);
37     $setup(negedge a && not_a, posedge gatex, a_xin);
38     $setup(posedge gatex, negedge a && a, xin_a);
39     $setup(posedge gatex, posedge a && not_a, xin_a);
40
41     $setup(posedge b && b, posedge gatex, b_xin);
42     $setup(negedge b && not_b, posedge gatex, b_xin);
43     $setup(posedge gatex, negedge b && b, xin_b);
44     $setup(posedge gatex, posedge b && not_b, xin_b);
45 endspecify
46
47 always @(posedge gatex) begin
48     if (a==b && bin==1'b1) begin
49         //write case (using logical compare == so only valid logic values pass)
50         q <= a;
51
52         //no reset in QFPL, state is held indefinitely unlike other AQFP cells
53
54     end else if (a!=b && bin==1'b1) begin
55         //keep state
56     end else begin
57         //Possible errors:
58         //If QFPL bias is not initialized to '1' before operation
59         //then the QFPL should not work. (Detects misconnect of bias).
60
61         //If data are not valid (still Z or X), then a timing error occurred
62         //because of logical equality even 'z=='z' or 'x=='x' will not pass)
63
64         q <= 1'bx;
65     end
66 end
67 endmodule

```

Listing 2.17: qfpl Verilog model code.

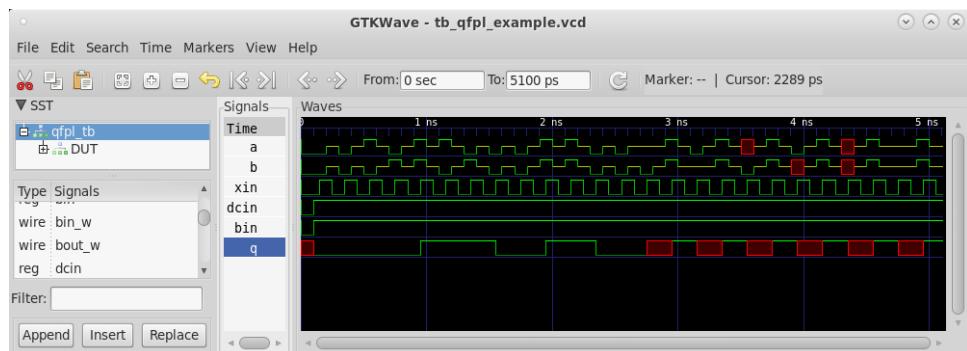


Figure 2.43: qfpl digital waveform. HDL '1': AQFP '1'; HDL '0': AQFP '0'; HDL 'z': inactive; HDL 'x': error.

**Switching energy**

To be investigated in the future.

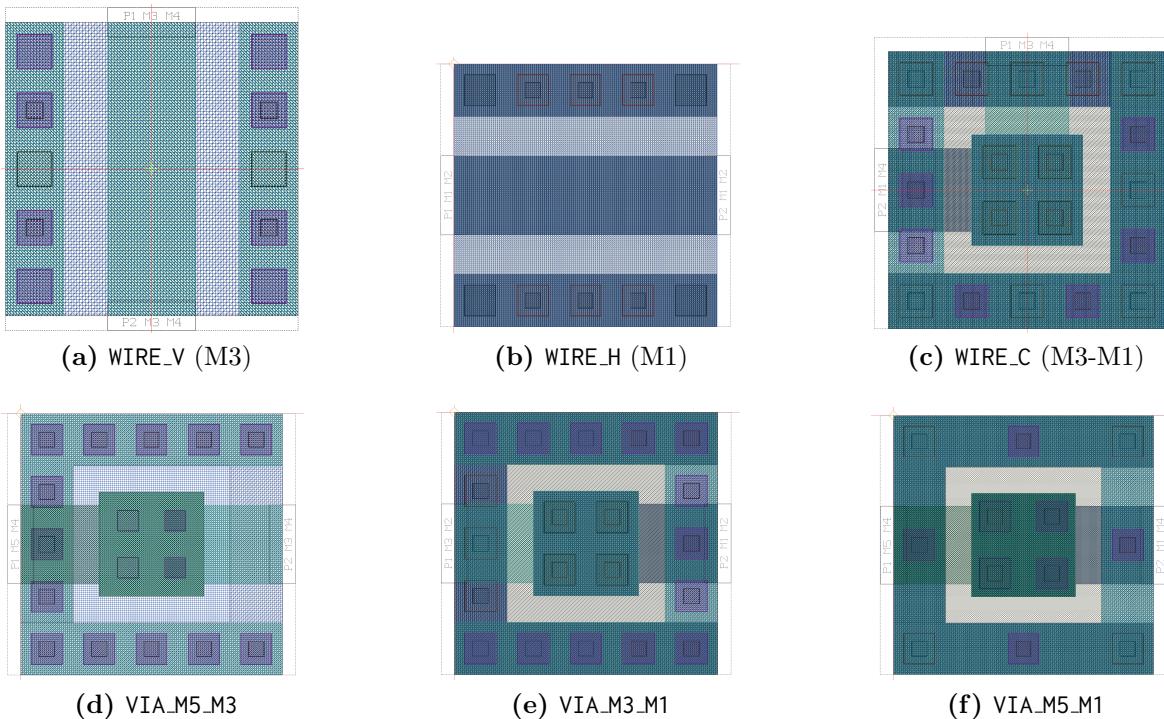
## 2.3 Interconnect slices

The interconnect of AQFP logic is composed of passive transmission lines (PTLs). PTLs are stripline structures where a signal line has a dedicated ground plane above and below it. RSFQ logic uses striplines to ballistically transport an SFQ pulse from RSFQ cell to another through active transmitter-receiver pairs. AQFP logic uses PTLs to send positive or negative current pulses and the logic cells can connect directly to PTLs without using transmitter-receiver circuits.

The active logic area is dedicated to layers above the M4 ground plane whereas the routing interconnecting exists below the M4 ground plane. The AQFP interconnect slices are  $10\text{ }\mu\text{m} \times 10\text{ }\mu\text{m}$ . Table 2.16 summarizes the different types of interconnect cells that are available and Fig. 2.44 shows their corresponding layouts.

**Table 2.16:** Summary of interconnect  $10\text{ }\mu\text{m} \times 10\text{ }\mu\text{m}$  slices.

Name	Signal layer	Ground layers	Inductance pH	Purpose
WIRE_V	M3	M4 M2	0.88751	north-south interconnects
WIRE_H	M1	M2 M0	0.88254	east-west interconnects
WIRE_C	M3 M1	M4 M0	0.91037	switch wiring direction
VIA_M5_M3	M5 M3	M4 M2	1.63553	logic cell (M5) to routing (M3-M1)
VIA_M3_M1	M3 M1	M4 M0	1.27220	stripline via between M3-M1
VIA_M5_M1	M5 M1	M4 M0	1.95804	stripline staggered via between M5-M1



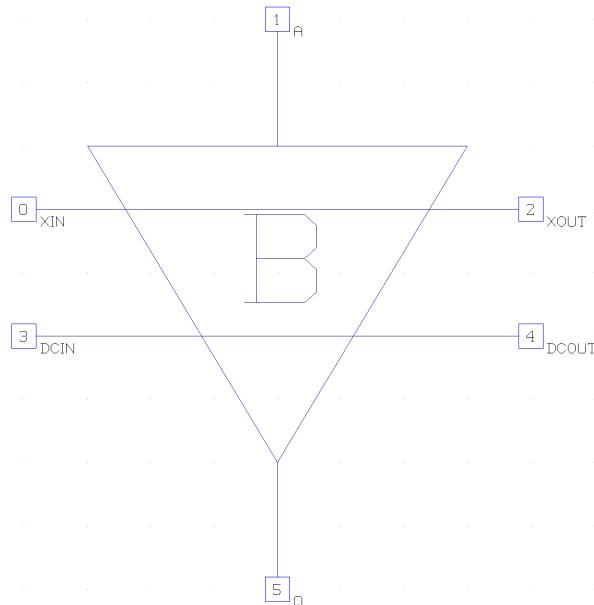
**Figure 2.44:** Cell-to-cell wire interconnect slices made of stripline-type passive transmission lines. Each slice is  $10\text{ }\mu\text{m} \times 10\text{ }\mu\text{m}$ .

## 2.4 Off-chip Interface

QDC (QFP-DC-Converter) is an off-chip interface circuit consisting of a dc-SQUID that converts an AQFP signal to an amplified unipolar return-to-zero (RZ) voltage signal for external read out. The qdc test circuit consists of a single buffer before the qdc input and the qdc itself. The qdc has 3 stages: inverter, booster, and stack. Stack is the dc-SQUID itself coupled to an AQFP buffer. The stack creates an output voltage only when it senses negative current at its input. Thus, the qdc includes an inverter so that a positive input results in a high output voltage level. The booster is used to amplify the output current level. Here we only introduce the booster and stack, together with simulation results of a qdc test circuit.

### 2.4.1 Booster

#### Symbol

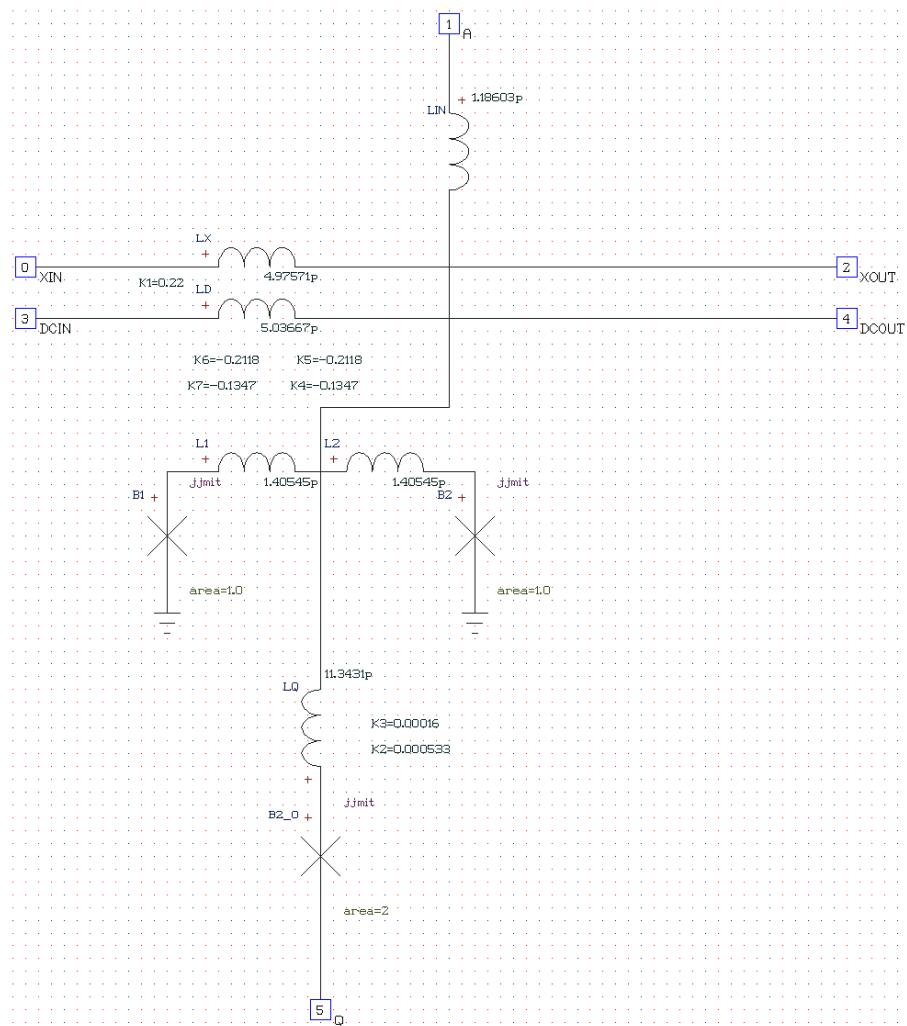


**Figure 2.45:** booster symbol.

**Table 2.17:** booster pin list.

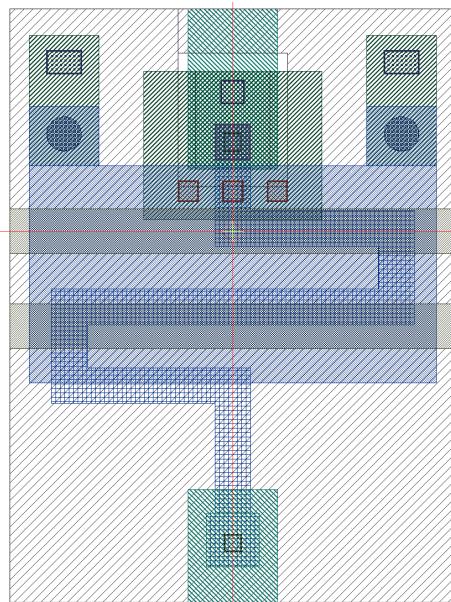
Pin	Description
<b>A</b>	data input
<b>XIN</b>	serial clock input
<b>DCIN</b>	dc offset input
<b>Q</b>	data output
<b>XOUT</b>	serial clock output
<b>DCOUT</b>	dc offset output

## Schematic



**Figure 2.46:** booster schematic.

## Layout



**Figure 2.47:** booster layout.

## Analog model

```

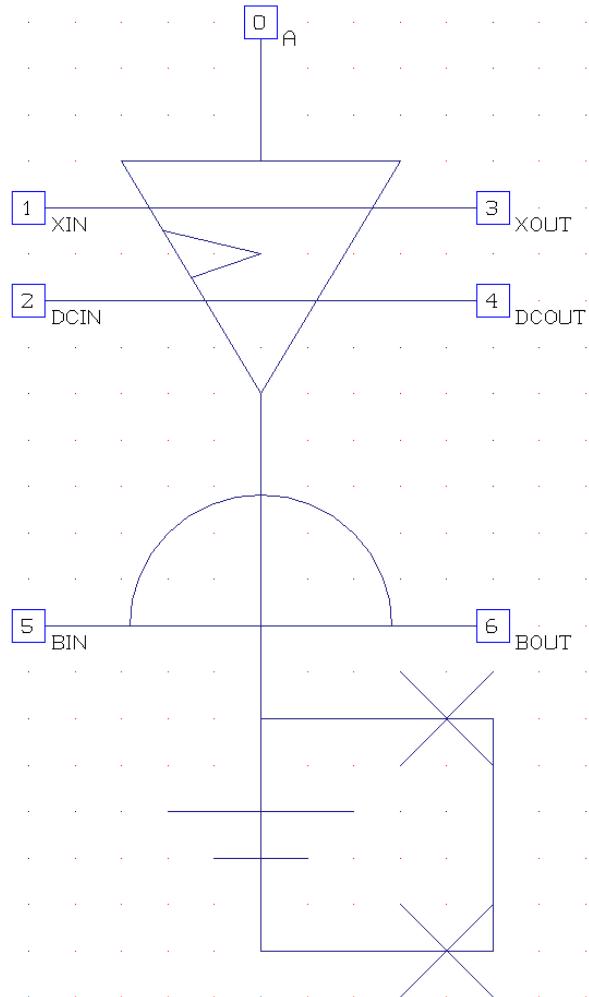
1 * Generated by Xic from cell booster
2
3 .subckt booster XIN A XOUT DCIN DCOUT Q
4 B1 8 0 11 jjmit area=1.0
5 B2 9 0 12 jjmit area=1.0
6 B2_0 10 Q 13 jjmit area=2
7 K1 LX LD 0.22
8 K2 LD LQ 0.000533
9 K3 LX LQ 0.00016
10 K4 L2 LD -0.1347
11 K5 L2 LX -0.2118
12 K6 LX L1 -0.2118
13 K7 LD L1 -0.1347
14 L1 8 7 1.40545p
15 L2 7 9 1.40545p
16 LD DCIN DCOUT 5.03667p
17 LIN A 7 1.18603p
18 LQ 10 7 11.3431p
19 LX XIN XOUT 4.97571p
20 .ends booster
21 .model jjmit jj(rtype=1, vg=2.6m,
22 + icrit=0.1m, r0=144, rn=16, cap=0.07p)

```

**Listing 2.18:** booster netlist (.elecnet).

## 2.4.2 Stack

### Symbol

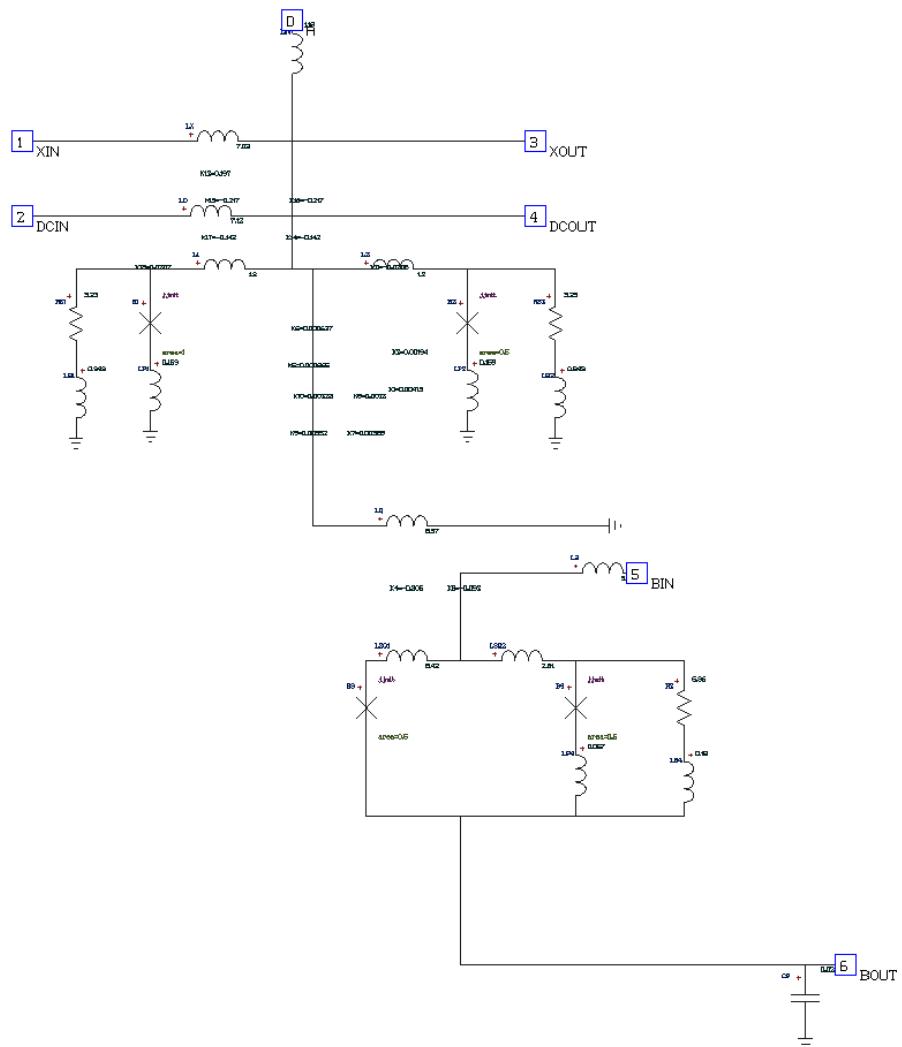


**Figure 2.48:** stack symbol.

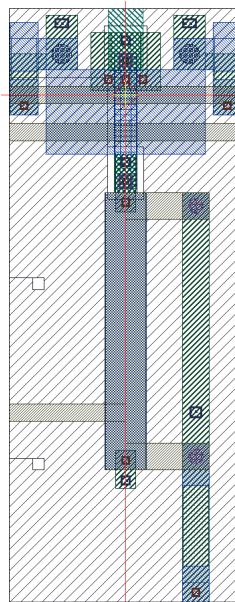
**Table 2.18:** stack pin list.

Pin	Description
A	data input
XIN	serial clock input
DCIN	dc offset input
BIN	bias input for SQUID
XOUT	serial clock output
DCOUT	dc offset output
BOUT	bias output for SQUID

## Schematic



**Figure 2.49:** stack schematic.



**Figure 2.50:** stack layout.

## Analog model

```

1 * Generated by Xic from cell stack
2
3 .subckt stack A XIN DCIN XOUT DCOUT BIN BOUT
4 B1 9 17 20 jjmit area=1
5 B2 10 18 21 jjmit area=0.5
6 B3 14 BOUT 22 jjmit area=0.5
7 B4 15 19 23 jjmit area=0.5
8 CP BOUT 0 0.02
9 K1 LD L3 0.00415
10 K2 L3 LX 0.00194
11 K3 LSQ2 LQ -0.092
12 K4 LQ LSQ1 -0.305
13 K5 LD LQ 0.000865
14 K6 LQ LX 0.000637
15 K7 LSQ2 LD 0.00389
16 K8 LX LSQ2 0.0012
17 K9 LSQ1 LD 0.00552
18 K10 LX LSQ1 0.00223
19 K11 LX LS2 -0.0206
20 K12 LD LX 0.197
21 K13 LS1 LX 0.0207
22 K14 L2 LD -0.142
23 K15 L1 LX -0.217
24 K16 L2 LX -0.217
25 K17 LD L1 -0.142
26 L1 9 8 1.2
27 L2 8 10 1.2
28 L3 13 BIN 5.25
29 LD DCIN DCOUT 7.12
30 LIN A 8 1.19
31 LP1 17 0 0.159
32 LP2 18 0 0.159
33 LP4 19 BOUT 0.057
34 LQ 8 0 8.97
35 LS1 11 0 0.943
36 LS2 12 0 0.943
37 LS4 16 BOUT 0.18
38 LSQ1 14 13 8.42
39 LSQ2 13 15 2.81

```

```

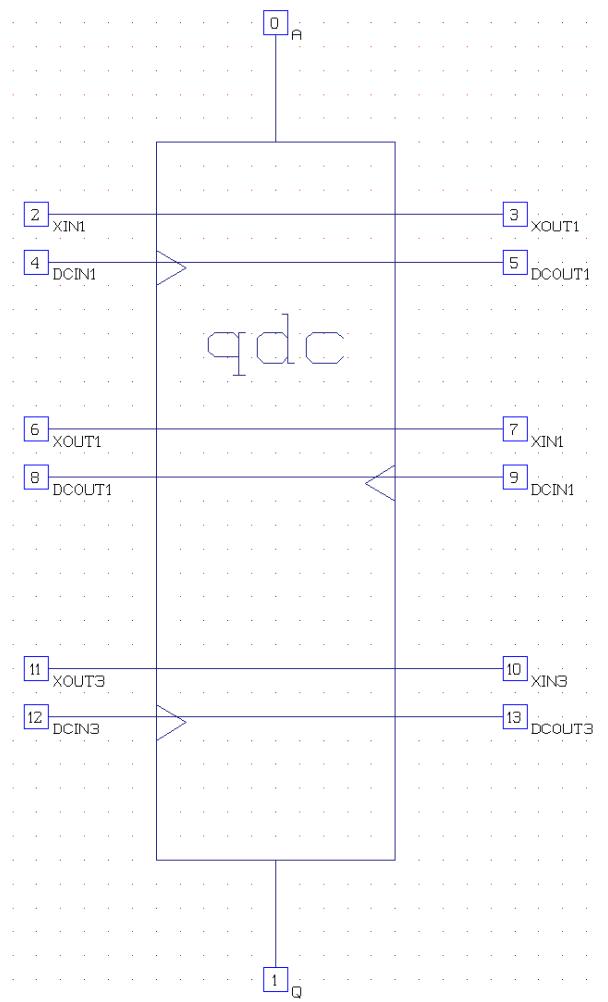
40 | LX XIN XOUT 7.03
41 | R2 15 16 6.36
42 | RS1 9 11 3.23
43 | RS2 10 12 3.23
44 | .ends stack
45 | .model jjmit jj(rtype=1, vg=2.6m,
46 | + icrit=0.1m, r0=144, rn=16, cap=0.07p)

```

**Listing 2.19:** stack netlist (.elecnet).

### 2.4.3 QDC

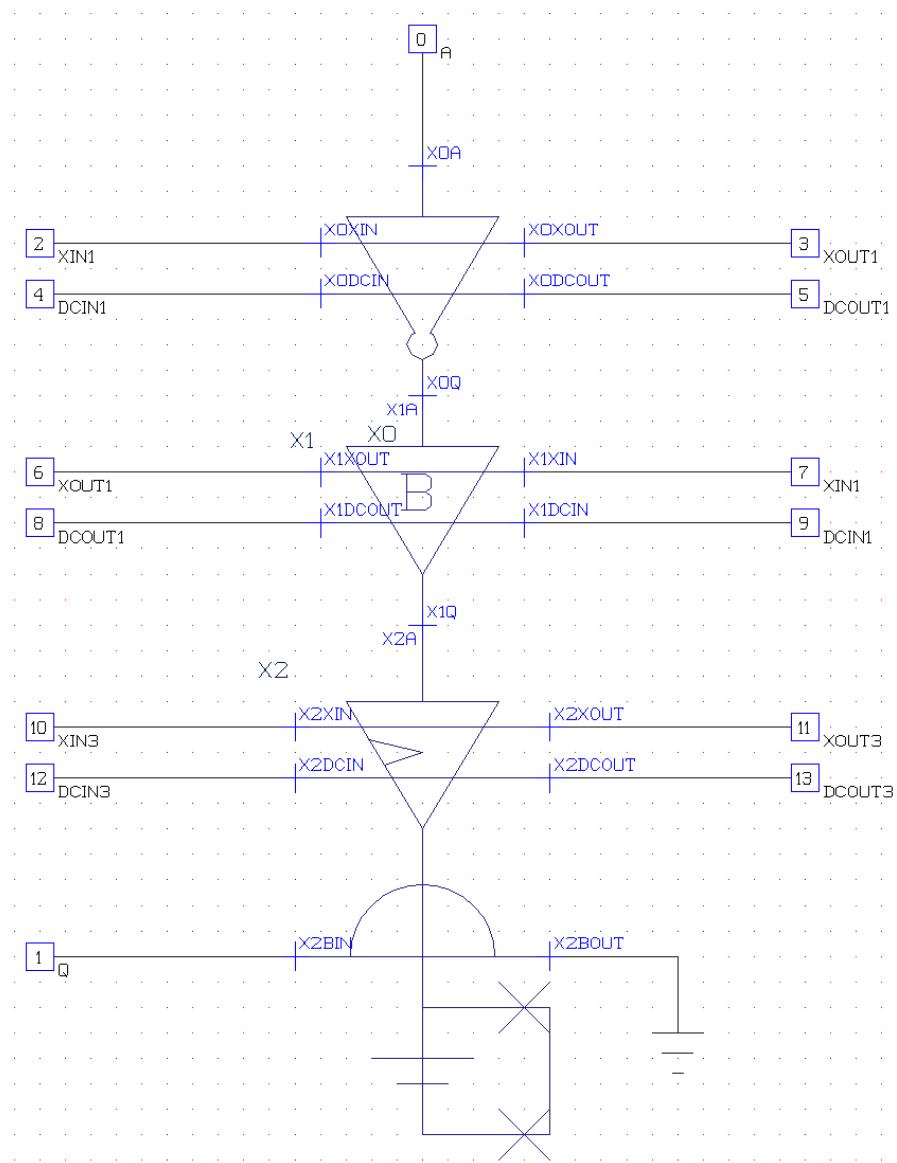
#### Symbol

**Figure 2.51:** qdc symbol.

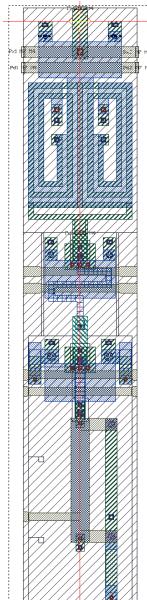
**Table 2.19:** qdc pin list.

Pin	Description
<b>A</b>	data input
<b>XIN1</b>	serial AC clock input (inv)
<b>DCIN1</b>	dc offset input (inv)
<b>XIN2</b>	serial AC clock input (booster)
<b>DCIN2</b>	dc offset input (booster)
<b>XIN3</b>	serial AC clock input (stack)
<b>DCIN3</b>	dc offset input (stack)
<b>XOUT1</b>	serial AC clock output (inv)
<b>DCOUT1</b>	dc offset output (inv)
<b>XOUT2</b>	serial AC clock output (booster)
<b>DCOUT2</b>	dc offset output (booster)
<b>XOUT3</b>	serial AC clock output (stack)
<b>DCOUT3</b>	dc offset output (stack)
<b>Q</b>	data output (observed through bias input of SQUID)

## Schematic



**Figure 2.52:** qdc schematic.



**Figure 2.53:** qdc layout.

## Analog model

```

1 * Generated by Xic from cell qdc
2
3 .subckt qdc A Q XIN1 XOUT1 DCIN1 DCOUT1 XOUT1 XIN1 DCOUT1 DCIN1 XIN3 XOUT3
4 + DCIN3 DCOUT3
5 X0 XIN1 A XOUT1 DCIN1 DCOUT1 11 inv
6 X1 XIN1 11 XOUT1 DCIN1 DCOUT1 12 booster
7 X2 12 XIN3 DCIN3 XOUT3 DCOUT3 Q 0 stack
8 .ends qdc
9 .model jjmit jj(rtype=1, vg=2.6m,
10 + icrit=0.1m, r0=144, rn=16, cap=0.07p)
11
12
13 .subckt stack A XIN DCIN XOUT DCOUT BIN BOUT
14 B1 9 17 20 jjmit area=1
15 B2 10 18 21 jjmit area=0.5
16 B3 14 BOUT 22 jjmit area=0.5
17 B4 15 19 23 jjmit area=0.5
18 CP BOUT 0 0.02
19 K1 LD L3 0.00415
20 K2 L3 LX 0.00194
21 K3 LSQ2 LQ -0.092
22 K4 LQ LSQ1 -0.305
23 K5 LD LQ 0.000865
24 K6 LQ LX 0.000637
25 K7 LSQ2 LD 0.00389
26 K8 LX LSQ2 0.0012
27 K9 LSQ1 LD 0.00552
28 K10 LX LSQ1 0.00223
29 K11 LX LS2 -0.0206
30 K12 LD LX 0.197
31 K13 LS1 LX 0.0207
32 K14 L2 LD -0.142
33 K15 L1 LX -0.217
34 K16 L2 LX -0.217
35 K17 LD L1 -0.142
36 L1 9 8 1.2
37 L2 8 10 1.2
38 L3 13 BIN 5.25
39 LD DCIN DCOUT 7.12

```

```

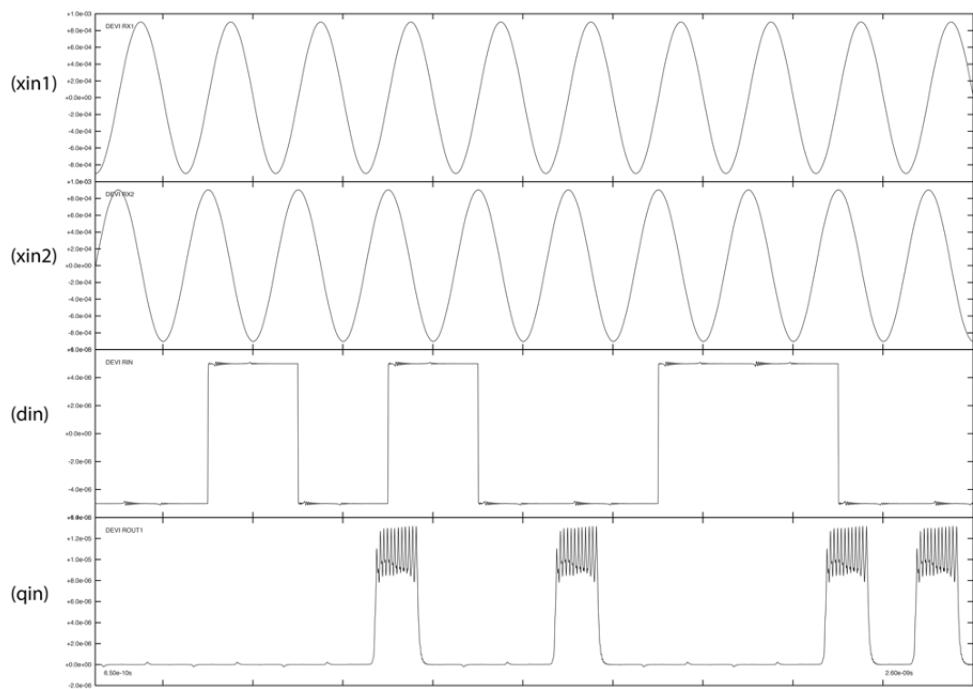
40 | LIN A 8 1.19
41 | LP1 17 0 0.159
42 | LP2 18 0 0.159
43 | LP4 19 BOUT 0.057
44 | LQ 8 0 8.97
45 | LS1 11 0 0.943
46 | LS2 12 0 0.943
47 | LS4 16 BOUT 0.18
48 | LSQ1 14 13 8.42
49 | LSQ2 13 15 2.81
50 | LX XIN XOUT 7.03
51 | R2 15 16 6.36
52 | RS1 9 11 3.23
53 | RS2 10 12 3.23
54 .ends stack
55
56 .subckt inv XIN A XOUT DCIN DCOUT Q
57 B1 8 0 11 jjmit area=0.6
58 B2 9 0 12 jjmit area=0.6
59 B2_0 10 0 13 jjmit area=2
60 K1 LQ LD 0
61 K2 LX LD 0.2379
62 K3 LD LOUT 0
63 K4 LX LOUT 0
64 K5 LX LQ 0
65 K6 LOUT LQ 0.3756
66 K7 L2 LD -0.1647
67 K8 L2 LX -0.2265
68 K9 LX L1 -0.2265
69 K10 LD L1 -0.165
70 L1 8 7 1.49p
71 L2 7 9 1.49p
72 LD DCIN DCOUT 6.48p
73 LIN A 7 1.43p
74 LOUT 10 Q 27.1p
75 LQ 7 0 5.7p
76 LX XIN XOUT 6.49p
77 .ends inv
78
79 .subckt booster XIN A XOUT DCIN DCOUT Q
80 B1 8 0 11 jjmit area=1.0
81 B2 9 0 12 jjmit area=1.0
82 B2_0 10 Q 13 jjmit area=2
83 K1 LX LD 0.22
84 K2 LD LQ 0.000533
85 K3 LX LQ 0.00016
86 K4 L2 LD -0.1347
87 K5 L2 LX -0.2118
88 K6 LX L1 -0.2118
89 K7 LD L1 -0.1347
90 L1 8 7 1.40545p
91 L2 7 9 1.40545p
92 LD DCIN DCOUT 5.03667p
93 LIN A 7 1.18603p
94 LQ 10 7 11.3431p
95 LX XIN XOUT 4.97571p
96 .ends booster

```

**Listing 2.20:** qdc netlist (.elecnet).

## Simulation result

An input of 0 1 0 1 0 0 1 1 is sent to the input of the qdc which corresponds to the output shown on the waveform. Signals from top to bottom: AC source 1 (xin1) (generates phase 1 and 3), AC source 2 (xin2) (generates phase 2 and 4), Input at the buffer before the qdc and the output of qdc (measured across a resistor connected to qdc's output). Input peak-to-peak amplitude is  $\pm 5 \mu\text{A}$ , AC amplitude is  $\pm 800 \mu\text{A}$ , and DC is set to 1.2 mA.



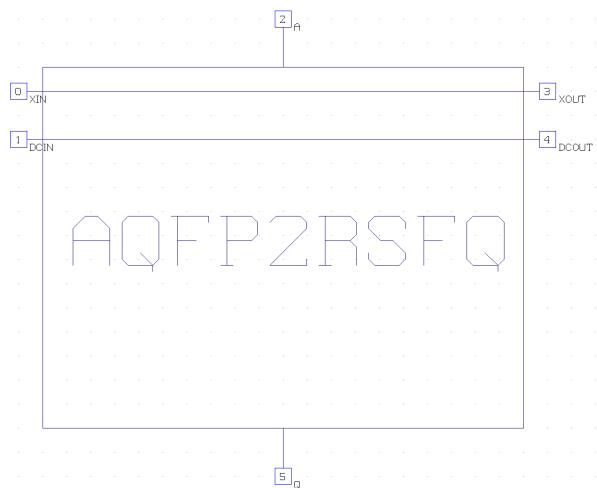
**Figure 2.54:** qdc analog waveform.

## 2.5 On-chip Interfaces

### 2.5.1 AQFP2RSFQ

`aqfp2rsfq` is an interface that allows AQFP logic to transfer its current-based data to SFQ logic which uses SFQ-encoded data. It is based on an AQFP `bfr` cell and a magnetically coupled dc/SFQ converter. Both components are synchronized to the AC excitation current such when it rises, the AQFP buffer sets its output while an SFQ clock is generated through a Josephson junction switching event caused by magnetic flux applied from the AC excitation current via magnetic coupling. The output of AQFP buffer is magnetically coupled to the input branch of the Josephson comparator in the dc/SFQ converter. The polarity of this coupling is negative so the circuit effectively behaves like an inverter. While it is possible to make the circuit non-inverting, the negative coupling is more natural in physical layout. The comparator will produce an appropriate inverting output when the SFQ clock arrives at the comparator. When the AQFP has a logic ‘0’ state during excitation, the dc/SFQ converter will produce an output SFQ pulse. Otherwise, no SFQ pulse is generated.

#### Symbol



**Figure 2.55:** `aqfp2rsfq` symbol.

**Table 2.20:** `aqfp2rsfq` pin list.

Pin	Description
<b>A</b>	data input (AQFP)
<b>XIN</b>	serial clock input
<b>DCIN</b>	dc offset input
<b>Q</b>	data output (RSFQ)
<b>XOUT</b>	serial clock output
<b>DCOUT</b>	dc offset output

## Schematic

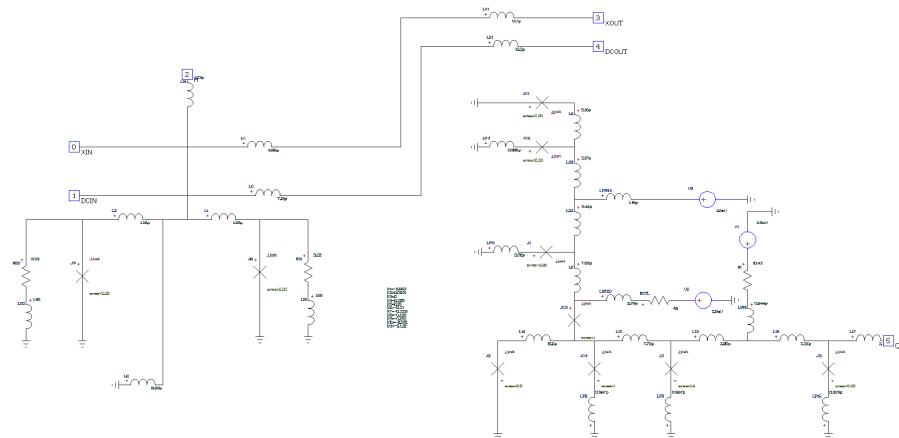


Figure 2.56: aqfp2rsfq schematic.

## Layout

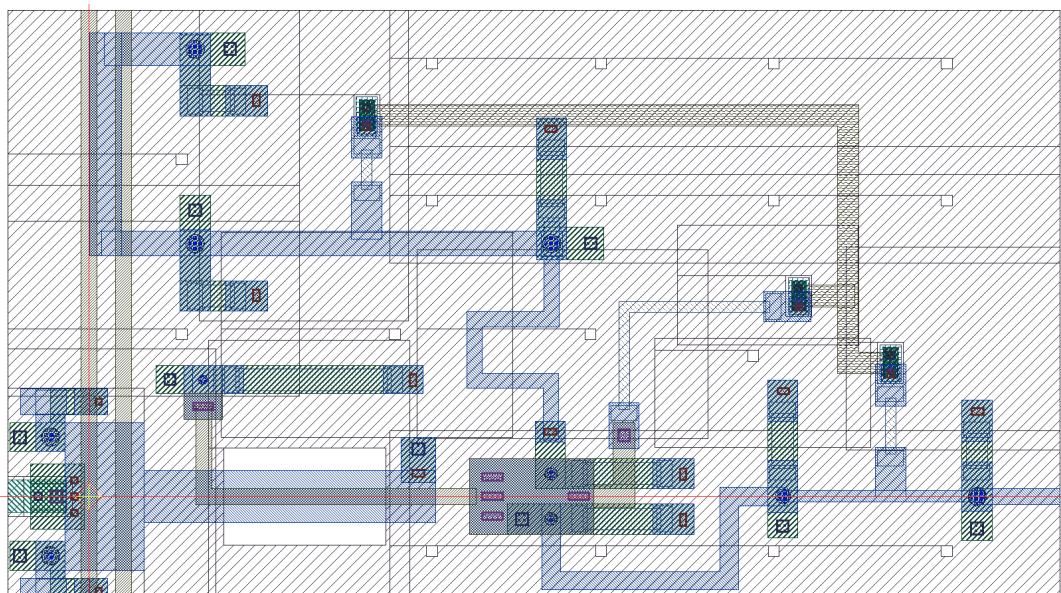


Figure 2.57: aqfp2rsfq layout.

## Analog model

```

1 * Generated by Xic from cell aqfp2rsfq
2
3 .subckt aqfp2rsfq XIN DCIN A XOUT DCOUT Q
4 J1 26 16 36 jjmit area=2.20
5 J2 32 21 42 jjmit area=1.4
6 J3 33 23 43 jjmit area=2.20
7 J8 15 0 37 jjmit area=2.20
8 J9 14 0 38 JJmit area=2.20
9 JC1 0 9 34 jjmit area=2.20

```

```

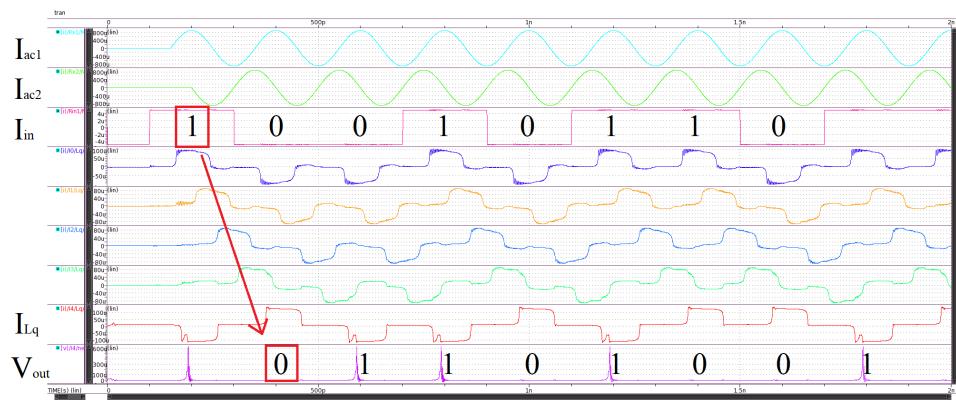
10 | JC2 24 11 35 jjmit area=2.20
11 | JC3 17 20 39 jjmit area=1
12 | JC4 31 20 41 jjmit area=1
13 | JE 0 19 40 jjmit area=0.5
14 | K1 LQ L10 -0.563
15 | K2 LQ LD 0.0001
16 | K3 LQ LX 0
17 | K4 LX LD 0.205
18 | K5 LX1 LD1 0.15
19 | K6 LX1 L6 -0.21
20 | K7 LD1 L6 -0.223
21 | K8 LD L1 -0.128
22 | K9 L1 LX -0.192
23 | K10 LX L2 -0.192
24 | K11 L2 LD -0.128
25 | L0 16 17 7.83p
26 | L1 10 15 1.26p
27 | L2 14 10 1.26p
28 | L6 9 11 5.16p
29 | L10 19 20 15.5p
30 | L12 20 21 7.75p
31 | L13 21 22 2.85p
32 | L15 22 23 2.32p
33 | L17 23 Q 2.11p
34 | L22 12 16 3.44p
35 | L33 11 12 2.17p
36 | LD DCIN 8 7.15p
37 | LD1 8 DCOUT 12.2p
38 | LIN A 10 1.23p
39 | LP4 0 24 0.885p
40 | LP8 0 31 0.567p
41 | LP9 0 32 0.567p
42 | LP11 0 26 0.96p
43 | LP16 0 33 0.324p
44 | LPR1 29 22 0.544p
45 | LPR33 12 13 1.18p
46 | LQ 0 10 8.68p
47 | LRP20 17 30 2.78p
48 | LS1 27 0 1.65
49 | LS2 28 0 1.65
50 | LX XIN 7 6.86p
51 | LX1 7 XOUT 12.1p
52 | R1 25 29 10.43
53 | RCTL 30 18 45
54 | RS1 15 27 3.23
55 | RS2 14 28 3.23
56 | .ends aqfp2rsfq
57 | .model jjmit jj(rtype=1, vg=2.6m,
58 | + icrit=0.1m, r0=144, rn=16, cap=0.07p)

```

**Listing 2.21:** aqfp2rsfq netlist (.elecnet).

### Simulation result

Simulation waveform of the aqfp2rsfq. The data input peak-to-peak amplitude is  $\pm 5 \mu\text{A}$ , AC amplitude is  $800 \mu\text{A}$ , and DC is set to  $1.2 \text{ mA}$ . The dc/SFQ component uses a bias voltage of  $2.5 \text{ mV}$ . The AQFP data pattern is 10010110 which resulted in the SFQ comparator producing an inverted data pattern of 01101001 due to the negative coupling between the AQFP and dc/SFQ converter.



**Figure 2.58:** aqfp2rsfq analog waveform.

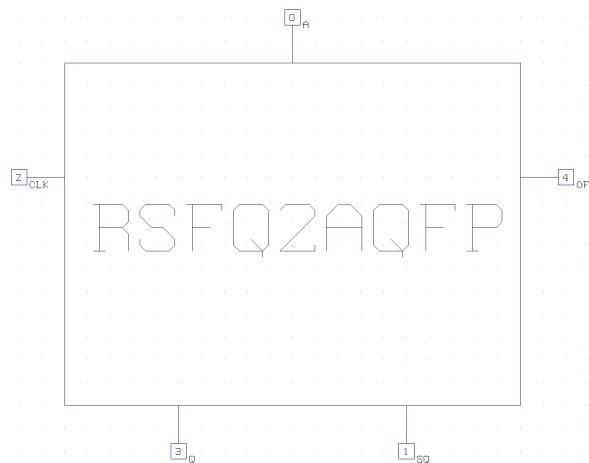
### Switching energy

To be investigated in the future.

## 2.5.2 RSFQ2AQFP

`rsfq2aqfp` is an interface that allows RSFQ logic to transfer its SFQ-based data to AQFP logic which operates on bidirectional current-encoded data. It is based on an RSFQ DFF whose storage loop is magnetically coupled to an output inductor. An inductor with about  $-400 \mu\text{A}$  offset current is coupled to the output inductor to shift the current levels induced into the output inductor from unipolar to bipolar. This bipolar current is then suitable as data input for AQFP. When the DFF is in logic state '1', a positive output current is produced. Otherwise, the output current will remain negative. An SFQ clock is used to reset the `rsfq2aqfp` interface back to state '0'.

### Symbol

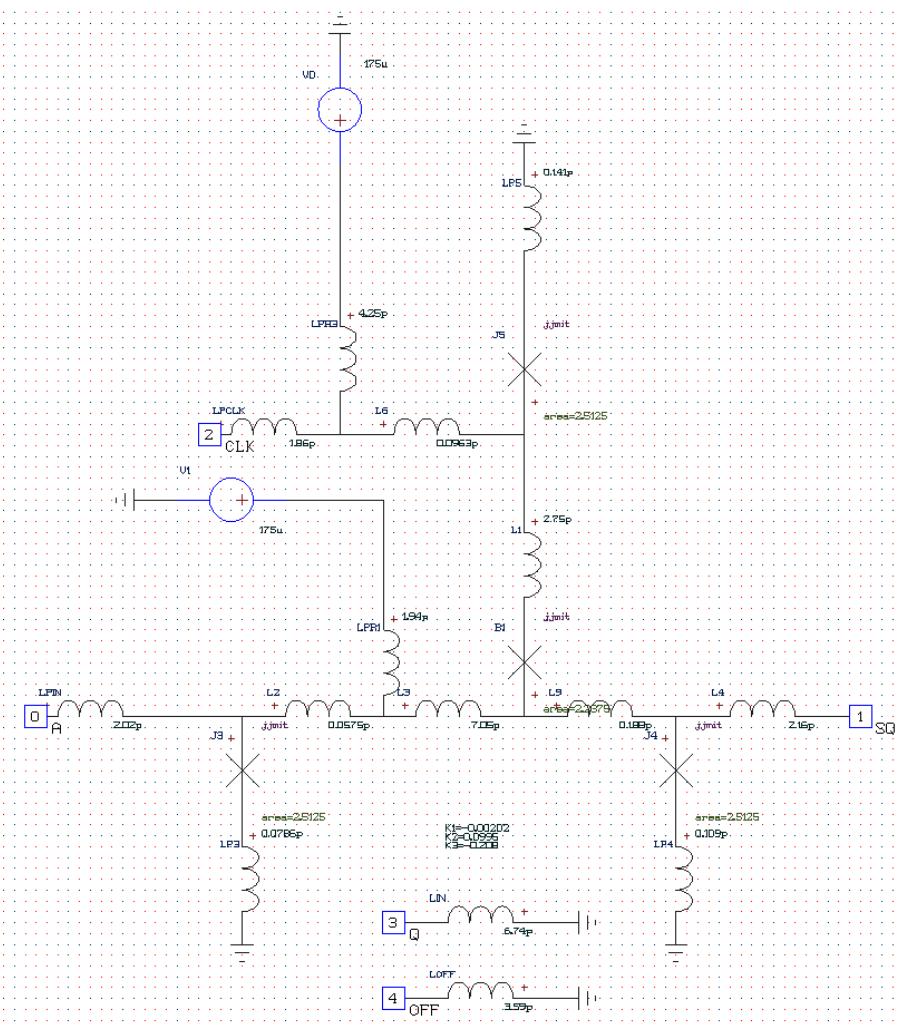


**Figure 2.59:** `rsfq2aqfp` symbol.

**Table 2.21:** `rsfq2aqfp` pin list.

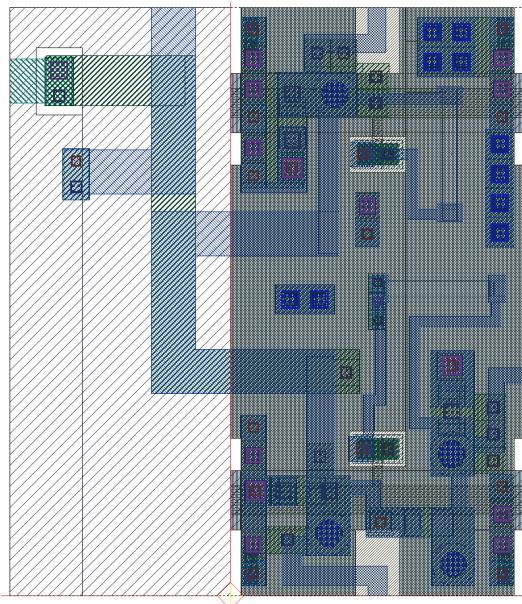
Pin	Description
<b>A</b>	data input (RSFQ)
<b>CLK</b>	clock (RSFQ)
<b>OFF</b>	dc offset to shift the level of Q
<b>Q</b>	data output (AQFP)
<b>SQ</b>	data output (SFQ) to eject SFQ pulse

## Schematic



**Figure 2.60:** rsfq2aqfp schematic.

## Layout



**Figure 2.61:** rsfq2aqfp layout.

## Analog model

```

1 * Generated by Xic from cell rsfq2aqfp
2
3 .subckt rsfq2aqfp A SQ CLK Q OFF
4 J3 11 15 21 jjmit area=2.5125
5 J4 14 16 22 jjmit area=2.5125
6 J5 9 7 17 jjmit area=2.5125
7 K1 L3 LOFF -0.00202
8 K2 LIN LOFF 0.0995
9 K3 LIN L3 -0.208
10 L2 11 12 0.0575p
11 L3 12 13 7.05p
12 L4 14 SQ 2.16p
13 L6 8 9 0.0963p
14 L9 13 14 0.188p
15 LIN 0 Q 6.74p
16 LOFF 0 OFF 3.59p
17 LP3 15 0 0.0786p
18 LP4 16 0 0.109p
19 LP5 0 7 0.141p
20 LPCLK CLK 8 1.86p
21 LPIN A 11 2.02p
22 LPR1 10 12 1.94p
23 LPR3 6 8 4.25p
24 .ends rsfq2aqfp
25 .model jjmit jj(rtype=1, vg=2.6m,
26 + icrit=0.1m, r0=144, rn=16, cap=0.07p)

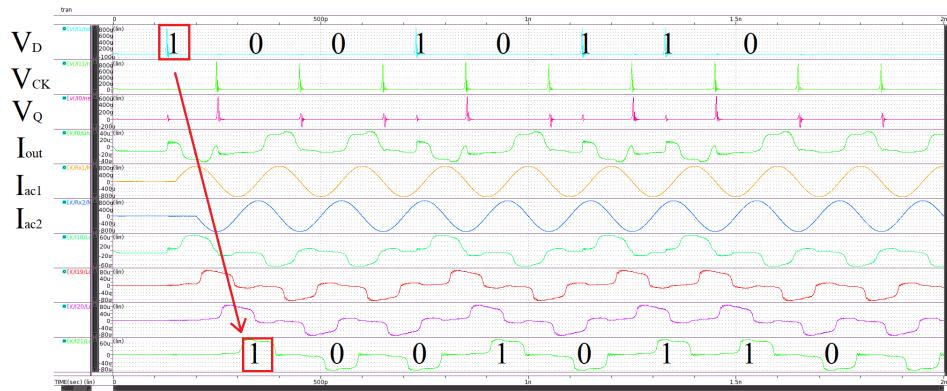
```

**Listing 2.22:** rsfq2aqfp netlist (.elecnet).

## Simulation result

Simulation waveform of the rsfq2aqfp. The data input is provided through JTLs connected to the RSFQ-based DFF with an input pattern of 10010110. An SFQ clock pulse is provided at the same frequency as the 5 GHz AQFP AC excitation clock. The

AC amplitude is 800  $\mu$ A, and DC is set to 1.2 mA. The bipolar AQFP output current matches the same data as the SFQ-based encoding of 10010110.



**Figure 2.62:** rsfq2aqfp analog waveform.

### Switching energy

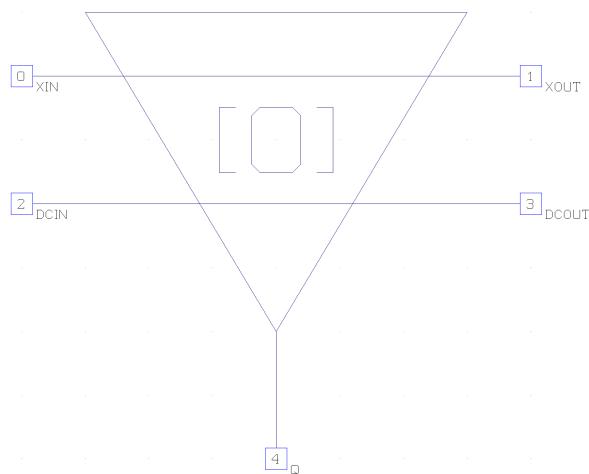
To be investigated in the future.

## 2.6 Sub-Cells

### 2.6.1 Constant

Constant cells contain constant 0 (const0) and constant 1 (const1) that are building blocks to develop AQFP logic AND and OR cells. Both const0 and const1 are designed by changing the symmetric architecture of a SQUID into asymmetric to generate the constant positive current (as logic ‘1’) or negative current (as logic ‘0’). Here we only introduce the constant 0.

#### Symbol

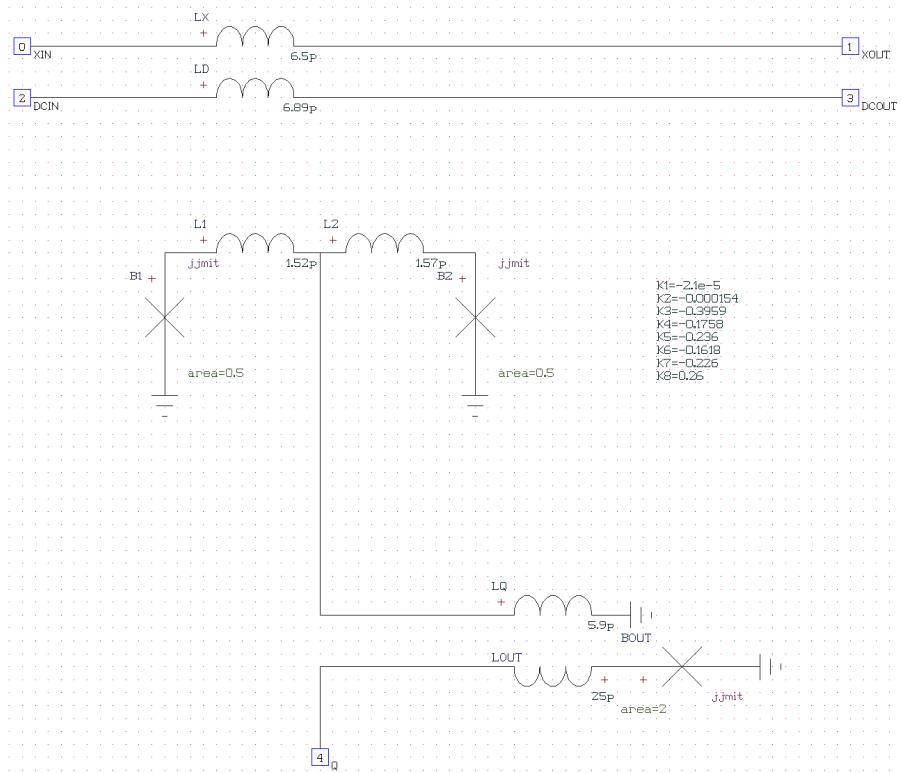


**Figure 2.63:** const0 symbol.

**Table 2.22:** const0 pin list.

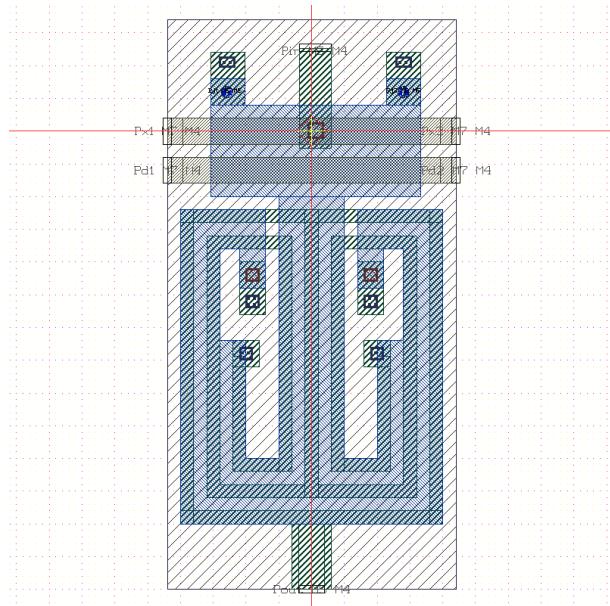
Pin	Description
XIN	serial clock input
DCIN	dc offset input
Q	data output
XOUT	serial clock output
DCOUT	dc offset output

## Schematic



**Figure 2.64:** `const0` schematic.

## Layout



**Figure 2.65:** `const0` layout.

## Analog model

```

1 * Generated by Xic from cell const0
2
3 .subckt const0 XIN XOUT DCIN DCOUT DOUT
4 B1 6 0 10 jjmit area=0.5
5 B2 8 0 11 jjmit area=0.5
6 BOUT 9 0 12 jjmit area=2
7 K1 LX LOUT -2.1e-5
8 K2 LOUT LD -0.000154
9 K3 LQ LOUT -0.3959
10 K4 L2 LD -0.1758
11 K5 L2 LX -0.236
12 K6 LD L1 -0.1618
13 K7 L1 LX -0.226
14 K8 LX LD 0.26
15 L1 6 7 1.52p
16 L2 7 8 1.57p
17 LD DCIN DCOUT 6.89p
18 LOUT 9 DOUT 25p
19 LQ 7 0 5.9p
20 LX XIN XOUT 6.5p
21 .ends const0
22 .model jjmit jj(rtype=1, vg=2.6m,
23 + icrit=0.1m, r0=144, rn=16, cap=0.07p)

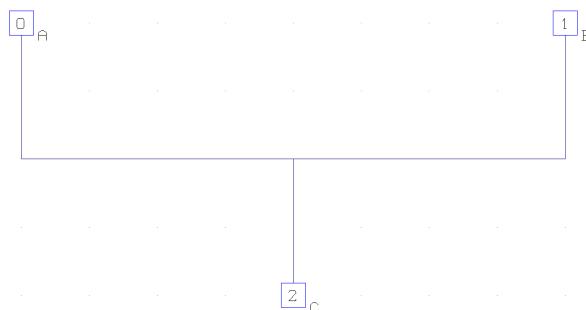
```

**Listing 2.23:** const0 netlist (.elecnet).

### 2.6.2 Branch

A 1-to-n (or n-to-1) branch, which consists of (n+1) superconducting inductors, is used to split or merge AQFP current. It is a basic building block to make AQFP logic cells such as AND, OR, Majority and Splitter introduced in section II. Here we only introduce 1-to-2 branch, others can be found as separate files in the deliverables.

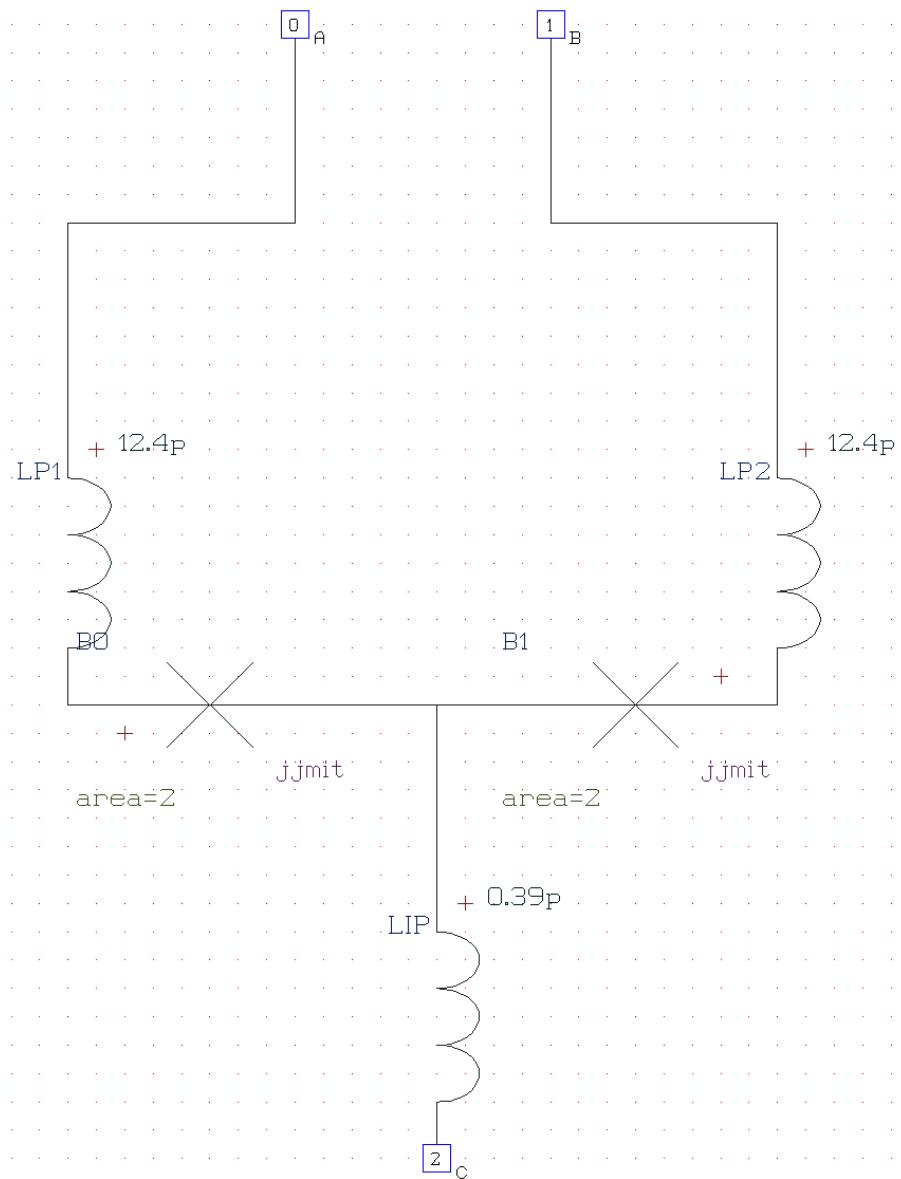
#### Symbol



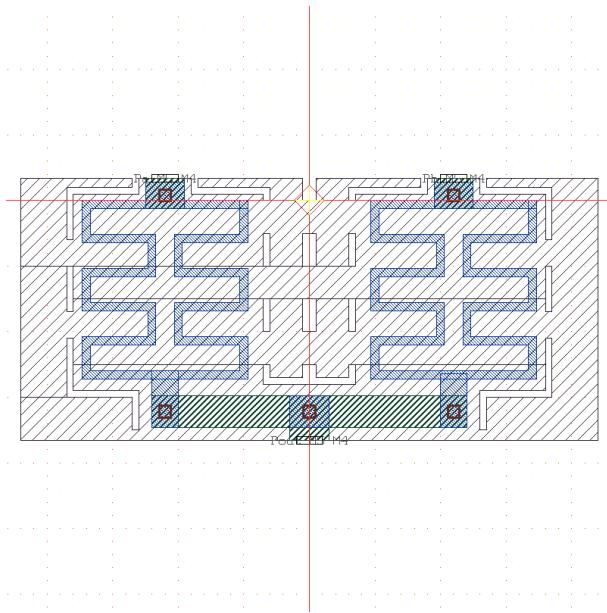
**Figure 2.66:** branch2 symbol.

**Table 2.23:** branch2 pin list.

Pin	Description
A	data inout
B	data inout
C	data inout

**Schematic****Figure 2.67:** branch2 schematic.

## Layout



**Figure 2.68:** branch2 layout.

## Analog model

```

1 * Generated by Xic from cell branch2
2
3 .subckt branch2 A B C
4 B0 5 4 7 jjmit area=2
5 B1 6 4 8 jjmit area=2
6 LIP 4 C 0.39p
7 LP1 A 5 12.4p
8 LP2 B 6 12.4p
9 .ends branch2
10 .model jjmit jj(rtype=1, vg=2.6m,
11 + icrit=0.1m, r0=144, rn=16, cap=0.07p)

```

**Listing 2.24:** branch2 netlist (.elecnet).

### 2.6.3 HDL ac/dc interface

Verilog module ‘biasDir\_b.v’ is an internal module for each AQFP logic gate for handling the excitation ac clock (xin/xout) and dc bias (dcin/dcout). Because some cells such as ‘bfr’ can be placed in a normal or flipped orientation, it was necessary to develop a bi-directional interface to handle the ac/dc bias. For gates such as AND or OR which can only be placed in a single direction relative to the bias direction, we enforce a uni-directional version of this interface. This interface also determines the relative directions of ac and dc bias applied to the cell. If their directions are the same, the ac clock (modeled as a digital square wave) will be applied to the logic cell as is. If their directions are different, the gate will receive an inverted version of the ac clock. This allows us to model 4-phase clocking at the HDL level using two ac clocks (ac1 with a 0 degree shift, and ac2 with a -90 degree shift) and a dc bias (modeled as a 0 to 1 transition at the beginning of simulation).

## Digital model

```

1 //-----
2 // Design Name : biasDir
3 // File Name   : biasDir.v
4 // Function     : determines direction of excitation
5 //                 bias and creates normalized gate
6 //                 excitation signal
7 // Developer   : Christopher Ayala & Olivia Chen
8 //                 (olivia.chen@ieee.org)
9 //-----
10 'timescale 1ps/10fs
11
12 module biasDir_b(xin, xout, dcin, dcout, gatex);
13
14 parameter propagationDelay = 0.198;
15
16 inout xin, xout;
17 inout dcin, dcout;
18 output gatex;
19 reg xiFrst, xoFrst, dcifrst, dcoFrst, xiReg, xoReg, dciReg, dcoReg;
20 reg fndDirx, fndDirdc, gatex, sameDir, clock;
21
22 initial begin
23     xiFrst = 1'b0;
24     xoFrst = 1'b0;
25     dcifrst = 1'b0;
26     dcoFrst = 1'b0;
27     xiReg = 1'b0;
28     xoReg = 1'b0;
29     dciReg = 1'b0;
30     dcoReg = 1'b0;
31     fndDirx = 1'b0;
32     fndDirdc = 1'b0;
33     gatex = 1'b0;
34     sameDir = 1'b0;
35     clock = 1'b0;
36 end
37
38 always@(xin or xout or dcin or dcout) begin
39     if((xin==1'b1 || xin==1'b0) && !fndDirx) begin
40         xiFrst = 1'b1;
41         fndDirx = 1'b1;
42     end
43
44     if((xout==1'b1 || xout==1'b0) && !fndDirx) begin
45         xoFrst = 1'b1;
46         fndDirx = 1'b1;
47     end
48
49     if((dcin==1'b1) && !fndDirdc) begin
50         dcifrst = 1'b1;
51         fndDirdc = 1'b1;
52     end
53
54     if((dcout==1'b1) && !fndDirdc) begin
55         dcoFrst = 1'b1;
56         fndDirdc = 1'b1;
57     end
58
59     xiReg <= #propagationDelay xin;
60     xoReg <= #propagationDelay xout;
61     dciReg <= dcin;
62     dcoReg <= dcout;
63     clock <= xiFrst ? xin : xout;
64     sameDir <= dcifrst ^~ xiFrst;
65     gatex <= sameDir? clock : !clock;
66 end
67

```

```

68 |   assign xin = xoFrst ? xoReg : 1'bz;
69 |   assign xout = xiFrst ? xiReg : 1'bz;
70 |   assign dcin = dcoFrst ? dcoReg : 1'bz;
71 |   assign dout = dciFrst ? dciReg : 1'bz;
72 |
73 | endmodule

```

**Listing 2.25:** HDL ac/dc interface Verilog model code.

## 2.6.4 HDL dc interface

Verilog module ‘biasDC.v’ is an internal module for special cells such as the `storage_gate` which only have a dc bias line. This module does not apply any special normalization but it is necessary for resolving the bi-directional ports of the dc bias in HDL gate-level modeling.

### Digital model

```

1 //-----
2 // Design Name : biasDC
3 // File Name   : biasDC.v
4 // Function     : determines direction of DC bias and
5 //                  resolves direction of bi-directional ports
6 // Developer   : Christopher Ayala (chris.ayala@ieee.org)
7 //-----
8
9 `timescale 1ps/10fs
10
11 module biasDC(a, b);
12
13 parameter propagationDelay = 0.033;
14 parameter length = 1;
15
16 inout a, b;
17
18 reg aFrst, bFrst, aReg, bReg, fndDir;
19
20 initial begin
21   aFrst = 1'b0;
22   bFrst = 1'b0;
23   aReg = 1'b0;
24   bReg = 1'b0;
25   fndDir = 1'b0;
26 end
27
28 always@(a or b) begin
29   if((a==1'b1 || a==1'b0) && !fndDir) begin
30     aFrst = 1'b1;
31     fndDir = 1'b1;
32   end
33
34   if((b==1'b1 || b==1'b0) && !fndDir) begin
35     bFrst = 1'b1;
36     fndDir = 1'b1;
37   end
38
39   aReg <= #(propagationDelay*length) a;
40   bReg <= #(propagationDelay*length) b;
41 end
42
43 assign a = bFrst ? bReg : 1'bz;
44 assign b = aFrst ? aReg : 1'bz;
45
46 endmodule

```

**Listing 2.26:** HDL dc interface Verilog model code.

## 2.7 Standard Delay Format (SDF)

Included in the cell library under the `verilog` sub-directory, we include a global Standard Delay Format (SDF) file which includes timing parameters extracted from AQFPTX [4]. This SDF file is for the standard 5 GHz clock rate under nominal bias levels. The listing is shown in Listing 2.27. As noted in the roadmap, the `specify` statements in conjunction with the data generated in the SDF are still preliminary as an appropriate Verilog simulator supporting the SDF constructs was not yet available until now. In Phase 2B, we will ensure the timing checks and timing parameters are working with the newly developed simulator.

```

1  (DELAYFILE
2   (SDFVERSION "4.0")
3   (DESIGN "top")
4   (DATE "Wednesday June 13 GMT 2020")
5   (VENDOR "")
6   (PROGRAM "AQFPTX")
7   (VERSION "1.3")
8   (DIVIDER /)
9   (PROCESS "mit")
10  (TEMPERATURE 1:2:4)
11  (TIMESCALE 1ps)
12
13  (CELL
14    (CELLTYPE "inv")
15    (INSTANCE *)
16    (DELAY
17      (ABSOLUTE
18        (COND xin
19          (IOPATH xin q (17.36))
20        )
21      )
22    )
23    (TIMINGCHECK
24      (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
25      (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
26      (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
27      (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
28
29    )
30  )
31
32  (CELL
33    (CELLTYPE "and2_nn")
34    (INSTANCE *)
35    (DELAY
36      (ABSOLUTE
37        (COND xin
38          (IOPATH xin q (17.36))
39        )
40      )
41    )
42    (TIMINGCHECK
43      (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
44      (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
45      (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
46      (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
47      (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
48      (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
49      (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
50      (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
51
52    )
53  )
54
55  (CELL

```

```

56     (CELLTYPE "and2_np")
57     (INSTANCE *)
58     (DELAY
59       (ABSOLUTE
60         (COND xin
61           (IOPATH xin q (17.36))
62         )
63       )
64     )
65   (TIMINGCHECK
66     (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
67     (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
68     (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
69     (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
70     (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
71     (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
72     (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
73     (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
74   )
75 )
76
77 (CELL
78   (CELLTYPE "and2_pn")
79   (INSTANCE *)
80   (DELAY
81     (ABSOLUTE
82       (COND xin
83         (IOPATH xin q (17.36))
84       )
85     )
86   )
87   (TIMINGCHECK
88     (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
89     (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
90     (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
91     (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
92     (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
93     (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
94     (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
95     (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
96   )
97 )
98
99 (CELL
100   (CELLTYPE "and2_pp")
101   (INSTANCE *)
102   (DELAY
103     (ABSOLUTE
104       (COND xin
105         (IOPATH xin q (17.36))
106       )
107     )
108   )
109   (TIMINGCHECK
110     (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
111     (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
112     (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
113     (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
114     (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
115     (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
116     (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
117     (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
118   )
119 )
120
121 (CELL
122   (CELLTYPE "bfr")
123
124
125

```

```

126     (INSTANCE *)
127     (DELAY
128         (ABSOLUTE
129             (COND xin
130                 (IOPATH xin q (17.36))
131             )
132         )
133     )
134     (TIMINGCHECK
135         (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
136         (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
137         (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
138         (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
139     )
140   )
141 )
142
143 (CELL
144   (CELLTYPE "maj3_nnn")
145   (INSTANCE *)
146   (DELAY
147       (ABSOLUTE
148           (COND xin
149               (IOPATH xin q (17.36))
150           )
151       )
152   )
153   (TIMINGCHECK
154       (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
155       (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
156       (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
157       (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
158       (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
159       (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
160       (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
161       (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
162       (SETUP (COND c (posedge c)) (posedge gatex) (-13.00))
163       (SETUP (COND not_c (negedge c)) (posedge gatex) (-9.45))
164       (SETUP (posedge gatex) (COND c (negedge c)) (13.60))
165       (SETUP (posedge gatex) (COND not_c (posedge c)) (13.40))
166   )
167 )
168
169 (CELL
170   (CELLTYPE "maj3_nnp")
171   (INSTANCE *)
172   (DELAY
173       (ABSOLUTE
174           (COND xin
175               (IOPATH xin q (17.36))
176           )
177       )
178   )
179   (TIMINGCHECK
180       (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
181       (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
182       (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
183       (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
184       (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
185       (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
186       (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
187       (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
188       (SETUP (COND c (posedge c)) (posedge gatex) (-13.00))
189       (SETUP (COND not_c (negedge c)) (posedge gatex) (-9.45))
190       (SETUP (posedge gatex) (COND c (negedge c)) (13.60))
191       (SETUP (posedge gatex) (COND not_c (posedge c)) (13.40))
192   )
193 )
194
195 (CELL

```

```

196      (CELLTYPE "maj3_npn")
197      (INSTANCE *)
198      (DELAY
199          (ABSOLUTE
200              (COND xin
201                  (IOPATH xin q (17.36))
202              )
203          )
204      )
205      (TIMINGCHECK
206          (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
207          (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
208          (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
209          (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
210          (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
211          (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
212          (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
213          (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
214          (SETUP (COND c (posedge c)) (posedge gatex) (-13.00))
215          (SETUP (COND not_c (negedge c)) (posedge gatex) (-9.45))
216          (SETUP (posedge gatex) (COND c (negedge c)) (13.60))
217          (SETUP (posedge gatex) (COND not_c (posedge c)) (13.40))
218      )
219  )
220
221  (CELL
222      (CELLTYPE "maj3_npp")
223      (INSTANCE *)
224      (DELAY
225          (ABSOLUTE
226              (COND xin
227                  (IOPATH xin q (17.36))
228              )
229          )
230      )
231      (TIMINGCHECK
232          (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
233          (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
234          (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
235          (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
236          (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
237          (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
238          (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
239          (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
240          (SETUP (COND c (posedge c)) (posedge gatex) (-13.00))
241          (SETUP (COND not_c (negedge c)) (posedge gatex) (-9.45))
242          (SETUP (posedge gatex) (COND c (negedge c)) (13.60))
243          (SETUP (posedge gatex) (COND not_c (posedge c)) (13.40))
244      )
245  )
246
247  (CELL
248      (CELLTYPE "maj3_pnn")
249      (INSTANCE *)
250      (DELAY
251          (ABSOLUTE
252              (COND xin
253                  (IOPATH xin q (17.36))
254              )
255          )
256      )
257  )
258  (TIMINGCHECK
259          (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
260          (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
261          (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
262          (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
263          (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
264          (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
265          (SETUP (posedge gatex) (COND b (negedge b)) (13.60))

```

```

266      (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
267      (SETUP (COND c (posedge c)) (posedge gatex) (-13.00))
268      (SETUP (COND not_c (negedge c)) (posedge gatex) (-9.45))
269      (SETUP (posedge gatex) (COND c (negedge c)) (13.60))
270      (SETUP (posedge gatex) (COND not_c (posedge c)) (13.40))
271    )
272  )
273
274  (CELL
275    (CELLTYPE "maj3_pnp")
276    (INSTANCE *)
277    (DELAY
278      (ABSOLUTE
279        (COND xin
280          (IOPATH xin q (17.36))
281        )
282      )
283    )
284    (TIMINGCHECK
285      (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
286      (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
287      (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
288      (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
289      (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
290      (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
291      (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
292      (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
293      (SETUP (COND c (posedge c)) (posedge gatex) (-13.00))
294      (SETUP (COND not_c (negedge c)) (posedge gatex) (-9.45))
295      (SETUP (posedge gatex) (COND c (negedge c)) (13.60))
296      (SETUP (posedge gatex) (COND not_c (posedge c)) (13.40))
297    )
298  )
299
300  (CELL
301    (CELLTYPE "maj3_ppn")
302    (INSTANCE *)
303    (DELAY
304      (ABSOLUTE
305        (COND xin
306          (IOPATH xin q (17.36))
307        )
308      )
309    )
310    (TIMINGCHECK
311      (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
312      (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
313      (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
314      (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
315      (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
316      (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
317      (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
318      (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
319      (SETUP (COND c (posedge c)) (posedge gatex) (-13.00))
320      (SETUP (COND not_c (negedge c)) (posedge gatex) (-9.45))
321      (SETUP (posedge gatex) (COND c (negedge c)) (13.60))
322      (SETUP (posedge gatex) (COND not_c (posedge c)) (13.40))
323    )
324  )
325
326  (CELL
327    (CELLTYPE "maj3_ppp")
328    (INSTANCE *)
329    (DELAY
330      (ABSOLUTE
331        (COND xin
332          (IOPATH xin q (17.36))
333        )
334      )
335    )

```

```

336     (TIMINGCHECK
337         (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
338         (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
339         (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
340         (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
341         (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
342         (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
343         (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
344         (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
345         (SETUP (COND c (posedge c)) (posedge gatex) (-13.00))
346         (SETUP (COND not_c (negedge c)) (posedge gatex) (-9.45))
347         (SETUP (posedge gatex) (COND c (negedge c)) (13.60))
348         (SETUP (posedge gatex) (COND not_c (posedge c)) (13.40))
349     )
350   )
351
352 (CELL
353     (CELLTYPE "maj5_ppppp")
354     (INSTANCE *)
355     (DELAY
356       (ABSOLUTE
357         (COND xin
358           (IOPATH xin q (17.36))
359         )
360       )
361     )
362     (TIMINGCHECK
363         (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
364         (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
365         (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
366         (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
367         (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
368         (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
369         (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
370         (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
371         (SETUP (COND c (posedge c)) (posedge gatex) (-13.00))
372         (SETUP (COND not_c (negedge c)) (posedge gatex) (-9.45))
373         (SETUP (posedge gatex) (COND c (negedge c)) (13.60))
374         (SETUP (posedge gatex) (COND not_c (posedge c)) (13.40))
375         (SETUP (COND d (posedge d)) (posedge gatex) (-13.00))
376         (SETUP (COND not_d (negedge d)) (posedge gatex) (-9.45))
377         (SETUP (posedge gatex) (COND d (negedge d)) (13.60))
378         (SETUP (posedge gatex) (COND not_d (posedge d)) (13.40))
379         (SETUP (COND e (posedge e)) (posedge gatex) (-13.00))
380         (SETUP (COND not_e (negedge e)) (posedge gatex) (-9.45))
381         (SETUP (posedge gatex) (COND e (negedge e)) (13.60))
382         (SETUP (posedge gatex) (COND not_e (posedge e)) (13.40))
383     )
384   )
385
386 (CELL
387     (CELLTYPE "qfp1")
388     (INSTANCE *)
389     (DELAY
390       (ABSOLUTE
391         (COND xin
392           (IOPATH xin q (17.36))
393         )
394       )
395     )
396     (TIMINGCHECK
397         (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
398         (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
399         (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
400         (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
401         (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
402         (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
403         (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
404         (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
405     )

```

```

406    )
407
408  (CELL
409    (CELLTYPE "or2_nn")
410    (INSTANCE *)
411    (DELAY
412      (ABSOLUTE
413        (COND xin
414          (IOPATH xin q (17.36))
415        )
416      )
417    )
418    (TIMINGCHECK
419      (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
420      (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
421      (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
422      (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
423      (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
424      (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
425      (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
426      (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
427    )
428  )
429
430
431  (CELL
432    (CELLTYPE "or2_np")
433    (INSTANCE *)
434    (DELAY
435      (ABSOLUTE
436        (COND xin
437          (IOPATH xin q (17.36))
438        )
439      )
440    )
441    (TIMINGCHECK
442      (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
443      (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
444      (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
445      (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
446      (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
447      (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
448      (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
449      (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
450    )
451  )
452
453
454  (CELL
455    (CELLTYPE "or2_pn")
456    (INSTANCE *)
457    (DELAY
458      (ABSOLUTE
459        (COND xin
460          (IOPATH xin q (17.36))
461        )
462      )
463    )
464    (TIMINGCHECK
465      (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
466      (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
467      (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
468      (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
469      (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
470      (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
471      (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
472      (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
473    )
474  )
475

```

```

476
477 (CELL
478   (CELLTYPE "or2_pp")
479   (INSTANCE *)
480   (DELAY
481     (ABSOLUTE
482       (COND xin
483         (IOPATH xin q (17.36))
484       )
485     )
486   )
487   (TIMINGCHECK
488     (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
489     (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
490     (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
491     (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
492     (SETUP (COND b (posedge b)) (posedge gatex) (-13.00))
493     (SETUP (COND not_b (negedge b)) (posedge gatex) (-9.45))
494     (SETUP (posedge gatex) (COND b (negedge b)) (13.60))
495     (SETUP (posedge gatex) (COND not_b (posedge b)) (13.40))
496   )
497 )
498
499 (CELL
500   (CELLTYPE "spl2")
501   (INSTANCE *)
502   (DELAY
503     (ABSOLUTE
504       (COND xin
505         (IOPATH xin q0 (17.36))
506       )
507       (COND xin
508         (IOPATH xin q1 (17.36))
509       )
510     )
511   )
512   (TIMINGCHECK
513     (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
514     (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
515     (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
516     (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
517   )
518 )
519
520 )
521
522 (CELL
523   (CELLTYPE "spl3")
524   (INSTANCE *)
525   (DELAY
526     (ABSOLUTE
527       (COND xin
528         (IOPATH xin q0 (17.36))
529       )
530       (COND xin
531         (IOPATH xin q1 (17.36))
532       )
533       (COND xin
534         (IOPATH xin q2 (17.36))
535       )
536     )
537   )
538   (TIMINGCHECK
539     (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
540     (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
541     (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
542     (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
543   )
544 )
545 )

```

```
546  (CELL
547    (CELLTYPE "spl4")
548    (INSTANCE *)
549    (DELAY
550      (ABSOLUTE
551        (COND xin
552          (IOPATH xin q0 (17.36))
553        )
554        (COND xin
555          (IOPATH xin q1 (17.36))
556        )
557        (COND xin
558          (IOPATH xin q2 (17.36))
559        )
560        (COND xin
561          (IOPATH xin q3 (17.36))
562        )
563      )
564    )
565  )
566  (TIMINGCHECK
567    (SETUP (COND a (posedge a)) (posedge gatex) (-13.00))
568    (SETUP (COND not_a (negedge a)) (posedge gatex) (-9.45))
569    (SETUP (posedge gatex) (COND a (negedge a)) (13.60))
570    (SETUP (posedge gatex) (COND not_a (posedge a)) (13.40))
571  )
572 )
573 )
574 )
```

**Listing 2.27:** SDF file included in the library.

## **Part II**

# **RSFQ Logic**

# 3. Introduction and Setup

## 3.1 Introduction

This RSFQ cell library is developed under the IARPA SuperTools/ColdFlux contract via the U.S. Army Research Office grant W911NF-17-1-0120. The aim is to create a generic and open-source cell library with RSFQ logic [9] as part of the IARPA SuperTools Program[10], [11]. The cell library is continually updated and the latest version of the library can always be found at: <https://github.com/sunmagnetics/RSFQlib>. The RSFQ cell library on GitHub does not include the layout files as these files include Government-furnished information (GFI).

The free and open-source tools *XIC* [12], *JoSIM* [13], [14], *JoSIM-tools* [15], *KLayout* and *TimEx* [16], [17] is used to develop and test the RSFQ cells. The circuit schematics are drawn using *XIC*. *JoSIM* is used as the SPICE engine for simulating the cells, while *JoSIM-tools* is used for operating margin analysis as well as cell parameter optimization. *KLayout* is used to construct the cell layouts. *TimEx* is used to extract the characteristics of the cell to generate the Mealy Finite State Machine diagram and Verilog files. Additionally, *InductEx* [3], [18] is used for impedance extraction during cell layout design. A free version of *InductEx* is available, but has limited capacity.

The RSFQ cell library is currently designed to only be connected using Passive Transmission Lines (PTLs). The cells are designed with integrated PTL transmitters and receivers to minimize complexity and surface area required on a chip. Separate PTL transmitters and receivers are therefore no longer necessary when connecting the cells to PTLs. To indicate the integration of PTL transmitters and receivers within a cell, the letter ‘T’ is added at the end of a cell name, for example the DFF with integrated PTL transmitters and receivers will be referred to as DFFT.

The following core cells are included in the RSFQ cell library:

- Interconnects: JTLT, SPLITT, MERGET, PTLTX and PTLRX.
- Logic cells: AND2T, OR2T, XORT and NOTT.
- Buffers: DFFT, NDROT, BUFF and BUFFT.
- Interfacing cells: DCSFQ, DCSFQ-PTLTX, PTLRX-SFQDC and SFQDC.

More complex functions can be constructed through connecting several core cells. Versions of each cell without integrated PTL transmitters and receivers are also in

development. The cells are currently optimized to run at a maximum clock frequency of 50 GHz.

Each delivered cell is documented in 5 parts:

1. **Schematic:** The schematic of a cell is constructed using *Xic* and is delivered in the native *Xic* format.
2. **Layout:**
  - (a) The physical layout of the cells can be constructed using *Xic* or *KLayout* and is delivered in standard GDSII format.
  - (b) The *InductEx* extraction is also included.
3. **Analog model:**
  - (a) **Netlist:** The netlist presents the device-level construction of a circuit. The netlist can be generated and adapted from the schematic file using *Xic* or can be constructed by hand.
  - (b) **Pin list:** The pin labels and function of each pin is listed.
  - (c) **Simulation results:** JoSIM is used for all circuit simulations.
4. **Digital model:**
  - (a) **Verilog model:** The behavior-level model of a cell with timing specifications included within the model. All verilog models are extracted using *TimEx* and is delivered in standard HDL Verilog format.
  - (b) **Simulation results:** The digital simulation testbench is generated through *TimEx* and is run using *Icarus Verilog* and wave viewer *GTKWave*. Each edge event indicated an SFQ pulse.
  - (c) **Mealy finite state machine diagram:** The state machine diagram is extracted using *TimEx* and is delivered in standard PDF format.
5. **Power consumption:** The power consumption of each cell is calculated in terms of static and dynamic power consumption. Following [19], dynamic power consumption can be calculated as  $P_d = f\Phi_0 I_c$  and static power consumption can be calculated as  $P_s = I_b V_b$ .

## 3.2 Setup

The latest version of the RSFQ cell library can be found at: <https://github.com/sunmagnetics/RSFQlib>. The RSFQ cell library is simulated and tested using several free and/or open-source tools:

- *Xic* is part of *XicTools* and can be found at <http://www.wrcad.com/xic.html>.
- *JoSIM* can be found at <https://github.com/JoeyDelp/JoSIM/>.
- *JoSIM-tools* can be found at <https://github.com/pleroux0/josim-tools>.
- *TimEx* can be found at <https://github.com/sunmagnetics/TimEx>.
- *KLayout* can be found at <https://www.klayout.de/>.
- *InductEx* can be found at <https://www.inductex.info>.
- *Icarus Verilog* can be found at <http://iverilog.icarus.com/>.
- *GTKWave* can be found at <http://gtkwave.sourceforge.net/>.

No additional setup is required to use the RSFQ cell library.

## 3.3 License

The generic RSFQ cell library, excluding the cell layouts, is free to distribute and/or modify under the terms of the MIT license.

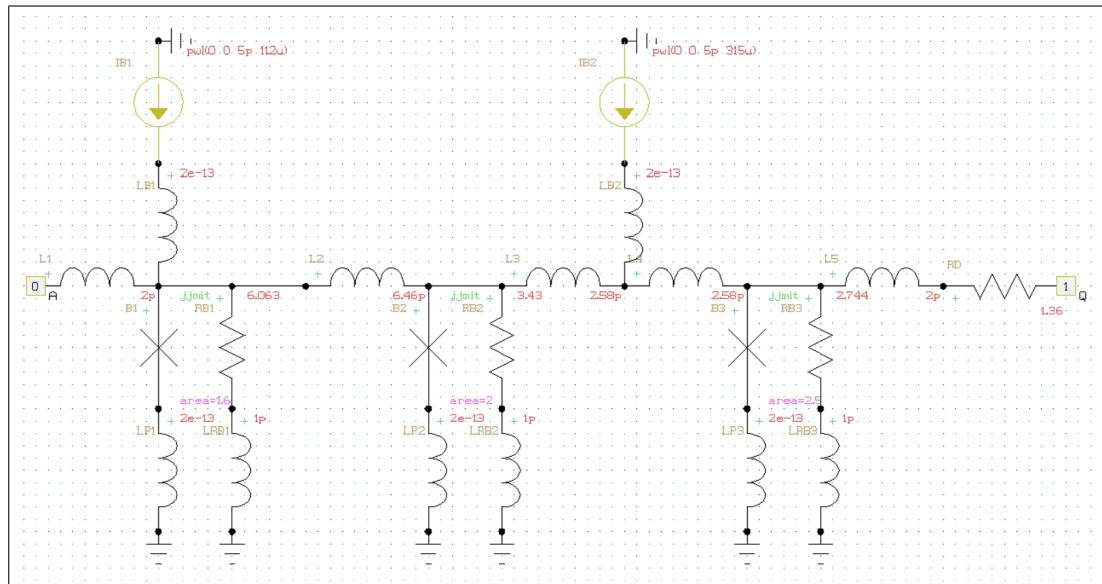
## 4. RSFQ Cell Library

### 4.1 Interconnects

#### 4.1.1 JTLT

The JTLT, Josephson transmission line, cell is commonly used to reestablish and propagate RSFQ pulses when long PTL connections are required. The cell has integrated PTL transmitters and receivers and is meant to connect directly to a PTL.

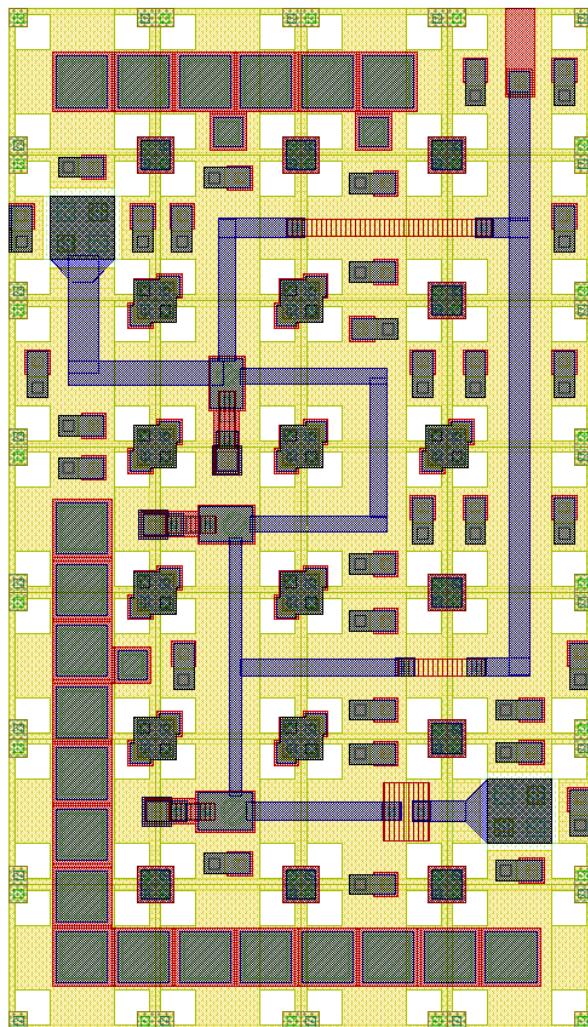
#### Schematic



**Figure 4.1:** Schematic of RSFQ JTLT.

## Layout

The physical layout for the RSFQ JTLT is shown in Fig. 4.2 and the resulting InductEx extraction is shown in Listing 4.1. The layout height is  $70 \mu m$  and the width is  $40 \mu m$ .



**Figure 4.2:** RSFQ JTLT Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_JTLT_v1p5.GDS -n LSmitll_JTLT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_JTLT_v1p5_idx.cir read. Totals: L = 10, k = 0, P = 7.
7 | Total fundamental loops identified in netlist = 6
8 | Using TetraHenry with analytical integration.
9 | 1188 structures read. Reduced 1188 objects to 1118 polygons and 4 terminals.
10 | Top level structure is "LSMITLL_JTLT_V1P5".
11 | GDS file LSmitll_JTLT_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 | Object in layer I5 moved to TERM layer. (Pj1)
13 | Object in layer I5 moved to TERM layer. (Pj2)
14 | Object in layer I5 moved to TERM layer. (Pj3)
15 | Terminal blocks = 7; Labels = 7; Extracted Ports = 7
16 |
17 | Port           Positive terminal     Negative terminal
18 | P1             M6, line along x;  M4, same as "+" terminal.
19 | P2             M6, polygon;       M4, same as "+" terminal.
20 | PB1            M6, polygon;       M4, same as "+" terminal.
21 | PB2            M6, polygon;       M4, same as "+" terminal.
22 | J1             M6, polygon;       M5, same as "+" terminal.
23 | J2             M6, polygon;       M5, same as "+" terminal.
24 | J3             M6, polygon;       M5, same as "+" terminal.
25 |
26 | SVD info: Condition nr. = 5.061; unknowns = 20; rank = 20.
27 |
28 | Impedance      Inductance [H]      Resistance [Ohm]    AbsDiff      PercDiff
29 | Name   Design   Extracted   Design   Extracted   (L only)   (L only)
30 | L1     --        2.89322E-12 --        --        +2.8932E-12 --%
31 | L2     6.46E-12  6.4667E-12 --        --        +6.7015E-15 +0.10374%
32 | L3     2.58E-12  2.57146E-12 --        --        -8.5375E-15 -0.33091%
33 | L4     2.58E-12  2.56823E-12 --        --        -1.1774E-14 -0.45635%
34 | L5     --        2.39515E-12 --        --        +2.3951E-12 --%
35 | LB1    --        3.21204E-12 --        --        +3.212E-12 --%
36 | LB2    --        2.8367E-12 --        --        +2.8367E-12 --%
37 | LP1    --        5.39345E-13 --        --        +5.3934E-13 --%
38 | LP2    --        5.44485E-13 --        --        +5.4448E-13 --%
39 | LP3    --        5.08968E-13 --        --        +5.0897E-13 --%
40 |
41 | Ports   Design   Extracted   AbsDiff   PercDiff
42 | J1      0.00016  0.00017055
43 | J2      0.0002   0.00020853
44 | J3      0.00025  0.00025893
45 |
46 | Error bound on extracted values: 0.792036%
47 |
48 | Deallocating memory.
49 | Cycles found in 0.027 seconds.
50 | SVD solution in 0.014 seconds.
51 | Job finished in 113.946 seconds.

```

**Listing 4.1:** RSFQ JTLT InductEx extraction.

## Analog model

```

1  * Author: L. Schindler
2  * Version: 1.5.1
3  * Last modification date: 18 June 2020
4  * Last modification by: L. Schindler
5
6  *$Ports
7  .subckt LSMITLL_JTLL a q
8  .model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
9  .param Phi0=2.067833848E-15
10 .param B0=1
11 .param Ic0=0.0001
12 .param IcRs=100u*6.859904418
13 .param B0Rs=IcRs/Ic0*B0
14 .param Rsheet=2
15 .param Lsheet=1.13e-12
16 .param LP=0.2p
17 .param ICreceive=1.6
18 .param ICtrans=2.5
19 .param Lptl=2p
20 .param LB=2p
21 .param BiasCoef=0.7
22 .param RD=1.36
23 .param B1=ICreceive
24 .param B2=ICtrans/1.25
25 .param B3=ICtrans
26 .param IB1=B1*Ic0*BiasCoef
27 .param IB2=(B2+B3)*Ic0*BiasCoef
28 .param L1=Lptl
29 .param L2=Phi0/(2*B1*Ic0)
30 .param L3=(Phi0/(2*B2*Ic0))/2
31 .param L4=L3
32 .param L5=Lptl
33 .param LP1=LP
34 .param LP2=LP
35 .param LP3=LP
36 .param LB1=LB
37 .param LB2=LB
38 .param RB1=B0Rs/B1
39 .param RB2=B0Rs/B2
40 .param RB3=B0Rs/B3
41 .param LRB1=(RB1/Rsheet)*Lsheet+LP
42 .param LRB2=(RB2/Rsheet)*Lsheet+LP
43 .param LRB3=(RB3/Rsheet)*Lsheet+LP
44 B1      6      7      jjmit area=B1
45 B2      9      10     jjmit area=B2
46 B3      12     13     jjmit area=B3
47 IB1     0      18     pw1(0      0 5p IB1)
48 IB2     0      19     pw1(0      0 5p IB2)
49 L1      a      6      L1
50 L2      6      9      L2
51 L3      9      16     L3
52 L4      16     12     L4
53 L5      12     17     L5
54 LB1     6      18     LB1
55 LB2     16     19     LB2
56 LP1     0      7      LP1
57 LP2     0      10     LP2
58 LP3     0      13     LP3
59 LRB1    0      8      LRB1
60 LRB2    0      11     LRB2
61 LRB3    0      14     LRB3
62 RB1     8      6      RB1
63 RB2     11     9      RB2
64 RB3     14     12     RB3
65 RD      17     q      RD
66 .ends

```

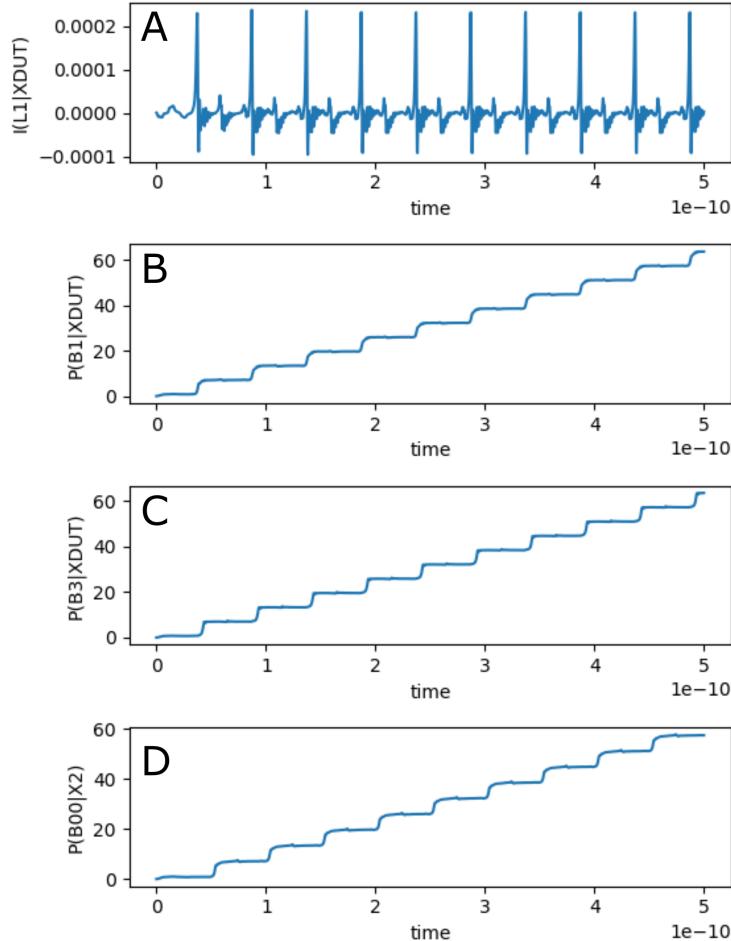
**Listing 4.2:** RSFQ JTLL JoSIM netlist.

**Table 4.1:** RSFQ JTLT pin list.

Pin	Description
<b>a</b>	Data input
<b>q</b>	Data output

The simulation results for the RSFQ JTLT using JoSIM is shown in Fig. 4.3. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q**, and
- (d) the phase over the input JJ of the load circuit connected via a PTL to the JTLT.

**Figure 4.3:** RSFQ JTLT analog simulation results.

## Digital model

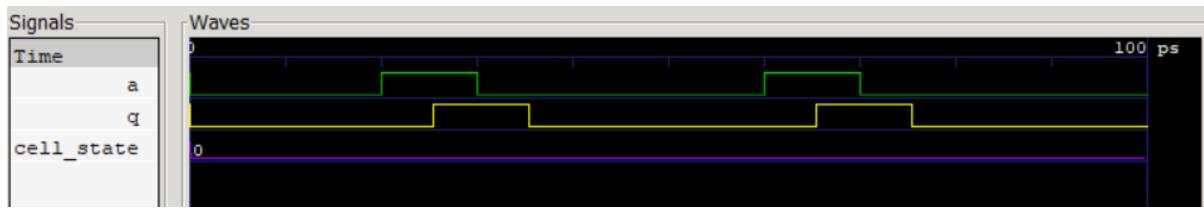
```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 //
9 `timescale 1ps/100fs
10 module LSmitll_JTLT_v1p5 (a, q);
11
12 input
13   a;
14
15 output
16   q;
17
18 reg
19   q;
20
21 real
22   delay_state0_a_q = 5.5,
23   ct_state0_a_a = 6.6;
24
25 reg
26   errorsignal_a;
27
28 integer
29   outfile,
30   cell_state; // internal state of the cell
31
32 initial
33 begin
34   errorsignal_a = 0;
35   cell_state = 0; // Startup state
36   q = 0; // All outputs start at 0
37 end
38
39 always @(posedge a or negedge a) // execute at positive and negative edges of input
40 begin
41   if ($time>4) // arbitrary steady-state time)
42     begin
43       if (errorsignal_a == 1'b1) // A critical timing is active for this input
44         begin
45           outfile = $fopen("errors.txt", "a");
46           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
47                         ↪ ", $stime);
48           $fclose(outfile);
49           q <= 1'bX; // Set all outputs to unknown
50         end
51       if (errorsignal_a == 0)
52         begin
53           case (cell_state)
54             0: begin
55               q <= #(delay_state0_a_q) !q;
56               errorsignal_a = 1; // Critical timing on this input; assign
57               ↪ immediately
58               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
59               ↪ after critical timing expires
60             end
61           endcase
62         end
63     end
64   end
65 endmodule

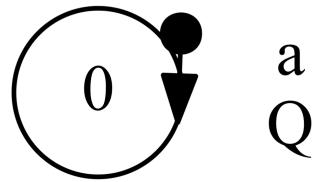
```

**Listing 4.3:** RSFQ JTLT verilog model.

The digital simulation results for the RSFQ JTLT is shown in Fig. 4.4 and the Mealy finite state machine diagram, extracted using *TimEx*, is shown in Fig. 4.5.



**Figure 4.4:** RSFQ JTLT digital simulation results.



**Figure 4.5:** RSFQ JTLT Mealy finite state machine diagram.

## Power Consumption

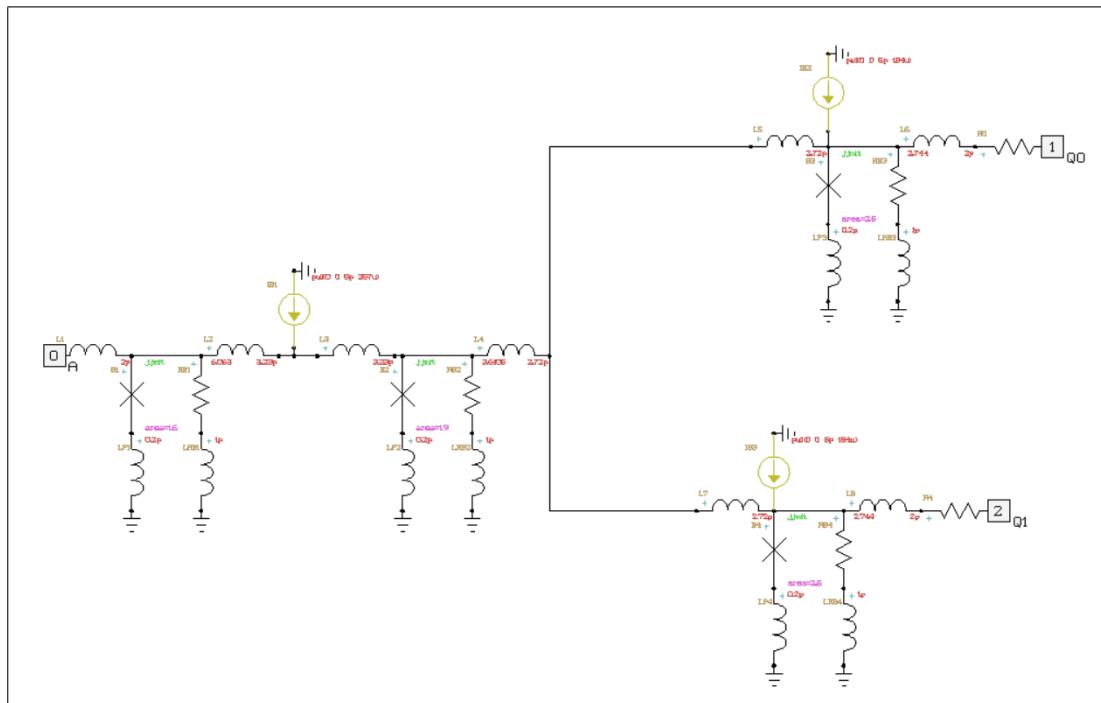
**Table 4.2:** RSFQ JTLT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	111	1.26
2	111	2.52
5	111	6.31
10	111	12.6
20	111	25.2
50	111	63.1

### 4.1.2 SPLITT

The SPLITT cell is used to split a single pulse signal line into two duplicate output pulse signal lines. The cell has integrated PTL transmitters and receivers and is meant to connect directly to a PTL.

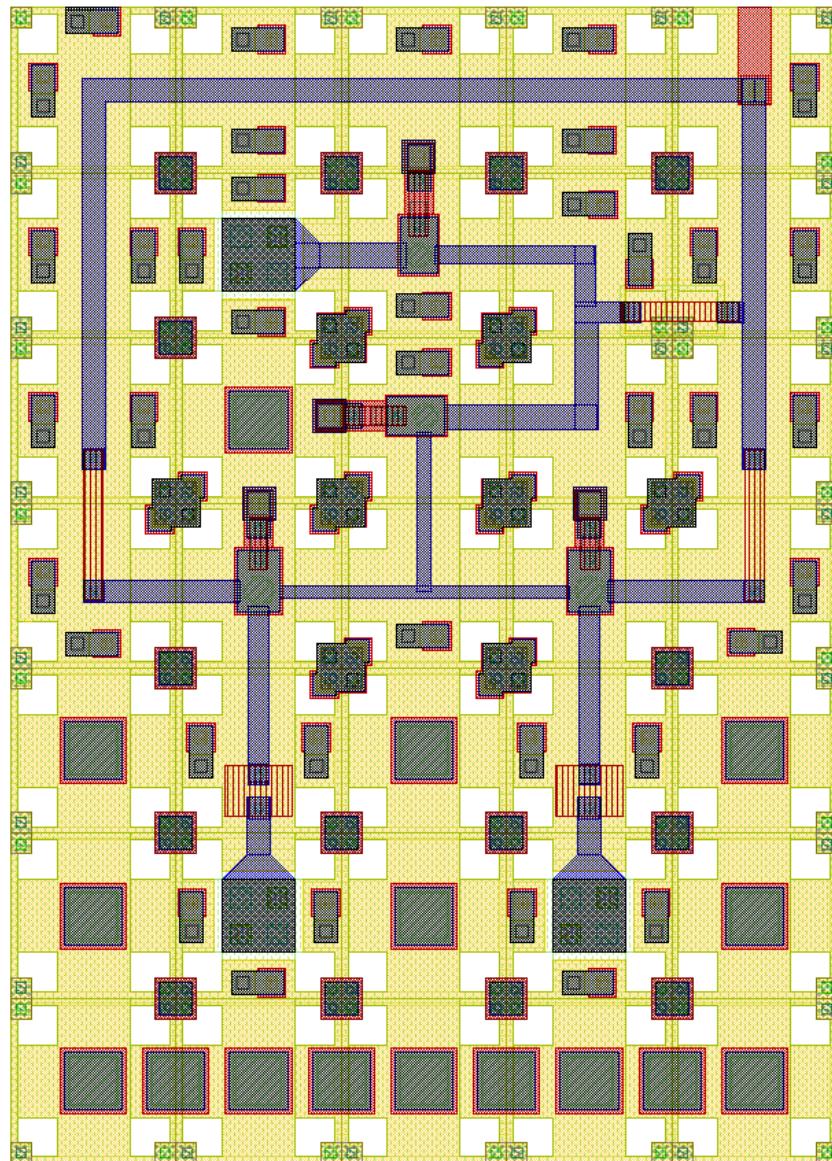
#### Schematic



**Figure 4.6:** Schematic of RSFQ SPLITT.

## Layout

The physical layout for the RSFQ SPLITT is shown in Fig. 4.7 and the resulting InductEx extraction is shown in Listing 4.4. The layout height is  $70 \mu\text{m}$  and the width is  $50 \mu\text{m}$ .



**Figure 4.7:** RSFQ SPLITT layout.

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_SPLITT_v1p5.gds -n LSmitll_SPLITT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_SPLITT_v1p5_idx.cir read. Totals: L = 15, k = 0, P = 10.
7 | Total fundamental loops identified in netlist = 9
8 | Using TetraHenry with analytical integration.
9 | 1379 structures read. Reduced 1379 objects to 1346 polygons and 6 terminals.
10 | Top level structure is "LSMITLL_SPLITT_V1P5".
11 | GDS file LSmitll_SPLITT_v1p5.gds read: db units in 1E-9 m, 0.001 units per user unit.
12 | Object in layer I5 moved to TERM layer. (Pj1)
13 | Object in layer I5 moved to TERM layer. (Pj2)
14 | Object in layer I5 moved to TERM layer. (Pj3)
15 | Object in layer I5 moved to TERM layer. (Pj4)
16 | Terminal blocks = 10; Labels = 10; Extracted Ports = 10
17 |
18 | Port          Positive terminal    Negative terminal
19 | P1            M6, line along y; M4, same as "+" terminal.
20 | P2            M6, line along x; M4, same as "+" terminal.
21 | P3            M6, line along x; M4, same as "+" terminal.
22 | PB1           M6, line along y; M4, same as "+" terminal.
23 | PB2           M6, polygon;      M4, same as "+" terminal.
24 | PB3           M6, polygon;      M4, same as "+" terminal.
25 | J1            M6, polygon;      M5, same as "+" terminal.
26 | J2            M6, polygon;      M5, same as "+" terminal.
27 | J3            M6, polygon;      M5, same as "+" terminal.
28 | J4            M6, polygon;      M5, same as "+" terminal.
29 |
30 | SVD info: Condition nr. = 8.562; unknowns = 30; rank = 30.
31 |
32 | Impedance     Inductance [H]       Resistance [Ohm]      AbsDiff      PercDiff
33 | Name          Design        Extracted      Design        Extracted      (L only)      (L only)
34 | L1            --           1.50149E-12  --           --           +1.5015E-12  --%
35 | L2            2.84E-12     2.82215E-12  --           --           -1.7855E-14  -0.62869%
36 | L3            2.84E-12     2.83155E-12  --           --           -8.4487E-15  -0.29749%
37 | L4            2.69E-12     2.68895E-12  --           --           -1.0457E-15  -0.038873%
38 | L5            2.69E-12     2.69743E-12  --           --           +7.4322E-15  +0.27629%
39 | L6            --           2.36538E-12  --           --           +2.3654E-12  --%
40 | L7            2.69E-12     2.69634E-12  --           --           +6.3413E-15  +0.23573%
41 | L8            --           2.36586E-12  --           --           +2.3659E-12  --%
42 | LP1           --           4.58145E-13  --           --           +4.5814E-13  --%
43 | LP2           --           5.30306E-13  --           --           +5.3031E-13  --%
44 | LP3           --           4.94587E-13  --           --           +4.9459E-13  --%
45 | LP4           --           4.93676E-13  --           --           +4.9368E-13  --%
46 | LB1           --           6.25411E-13  --           --           +6.2541E-13  --%
47 | LB2           --           2.15533E-12  --           --           +2.1553E-12  --%
48 | LB3           --           2.12844E-12  --           --           +2.1284E-12  --%
49 |
50 | Ports         Design        Extracted      AbsDiff      PercDiff
51 | J1            0.00016      0.00016855
52 | J2            0.000167     0.00017455
53 | J3            0.00025      0.00025893
54 | J4            0.00025      0.00025893
55 |
56 | Error bound on extracted values: 1.17944%
57 |
58 | Deallocating memory.
59 | Cycles found in 0.030 seconds.
60 | SVD solution in 0.013 seconds.
61 | Job finished in 150.310 seconds.

```

**Listing 4.4:** RSFQ SPLITT InductEx extraction.

## Analog model

```

1  * Author: L. Schindler
2  * Version: 1.5.1
3  * Last modification date: 18 June 2020
4  * Last modification by: L. Schindler
5
6  *$Ports
7  .subckt LSMITLL_SPLITT a q0 q1
8  .model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
9  .param Phi0=2.067833848E-15
10 .param B0=1
11 .param Ic0=0.0001
12 .param IcRs=100u*6.859904418
13 .param B0Rs=IcRs/Ic0*B0
14 .param Rsheet=2
15 .param Lsheet=1.13e-12
16 .param LP=0.2p
17 .param IC=1.9
18 .param ICreceive=1.6
19 .param ICtrans=2.5
20 .param Lptl=2p
21 .param BiasCoef=0.735
22 .param RD=1.36
23 .param B1=ICreceive
24 .param B2=IC
25 .param B3=ICtrans
26 .param B4=ICtrans
27 .param IB1=BiasCoef*(B1*Ic0+B2*Ic0)
28 .param IB2=BiasCoef*(B3*Ic0)
29 .param IB3=BiasCoef*(B4*Ic0)
30 .param L1=Lptl
31 .param L2=(Phi0/(2*B1*Ic0))/2
32 .param L3=(Phi0/(2*B1*Ic0))/2
33 .param L4=(Phi0/(2*B2*Ic0))/2
34 .param L5=(Phi0/(2*B2*Ic0))/2
35 .param L6=Lptl
36 .param L7=(Phi0/(2*B2*Ic0))/2
37 .param L8=Lptl
38 .param RB1=B0Rs/B1
39 .param RB2=B0Rs/B2
40 .param RB3=B0Rs/B3
41 .param RB4=B0Rs/B4
42 .param LRB1=(RB1/Rsheet)*Lsheet
43 .param LRB2=(RB2/Rsheet)*Lsheet
44 .param LRB3=(RB3/Rsheet)*Lsheet
45 .param LRB4=(RB4/Rsheet)*Lsheet
46 IB1 0 4 pwl(0 0 5p IB1)
47 IB2 0 8 pwl(0 0 5p IB2)
48 IB3 0 11 pwl(0 0 5p IB3)
49 B1 2 3 jjmit area=B1
50 B2 5 6 jjmit area=B2
51 B3 8 9 jjmit area=B3
52 B4 11 12 jjmit area=B4
53 L1 a 2 L1
54 L2 2 4 L2
55 L3 4 5 L3
56 L4 5 7 L4
57 L5 7 8 L5
58 L6 8 10 L6
59 L7 7 11 L7
60 L8 11 13 L8
61 LP1 3 0 0.2p
62 LP2 6 0 0.2p
63 LP3 9 0 0.2p
64 LP4 12 0 0.2p
65 RB1 2 102 RB1
66 LRB1 102 0 LRB1
67 RB2 5 105 RB2

```

```

68 | LRB2 105 0 LRB2
69 | RB3 8 108 RB3
70 | LRB3 108 0 LRB3
71 | RB4 11 111 RB4
72 | LRB4 111 0 LRB4
73 | RD1 13 q0 RD
74 | RD2 10 q1 RD
75 | .ends

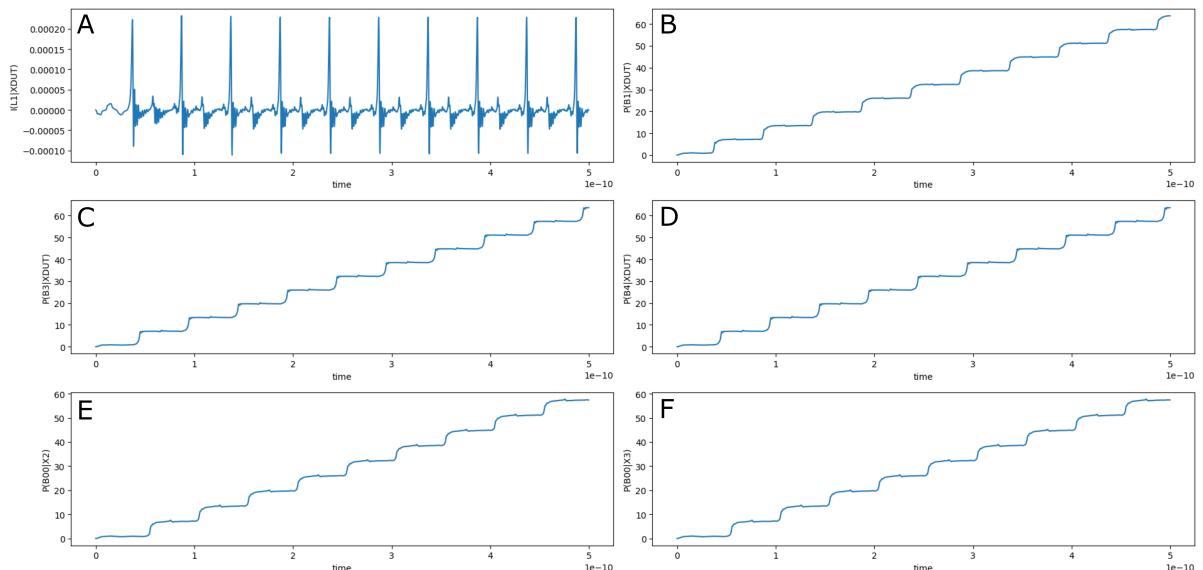
```

**Listing 4.5:** RSFQ SPLITT JoSIM netlist.**Table 4.3:** RSFQ SPLITT pin list.

Pin	Description
<b>a</b>	Data input
<b>q0</b>	Data output
<b>q1</b>	Data output

The JoSIM simulation results for the RSFQ SPLITT are shown in Fig. 4.8. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q0**,
- (d) the phase over the output JJ of pin **q1**,
- (e) the phase over the input JJ of the load cell connected to pin **q0** through a PTL, and
- (f) the phase over the input JJ of the load cell connected to pin **q1** through a PTL.

**Figure 4.8:** RSFQ SPLITT analog simulation results.

## Digital model

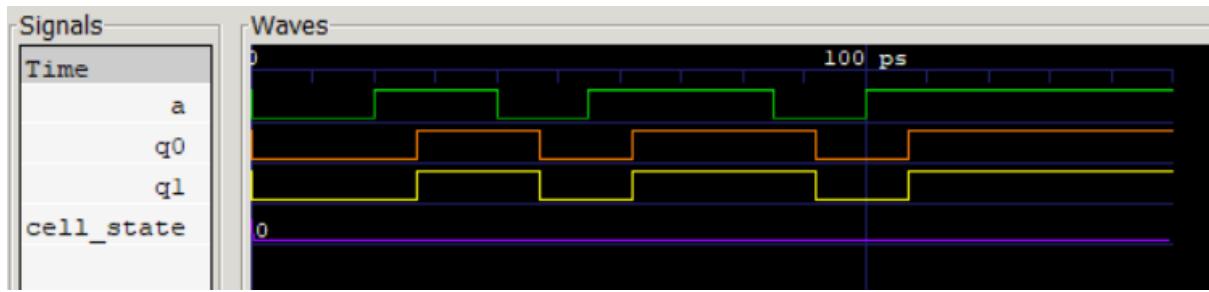
```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 //
9 'timescale 1ps/100fs
10 module LSmitll_SPLITT_v1p5 (a, q0, q1);
11
12 input
13   a;
14 output
15   q0, q1;
16 reg
17   q0, q1;
18 real
19   delay_state0_a_q0 = 7.0,
20   delay_state0_a_q1 = 7.0,
21   ct_state0_a_a = 10.3;
22
23 reg
24   errorsignal_a;
25
26 integer
27   outfile,
28   cell_state; // internal state of the cell
29
30 initial
31 begin
32   errorsignal_a = 0;
33   cell_state = 0; // Startup state
34   q0 = 0; // All outputs start at 0
35   q1 = 0; // All outputs start at 0
36 end
37
38 always @(posedge a or negedge a) // execute at positive and negative edges of input
39 begin
40   if ($time>4) // arbitrary steady-state time)
41     begin
42       if (errorsignal_a == 1'b1) // A critical timing is active for this input
43         begin
44           outfile = $fopen("errors.txt", "a");
45           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
46           ↪ ", $stime);
47           $fclose(outfile);
48           q0 <= 1'bX; // Set all outputs to unknown
49           q1 <= 1'bX; // Set all outputs to unknown
50         end
51       if (errorsignal_a == 0)
52         begin
53           case (cell_state)
54             0: begin
55               q0 <= #(delay_state0_a_q0) !q0;
56               q1 <= #(delay_state0_a_q1) !q1;
57               errorsignal_a = 1; // Critical timing on this input; assign
58               ↪ immediately
59               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
59               ↪ after critical timing expires
60             end
61           endcase
62         end
63     end
64   end
65 endmodule

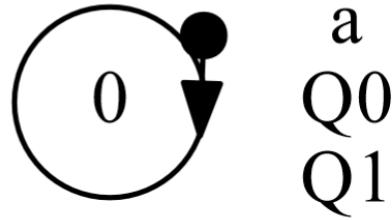
```

**Listing 4.6:** RSFQ SPLITT verilog model.

The digital simulation results for the RSFQ SPLITT is shown in Fig. 4.9 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.10.



**Figure 4.9:** RSFQ SPLITT digital simulation results.



**Figure 4.10:** RSFQ SPLITT Mealy finite state diagram.

## Power consumption

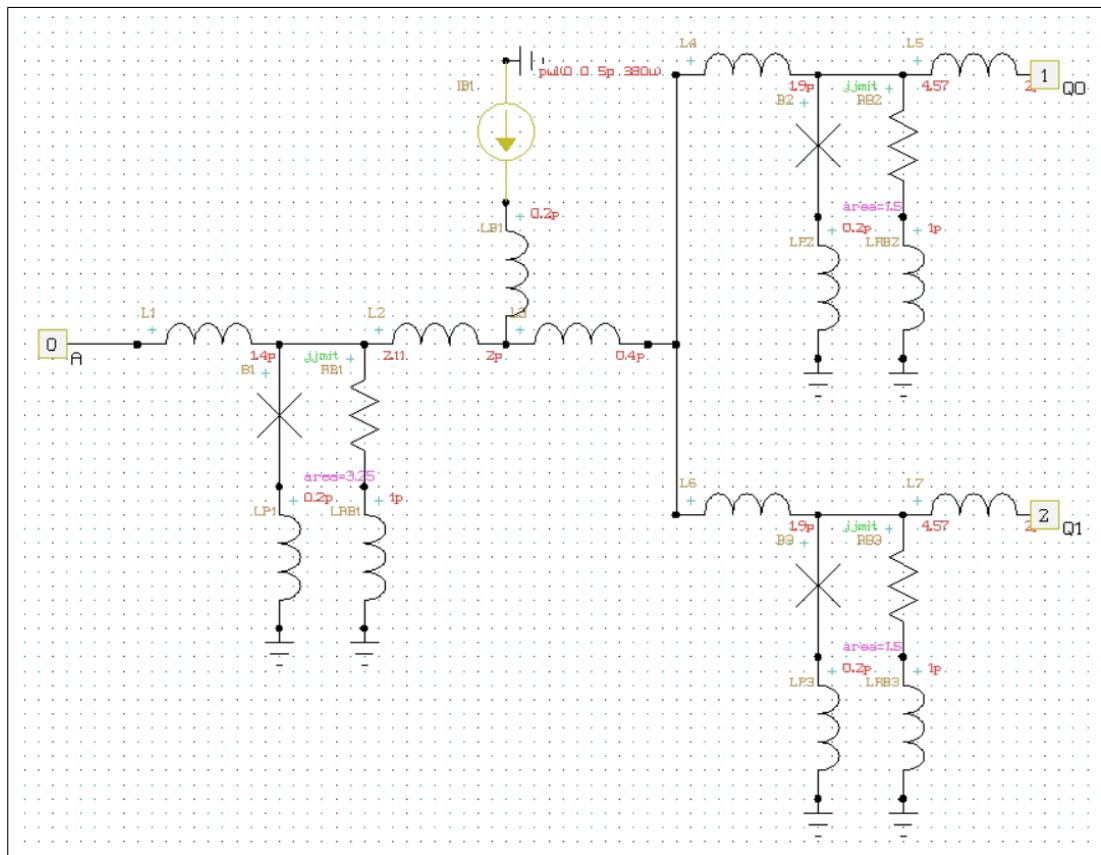
**Table 4.4:** RSFQ SPLITT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	162	1.76
2	162	3.52
5	162	8.79
10	162	17.6
20	162	35.2
50	162	87.9

### 4.1.3 CLKSPLT

The CLKSPLT cell is a splitter cell used for clock splitting. It is designed to have the same a-to-q delay as the CLKSPLTT, BUFF and BUFFT cell. The CLKSPLT does not have integrated PTL transmitters and receivers and connecting the cell directly to a PTL is not recommended.

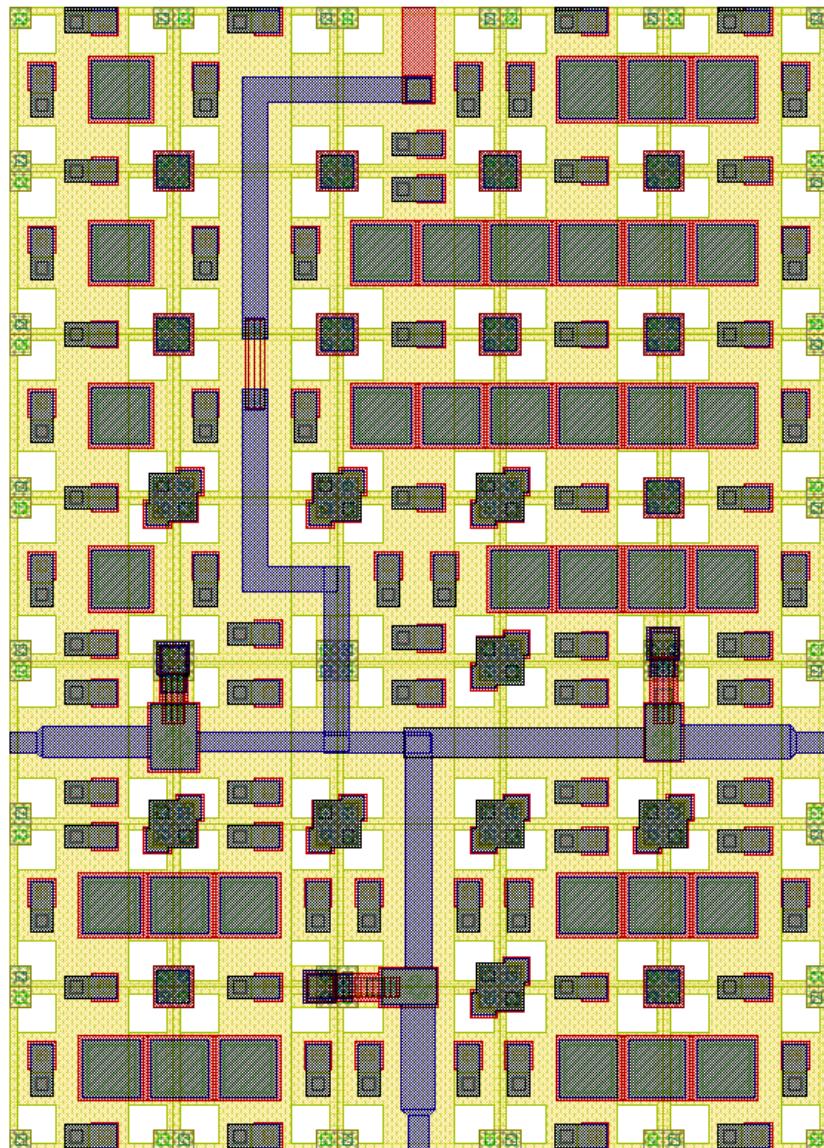
#### Schematic



**Figure 4.11:** Schematic of RSFQ CLKSPLT.

## Layout

The physical layout of the RSFQ CLKSPKT is shown in Fig. 4.12 and the resulting InductEx extraction is shown in Listing 4.7. The height of the layout is  $70 \mu m$  and the width is  $50 \mu m$ . If required, an additional and smaller layout can be made to minimize chip space for clock splitting.



**Figure 4.12:** RSFQ CLKSPKT layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_CLKSPLT_v1p5p1.GDS -n LSmitll_CLKSPLT_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_CLKSPLT_idx.cir read. Totals: L = 11, k = 0, P = 7.
7 | Total fundamental loops identified in netlist = 6
8 | Using TetraHenry with analytical integration.
9 | 1653 structures read. Reduced 1653 objects to 1519 polygons and 4 terminals.
10 | Top level structure is "LSMITLL_CLKSPLT_V1P5P1".
11 | GDS file LSmitll_CLKSPLT_v1p5p1.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 | Object in layer I5 moved to TERM layer. (Pj1)
13 | Object in layer I5 moved to TERM layer. (Pj2)
14 | Object in layer I5 moved to TERM layer. (Pj3)
15 | Terminal blocks = 7; Labels = 7; Extracted Ports = 7
16 |
17 | Port           Positive terminal     Negative terminal
18 | P1             M6, line along y;    M4, same as "+" terminal.
19 | P2             M6, line along y;    M4, same as "+" terminal.
20 | P3             M6, line along x;    M4, same as "+" terminal.
21 | PB1            M6, polygon;       M4, same as "+" terminal.
22 | J1             M6, polygon;       M5, same as "+" terminal.
23 | J2             M6, polygon;       M5, same as "+" terminal.
24 | J3             M6, polygon;       M5, same as "+" terminal.
25 |
26 | SVD info: Condition nr. = 7.934; unknowns = 22; rank = 22.
27 |
28 | Impedance      Inductance [H]      Resistance [Ohm]      AbsDiff      PercDiff
29 | Name   Design   Extracted   Design   Extracted   (L only)   (L only)
30 | L1     2E-12   2.00245E-12 --        --        +2.4493E-15 +0.12246%
31 | L2     2E-12   1.99792E-12 --        --        -2.0779E-15 -0.10389%
32 | L3     1E-12   1.00373E-12 --        --        +3.7267E-15 +0.37267%
33 | L4     2.3E-12  2.3219E-12 --        --        +2.1899E-14 +0.95214%
34 | L5     2E-12   1.98942E-12 --        --        -1.0584E-14 -0.5292%
35 | L6     2.3E-12  2.33197E-12 --        --        +3.1972E-14 +1.3901%
36 | L7     2E-12   1.98418E-12 --        --        -1.5819E-14 -0.79093%
37 | LP1    --      4.39941E-13 --        --        +4.3994E-13 --%
38 | LP2    --      5.03617E-13 --        --        +5.0362E-13 --%
39 | LP3    --      5.10561E-13 --        --        +5.1056E-13 --%
40 | LB1    --      4.67421E-12 --        --        +4.6742E-12 --%
41 |
42 | Ports   Design   Extracted   AbsDiff   PercDiff
43 | J1      0.000325  0.00033376
44 | J2      0.00015   0.00015829
45 | J3      0.00015   0.00015829
46 |
47 | Error bound on extracted values: 0.0925697%
48 |
49 | Deallocating memory.
50 | Cycles found in 0.027 seconds.
51 | SVD solution in 0.015 seconds.
52 | Job finished in 154.433 seconds.

```

**Listing 4.7:** RSFQ CLKSPKT InductEx extraction.

## Analog model

```

1 * Author: L. Schindler
2 * Version: 1.5.1
3 * Last modification date: 24 June 2020
4 * Last modification by: L. Schindler
5
6 *$Ports
7 .subckt LSMITLL_CLKSPLT a q0 q1
8 .model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
9 .param B0=1
10 .param Ic0=0.0001
11 .param IcRs=100u*6.859904418
12 .param B0Rs=IcRs/Ic0*B0
13 .param Rsheet=2
14 .param Lsheet=1.13e-12
15 .param B01rx1=1.01
16 .param B01tx1=1.70
17 .param B1=1.70
18 .param B2=1.21
19 .param IB01rx1=0.000135
20 .param IB01tx1=7.6e-05
21 .param IB1=0.000360
22 .param L01rx1=2.6757035519114777e-13
23 .param L02tx1=2.2253212527851025e-12
24 .param L1=1.5258529970572481e-12
25 .param L2=2.9153847294043574e-12
26 .param L3=4.813688043861165e-13
27 .param L4=1.2716425006912427e-12
28 .param L5=1.2572241510058017e-12
29 .param LRB01rx1=(RB01rx1/Rsheet)*Lsheet
30 .param LRB01tx1=(RB01tx1/Rsheet)*Lsheet
31 .param LRB1=(RB1/Rsheet)*Lsheet
32 .param LRB2=(RB2/Rsheet)*Lsheet
33 .param RB01rx1=B0Rs/B01rx1
34 .param RB01tx1=B0Rs/B01tx1
35 .param RB1=B0Rs/B1
36 .param RB2=B0Rs/B2
37 B01rx1 6 20 jjmit area=B01rx1
38 B01tx1 5 16 jjmit area=B01tx1
39 B01tx2 9 28 jjmit area=B01tx1
40 B1 7 22 jjmit area=B1
41 B2 4 14 jjmit area=B2
42 B3 8 25 jjmit area=B2
43 IB01rx1 0 12 pw1(0 0 5p IB01rx1)
44 IB01tx1 0 10 pw1(0 0 5p IB01tx1)
45 IB01tx2 0 27 pw1(0 0 5p IB01tx1)
46 IB1 0 13 pw1(0 0 5p IB1)
47 L01rx1 a 6 L01rx1
48 L02tx1 5 q0 L02tx1
49 L02tx2 9 q1 L02tx1
50 L1 6 7 L1
51 L2 7 18 L2
52 L3 18 19 L3
53 L4 4 19 L4
54 L5 4 5 L5
55 L6 19 8 L4
56 L7 8 9 L5
57 LP01rx1 20 0 0.34p
58 LP01tx1 16 0 0.05p
59 LP01tx2 28 0 0.05p
60 LP1 22 0 0.2p
61 LP2 14 0 0.2p
62 LP3 25 0 0.2p
63 LPR01rx1 12 6 0.2p
64 LPR01tx1 10 5 0.2p
65 LPR01tx2 9 27 0.2p
66 LPRIB1 13 18 0.2p
67 LRB01rx1 21 0 LRB01rx1

```

```
68 | LRB01tx1 17 0 LRB01tx1
69 | LRB01tx2 29 0 LRB01tx1
70 | LRB1 23 0 LRB1
71 | LRB2 15 0 LRB2
72 | LRB3 26 0 LRB2
73 | RB01rx1 6 21 RB01rx1
74 | RB01tx1 5 17 RB01tx1
75 | RB01tx2 9 29 RB01tx1
76 | RB1 7 23 RB1
77 | RB2 4 15 RB2
78 | RB3 8 26 RB2
79 | .ends
```

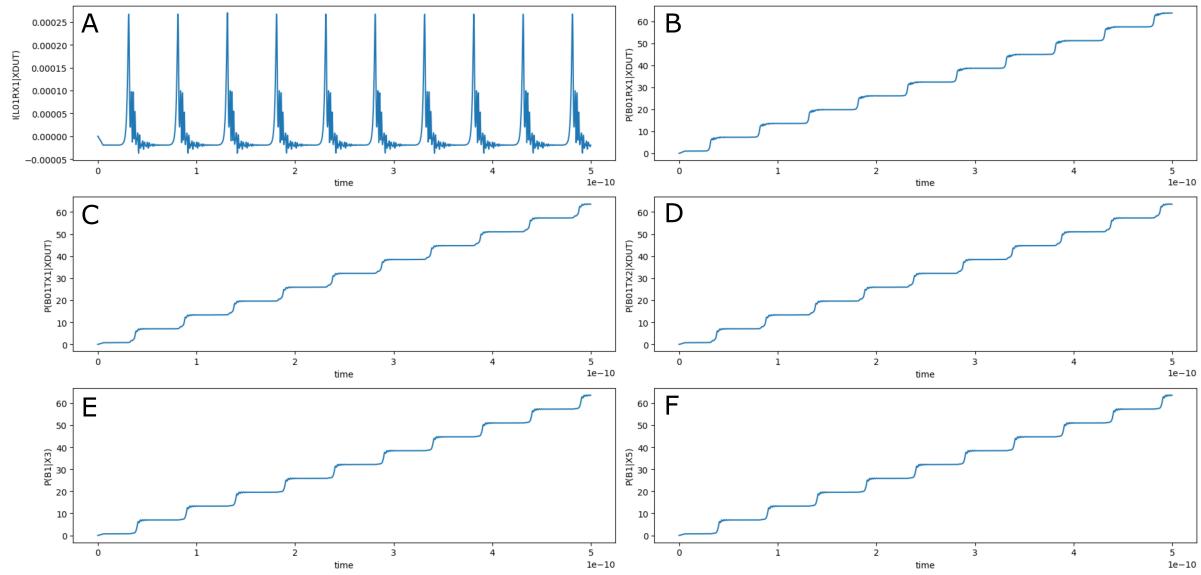
**Listing 4.8:** RSFQ CLKSPLT JoSIM netlist.

**Table 4.5:** RSFQ CLKSPLT pin list.

Pin	Description
a	Data input
q0	Data output
q1	Data output

The JoSIM simulation results for the RSFQ CLKSPLT are shown in Fig. 4.13. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q0**,
- (d) the phase over the output JJ of pin **q1**,
- (e) the phase over the input JJ of the load cell connected to pin **q0**, and
- (f) the phase over the input JJ of the load cell connected to pin **q1**.



**Figure 4.13:** RSFQ CLKSPLT analog simulation results.

## Digital model

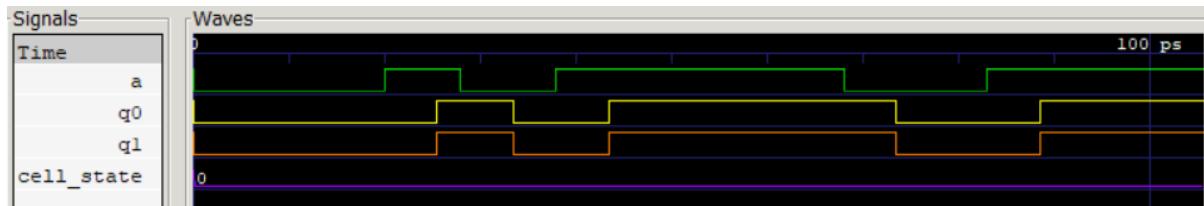
```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 // -----
9 `timescale 1ps/100fs
10 module LSmitll_CLKSPLT_v1p5 (a, q0, q1);
11
12 input
13   a;
14 output
15   q0, q1;
16 reg
17   q0, q1;
18
19 real
20   delay_state0_a_q0 = 5.5,
21   delay_state0_a_q1 = 5.5,
22   ct_state0_a_a = 3.5;
23 reg
24   errorsignal_a;
25
26 integer
27   outfile,
28   cell_state; // internal state of the cell
29
30 initial
31 begin
32   errorsignal_a = 0;
33   cell_state = 0; // Startup state
34   q0 = 0; // All outputs start at 0
35   q1 = 0; // All outputs start at 0
36 end
37
38 always @(posedge a or negedge a) // execute at positive and negative edges of input
39 begin
40   if ($time>4) // arbitrary steady-state time)
41     begin
42       if (errorsignal_a == 1'b1) // A critical timing is active for this input
43         begin
44           outfile = $fopen("errors.txt", "a");
45           $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n"
46           ↪ ", $stime);
47           $fclose(outfile);
48           q0 <= 1'bX; // Set all outputs to unknown
49           q1 <= 1'bX; // Set all outputs to unknown
50         end
51       if (errorsignal_a == 0)
52         begin
53           case (cell_state)
54             0: begin
55               q0 <= #(delay_state0_a_q0) !q0;
56               q1 <= #(delay_state0_a_q1) !q1;
57               errorsignal_a = 1; // Critical timing on this input; assign
58               ↪ immediately
59               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
59               ↪ after critical timing expires
60             end
61           endcase
62         end
63     end
64   end
65 endmodule

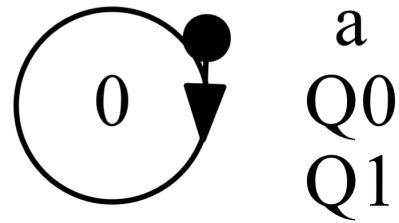
```

**Listing 4.9:** RSFQ CLKSPLT verilog model.

The digital simulation results for the RSFQ CLKSPLT is shown in Fig. 4.14 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.15.



**Figure 4.14:** RSFQ CLKSPLT digital simulation results.



**Figure 4.15:** RSFQ CLKSPLT Mealy finite state diagram.

## Power consumption

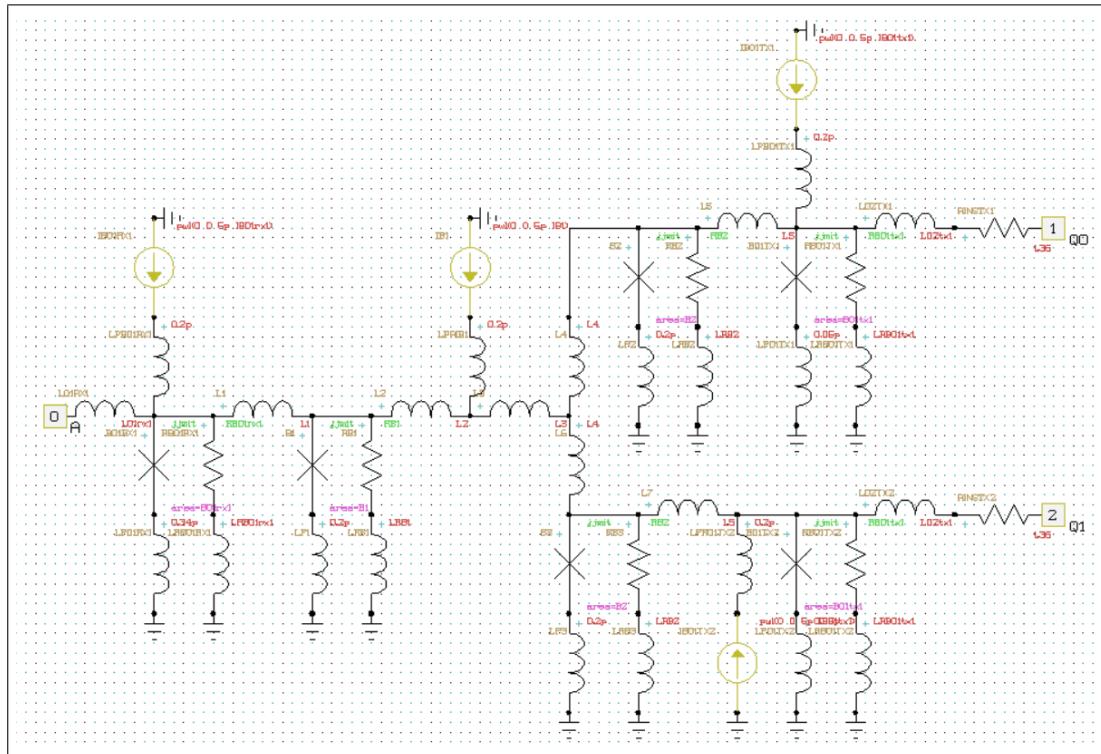
**Table 4.6:** RSFQ CLKSPLT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	168	1.76
2	168	3.53
5	168	8.82
10	168	17.6
20	168	35.3
50	168	88.2

#### 4.1.4 CLKSPLTT

The CLKSPLTT cell is a splitter cell used for clock splitting. It is designed to have the same a-to-q delay as the CLKSPLT, BUFF and BUFFT cell. The CLKSPLTT has integrated PTL transmitters and receivers is designed to be directly connected to a PTL.

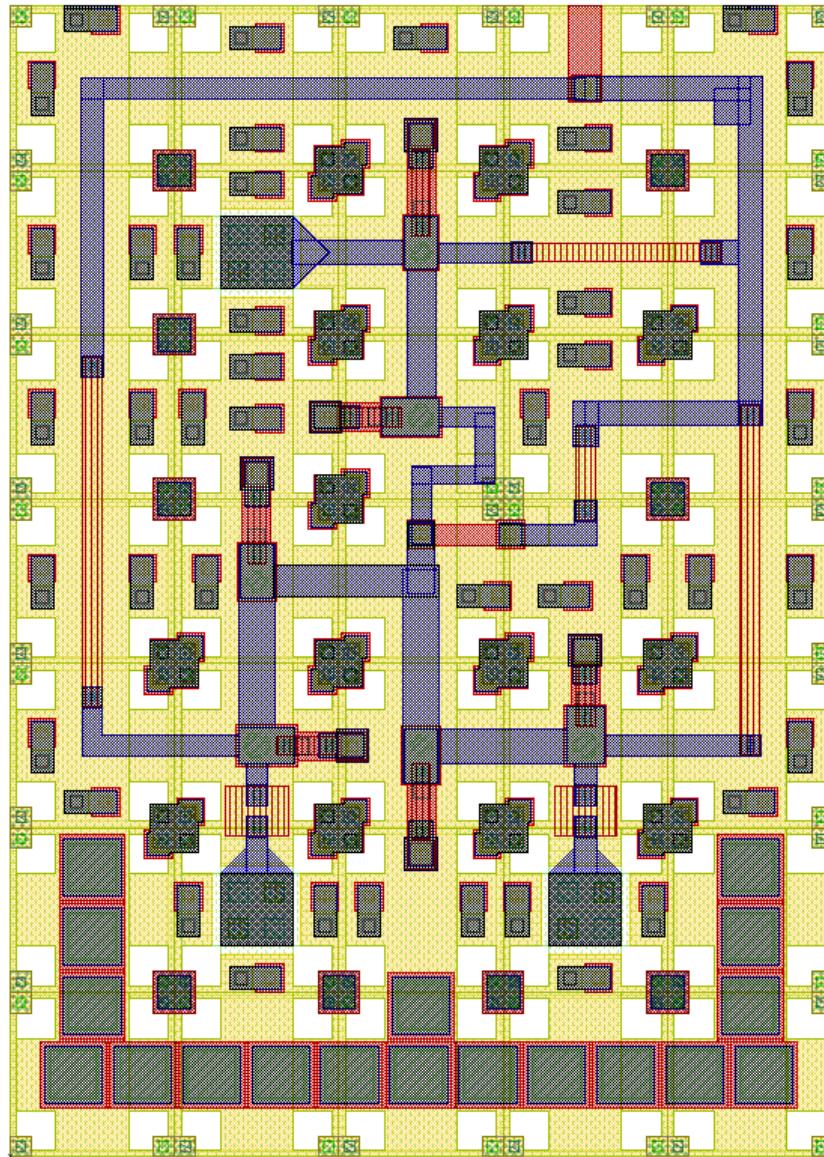
##### Schematic



**Figure 4.16:** Schematic of RSFQ CLKSPLTT.

## Layout

The physical layout of the RSFQ CLKSPPLTT is shown in Fig. 4.17 and the resulting InductEx extraction is shown in Listing 4.10. The height of the layout is  $70 \mu m$  and the width is  $50 \mu m$ .



**Figure 4.17:** RSFQ CLKSPPLTT layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_CLKSPLTT_v1p5p1.GDS -n LSmitll_CLKSPLTT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_CLKSPLTT_v1p5_idx.cir read. Totals: L = 20, k = 0, P = 13.
7 | Total fundamental loops identified in netlist = 12
8 | Using TetraHenry with analytical integration.
9 | 1628 structures read. Reduced 1628 objects to 1472 polygons and 7 terminals.
10 | Top level structure is "LSMITLL_CLKSPLTT_V1P5P1".
11 | GDS file LSmitll_CLKSPLTT_v1p5p1.GDS read: db units in 1E-9 m, 0.001 units per user unit.

```

```

12 | Object in layer I5 moved to TERM layer. (Pj1)
13 | Object in layer I5 moved to TERM layer. (Pj2)
14 | Object in layer I5 moved to TERM layer. (Pj3)
15 | Object in layer I5 moved to TERM layer. (Pj4)
16 | Object in layer I5 moved to TERM layer. (Pj5)
17 | Object in layer I5 moved to TERM layer. (Pj6)
18 | Terminal blocks = 13; Labels = 13; Extracted Ports = 13
19 |
20 | Port           Positive terminal   Negative terminal
21 | P1            M6, line along y;  M4, same as "+" terminal.
22 | P2            M6, polygon;      M4, same as "+" terminal.
23 | P3            M6, polygon;      M4, same as "+" terminal.
24 | PB1           M6, polygon;      M4, same as "+" terminal.
25 | PB2           M6, polygon;      M4, same as "+" terminal.
26 | PB3           M6, polygon;      M4, same as "+" terminal.
27 | PB4           M6, polygon;      M4, same as "+" terminal.
28 | J1            M6, polygon;      M5, same as "+" terminal.
29 | J2            M6, polygon;      M5, same as "+" terminal.
30 | J3            M6, polygon;      M5, same as "+" terminal.
31 | J4            M6, polygon;      M5, same as "+" terminal.
32 | J5            M6, polygon;      M5, same as "+" terminal.
33 | J6            M6, polygon;      M5, same as "+" terminal.
34 |
35 | SVD info: Condition nr. = 7.754; unknowns = 40; rank = 40.
36 |
37 | Impedance     Inductance [H]       Resistance [Ohm]      AbsDiff      PercDiff
38 | Name          Design        Extracted    Design        Extracted    (L only)    (L only)
39 | L1            --           1.49169E-12  --           --           +1.4917E-12  --%
40 | L2            1.526E-12    1.53461E-12  --           --           +8.6065E-15  +0.56399%
41 | L3            2.915E-12    2.87691E-12  --           --           -3.809E-14   -1.3067%
42 | L4            4.8E-13      4.79727E-13  --           --           -2.7336E-16  -0.056949%
43 | L5            1.27E-12     1.29653E-12  --           --           +2.6531E-14  +2.0891%
44 | L6            1.27E-12     1.28261E-12  --           --           +1.2609E-14  +0.99283%
45 | L7            1.257E-12    1.29052E-12  --           --           +3.3524E-14  +2.667%
46 | L8            1.257E-12    1.30541E-12  --           --           +4.8409E-14  +3.8512%
47 | L9            --           6.86244E-13  --           --           +6.8624E-13  --%
48 | L10           --           6.78006E-13  --           --           +6.7801E-13  --%
49 | LB1           --           1.4803E-12   --           --           +1.4803E-12  --%
50 | LB2           --           2.73025E-12  --           --           +2.7303E-12  --%
51 | LB3           --           2.22471E-12  --           --           +2.2247E-12  --%
52 | LB4           --           2.7607E-12   --           --           +2.7607E-12  --%
53 | LP1           --           5.28207E-13  --           --           +5.2821E-13  --%
54 | LP2           --           5.2066E-13   --           --           +5.2066E-13  --%
55 | LP3           --           5.73088E-13  --           --           +5.7309E-13  --%
56 | LP4           --           4.29024E-13  --           --           +4.2902E-13  --%
57 | LP5           --           5.82022E-13  --           --           +5.8202E-13  --%
58 | LP6           --           4.62166E-13  --           --           +4.6217E-13  --%
59 |
60 | Ports          Design        Extracted    AbsDiff      PercDiff
61 | J1            0.000101    0.00010875
62 | J2            0.00017      0.00017853
63 | J3            0.000121    0.00012895
64 | J4            0.00017      0.00017853
65 | J5            0.000121    0.00012895
66 | J6            0.00017      0.00017853
67 |
68 | Error bound on extracted values: 5.45866%
69 |
70 | Deallocating memory.
71 | Cycles found in 0.030 seconds.
72 | SVD solution in 0.014 seconds.
73 | Job finished in 166.023 seconds.

```

**Listing 4.10:** RSFQ CLKSPPLIT InductEx extraction.

## Analog model

```

1  * Author: L. Schindler
2  * Version: 1.5.1
3  * Last modification date: 18 June 2020
4  * Last modification by: L. Schindler
5
6  *$Ports a q0 q1
7  .subckt LSMITLL_CLKSPLTT a q0 q1
8  .model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
9  .param Phi0=2.067833848E-15
10 .param B0=1
11 .param Ic0=0.0001
12 .param IcRs=100u*6.859904418
13 .param B0Rs=IcRs/Ic0*B0
14 .param Rsheet=2
15 .param Lsheet=1.13e-12
16 .param LP=0.2p
17 .param IC=1.9
18 .param ICreceive=1.6
19 .param ICtrans=2.5
20 .param Lptl=2p
21 .param LB=2p
22 .param BiasCoef=0.83
23 .param RD=1.36
24 .param B1=ICreceive
25 .param B2=IC
26 .param B3=ICtrans
27 .param B4=ICtrans
28 .param IB1=BiasCoef*(B1*Ic0+B2*Ic0)
29 .param IB2=BiasCoef*(B3*Ic0)
30 .param IB3=BiasCoef*(B4*Ic0)
31 .param L1=Lptl
32 .param L2=(Phi0/(2*B1*Ic0))*(B2/(B1+B2))
33 .param L3=(Phi0/(2*B1*Ic0))*(B1/(B1+B2))
34 .param L4=(Phi0/(2*B2*Ic0))/2
35 .param L5=(Phi0/(2*B2*Ic0))/2
36 .param L6=Lptl
37 .param L7=(Phi0/(2*B2*Ic0))/2
38 .param L8=Lptl
39 .param RB1=B0Rs/B1
40 .param RB2=B0Rs/B2
41 .param RB3=B0Rs/B3
42 .param RB4=B0Rs/B4
43 .param LRB1=(RB1/Rsheet)*Lsheet
44 .param LRB2=(RB2/Rsheet)*Lsheet
45 .param LRB3=(RB3/Rsheet)*Lsheet
46 .param LRB4=(RB4/Rsheet)*Lsheet
47 IB1 0 4 pw1(0 0 5p IB1)
48 IB2 0 8 pw1(0 0 5p IB2)
49 IB3 0 11 pw1(0 0 5p IB3)
50 B1 2 3 jjmit area=B1
51 B2 5 6 jjmit area=B2
52 B3 8 9 jjmit area=B3
53 B4 11 12 jjmit area=B4
54 L1 a 2 L1
55 L2 2 4 L2
56 L3 4 5 L3
57 L4 5 7 L4
58 L5 7 8 L5
59 L6 8 10 L6
60 L7 7 11 L7
61 L8 11 13 L8
62 LP1 3 0 0.2p
63 LP2 6 0 0.2p
64 LP3 9 0 0.2p
65 LP4 12 0 0.2p
66 RB1 2 102 RB1
67 LRB1 102 0 LRB1

```

```
68 | RB2 5 105 RB2
69 | LRB2 105 0 LRB2
70 | RB3 8 108 RB3
71 | LRB3 108 0 LRB3
72 | RB4 11 111 RB4
73 | LRB4 111 0 LRB4
74 | RD1 13 q0 RD
75 | RD2 10 q1 RD
76 | .ends
```

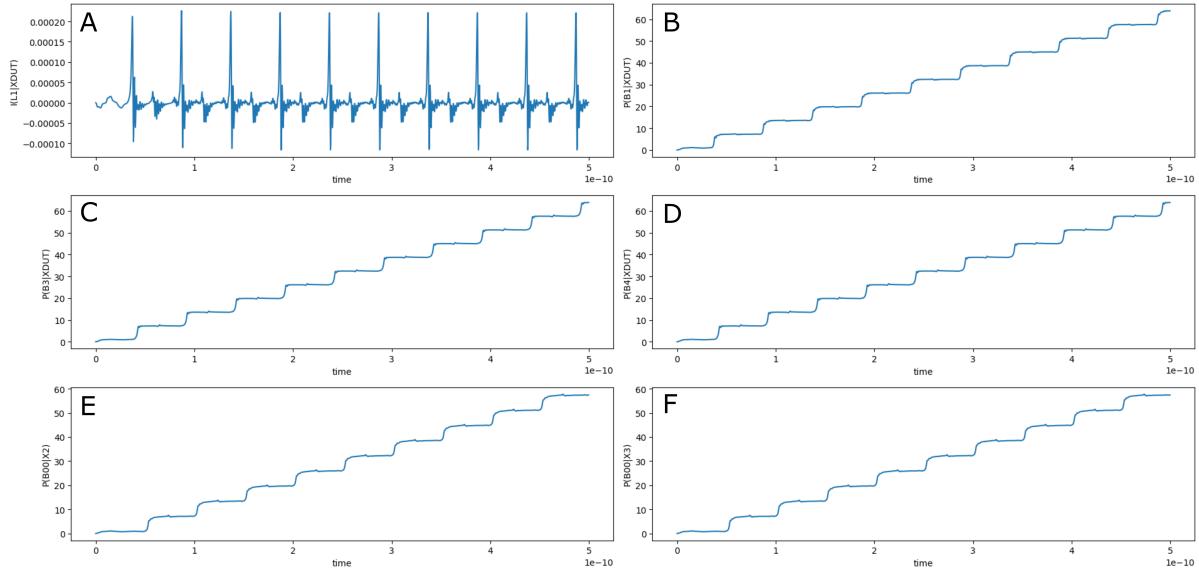
**Listing 4.11:** RSFQ CLKSPPLIT JoSIM netlist.

**Table 4.7:** RSFQ CLKSPPLIT pin list.

Pin	Description
a	Data input
q0	Data output
q1	Data output

The JoSIM simulation results for the RSFQ CLKSPPLITT are shown in Fig. 4.18. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q0**,
- (d) the phase over the output JJ of pin **q1**,
- (e) the phase over the input JJ of the load cell connected to pin **q0**, and
- (f) the phase over the input JJ of the load cell connected to pin **q1**.



**Figure 4.18:** RSFQ CLKSPPLITT analog simulation results.

## Digital model

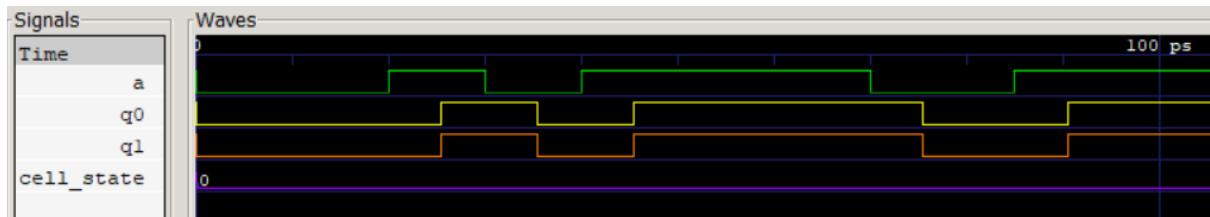
```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 // -----
9 `timescale 1ps/100fs
10 module LSmitll_CLKSPLTT_v1p5 (a, q0, q1);
11
12 input
13   a;
14 output
15   q0, q1;
16 reg
17   q0, q1;
18
19 real
20   delay_state0_a_q0 = 5.5,
21   delay_state0_a_q1 = 5.5,
22   ct_state0_a_a = 7.0;
23 reg
24   errorsignal_a;
25
26 integer
27   outfile,
28   cell_state; // internal state of the cell
29
30 initial
31 begin
32   errorsignal_a = 0;
33   cell_state = 0; // Startup state
34   q0 = 0; // All outputs start at 0
35   q1 = 0; // All outputs start at 0
36 end
37
38 always @(posedge a or negedge a) // execute at positive and negative edges of input
39 begin
40   if ($time>4) // arbitrary steady-state time)
41     begin
42       if (errorsignal_a == 1'b1) // A critical timing is active for this input
43         begin
44           outfile = $fopen("errors.txt", "a");
45           $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n"
46           ↪ ", $stime);
47           $fclose(outfile);
48           q0 <= 1'bX; // Set all outputs to unknown
49           q1 <= 1'bX; // Set all outputs to unknown
50         end
51       if (errorsignal_a == 0)
52         begin
53           case (cell_state)
54             0: begin
55               q0 <= #(delay_state0_a_q0) !q0;
56               q1 <= #(delay_state0_a_q1) !q1;
57               errorsignal_a = 1; // Critical timing on this input; assign
58               ↪ immediately
59               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
59               ↪ after critical timing expires
60             end
61           endcase
62         end
63     end
64   end
65 endmodule

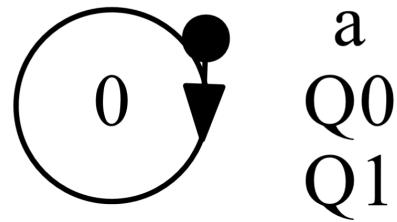
```

**Listing 4.12:** RSFQ CLKSPLTT verilog model.

The digital simulation results for the RSFQ CLKSPPLTT is shown in Fig. 4.19 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.20.



**Figure 4.19:** RSFQ CLKSPPLTT digital simulation results.



**Figure 4.20:** RSFQ CLKSPPLTT Mealy finite state diagram.

## Power consumption

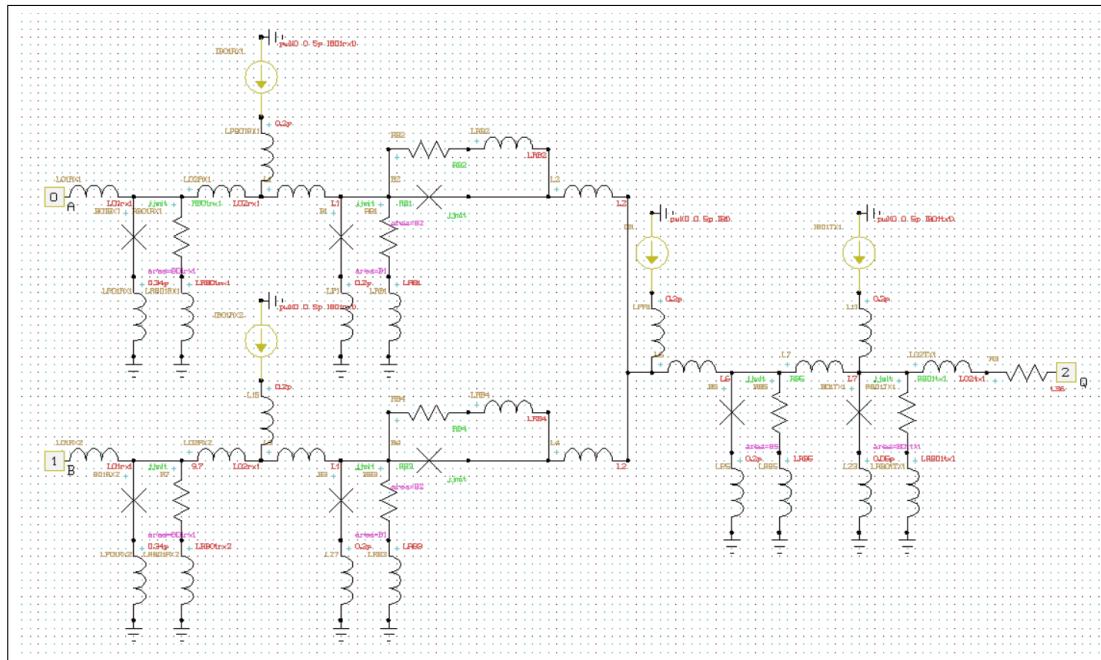
**Table 4.8:** RSFQ CLKSPPLTT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	186	1.76
2	186	3.52
5	186	8.79
10	186	17.6
20	186	35.2
50	186	87.9

### 4.1.5 MERGET

The MERGET joins two input pulse signal lines and provides a single output pulse signal line. If there is a pulse on either input lines, the MERGET will generate a pulse on the output signal line. The MERGET has integrated PTL transmitters and receivers is designed to be directly connected to a PTL.

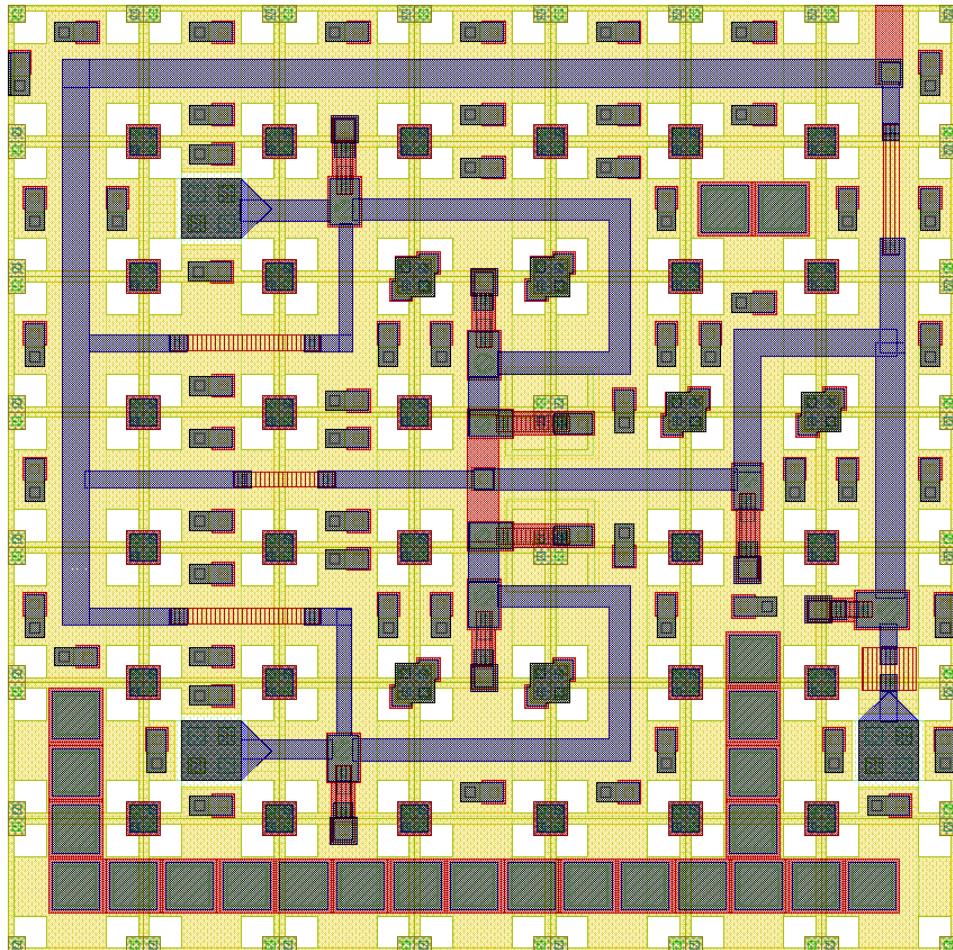
#### Schematic



**Figure 4.21:** Schematic of RSFQ MERGET.

## Layout

The physical layout of the RSFQ MERGET is shown in Fig. 4.22 and the resulting InductEx extraction is shown in Listing 4.13. The height of the layout is  $70 \mu\text{m}$  and the width is  $70 \mu\text{m}$ .



**Figure 4.22:** RSFQ MERGET layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_MERGET_v1p5.GDS -n LSmitll_MERGET_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_MERGET_v1p5_idx.cir read. Totals: L = 20, k = 0, P = 15.
7 | Total fundamental loops identified in netlist = 12
8 | Using TetraHenry with analytical integration.
9 | 3031 structures read. Reduced 3031 objects to 1868 polygons and 7 terminals.
10 | Top level structure is "LSMITLL_MERGET_V1P5".
11 | GDS file LSmitll_MERGET_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 | Object in layer I5 moved to TERM layer. (Pj1)
13 | Object in layer I5 moved to TERM layer. (Pj2)
14 | Object in layer I5 moved to TERM layer. (Pj3)
15 | Object in layer I5 moved to TERM layer. (Pj4)
16 | Object in layer I5 moved to TERM layer. (Pj5)
17 | Object in layer I5 moved to TERM layer. (Pj6)
18 | Object in layer I5 moved to TERM layer. (Pj7)
19 | Object in layer I5 moved to TERM layer. (Pj8)
20 | Terminal blocks = 15; Labels = 15; Extracted Ports = 15

```

```

21
22 Port          Positive terminal    Negative terminal
23 P1            M6,   line along y; M4,   same as "+" terminal.
24 P2            M6,   line along y; M4,   same as "+" terminal.
25 P3            M6,   line along x; M4,   same as "+" terminal.
26 PB1           M6,   line along y; M4,   same as "+" terminal.
27 PB2           M6,   line along y; M4,   same as "+" terminal.
28 PB3           M6,   line along y; M4,   same as "+" terminal.
29 PB4           M6,   line along x; M4,   same as "+" terminal.
30 J1            M6,   polygon;      M5,   same as "+" terminal.
31 J2            M6,   polygon;      M5,   same as "+" terminal.
32 J3            M6,   polygon;      M5,   same as "+" terminal.
33 J4            M6,   polygon;      M5,   same as "+" terminal.
34 J5            M6,   polygon;      M5,   same as "+" terminal.
35 J6            M6,   polygon;      M5,   same as "+" terminal.
36 J7            M6,   polygon;      M5,   same as "+" terminal.
37 J8            M6,   polygon;      M5,   same as "+" terminal.
38
39 SVD info: Condition nr. = 22.23; unknowns = 40; rank = 40.
40
41 Impedance     Inductance [H]       Resistance [Ohm]     AbsDiff      PercDiff
42 Name          Design        Extracted    Design        Extracted    (L only)    (L only)
43 L1            --           1.43596E-12  --           --           +1.436E-12  --%
44 L2            7E-12        6.9603E-12  --           --           -3.9696E-14 -0.56709%
45 L3            1.1516E-12  1.1585E-12  --           --           +6.8974E-15 +0.59894%
46 L4            --           1.46901E-12  --           --           +1.469E-12  --%
47 L5            7E-12        6.98178E-12  --           --           -1.8223E-14 -0.26033%
48 L6            1.1516E-12  1.16474E-12  --           --           +1.3135E-14 +1.1406%
49 L7            3.432E-12   3.42648E-12  --           --           -5.5184E-15 -0.16079%
50 L8            2.706E-12   2.72351E-12  --           --           +1.7511E-14 +0.6471%
51 L9            2.706E-12   2.72509E-12  --           --           +1.9087E-14 +0.70534%
52 L10           --           4.94845E-13  --           --           +4.9484E-13 --%
53 LB1           --           2.78262E-12  --           --           +2.7826E-12 --%
54 LB2           --           2.76369E-12  --           --           +2.7637E-12 --%
55 LB3           --           2.49926E-12  --           --           +2.4993E-12 --%
56 LB4           --           1.32299E-12  --           --           +1.323E-12  --%
57 LP1           --           4.81069E-13  --           --           +4.8107E-13 --%
58 LP2           --           5.38402E-13  --           --           +5.384E-13  --%
59 LP4           --           4.79009E-13  --           --           +4.7901E-13 --%
60 LP5           --           5.35867E-13  --           --           +5.3587E-13 --%
61 LP7           --           5.92031E-13  --           --           +5.9203E-13 --%
62 LP8           --           3.667E-13   --           --           +3.667E-13  --%
63
64 Ports         Design        Extracted  AbsDiff      PercDiff
65 J1            --           0.00016855
66 J2            --           0.00016197
67 J3            --           0.00010274
68 J4            --           0.00016855
69 J5            --           0.00016197
70 J6            --           0.00010274
71 J7            --           0.00012397
72 J8            --           0.00025893
73
74 Error bound on extracted values: 2.75924%
75
76 Deallocating memory.
77 Cycles found in 0.028 seconds.
78 SVD solution in 0.015 seconds.
79 Job finished in 259.423 seconds.

```

**Listing 4.13:** RSFQ MERGET InductEx extraction.

## Analog model

```

1 * Author: L. Schindler
2 * Version: 1.5.1
3 * Last modification date: 18 June 2020
4 * Last modification by: L. Schindler
5
6 *$Ports
7 .subckt LSmitll_MERGET a b q
8 .model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
9 .param B0=1
10 .param Ic0=0.0001
11 .param IcRs=100u*6.859904418
12 .param B0Rs=IcRs/Ic0*B0
13 .param Rsheet=2
14 .param Lsheet=1.13e-12
15 .param B01rx1=0.88429
16 .param B01tx1=0.842106
17 .param B1=1.45438
18 .param B2=0.960422
19 .param B5=0.805138
20 .param IB01rx1=0.000106334
21 .param IB01tx1=5.04979e-5
22 .param IB1=0.000186124
23 .param L01rx1=2e-012
24 .param L02rx1=1.27924e-012
25 .param L02tx1=4.81637e-012
26 .param L1=1.75737e-012
27 .param L2=2e-012
28 .param L6=2.22418e-012
29 .param L7=8.49377e-012
30 .param LRB01rx1=(RB01rx1/Rsheet)*Lsheet
31 .param LRB01rx2=(RB01rx2/Rsheet)*Lsheet
32 .param LRB01tx1=(RB01tx1/Rsheet)*Lsheet
33 .param LRB1=(RB1/Rsheet)*Lsheet
34 .param LRB2=(RB2/Rsheet)*Lsheet
35 .param LRB3=(RB3/Rsheet)*Lsheet
36 .param LRB4=(RB4/Rsheet)*Lsheet
37 .param LRB5=(RB5/Rsheet)*Lsheet
38 .param RB01rx1=B0Rs/B01rx1
39 .param RB01rx2=B0Rs/B01rx1
40 .param RB01tx1=B0Rs/B01tx1
41 .param RB1=B0Rs/B1
42 .param RB2=B0Rs/B2
43 .param RB3=B0Rs/B1
44 .param RB4=B0Rs/B2
45 .param RB5=B0Rs/B5
46 B01rx1 6 18 jjmit area=B01rx1
47 B01rx2 13 32 jjmit area=B01rx1
48 B01tx1 10 28 jjmit area=B01tx1
49 B1 7 20 jjmit area=B1
50 B2 4 5 jjmit area=B2
51 B3 14 34 jjmit area=B1
52 B4 11 12 jjmit area=B2
53 B5 9 26 jjmit area=B5
54 IB01rx1 0 15 pw1(0 0 5p IB01rx1)
55 IB01rx2 0 24 pw1(0 0 5p IB01rx1)
56 IB01tx1 0 23 pw1(0 0 5p IB01tx1)
57 IB1 0 22 pw1(0 0 5p IB1)
58 L01rx1 a 6 L01rx1
59 L01rx2 b 13 L01rx1
60 L02rx1 6 16 L02rx1
61 L02rx2 13 30 L02rx1
62 L02tx1 10 25 L02tx1
63 L1 16 7 L1
64 L2 5 8 L2
65 L3 30 14 L1
66 L12 23 10 0.2p
67 L16 24 30 0.2p

```

```

68 | L1b 7 4 1p
69 | L25 28 0 0.05p
70 | L29 34 0 0.2p
71 | L3b 14 11 1p
72 | L4 12 8 L2
73 | L6 8 9 L6
74 | L7 9 10 L7
75 | LP01rx1 18 0 0.34p
76 | LP01rx2 32 0 0.34p
77 | LP1 20 0 0.2p
78 | LP5 26 0 0.2p
79 | LPR01rx1 15 16 0.2p
80 | LPR1 22 8 0.2p
81 | LRB01rx1 19 0 LRB01rx1
82 | LRB01rx2 33 0 LRB01rx2
83 | LRB01tx1 29 0 LRB01tx1
84 | LRB1 21 0 LRB1
85 | LRB2 17 5 LRB2
86 | LRB3 35 0 LRB3
87 | LRB4 31 12 LRB4
88 | LRB5 27 0 LRB5
89 | R3 25 q 1.36
90 | RB01rx2 13 33 RB01rx2
91 | RB01rx1 6 19 RB01rx1
92 | RB01tx1 10 29 RB01tx1
93 | RB1 7 21 RB1
94 | RB2 4 17 RB2
95 | RB3 14 35 RB3
96 | RB4 11 31 RB4
97 | RB5 9 27 RB5
98 | .ends

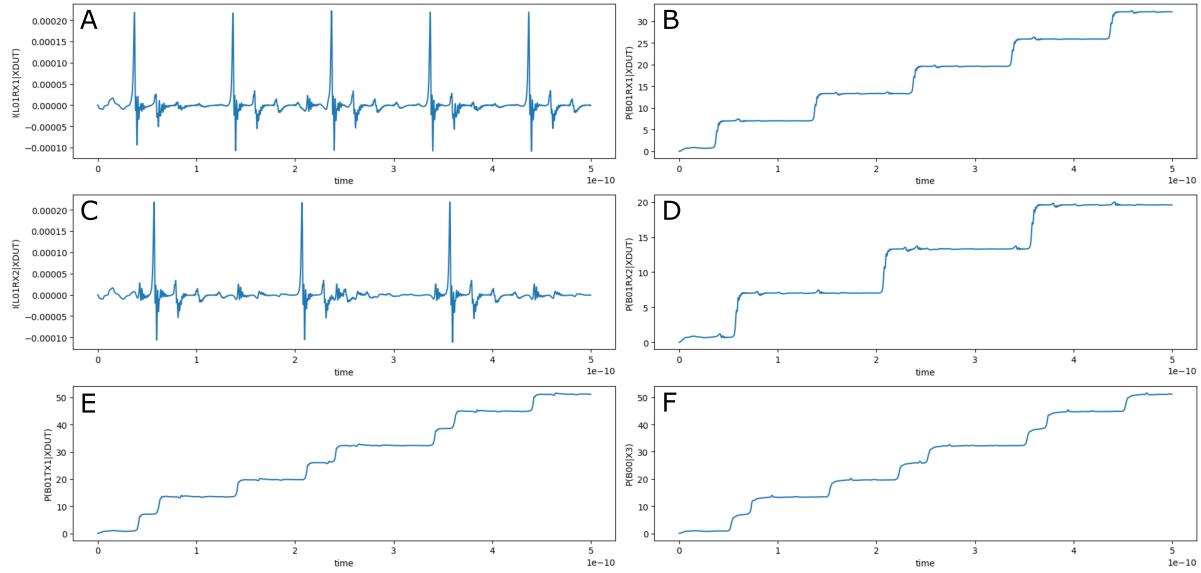
```

**Listing 4.14:** RSFQ MERGET JoSIM netlist.**Table 4.9:** RSFQ MERGET pin list.

<b>Pin</b>	<b>Description</b>
<b>a</b>	Data input
<b>b</b>	Data input
<b>q</b>	Data output

The JoSIM simulation results for the RSFQ MERGET are shown in Fig. 4.23. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b**,
- (d) the phase over the input JJ of pin **b**,
- (e) the phase over the output JJ of pin **q**,
- (f) the phase over the input JJ of the load cell connected to pin **q** via a PTL.



**Figure 4.23:** RSFQ MERGET analog simulation results.

## Digital model

```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 // -----
9 `timescale 1ps/100fs
10 module LSmitll_MERGET_v1p5 (a, b, q);
11
12 input
13   a, b;
14
15 output
16   q;
17
18 reg
19   q;
20
21 real
22   delay_state0_a_q = 5.3,
23   delay_state0_b_q = 5.3,
24   ct_state0_a_a = 4.8,
25   ct_state0_a_b = 1.6,
26   ct_state0_b_a = 1.6,
27   ct_state0_b_b = 4.8;
28
29 reg
30   errorsignal_a,
31   errorsignal_b;
32
33 integer
34   outfile,
35   cell_state; // internal state of the cell
36
37 initial
38 begin
39     errorsignal_a = 0;
40     errorsignal_b = 0;
41     cell_state = 0; // Startup state
42     q = 0; // All outputs start at 0
43 end
44
45 always @ (posedge a or negedge a) // execute at positive and negative edges of input
46 begin
47     if ($time > 4) // arbitrary steady-state time)
48         begin
49             if (errorsignal_a == 1'b1) // A critical timing is active for this input
50                 begin
51                     outfile = $fopen("errors.txt", "a");
52                     $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n"
53                               "    ↪ ", $stime);
54                     $fclose(outfile);
55                     q <= 1'bX; // Set all outputs to unknown
56                 end
57             if (errorsignal_a == 0)
58                 begin
59                     case (cell_state)
60                         0: begin
61                             q <= #(delay_state0_a_q) !q;
62                             errorsignal_a = 1; // Critical timing on this input; assign
63                               "    ↪ immediately
64                             errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
65                               "    ↪ after critical timing expires
66                             errorsignal_b = 1; // Critical timing on this input; assign
67                               "    ↪ immediately

```

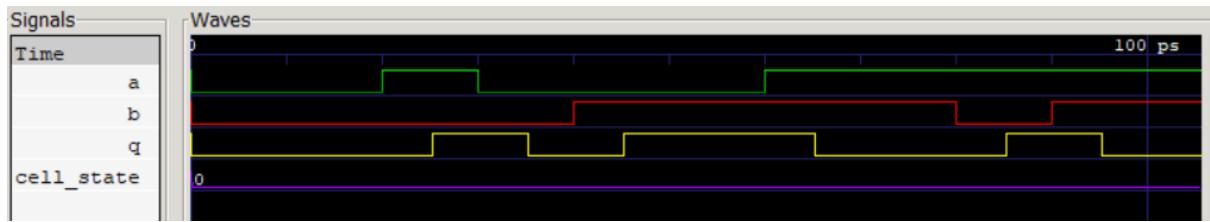
```

64          errorsignal_b <= #(ct_state0_a_b) 0; // Clear error signal
65          // after critical timing expires
66      end
67      endcase
68  end
69 end
70
71 always @(posedge b or negedge b) // execute at positive and negative edges of input
72 begin
73   if ($time>4) // arbitrary steady-state time)
74     begin
75       if (errorsignal_b == 1'b1) // A critical timing is active for this input
76         begin
77           outfile = $fopen("errors.txt", "a");
78           $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
79           // ", $stime);
80           $fclose(outfile);
81           q <= 1'bX; // Set all outputs to unknown
82         end
83       if (errorsignal_b == 0)
84         begin
85           case (cell_state)
86             0: begin
87               q <= #(delay_state0_b_q) !q;
88               errorsignal_a = 1; // Critical timing on this input; assign
89               // immediately
90               errorsignal_a <= #(ct_state0_b_a) 0; // Clear error signal
91               // after critical timing expires
92               errorsignal_b = 1; // Critical timing on this input; assign
93               // immediately
94               errorsignal_b <= #(ct_state0_b_b) 0; // Clear error signal
95               // after critical timing expires
96             end
97           endcase
98         end
99     end
100 endmodule

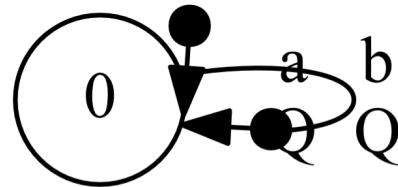
```

**Listing 4.15:** RSFQ MERGET verilog model.

The digital simulation results for the RSFQ MERGET is shown in Fig. 4.24 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.25.



**Figure 4.24:** RSFQ MERGET digital simulation results.



**Figure 4.25:** RSFQ MERGET Mealy finite state diagram.

## Power consumption

**Table 4.10:** RSFQ MERGET power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	117	1.71
2	117	3.41
5	117	8.53
10	117	17.1
20	117	34.1
50	117	85.3

#### 4.1.6 PTLTX

The RSFQ PTLTX is a cell which transmits a pulse signal over a PTL. It is connected to cells that are not designed to connect to PTLs when a PTL connection is required.

##### Schematic

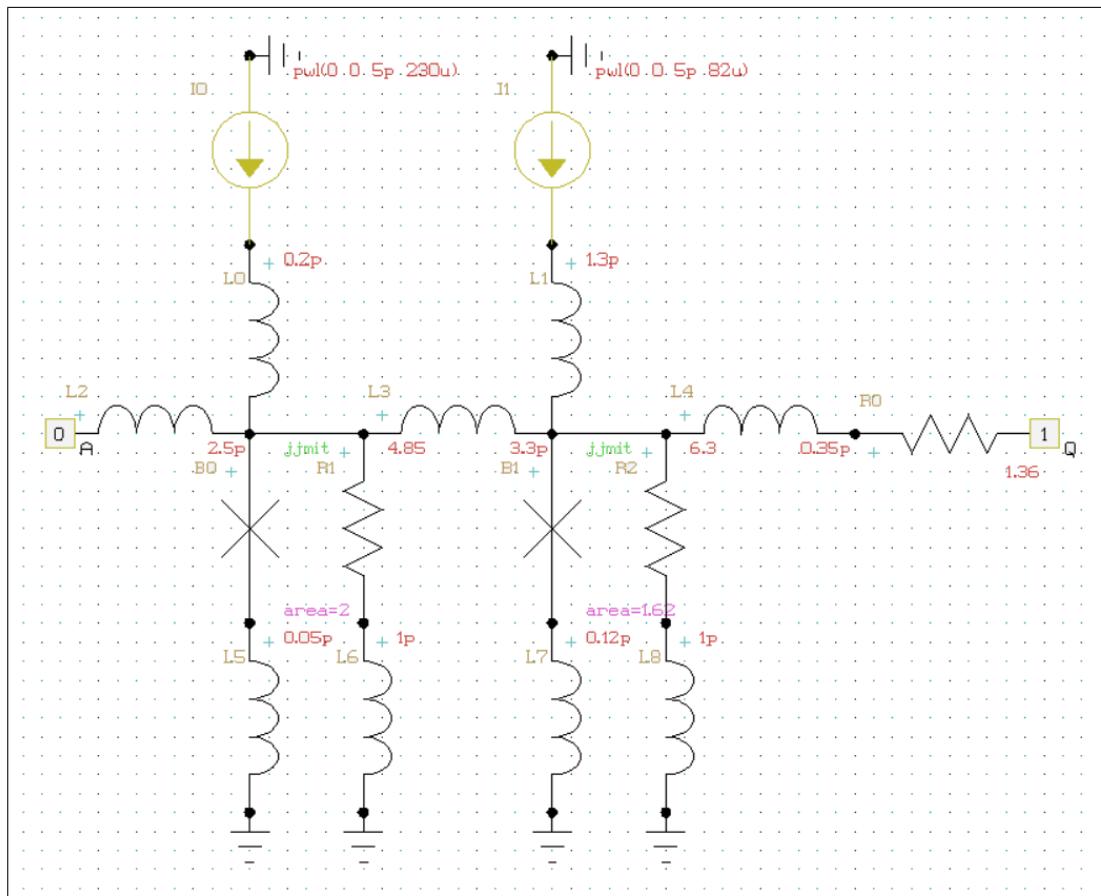
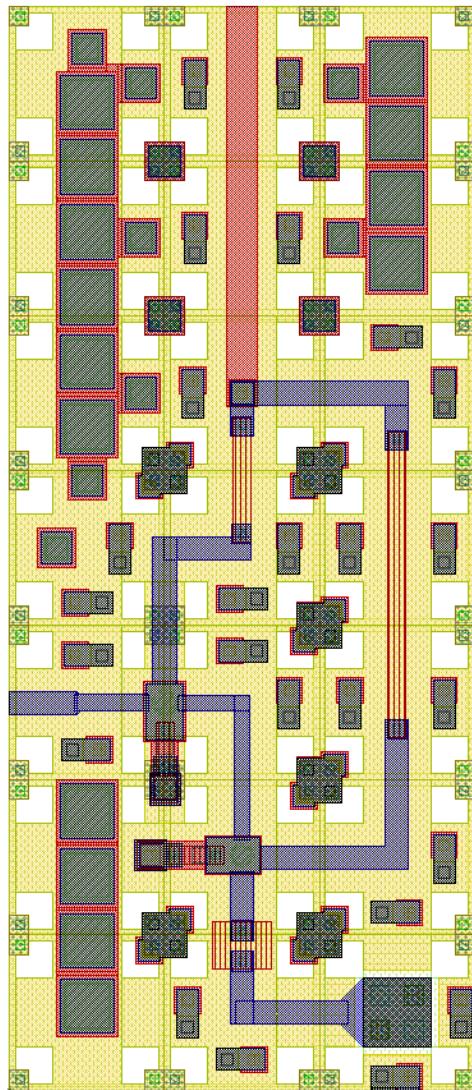


Figure 4.26: Schematic of RSFQ PTLTX.

## Layout

The physical layout for the RSFQ PTLTX is shown in Fig. 4.27 and the resulting InductEx extraction is shown in Listing 4.16. The layout height is  $70 \mu\text{m}$  and the width is  $30 \mu\text{m}$ .



**Figure 4.27:** RSFQ PTLTX Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_PTLTX_v1p5.GDS -n LSmitll_ptltx_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_ptltx_v1p5_idx.cir read. Totals: L = 7, k = 0, P = 6.
7 | Total fundamental loops identified in netlist = 5
8 | Using TetraHenry with analytical integration.
9 | 898 structures read. Reduced 898 objects to 842 polygons and 4 terminals.
10 | Top level structure is "LSMITLL_PTLTX_V1P5".
11 | GDS file LSmitll_PTLTX_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 | Object in layer I5 moved to TERM layer. (Pj1)
13 | Object in layer I5 moved to TERM layer. (Pj2)
14 | Terminal blocks = 6; Labels = 6; Extracted Ports = 6
15 |
16 | Port           Positive terminal    Negative terminal
17 | P1             M6, line along y; M4, same as "+" terminal.
18 | P2             M6, polygon;       M4, same as "+" terminal.
19 | P3             M6, polygon;       M4, same as "+" terminal.
20 | P4             M6, polygon;       M4, same as "+" terminal.
21 | J1             M6, polygon;       M5, same as "+" terminal.
22 | J2             M6, polygon;       M5, same as "+" terminal.
23 |
24 | SVD info: Condition nr. = 3.491; unknowns = 14; rank = 14.
25 |
26 | Impedance     Inductance [H]      Resistance [Ohm]      AbsDiff      PercDiff
27 | Name          Design            Extracted        Design        Extracted    (L only)    (L only)
28 | L1            2.5E-12          2.49244E-12    --          --          -7.5618E-15 -0.30247%
29 | L2            3.3E-12          3.30827E-12    --          --          +8.2664E-15 +0.2505%
30 | L3            --              1.00626E-12    --          --          +1.0063E-12 --%
31 | LP1           --              5.06259E-13    --          --          +5.0626E-13 --%
32 | LP2           --              4.76485E-13    --          --          +4.7648E-13 --%
33 | LB1           --              2.87048E-12    --          --          +2.8705E-12 --%
34 | LB2           --              3.42025E-12    --          --          +3.4203E-12 --%
35 |
36 | Ports         Design          Extracted      AbsDiff      PercDiff
37 | J1            0.0002          0.00020853
38 | J2            0.000162        0.00017055
39 |
40 | Error bound on extracted values: 2.97934%
41 |
42 | Deallocating memory.
43 | Cycles found in 0.028 seconds.
44 | SVD solution in 0.017 seconds.
45 | Job finished in 78.918 seconds.

```

**Listing 4.16:** RSFQ PTLTX InductEx extraction.

## Analog model

```

1 * Author: L. Schindler
2 * Version: 1.5.1
3 * Last modification date: 18 June 2020
4 * Last modification by: L. Schindler
5
6 * Ports
7 .subckt LSmitll_PTLTX a q
8 .model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
9 B0 3 8 12 jjmit area=2
10 B1 4 10 13 jjmit area=1.62
11 I0 0 5 pwl(0 0 5p 230u)
12 I1 0 6 pwl(0 0 5p 82u)
13 L0 5 3 0.2p
14 L1 6 4 1.3p
15 L2 a 3 2.5p
16 L3 3 4 3.3p
17 L4 4 7 0.35p
18 L5 8 0 0.05p
19 L6 9 0 1p
20 L7 10 0 0.12p
21 L8 11 0 1p
22 R0 7 q 1.36
23 R1 3 9 4.85
24 R2 4 11 6.3
25 .ends

```

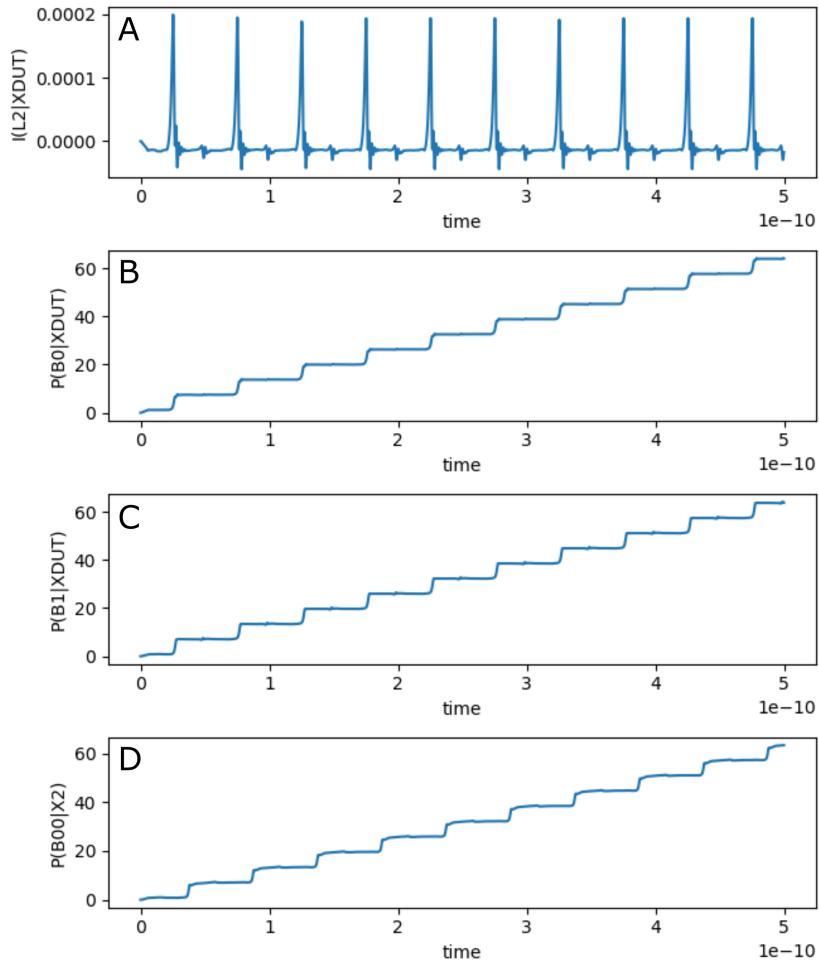
**Listing 4.17:** RSFQ PTLTX JoSIM netlist.

**Table 4.11:** RSFQ PTLTX pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ PTLTX using JoSIM is shown in Fig. 4.28. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q**, and
- (d) the phase over the input JJ of the load circuit connected via a PTL to the PTLTX.



**Figure 4.28:** RSFQ PTLTX analog simulation results.

## Digital model

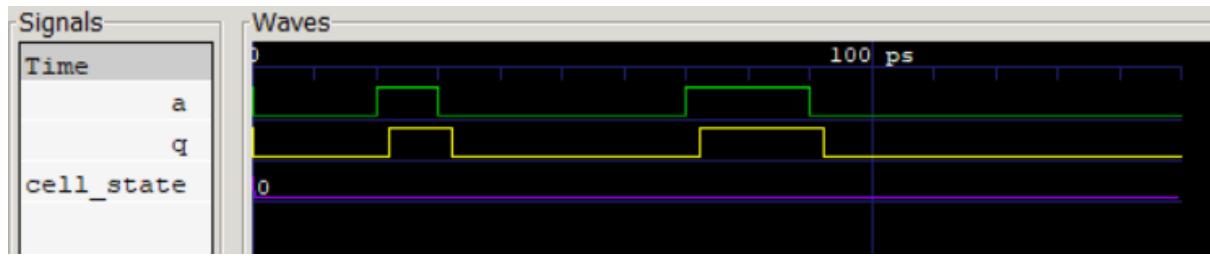
```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 //
9 `timescale 1ps/100fs
10 module LSmitll_ptltx_v1p5 (a, q);
11
12 input
13   a;
14
15 output
16   q;
17
18 reg
19   q;
20
21 real
22   delay_state0_a_q = 2.2,
23   ct_state0_a_a = 3.5;
24
25 reg
26   errorsignal_a;
27
28 integer
29   outfile,
30   cell_state; // internal state of the cell
31
32 initial
33 begin
34   errorsignal_a = 0;
35   cell_state = 0; // Startup state
36   q = 0; // All outputs start at 0
37 end
38
39 always @(posedge a or negedge a) // execute at positive and negative edges of input
40 begin
41   if ($time>4) // arbitrary steady-state time)
42     begin
43       if (errorsignal_a == 1'b1) // A critical timing is active for this input
44         begin
45           outfile = $fopen("errors.txt", "a");
46           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
47                         ↪ ", $stime);
48           $fclose(outfile);
49           q <= 1'bX; // Set all outputs to unknown
50         end
51       if (errorsignal_a == 0)
52         begin
53           case (cell_state)
54             0: begin
55               q <= #(delay_state0_a_q) !q;
56               errorsignal_a = 1; // Critical timing on this input; assign
57               ↪ immediately
58               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
59               ↪ after critical timing expires
60             end
61           endcase
62         end
63     end
64   end
65 endmodule

```

**Listing 4.18:** RSFQ PTLTX verilog model.

The digital simulation results for the RSFQ PTLTX is shown in Fig. 4.29 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.30.



**Figure 4.29:** RSFQ PTLTX digital simulation results.



**Figure 4.30:** RSFQ PTLTX Mealy finite state machine diagram.

## Power Consumption

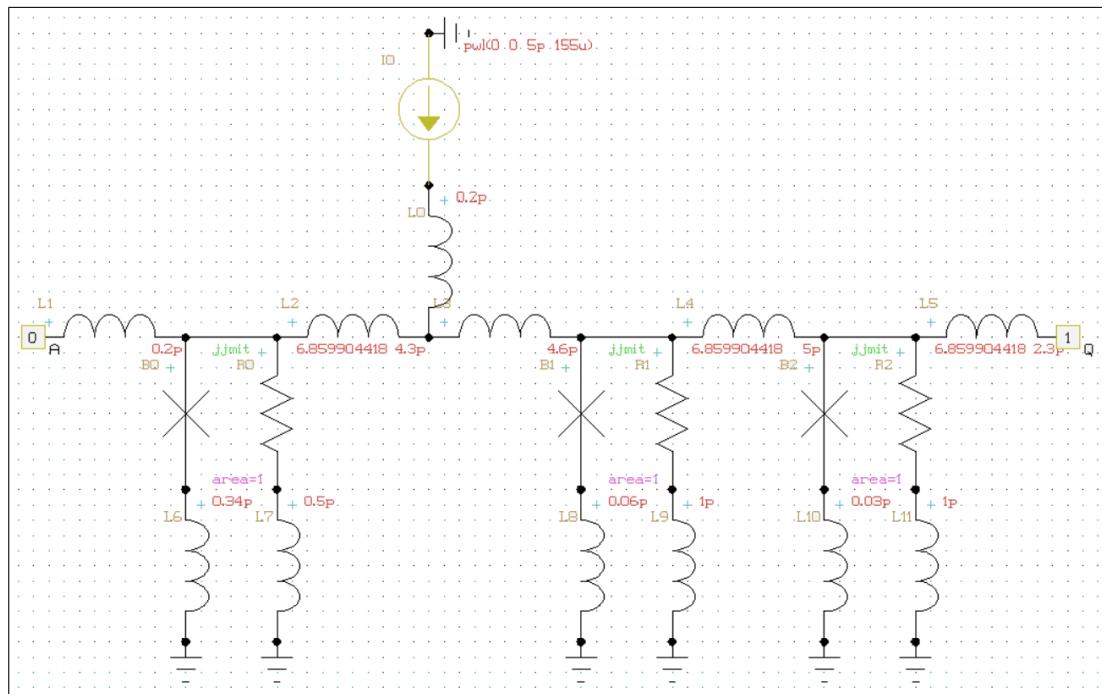
**Table 4.12:** RSFQ PTLTX power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	81	0.75
2	81	1.50
5	81	3.74
10	81	7.49
20	81	15.0
50	81	37.4

#### 4.1.7 PTLRX

The PTLRX is a receiver cell which receives a pulse signal from a PTL. It is connected to cells that are not designed to connect to PTLs when a PTL connection is required.

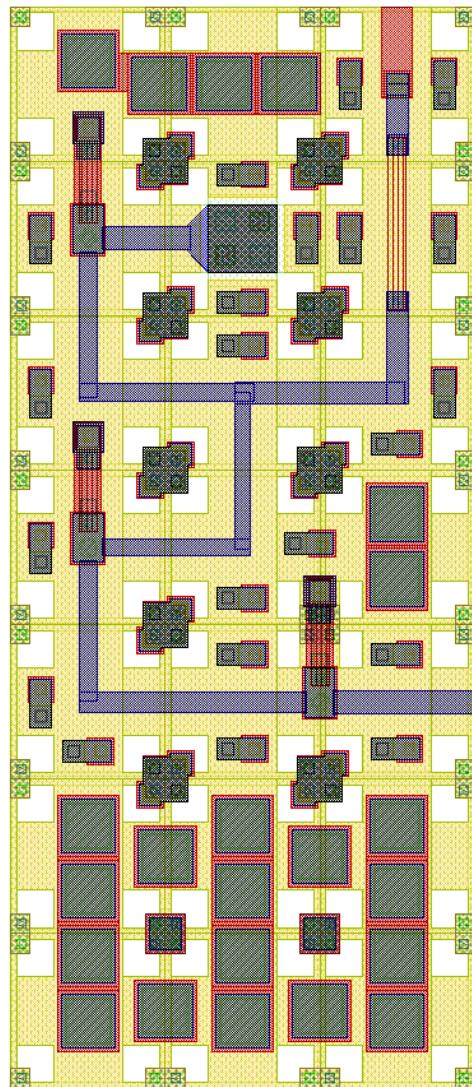
##### Schematic



**Figure 4.31:** Schematic of RSFQ PTLRX.

## Layout

The physical layout for the RSFQ PTLRX is shown in Fig. 4.32 and the resulting InductEx extraction is shown in Listing 4.19. The layout height is  $70 \mu\text{m}$  and the width is  $30 \mu\text{m}$ .



**Figure 4.32:** RSFQ PTLRX Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_PTLRX_v1p5.GDS -n LSmitll_ptlrx_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_ptlrx_v1p5_idx.cir read. Totals: L = 9, k = 0, P = 6.
7 | Total fundamental loops identified in netlist = 5
8 | Using TetraHenry with analytical integration.
9 | 881 structures read. Reduced 881 objects to 845 polygons and 3 terminals.
10 | Top level structure is "LSMITLL_PTLRX_V1P5".
11 | GDS file LSmitll_PTLRX_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 | Object in layer I5 moved to TERM layer. (Pj1)
13 | Object in layer I5 moved to TERM layer. (Pj2)
14 | Object in layer I5 moved to TERM layer. (Pj3)
15 | Terminal blocks = 6; Labels = 6; Extracted Ports = 6
16 |
17 | Port           Positive terminal     Negative terminal
18 | P1             M6, line along y;  M4, same as "+" terminal.
19 | P2             M6, polygon;       M4, same as "+" terminal.
20 | P3             M6, line along y;  M4, same as "+" terminal.
21 | J1             M6, polygon;       M5, same as "+" terminal.
22 | J2             M6, polygon;       M5, same as "+" terminal.
23 | J3             M6, polygon;       M5, same as "+" terminal.
24 |
25 | SVD info: Condition nr. = 10.05; unknowns = 18; rank = 18.
26 |
27 | Impedance      Inductance [H]      Resistance [Ohm]      AbsDiff      PercDiff
28 | Name           Design            Extracted          Design            Extracted      (L only)      (L only)
29 | L1              --               1.46476E-12    --               --           +1.4648E-12  --%
30 | L2              4.3E-12         4.28216E-12    --               --           -1.7838E-14 -0.41483%
31 | L3              4.6E-12         4.63061E-12    --               --           +3.0611E-14 +0.66546%
32 | L4              5E-12            4.98366E-12    --               --           -1.6344E-14 -0.32687%
33 | L5              2.3E-12         2.28808E-12    --               --           -1.192E-14  -0.51826%
34 | LB1             --               3.25119E-12    --               --           +3.2512E-12  --%
35 | LP1             --               5.57791E-13    --               --           +5.5779E-13  --%
36 | LP2             --               6.14427E-13    --               --           +6.1443E-13  --%
37 | LP3             --               5.44764E-13    --               --           +5.4476E-13  --%
38 |
39 | Ports          Design            Extracted          AbsDiff      PercDiff
40 | J1              0.0001          0.00010794
41 | J2              0.0001          0.00010794
42 | J3              0.0001          0.00010794
43 |
44 | Error bound on extracted values: 0.119751%
45 |
46 | Deallocating memory.
47 | Cycles found in 0.028 seconds.
48 | SVD solution in 0.015 seconds.
49 | Job finished in 77.204 seconds.

```

**Listing 4.19:** RSFQ PTLRX InductEx extraction.

## Analog model

```

1 * Author: L. Schindler
2 * Version: 1.5.1
3 * Last modification date: 18 June 2020
4 * Last modification by: L. Schindler
5
6 * Ports
7 .subckt LSmitll_PTLRX a q
8 .model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
9 B0 3 8 14 jjmit area=1
10 B1 4 10 15 jjmit area=1
11 B2 5 12 16 jjmit area=1
12 I0 0 6 pwl(0 0 5p 155u)
13 L0 6 7 0.2p
14 L1 a 3 0.2p
15 L2 3 7 4.3p
16 L3 7 4 4.6p
17 L4 4 5 5p
18 L5 5 q 2.3p
19 L6 8 0 0.34p
20 L7 9 0 0.5p
21 L8 10 0 0.06p
22 L9 11 0 1p
23 L10 12 0 0.03p
24 L11 13 0 1p
25 R0 3 9 6.859904418
26 R1 4 11 6.859904418
27 R2 5 13 6.859904418
28 .ends

```

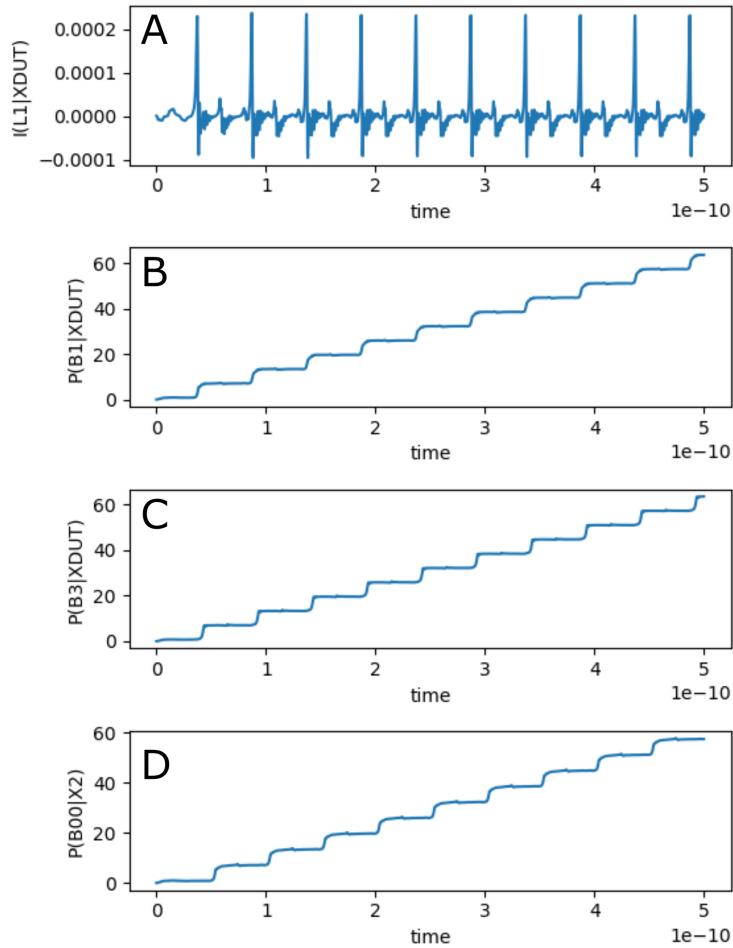
**Listing 4.20:** RSFQ PTLRX JoSIM netlist.

**Table 4.13:** RSFQ PTLRX pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ PTLRX using JoSIM is shown in Fig. 4.33. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q**, and
- (d) the phase over the input JJ of the load circuit connected to pin **q**.



**Figure 4.33:** RSFQ PTLRX analog simulation results.

## Digital model

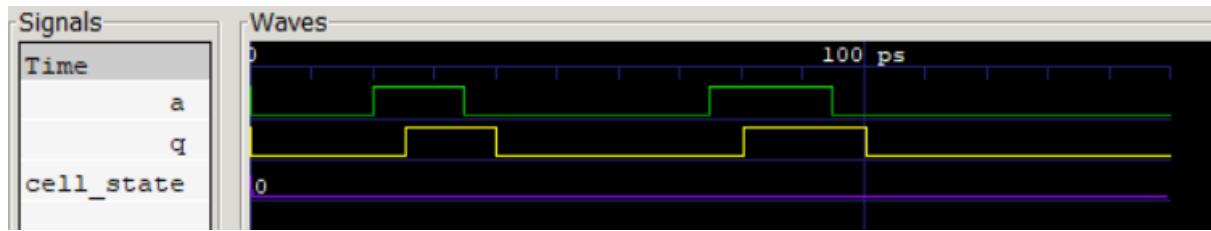
```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 //
9 'timescale 1ps/100fs
10 module LSmitll_ptlrx_v1p5 (a, q);
11
12 input
13   a;
14
15 output
16   q;
17
18 reg
19   q;
20
21 real
22   delay_state0_a_q = 5.3,
23   ct_state0_a_a = 11.3;
24
25 reg
26   errorsignal_a;
27
28 integer
29   outfile,
30   cell_state; // internal state of the cell
31
32 initial
33 begin
34     errorsignal_a = 0;
35     cell_state = 0; // Startup state
36     q = 0; // All outputs start at 0
37 end
38
39 always @(posedge a or negedge a) // execute at positive and negative edges of input
40 begin
41     if ($time>4) // arbitrary steady-state time)
42     begin
43         if (errorsignal_a == 1'b1) // A critical timing is active for this input
44         begin
45             outfile = $fopen("errors.txt", "a");
46             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
47                         " ", $stime);
48             $fclose(outfile);
49             q <= 1'bX; // Set all outputs to unknown
50         end
51         if (errorsignal_a == 0)
52         begin
53             case (cell_state)
54               0: begin
55                 q <= #(delay_state0_a_q) !q;
56                 errorsignal_a = 1; // Critical timing on this input; assign
57                 // immediately
58                 errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
59                 // after critical timing expires
60               end
61             endcase
62           end
63     end
64 endmodule

```

**Listing 4.21:** RSFQ PTLRX verilog model.

The digital simulation results for the RSFQ PTLRX is shown in Fig. 4.34 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.35.



**Figure 4.34:** RSFQ PTLRX digital simulation results.



**Figure 4.35:** RSFQ PTLRX Mealy finite state machine diagram.

## Power Consumption

**Table 4.14:** RSFQ PTLRX power consumption.

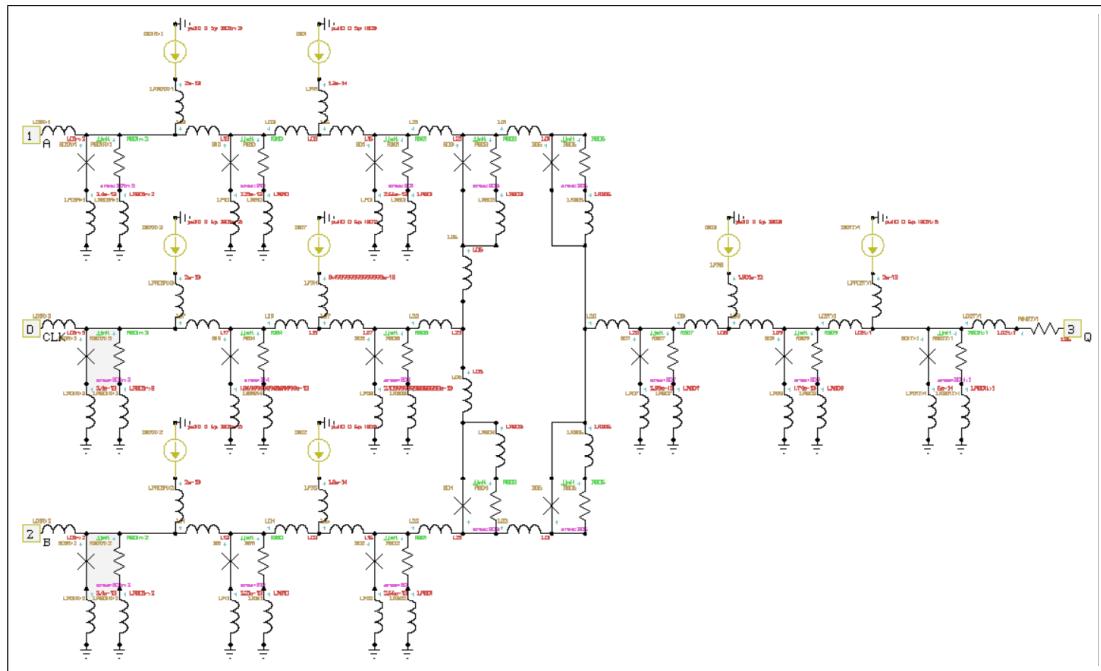
Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	40.3	0.62
2	40.3	1.24
5	40.3	3.10
10	40.3	6.20
20	40.3	12.4
50	40.3	31.0

## 4.2 Logic Cells

### 4.2.1 AND2T

The RSFQ AND2T cell generates an output pulse if pulses from both input signal lines were received before the clock signal. The AND2T is designed with integrated PTL transmitters and receivers and is meant to be connected directly to a PTL.

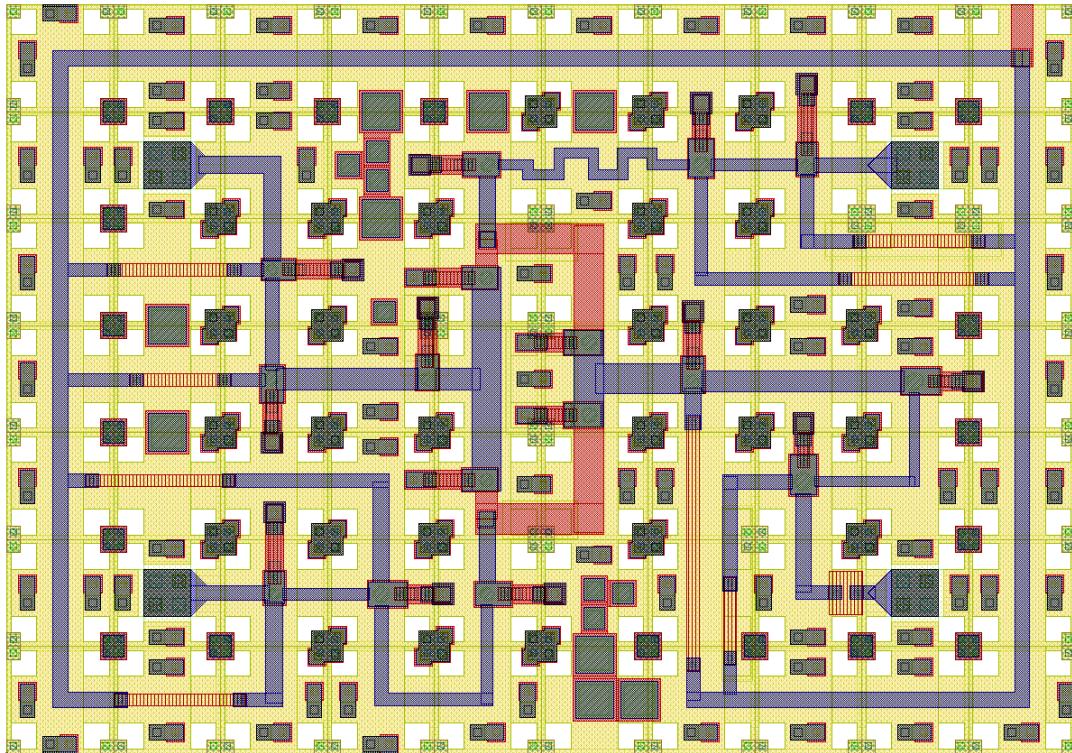
#### Schematic



**Figure 4.36:** Schematic of RSFQ AND2T.

## Layout

The physical layout for the RSFQ AND2T is shown in Fig. 4.37 and the resulting InductEx extraction is shown in Listing 4.22. The layout height is  $70 \mu m$  and the width is  $100 \mu m$ .



**Figure 4.37:** RSFQ AND2T Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_AND2T_v1p5.GDS -n LSmitll_AND2T_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_AND2T_v1p5_idx.cir read. Totals: L = 40, k = 0, P = 28.
7 | Total fundamental loops identified in netlist = 24
8 | Using TetraHenry with analytical integration.
9 | 2849 structures read. Reduced 2849 objects to 2647 polygons and 12 terminals.
10 | Top level structure is "LSMITLL_AND2T_V1P5".
11 | GDS file LSmitll_AND2T_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 | Port clk not in netlist. Ignored.
13 | Object in layer I5 moved to TERM layer. (Pj1)
14 | Object in layer I5 moved to TERM layer. (Pj2)
15 | Object in layer I5 moved to TERM layer. (Pj3)
16 | Object in layer I5 moved to TERM layer. (Pj4)
17 | Object in layer I5 moved to TERM layer. (Pj5)
18 | Object in layer I5 moved to TERM layer. (Pj6)
19 | Object in layer I5 moved to TERM layer. (Pj7)
20 | Object in layer I5 moved to TERM layer. (Pj8)
21 | Object in layer I5 moved to TERM layer. (Pj9)
22 | Object in layer I5 moved to TERM layer. (Pj10)
23 | Object in layer I5 moved to TERM layer. (Pj11)
24 | Object in layer I5 moved to TERM layer. (Pj12)
25 | Object in layer I5 moved to TERM layer. (Pj13)
26 | Object in layer I5 moved to TERM layer. (Pj14)
27 | Object in layer I5 moved to TERM layer. (Pj15)
28 | Object in layer I5 moved to TERM layer. (Pj16)
29 | Terminal blocks = 28; Labels = 29; Extracted Ports = 28
30 |
31 | Port           Positive terminal      Negative terminal
32 | P1             M6, line along y;    M4, same as "+" terminal.
33 | P2             M6, line along y;    M4, same as "+" terminal.
34 | P3             M6, line along y;    M4, same as "+" terminal.
35 | P4             M6, polygon;        M4, same as "+" terminal.
36 | PB1            M6, polygon;        M4, same as "+" terminal.
37 | PB2            M6, polygon;        M4, same as "+" terminal.
38 | PB3            M6, polygon;        M4, same as "+" terminal.
39 | PB4            M6, polygon;        M4, same as "+" terminal.
40 | PB5            M6, polygon;        M4, same as "+" terminal.
41 | PB6            M6, polygon;        M4, same as "+" terminal.
42 | PB7            M6, polygon;        M4, same as "+" terminal.
43 | PB8            M6, polygon;        M4, same as "+" terminal.
44 | J1              M6, polygon;       M5, same as "+" terminal.
45 | J2              M6, polygon;       M5, same as "+" terminal.
46 | J3              M6, polygon;       M5, same as "+" terminal.
47 | J4              M5, polygon;       M6, same as "+" terminal.
48 | J5              M5, polygon;       M6, same as "+" terminal.
49 | J6              M6, polygon;       M5, same as "+" terminal.
50 | J7              M6, polygon;       M5, same as "+" terminal.
51 | J8              M6, polygon;       M5, same as "+" terminal.
52 | J9              M6, polygon;       M5, same as "+" terminal.
53 | J10             M6, polygon;       M5, same as "+" terminal.
54 | J11             M6, polygon;       M5, same as "+" terminal.
55 | J12             M6, polygon;       M5, same as "+" terminal.
56 | J13             M6, polygon;       M5, same as "+" terminal.
57 | J14             M6, polygon;       M5, same as "+" terminal.
58 | J15             M6, polygon;       M5, same as "+" terminal.
59 | J16             M6, polygon;       M5, same as "+" terminal.
60 |
61 | SVD info: Condition nr. = 8.412; unknowns = 80; rank = 80.
62 |
63 | Impedance     Inductance [H]      Resistance [Ohm]      AbsDiff      PercDiff
64 | Name          Design            Extracted          Design          Extracted    (L only)      (L only)
65 | L1            --               1.60073E-12    --           --          +1.6007E-12  --%
66 | L2            2.23E-12        2.25151E-12    --           --          +2.1505E-14  +0.96436%
67 | L4            6.105E-12       6.11619E-12    --           --          +1.1188E-14  +0.18326%
68 | L5            1.2909E-12      1.29165E-12    --           --          +7.4642E-16  +0.057821%
69 | L6            2.58E-12         2.59574E-12    --           --          +1.574E-14   +0.61009%
70 | L7            1.1464E-12      1.159839E-12   --           --          +4.5199E-13  +39.427%

```

```

71 | L8      --      3.11847E-12 --      --      +3.1185E-12 --%
72 | L9      1.9428E-12 1.94567E-12 --      --      +2.8651E-15 +0.14747%
73 | L11     1.9932E-12 1.98734E-12 --      --      -5.8588E-15 -0.29394%
74 | L12     --      6.07532E-13 --      --      +6.0753E-13 --%
75 | L13     --      1.64628E-12 --      --      +1.6463E-12 --%
76 | L14     2.23E-12   2.22004E-12 --      --      -9.9623E-15 -0.44674%
77 | L16     6.105E-12   6.02447E-12 --      --      -8.0528E-14 -1.3191%
78 | L17     1.2909E-12 1.23479E-12 --      --      -5.6106E-14 -4.3463%
79 | L18     2.58E-12    2.59837E-12 --      --      +1.8368E-14 +0.71195%
80 | L19     1.1464E-12 1.159255E-12 --      --      +4.4615E-13 +38.918%
81 | L20     4E-13      8.96801E-13 --      --      +4.968E-13 +124.2%
82 | L22     2.925E-12   2.96832E-12 --      --      +4.3321E-14 +1.481%
83 | L23     4.644E-12   4.70343E-12 --      --      +5.943E-14 +1.2797%
84 | L24     --      2.59567E-12 --      --      +2.5957E-12 --%
85 | LB1    --      2.57564E-12 --      --      +2.5756E-12 --%
86 | LB2    --      4.95898E-12 --      --      +4.959E-12 --%
87 | LB3    --      8.25429E-13 --      --      +8.2543E-13 --%
88 | LB4    --      9.86159E-13 --      --      +9.8616E-13 --%
89 | LB5    --      2.61941E-12 --      --      +2.6194E-12 --%
90 | LB6    --      5.13694E-12 --      --      +5.1369E-12 --%
91 | LB7    --      8.14214E-13 --      --      +8.1421E-13 --%
92 | LB8    --      3.19526E-12 --      --      +3.1953E-12 --%
93 | LP1    --      5.35804E-13 --      --      +5.358E-13 --%
94 | LP2    --      5.41416E-13 --      --      +5.4142E-13 --%
95 | LP3    --      5.31678E-13 --      --      +5.3168E-13 --%
96 | LP6    --      5.4205E-13 --      --      +5.4205E-13 --%
97 | LP7    --      5.01792E-13 --      --      +5.0179E-13 --%
98 | LP8    --      5.52821E-13 --      --      +5.5282E-13 --%
99 | LP9    --      5.37028E-13 --      --      +5.3703E-13 --%
100 | LP10   --      5.37254E-13 --      --      +5.3725E-13 --%
101 | LP11   --      5.86571E-13 --      --      +5.8657E-13 --%
102 | LP14   --      5.36996E-13 --      --      +5.37E-13 --%
103 | LP15   --      5.39743E-13 --      --      +5.3974E-13 --%
104 | LP16   --      5.29126E-13 --      --      +5.2913E-13 --%
105
106 Ports   Design   Extracted  AbsDiff    PercDiff
107 J1      0.000088  0.000095735
108 J2      0.000176  0.00018464
109 J3      0.000132  0.00013971
110 J4      0.000113  0.00012116
111 J5      0.000153  0.00016161
112 J6      0.00009  0.00009764
113 J7      0.00015  0.00015829
114 J8      0.000117  0.0001249
115 J9      0.000088  0.000095735
116 J10     0.000176  0.00018464
117 J11     0.000132  0.00013971
118 J12     0.000113  0.00012116
119 J13     0.000153  0.00016161
120 J14     0.000126  0.00013429
121 J15     0.000204  0.00021285
122 J16     0.000227  0.00023609
123
124 Error bound on extracted values: 4.50093%
125
126 Deallocating memory.
127 Cycles found in 0.033 seconds.
128 SVD solution in 0.050 seconds.
129 Job finished in 410.701 seconds.

```

**Listing 4.22:** RSFQ AND2T InductEx extraction.

## Analog model

```

1  * Author: L. Schindler
2  * Version: 1.5.1
3  * Last modification date: 18 June 2020
4  * Last modification by: L. Schindler
5
6  *$Ports
7      a b clk
8      ↪ q
9 .subckt LSmitll_AND2T a b clk q
10 .model jjmit jj(rtype=1, vg=2.8mV, cap
11     ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
12     ↪ )
13 .param B0=1.0
14 .param Ic0=0.0001
15 .param IcRs=100u*6.859904418
16 .param B0Rs=IcRs/Ic0*B0
17 .param Rsheet=2
18 .param Lsheet=1.13e-12
19 .param B01=1.31899
20 .param B01rx2=0.88063
21 .param B01rx3=0.90139
22 .param B01tx1=2.26625
23 .param B03=1.13403
24 .param B05=1.52701
25 .param B07=1.25725
26 .param B08=1.56701
27 .param B09=2.03545
28 .param B10=1.75934
29 .param B14=1.50181
30 .param IB01=0.000113269
31 .param IB01rx2=0.000131447
32 .param IB01rx3=0.000127540
33 .param IB01tx1=0.000213665
34 .param IB03=0.000062676
35 .param IB07=0.000179300
36 .param L01=2.57966e-12
37 .param L01rx2=1.53695e-12
38 .param L01rx3=1.77460e-12
39 .param L01tx1=1.53695e-12
40 .param L02tx1=2.74282e-12
41 .param L03=1.93254e-12
42 .param L05=1.14641e-12
43 .param L07=1.99319e-12
44 .param L08=3.9e-14
45 .param L09=2.92475e-12
46 .param L13=2.23040e-12
47 .param L15=6.10490e-12
48 .param L17=1.94280e-12
49 .param L19=2.03734e-13
50 .param L20=3.99011e-13
51 .param L21=1.29090e-13
52 .param L23=1e-14
53 .param LRB01=(RB01/Rsheet)*Lsheet
54 .param LRB01rx2=(RB01rx2/Rsheet)*Lsheet
55 .param LRB01rx3=(RB01rx3/Rsheet)*Lsheet
56 .param LRB01tx1=(RB01tx1/Rsheet)*Lsheet
57 .param LRB03=(RB03/Rsheet)*Lsheet
58 .param LRB05=(RB05/Rsheet)*Lsheet
59 .param LRB07=(RB07/Rsheet)*Lsheet
60 .param LRB08=(RB08/Rsheet)*Lsheet
61 .param LRB09=(RB09/Rsheet)*Lsheet
62 .param LRB10=(RB10/Rsheet)*Lsheet
63 .param LRB14=(RB14/Rsheet)*Lsheet
64 .param RB03=B0Rs/B03
65 .param RB05=B0Rs/B05
66 .param RB07=B0Rs/B07
67 .param RB08=B0Rs/B08
68 .param RB09=B0Rs/B09
69 .param RB10=B0Rs/B10
70 .param RB14=B0Rs/B14
71 B01 7 32 jjmit area=B01
72 B01RX1 5 28 jjmit area=B01rx2
73 B01RX2 20 60 jjmit area=B01rx2
74 B01RX3 13 43 jjmit area=B01rx3
75 B01TX1 18 53 jjmit area=B01tx1
76 B02 22 64 jjmit area=B01
77 B03 8 10 jjmit area=B03
78 B04 23 19 jjmit area=B03
79 B05 9 11 jjmit area=B05
80 B06 24 11 jjmit area=B05
81 B07 16 49 jjmit area=B07
82 B08 15 47 jjmit area=B08
83 B09 17 51 jjmit area=B09
84 B10 6 30 jjmit area=B10
85 B11 21 62 jjmit area=B10
86 B14 14 45 jjmit area=B14
87 IB01 0 26 pw1(0 0 5p IB01)
88 IB01RX1 0 25 pw1(0 0 5p IB01rx2)
89 IB01RX2 0 55 pw1(0 0 5p IB01rx2)
90 IB01RX3 0 36 pw1(0 0 5p IB01rx3)
91 IB01TX1 0 39 pw1(0 0 5p IB01tx1)
92 IB02 0 56 pw1(0 0 5p IB01)
93 IB03 0 38 pw1(0 0 5p IB03)
94 IB07 0 37 pw1(0 0 5p IB07)
95 L01 8 9 L01
96 L01RX1 a 5 L01rx2
97 L01RX2 b 20 L01rx2
98 L01RX3 clk 13 L01rx3
99 L01TX1 17 18 L01tx1
100 L02 23 24 L01
101 L02TX1 18 42 L02tx1
102 L03 6 27 L03
103 L04 21 59 L03
104 L05 10 12 L05
105 L06 12 19 L05
106 L07 40 15 L07
107 L08 16 41 L08
108 L09 41 17 L09
109 L13 5 6 L13
110 L14 20 21 L13
111 L15 27 7 L15
112 L16 59 22 L15
113 L17 13 14 L17
114 L19 14 40 L19
115 L20 11 16 L20
116 L21 7 8 L21
117 L22 22 23 L21
118 L23 15 12 L23
119 LP01 32 0 2.55e-13
120 LP01RX1 28 0 3.4e-13
121 LP01RX2 60 0 3.4e-13
122 LP01RX3 43 0 3.4e-13
123 LP01TX1 53 0 5e-14
124 LP02 64 0 2.55e-13
125 LP07 49 0 2.99e-13
126 LP08 47 0 2.11e-13
127 LP09 51 0 1.74e-13
128 LP10 30 0 2.21e-13
129 LP11 62 0 2.21e-13

```

```

130 | LP14 45 0 1.87e-13
131 | LPR01RX1 25 5 2e-13
132 | LPR01RX2 55 20 2e-13
133 | LPR01RX3 36 13 2e-13
134 | LPR01TX1 39 18 2e-13
135 | LPR1 26 27 1.3e-14
136 | LPR2 56 59 1.3e-14
137 | LPR3 38 41 1.901e-12
138 | LPR4 37 40 8.5e-13
139 | LRB01 33 0 LRB01
140 | LRB01RX1 29 0 LRB01rx2
141 | LRB01RX2 61 0 LRB01rx2
142 | LRB01RX3 44 0 LRB01rx3
143 | LRB01TX1 54 0 LRB01tx1
144 | LRB02 65 0 LRB01
145 | LRB03 34 10 LRB03
146 | LRB04 19 57 LRB03
147 | LRB05 35 11 LRB05
148 | LRB06 11 58 LRB05
149 | LRB07 50 0 LRB07
150 | LRB08 48 0 LRB08
151 | LRB09 52 0 LRB09
152 | LRB10 31 0 LRB10
153 | LRB11 63 0 LRB10
154 | LRB14 46 0 LRB14
155 | RB01 7 33 RB01
156 | RB01RX1 5 29 RB01rx2
157 | RB01RX2 20 61 RB01rx2
158 | RB01RX3 13 44 RB01rx3
159 | RB01TX1 18 54 RB01tx1
160 | RB02 22 65 RB01
161 | RB03 8 34 RB03
162 | RB04 57 23 RB03
163 | RB05 9 35 RB05
164 | RB06 58 24 RB05
165 | RB07 16 50 RB07
166 | RB08 15 48 RB08
167 | RB09 17 52 RB09
168 | RB10 6 31 RB10
169 | RB11 21 63 RB10
170 | RB14 14 46 RB14
171 | RINSTX1 42 q 1.36
172 | .ends

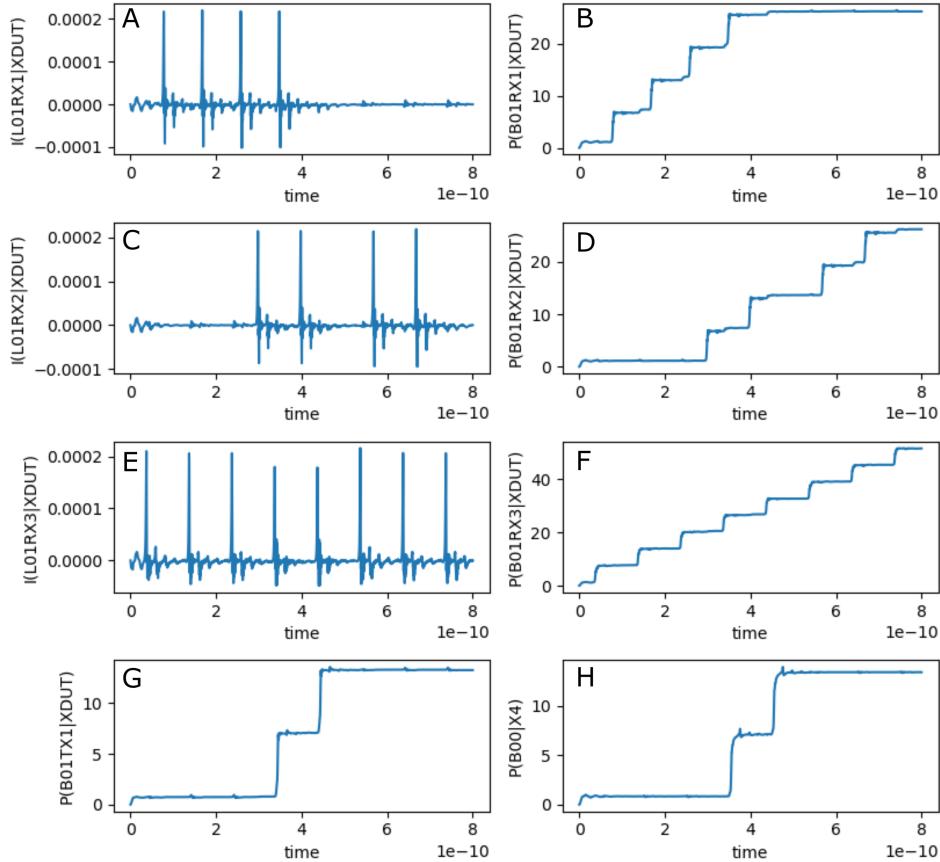
```

**Listing 4.23:** RSFQ AND2T JoSIM netlist.**Table 4.15:** RSFQ AND2T pin list.

Pin	Description
a	Data input
b	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ AND2T using JoSIM is shown in Fig. 4.38. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b**,
- (d) the phase over the input JJ of pin **b**,
- (e) the current through the input inductor connected to pin **clk**,
- (f) the phase over the input JJ of pin **clk**,
- (g) the phase over the output JJ of pin **q**, and
- (h) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.



**Figure 4.38:** RSFQ AND2T analog simulation results.

## Digital model

```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 // -----
9 `timescale 1ps/100fs
10 module LSmitll_AND2T_v1p5 (a, b, clk, q);
11
12 input
13   a, b, clk;
14
15 output
16   q;
17
18 reg
19   q;
20
21 real
22   delay_state3_clk_q = 7.0,
23   ct_state0_clk_a = 3.3,
24   ct_state0_clk_b = 3.3,
25   ct_state1_clk_a = 2.5,
26   ct_state1_clk_b = 2.8,
27   ct_state2_clk_a = 2.8,
28   ct_state2_clk_b = 2.5,
29   ct_state3_clk_a = 1.8,
30   ct_state3_clk_b = 1.5;
31
32 reg
33   errorsignal_a,
34   errorsignal_b,
35   errorsignal_clk;
36
37 integer
38   outfile,
39   cell_state; // internal state of the cell
40
41 initial
42 begin
43   errorsignal_a = 0;
44   errorsignal_b = 0;
45   errorsignal_clk = 0;
46   cell_state = 0; // Startup state
47   q = 0; // All outputs start at 0
48 end
49
50 always @(posedge a or negedge a) // execute at positive and negative edges of input
51 begin
52   if ($time>4) // arbitrary steady-state time)
53     begin
54       if (errorsignal_a == 1'b1) // A critical timing is active for this input
55         begin
56           outfile = $fopen("errors.txt", "a");
57           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m; %0d_ps.\n"
58           ↪ ", $stime);
59           $fclose(outfile);
60           q <= 1'bX; // Set all outputs to unknown
61         end
62       if (errorsignal_a == 0)
63         begin
64           case (cell_state)
65             0: begin
66               cell_state = 1; // Blocking statement -- immediately
67             end

```

```

67          1: begin
68              end
69          2: begin
70              cell_state = 3; // Blocking statement -- immediately
71              end
72          3: begin
73              end
74      endcase
75  end
76 end
77
78 always @(posedge b or negedge b) // execute at positive and negative edges of input
79 begin
80     if ($time>4) // arbitrary steady-state time)
81     begin
82         if (errorsignal_b == 1'b1) // A critical timing is active for this input
83         begin
84             outfile = $fopen("errors.txt", "a");
85             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
86             ↪ ", $stime);
87             $fclose(outfile);
88             q <= 1'bX; // Set all outputs to unknown
89         end
90     if (errorsignal_b == 0)
91     begin
92         case (cell_state)
93             0: begin
94                 cell_state = 2; // Blocking statement -- immediately
95                 end
96             1: begin
97                 cell_state = 3; // Blocking statement -- immediately
98                 end
99             2: begin
100                end
101            3: begin
102                end
103            endcase
104        end
105    end
106 end
107
108 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
109 begin
110     if ($time>4) // arbitrary steady-state time)
111     begin
112         if (errorsignal_clk == 1'b1) // A critical timing is active for this input
113         begin
114             outfile = $fopen("errors.txt", "a");
115             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
116             ↪ ", $stime);
117             $fclose(outfile);
118             q <= 1'bX; // Set all outputs to unknown
119         end
120     if (errorsignal_clk == 0)
121     begin
122         case (cell_state)
123             0: begin
124                 errorsignal_a = 1; // Critical timing on this input; assign
125                 ↪ immediately
126                 errorsignal_a <= #(ct_state0_clk_a) 0; // Clear error signal
127                 ↪ after critical timing expires
128                 errorsignal_b = 1; // Critical timing on this input; assign
129                 ↪ immediately
130                 errorsignal_b <= #(ct_state0_clk_b) 0; // Clear error signal
131                 ↪ after critical timing expires
132             end
133         begin
134             cell_state = 0; // Blocking statement -- immediately
135             errorsignal_a = 1; // Critical timing on this input; assign

```

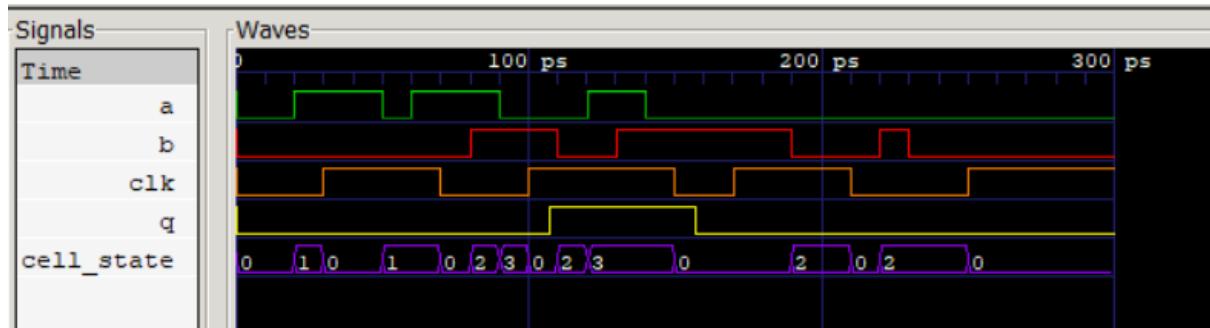
```

131           ↳ immediately
132           errorsignal_a <= #(ct_state1_clk_a) 0; // Clear error signal
133           ↳ after critical timing expires
134           errorsignal_b = 1; // Critical timing on this input; assign
135           ↳ immediately
136           errorsignal_b <= #(ct_state1_clk_b) 0; // Clear error signal
137           ↳ after critical timing expires
138       end
139   begin
140       cell_state = 0; // Blocking statement -- immediately
141       errorsignal_a = 1; // Critical timing on this input; assign
142           ↳ immediately
143           errorsignal_a <= #(ct_state2_clk_a) 0; // Clear error signal
144           ↳ after critical timing expires
145           errorsignal_b = 1; // Critical timing on this input; assign
146           ↳ immediately
147           errorsignal_b <= #(ct_state2_clk_b) 0; // Clear error signal
148           ↳ after critical timing expires
149       end
150   endcase
151 end
152 end
153
154 endmodule

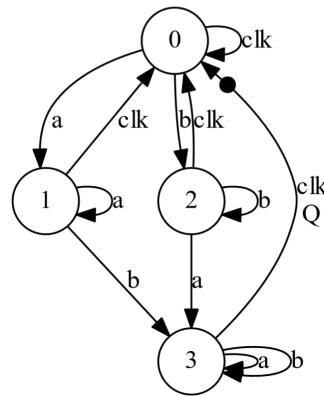
```

**Listing 4.24:** RSFQ AND2T verilog model.

The digital simulation results for the RSFQ AND2T is shown in Fig. 4.39 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.40.



**Figure 4.39:** RSFQ AND2T digital simulation results.



**Figure 4.40:** RSFQ AND2T Mealy finite state machine diagram.

## Power Consumption

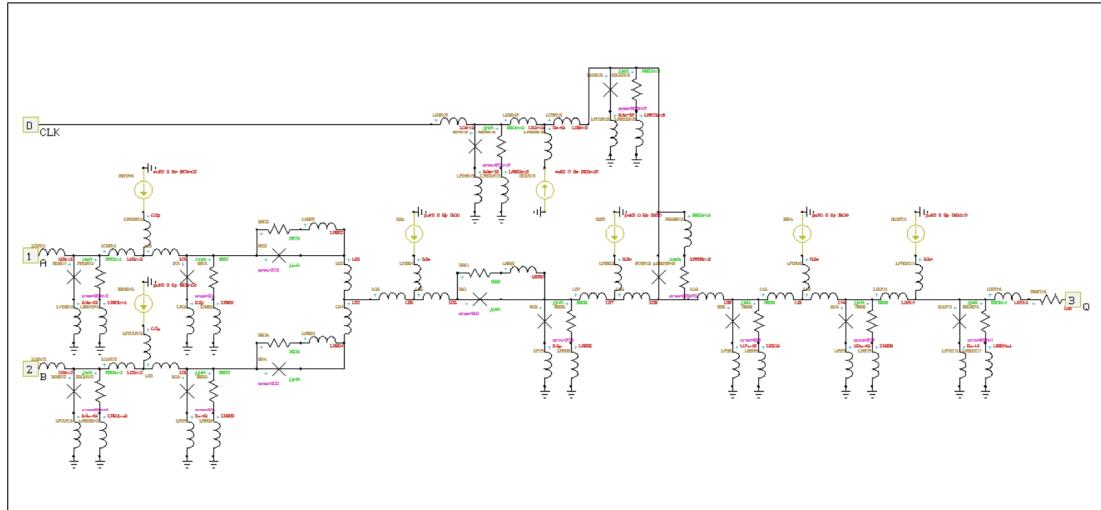
**Table 4.16:** RSFQ AND2T power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	279	4.71
2	279	9.42
5	279	23.5
10	279	47.1
20	279	94.2
50	279	235

### 4.2.2 OR2T

The RSFQ OR2T cell generates an output pulse if an input pulse from either input lines was received before the clock signal. The OR2T cell is designed with integrated PTL transmitters and receivers and is intended to be connected directly to a PTL.

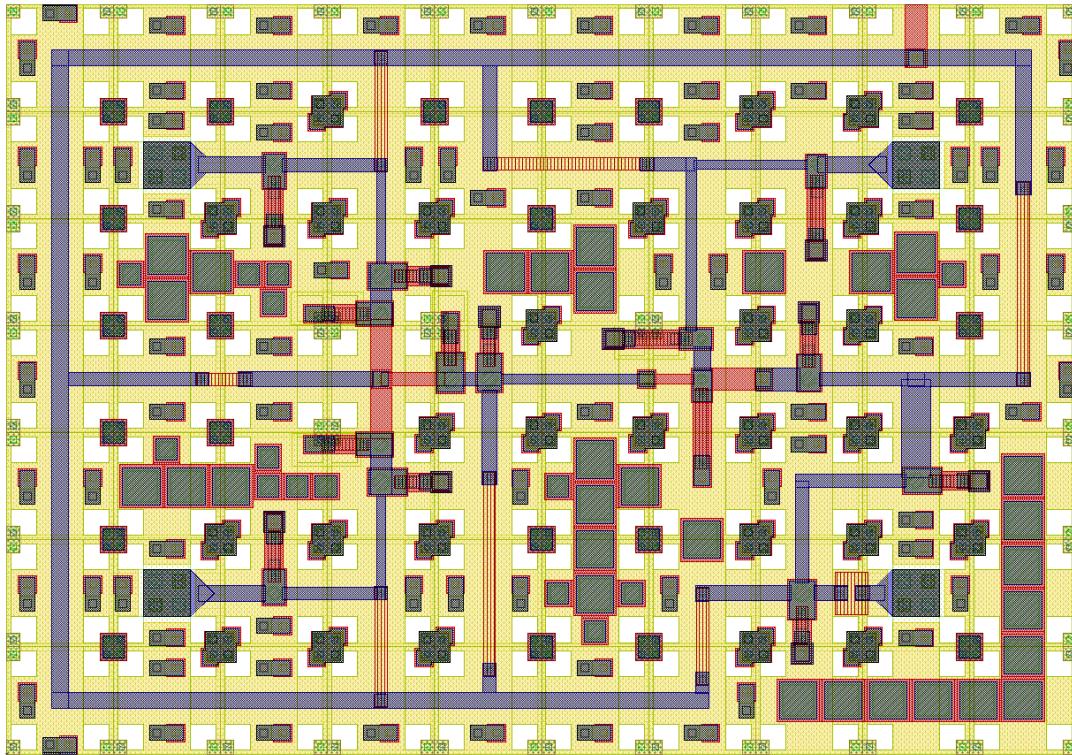
#### Schematic



**Figure 4.41:** Schematic of RSFQ OR2T.

## Layout

The physical layout for the RSFQ OR2T is shown in Fig. 4.42 and the resulting InductEx extraction is shown in Listing 4.25. The layout height is  $70 \mu m$  and the width is  $100 \mu m$ .



**Figure 4.42:** RSFQ OR2T Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_OR2T_v1p5.GDS -n LSmitll_OR2T_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_OR2T_v1p5_idx.cir read. Totals: L = 36, k = 0, P = 25.
7 | Total fundamental loops identified in netlist = 20
8 | Using TetraHenry with analytical integration.
9 | 3019 structures read. Reduced 3019 objects to 2798 polygons and 11 terminals.
10 | Top level structure is "LSMITLL_OR2T_V1P5".
11 | GDS file LSmitll_OR2T_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 | Port clk not in netlist. Ignored.
13 | Object in layer I5 moved to TERM layer. (Pj1)
14 | Object in layer I5 moved to TERM layer. (Pj2)
15 | Object in layer I5 moved to TERM layer. (Pj3)
16 | Object in layer I5 moved to TERM layer. (Pj4)
17 | Object in layer I5 moved to TERM layer. (Pj5)
18 | Object in layer I5 moved to TERM layer. (Pj6)
19 | Object in layer I5 moved to TERM layer. (Pj7)
20 | Object in layer I5 moved to TERM layer. (Pj8)
21 | Object in layer I5 moved to TERM layer. (Pj9)
22 | Object in layer I5 moved to TERM layer. (Pj10)
23 | Object in layer I5 moved to TERM layer. (Pj11)
24 | Object in layer I5 moved to TERM layer. (Pj12)
25 | Object in layer I5 moved to TERM layer. (Pj13)
26 | Object in layer I5 moved to TERM layer. (Pj14)
27 | Terminal blocks = 25; Labels = 26; Extracted Ports = 25
28 |
29 | Port           Positive terminal    Negative terminal
30 | P1             M6, line along y; M4, same as "+" terminal.
31 | P2             M6, line along y; M4, same as "+" terminal.
32 | P3             M6, line along y; M4, same as "+" terminal.
33 | P4             M6, polygon;      M4, same as "+" terminal.
34 | PB1            M6, polygon;      M4, same as "+" terminal.
35 | PB2            M6, polygon;      M4, same as "+" terminal.
36 | PB3            M6, polygon;      M4, same as "+" terminal.
37 | PB4            M6, polygon;      M4, same as "+" terminal.
38 | PB5            M6, polygon;      M4, same as "+" terminal.
39 | PB6            M6, polygon;      M4, same as "+" terminal.
40 | PB7            M6, polygon;      M4, same as "+" terminal.
41 | J1             M6, polygon;      M5, same as "+" terminal.
42 | J2             M6, polygon;      M5, same as "+" terminal.
43 | J3             M6, polygon;      M5, same as "+" terminal.
44 | J4             M6, polygon;      M5, same as "+" terminal.
45 | J5             M6, polygon;      M5, same as "+" terminal.
46 | J6             M6, polygon;      M5, same as "+" terminal.
47 | J7             M5, polygon;      M6, same as "+" terminal.
48 | J8             M6, polygon;      M5, same as "+" terminal.
49 | J9             M6, polygon;      M5, same as "+" terminal.
50 | J10            M6, polygon;      M5, same as "+" terminal.
51 | J11            M6, polygon;      M5, same as "+" terminal.
52 | J12            M6, polygon;      M5, same as "+" terminal.
53 | J13            M6, polygon;      M5, same as "+" terminal.
54 | J14            M6, polygon;      M5, same as "+" terminal.
55 |
56 | SVD info: Condition nr. = 15.36; unknowns = 72; rank = 72.
57 |
58 | Impedance     Inductance [H]       Resistance [Ohm]      AbsDiff      PercDiff
59 | Name          Design        Extracted      Design        Extracted      (L only)      (L only)
60 | L1            --           1.56576E-12  --           --           +1.5658E-12  --%
61 | L2            2.0822E-12  2.07611E-12  --           --           -6.0936E-15 -0.29265%
62 | L3            2.6809E-12  2.67435E-12  --           --           -6.5483E-15 -0.24426%
63 | L4            1.3486E-12  1.34248E-12  --           --           -6.1193E-15 -0.45375%
64 | L5            --           1.5833E-12   --           --           +1.5833E-12  --%
65 | L6            2.0822E-12  2.08865E-12  --           --           +6.4494E-15  +0.30974%
66 | L7            2.6809E-12  2.67708E-12  --           --           -3.8191E-15  -0.14246%
67 | L8            1.3486E-12  1.34422E-12  --           --           -4.3756E-15  -0.32445%
68 | L10           1.889E-12   1.87128E-12  --           --           -1.772E-14   -0.93806%
69 | L12           5.4916E-12  5.43634E-12  --           --           -5.5265E-14  -1.0063%
70 | L13           --           1.4674E-12   --           --           +1.4674E-12  --%

```

```

71 | L14      3.3652E-12  3.35955E-12  --      --      -5.65E-15   -0.1679%
72 | L15      4.0267E-12  3.98704E-12  --      --      -3.9664E-14  -0.98503%
73 | L16      --         5.9501E-13   --      --      +5.9501E-13   --%
74 | L17      1.5727E-12  1.5753E-12   --      --      +2.5958E-15  +0.16505%
75 | L18      2.0776E-12  2.05735E-12  --      --      -2.0246E-14  -0.97449%
76 | L19      8.85E-13    9.05707E-13  --      --      +2.0707E-14  +2.3397%
77 | L20      4.2904E-12  4.29095E-12  --      --      +5.5498E-16  +0.012935%
78 | L21      --         7.63945E-13  --      --      +7.6394E-13   --%
79 | LB1     --         2.75189E-13  --      --      +2.7519E-13   --%
80 | LB2     --         2.78685E-13  --      --      +2.7868E-13   --%
81 | LB3     --         2.83116E-12  --      --      +2.8312E-12   --%
82 | LB4     --         1.91903E-12  --      --      +1.919E-12    --%
83 | LB5     --         1.13608E-12  --      --      +1.1361E-12   --%
84 | LB6     --         2.21616E-12  --      --      +2.2162E-12   --%
85 | LB7     --         2.02089E-12  --      --      +2.0209E-12   --%
86 | LP1     --         4.89448E-13  --      --      +4.8945E-13   --%
87 | LP2     --         4.67731E-13  --      --      +4.6773E-13   --%
88 | LP4     --         4.85068E-13  --      --      +4.8507E-13   --%
89 | LP5     --         4.66522E-13  --      --      +4.6652E-13   --%
90 | LP8     --         5.07324E-13  --      --      +5.0732E-13   --%
91 | LP9     --         5.24369E-13  --      --      +5.2437E-13   --%
92 | LP10    --         5.47545E-13  --      --      +5.4754E-13   --%
93 | LP12    --         4.82536E-13  --      --      +4.8254E-13   --%
94 | LP13    --         5.2846E-13   --      --      +5.2846E-13   --%
95 | LP14    --         4.44578E-13  --      --      +4.4458E-13   --%
96
97 Ports      Design      Extracted      AbsDiff      PercDiff
98 J1          0.000117    0.0001249
99 J2          0.000195    0.00020358
100 J3         0.000131    0.00013903
101 J4         0.000117    0.0001249
102 J5         0.000195    0.00020358
103 J6         0.000131    0.00013903
104 J7         0.00022     0.00022853
105 J8         0.000172    0.00018001
106 J9         0.000081    0.000088493
107 J10        0.000075    0.000082555
108 J11        0.000063    0.000070413
109 J12        0.00014     0.00014826
110 J13        0.000162    0.00017055
111 J14        0.00019     0.0001986
112
113 Error bound on extracted values: 5.59447%
114
115 Deallocating memory.
116 Cycles found in 0.033 seconds.
117 SVD solution in 0.039 seconds.
118 Job finished in 440.152 seconds.

```

**Listing 4.25:** RSFQ OR2T InductEx extraction.

## Analog model

```

1  * Author: L. Schindler
2  * Version: 1.5.1
3  * Last modification date: 18 June 2020
4  * Last modification by: L. Schindler
5
6  *$Ports
7  .subckt LSmitll_OR2T a b clk q
8  .model jjmit jj(rtype=1, vg=2.8mV, cap
9    ↳ =0.07pF, r0=160, rn=16, icrit=0.1mA
10   ↳ )
11 .param B0=1
12 .param Ic0=0.0001
13 .param IcRs=100u*6.859904418
14 .param B0Rs=IcRs/Ic0*B0
15 .param Rsheet=2
16 .param Lsheet=1.13e-12
17 .param B01=1.9518
18 .param B01rx2=1.1720
19 .param B01rx3=0.8056
20 .param B01tx1=1.9004
21 .param B02=1.3074
22 .param B02rx3=0.7521
23 .param B03rx3=0.6339
24 .param B05=1.7221
25 .param B08=1.3953
26 .param B09=1.6170
27 .param B10=2.2048
28 .param IB01=0.0003277005
29 .param IB01rx2=0.0001412752
30 .param IB01rx3=9.8325e-05
31 .param IB01tx1=0.0001765029
32 .param IB02=8.1358e-05
33 .param IB04=8.0964e-05
34 .param L01=2.6809e-12
35 .param L01rx2=2.0307e-12
36 .param L01rx3=1.4136e-12
37 .param L01tx1=4.2904e-12
38 .param L02=1.3486e-12
39 .param L02rx2=2.0822e-12
40 .param L02rx3=3.3652e-12
41 .param L02tx1=2.7779e-12
42 .param L03rx3=4.0267e-12
43 .param L05=3.7250e-13
44 .param L06=1.8890e-12
45 .param L07=2.1922e-13
46 .param L08=5.4916e-12
47 .param L09=1.5727e-12
48 .param L13=2.0776e-12
49 .param L14=8.8496e-13
50 .param LRB01=(RB01/Rsheet)*Lsheet
51 .param LRB01rx1=(RB01rx1/Rsheet)*Lsheet
52 .param LRB01rx2=(RB01rx2/Rsheet)*Lsheet
53 .param LRB01rx3=(RB01rx3/Rsheet)*Lsheet
54 .param LRB01tx1=(RB01tx1/Rsheet)*Lsheet
55 .param LRB02=(RB02/Rsheet)*Lsheet
56 .param LRB02rx3=(RB02rx3/Rsheet)*Lsheet
57 .param LRB04=(RB04/Rsheet)*Lsheet
58 .param LRB05=(RB05/Rsheet)*Lsheet
59 .param LRB08=(RB08/Rsheet)*Lsheet
60 .param LRB09=(RB09/Rsheet)*Lsheet
61 .param LRB10=(RB10/Rsheet)*Lsheet
62 .param RB01=B0Rs/B01
63 .param RB01rx1=B0Rs/B01rx2
64 .param RB01rx2=B0Rs/B01rx2
65 .param RB01rx3=B0Rs/B01rx3
66 .param RB01tx1=B0Rs/B01tx1
67 .param RB02=B0Rs/B02
68 .param RB02rx3=B0Rs/B02rx3
69 .param RB03=B0Rs/B01
70 .param RB03rx3=B0Rs/B03rx3
71 .param RB04=B0Rs/B02
72 .param RB05=B0Rs/B05
73 .param RB08=B0Rs/B08
74 .param RB09=B0Rs/B09
75 .param RB10=B0Rs/B10
76 B01 7 36 jjmit area=B01
77 B01rx1 9 34 jjmit area=B01rx2
78 B01rx2 19 54 jjmit area=B01rx2
79 B01rx3 6 23 jjmit area=B01rx3
80 B01tx1 16 50 jjmit area=B01tx1
81 B02 7 8 jjmit area=B02
82 B02rx3 5 20 jjmit area=B02rx3
83 B03 17 56 jjmit area=B01
84 B03rx3 5 13 jjmit area=B03rx3
85 B04 17 18 jjmit area=B02
86 B05 11 44 jjmit area=B05
87 B08 14 46 jjmit area=B08
88 B09 15 48 jjmit area=B09
89 B10 10 11 jjmit area=B10
90 IB01 0 28 pw1(0 0 5p IB01)
91 IB01rx1 0 26 pw1(0 0 5p IB01rx2)
92 IB01rx2 0 42 pw1(0 0 5p IB01rx2)
93 IB01rx3 0 25 pw1(0 0 5p IB01rx3)
94 IB01tx1 0 32 pw1(0 0 5p IB01tx1)
95 IB02 0 29 pw1(0 0 5p IB02)
96 IB04 0 31 pw1(0 0 5p IB04)
97 L01 27 7 L01
98 L01rx1 a 9 L01rx2
99 L01rx2 b 19 L01rx2
100 L01rx3 clk 6 L01rx3
101 L01tx1 15 16 L01tx1
102 L02 8 12 L02
103 L02rx1 9 27 L02rx2
104 L02rx2 19 52 L02rx2
105 L02rx3 6 22 L02rx3
106 L02tx1 16 43 L02tx1
107 L03 52 17 L01
108 L03rx3 22 5 L03rx3
109 L04 12 18 L02
110 L05 12 38 L05
111 L06 38 10 L06
112 L07 11 39 L07
113 L08 39 13 L08
114 L09 13 14 L09
115 L13 14 40 L13
116 L14 40 15 L14
117 LP01 36 0 0.2p
118 LP01rx1 34 0 3.4e-13
119 LP01rx2 54 0 3.4e-13
120 LP01rx3 23 0 3.4e-13
121 LP01tx1 50 0 5e-14
122 LP02rx3 20 0 3.4e-13
123 LP03 56 0 2e-13
124 LP05 44 0 0.2p
125 LP08 46 0 1.17e-13
126 LP09 48 0 1.51e-13
127 LPIB01 28 38 0.2p
128 LPIB02 29 39 0.2p
129 LPIB04 31 40 0.2p
130 LPR01rx1 26 27 0.2p

```

```

131 | LPR01rx2 42 52 0.2p
132 | LPR01rx3 22 25 2e-13
133 | LPR01tx1 32 16 0.2p
134 | LRB01 37 0 LRB01
135 | LRB01rx1 35 0 LRB01rx1
136 | LRB01rx2 55 0 LRB01rx2
137 | LRB01rx3 24 0 LRB01rx3
138 | LRB01tx1 51 0 LRB01tx1
139 | LRB02 33 8 LRB02
140 | LRB02rx3 21 0 LRB02rx3
141 | LRB03 57 0 LRB03
142 | LRB03rx3 30 13 LRB03rx3
143 | LRB04 53 18 LRB04
144 | LRB05 45 0 LRB05
145 | LRB08 47 0 LRB08
146 | LRB09 49 0 LRB09
147 | LRB10 41 11 LRB10
148 | RB01 7 37 RB01
149 | RB01rx1 9 35 RB01rx1
150 | RB01rx2 19 55 RB01rx2
151 | RB01rx3 6 24 RB01rx3
152 | RB01tx1 16 51 RB01tx1
153 | RB02 7 33 RB02
154 | RB02rx3 5 21 RB02rx3
155 | RB03 17 57 RB03
156 | RB03rx3 5 30 RB03rx3
157 | RB04 17 53 RB04
158 | RB05 11 45 RB05
159 | RB08 14 47 RB08
160 | RB09 15 49 RB09
161 | RB10 10 41 RB10
162 | RINSTx1 43 q 1.36
163 | .ends

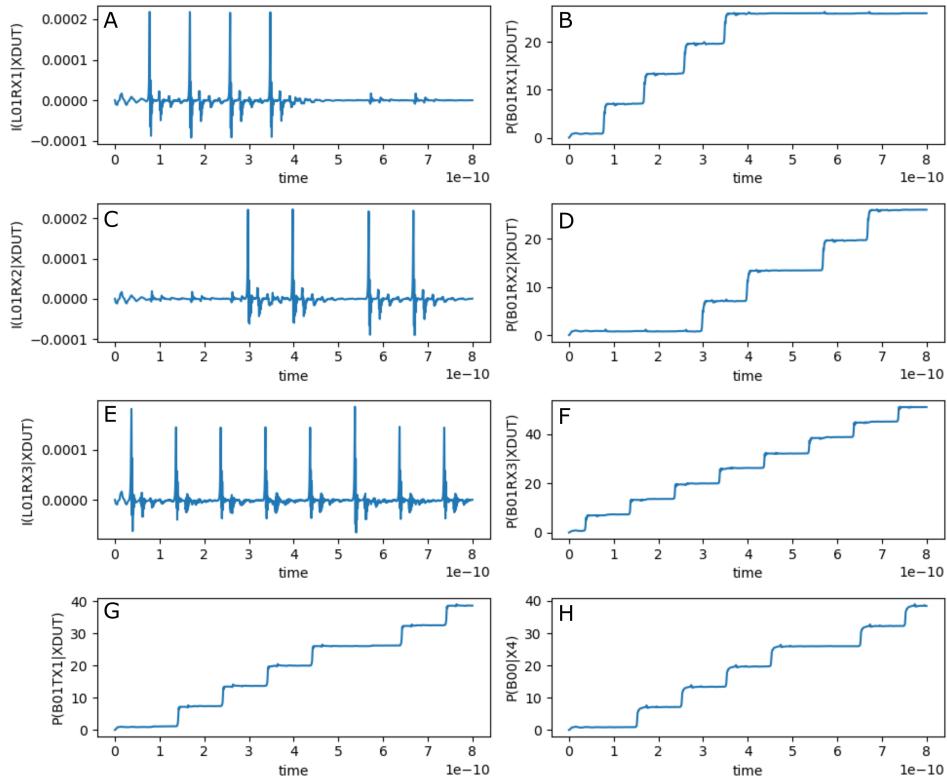
```

**Listing 4.26:** RSFQ OR2T JoSIM netlist.**Table 4.17:** RSFQ OR2T pin list.

Pin	Description
a	Data input
b	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ OR2T using JoSIM is shown in Fig. 4.43. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b**,
- (d) the phase over the input JJ of pin **b**,
- (e) the current through the input inductor connected to pin **clk**,
- (f) the phase over the input JJ of pin **clk**,
- (g) the phase over the output JJ of pin **q**, and
- (h) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.



**Figure 4.43:** RSFQ OR2T analog simulation results.

## Digital model

```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 // -----
9 `timescale 1ps/100fs
10 module LSmitll_OR2T_v1p5 (a, b, clk, q);
11
12 input
13   a, b, clk;
14 output
15   q;
16 reg
17   q;
18
19 real
20   delay_state1_clk_q = 5.5,
21   ct_state0_a_clk = 2.3,
22   ct_state0_b_clk = 2.3,
23   ct_state1_a_clk = 1.6,
24   ct_state1_b_clk = 1.6;
25
26 reg
27   errorsignal_a,
28   errorsignal_b,
29   errorsignal_clk;
30 integer
31   outfile,
32   cell_state; // internal state of the cell
33
34 initial
35 begin
36   errorsignal_a = 0;
37   errorsignal_b = 0;
38   errorsignal_clk = 0;
39   cell_state = 0; // Startup state
40   q = 0; // All outputs start at 0
41 end
42
43 always @(posedge a or negedge a) // execute at positive and negative edges of input
44 begin
45   if ($time>4) // arbitrary steady-state time)
46     begin
47       if (errorsignal_a == 1'b1) // A critical timing is active for this input
48         begin
49           outfile = $fopen("errors.txt", "a");
50           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
51           ↪ ", $stime);
52           $fclose(outfile);
53           q <= 1'bX; // Set all outputs to unknown
54         end
55       if (errorsignal_a == 0)
56         begin
57           case (cell_state)
58             0: begin
59               cell_state = 1; // Blocking statement -- immediately
60               errorsignal_clk = 1; // Critical timing on this input; assign
61               ↪ immediately
62               errorsignal_clk <= #(ct_state0_a_clk) 0; // Clear error signal
63               ↪ after critical timing expires
64             end
65           1: begin
66               errorsignal_clk = 1; // Critical timing on this input; assign
67               ↪ immediately
68             end
69           endcase
70         end
71       end
72     end
73   end
74 end
75
76 
```

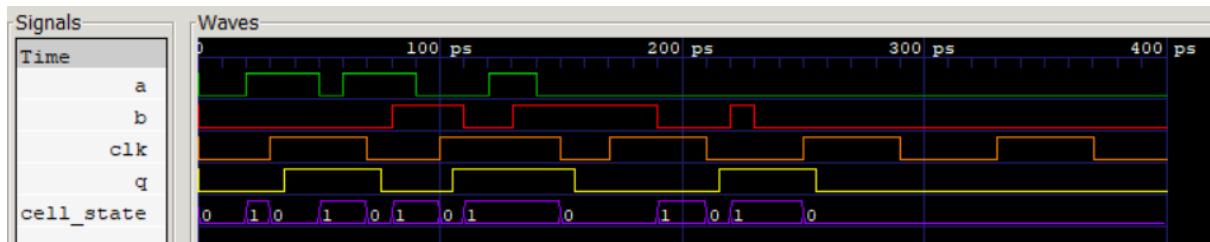
```

64           errorsignal_clk <= #(ct_state1_a_clk) 0; // Clear error signal
65           // after critical timing expires
66       end
67   endcase
68 end
69
70
71 always @(posedge b or negedge b) // execute at positive and negative edges of input
72 begin
73     if ($time>4) // arbitrary steady-state time)
74     begin
75         if (errorsignal_b == 1'b1) // A critical timing is active for this input
76         begin
77             outfile = $fopen("errors.txt", "a");
78             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n
79             ", $stime);
80             $fclose(outfile);
81             q <= 1'bX; // Set all outputs to unknown
82         end
83         if (errorsignal_b == 0)
84         begin
85             case (cell_state)
86             0: begin
87                 cell_state = 1; // Blocking statement -- immediately
88                 errorsignal_clk = 1; // Critical timing on this input; assign
89                 // immediately
90                 errorsignal_clk <= #(ct_state0_b_clk) 0; // Clear error signal
91                 // after critical timing expires
92             end
93             1: begin
94                 errorsignal_clk = 1; // Critical timing on this input; assign
95                 // immediately
96                 errorsignal_clk <= #(ct_state1_b_clk) 0; // Clear error signal
97                 // after critical timing expires
98             end
99         endcase
100    end
101
102 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
103 begin
104     if ($time>4) // arbitrary steady-state time)
105     begin
106         if (errorsignal_clk == 1'b1) // A critical timing is active for this input
107         begin
108             outfile = $fopen("errors.txt", "a");
109             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n
110             ", $stime);
111             $fclose(outfile);
112             q <= 1'bX; // Set all outputs to unknown
113         end
114         if (errorsignal_clk == 0)
115         begin
116             case (cell_state)
117             0: begin
118                 end
119             1: begin
120                 q <= #(delay_state1_clk_q) !q;
121                 cell_state = 0; // Blocking statement -- immediately
122             end
123         endcase
124     end
125 end
126
127 endmodule

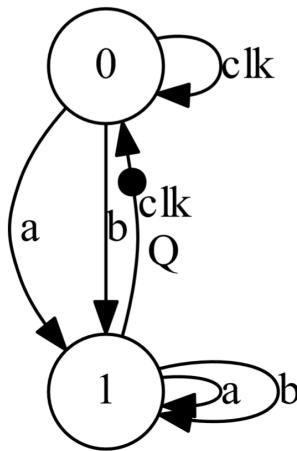
```

Listing 4.27: RSFQ OR2T verilog model.

The digital simulation results for the RSFQ OR2T is shown in Fig. 4.44 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.45.



**Figure 4.44:** RSFQ OR2T digital simulation results.



**Figure 4.45:** RSFQ OR2T Mealy finite state machine diagram.

## Power Consumption

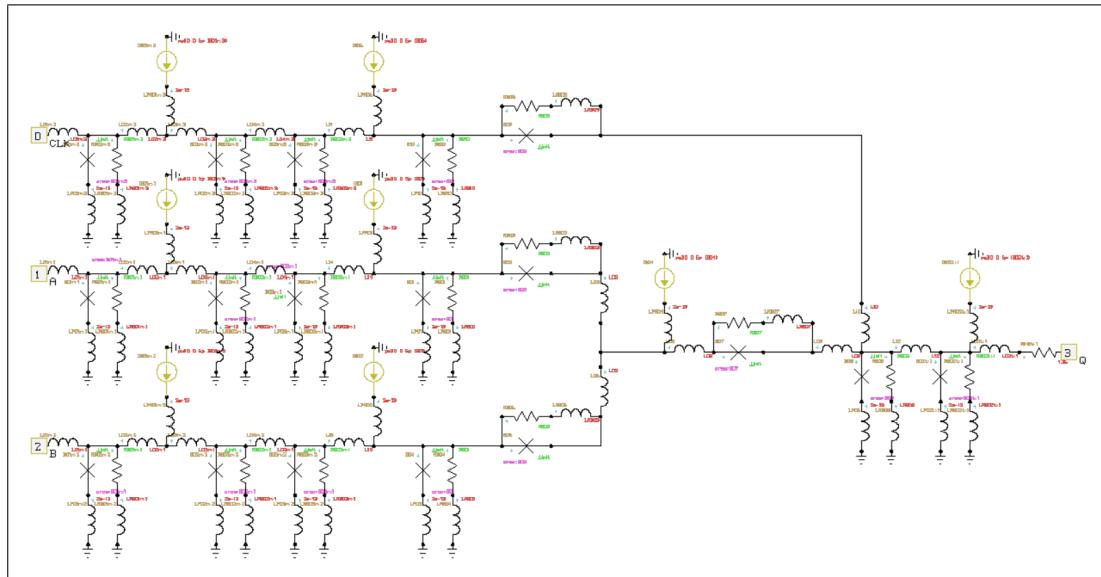
**Table 4.18:** RSFQ OR2T power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	272	4.11
2	272	8.23
5	272	20.6
10	272	41.1
20	272	82.3
50	272	206

### 4.2.3 XORT

The RSFQ XORT cell generates an output pulse exclusively if a pulse from a single input line was received before the clock signal. The XORT cell is designed with integrated PTL transmitters and receivers and is intended to be connected directly to a PTL.

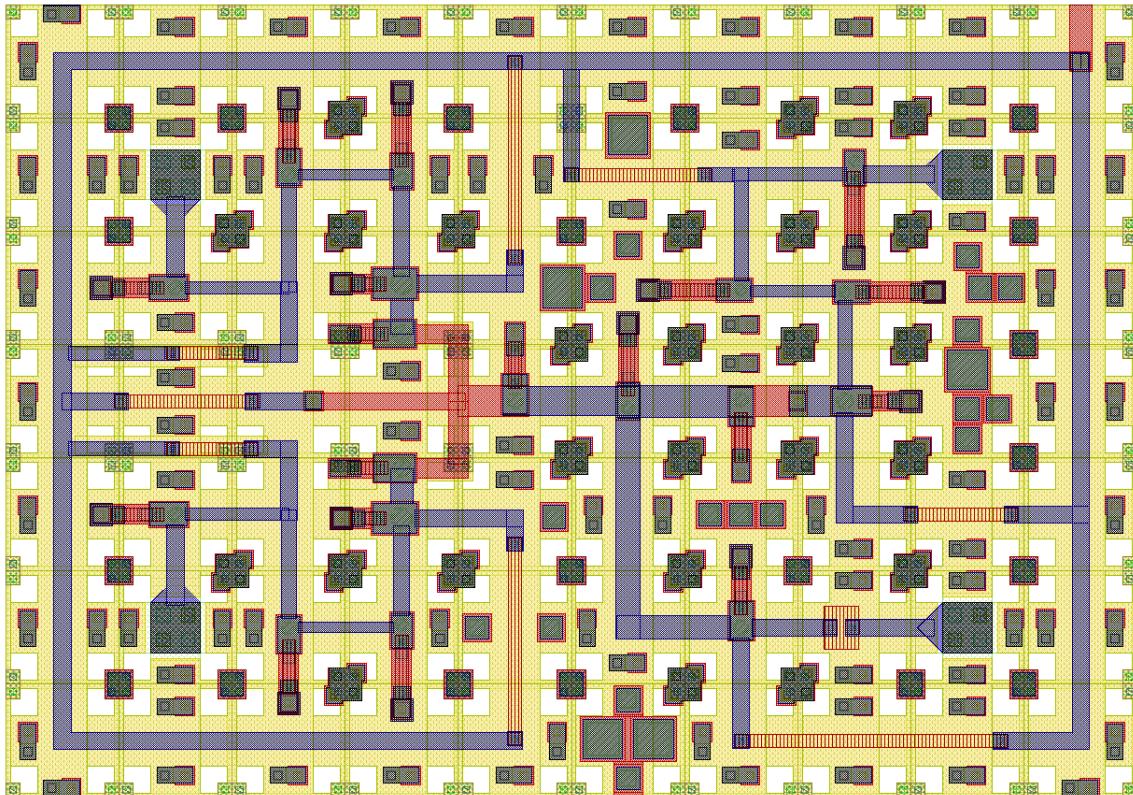
#### Schematic



**Figure 4.46:** Schematic of RSFQ XORT.

## Layout

The physical layout for the RSFQ XORT is shown in Fig. 4.47 and the resulting InductEx extraction is shown in Listing 4.28. The layout height is  $70 \mu\text{m}$  and the width is  $100 \mu\text{m}$ .



**Figure 4.47:** RSFQ XORT Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_XORT_v1p5.GDS -n LSmitll_XORT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_XORT_v1p5_idx.cir read. Totals: L = 43, k = 0, P = 30.
7 | Total fundamental loops identified in netlist = 25
8 | Using TetraHenry with analytical integration.
9 | 2972 structures read. Reduced 2972 objects to 2763 polygons and 12 terminals.
10 | Top level structure is "LSMITLL_XORT_V1P5".
11 | GDS file LSmitll_XORT_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 | Port clk not in netlist. Ignored.
13 | Object in layer I5 moved to TERM layer. (Pj1)
14 | Object in layer I5 moved to TERM layer. (Pj2)
15 | Object in layer I5 moved to TERM layer. (Pj3)
16 | Object in layer I5 moved to TERM layer. (Pj4)
17 | Object in layer I5 moved to TERM layer. (Pj5)
18 | Object in layer I5 moved to TERM layer. (Pj6)
19 | Object in layer I5 moved to TERM layer. (Pj7)
20 | Object in layer I5 moved to TERM layer. (Pj8)
21 | Object in layer I5 moved to TERM layer. (Pj9)
22 | Object in layer I5 moved to TERM layer. (Pj10)
23 | Object in layer I5 moved to TERM layer. (Pj11)
24 | Object in layer I5 moved to TERM layer. (Pj12)
25 | Object in layer I5 moved to TERM layer. (Pj13)
26 | Object in layer I5 moved to TERM layer. (Pj14)
27 | Object in layer I5 moved to TERM layer. (Pj15)
28 | Object in layer I5 moved to TERM layer. (Pj16)

```

```

29 | Object in layer I5 moved to TERM layer. (Pj17)
30 | Object in layer I5 moved to TERM layer. (Pj18)
31 | Terminal blocks = 30; Labels = 31; Extracted Ports = 30
32 |
33 | Port           Positive terminal    Negative terminal
34 | P1             M6, line along x;   M4, same as "+" terminal.
35 | P2             M6, line along x;   M4, same as "+" terminal.
36 | P3             M6, line along y;   M4, same as "+" terminal.
37 | P4             M6, polygon;       M4, same as "+" terminal.
38 | PB1            M6, polygon;       M4, same as "+" terminal.
39 | PB2            M6, polygon;       M4, same as "+" terminal.
40 | PB3            M6, polygon;       M4, same as "+" terminal.
41 | PB4            M6, polygon;       M4, same as "+" terminal.
42 | PB5            M6, polygon;       M4, same as "+" terminal.
43 | PB6            M6, polygon;       M4, same as "+" terminal.
44 | PB7            M6, polygon;       M4, same as "+" terminal.
45 | PB8            M6, polygon;       M4, same as "+" terminal.
46 | J1              M6, polygon;      M5, same as "+" terminal.
47 | J2              M6, polygon;      M5, same as "+" terminal.
48 | J3              M6, polygon;      M5, same as "+" terminal.
49 | J4              M6, polygon;      M5, same as "+" terminal.
50 | J5              M6, polygon;      M5, same as "+" terminal.
51 | J6              M6, polygon;      M5, same as "+" terminal.
52 | J7              M6, polygon;      M5, same as "+" terminal.
53 | J8              M6, polygon;      M5, same as "+" terminal.
54 | J9              M6, polygon;      M5, same as "+" terminal.
55 | J10             M6, polygon;      M5, same as "+" terminal.
56 | J11             M6, polygon;      M5, same as "+" terminal.
57 | J12             M6, polygon;      M5, same as "+" terminal.
58 | J13             M6, polygon;      M5, same as "+" terminal.
59 | J14             M6, polygon;      M5, same as "+" terminal.
60 | J15             M5, polygon;      M6, same as "+" terminal.
61 | J16             M5, polygon;      M6, same as "+" terminal.
62 | J17             M6, polygon;      M5, same as "+" terminal.
63 | J18             M6, polygon;      M5, same as "+" terminal.
64 |
65 | SVD info: Condition nr. = 5.664; unknowns = 86; rank = 86.
66 |
67 | Impedance      Inductance [H]      Resistance [Ohm]      AbsDiff      PercDiff
68 | Name           Design          Extracted        Design          Extracted    (L only)      (L only)
69 | L1              --              1.43366E-12    --              --          +1.4337E-12  --%
70 | L2              2.1529E-12     2.15066E-12    --              --          -2.2382E-15 -0.10396%
71 | L3              1.9729E-12     1.95185E-12    --              --          -2.1048E-14 -1.0669%
72 | L4              2.3966E-12     2.38059E-12    --              --          -1.6015E-14 -0.66823%
73 | L5              1.6354E-12     1.63433E-12    --              --          -1.0673E-15 -0.065261%
74 | L6              2.2793E-12     2.27355E-12    --              --          -5.75E-15   -0.25227%
75 | L7              --              1.4265E-12     --              --          +1.4265E-12  --%
76 | L8              2.1529E-12     2.15169E-12    --              --          -1.2074E-15 -0.056081%
77 | L9              1.9729E-12     1.9544E-12     --              --          -1.8502E-14 -0.93781%
78 | L10             2.3966E-12     2.3794E-12     --              --          -1.7199E-14 -0.71765%
79 | L11             1.6354E-12     1.63063E-12    --              --          -4.7737E-15 -0.2919%
80 | L12             2.2793E-12     2.27042E-12    --              --          -8.8785E-15 -0.38953%
81 | L13             --              1.57592E-12    --              --          +1.5759E-12  --%
82 | L14             2.2381E-12     2.25047E-12    --              --          +1.2371E-14  +0.55277%
83 | L15             2.0205E-12     2.00348E-12    --              --          -1.7017E-14 -0.84223%
84 | L16             2.0178E-12     2.02314E-12    --              --          +5.3403E-15 +0.26466%
85 | L17             1.8033E-12     1.78416E-12    --              --          -1.9137E-14 -1.0612%
86 | L18             2.2246E-12     2.18833E-12    --              --          -3.6268E-14 -1.6303%
87 | L19             1.7515E-12     1.75481E-12    --              --          +3.3059E-15 +0.18874%
88 | L20             3.8658E-12     3.88399E-12    --              --          +1.8187E-14 +0.47045%
89 | L21             --              1.59174E-12    --              --          +1.5917E-12  --%
90 | LP1             --              5.19299E-13    --              --          +5.193E-13   --%
91 | LP2             --              5.79257E-13    --              --          +5.7926E-13  --%
92 | LP3             --              5.76642E-13    --              --          +5.7664E-13  --%
93 | LP4             --              4.79876E-13    --              --          +4.7988E-13  --%
94 | LP6             --              5.2107E-13     --              --          +5.2107E-13  --%
95 | LP7             --              5.75992E-13    --              --          +5.7599E-13  --%
96 | LP8             --              5.77165E-13    --              --          +5.7716E-13  --%
97 | LP9             --              4.781E-13      --              --          +4.781E-13   --%
98 | LP11            --              5.184E-13      --              --          +5.184E-13   --%

```

```

99 | LP12    --      6.01266E-13 --      --      +6.0127E-13 --%
100 | LP13    --      5.96996E-13 --      --      +5.97E-13  --%
101 | LP14    --      5.27298E-13 --      --      +5.273E-13 --%
102 | LP17    --      5.93281E-13 --      --      +5.9328E-13 --%
103 | LP18    --      5.33178E-13 --      --      +5.3318E-13 --%
104 | LB1     --      1.86465E-12 --      --      +1.8647E-12 --%
105 | LB2     --      2.30401E-12 --      --      +2.304E-12  --%
106 | LB3     --      1.86071E-12 --      --      +1.8607E-12 --%
107 | LB4     --      2.29666E-12 --      --      +2.2967E-12 --%
108 | LB5     --      9.22503E-13 --      --      +9.225E-13  --%
109 | LB6     --      2.91768E-12 --      --      +2.9177E-12 --%
110 | LB7     --      4.09282E-12 --      --      +4.0928E-12 --%
111 | LB8     --      2.01676E-12 --      --      +2.0168E-12 --%
112 |
113 | Ports   Design   Extracted AbsDiff   PercDiff
114 | J1      0.000121  0.00012895
115 | J2      0.000116  0.00012397
116 | J3      0.00009   0.00009764
117 | J4      0.00028   0.00028898
118 | J5      0.000192  0.00020036
119 | J6      0.000121  0.00012895
120 | J7      0.000116  0.00012397
121 | J8      0.00009   0.00009764
122 | J9      0.00028   0.00028898
123 | J10     0.000192  0.00020036
124 | J11     0.000072  0.00007941
125 | J12     0.000077  0.000084655
126 | J13     0.000083  0.0000907
127 | J14     0.000169  0.00017758
128 | J15     0.000129  0.00013711
129 | J16     0.000149  0.00015691
130 | J17     0.000093  0.00010059
131 | J18     0.000137  0.00014499
132 |
133 | Error bound on extracted values: 2.47313%
134 |
135 | Deallocating memory.
136 | Cycles found in 0.031 seconds.
137 | SVD solution in 0.048 seconds.
138 | Job finished in 558.757 seconds.

```

**Listing 4.28:** RSFQ XORT InductEx extraction.

## Analog model

```

1  * Author: L. Schindler
2  * Version: 1.5.1
3  * Last modification date: 18 June 2020
4  * Last modification by: L. Schindler
5
6  *$Ports
7  .subckt LSmitll_XORT a b clk q
8  .model jjmit jj(rtype=1, vg=2.8mV, cap
9    ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
10   ↪ )
11 .param B0=1
12 .param Ic0=0.0001
13 .param IcRs=100u*6.859904418
14 .param B0Rs=IcRs/Ic0*B0
15 .param Rsheet=2
16 .param Lsheet=1.13e-12
17 .param B01=2.7984
18 .param B01rx1=1.2124
19 .param B01rx3=0.7236
20 .param B02rx1=1.1586
21 .param B02rx3=0.7720
22 .param B02tx1=1.3695
23 .param B03=1.9159
24 .param B03rx1=0.8978
25 .param B03rx3=0.8280
26 .param B07=1.4857
27 .param B08=0.9336
28 .param B09=1.2859
29 .param B10=1.6863
30 .param IB01=8.9218e-05
31 .param IB01rx1=0.000229789
32 .param IB01rx3=0.000131858
33 .param IB02tx1=6.64568e-05
34 .param IB04=0.000134046
35 .param IB05=0.000177629
36 .param L01rx1=1.8604e-12
37 .param L01rx3=1.8928e-12
38 .param L02rx1=2.1529e-12
39 .param L02rx3=2.2381e-12
40 .param L03=2.2793e-12
41 .param L03rx1=1.9729e-12
42 .param L03rx3=2.0205e-12
43 .param L03tx1=2.2261e-12
44 .param L04rx1=2.3966e-12
45 .param L04rx3=2.0178e-12
46 .param L08=1.7515e-12
47 .param L09=1.2620e-12
48 .param L10=2.2246e-12
49 .param L11=1.8033e-12
50 .param L12=3.8658e-12
51 .param L14=1.6354e-12
52 .param LRB01=(RB01/Rsheet)*Lsheet
53 .param LRB01rx1=(RB01rx1/Rsheet)*Lsheet
54 .param LRB01rx3=(RB01rx3/Rsheet)*Lsheet
55 .param LRB02rx1=(RB02rx1/Rsheet)*Lsheet
56 .param LRB02rx3=(RB02rx3/Rsheet)*Lsheet
57 .param LRB03rx1=(RB03rx1/Rsheet)*Lsheet
58 .param LRB03rx3=(RB03rx3/Rsheet)*Lsheet
59 .param LRB07=(RB07/Rsheet)*Lsheet
60 .param LRB08=(RB08/Rsheet)*Lsheet
61 .param LRB09=(RB09/Rsheet)*Lsheet
62 .param LRB10=(RB10/Rsheet)*Lsheet
63 .param RB01=B0Rs/B01
64 .param RB01rx1=B0Rs/B01rx1
65 .param RB01rx3=B0Rs/B01rx3
66 .param RB02rx1=B0Rs/B02rx1
67 .param RB02rx3=B0Rs/B02rx3
68 .param RB02tx1=B0Rs/B02tx1
69 .param RB03=B0Rs/B03
70 .param RB03rx1=B0Rs/B03rx1
71 .param RB03rx3=B0Rs/B03rx3
72 .param RB07=B0Rs/B07
73 .param RB08=B0Rs/B08
74 .param RB09=B0Rs/B09
75 .param RB10=B0Rs/B10
76 B01 10 49 jjmit area=B01
77 B01rx1 12 43 jjmit area=B01rx1
78 B01rx2 22 61 jjmit area=B01rx3
79 B01rx3 7 29 jjmit area=B01rx3
80 B02rx1 13 45 jjmit area=B02rx1
81 B02rx2 23 63 jjmit area=B02rx1
82 B02rx3 8 31 jjmit area=B02rx3
83 B02tx1 19 57 jjmit area=B02tx1
84 B03 10 11 jjmit area=B03
85 B03rx1 14 47 jjmit area=B03rx1
86 B03rx2 24 65 jjmit area=B03rx1
87 B03rx3 9 33 jjmit area=B03rx3
88 B04 20 67 jjmit area=B01
89 B06 20 21 jjmit area=B03
90 B07 16 17 jjmit area=B07
91 B08 18 55 jjmit area=B08
92 B09 5 6 jjmit area=B09
93 B10 5 35 jjmit area=B10
94 IB01 0 38 pwl(0 0 5p IB01)
95 IB01rx1 0 37 pwl(0 0 5p IB01rx1)
96 IB01rx2 0 53 pwl(0 0 5p IB01rx1)
97 IB01rx3 0 25 pwl(0 0 5p IB01rx3)
98 IB02 0 54 pwl(0 0 5p IB01)
99 IB02tx1 0 42 pwl(0 0 5p IB02tx1)
100 IB04 0 41 pwl(0 0 5p IB04)
101 IB05 0 26 pwl(0 0 5p IB05)
102 L01rx1 a 12 L01rx1
103 L01rx2 b 22 L01rx1
104 L01rx3 clk 7 L01rx3
105 L02rx1 12 39 L02rx1
106 L02rx2 22 59 L02rx1
107 L02rx3 7 27 L02rx3
108 L03 11 15 L03
109 L03rx1 39 13 L03rx1
110 L03rx2 59 23 L03rx1
111 L03rx3 27 8 L03rx3
112 L03tx1 19 52 L03tx1
113 L04rx1 13 14 L04rx1
114 L04rx2 23 24 L04rx1
115 L04rx3 8 9 L04rx3
116 L06 15 21 L03
117 L08 15 16 L08
118 L09 17 18 L09
119 L10 6 18 L10
120 L11 9 5 L11
121 L12 18 19 L12
122 L14 14 10 L14
123 L15 24 20 L14
124 LP01 49 0 2e-13
125 LP01rx1 43 0 2e-13
126 LP01rx2 61 0 2e-13
127 LP01rx3 29 0 2e-13
128 LP02rx1 45 0 2e-13
129 LP02rx2 63 0 2e-13
130 LP02rx3 31 0 2e-13

```

```

131 | LP02tx1 57 0 2e-13          159 | LRB06 60 21 LRB03
132 | LP03 67 0 2e-13           160 | LRB07 51 17 LRB07
133 | LP03rx1 47 0 2e-13          161 | LRB08 56 0 LRB08
134 | LP03rx2 65 0 2e-13          162 | LRB09 28 6 LRB09
135 | LP03rx3 33 0 2e-13          163 | LRB10 36 0 LRB10
136 | LP05 55 0 2e-13           164 | RB01 10 50 RB01
137 | LP10 35 0 2e-13           165 | RB01rx1 12 44 RB01rx1
138 | LPR01 38 10 2e-13          166 | RB01rx2 22 62 RB01rx1
139 | LPR01rx1 37 39 2e-13        167 | RB01rx3 7 30 RB01rx3
140 | LPR01rx2 53 59 2e-13        168 | RB02rx1 13 46 RB02rx1
141 | LPR01rx3 25 27 2e-13        169 | RB02rx2 23 64 RB02rx1
142 | LPR02 54 20 2e-13          170 | RB02rx3 8 32 RB02rx3
143 | LPR02tx1 42 19 2e-13        171 | RB02tx1 19 58 RB02tx1
144 | LPR04 41 15 2e-13          172 | RB03 10 40 RB03
145 | LPR05 26 5 2e-13           173 | RB03rx1 14 48 RB03rx1
146 | LRB01 50 0 LRB01           174 | RB03rx2 24 66 RB03rx1
147 | LRB01rx1 44 0 LRB01rx1       175 | RB03rx3 9 34 RB03rx3
148 | LRB01rx2 62 0 LRB01rx1       176 | RB04 20 68 RB01
149 | LRB01rx3 30 0 LRB01rx3       177 | RB06 20 60 RB03
150 | LRB02rx1 46 0 LRB02rx1       178 | RB07 16 51 RB07
151 | LRB02rx2 64 0 LRB02rx1       179 | RB08 18 56 RB08
152 | LRB02rx3 32 0 LRB02rx3       180 | RB09 5 28 RB09
153 | LRB02tx1 58 0 LRB02tx1       181 | RB10 5 36 RB10
154 | LRB03 40 11 LRB03           182 | RINSTx1 52 q 1.36
155 | LRB03rx1 48 0 LRB03rx1       183 | .ends
156 | LRB03rx2 66 0 LRB03rx1
157 | LRB03rx3 34 0 LRB03rx3
158 | LRB04 68 0 LRB01

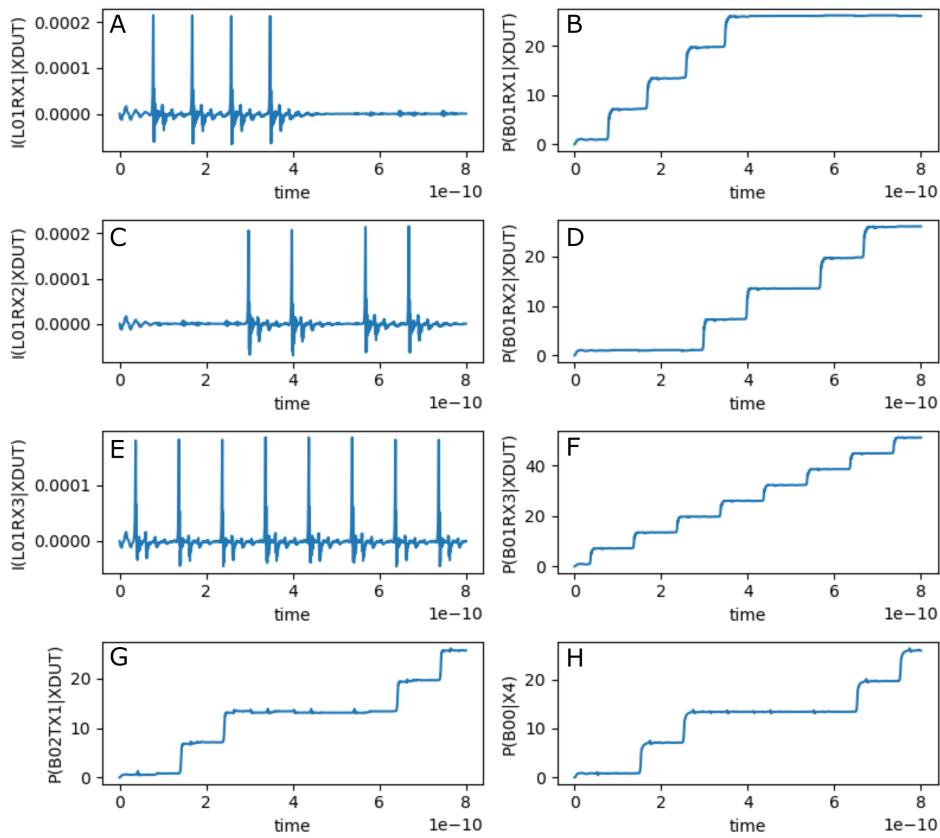
```

**Listing 4.29:** RSFQ XORT JoSIM netlist.**Table 4.19:** RSFQ XORT pin list.

Pin	Description
<b>a</b>	Data input
<b>b</b>	Data input
<b>clk</b>	Clock input
<b>q</b>	Data output

The simulation results for the RSFQ XORT using JoSIM is shown in Fig. 4.48. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b**,
- (d) the phase over the input JJ of pin **b**,
- (e) the current through the input inductor connected to pin **clk**,
- (f) the phase over the input JJ of pin **clk**,
- (g) the phase over the output JJ of pin **q**, and
- (h) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.



**Figure 4.48:** RSFQ XORT analog simulation results.

## Digital model

```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 // -----
9 `timescale 1ps/100fs
10 module LSmitll_XORT_v1p5 (a, b, clk, q);
11
12 input
13   a, b, clk;
14
15 output
16   q;
17
18 reg
19   q;
20
21 real
22   delay_state1_clk_q = 5.2,
23   delay_state2_clk_q = 5.2,
24   ct_state0_a_clk = 2.5,
25   ct_state0_b_clk = 2.5,
26   ct_state1_a_b = 12.5,
27   ct_state1_a_clk = 15.0,
28   ct_state1_b_b = 3.3,
29   ct_state1_clk_b = 3.8,
30   ct_state2_a_a = 3.3,
31   ct_state2_b_a = 12.5,
32   ct_state2_b_clk = 15.0,
33   ct_state2_clk_a = 3.8;
34
35 reg
36   errorsignal_a,
37   errorsignal_b,
38   errorsignal_clk;
39
40 integer
41   outfile,
42   cell_state; // internal state of the cell
43
44 initial
45 begin
46   errorsignal_a = 0;
47   errorsignal_b = 0;
48   errorsignal_clk = 0;
49   cell_state = 0; // Startup state
50   q = 0; // All outputs start at 0
51 end
52
53 always @(posedge a or negedge a) // execute at positive and negative edges of input
54 begin
55   if ($time>4) // arbitrary steady-state time)
56     begin
57       if (errorsignal_a == 1'b1) // A critical timing is active for this input
58         begin
59           outfile = $fopen("errors.txt", "a");
60           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m; %0d_ps.\n"
61           ↪ ", $stime);
62           $fclose(outfile);
63           q <= 1'bX; // Set all outputs to unknown
64         end
65       if (errorsignal_a == 0)
66         begin
67           case (cell_state)

```

```

67      0: begin
68          cell_state = 1; // Blocking statement -- immediately
69          errorsignal_clk = 1; // Critical timing on this input; assign
70          ↪ immediately
71          errorsignal_clk <= #(ct_state0_a_clk) 0; // Clear error signal
72          ↪ after critical timing expires
73      end
74      1: begin
75          errorsignal_b = 1; // Critical timing on this input; assign
76          ↪ immediately
77          errorsignal_b <= #(ct_state1_a_b) 0; // Clear error signal
78          ↪ after critical timing expires
79          errorsignal_clk = 1; // Critical timing on this input; assign
80          ↪ immediately
81          errorsignal_clk <= #(ct_state1_a_clk) 0; // Clear error signal
82          ↪ after critical timing expires
83      end
84      2: begin
85          cell_state = 0; // Blocking statement -- immediately
86          errorsignal_a = 1; // Critical timing on this input; assign
87          ↪ immediately
88          errorsignal_a <= #(ct_state2_a_a) 0; // Clear error signal
89          ↪ after critical timing expires
90      end
91  endcase
92 end
93
94 always @(posedge b or negedge b) // execute at positive and negative edges of input
95 begin
96     if ($time>4) // arbitrary steady-state time)
97     begin
98         if (errorsignal_b == 1'b1) // A critical timing is active for this input
99         begin
100             outfile = $fopen("errors.txt", "a");
101             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n
102             ↪ ", $stime);
103             $fclose(outfile);
104             q <= 1'bX; // Set all outputs to unknown
105         end
106         if (errorsignal_b == 0)
107         begin
108             case (cell_state)
109             0: begin
110                 cell_state = 2; // Blocking statement -- immediately
111                 errorsignal_clk = 1; // Critical timing on this input; assign
112                 ↪ immediately
113                 errorsignal_clk <= #(ct_state0_b_clk) 0; // Clear error signal
114                 ↪ after critical timing expires
115             end
116             1: begin
117                 cell_state = 0; // Blocking statement -- immediately
118                 errorsignal_b = 1; // Critical timing on this input; assign
119                 ↪ immediately
120                 errorsignal_b <= #(ct_state1_b_b) 0; // Clear error signal
121                 ↪ after critical timing expires
122             end
123             2: begin
124                 errorsignal_a = 1; // Critical timing on this input; assign
125                 ↪ immediately
126                 errorsignal_a <= #(ct_state2_b_a) 0; // Clear error signal
127                 ↪ after critical timing expires
128                 errorsignal_clk = 1; // Critical timing on this input; assign
129                 ↪ immediately
130                 errorsignal_clk <= #(ct_state2_b_clk) 0; // Clear error signal
131                 ↪ after critical timing expires
132             end
133         endcase
134     end
135 
```

```

120      end
121  end
122
123  always @(posedge clk or negedge clk) // execute at positive and negative edges of input
124    begin
125      if ($time>4) // arbitrary steady-state time)
126        begin
127          if (errorsignal_clk == 1'b1) // A critical timing is active for this input
128            begin
129              outfile = $fopen("errors.txt", "a");
130              $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
131                         ↪ ", $stime);
132              $fclose(outfile);
133              q <= 1'bX; // Set all outputs to unknown
134            end
135          if (errorsignal_clk == 0)
136            begin
137              case (cell_state)
138                0: begin
139                  end
140                1: begin
141                  q <= #(delay_state1_clk_q) !q;
142                  cell_state = 0; // Blocking statement -- immediately
143                  errorsignal_b = 1; // Critical timing on this input; assign
144                                ↪ immediately
145                  errorsignal_b <= #(ct_state1_clk_b) 0; // Clear error signal
146                                ↪ after critical timing expires
147                end
148              2: begin
149                  q <= #(delay_state2_clk_q) !q;
150                  cell_state = 0; // Blocking statement -- immediately
151                  errorsignal_a = 1; // Critical timing on this input; assign
152                                ↪ immediately
153                  errorsignal_a <= #(ct_state2_clk_a) 0; // Clear error signal
154                                ↪ after critical timing expires
155                end
156            endcase
157        end
158    end
159
160 endmodule

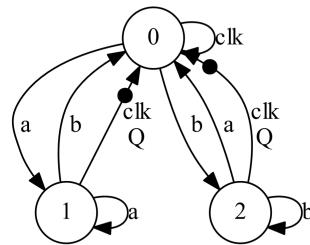
```

**Listing 4.30:** RSFQ XORT verilog model.

The digital simulation results for the RSFQ XORT is shown in Fig. 4.49 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.50.



**Figure 4.49:** RSFQ XORT digital simulation results.



**Figure 4.50:** RSFQ XORT Mealy finite state machine diagram.

## Power Consumption

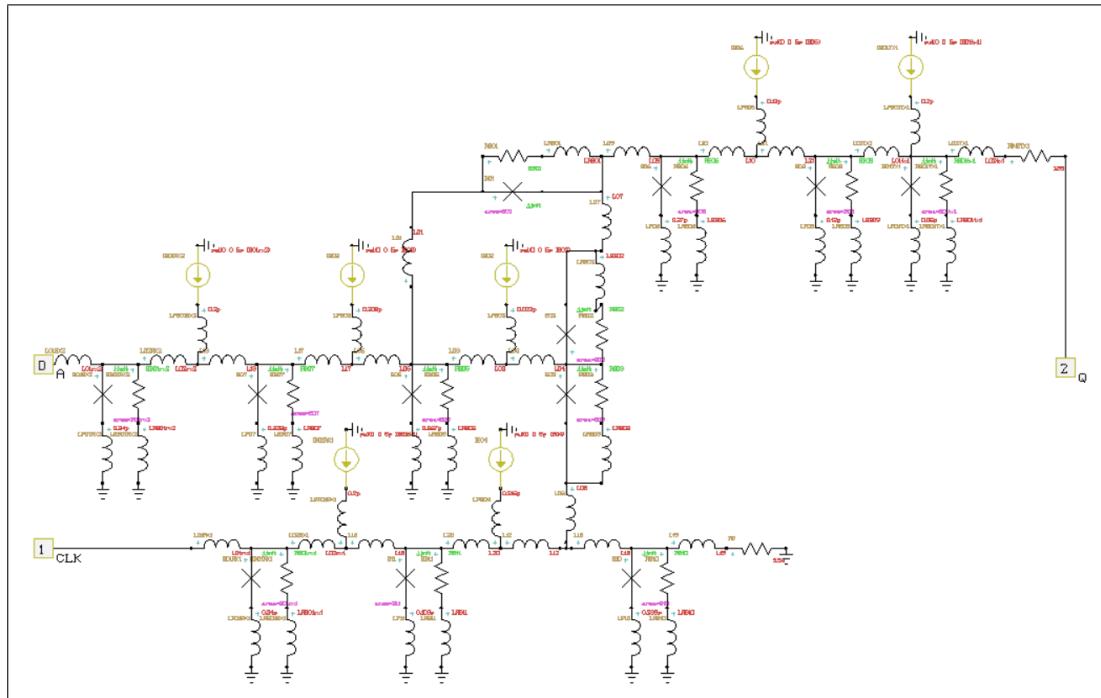
**Table 4.20:** RSFQ XORT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	298	5.18
2	298	10.4
5	298	25.9
10	298	51.8
20	298	104
50	298	259

#### 4.2.4 NOTT

The RSFQ NOTT cell is a signal inverting cell driven by a clock pulse signal line. The NOTT cell is designed with integrated PTL transmitters and receivers and is intended for direct connections with PTLs.

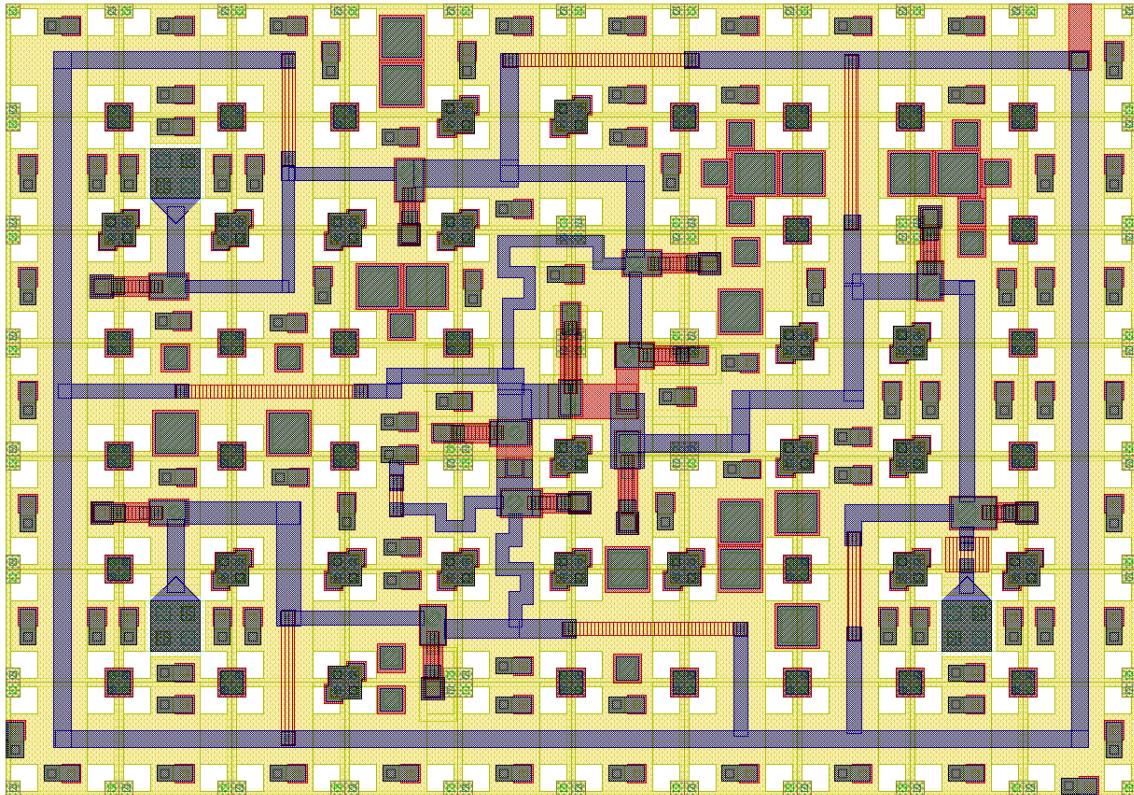
##### Schematic



**Figure 4.51:** Schematic of RSFQ NOTT.

## Layout

The physical layout for the RSFQ NOTT is shown in Fig. 4.52 and the resulting InductEx extraction is shown in Listing 4.31. The layout height is  $70 \mu m$  and the width is  $100 \mu m$ .



**Figure 4.52:** RSFQ NOTT Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_NOTT_v1p5.GDS -n LSmitll_NOTT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_NOTT_v1p5_idx.cir read. Totals: L = 37, k = 0, P = 23.
7 | Total fundamental loops identified in netlist = 20
8 | Using TetraHenry with analytical integration.
9 | 2868 structures read. Reduced 2868 objects to 2679 polygons and 11 terminals.
10 | Top level structure is "LSMITLL_NOTT_V1P5".
11 | GDS file LSmitll_NOTT_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 | Port clk not in netlist. Ignored.
13 | Object in layer I5 moved to TERM layer. (Pj1)
14 | Object in layer I5 moved to TERM layer. (Pj2)
15 | Object in layer I5 moved to TERM layer. (Pj3)
16 | Object in layer I5 moved to TERM layer. (Pj4)
17 | Object in layer I5 moved to TERM layer. (Pj5)
18 | Object in layer I5 moved to TERM layer. (Pj6)
19 | Object in layer I5 moved to TERM layer. (Pj7)
20 | Object in layer I5 moved to TERM layer. (Pj8)
21 | Object in layer I5 moved to TERM layer. (Pj9)
22 | Object in layer I5 moved to TERM layer. (Pj10)
23 | Object in layer I5 moved to TERM layer. (Pj11)
24 | Object in layer I5 moved to TERM layer. (Pj12)
25 | Terminal blocks = 23; Labels = 24; Extracted Ports = 23
26 |
27 | Port           Positive terminal      Negative terminal
28 | P1             M6, line along x;    M4, same as "+" terminal.
29 | P2             M6, line along x;    M4, same as "+" terminal.
30 | P3             M6, polygon;        M4, same as "+" terminal.
31 | PR1            M6, polygon;        M4, same as "+" terminal.
32 | PB1            M6, polygon;        M4, same as "+" terminal.
33 | PB2            M6, polygon;        M4, same as "+" terminal.
34 | PB3            M6, polygon;        M4, same as "+" terminal.
35 | PB4            M6, polygon;        M4, same as "+" terminal.
36 | PB5            M6, polygon;        M4, same as "+" terminal.
37 | PB6            M6, polygon;        M4, same as "+" terminal.
38 | PB7            M6, polygon;        M4, same as "+" terminal.
39 | J1              M6, polygon;        M5, same as "+" terminal.
40 | J2              M6, polygon;        M5, same as "+" terminal.
41 | J3              M6, polygon;        M5, same as "+" terminal.
42 | J4              M6, polygon;        M5, same as "+" terminal.
43 | J5              M6, polygon;        M5, same as "+" terminal.
44 | J6              M6, polygon;        M5, same as "+" terminal.
45 | J7              M6, polygon;        M5, same as "+" terminal.
46 | J8              M6, polygon;        M5, same as "+" terminal.
47 | J9              M6, polygon;        M5, same as "+" terminal.
48 | J10             M6, polygon;        M5, same as "+" terminal.
49 | J11             M6, polygon;        M5, same as "+" terminal.
50 | J12             M6, polygon;        M5, same as "+" terminal.
51 |
52 | SVD info: Condition nr. = 22.3; unknowns = 74; rank = 74.
53 |
54 | Impedance     Inductance [H]       Resistance [Ohm]      AbsDiff      PercDiff
55 | Name          Design      Extracted    Design      Extracted    (L only)    (L only)
56 | L1            --          1.48938E-12  --          --          +1.4894E-12  --%
57 | L2            2.5468E-12  2.56089E-12  --          --          +1.4091E-14  +0.55328%
58 | L3            2.6117E-12  2.61229E-12  --          --          +5.8684E-16  +0.02247%
59 | L4            1.1676E-12  1.17091E-12  --          --          +3.3091E-15  +0.28341%
60 | L5            2.6532E-12  2.63295E-12  --          --          -2.0252E-14  -0.76332%
61 | L7            3.1681E-12  3.08826E-12  --          --          -7.9836E-14  -2.52%
62 | L8            8.6946E-13  9.61256E-13  --          --          +9.1796E-14  +10.558%
63 | L9            --          1.46645E-12  --          --          +1.4664E-12  --%
64 | L10           4.4718E-12  4.48451E-12  --          --          +1.2713E-14  +0.28429%
65 | L11           2.1566E-12  2.17245E-12  --          --          +1.5845E-14  +0.73474%
66 | L12           9.918E-13   1.00918E-12  --          --          +1.7376E-14  +1.752%
67 | L13           3.286E-12   3.27206E-12  --          --          -1.3944E-14  -0.42436%
68 | L14           6.5962E-12  6.56753E-12  --          --          -2.8666E-14  -0.43458%
69 | L15           4.2413E-13  3.03051E-13  --          --          -1.2108E-13  -28.548%
70 | L16           2.2847E-12  2.29566E-12  --          --          +1.096E-14   +0.47972%

```

```

71 | L17      4.9986E-13  9.72893E-13 --      --      +4.7303E-13 +94.633%
72 | L18      2.8417E-13  4.94044E-13 --      --      +2.0987E-13 +73.855%
73 | L19      5.3651E-12  5.3561E-12 --      --      -8.9958E-15 -0.16767%
74 | L20      7.4611E-13  7.4752E-13 --      --      +1.4102E-15 +0.18901%
75 | L21      4.5195E-12  4.60071E-12 --      --      +8.1211E-14 +1.7969%
76 | L22      --         5.80064E-13 --      --      +5.8006E-13 --%
77 | LB1     --         3.14179E-13 --      --      +3.1418E-13 --%
78 | LB2     --         1.10014E-12 --      --      +1.1001E-12 --%
79 | LB3     --         5.15959E-13 --      --      +5.1596E-13 --%
80 | LB4     --         1.95831E-12 --      --      +1.9583E-12 --%
81 | LB5     --         2.94385E-12 --      --      +2.9438E-12 --%
82 | LB6     --         1.30273E-12 --      --      +1.3027E-12 --%
83 | LB7     --         2.38089E-12 --      --      +2.3809E-12 --%
84 | LP1     --         5.25578E-13 --      --      +5.2558E-13 --%
85 | LP2     --         4.98227E-13 --      --      +4.9823E-13 --%
86 | LP3     --         5.10771E-13 --      --      +5.1077E-13 --%
87 | LP6     --         5.23879E-13 --      --      +5.2388E-13 --%
88 | LP7     --         4.79962E-13 --      --      +4.7996E-13 --%
89 | LP8     --         5.71586E-13 --      --      +5.7159E-13 --%
90 | LP10    --         5.92522E-13 --      --      +5.9252E-13 --%
91 | LP11    --         4.98834E-13 --      --      +4.9883E-13 --%
92 | LP12    --         3.90333E-13 --      --      +3.9033E-13 --%
93
94 Ports      Design      Extracted      AbsDiff      PercDiff
95 J1          --          0.00013429
96 J2          --          0.00014995
97 J3          --          0.00018001
98 J4          --          0.00012983
99 J5          --          0.000084655
100 J6         --          0.00013321
101 J7         --          0.0002299
102 J8         --          0.00012983
103 J9         --          0.00014313
104 J10        --          0.00011204
105 J11        --          0.00014944
106 J12        --          0.00029325
107
108 Error bound on extracted values: 4.27715%
109
110 Deallocating memory.
111 Cycles found in 0.029 seconds.
112 SVD solution in 0.040 seconds.
113 Job finished in 434.799 seconds.

```

**Listing 4.31:** RSFQ NOTT InductEx extraction.

## Analog model

```

1  * Author: L. Schindler
2  * Version: 1.5.1
3  * Last modification date: 18 June 2020
4  * Last modification by: L. Schindler
5
6  * Copyright (c) 2018-2020 Lieze Schindler,
7      ↪ Stellenbosch University
8
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42   ↪ ARISING FROM,
43   ↪ OUT OF OR IN CONNECTION WITH THE LIBRARY
44   ↪ OR THE USE OR OTHER DEALINGS IN
45   ↪ THE
46   ↪ LIBRARY.
47
48   *For questions about the library, contact
49   ↪ Lieze Schindler, 17528283@sun.ac.za
50
51   *$Ports
52   ↪ a clk q
53
54 .subckt LSmitll_NOTT a clk q
55 .model jjmit jj(rtype=1, vg=2.8mV, cap
56   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
57   ↪ )
58
59 .param B0=1
60 .param Ic0=0.0001
61 .param IcRs=100u*6.859904418
62 .param B0Rs=IcRs/Ic0*B0
63 .param Rsheet=2
64 .param Lsheet=1.13e-12
65 .param B01=1.3488
66 .param B01rx1=1.2613
67 .param B01rx2=1.2476
68 .param B01tx1=2.8510
69 .param B02=0.7718
70
71   .param B03=1.2227
72   .param B05=1.2221
73   .param B06=1.0432
74   .param B07=2.2139
75   .param B09=1.4100
76   .param B10=1.7227
77   .param B11=1.4193
78   .param IB01rx1=0.000146094
79   .param IB01rx2=0.000181215
80   .param IB01tx1=0.000187178
81   .param IB02=9.6978e-05
82   .param IB03=9.5221e-05
83   .param IB04=0.000101564
84   .param IB06=0.000108369
85   .param L01=2.2847e-12
86   .param L01rx1=1.8571e-12
87   .param L01rx2=2.1457e-12
88   .param L01tx1=4.5195e-12
89   .param L02rx1=4.4718e-12
90   .param L02rx2=2.5468e-12
91   .param L02tx1=3.4724e-12
92   .param L03=6.5962e-12
93   .param L04=4.2413e-13
94   .param L06=3.2860e-12
95   .param L07=4.9986e-13
96   .param L08=8.6946e-13
97   .param L09=2.8417e-13
98   .param L10=7.3651e-12
99   .param L12=2.6532e-12
100  .param L13=2.1566e-12
101  .param L16=2.6117e-12
102  .param L17=9.9180e-13
103  .param L18=2.5842e-13
104  .param L19=3.1681e-12
105  .param L20=1.1676e-12
106  .param L21=7.4611e-13
107  .param LRB01=(RB01/Rsheet)*Lsheet
108  .param LRB01rx1=(RB01rx1/Rsheet)*Lsheet
109  .param LRB01rx2=(RB01rx2/Rsheet)*Lsheet
110  .param LRB01tx1=(RB01tx1/Rsheet)*Lsheet
111  .param LRB02=(RB02/Rsheet)*Lsheet
112  .param LRB03=(RB03/Rsheet)*Lsheet
113  .param LRB05=(RB05/Rsheet)*Lsheet
114  .param LRB06=(RB06/Rsheet)*Lsheet
115  .param LRB07=(RB07/Rsheet)*Lsheet
116  .param LRB09=(RB09/Rsheet)*Lsheet
117  .param LRB10=(RB10/Rsheet)*Lsheet
118  .param LRB11=(RB11/Rsheet)*Lsheet
119  .param RB01=B0Rs/B01
120  .param RB01rx1=B0Rs/B01rx1
121  .param RB01rx2=B0Rs/B01rx2
122  .param RB01tx1=B0Rs/B01tx1
123  .param RB02=B0Rs/B02
124  .param RB03=B0Rs/B03
125  .param RB05=B0Rs/B05
126  .param RB06=B0Rs/B06
127  .param RB07=B0Rs/B07
128  .param RB09=B0Rs/B09
129  .param RB10=B0Rs/B10
130  .param RB11=B0Rs/B11
131  B01 4 5 jjmit area=B01
132  B01rx1 17 49 jjmit area=B01rx1
133  B01rx2 12 37 jjmit area=B01rx2
134  B01tx1 8 29 jjmit area=B01tx1
135  B02 14 9 jjmit area=B02
136  B03 14 15 jjmit area=B03

```

```

108 | B05 10 41 jjmit area=B05      148 | LP07 39 0 0.328p
109 | B06 6 25 jjmit area=B06      149 | LP09 27 0 0.12p
110 | B07 13 39 jjmit area=B07      150 | LP10 53 0 0.239p
111 | B09 7 27 jjmit area=B09      151 | LP11 51 0 0.109p
112 | B10 19 53 jjmit area=B10      152 | LPR01rx1 46 44 0.2p
113 | B11 18 51 jjmit area=B11      153 | LPR01rx2 31 34 0.2p
114 | IB01rx1 0 44 pwl(0 0 5p IB01rx1) 154 | LPR01tx1 21 8 0.2p
115 | IB01rx2 0 31 pwl(0 0 5p IB01rx2) 155 | LPR02 33 36 0.023p
116 | IB01tx1 0 21 pwl(0 0 5p IB01tx1) 156 | LPR03 32 35 0.208p
117 | IB02 0 33 pwl(0 0 5p IB02)      157 | LPR04 47 45 0.216p
118 | IB03 0 32 pwl(0 0 5p IB03)      158 | LPR06 20 22 0.13p
119 | IB04 0 45 pwl(0 0 5p IB04)      159 | LRB01 23 5 LRB01
120 | IB06 0 20 pwl(0 0 5p IB06)      160 | LRB01rx1 50 0 LRB01rx1
121 | L01 10 4 L01                  161 | LRB01rx2 38 0 LRB01rx2
122 | L01rx1 a 17 L01rx1            162 | LRB01tx1 30 0 LRB01tx1
123 | L01rx2 clk 12 L01rx2          163 | LRB02 9 11 LRB02
124 | L01tx1 7 8 L01tx1            164 | LRB03 43 15 LRB03
125 | L02rx1 17 46 L02rx1          165 | LRB05 42 0 LRB05
126 | L02rx2 12 34 L02rx2          166 | LRB06 26 0 LRB06
127 | L02tx1 8 24 L02tx1          167 | LRB07 40 0 LRB07
128 | L03 10 36 L03                168 | LRB09 28 0 LRB09
129 | L04 36 14 L04                169 | LRB10 54 0 LRB10
130 | L06 35 10 L06                170 | LRB11 52 0 LRB11
131 | L07 5 9 L07                  171 | RB01 4 23 RB01
132 | L08 15 16 L08                172 | RB01rx1 17 50 RB01rx1
133 | L09 5 6 L09                  173 | RB01rx2 12 38 RB01rx2
134 | L10 6 22 L10                 174 | RB01tx1 8 30 RB01tx1
135 | L12 47 16 L12                175 | RB02 11 14 RB02
136 | L13 34 13 L13                176 | RB03 14 43 RB03
137 | L16 46 18 L16                177 | RB05 10 42 RB05
138 | L17 13 35 L17                178 | RB06 6 26 RB06
139 | L18 16 19 L18                179 | RB07 13 40 RB07
140 | L19 19 48 L19                180 | RB09 7 28 RB09
141 | L20 18 47 L20                181 | RB10 19 54 RB10
142 | L21 22 7 L21                  182 | RB11 18 52 RB11
143 | LP01rx1 49 0 0.34p           183 | RD 48 0 3.54
144 | LP01rx2 37 0 0.34p           184 | RINStx1 24 q 1.36
145 | LP01tx1 29 0 0.05p           185 | .ends
146 | LP05 41 0 0.567p
147 | LP06 25 0 0.27p

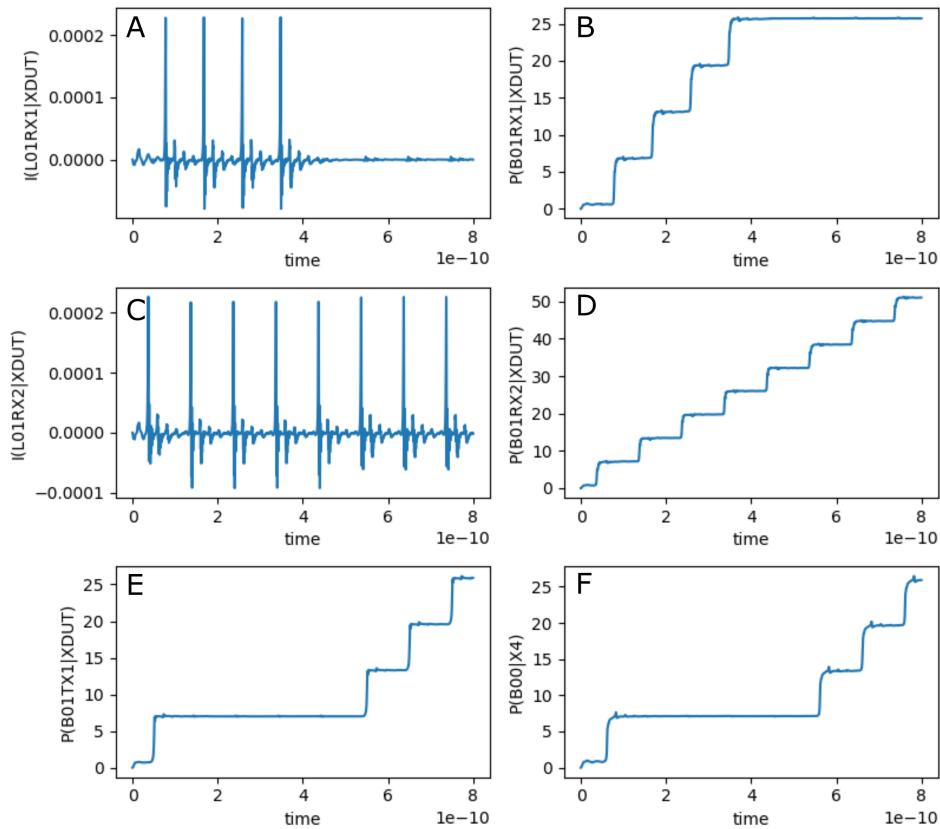
```

**Listing 4.32:** RSFQ NOTT JoSIM netlist.**Table 4.21:** RSFQ NOTT pin list.

Pin	Description
a	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ NOTT using JoSIM is shown in Fig. 4.53. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **clk**,
- (d) the phase over the input JJ of pin **clk**,
- (e) the phase over the output JJ of pin **q**, and
- (f) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.



**Figure 4.53:** RSFQ NOTT analog simulation results.

## Digital model

```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 // -----
9 `timescale 1ps/100fs
10 module LSmitll_NOTT_v1p5 (a, clk, q);
11
12 input
13   a, clk;
14
15 output
16   q;
17
18 reg
19   q;
20
21 real
22   delay_state0_clk_q = 13.5,
23   ct_state0_clk_a = 6.6,
24   ct_state0_clk_clk = 16.6,
25   ct_state1_a_clk = 11.8;
26
27 reg
28   errorsignal_a,
29   errorsignal_clk;
30
31 integer
32   outfile,
33   cell_state; // internal state of the cell
34
35 initial
36 begin
37   errorsignal_a = 0;
38   errorsignal_clk = 0;
39   cell_state = 0; // Startup state
40   q = 0; // All outputs start at 0
41 end
42
43 always @ (posedge a or negedge a) // execute at positive and negative edges of input
44 begin
45   if ($time > 4) // arbitrary steady-state time)
46     begin
47       if (errorsignal_a == 1'b1) // A critical timing is active for this input
48         begin
49           outfile = $fopen("errors.txt", "a");
50           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
51           ↪ ", $stime);
52           $fclose(outfile);
53           q <= 1'bX; // Set all outputs to unknown
54         end
55       if (errorsignal_a == 0)
56         begin
57           case (cell_state)
58             0: begin
59               cell_state = 1; // Blocking statement -- immediately
60             end
61             1: begin
62               errorsignal_clk = 1; // Critical timing on this input; assign
63               ↪ immediately
64               errorsignal_clk <= #(ct_state1_a_clk) 0; // Clear error signal
               ↪ after critical timing expires
             end
           endcase
         end
       end
     end
   end
 
```

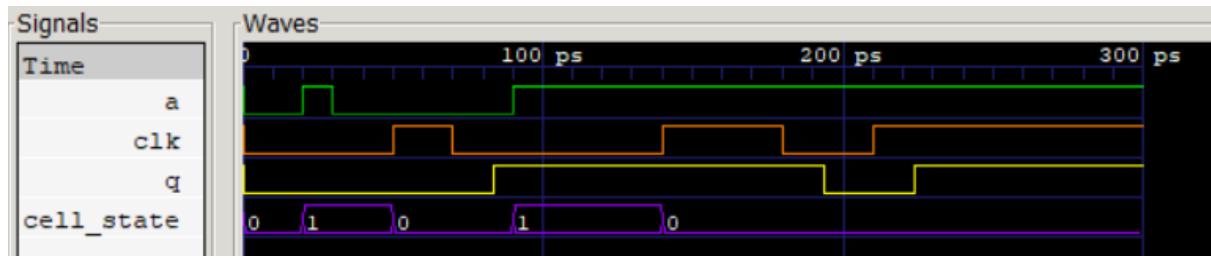
```

65           end
66       end
67   end
68
69 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
70   begin
71     if ($time>4) // arbitrary steady-state time)
72     begin
73       if (errorsignal_clk == 1'b1) // A critical timing is active for this input
74       begin
75         outfile = $fopen("errors.txt", "a");
76         $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
77                     ↪ ", $stime);
78         $fclose(outfile);
79         q <= 1'bX; // Set all outputs to unknown
80       end
81     if (errorsignal_clk == 0)
82     begin
83       case (cell_state)
84         0: begin
85           q <= #(delay_state0_clk_q) !q;
86           errorsignal_a = 1; // Critical timing on this input; assign
87             ↪ immediately
88           errorsignal_a <= #(ct_state0_clk_a) 0; // Clear error signal
89             ↪ after critical timing expires
90           errorsignal_clk = 1; // Critical timing on this input; assign
91             ↪ immediately
92           errorsignal_clk <= #(ct_state0_clk_clk) 0; // Clear error
93             ↪ signal after critical timing expires
94         end
95       1: begin
96         cell_state = 0; // Blocking statement -- immediately
97       end
98     endcase
99   end
100 end
101
102 endmodule

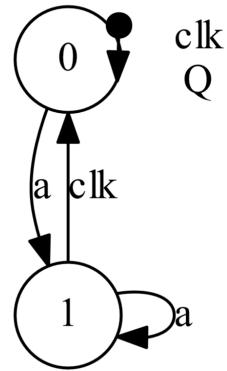
```

**Listing 4.33:** RSFQ NOTT verilog model.

The digital simulation results for the RSFQ NOTT is shown in Fig. 4.54 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.55.



**Figure 4.54:** RSFQ NOTT digital simulation results.



**Figure 4.55:** RSFQ NOTT Mealy finite state machine diagram.

## Power Consumption

**Table 4.22:** RSFQ NOTT power consumption.

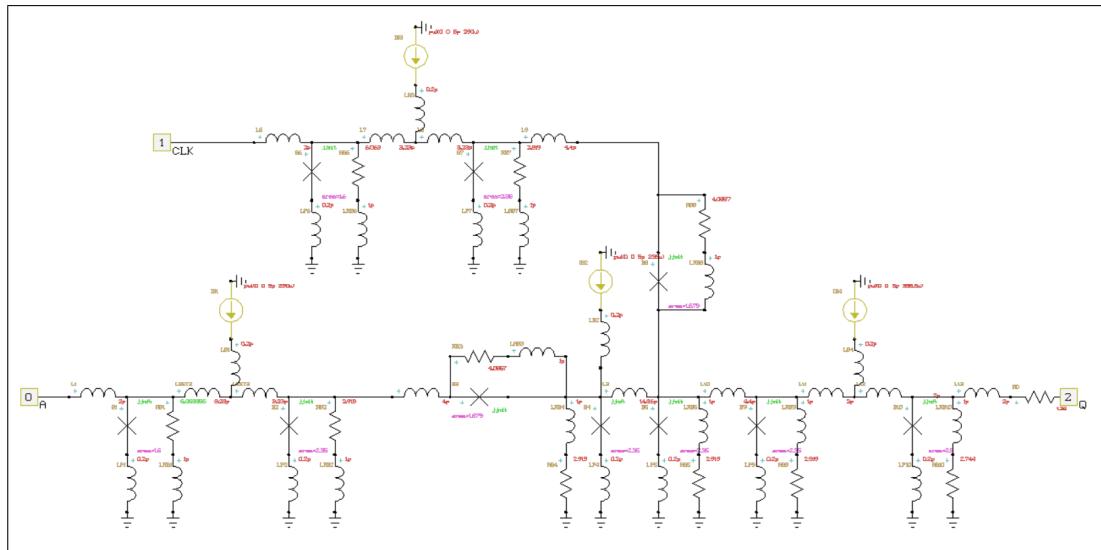
Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	238	3.67
2	238	7.33
5	238	18.3
10	238	36.7
20	238	73.3
50	238	183

## 4.3 Buffers

### 4.3.1 DFFT

The RSFQ DFFT, D flip-flop, is a multi-state device used to transmit an input set pulse synchronised with a reset (typically clock) signal. The DFFT is designed with integrated PTL transmitters and receivers and is intended to connect directly to PTLs.

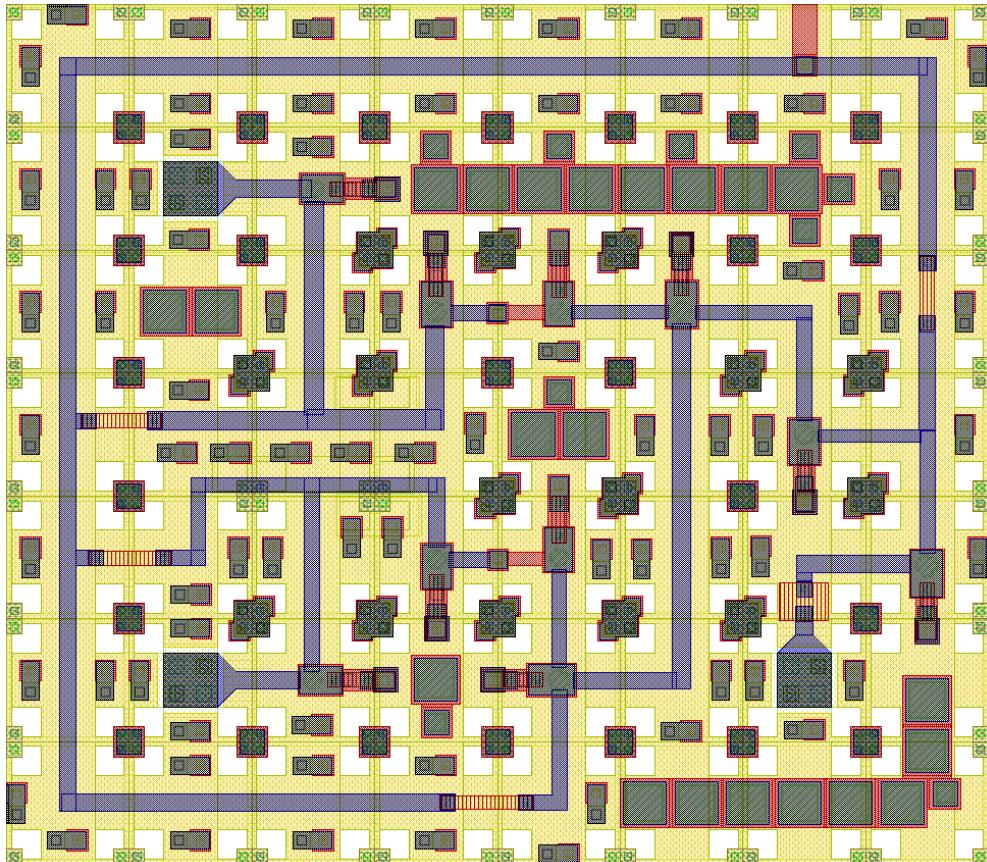
## Schematic



**Figure 4.56:** Schematic of RSFQ DFFT.

## Layout

The physical layout for the RSFQ DFFT is shown in Fig. 4.57 and the resulting InductEx extraction is shown in Listing 4.34. The layout height is  $70 \mu\text{m}$  and the width is  $80 \mu\text{m}$ .



**Figure 4.57:** RSFQ DFFT Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 | SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_DFFT_v1p5.gds -n LSmitll_DFFT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_DFFT_v1p5_idx.cir read. Totals: L = 25, k = 0, P = 17.
7 | Total fundamental loops identified in netlist = 14
8 | Using TetraHenry with analytical integration.
9 | 2405 structures read. Reduced 2405 objects to 2229 polygons and 7 terminals.
10 | Top level structure is "LSMITLL_DFFT".
11 | GDS file LSmitll_DFFT_v1p5.gds read: db units in 1E-9 m, 0.001 units per user unit.
12 | Port clk not in netlist. Ignored.
13 | Object in layer I5 moved to TERM layer. (Pj1)
14 | Object in layer I5 moved to TERM layer. (Pj2)
15 | Object in layer I5 moved to TERM layer. (Pj3)
16 | Object in layer I5 moved to TERM layer. (Pj4)
17 | Object in layer I5 moved to TERM layer. (Pj5)
18 | Object in layer I5 moved to TERM layer. (Pj6)
19 | Object in layer I5 moved to TERM layer. (Pj7)
20 | Object in layer I5 moved to TERM layer. (Pj8)
21 | Object in layer I5 moved to TERM layer. (Pj9)
22 | Object in layer I5 moved to TERM layer. (Pj10)
23 | Terminal blocks = 17; Labels = 18; Extracted Ports = 17
24 |
25 | Port           Positive terminal    Negative terminal

```

```

26 | P1          M6,    line along y; M4,    same as "+" terminal.
27 | P2          M6,    line along y; M4,    same as "+" terminal.
28 | P3          M6,    line along y; M4,    same as "+" terminal.
29 | PB1         M6,    line along y; M4,    same as "+" terminal.
30 | PB2         M6,    line along y; M4,    same as "+" terminal.
31 | PB3         M6,    line along y; M4,    same as "+" terminal.
32 | PB4         M6,    line along x; M4,    same as "+" terminal.
33 | J1          M6,    polygon;      M5,    same as "+" terminal.
34 | J2          M6,    polygon;      M5,    same as "+" terminal.
35 | J3          M5,    polygon;      M6,    same as "+" terminal.
36 | J4          M6,    polygon;      M5,    same as "+" terminal.
37 | J5          M6,    polygon;      M5,    same as "+" terminal.
38 | J6          M6,    polygon;      M5,    same as "+" terminal.
39 | J7          M6,    polygon;      M5,    same as "+" terminal.
40 | J8          M5,    polygon;      M6,    same as "+" terminal.
41 | J9          M6,    polygon;      M5,    same as "+" terminal.
42 | J10         M6,    polygon;      M5,    same as "+" terminal.
43
44 SVD info: Condition nr. = 9.759; unknowns = 50; rank = 50.
45
46 Impedance   Inductance [H]       Resistance [Ohm]     AbsDiff      PercDiff
47 Name        Design      Extracted    Design      Extracted  (L only)    (L only)
48 L1          --          1.5637E-12  --          --          +1.5637E-12  --%
49 L2          3.28E-12    3.3024E-12  --          --          +2.2404E-14  +0.68305%
50 L3          3.28E-12    3.2234E-12  --          --          -5.6604E-14  -1.7257%
51 L4          4.06E-12    4.01455E-12  --          --          -4.5452E-14  -1.1195%
52 L5          7.51E-12    7.45324E-12  --          --          -5.6759E-14  -0.75578%
53 L6          --          1.62164E-12  --          --          +1.6216E-12  --%
54 L7          3.04E-12    3.06566E-12  --          --          +2.5658E-14  +0.844%
55 L8          3.04E-12    3.01289E-12  --          --          -2.7114E-14  -0.89191%
56 L9          4.21E-12    4.20385E-12  --          --          -6.1531E-15  -0.14615%
57 L10         4.02E-12    3.9935E-12   --          --          -2.6498E-14  -0.65916%
58 L11         2.15E-12    2.12269E-12  --          --          -2.7311E-14  -1.2703%
59 L12         2.15E-12    2.1382E-12   --          --          -1.1803E-14  -0.54896%
60 L13         --          1.85888E-12  --          --          +1.8589E-12  --%
61 LP1         --          5.12978E-13   --          --          +5.1298E-13  --%
62 LP2         --          5.1029E-13   --          --          +5.1029E-13  --%
63 LP4         --          5.20691E-13  --          --          +5.2069E-13  --%
64 LP5         --          5.28352E-13  --          --          +5.2835E-13  --%
65 LP6         --          4.99443E-13  --          --          +4.9944E-13  --%
66 LP7         --          5.15628E-13  --          --          +5.1563E-13  --%
67 LP9         --          5.1113E-13   --          --          +5.1113E-13  --%
68 LP10        --          5.12546E-13  --          --          +5.1255E-13  --%
69 LB1         --          3.81288E-12  --          --          +3.8129E-12  --%
70 LB2         --          2.46377E-12  --          --          +2.4638E-12  --%
71 LB3         --          1.72715E-12  --          --          +1.7271E-12  --%
72 LB4         --          1.95727E-12  --          --          +1.9573E-12  --%
73
74 Ports       Design      Extracted  AbsDiff      PercDiff
75 J1          0.00016     0.00017055
76 J2          0.000189    0.00019733
77 J3          0.000172    0.00017942
78 J4          0.000232    0.00024083
79 J5          0.000212    0.00022067
80 J6          0.00016     0.00017055
81 J7          0.000198    0.00020657
82 J8          0.000171    0.00017942
83 J9          0.000212    0.00022067
84 J10         0.00025     0.00025893
85
86 Error bound on extracted values: 1.52366%
87
88 Deallocating memory.
89 Cycles found in 0.030 seconds.
90 SVD solution in 0.021 seconds.
91 Job finished in 293.335 seconds.

```

Listing 4.34: RSFQ DFFT InductEx extraction.

## Analog model

```

1  * Author: L. Schindler
2  * Version: 1.5.1
3  * Last modification date: 18 June 2020
4  * Last modification by: L. Schindler
5
6  *$Ports
7  .subckt LSMITLL_DFFT a clk q
8  .model jjmit jj(rtype=1, vg=2.8mV, cap
9    ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
10   ↪ )
11 .param Phi0=2.067833848E-15
12 .param B0=1
13 .param Ic0=0.0001
14 .param IcRs=100u*6.859904418
15 .param B0Rs=IcRs/Ic0*B0
16 .param Rsheet=2
17 .param Lsheet=1.13e-12
18 .param LP=0.2p
19 .param IC=2.5
20 .param ICreceive=2.0
21 .param ICtrans=2.5
22 .param Lptl=2p
23 .param LB=2p
24 .param BiasCoef=0.7
25 .param RD=1.36
26 .param B1=ICreceive
27 .param B2=IC
28 .param B3=IC/1.4
29 .param B4=IC
30 .param B5=IC
31 .param B6=ICreceive
32 .param B7=IC
33 .param B8=IC/1.4
34 .param B9=IC
35 .param B10=ICtrans
36 .param IB1=BiasCoef*(B1*Ic0+B2*Ic0)
37 .param IB2=IC*Ic0
38 .param IB3=BiasCoef*(B6*Ic0+B7*Ic0)
39 .param IB4=BiasCoef*(B9*Ic0+B10*Ic0)
40 .param L1=Lptl
41 .param L2=(Phi0/(2*B1*Ic0))/2
42 .param L3=(Phi0/(2*B1*Ic0))/2
43 .param L4=Phi0/(2*B2*Ic0)
44 .param L5=Phi0/(B4*Ic0)
45 .param L6=Lptl
46 .param L7=(Phi0/(2*B6*Ic0))/2
47 .param L8=(Phi0/(2*B6*Ic0))/2
48 .param L9=Phi0/(2*B7*Ic0)
49 .param L10=Phi0/(2*B5*Ic0)
50 .param L11=(Phi0/(2*B9*Ic0))/2
51 .param L12=(Phi0/(2*B9*Ic0))/2
52 .param L13=Lptl
53 .param RB1=B0Rs/B1
54 .param RB2=B0Rs/B2
55 .param RB3=B0Rs/B3
56 .param RB4=B0Rs/B4
57 .param RB5=B0Rs/B5
58 .param RB6=B0Rs/B6
59 .param RB7=B0Rs/B7
60 .param RB8=B0Rs/B8
61 .param RB9=B0Rs/B9
62 .param RB10=B0Rs/B10
63 .param LRB1=(RB1/Rsheet)*Lsheet+LP
64 .param LRB2=(RB2/Rsheet)*Lsheet+LP
65 .param LRB5=(RB5/Rsheet)*Lsheet+LP
66 .param LRB6=(RB6/Rsheet)*Lsheet+LP
67 .param LRB7=(RB7/Rsheet)*Lsheet+LP
68 .param LRB8=(RB8/Rsheet)*Lsheet+LP
69 .param LRB9=(RB9/Rsheet)*Lsheet+LP
70 .param LRB10=(RB10/Rsheet)*Lsheet+LP
71 .param LP1=LP
72 .param LP2=LP
73 .param LP4=LP
74 .param LP5=LP
75 .param LP6=LP
76 .param LP7=LP
77 .param LP9=LP
78 .param LP10=LP
79 .param LB1=LB
80 .param LB2=LB
81 .param LB3=LB
82 .param LB4=LB
83 IB1 0 5 pw1(0 0 5p IB1)
84 IB2 0 11 pw1(0 0 5p IB2)
85 IB3 0 18 pw1(0 0 5p IB3)
86 IB4 0 25 pw1(0 0 5p IB4)
87 B1 2 3 jjmit area=B1
88 B2 6 7 jjmit area=B2
89 B3 8 9 jjmit area=B3
90 B4 9 10 jjmit area=B4
91 B5 12 13 jjmit area=B5
92 B6 15 16 jjmit area=B6
93 B7 19 20 jjmit area=B7
94 B8 21 12 jjmit area=B8
95 B9 22 23 jjmit area=B9
96 B10 26 27 jjmit area=B10
97 L1 a 2 L1
98 L2 2 4 L2
99 L3 4 6 L3
100 L4 6 8 L4
101 L5 9 12 L5
102 L6 clk 15 L6
103 L7 15 17 L7
104 L8 17 19 L8
105 L9 19 21 L9
106 L10 12 22 L10
107 L11 22 24 L11
108 L12 24 26 L12
109 L13 26 28 L13
110 LP1 3 0 LP1
111 LP2 7 0 LP2
112 LP4 10 0 LP4
113 LP5 13 0 LP5
114 LP6 16 0 LP6
115 LP7 20 0 LP7
116 LP9 23 0 LP9
117 LP10 27 0 LP10
118 LB1 4 5 LB1
119 LB2 9 11 LB2
120 LB3 17 18 LB3
121 LB4 24 25 LB4
122 RB1 2 102 RB1
123 RB2 6 106 RB2
124 RB3 8 108 RB3
125 RB4 9 109 RB4
126 RB5 12 112 RB5
127 RB6 15 115 RB6
128 RB7 19 119 RB7
129 RB8 21 121 RB8
130 RB9 22 122 RB9

```

```

131 | RB10 26 126 RB10
132 | LRB1 102 0 LRB1
133 | LRB2 106 0 LRB2
134 | LRB3 108 9 LRB3
135 | LRB4 109 0 LRB4
136 | LRB5 112 0 LRB5
137 | LRB6 115 0 LRB6
138 | LRB7 119 0 LRB7
139 | LRB8 121 12 LRB8
140 | LRB9 122 0 LRB9
141 | LRB10 126 0 LRB10
142 | RD 28 q RD
143 .ends

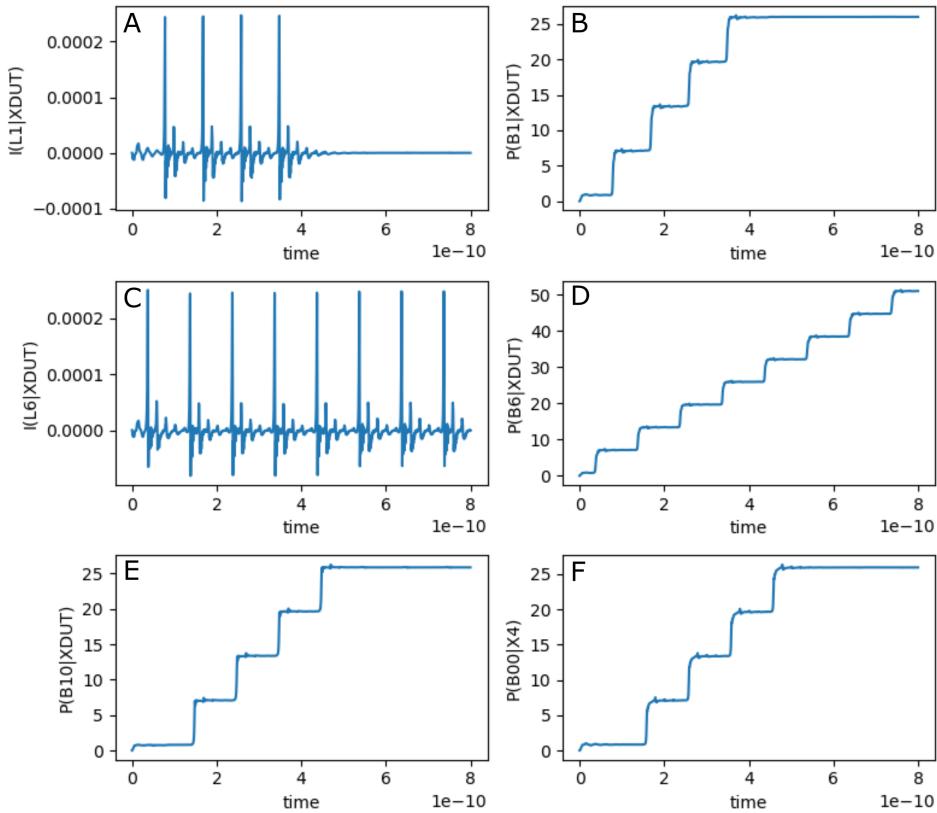
```

**Listing 4.35:** RSFQ DFFT JoSIM netlist.**Table 4.23:** RSFQ DFFT pin list.

<b>Pin</b>	<b>Description</b>
<b>a</b>	Data input
<b>clk</b>	Clock input
<b>q</b>	Data output

The simulation results for the RSFQ DFFT using JoSIM is shown in Fig. 4.58. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **clk**,
- (d) the phase over the input JJ of pin **clk**,
- (e) the phase over the output JJ of pin **q**, and
- (f) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.



**Figure 4.58:** RSFQ DFFT analog simulation results.

## Digital model

```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 // -----
9 `timescale 1ps/100fs
10 module LSmitll_DFFT_v1p5 (a, clk, q);
11
12 input
13   a, clk;
14
15 output
16   q;
17
18 reg
19   q;
20
21 real
22   delay_state1_clk_q = 10.3,
23   ct_state0_clk_a = 1.0,
24   ct_state1_a_clk = 1.0;
25
26 reg
27   errorsignal_a,
28   errorsignal_clk;
29
30 integer
31   outfile,
32   cell_state; // internal state of the cell
33
34 initial
35 begin
36   errorsignal_a = 0;
37   errorsignal_clk = 0;
38   cell_state = 0; // Startup state
39   q = 0; // All outputs start at 0
40 end
41
42 always @ (posedge a or negedge a) // execute at positive and negative edges of input
43 begin
44   if ($time > 4) // arbitrary steady-state time)
45     begin
46       if (errorsignal_a == 1'b1) // A critical timing is active for this input
47         begin
48           outfile = $fopen("errors.txt", "a");
49           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m; %0d_ps.\n"
50           ↪ ", $stime);
51           $fclose(outfile);
52           q <= 1'bX; // Set all outputs to unknown
53         end
54       if (errorsignal_a == 0)
55         begin
56           case (cell_state)
57             0: begin
58               cell_state = 1; // Blocking statement -- immediately
59             end
60             1: begin
61               errorsignal_clk = 1; // Critical timing on this input; assign
62               ↪ immediately
63               errorsignal_clk <= #(ct_state1_a_clk) 0; // Clear error signal
64               ↪ after critical timing expires
65             end
66           endcase
67         end
68     end
69   end
70 end
71
72
73
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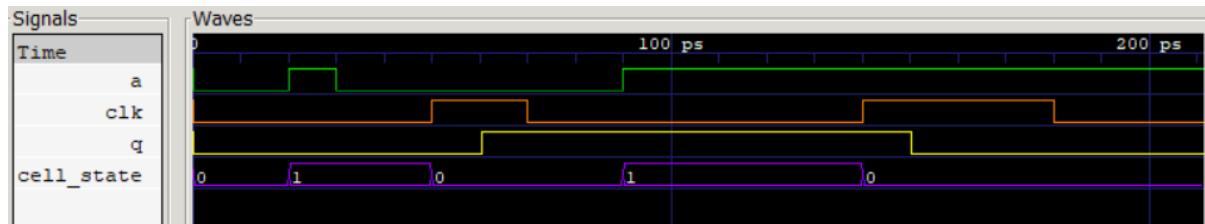
```

65      end
66  end
67
68 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
69 begin
70   if ($time>4) // arbitrary steady-state time)
71   begin
72     if (errorsignal_clk == 1'b1) // A critical timing is active for this input
73     begin
74       outfile = $fopen("errors.txt", "a");
75       $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;,%0d_ps.\n"
76                   ↪ ", $stime);
77       $fclose(outfile);
78       q <= 1'bX; // Set all outputs to unknown
79     end
80   if (errorsignal_clk == 0)
81   begin
82     case (cell_state)
83     0: begin
84       errorsignal_a = 1; // Critical timing on this input; assign
85                   ↪ immediately
86       errorsignal_a <= #(ct_state0_clk_a) 0; // Clear error signal
87                   ↪ after critical timing expires
88     end
89   1: begin
90     q <= #(delay_state1_clk_q) !q;
91     cell_state = 0; // Blocking statement -- immediately
92   end
93   endcase
94 end
95 endmodule

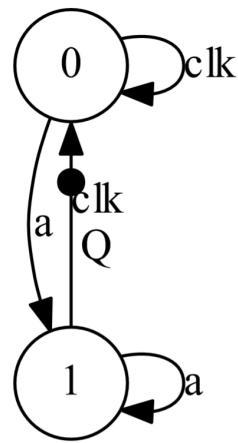
```

**Listing 4.36:** RSFQ DFFT verilog model.

The digital simulation results for the RSFQ DFFT is shown in Fig. 4.59 and the Mealy finite state machine diagram, extracted using *TimEx*, is shown in Fig. 4.60.



**Figure 4.59:** RSFQ DFFT digital simulation results.



**Figure 4.60:** RSFQ DFFT Mealy finite state machine diagram.

## Power Consumption

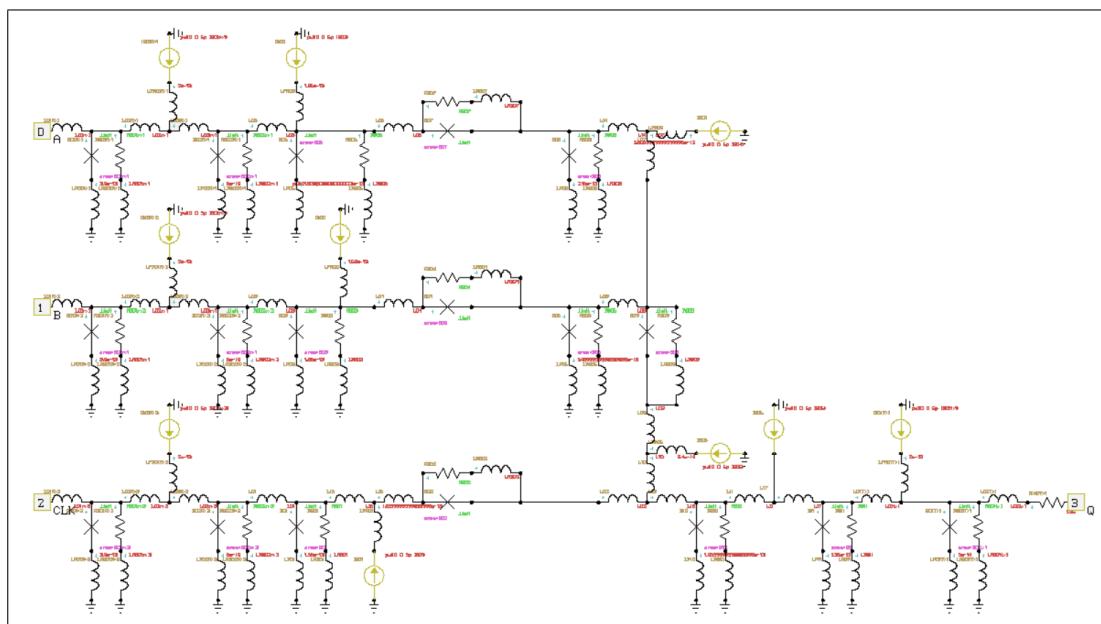
**Table 4.24:** RSFQ JTLT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	320	4.67
2	320	9.33
5	320	23.3
10	320	46.7
20	320	93.3
50	320	233

### 4.3.2 NDROT

The NDROT, non-destructive readout, cell is a memory device controlled by a set, reset and clock input signal. When an input set signal is received, the NDROT will generate an output pulse after each clock signal until an input reset signal is received. The NDROT is designed with integrated PTL transmitters and receivers and is intended to connect directly to PTLs.

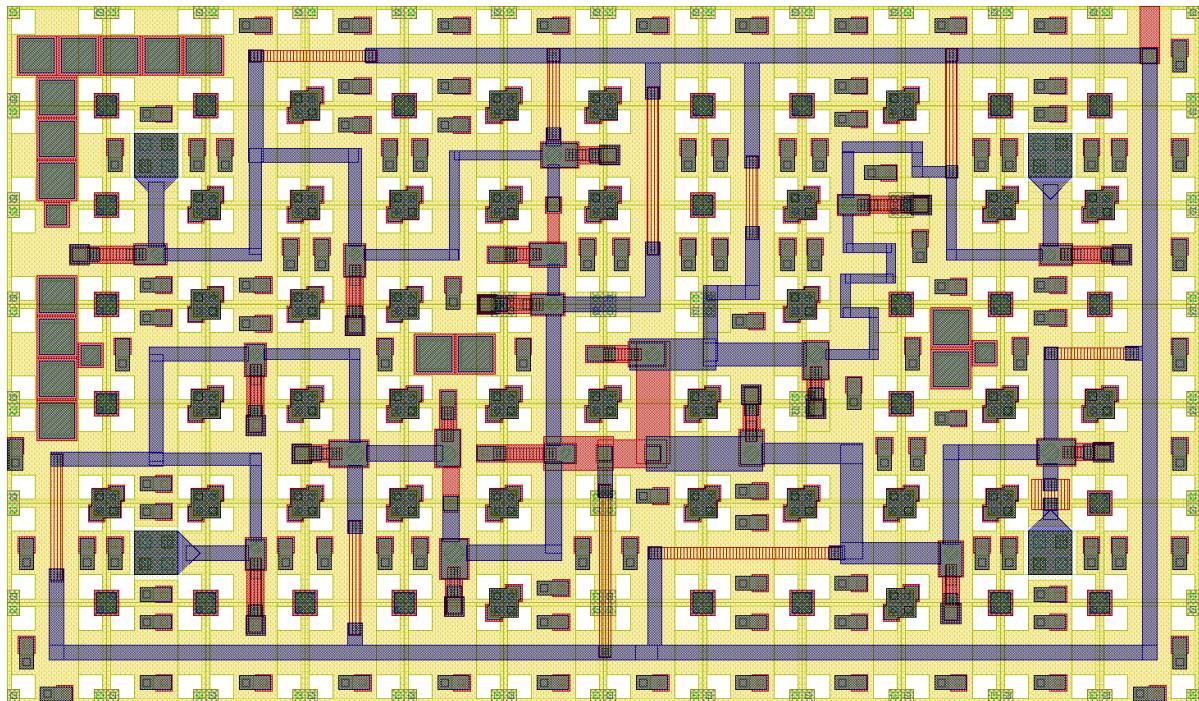
#### Schematic



**Figure 4.61:** Schematic of RSFQ NDROT.

## Layout

The physical layout for the RSFQ NDROT is shown in Fig. 4.62 and the resulting InductEx extraction is shown in Listing 4.37. The layout height is  $70 \mu m$  and the width is  $120 \mu m$ .



**Figure 4.62:** RSFQ NDROT Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_NDROT_v1p5.GDS -n LSmitll_NDROT_V1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_NDROT_v1p5_idx.cir read. Totals: L = 49, k = 0, P = 32.
7 | Total fundamental loops identified in netlist = 27
8 | Using TetraHenry with analytical integration.
9 | 3534 structures read. Reduced 3534 objects to 3260 polygons and 14 terminals.
10 | Top level structure is "LSMITLL_NDROT_V1P5".
11 | GDS file LSmitll_NDROT_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 | Port in_clk not in netlist. Ignored.
13 | Object in layer I5 moved to TERM layer. (Pj1)
14 | Object in layer I5 moved to TERM layer. (Pj2)
15 | Object in layer I5 moved to TERM layer. (Pj3)
16 | Object in layer I5 moved to TERM layer. (Pj4)
17 | Object in layer I5 moved to TERM layer. (Pj5)
18 | Object in layer I5 moved to TERM layer. (Pj6)
19 | Object in layer I5 moved to TERM layer. (Pj7)
20 | Object in layer I5 moved to TERM layer. (Pj8)
21 | Object in layer I5 moved to TERM layer. (Pj9)
22 | Object in layer I5 moved to TERM layer. (Pj10)
23 | Object in layer I5 moved to TERM layer. (Pj11)
24 | Object in layer I5 moved to TERM layer. (Pj12)
25 | Object in layer I5 moved to TERM layer. (Pj13)
26 | Object in layer I5 moved to TERM layer. (Pj14)
27 | Object in layer I5 moved to TERM layer. (Pj15)
28 | Object in layer I5 moved to TERM layer. (Pj16)
29 | Object in layer I5 moved to TERM layer. (Pj17)
30 | Object in layer I5 moved to TERM layer. (Pj18)
31 | Terminal blocks = 32; Labels = 33; Extracted Ports = 32
32 |

```

```

33 | Port          Positive terminal    Negative terminal
34 | P1            M6, line along x; M4, same as "+" terminal.
35 | P2            M6, line along y; M4, same as "+" terminal.
36 | P3            M6, line along x; M4, same as "+" terminal.
37 | P4            M6, polygon;      M4, same as "+" terminal.
38 | PB1           M6, polygon;      M4, same as "+" terminal.
39 | PB2           M6, polygon;      M4, same as "+" terminal.
40 | PB3           M6, polygon;      M4, same as "+" terminal.
41 | PB4           M6, polygon;      M4, same as "+" terminal.
42 | PB5           M6, polygon;      M4, same as "+" terminal.
43 | PB6           M6, polygon;      M4, same as "+" terminal.
44 | PB7           M6, polygon;      M4, same as "+" terminal.
45 | PB8           M6, polygon;      M4, same as "+" terminal.
46 | PB9           M6, polygon;      M4, same as "+" terminal.
47 | PB10          M6, polygon;      M4, same as "+" terminal.
48 | J1            M6, polygon;      M5, same as "+" terminal.
49 | J2            M6, polygon;      M5, same as "+" terminal.
50 | J3            M6, polygon;      M5, same as "+" terminal.
51 | J4            M5, polygon;      M6, same as "+" terminal.
52 | J5            M6, polygon;      M5, same as "+" terminal.
53 | J6            M6, polygon;      M5, same as "+" terminal.
54 | J7            M6, polygon;      M5, same as "+" terminal.
55 | J8            M6, polygon;      M5, same as "+" terminal.
56 | J9            M6, polygon;      M5, same as "+" terminal.
57 | J10           M6, polygon;      M5, same as "+" terminal.
58 | J11           M6, polygon;      M5, same as "+" terminal.
59 | J12           M6, polygon;      M5, same as "+" terminal.
60 | J13           M6, polygon;      M5, same as "+" terminal.
61 | J14           M6, polygon;      M5, same as "+" terminal.
62 | J15           M6, polygon;      M5, same as "+" terminal.
63 | J16           M6, polygon;      M5, same as "+" terminal.
64 | J17           M6, polygon;      M5, same as "+" terminal.
65 | J18           M6, polygon;      M5, same as "+" terminal.
66
67 SVD info: Condition nr. = 24.05; unknowns = 98; rank = 98.
68
69 Impedance   Inductance [H]       Resistance [Ohm]     AbsDiff      PercDiff
70 Name        Design      Extracted    Design      Extracted    (L only)    (L only)
71 L1          --          1.48915E-12  --          --          +1.4892E-12  --%
72 L2          4.0481E-12  4.0116E-12  --          --          -3.6504E-14 -0.90175%
73 L3          3.6036E-12  3.58661E-12  --          --          -1.6989E-14 -0.47145%
74 L4          7.2183E-12  7.19858E-12  --          --          -1.9717E-14 -0.27316%
75 L5          3.0677E-12  3.06389E-12  --          --          -3.8096E-15 -0.12418%
76 L7          2.5596E-12  2.54719E-12  --          --          -1.2411E-14 -0.48487%
77 L8          --          1.55031E-12  --          --          +1.5503E-12  --%
78 L9          4.0481E-12  4.07033E-12  --          --          +2.2227E-14 +0.54906%
79 L10         3.6036E-12  3.58197E-12  --          --          -2.1631E-14 -0.60026%
80 L11         4.3879E-12  4.36209E-12  --          --          -2.5815E-14 -0.58831%
81 L12         3.217E-12   3.21634E-12  --          --          -6.5613E-16 -0.020396%
82 L13         3.2439E-12  3.25118E-12  --          --          +7.2792E-15 +0.2244%
83 L14         --          1.54044E-12  --          --          +1.5404E-12  --%
84 L15         4.3135E-12  4.33251E-12  --          --          +1.901E-14  +0.44072%
85 L16         3.926E-12   3.92903E-12  --          --          +3.0296E-15 +0.077167%
86 L17         7.5833E-12  7.50305E-12  --          --          -8.0252E-14 -1.0583%
87 L18         1.2875E-12  1.30037E-12  --          --          +1.2867E-14 +0.99934%
88 L19         1.0678E-12  1.50349E-12  --          --          +4.3569E-13 +40.802%
89 L21         3.7382E-13  5.7611E-13   --          --          +2.0229E-13 +54.114%
90 L22         5.2995E-13  5.39797E-13  --          --          +9.8473E-15 +1.8582%
91 L23         9.5137E-13  1.06471E-12  --          --          +1.1334E-13 +11.914%
92 L24         2.5089E-12  2.50214E-12  --          --          -6.7551E-15 -0.26925%
93 L25         1.2791E-12  1.2826E-12   --          --          +3.5029E-15 +0.27386%
94 L26         3.5427E-12  3.55781E-12  --          --          +1.5113E-14 +0.42658%
95 L27         --          6.57709E-13  --          --          +6.5771E-13  --%
96 LP1          --          5.46871E-13  --          --          +5.4687E-13  --%
97 LP2          --          5.85175E-13  --          --          +5.8517E-13  --%
98 LP3          --          4.31117E-13  --          --          +4.3112E-13  --%
99 LP5          --          5.99747E-13  --          --          +5.9975E-13  --%
100 LP6          --          5.10392E-13  --          --          +5.1039E-13  --%
101 LP7          --          5.64586E-13  --          --          +5.6459E-13  --%
102 LP8          --          4.84967E-13  --          --          +4.8497E-13  --%

```

```

103 | LP10    --      4.77636E-13 --      --      +4.7764E-13 --%
104 | LP12    --      5.45247E-13 --      --      +5.4525E-13 --%
105 | LP13    --      5.44328E-13 --      --      +5.4433E-13 --%
106 | LP14    --      4.9116E-13 --      --      +4.9116E-13 --%
107 | LP16    --      4.99509E-13 --      --      +4.9951E-13 --%
108 | LP17    --      5.24198E-13 --      --      +5.242E-13 --%
109 | LP18    --      4.16652E-13 --      --      +4.1665E-13 --%
110 | LB1     --      2.10012E-12 --      --      +2.1001E-12 --%
111 | LB2     --      4.02957E-13 --      --      +4.0296E-13 --%
112 | LB3     --      2.91892E-12 --      --      +2.9189E-12 --%
113 | LB4     --      2.22202E-12 --      --      +2.222E-12 --%
114 | LB5     --      1.45598E-12 --      --      +1.456E-12 --%
115 | LB6     --      2.78673E-13 --      --      +2.7867E-13 --%
116 | LB7     --      2.99385E-12 --      --      +2.9938E-12 --%
117 | LB8     --      9.92666E-13 --      --      +9.9267E-13 --%
118 | LB9     --      4.98289E-13 --      --      +4.9829E-13 --%
119 | LB10    --      2.12412E-12 --      --      +2.1241E-12 --%
120
121 Ports   Design   Extracted  AbsDiff   PercDiff
122 J1      0.000086  0.000093558
123 J2      0.0001    0.00010794
124 J3      0.000191  0.0001998
125 J4      0.000178  0.00018513
126 J5      0.000116  0.00012397
127 J6      0.000086  0.000093558
128 J7      0.0001    0.00010794
129 J8      0.000235  0.00024373
130 J9      0.000196  0.00020513
131 J10     0.000284  0.00029299
132 J11     0.000078  0.000085495
133 J12     0.000099  0.00010693
134 J13     0.000094  0.00010169
135 J14     0.000218  0.00022671
136 J15     0.000165  0.00017332
137 J16     0.000163  0.00017134
138 J17     0.000151  0.00015939
139 J18     0.000236  0.00024495
140
141 Error bound on extracted values: 6.07859%
142
143 Deallocating memory.
144 Cycles found in 0.029 seconds.
145 SVD solution in 0.071 seconds.
146 Job finished in 675.467 seconds.

```

**Listing 4.37:** RSFQ NDROT InductEx extraction.

## Analog model

```

1  * Author: L. Schindler
2  * Version: 1.5.1
3  * Last modification date: 18 June 2020
4  * Last modification by: L. Schindler
5
6  *$Ports
7  .subckt LSmitll_NDROT a b clk q
8  .model jjmit jj(rtype=1, vg=2.8mV, cap
9    ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
10   ↪ )
11 .param B0=1
12 .param Ic0=0.0001
13 .param IcRs=100u*6.859904418
14 .param B0Rs=IcRs/Ic0*B0
15 .param Rsheet=2
16 .param Lsheet=1.13e-12
17 .param B01=2.1788
18 .param B01rx1=0.8597
19 .param B01rx3=0.9892
20 .param B01tx1=2.3613
21 .param B02=1.6498
22 .param B02rx1=1.0002
23 .param B02rx3=0.9426
24 .param B03=2.3464
25 .param B04=1.9597
26 .param B05=2.8368
27 .param B06=1.9079
28 .param B07=1.7749
29 .param B08=1.1619
30 .param B09=0.7782
31 .param B10=1.6313
32 .param IB01=0.000223851
33 .param IB01rx1=0.000134142
34 .param IB01rx3=0.000131798
35 .param IB01tx1=0.000195509
36 .param IB02=0.000152193
37 .param IB03=0.000198086
38 .param IB04=9.85166e-05
39 .param IB05=9.47282e-05
40 .param IB06=6.36747e-05
41 .param L01=7.5833e-012
42 .param L01rx1=1.9122e-012
43 .param L01rx3=1.7869e-12
44 .param L01tx1=3.5427e-12
45 .param L02=1.3381e-12
46 .param L02rx1=4.0481e-12
47 .param L02rx3=4.3135e-12
48 .param L02tx1=3.5270e-12
49 .param L03=4.3879e-12
50 .param L03rx1=3.6036e-12
51 .param L03rx3=3.9260e-12
52 .param L04=3.2170e-12
53 .param L05=7.2183e-12
54 .param L06=3.0677e-12
55 .param L07=2.5596e-12
56 .param L08=3.2439e-12
57 .param L09=3.7382e-13
58 .param L10=5.2995e-13
59 .param L11=2.5089e-12
60 .param L13=9.5137e-13
61 .param L14=4.7528e-14
62 .param L15=1.2875e-12
63 .param L16=1.0678e-12
64 .param LRB01=(RB01/Rsheet)*Lsheet
65 .param LRB01rx1=(RB01rx1/Rsheet)*Lsheet
66 .param LRB01rx3=(RB01rx3/Rsheet)*Lsheet
67 .param LRB01tx1=(RB01tx1/Rsheet)*Lsheet
68 .param LRB02=(RB02/Rsheet)*Lsheet
69 .param LRB02rx1=(RB02rx1/Rsheet)*Lsheet
70 .param LRB02rx2=(RB02rx2/Rsheet)*Lsheet
71 .param LRB02rx3=(RB02rx3/Rsheet)*Lsheet
72 .param LRB03=(RB03/Rsheet)*Lsheet
73 .param LRB04=(RB04/Rsheet)*Lsheet
74 .param LRB05=(RB05/Rsheet)*Lsheet
75 .param LRB06=(RB06/Rsheet)*Lsheet
76 .param LRB07=(RB07/Rsheet)*Lsheet
77 .param LRB08=(RB08/Rsheet)*Lsheet
78 .param LRB09=(RB09/Rsheet)*Lsheet
79 .param LRB10=(RB10/Rsheet)*Lsheet
80 .param LRB11=(RB11/Rsheet)*Lsheet
81 .param RB01=B0Rs/B01
82 .param RB01rx1=B0Rs/B01rx1
83 .param RB01rx2=B0Rs/B01rx1
84 .param RB01rx3=B0Rs/B01rx3
85 .param RB01tx1=B0Rs/B01tx1
86 .param RB02=B0Rs/B02
87 .param RB02rx1=B0Rs/B02rx1
88 .param RB02rx2=B0Rs/B02rx1
89 .param RB02rx3=B0Rs/B02rx3
90 .param RB03=B0Rs/B03
91 .param RB04=B0Rs/B04
92 .param RB05=B0Rs/B05
93 .param RB06=B0Rs/B06
94 .param RB07=B0Rs/B07
95 .param RB08=B0Rs/B08
96 .param RB09=B0Rs/B09
97 .param RB10=B0Rs/B10
98 .param RB11=B0Rs/B11
99 B01 22 66 jjmit area=B01
100 B01rx1 7 32 jjmit area=B01rx1
101 B01rx2 13 44 jjmit area=B01rx1
102 B01rx3 20 62 jjmit area=B01rx3
103 B01tx1 25 73 jjmit area=B01tx1
104 B02 18 19 jjmit area=B02
105 B02rx1 8 34 jjmit area=B02rx1
106 B02rx2 14 46 jjmit area=B02rx1
107 B02rx3 21 64 jjmit area=B02rx3
108 B03 15 48 jjmit area=B03
109 B04 11 12 jjmit area=B04
110 B05 12 50 jjmit area=B05
111 B06 9 36 jjmit area=B06
112 B07 5 6 jjmit area=B07
113 B08 6 38 jjmit area=B08
114 B09 10 16 jjmit area=B09
115 B10 23 69 jjmit area=B10
116 B11 24 71 jjmit area=B11
117 IB01 0 68 pw1(0 0 5p IB01)
118 IB01rx1 0 26 pw1(0 0 5p IB01rx1)
119 IB01rx2 0 40 pw1(0 0 5p IB01rx1)
120 IB01rx3 0 53 pw1(0 0 5p IB01rx3)
121 IB01tx1 0 55 pw1(0 0 5p IB01tx1)
122 IB02 0 41 pw1(0 0 5p IB02)
123 IB03 0 27 pw1(0 0 5p IB03)
124 IB04 0 30 pw1(0 0 5p IB04)
125 IB05 0 56 pw1(0 0 5p IB05)
126 IB06 0 17 pw1(0 0 5p IB06)
127 L01 21 22 L01
128 L01rx1 a 7 L01rx1
129 L01rx2 b 13 L01rx1

```

```

130 | L01rx3 clk 20 L01rx3
131 | L01tx1 24 25 L01tx1
132 | L02 19 58 L02
133 | L02rx1 7 28 L02rx1
134 | L02rx2 13 42 L02rx1
135 | L02rx3 20 57 L02rx3
136 | L02tx1 25 61 L02tx1
137 | L03 14 15 L03
138 | L03rx1 28 8 L03rx1
139 | L03rx2 42 14 L03rx1
140 | L03rx3 57 21 L03rx3
141 | L04 15 11 L04
142 | L05 8 9 L05
143 | L06 9 5 L06
144 | L07 31 10 L07
145 | L08 12 10 L08
146 | L09 16 54 L09
147 | L10 54 58 L10
148 | L11 23 17 L11
149 | L13 58 23 L13
150 | L14 6 31 L14
151 | L15 22 60 L15
152 | L16 60 18 L16
153 | L17 17 24 L17
154 | LP01 66 0 1.56e-13
155 | LP01rx1 32 0 3.4e-13
156 | LP01rx2 44 0 3.4e-13
157 | LP01rx3 62 0 3.4e-13
158 | LP01tx1 73 0 5e-14
159 | LP02rx1 34 0 6e-14
160 | LP02rx2 46 0 6e-14
161 | LP02rx3 64 0 6e-14
162 | LP03 48 0 1.35e-13
163 | LP05 50 0 1.46e-13
164 | LP06 36 0 1.33e-13
165 | LP08 38 0 2.16e-13
166 | LP10 69 0 1.46e-13
167 | LP11 71 0 1.35e-13
168 | LPR01 60 68 1.82e-13
169 | LPR01rx1 26 28 2e-13
170 | LPR01rx2 40 42 2e-13
171 | LPR01rx3 53 57 2e-13
172 | LPR01tx1 55 25 2e-13
173 | LPR02 41 15 1.53e-13
174 | LPR03 27 9 1.85e-13
175 | LPR04 30 31 2.506e-12
176 | LPR05 54 56 3.4e-14
177 | LRB01 67 0 LRB01
178 | LRB01rx1 33 0 LRB01rx1
179 | LRB01rx2 45 0 LRB01rx1
180 | LRB01rx3 63 0 LRB01rx3
181 | LRB01tx1 74 0 LRB01tx1
182 | LRB02 59 19 LRB02
183 | LRB02rx1 35 0 LRB02rx1
184 | LRB02rx2 47 0 LRB02rx2
185 | LRB02rx3 65 0 LRB02rx3
186 | LRB03 49 0 LRB03
187 | LRB04 43 12 LRB04
188 | LRB05 51 0 LRB05
189 | LRB06 37 0 LRB06
190 | LRB07 29 6 LRB07
191 | LRB08 39 0 LRB08
192 | LRB09 52 16 LRB09
193 | LRB10 70 0 LRB10
194 | LRB11 72 0 LRB11
195 | RB01 22 67 RB01
196 | RB01rx1 7 33 RB01rx1
197 | RB01rx2 13 45 RB01rx2
198 | RB01rx3 20 63 RB01rx3
199 | RB01tx1 25 74 RB01tx1
200 | RB02 18 59 RB02
201 | RB02rx1 8 35 RB02rx1
202 | RB02rx2 14 47 RB02rx2
203 | RB02rx3 21 65 RB02rx3
204 | RB03 15 49 RB03
205 | RB04 11 43 RB04
206 | RB05 12 51 RB05
207 | RB06 9 37 RB06
208 | RB07 5 29 RB07
209 | RB08 6 39 RB08
210 | RB09 10 52 RB09
211 | RB10 23 70 RB10
212 | RB11 24 72 RB11
213 | RINStx1 61 q 1.36
214 | .ends

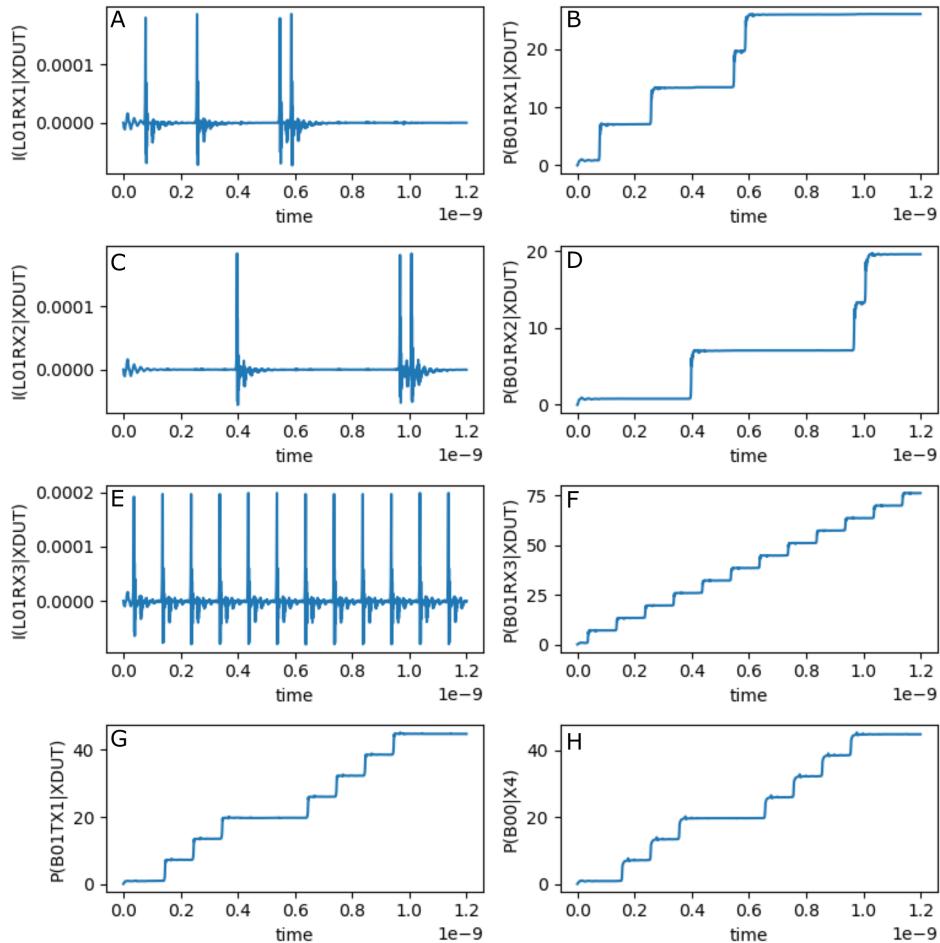
```

**Listing 4.38:** RSFQ NDROT JoSIM netlist.**Table 4.25:** RSFQ NDROT pin list.

Pin	Description
a	Data input (set signal)
b	Data input (reset signal)
clk	Clock input
q	Data output

The simulation results for the RSFQ NDROT using JoSIM is shown in Fig. 4.63. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a** (set signal),
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b** (reset signal),
- (d) the phase over the input JJ of pin **b**,
- (e) the current through the input inductor connected to pin **clk**,
- (f) the phase over the input JJ of pin **clk**,
- (g) the phase over the output JJ of pin **q**, and
- (h) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.



**Figure 4.63:** RSFQ NDROT analog simulation results.

## Digital model

```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 // -----
9 `timescale 1ps/100fs
10 module LSmitll_NDROT_v1p5 (a, b, clk, q);
11
12 input
13   a, b, clk;
14
15 output
16   q;
17
18 reg
19   q;
20
21 real
22   delay_state1_clk_q = 9.0,
23   ct_state0_b_a = 4.5,
24   ct_state1_a_b = 0.8,
25   ct_state1_clk_clk = 9.5;
26
27 reg
28   errorsignal_a,
29   errorsignal_b,
30   errorsignal_clk;
31
32 integer
33   outfile,
34   cell_state; // internal state of the cell
35
36 initial
37 begin
38     errorsignal_a = 0;
39     errorsignal_b = 0;
40     errorsignal_clk = 0;
41     cell_state = 0; // Startup state
42     q = 0; // All outputs start at 0
43 end
44
45 always @(*posedge a or negedge a) // execute at positive and negative edges of input
46 begin
47     if ($time>4) // arbitrary steady-state time)
48     begin
49         if (errorsignal_a == 1'b1) // A critical timing is active for this input
50         begin
51             outfile = $fopen("errors.txt", "a");
52             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
53                         ↪ ", $stime);
54             $fclose(outfile);
55             q <= 1'bX; // Set all outputs to unknown
56         end
57         if (errorsignal_a == 0)
58         begin
59             case (cell_state)
60             0: begin
61                 cell_state = 1; // Blocking statement -- immediately
62             end
63             1: begin
64                 errorsignal_b = 1; // Critical timing on this input; assign
65                 ↪ immediately
66                 errorsignal_b <= #(ct_state1_a_b) 0; // Clear error signal
67                 ↪ after critical timing expires

```

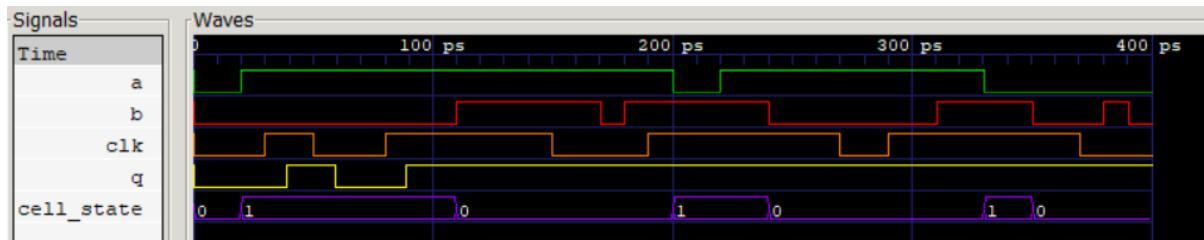
```

65           end
66       endcase
67   end
68 end
69
70 always @(posedge b or negedge b) // execute at positive and negative edges of input
71 begin
72     if ($time>4) // arbitrary steady-state time)
73     begin
74         if (errorsignal_b == 1'b1) // A critical timing is active for this input
75         begin
76             outfile = $fopen("errors.txt", "a");
77             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
78                         ↪ ", $stime);
79             $fclose(outfile);
80             q <= 1'bX; // Set all outputs to unknown
81         end
82         if (errorsignal_b == 0)
83         begin
84             case (cell_state)
85                 0: begin
86                     errorsignal_a = 1; // Critical timing on this input; assign
87                         ↪ immediately
88                     errorsignal_a <= #(ct_state0_b_a) 0; // Clear error signal
89                         ↪ after critical timing expires
90                 end
91                 1: begin
92                     cell_state = 0; // Blocking statement -- immediately
93                 end
94             endcase
95         end
96     end
97 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
98 begin
99     if ($time>4) // arbitrary steady-state time)
100    begin
101        if (errorsignal_clk == 1'b1) // A critical timing is active for this input
102        begin
103            outfile = $fopen("errors.txt", "a");
104            $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
105                         ↪ ", $stime);
106            $fclose(outfile);
107            q <= 1'bX; // Set all outputs to unknown
108        end
109        if (errorsignal_clk == 0)
110        begin
111            case (cell_state)
112                0: begin
113                    end
114                1: begin
115                    q <= #(delay_state1_clk_q) !q;
116                    errorsignal_clk = 1; // Critical timing on this input; assign
117                         ↪ immediately
118                    errorsignal_clk <= #(ct_state1_clk_clk) 0; // Clear error
119                         ↪ signal after critical timing expires
120                end
121            endcase
122        end
123    end
124 endmodule

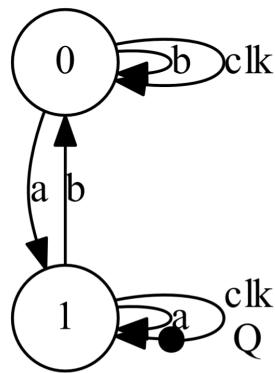
```

Listing 4.39: RSFQ NDROT verilog model.

The digital simulation results for the RSFQ NDROT is shown in Fig. 4.64 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.65.



**Figure 4.64:** RSFQ NDROT digital simulation results.



**Figure 4.65:** RSFQ NDROT Mealy finite state machine diagram.

## Power Consumption

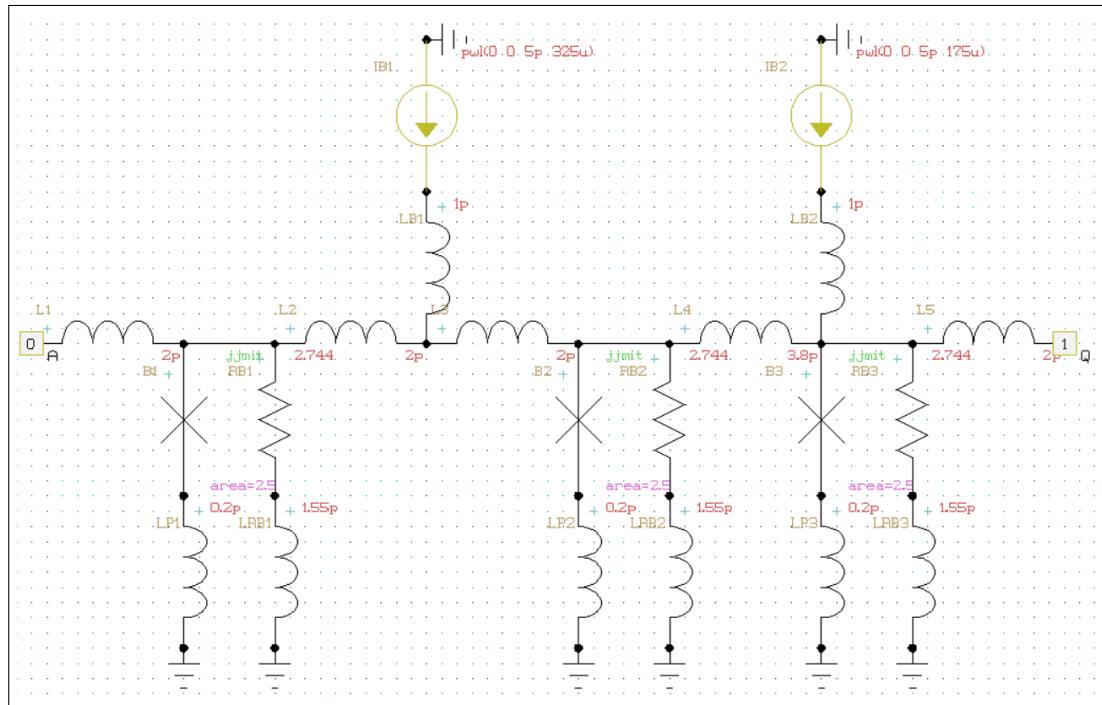
**Table 4.26:** RSFQ NDROT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	371	5.74
2	371	11.5
5	371	28.7
10	371	57.4
20	371	115
50	371	287

### 4.3.3 BUFF

The RSFQ BUFF cell is a buffer cell intended for clock balancing. It is designed to have the same a-to-q delay as the CLKSPLT, CLKSPLTT and BUFFT cell. The BUFF does not have integrated PTL transmitters and receivers and connecting the cell directly to a PTL is not recommended.

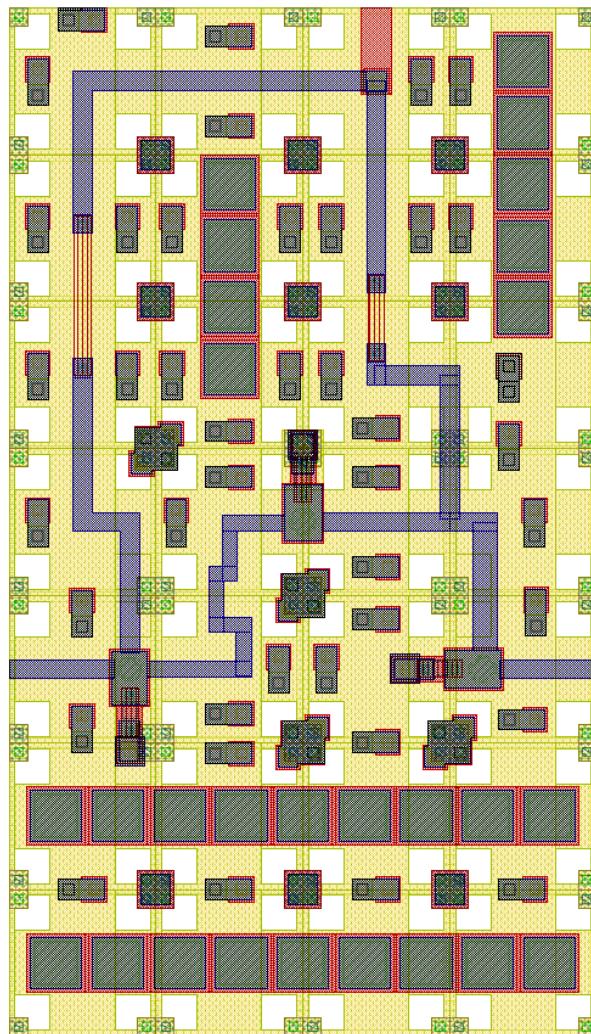
#### Schematic



**Figure 4.66:** Schematic of RSFQ BUFF.

## Layout

The physical layout for the RSFQ BUFF is shown in Fig. 4.67 and the resulting InductEx extraction is shown in Listing 4.40. The layout height is  $70 \mu m$  and the width is  $40 \mu m$ . If required, an additional and smaller layout can be made to minimize chip space for clock balancing.



**Figure 4.67:** RSFQ BUFF Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_BUFF_v1p5.GDS -n LSmitll_BUFF_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_BUFF_v1p5_idx.cir read. Totals: L = 10, k = 0, P = 7.
7 | Total fundamental loops identified in netlist = 6
8 | Using TetraHenry with analytical integration.
9 | 1192 structures read. Reduced 1192 objects to 1102 polygons and 4 terminals.
10 | Top level structure is "LSMITLL_BUFF".
11 | GDS file LSmitll_BUFF_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 | Object in layer I5 moved to TERM layer. (Pj1)
13 | Object in layer I5 moved to TERM layer. (Pj2)
14 | Object in layer I5 moved to TERM layer. (Pj3)
15 | Terminal blocks = 7; Labels = 7; Extracted Ports = 7
16 |
17 | Port           Positive terminal     Negative terminal
18 | P1             M6, line along y;  M4, same as "+" terminal.
19 | P2             M6, line along y;  M4, same as "+" terminal.
20 | PB1            M6, polygon;      M4, same as "+" terminal.
21 | PB2            M6, polygon;      M4, same as "+" terminal.
22 | J1             M6, polygon;      M5, same as "+" terminal.
23 | J2             M6, polygon;      M5, same as "+" terminal.
24 | J3             M6, polygon;      M5, same as "+" terminal.
25 |
26 | SVD info: Condition nr. = 6.023; unknowns = 20; rank = 20.
27 |
28 | Impedance     Inductance [H]       Resistance [Ohm]     AbsDiff      PercDiff
29 | Name          Design        Extracted    Design        Extracted    (L only)    (L only)
30 | L1            2E-12        2.03159E-12 --          --          +3.1593E-14 +1.5796%
31 | L2            5.2E-12       5.24662E-12 --          --          +4.6624E-14 +0.89662%
32 | L3            2.07E-12      2.03231E-12 --          --          -3.7686E-14 -1.8206%
33 | L4            2.07E-12      2.03606E-12 --          --          -3.3938E-14 -1.6395%
34 | L5            2E-12         1.93888E-12 --          --          -6.1115E-14 -3.0558%
35 | LB1           --           4.83917E-12 --          --          +4.8392E-12 --%
36 | LB2           --           3.33223E-12 --          --          +3.3322E-12 --%
37 | LP1           --           4.67809E-13 --          --          +4.6781E-13 --%
38 | LP2           --           4.70078E-13 --          --          +4.7008E-13 --%
39 | LP3           --           4.70474E-13 --          --          +4.7047E-13 --%
40 |
41 | Ports          Design        Extracted    AbsDiff      PercDiff
42 | J1            0.0002        0.00020853
43 | J2            0.00025       0.00025893
44 | J3            0.00025       0.00025893
45 |
46 | Error bound on extracted values: 1.46224%
47 |
48 | Deallocating memory.
49 | Cycles found in 0.027 seconds.
50 | SVD solution in 0.016 seconds.
51 | Job finished in 111.865 seconds.

```

**Listing 4.40:** RSFQ BUFF InductEx extraction.

## Analog model

```

1 * Author: L. Schindler
2 * Version: 1.5.1
3 * Last modification date: 11 June 2020
4 * Last modification by: L. Schindler
5
6 *$Ports
7 .subckt LSmitll_buff a q
8 .model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
9 B1 3 7 jjmit area=2.5
10 B2 4 9 jjmit area=2.5
11 B3 2 11 jjmit area=2.5
12 IB1 0 5 pwl(0 0 5p 325u)
13 IB2 0 2 pwl(0 0 5p 175u)
14 L1 a 3 2p
15 L2 3 6 2p
16 L3 6 4 2p
17 L4 4 2 3.8p
18 L5 2 q 2p
19 LB1 5 6 0.2p
20 LP1 7 0 0.2p
21 LP2 9 0 0.2p
22 LP3 11 0 0.2p
23 LRB1 3 8 1.55E-12
24 LRB2 4 10 1.55E-12
25 LRB3 12 0 1.55E-12
26 RB1 8 0 2.744
27 RB2 10 0 2.744
28 RB3 2 12 2.744
29 .ends

```

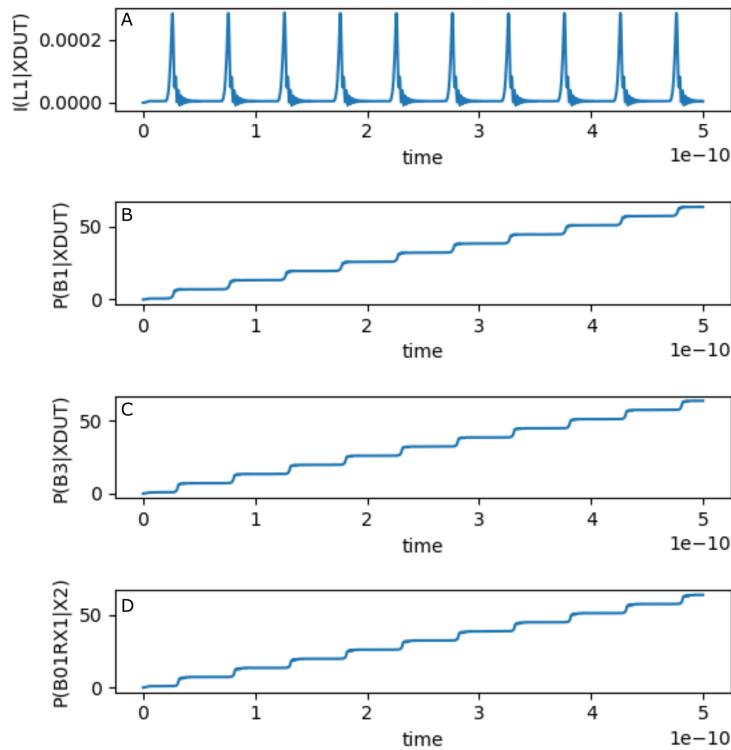
**Listing 4.41:** RSFQ BUFF JoSIM netlist.

**Table 4.27:** RSFQ BUFF pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ BUFF using JoSIM is shown in Fig. 4.68. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q**, and
- (d) the phase over the input JJ of the load circuit connected to pin **q**.



**Figure 4.68:** RSFQ BUFF analog simulation results.

## Digital model

```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 //
9 `timescale 1ps/100fs
10 module LSmitll_buff_v1p5 (a, q);
11
12 input
13   a;
14
15 output
16   q;
17
18 reg
19   q;
20
21 real
22   delay_state0_a_q = 5.5,
23   ct_state0_a_a = 3.5;
24
25 reg
26   errorsignal_a;
27
28 integer
29   outfile,
30   cell_state; // internal state of the cell
31
32 initial
33 begin
34   errorsignal_a = 0;
35   cell_state = 0; // Startup state
36   q = 0; // All outputs start at 0
37 end
38
39 always @(posedge a or negedge a) // execute at positive and negative edges of input
40 begin
41   if ($time>4) // arbitrary steady-state time)
42     begin
43       if (errorsignal_a == 1'b1) // A critical timing is active for this input
44         begin
45           outfile = $fopen("errors.txt", "a");
46           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
47                         ↪ ", $stime);
48           $fclose(outfile);
49           q <= 1'bX; // Set all outputs to unknown
50         end
51       if (errorsignal_a == 0)
52         begin
53           case (cell_state)
54             0: begin
55               q <= #(delay_state0_a_q) !q;
56               errorsignal_a = 1; // Critical timing on this input; assign
57               ↪ immediately
58               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
59               ↪ after critical timing expires
60             end
61           endcase
62         end
63     end
64   end
65 endmodule

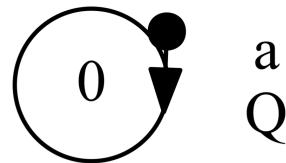
```

**Listing 4.42:** RSFQ BUFF verilog model.

The digital simulation results for the RSFQ BUFF is shown in Fig. 4.69 and the Mealy finite state machine diagram, extracted using *TimEx*, is shown in Fig. 4.70.



**Figure 4.69:** RSFQ BUFF digital simulation results.



**Figure 4.70:** RSFQ BUFF Mealy finite state machine diagram.

## Power Consumption

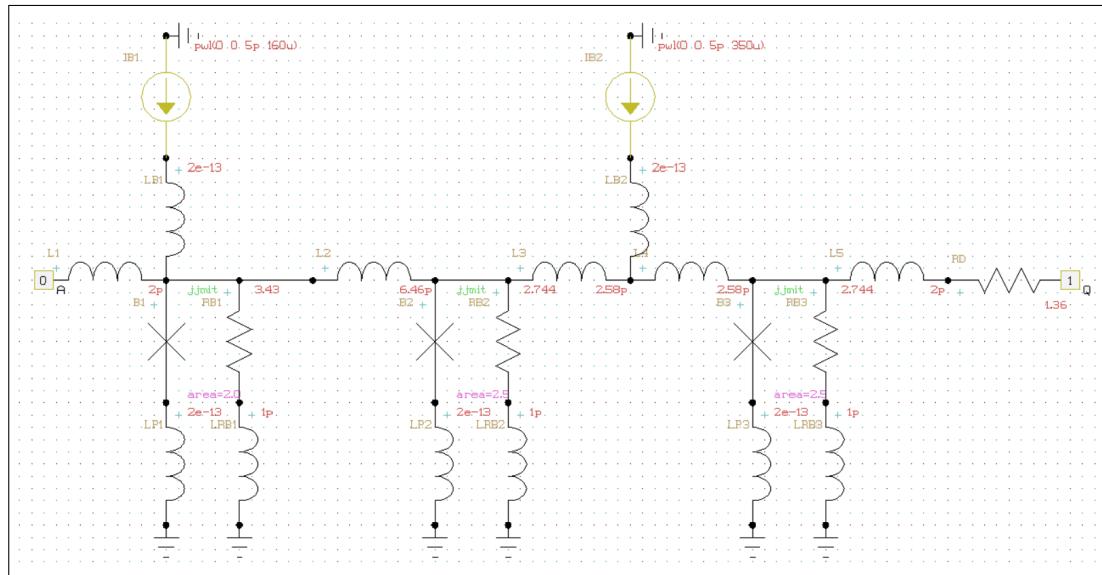
**Table 4.28:** RSFQ BUFF power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	130	1.55
2	130	3.10
5	130	7.75
10	130	15.5
20	130	31.0
50	130	77.5

#### 4.3.4 BUFFT

The RSFQ BUFFT cell is a buffer cell intended for clock balancing. It is designed to have the same a-to-q delay as the CLKSPLT, CLKSPLTT and BUFF cell. The BUFFT is designed with integrated PTL drivers and receivers and is intended to be connected directly to PTLs.

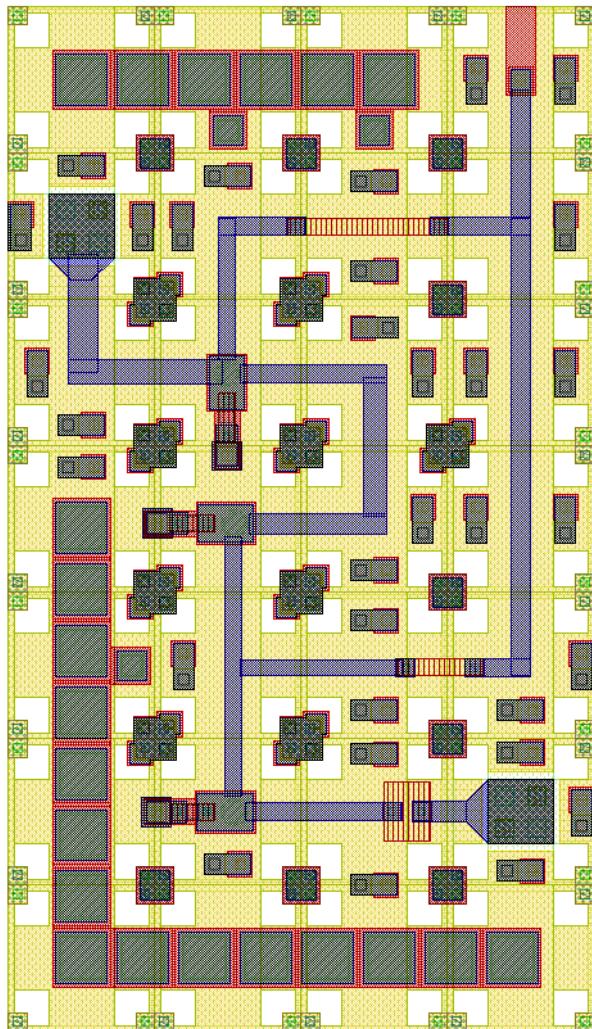
#### Schematic



**Figure 4.71:** Schematic of RSFQ BUFFT.

## Layout

The physical layout for the RSFQ BUFFT is shown in Fig. 4.72 and the resulting InductEx extraction is shown in Listing 4.43. The layout height is  $70 \mu\text{m}$  and the width is  $40 \mu\text{m}$ .



**Figure 4.72:** RSFQ BUFFT Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_BUFFT_v1p5.GDS -n LSmitll_BUFFT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_BUFFT_v1p5_idx.cir read. Totals: L = 10, k = 0, P = 7.
7 | Total fundamental loops identified in netlist = 6
8 | Using TetraHenry with analytical integration.
9 | 1188 structures read. Reduced 1188 objects to 1118 polygons and 4 terminals.
10 | Top level structure is "LSMITLL_BUFFT_V1P5".
11 | GDS file LSmitll_BUFFT_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 | Object in layer I5 moved to TERM layer. (Pj1)
13 | Object in layer I5 moved to TERM layer. (Pj2)
14 | Object in layer I5 moved to TERM layer. (Pj3)
15 | Terminal blocks = 7; Labels = 7; Extracted Ports = 7
16 |
17 | Port           Positive terminal     Negative terminal
18 | P1             M6, line along x;  M4, same as "+" terminal.
19 | P2             M6, polygon;       M4, same as "+" terminal.
20 | PB1            M6, polygon;       M4, same as "+" terminal.
21 | PB2            M6, polygon;       M4, same as "+" terminal.
22 | J1             M6, polygon;       M5, same as "+" terminal.
23 | J2             M6, polygon;       M5, same as "+" terminal.
24 | J3             M6, polygon;       M5, same as "+" terminal.
25 |
26 | SVD info: Condition nr. = 4.249; unknowns = 20; rank = 20.
27 |
28 | Impedance      Inductance [H]      Resistance [Ohm]      AbsDiff      PercDiff
29 | Name    Design    Extracted    Design    Extracted    (L only)    (L only)
30 | L1      --        2.88269E-12  --        --        +2.8827E-12  --%
31 | L2      5.2E-12   5.21421E-12  --        --        +1.421E-14   +0.27327%
32 | L3      2.07E-12  2.06667E-12  --        --        -3.3273E-15  -0.16074%
33 | L4      2.07E-12  2.06239E-12  --        --        -7.6057E-15  -0.36743%
34 | L5      --        2.40125E-12  --        --        +2.4013E-12  --%
35 | LB1    --        3.20092E-12  --        --        +3.2009E-12  --%
36 | LB2    --        2.8577E-12   --        --        +2.8577E-12  --%
37 | LP1    --        5.24521E-13  --        --        +5.2452E-13  --%
38 | LP2    --        5.12732E-13  --        --        +5.1273E-13  --%
39 | LP3    --        5.0586E-13   --        --        +5.0586E-13  --%
40 |
41 | Ports   Design    Extracted  AbsDiff    PercDiff
42 | J1      0.0002    0.00020853
43 | J2      0.00025   0.00025893
44 | J3      0.00025   0.00025893
45 |
46 | Error bound on extracted values: 0.779537%
47 |
48 | Deallocating memory.
49 | Cycles found in 0.029 seconds.
50 | SVD solution in 0.014 seconds.
51 | Job finished in 112.339 seconds.

```

**Listing 4.43:** RSFQ BUFFT InductEx extraction.

## Analog model

```

1 * Author: L. Schindler
2 * Version: 1.5.1
3 * Last modification date: 18 June 2020
4 * Last modification by: L. Schindler
5
6 *$Ports
7 .subckt LSmitll_bufft a q
8 .model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
9 B1 2 3 jjmit area=2.0
10 B2 6 7 jjmit area=2.5
11 B3 11 12 jjmit area=2.5
12 IB1 0 5 pwl(0 0 5p 160u)
13 IB2 0 10 pwl(0 0 5p 350u)
14 L1 a 2 2p
15 L2 2 6 5.2p
16 L3 6 9 2.07p
17 L4 9 11 2.07p
18 L5 11 14 2p
19 RD 14 q 1.36
20 LP1 3 0 0.2p
21 LP2 7 0 0.2p
22 LP3 12 0 0.2p
23 RB1 2 4 3.43
24 RB2 6 8 2.744
25 RB3 11 13 2.744
26 LRB1 4 0 1.94p
27 LRB2 8 0 1.55p
28 LRB3 13 0 1.55p
29 LB1 2 5 1p
30 LB2 9 10 1p
31 .ends

```

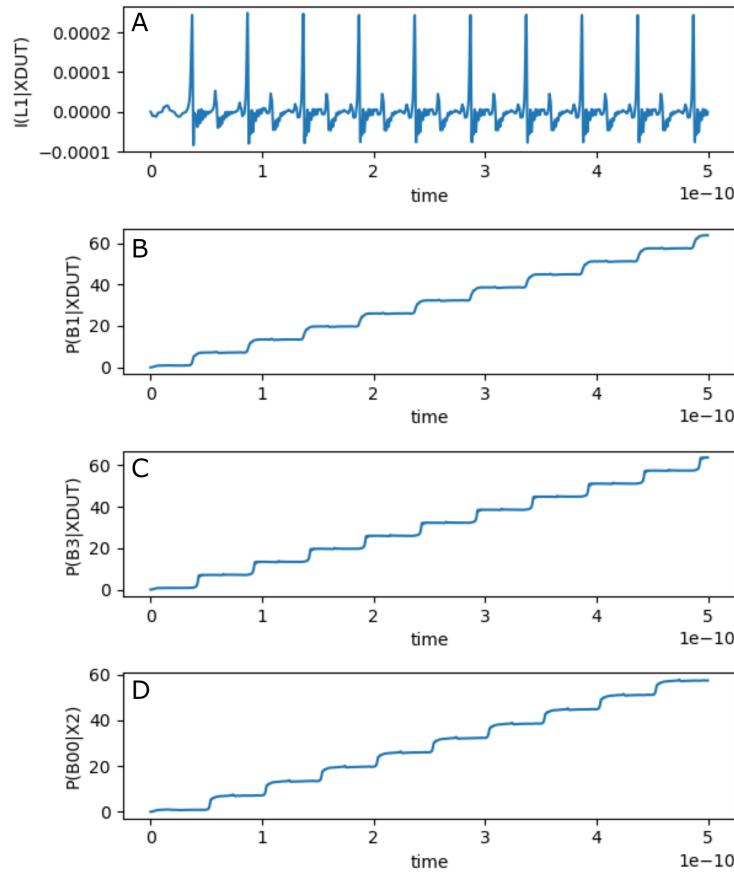
**Listing 4.44:** RSFQ BUFFT JoSIM netlist.

**Table 4.29:** RSFQ BUFFT pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ BUFFT using JoSIM is shown in Fig. 4.73. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q**, and
- (d) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.



**Figure 4.73:** RSFQ BUFFT analog simulation results.

## Digital model

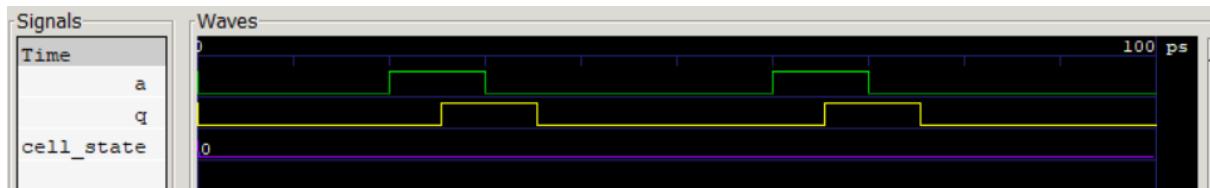
```

1 // -----
2 // Automatically extracted verilog file, created with TimEx v2.05
3 // Timing description and structural design for IARPA-BAA-14-03 via
4 // U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
5 // IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
6 // For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
7 // (c) 2016-2018 Stellenbosch University
8 //
9 `timescale 1ps/100fs
10 module LSmitll_bufft_v1p5 (a, q);
11
12 input
13   a;
14
15 output
16   q;
17
18 reg
19   q;
20
21 real
22   delay_state0_a_q = 5.5,
23   ct_state0_a_a = 7.0;
24
25 reg
26   errorsignal_a;
27
28 integer
29   outfile,
30   cell_state; // internal state of the cell
31
32 initial
33 begin
34   errorsignal_a = 0;
35   cell_state = 0; // Startup state
36   q = 0; // All outputs start at 0
37 end
38
39 always @(posedge a or negedge a) // execute at positive and negative edges of input
40 begin
41   if ($time>4) // arbitrary steady-state time)
42     begin
43       if (errorsignal_a == 1'b1) // A critical timing is active for this input
44         begin
45           outfile = $fopen("errors.txt", "a");
46           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
47                         ↪ ", $stime);
48           $fclose(outfile);
49           q <= 1'bX; // Set all outputs to unknown
50         end
51       if (errorsignal_a == 0)
52         begin
53           case (cell_state)
54             0: begin
55               q <= #(delay_state0_a_q) !q;
56               errorsignal_a = 1; // Critical timing on this input; assign
57               ↪ immediately
58               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
59               ↪ after critical timing expires
60             end
61           endcase
62         end
63     end
64   end
65 endmodule

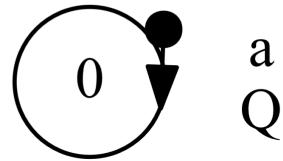
```

**Listing 4.45:** RSFQ BUFFT verilog model.

The digital simulation results for the RSFQ BUFFT is shown in Fig. 4.74 and the Mealy finite state machine diagram, extracted using *TimEx*, is shown in Fig. 4.75.



**Figure 4.74:** RSFQ BUFFT digital simulation results.



**Figure 4.75:** RSFQ BUFFT Mealy finite state machine diagram.

## Power Consumption

**Table 4.30:** RSFQ BUFFT power consumption.

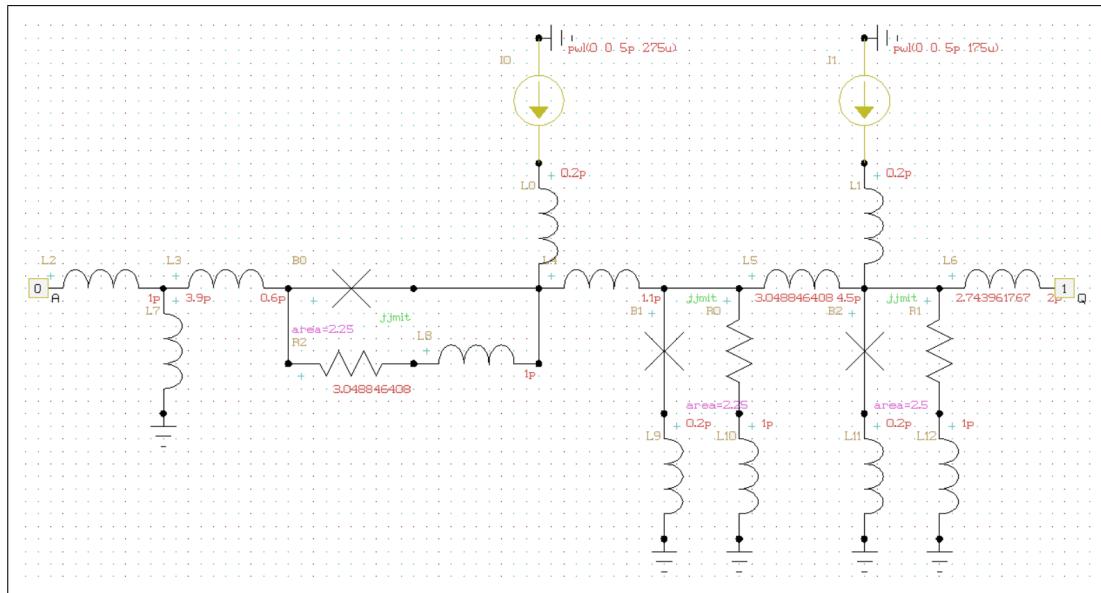
Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	133	1.45
2	133	2.89
5	133	7.24
10	133	14.5
20	133	28.9
50	133	72.4

## 4.4 Interface cells

### 4.4.1 DCSFQ

The RSFQ DCSFQ is an interface cell designed to convert input voltage pulses into SFQ pulses. The DCSFQ does not have an integrated PTL transmitter and is not intended to connect directly to a PTL output.

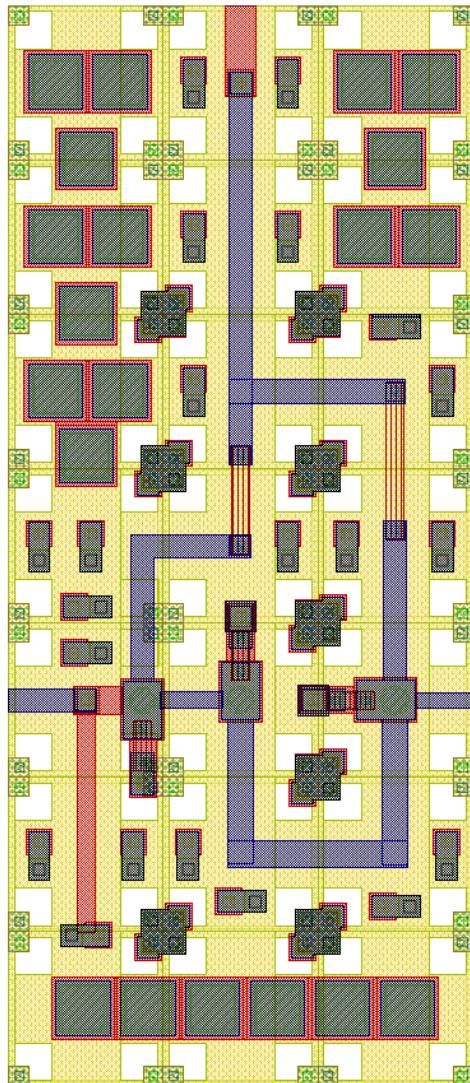
#### Schematic



**Figure 4.76:** Schematic of RSFQ DCSFQ.

## Layout

The physical layout for the RSFQ DCSFQ is shown in Fig. 4.77 and the resulting InductEx extraction is shown in Listing 4.46. The layout height is  $70 \mu\text{m}$  and the width is  $30 \mu\text{m}$ .



**Figure 4.77:** RSFQ DCSFQ Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_DCSFQ_v1p5.GDS -n LSmitll_DCSFQ_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_DCSFQ_v1p5_idx.cir read. Totals: L = 10, k = 0, P = 7.
7 | Total fundamental loops identified in netlist = 6
8 | Using TetraHenry with analytical integration.
9 | 838 structures read. Reduced 838 objects to 805 polygons and 4 terminals.
10 | Top level structure is "LSMITLL_DCSFQ_V1P5".
11 | GDS file LSmitll_DCSFQ_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 | Object in layer I5 moved to TERM layer. (Pj1)
13 | Object in layer I5 moved to TERM layer. (Pj2)
14 | Object in layer I5 moved to TERM layer. (Pj3)
15 | Terminal blocks = 7; Labels = 7; Extracted Ports = 7
16 |
17 | Port           Positive terminal     Negative terminal
18 | P1             M6, line along y;    M4, same as "+" terminal.
19 | P2             M6, line along y;    M4, same as "+" terminal.
20 | PB1            M6, polygon;       M4, same as "+" terminal.
21 | PB2            M6, polygon;       M4, same as "+" terminal.
22 | J1             M5, polygon;       M6, same as "+" terminal.
23 | J2             M6, polygon;       M5, same as "+" terminal.
24 | J3             M6, polygon;       M5, same as "+" terminal.
25 |
26 | SVD info: Condition nr. = 7.119; unknowns = 20; rank = 20.
27 |
28 | Impedance      Inductance [H]      Resistance [Ohm]      AbsDiff      PercDiff
29 | Name   Design   Extracted   Design   Extracted   (L only)   (L only)
30 | L1     1E-12    1.47068E-12  --        --        +4.7068E-13 +47.068%
31 | L2     3.9E-12   3.91959E-12  --        --        +1.959E-14  +0.50232%
32 | L3     6E-13     5.95746E-13  --        --        -4.2537E-15 -0.70894%
33 | L4     1.1E-12   1.12164E-12  --        --        +2.1639E-14 +1.9672%
34 | L5     4.5E-12   4.70289E-12  --        --        +2.0289E-13 +4.5087%
35 | L6     2E-12     1.52806E-12  --        --        -4.7194E-13 -23.597%
36 | LPB2    --       4.95543E-13  --        --        +4.9554E-13  --%
37 | LPB3    --       4.20985E-13  --        --        +4.2099E-13  --%
38 | LB1     --       2.98424E-12  --        --        +2.9842E-12  --%
39 | LB2     --       2.22935E-12  --        --        +2.2294E-12  --%
40 |
41 | Ports   Design   Extracted   AbsDiff   PercDiff
42 | J1      0.000225  0.00023374
43 | J2      0.000225  0.00023374
44 | J3      0.00025   0.00025893
45 |
46 | Error bound on extracted values: 3.60869%
47 |
48 | Deallocating memory.
49 | Cycles found in 0.026 seconds.
50 | SVD solution in 0.005 seconds.
51 | Job finished in 70.993 seconds.

```

**Listing 4.46:** RSFQ DCSFQ InductEx extraction.

## Analog model

```

1 * Author: L. Schindler
2 * Version: 1.5.1
3 * Last modification date: 18 June 2020
4 * Last modification by: L. Schindler
5
6 * Ports
7 .subckt LSmitll_DCSFQ a q
8 .model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
9 B0 3 4 jjmit area=2.25
10 B1 5 10 jjmit area=2.25
11 B2 6 12 jjmit area=2.5
12 I0 0 7 pwl(0 0 5p 275u)
13 I1 0 8 pwl(0 0 5p 175u)
14 L0 7 4 0.2p
15 L1 8 6 0.2p
16 L2 a 9 1p
17 L3 9 3 0.6p
18 L4 4 5 1.1p
19 L5 5 6 4.5p
20 L6 6 q 2p
21 L7 9 0 3.9p
22 L8 14 4 1p
23 L9 10 0 0.2p
24 L10 11 0 1p
25 L11 12 0 0.2p
26 L12 13 0 1p
27 R0 5 11 3.048846408
28 R1 6 13 2.743961767
29 R2 3 14 3.048846408
30 .ends

```

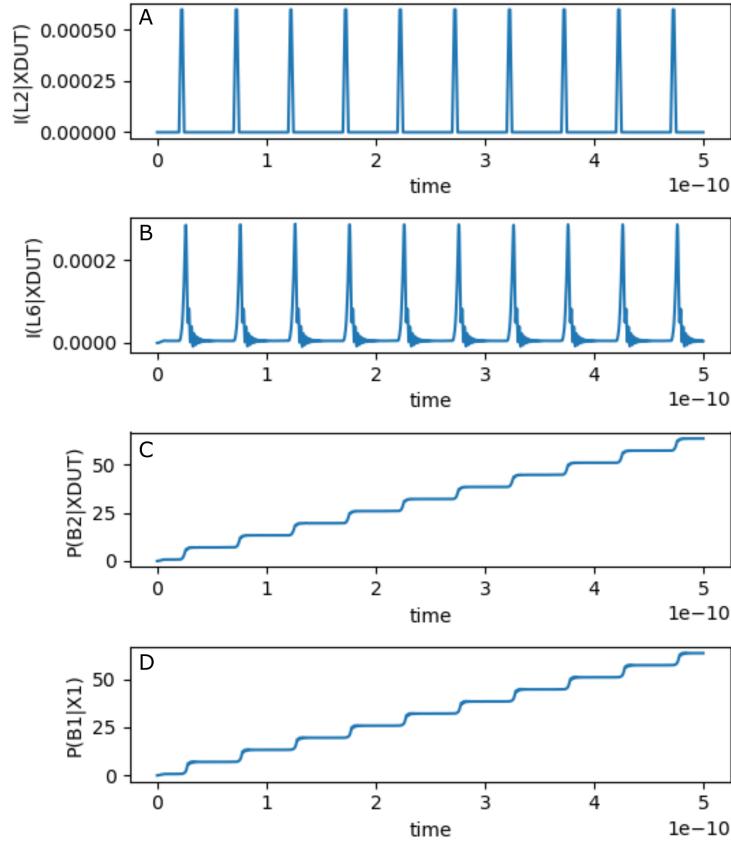
**Listing 4.47:** RSFQ DCSFQ JoSIM netlist.

**Table 4.31:** RSFQ DCSFQ pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ DCSFQ using JoSIM is shown in Fig. 4.78. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the current through the output inductor connected to pin **q**,
- (c) the phase over the output JJ of pin **q**, and
- (d) the phase over the input JJ of the load circuit connected to pin **q**.

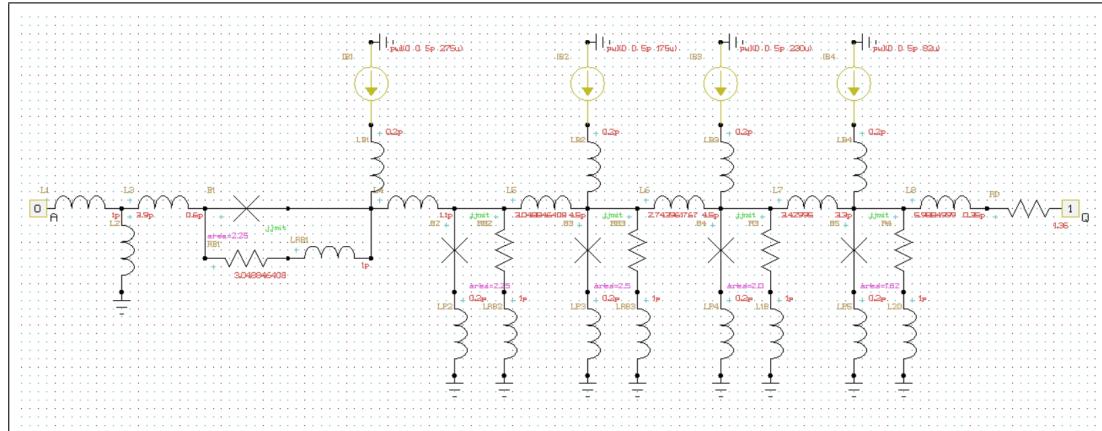


**Figure 4.78:** RSFQ DCSFQ analog simulation results.

#### 4.4.2 DCSFQ-PTLTX

The RSFQ DCSFQ-PTLTX is an interface cell designed to convert input voltage pulses into SFQ pulses. The DCSFQ-PTLTX has an integrated PTL transmitter and is intended to connect directly to a PTL output.

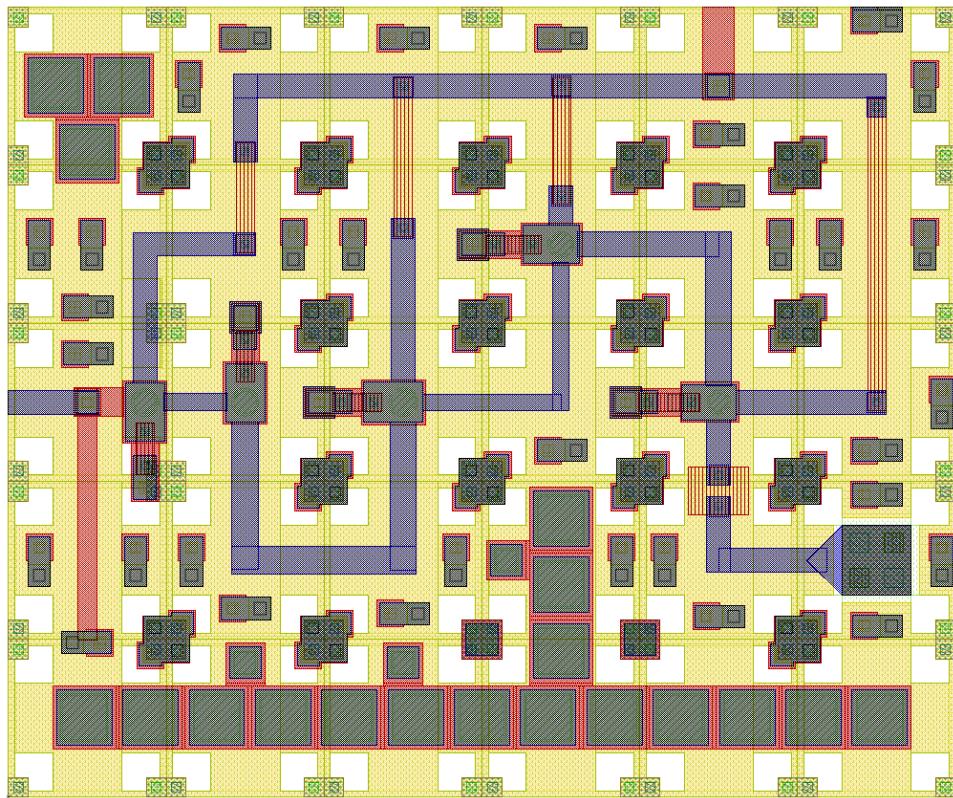
## Schematic



**Figure 4.79:** Schematic of RSFQ DCSFQ-PTLTX.

## Layout

The physical layout for the RSFQ DCSFQ-PTLTX is shown in Fig. 4.80 and the resulting InductEx extraction is shown in Listing 4.48. The layout height is  $50 \mu\text{m}$  and the width is  $60 \mu\text{m}$ .



**Figure 4.80:** RSFQ DCSFQ-PTLTX Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_DCSFQ_PTLTX_v1p5.GDS -n LSmitll_DCSFQ_PTLTX_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf
5 |   ↳ -th
6 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
7 | Spice netlist LSmitll_DCSFQ_PTLTX_v1p5_idx.cir read. Totals: L = 16, k = 0, P = 11.
8 | Total fundamental loops identified in netlist = 10
9 | Using TetraHenry with analytical integration.
10 | 1289 structures read. Reduced 1289 objects to 1193 polygons and 6 terminals.
11 | Top level structure is "LSMITLL_DCSFQ-PTLTX_V1P5".
12 | GDS file LSmitll_DCSFQ_PTLTX_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
13 | Object in layer I5 moved to TERM layer. (Pj1)
14 | Object in layer I5 moved to TERM layer. (Pj2)
15 | Object in layer I5 moved to TERM layer. (Pj3)
16 | Object in layer I5 moved to TERM layer. (Pj4)
17 | Object in layer I5 moved to TERM layer. (Pj5)
18 | Terminal blocks = 11; Labels = 11; Extracted Ports = 11
19 |
20 | Port           Positive terminal    Negative terminal
21 | P1             M6, line along y;  M4, same as "+" terminal.
22 | P2             M6, polygon;       M4, same as "+" terminal.
23 | PB1            M6, polygon;       M4, same as "+" terminal.
24 | PB2            M6, polygon;       M4, same as "+" terminal.
25 | PB3            M6, polygon;       M4, same as "+" terminal.
26 | PB4            M6, polygon;       M4, same as "+" terminal.
27 | J1              M5, polygon;       M6, same as "+" terminal.
28 | J2              M6, polygon;       M5, same as "+" terminal.
29 | J3              M6, polygon;       M5, same as "+" terminal.
30 | J4              M6, polygon;       M5, same as "+" terminal.
31 | J5              M6, polygon;       M5, same as "+" terminal.
32 | SVD info: Condition nr. = 13.28; unknowns = 32; rank = 32.
33 |
34 | Impedance     Inductance [H]      Resistance [Ohm]      AbsDiff      PercDiff
35 | Name          Design        Extracted      Design        Extracted      (L only)      (L only)
36 | L1            --           1.47032E-12  --           --           +1.4703E-12  --%
37 | L2            3.9E-12      3.90992E-12  --           --           +9.916E-15   +0.25426%
38 | L3            6E-13        5.98562E-13  --           --           -1.4379E-15  -0.23966%
39 | L4            1.1E-12      1.1097E-12   --           --           +9.7048E-15  +0.88225%
40 | L5            4.5E-12      4.51344E-12  --           --           +1.3442E-14  +0.29871%
41 | L6            4.5E-12      4.48805E-12  --           --           -1.1947E-14  -0.26548%
42 | L7            3.3E-12      3.31827E-12  --           --           +1.8274E-14  +0.55374%
43 | L8            --           9.57773E-13  --           --           +9.5777E-13  --%
44 | LP2           --           5.05901E-13  --           --           +5.059E-13   --%
45 | LP3           --           5.07474E-13  --           --           +5.0747E-13  --%
46 | LP4           --           4.58516E-13  --           --           +4.5852E-13  --%
47 | LP5           --           4.75969E-13  --           --           +4.7597E-13  --%
48 | LB1           --           2.98109E-12  --           --           +2.9811E-12  --%
49 | LB2           --           2.11931E-12  --           --           +2.1193E-12  --%
50 | LB3           --           5.96227E-13  --           --           +5.9623E-13  --%
51 | LB4           --           2.03793E-12  --           --           +2.0379E-12  --%
52 |
53 | Ports         Design        Extracted      AbsDiff      PercDiff
54 | J1            0.000225    0.00023374
55 | J2            0.000225    0.00023374
56 | J3            0.00025     0.00025893
57 | J4            0.0002      0.00020853
58 | J5            0.000162    0.00017055
59 |
60 | Error bound on extracted values: 3.89487%
61 |
62 | Deallocating memory.
63 | Cycles found in 0.030 seconds.
64 | SVD solution in 0.008 seconds.
65 | Job finished in 109.458 seconds.

```

**Listing 4.48:** RSFQ DCSFQ-PTLTX InductEx extraction.

## Analog model

```

1 * Author: L. Schindler
2 * Version: 1.5.1
3 * Last modification date: 18 June 2020
4 * Last modification by: L. Schindler
5
6 * Copyright (c) 2018-2020 Lieze Schindler, Stellenbosch University
7
8 * Permission is hereby granted, free of charge, to any person obtaining a copy
9 * of this cell library and associated documentation files (the "Library"), to deal
10 * in the Library without restriction, including without limitation the rights
11 * to use, copy, modify, merge, publish, distribute, sublicense, and/or sell
12 * copies of the Library, and to permit persons to whom the Library is
13 * furnished to do so, subject to the following conditions:
14
15 * The above copyright notice and this permission notice shall be included in all
16 * copies or substantial portions of the Library.
17
18 * THE LIBRARY IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR
19 * IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY,
20 * FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE
21 * AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER
22 * LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM,
23 * OUT OF OR IN CONNECTION WITH THE LIBRARY OR THE USE OR OTHER DEALINGS IN THE
24 * LIBRARY.
25
26 *For questions about the library, contact Lieze Schindler, 17528283@sun.ac.za
27
28 * Ports
29 .subckt LSmitll_DCSFQ_PTLTX a q
30 .model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
31 .param B0=1
32 .param Ic0=0.0001
33 .param IcRs=100u*6.859904418
34 .param B0Rs=IcRs/Ic0*B0
35 .param Rsheet=2
36 .param Lsheet=1.13e-12
37 .param LB=0.2p
38 .param LP=0.2p
39 .param B1=2.25
40 .param B2=2.25
41 .param B3=2.5
42 .param B4=2
43 .param B5=1.62
44 .param IB1=275u
45 .param IB2=175u
46 .param IB3=230u
47 .param IB4=82u
48 .param L1=1p
49 .param L2=3.9p
50 .param L3=0.6p
51 .param L4=1.1p
52 .param L5=4.5p
53 .param L6=4.5p
54 .param L7=3.3p
55 .param L8=0.35p
56 .param RD=1.36
57 .param RB1=B0Rs/B1
58 .param RB2=B0Rs/B2
59 .param RB3=B0Rs/B3
60 .param RB4=B0Rs/B4
61 .param RB5=B0Rs/B5
62 .param LRB1=(RB1/Rsheet)*Lsheet
63 .param LRB2=(RB2/Rsheet)*Lsheet
64 .param LRB3=(RB3/Rsheet)*Lsheet
65 .param LRB4=(RB4/Rsheet)*Lsheet
66 .param LRB5=(RB5/Rsheet)*Lsheet
67

```

```

68 | B1 2 3 jjmit area=B1
69 | B2 6 7 jjmit area=B2
70 | B3 9 10 jjmit area=B3
71 | B4 13 14 jjmit area=B4
72 | B5 17 18 jjmit area=B5
73 | IB1 0 5 pwl(0 0 5p IB1)
74 | IB2 0 12 pwl(0 0 5p IB2)
75 | IB3 0 16 pwl(0 0 5p IB3)
76 | IB4 0 20 pwl(0 0 5p IB4)
77 | LB1 5 3 LB
78 | LB2 12 9 LB
79 | LB3 16 13 LB
80 | LB4 20 17 LB
81 | L1 a 1 L1
82 | L2 1 0 L2
83 | L3 1 2 L3
84 | L4 3 6 L4
85 | L5 6 9 L5
86 | L6 9 13 L6
87 | L7 13 17 L7
88 | L8 17 21 L8
89 | LP2 7 0 LP
90 | LP3 10 0 LP
91 | LP4 14 0 LP
92 | LP5 18 0 LP
93 | LRB1 2 4 LRB1
94 | LRB2 8 0 LRB2
95 | LRB3 11 0 LRB3
96 | LRB4 15 0 LRB4
97 | LRB5 19 0 LRB5
98 | RB1 4 3 RB1
99 | RB2 6 8 RB2
100 | RB3 9 11 RB3
101 | RB4 13 15 RB4
102 | RB5 17 19 RB5
103 | RD 21 q RD
104 | .ends

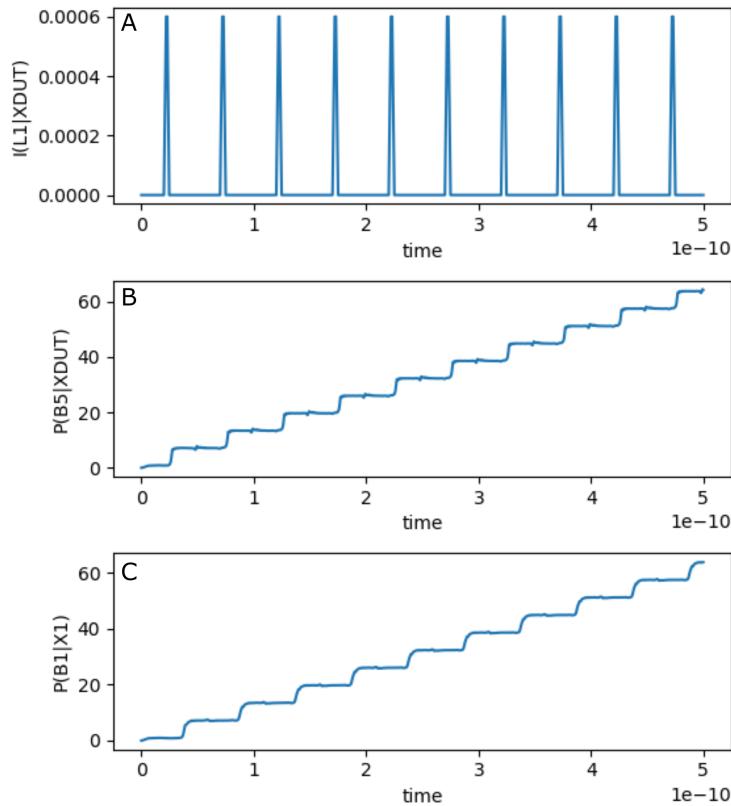
```

**Listing 4.49:** RSFQ DCSFQ-PTLTX JoSIM netlist.**Table 4.32:** RSFQ DCSFQ-PTLTX pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ DCSFQ-PTLTX using JoSIM is shown in Fig. 4.81. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the output JJ of pin **q**, and
- (c) the phase over the input JJ of the load circuit connected through a PTL to pin **q**.

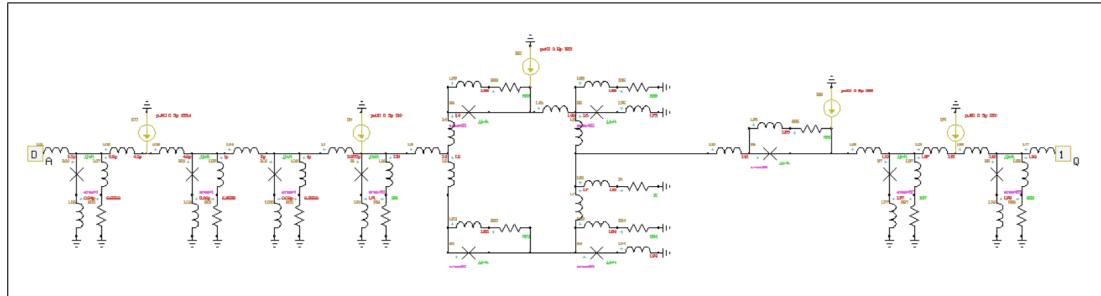


**Figure 4.81:** RSFQ DCSFQ-PTLTX analog simulation results.

### 4.4.3 PTLRX-SFQDC

The RSFQ PTLRX-SFQDC is an interface cell designed to convert SFQ pulses to an output voltage level which can be measured by standard equipment. The PTLRX-SFQDC has an integrated PTL receiver and is intended to be connected directly to a PTL input.

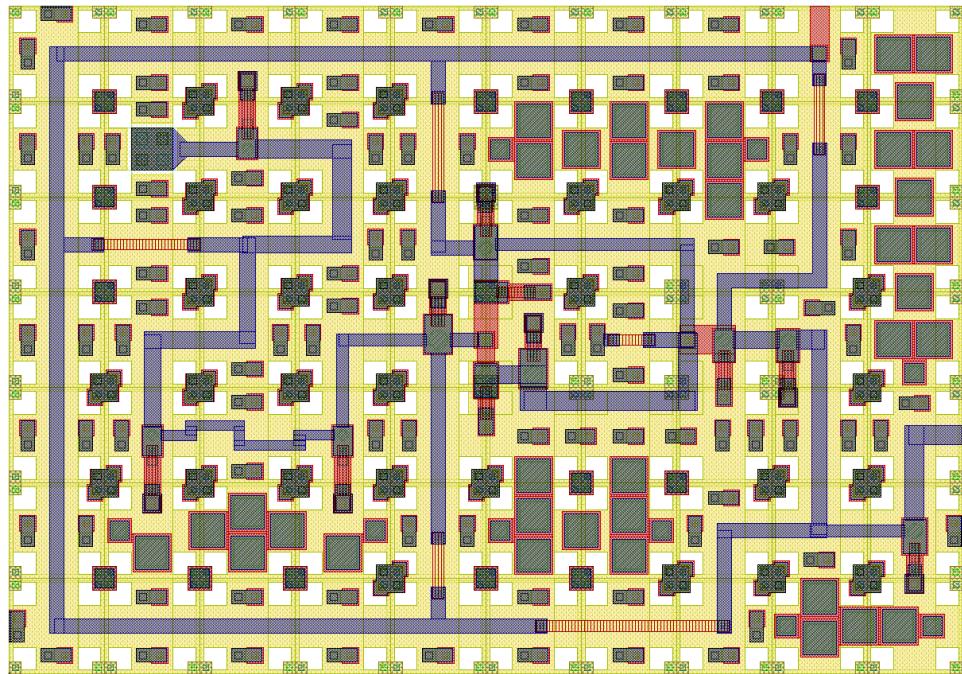
#### Schematic



**Figure 4.82:** Schematic of RSFQ PTLRX-SFQDC.

## Layout

The physical layout for the RSFQ PTLRX-SFQDC is shown in Fig. 4.83 and the resulting InductEx extraction is shown in Listing 4.50. The layout height is  $70 \mu\text{m}$  and the width is  $100 \mu\text{m}$ .



**Figure 4.83:** RSFQ PTLRX-SFQDC Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_PTLRX_SFQDC.GDS -n LSmitll_PTLRX_SFQDC_v1p5_idx.cir -l mitll_sfq5ee_set2.lfd -th
5 | Techfile mitll_sfq5ee_set2.lfd read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_PTLRX_SFQDC_v1p5_idx.cir read. Totals: L = 29, k = 0, P = 19.
7 | Total fundamental loops identified in netlist = 16
8 | Using TetraHenry with analytical integration.
9 | 3001 structures read. Reduced 3001 objects to 2770 polygons and 8 terminals.
10 | Top level structure is "LSMITLL_PTLRX_SFQDC".
11 | GDS file LSmitll_PTLRX_SFQDC.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 | Object in layer I5 moved to TERM layer. (Pj1)
13 | Object in layer I5 moved to TERM layer. (Pj2)
14 | Object in layer I5 moved to TERM layer. (Pj3)
15 | Object in layer I5 moved to TERM layer. (Pj4)
16 | Object in layer I5 moved to TERM layer. (Pj5)
17 | Object in layer I5 moved to TERM layer. (Pj6)
18 | Object in layer I5 moved to TERM layer. (Pj7)
19 | Object in layer I5 moved to TERM layer. (Pj8)
20 | Object in layer I5 moved to TERM layer. (Pj9)
21 | Object in layer I5 moved to TERM layer. (Pj10)
22 | Object in layer I5 moved to TERM layer. (Pj11)
23 | Terminal blocks = 19; Labels = 19; Extracted Ports = 19
24
25 | Port           Positive terminal    Negative terminal
26 | P1            M6, line along y;  M4, same as "+" terminal.
27 | P2            M6, line along y;  M4, same as "+" terminal.
28 | PR1           M6, polygon;      M4, same as "+" terminal.
29 | PB1           M6, polygon;      M4, same as "+" terminal.
30 | PB2           M6, polygon;      M4, same as "+" terminal.
31 | PB3           M6, polygon;      M4, same as "+" terminal.

```

```

32 | PB4          M6, polygon;      M4, same as "+" terminal.
33 | PB5          M6, polygon;      M4, same as "+" terminal.
34 | J1           M6, polygon;      M5, same as "+" terminal.
35 | J2           M6, polygon;      M5, same as "+" terminal.
36 | J3           M6, polygon;      M5, same as "+" terminal.
37 | J4           M6, polygon;      M5, same as "+" terminal.
38 | J5           M5, polygon;      M6, same as "+" terminal.
39 | J6           M6, polygon;      M5, same as "+" terminal.
40 | J7           M5, polygon;      M6, same as "+" terminal.
41 | J8           M6, polygon;      M5, same as "+" terminal.
42 | J9           M5, polygon;      M6, same as "+" terminal.
43 | J10          M6, polygon;      M5, same as "+" terminal.
44 | J11          M6, polygon;      M5, same as "+" terminal.
45
46 SVD info: Condition nr. = 10.31; unknowns = 58; rank = 58.
47
48 Impedance     Inductance [H]      Resistance [Ohm]      AbsDiff      PercDiff
49 Name          Design       Extracted    Design       Extracted   (L only)    (L only)
50 L1            --          1.49897E-12  --          --          +1.499E-12  --%
51 L2            4.3E-12    4.28097E-12  --          --          -1.9028E-14 -0.4425%
52 L3            4.6E-12    4.58405E-12  --          --          -1.5946E-14 -0.34666%
53 L4            5E-12      5.02465E-12  --          --          +2.4655E-14 +0.49309%
54 L5            3.822E-12  3.79261E-12  --          --          -2.9385E-14 -0.76885%
55 L6            8.27E-13   8.30297E-13  --          --          +3.2969E-15 +0.39865%
56 L7            1.12884E-12 1.16984E-12  --          --          +4.1002E-14 +3.6322%
57 L9            5.94E-12   5.94915E-12  --          --          +9.1498E-15 +0.15404%
58 L10           1.111E-12  1.10679E-12  --          --          -4.2145E-15 -0.37934%
59 L11           3.216E-12  3.23679E-12  --          --          +2.0788E-14 +0.64639%
60 L12           9.1E-13    8.90652E-13  --          --          -1.9348E-14 -2.1262%
61 L14           2.15E-13   5.767E-13   --          --          +3.617E-13 +168.23%
62 L15           9.54E-13   9.62382E-13  --          --          +8.3823E-15 +0.87865%
63 L16           3.699E-12  3.7028E-12   --          --          +3.7977E-15 +0.10267%
64 L17           2.01E-12   2.0198E-12  --          --          +9.8041E-15 +0.48776%
65 L18           --          2.4843E-12  --          --          +2.4843E-12 --%
66 LB1           --          1.26626E-12  --          --          +1.2663E-12 --%
67 LB2           --          3.93331E-12  --          --          +3.9333E-12 --%
68 LB3           --          1.90746E-12  --          --          +1.9075E-12 --%
69 LB4           --          5.3918E-12   --          --          +5.3918E-12 --%
70 LB5           --          3.7848E-12  --          --          +3.7848E-12 --%
71 LP1           --          5.10892E-13  --          --          +5.1089E-13 --%
72 LP2           --          6.02837E-13  --          --          +6.0284E-13 --%
73 LP3           --          5.97395E-13  --          --          +5.9739E-13 --%
74 LP4           --          4.67037E-13  --          --          +4.6704E-13 --%
75 LP6           --          4.99355E-13  --          --          +4.9935E-13 --%
76 LP8           --          4.69276E-13  --          --          +4.6928E-13 --%
77 LP10          --          5.0831E-13   --          --          +5.0831E-13 --%
78 LP11          --          5.23487E-13  --          --          +5.2349E-13 --%
79
80 Ports         Design       Extracted   AbsDiff      PercDiff
81 J1            0.0001     0.00010794
82 J2            0.0001     0.00010794
83 J3            0.0001     0.00010794
84 J4            0.000325   0.00033376
85 J5            0.00015    0.00015829
86 J6            0.000175   0.00018327
87 J7            0.0002     0.00020853
88 J8            0.0003     0.00030903
89 J9            0.00015   0.00015829
90 J10           0.00015   0.00015829
91 J11           0.0002     0.00020853
92
93 Error bound on extracted values: 1.65942%
94
95 Deallocating memory.
96 Cycles found in 0.028 seconds.
97 SVD solution in 0.028 seconds.
98 Job finished in 393.767 seconds.

```

Listing 4.50: RSFQ PTLRX-SFQDC InductEx extraction.

## Analog model

```

1 * Author: L. Schindler
2 * Version: 1.5.1
3 * Last modification date: 18 June 2020
4 * Last modification by: L. Schindler
5
6 * Ports
7 .subckt LSmitll_PTLRX_SFQDC a q
8 .model jjmit jj(rtype=1, vg=2.8mV, cap
9   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
10  ↪ )
11 B00 103 108 jjmit area=1
12 B01 104 110 jjmit area=1
13 B02 105 112 jjmit area=1
14 I00 0 106 pw1(0 0 5p 155u)
15 L00 106 107 0.2p
16 L01 a 103 0.2p
17 L02 103 107 4.3p
18 L03 107 104 4.6p
19 L04 104 105 5p
20 L05 105 5001 2.3p
21 L06 108 0 0.34p
22 L07 109 0 0.5p
23 L08 110 0 0.06p
24 L09 111 0 1p
25 L010 112 0 0.03p
26 L011 113 0 1p
27 R00 103 109 6.859904418
28 R01 104 111 6.859904418
29 R02 105 113 6.859904418
30 .param B0=1
31 .param Ic0=0.0001
32 .param IcRs=100u*6.859904418
33 .param B0Rs=IcRs/Ic0*B0
34 .param Rsheet=2
35 .param Lsheet=1.13e-12
36 .param B1=3.25
37 .param B2=2.00
38 .param B3=1.50
39 .param B4=3.00
40 .param B5=1.75
41 .param B6=1.50
42 .param B7=1.50
43 .param B8=2.00
44 .param L1=1.522p
45 .param L3=0.827p
46 .param L4=1.12884p
47 .param L5=1.11098p
48 .param L6=5.940p
49 .param L7=3.216p
50 .param L10=0.215p
51 .param L13=3.699p
52 .param L17=1.510p
53 .param L18=2.010p
54 .param L19=0.954p
55 .param L4b=0.178p
56 .param LB1=(RB1/Rsheet)*Lsheet
57 .param LB2=(RB2/Rsheet)*Lsheet
58 .param LB3=(RB3/Rsheet)*Lsheet
59 .param LB4=(RB4/Rsheet)*Lsheet
60 .param LB5=(RB5/Rsheet)*Lsheet
61 .param LB6=(RB6/Rsheet)*Lsheet
62 .param LB7=(RB7/Rsheet)*Lsheet
63 .param LB8=(RB8/Rsheet)*Lsheet
64 .param LP1=0.140p
65 .param LP4=0.524p
66 .param LP5=0.516p
67 .param LP7=0.086p
68 .param LP8=0.226p
69 .param LR1=0.91p
70 .param R1=0.375
71 .param RB1=B0Rs/B1
72 .param RB2=B0Rs/B2
73 .param RB3=B0Rs/B3
74 .param RB4=B0Rs/B4
75 .param RB5=B0Rs/B5
76 .param RB6=B0Rs/B6
77 .param RB7=B0Rs/B7
78 .param IB1=280u
79 .param IB2=150u
80 .param IB3=220u
81 .param IB4=80u
82 B1 8 20 jjmit area=B1
83 B2 12 13 jjmit area=B2
84 B3 3 4 jjmit area=B3
85 B4 13 29 jjmit area=B4
86 B5 5 16 jjmit area=B5
87 B6 6 7 jjmit area=B6
88 B7 10 22 jjmit area=B7
89 B8 11 24 jjmit area=B8
90 IB1 0 8 pw1(0 0 5p IB1)
91 IB2 0 4 pw1(0 0 5p IB2)
92 IB3 0 7 pw1(0 0 5p IB3)
93 IB4 0 18 pw1(0 0 5p IB4)
94 L1 5001 8 L1
95 L3 8 17 L3
96 L4 3 17 L4
97 L5 17 12 L5
98 L6 5 9 L6
99 L7 9 13 L7
100 L10 9 6 L10
101 L13 10 18 L13
102 L17 11 q L17
103 L18 18 11 L18
104 L19 7 10 L19
105 L4b 4 5 L4b
106 LB1 8 21 LB1
107 LB2 12 27 LB2
108 LB3 3 14 LB3
109 LB4 13 28 LB4
110 LB5 5 15 LB5
111 LB6 6 19 LB6
112 LB7 10 23 LB7
113 LB8 11 25 LB8
114 LP1 20 0 LP1
115 LP4 29 0 LP4
116 LP5 16 0 LP5
117 LP7 22 0 LP7
118 LP8 24 0 LP8
119 LR1 9 26 LR1
120 R1 26 0 R1
121 RB1 21 0 RB1
122 RB2 27 13 RB2
123 RB3 14 4 RB3
124 RB4 28 0 RB4
125 RB5 15 0 RB5
126 RB6 19 7 RB6
127 RB7 23 0 RB7
128 RB8 25 0 RB8
129 .ends

```

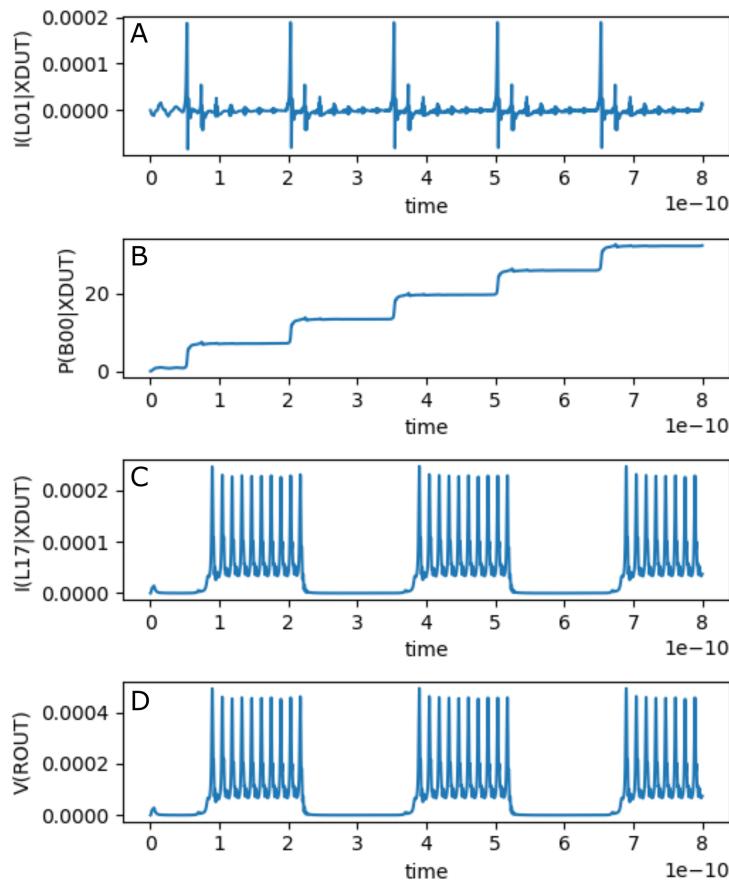
**Listing 4.51:** RSFQ PTLRX-SFQDC JoSIM netlist.

**Table 4.33:** RSFQ PTLRX-SFQDC pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ PTLRX-SFQDC using JoSIM is shown in Fig. 4.84. The figure shows the graph for:

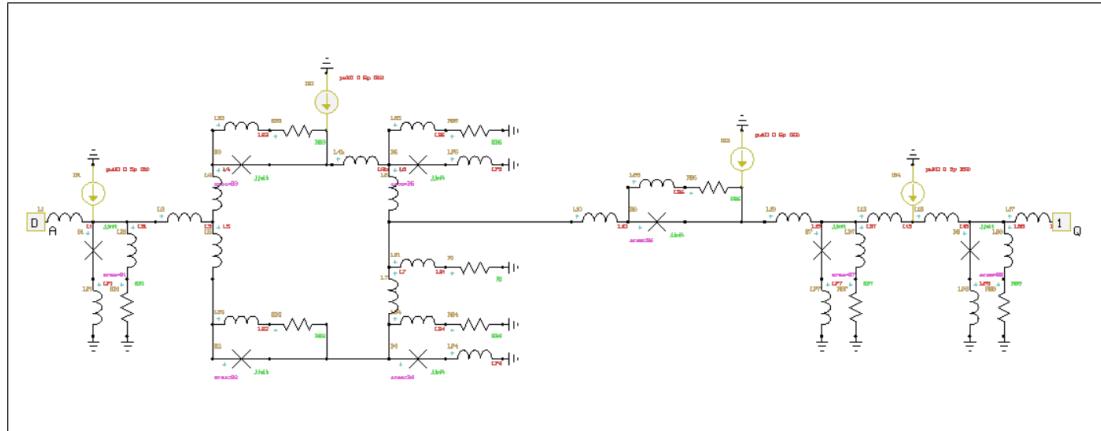
- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the output inductor connected to pin **q**, and
- (c) the voltage over the load resistor connected to pin **q**.

**Figure 4.84:** RSFQ PTLRX-SFQDC analog simulation results.

#### 4.4.4 SFQDC

The RSFQ SFQDC is an interface cell designed to convert SFQ pulses to an output voltage level which can be measured by standard equipment. The SFQDC does not have an integrated PTL receiver and is not intended to be connected directly to a PTL input.

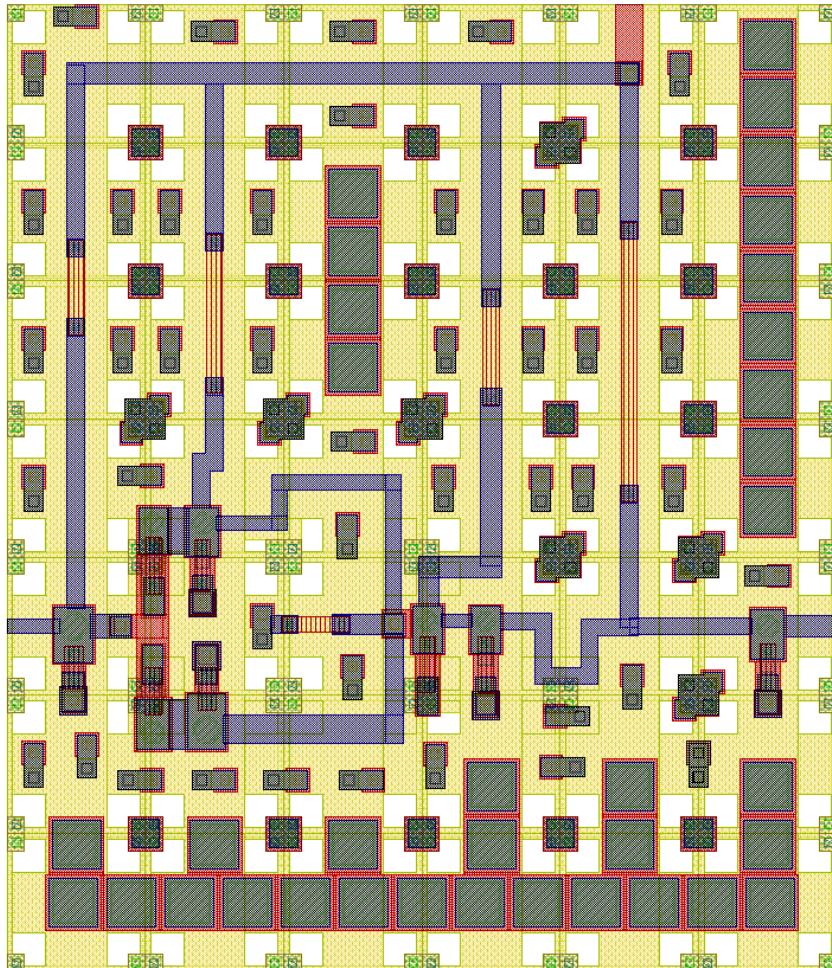
##### Schematic



**Figure 4.85:** Schematic of RSFQ SFQDC.

## Layout

The physical layout for the RSFQ SFQDC is shown in Fig. 4.86 and the resulting InductEx extraction is shown in Listing 4.52. The layout height is  $70 \mu m$  and the width is  $60 \mu m$ .



**Figure 4.86:** RSFQ SFQDC Layout

```

1 | InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2 | Licensed to:
3 |   SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4 | LSmitll_SFQDC_v1p5.gds -n LSmitll_SFQDC_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5 | Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6 | Spice netlist LSmitll_SFQDC_v1p5_idx.cir read. Totals: L = 21, k = 0, P = 15.
7 | Total fundamental loops identified in netlist = 12
8 | Using TetraHenry with analytical integration.
9 | 1715 structures read. Reduced 1715 objects to 1577 polygons and 7 terminals.
10 | Top level structure is "LSMITLL_SFQDC1".
11 | GDS file LSmitll_SFQDC_v1p5.gds read: db units in 1E-9 m, 0.001 units per user unit.
12 | Object in layer I5 moved to TERM layer. (Pj1)
13 | Object in layer I5 moved to TERM layer. (Pj2)
14 | Object in layer I5 moved to TERM layer. (Pj3)
15 | Object in layer I5 moved to TERM layer. (Pj4)
16 | Object in layer I5 moved to TERM layer. (Pj5)
17 | Object in layer I5 moved to TERM layer. (Pj6)
18 | Object in layer I5 moved to TERM layer. (Pj7)
19 | Object in layer I5 moved to TERM layer. (Pj8)
20 | Terminal blocks = 15; Labels = 15; Extracted Ports = 15

```

```

21
22 Port           Positive terminal    Negative terminal
23 P1             M6, line along y;  M4, same as "+" terminal.
24 P2             M6, polygon;      M4, same as "+" terminal.
25 P3             M6, polygon;      M4, same as "+" terminal.
26 P4             M6, polygon;      M4, same as "+" terminal.
27 P5             M6, polygon;      M4, same as "+" terminal.
28 P6             M6, polygon;      M4, same as "+" terminal.
29 P7             M6, line along y; M4, same as "+" terminal.
30 J1             M6, polygon;      M5, same as "+" terminal.
31 J2             M5, polygon;      M6, same as "+" terminal.
32 J3             M5, polygon;      M6, same as "+" terminal.
33 J4             M6, polygon;      M5, same as "+" terminal.
34 J5             M6, polygon;      M5, same as "+" terminal.
35 J6             M5, polygon;      M6, same as "+" terminal.
36 J7             M6, polygon;      M5, same as "+" terminal.
37 J8             M6, polygon;      M5, same as "+" terminal.
38
39 SVD info: Condition nr. = 6.634; unknowns = 42; rank = 42.
40
41 Impedance     Inductance [H]      Resistance [Ohm]    AbsDiff   PercDiff
42 Name          Design       Extracted   Design       Extracted  (L only)  (L only)
43 L1            1.522E-12  1.41237E-12 --        --        -1.0963E-13 -7.2029%
44 L3            8.27E-13   9.13884E-13 --        --        +8.6884E-14 +10.506%
45 L4            1.12884E-12 1.2865E-12 --        --        +1.5766E-13 +13.967%
46 L5            1.11098E-12 1.31119E-12 --        --        +2.0021E-13 +18.021%
47 L5B           3.216E-12  3.31349E-12 --        --        +9.7492E-14 +3.0315%
48 L6            5.94E-12   5.80096E-12 --        --        -1.3904E-13 -2.3407%
49 L10           2.15E-13   4.43293E-13 --        --        +2.2829E-13 +106.18%
50 L19           9.54E-13   7.57432E-13 --        --        -1.9657E-13 -20.605%
51 L13           3.699E-12  3.47827E-12 --        --        -2.2073E-13 -5.9674%
52 L18           2.01E-12   2.08681E-12 --        --        +7.6812E-14 +3.8215%
53 L17           1.51E-12   1.22092E-12 --        --        -2.8908E-13 -19.144%
54 LR1           9.1E-13    9.09181E-13 --        --        -8.1939E-16 -0.090042%
55 LB1           --          4.77388E-12 --        --        +4.7739E-12 --%
56 LB2           --          2.20374E-12 --        --        +2.2037E-12 --%
57 LB3           --          3.68595E-12 --        --        +3.686E-12 --%
58 LB4           --          2.08951E-12 --        --        +2.0895E-12 --%
59 LP1           --          3.69143E-13 --        --        +3.6914E-13 --%
60 LP4           --          4.10393E-13 --        --        +4.1039E-13 --%
61 LP5           --          4.92418E-13 --        --        +4.9242E-13 --%
62 LP7           --          5.08136E-13 --        --        +5.0814E-13 --%
63 LP8           --          4.00262E-13 --        --        +4.0026E-13 --%
64
65 Ports          Design      Extracted  AbsDiff   PercDiff
66 J1             0.000325  0.00033376
67 J2             0.0002    0.00020853
68 J3             0.00015   0.00015829
69 J4             0.0003    0.00030903
70 J5             0.000175  0.00018327
71 J6             0.00015   0.00015829
72 J7             0.00015   0.00015829
73 J8             0.0002    0.00020853
74
75 Error bound on extracted values: 5.15319%
76
77 Deallocating memory.
78 Cycles found in 0.028 seconds.
79 SVD solution in 0.015 seconds.
80 Job finished in 199.026 seconds.

```

**Listing 4.52:** RSFQ SFQDC InductEx extraction.

## Analog model

```

1  * Author: L. Schindler
2  * Version: 1.5.1
3  * Last modification date: 25 June 2020
4  * Last modification by: L. Schindler
5
6  *$ports      a      q
7  .subckt LSmitll_SFQDC a q
8  .model jjmit jj(rtype=1, vg=2.8mV, cap
9    ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
10   ↪ )
11  .param B0=1
12  .param Ic0=0.0001
13  .param IcRs=100u*6.859904418
14  .param B0Rs=IcRs/Ic0*B0
15  .param Rsheet=2
16  .param Lsheet=1.13e-12
17  .param B1=3.25
18  .param B2=2.00
19  .param B3=1.50
20  .param B4=3.00
21  .param B5=1.75
22  .param B6=1.50
23  .param B7=1.50
24  .param B8=2.00
25  .param L1=1.522p
26  .param L3=0.827p
27  .param L4=1.12884p
28  .param L5=1.11098p
29  .param L6=5.940p
30  .param L7=3.216p
31  .param L10=0.215p
32  .param L13=3.699p
33  .param L17=1.510p
34  .param L18=2.010p
35  .param L19=0.954p
36  .param L4b=0.178p
37  .param LB1=(RB1/Rsheet)*Lsheet
38  .param LB2=(RB2/Rsheet)*Lsheet
39  .param LB3=(RB3/Rsheet)*Lsheet
40  .param LB4=(RB4/Rsheet)*Lsheet
41  .param LB5=(RB5/Rsheet)*Lsheet
42  .param LB6=(RB6/Rsheet)*Lsheet
43  .param LB7=(RB7/Rsheet)*Lsheet
44  .param LB8=(RB8/Rsheet)*Lsheet
45  .param LP1=0.140p
46  .param LP4=0.524p
47  .param LP5=0.516p
48  .param LP7=0.086p
49  .param LP8=0.226p
50  .param LR1=0.91p
51  .param R1=0.375
52  .param RB1=B0Rs/B1
53  .param RB2=B0Rs/B2
54  .param RB3=B0Rs/B3
55  .param RB4=B0Rs/B4
56  .param RB5=B0Rs/B5
57  .param RB6=B0Rs/B6
58  .param RB7=B0Rs/B7
59  .param RB8=B0Rs/B8
60  .param IB1=280u
61  .param IB2=150u
62  B1 8 20 jjmit area=B1
63  B2 12 13 jjmit area=B2
64  B3 3 4 jjmit area=B3
65  B4 13 29 jjmit area=B4
66  B5 5 16 jjmit area=B5
67  B6 6 7 jjmit area=B6
68  B7 10 22 jjmit area=B7
69  B8 11 24 jjmit area=B8
70  IB1 0 8 pw1(0 0 5p IB1)
71  IB2 0 4 pw1(0 0 5p IB2)
72  IB3 0 7 pw1(0 0 5p IB3)
73  IB4 0 18 pw1(0 0 5p IB4)
74  L1 a 8 L1
75  L3 8 17 L3
76  L4 3 17 L4
77  L5 17 12 L5
78  L6 5 9 L6
79  L7 9 13 L7
80  L10 9 6 L10
81  L13 10 18 L13
82  L17 11 q L17
83  L18 18 11 L18
84  L19 7 10 L19
85  L4b 4 5 L4b
86  LB1 8 21 LB1
87  LB2 12 27 LB2
88  LB3 3 14 LB3
89  LB4 13 28 LB4
90  LB5 5 15 LB5
91  LB6 6 19 LB6
92  LB7 10 23 LB7
93  LB8 11 25 LB8
94  LP1 20 0 LP1
95  LP4 29 0 LP4
96  LP5 16 0 LP5
97  LP7 22 0 LP7
98  LP8 24 0 LP8
99  LR1 9 26 LR1
100 R1 26 0 R1
101 RB1 21 0 RB1
102 RB2 27 13 RB2
103 RB3 14 4 RB3
104 RB4 28 0 RB4
105 RB5 15 0 RB5
106 RB6 19 7 RB6
107 RB7 23 0 RB7
108 RB8 25 0 RB8
109 .ends

```

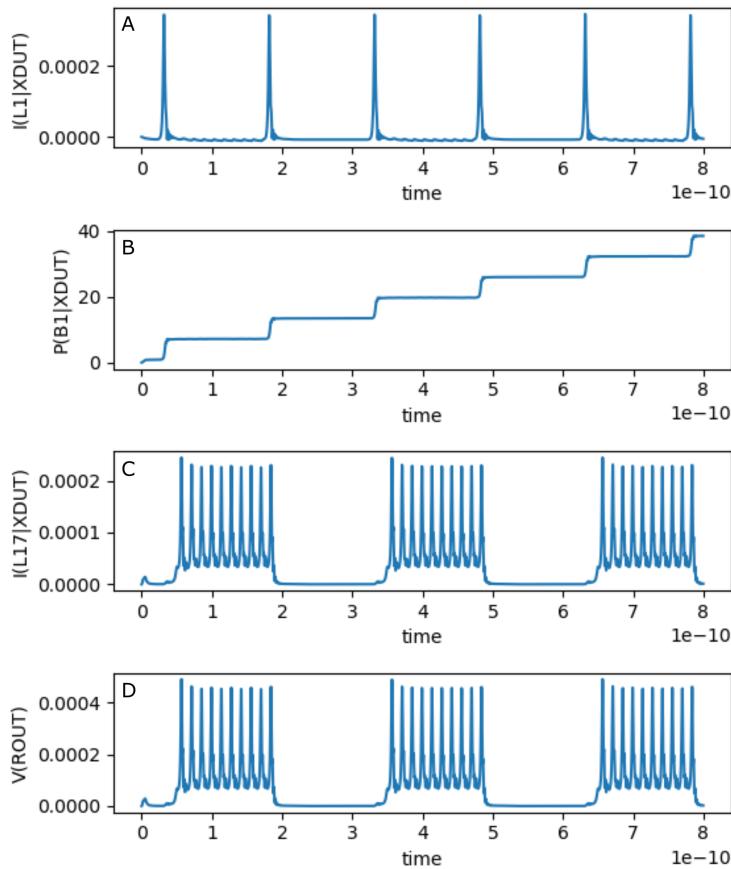
**Listing 4.53:** RSFQ SFQDC JoSIM netlist.

**Table 4.34:** RSFQ SFQDC pin list.

Pin	Description
<b>a</b>	Data input
<b>q</b>	Data output

The simulation results for the RSFQ SFQDC using JoSIM is shown in Fig. 4.87. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the output inductor connected to pin **q**, and
- (c) the voltage over the load resistor connected to pin **q**.

**Figure 4.87:** RSFQ SFQDC analog simulation results.

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