

# **CHAPTER SEVEN**

## **CUSTOM ASYNCHRONOUS RECEIVER/TRANSMITTER**

### **SOFTWARE DESIGN INFORMATION**

#### **INCLUDES:**

- CART** - Custom Asynchronous Receiver / Transmitter
- UART** - Universal Asynchronous Receiver / Transmitter

**CHAPTER 7**  
**CUSTOM ASYNCHRONOUS RECEIVER / TRANSMITTER**  
**SOFTWARE DESIGN INFORMATION**

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# CHAPTER 7

## CUSTOM ASYNCHRONOUS RECEIVER / TRANSMITTER

### SOFTWARE DESIGN INFORMATION

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## CHAPTER 7

### CUSTOM ASYNCHRONOUS RECEIVER / TRANSMITTER SOFTWARE DESIGN INFORMATION

#### 7-0 INTRODUCTION

The Custom Asynchronous Receiver/Transmitter (CART) featured on-board the 81C62 RAM/CART device and the 81C65 RAM/CART/DUCE device is an I/O port used for adding serial data communications to an 806X family system. This port is capable of operating in either of two modes: CART mode or Universal Asynchronous Receiver/Transmitter (UART) mode.

The CART mode supports the Ford Motor Company Data Communication Link (DCL) protocol while requiring minimal software overhead and processor intervention. In the CART mode, this I/O port serially communicates with other devices using a time division multiplex protocol. This protocol allows the port to handle a full block of data (called a frame) without software intervention. The frame consists of synchronization information and up to fifteen information words for user data transactions. The synchronization information requires this port to serve as the link master and all other devices on the DCL as slaves.

The UART mode provides a system with a simple alternative to the CART mode by supporting the most common and basic type of half-duplex industrial-standard serial data communication protocol. In the UART mode, the serial I/O port is configured to function as a double-buffered transmitter and receiver. The serial data format in the UART mode consists of a start bit, eight user data bits, and two stop bits. No master/slave relationship is required for the UART mode.

All serial I/O port serial data communications are asynchronous and occur in a half-duplex mode of operation at one-of-four program-selectable rates: 2400, 4800, 9600, or 19200 baud. An internal crystal oscillator generates the baud rate and all internal port timing signals. The oscillator is designed to operate with an external 4.9152 MHz crystal. The port provides automatic serial data formatting and stripping; however, it does not generate nor check data parity.

The serial I/O port maintains the individual status as well as the overall status of all transmit and receive serial transactions. The port provides false start bit detection for data reception. Upon completion of certain port operations, the port can be programmed to output an external interrupt signal to request service from a microprocessor.

The serial I/O port also features: a software controllable pause mode which can be used for halting port operations, a software initiated hardware reset capability, and an IC manufacturer test mode. The serial I/O port operates independently of all other on-board device circuits except when the port is accessed by a microprocessor. All software-accessible serial I/O port circuits are memory-mapped to enable direct accessing by the microprocessor and to simplify programming.

The paragraphs that follow provide information for developing software programs on the CART. Information contained in this chapter includes software examples that may be useful in an application program. It is assumed that the reader is familiar with the 8061/8065 microprocessor instruction set to be able to understand these examples. For additional information on the CART, refer to the "EEC-IV 806X Family Custom ICs Architecture and Hardware Reference Manual".

## 7-1 CART MODE

The following paragraphs describe the custom asynchronous receiver/transmitter (CART) mode of operation.

### 7-1.1 CART SERIAL DATA COMMUNICATIONS PROTOCOL

The CART mode enables the port to serially communicate with other devices using a time division protocol. This protocol allows the port to handle a full block of data (referred to as a frame) following initial software set-up. A frame consists of synchronization information and from zero to fifteen information words (IWs). The information words are provided for user serial data transactions. The number of information words per frame is software programmable. Figure 7-1 shows a full frame format.

A full CART data frame is divided into seventeen equal time periods or time slots as shown in Figure 7-1. The first two time slots of the frame are for synchronization information and are identified as slots #F. The first "F" slot is designated as an idle word slot and the second "F" slot is designated as a sync word slot. The remaining fifteen slots that follow are for the information words, and are identified as IW slots #0 through #E or IW0 through IWE, respectively.

The idle word slot of the frame does not have a slot format but is composed of 24 idle bits which pull the CART OUT signal line low for one slot time when transmitted by the CART. The sync word format is the same as the IW format and always contains data ^0000.

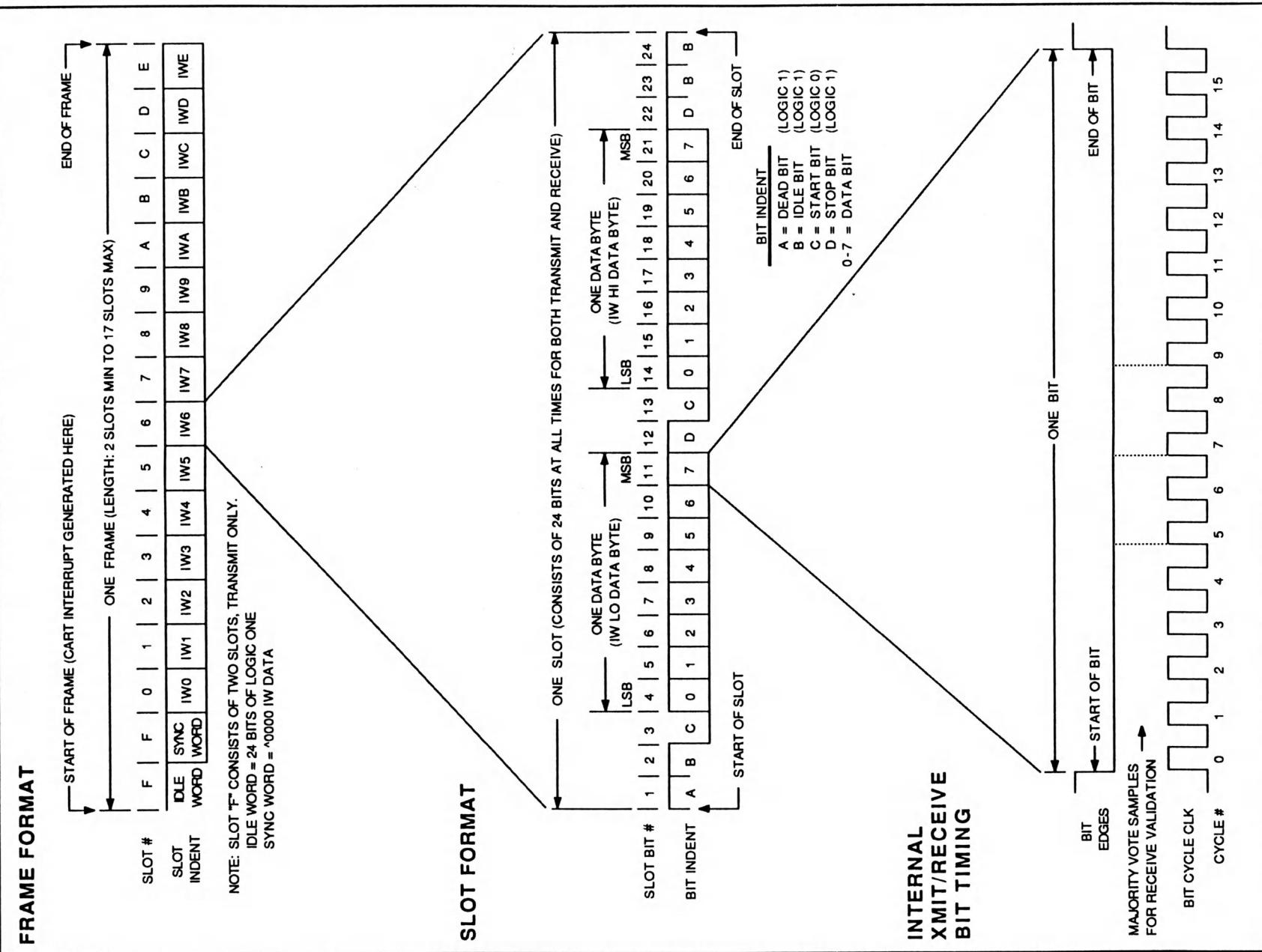
Each individual IW slot can be assigned as either a transmit slot for the serial transmission of data or a receive slot for the serial reception of data. The exact assignment (transmit or receive) of a slot is specified during the design stage of the system's data communication link. Assignment of IW slots #0 through #E is accomplished by software configuring a programmable transmit control register within the CART. The synchronization slots (slots #F) are transmit slots only.

The basic serial data format of any slot except for the idle word slot contains two standard UART type serial messages plus four additional bits. The standard UART serial message format being defined in sequence as one start bit, eight data bits, and at least one but no more than two stop bits. The four additional bits, two of which precede the UART formatted messages and two of which follow, are provided to: prevent contention between serial transmitters when one turns OFF and another turns ON, allow for signal propagation delays along the data communication lines, and allow for settling of the data communication lines following data transmission. All frame slots, including the idle word slot, are divided into 24 equal bit periods which are referred to as slot bits #1 through #24. Figure 7-1 also shows the format of a slot.

Slot bit #1 is a dead bit and slot bits #2, #23, and #24 are idle bits. These bits are all logic ones, however, they are designated differently to leave latitude in the protocol for future CART designs. During these bit times, the CART's serial data output signal line (CART OUT) is held low. The bits of the slot format shown in Figure 7-1 are inverted at the serial output of the CART.

Slot bits #3 through #12 and #13 through #23 comprise the user's serial data message format which is the same as two standard UART serial message formats. Slot bits #3 and #13 are start bits, slot bits #4 through #14 through #21 are for user data bytes, and slot bits #12 and #22 are stop bits. Slot bits #4 and #14 are the least significant bits of the user data bytes.

Each bit of a slot is subdivided into sixteen bit cycle clock periods for internal timing of the CART. The CART determines the logic level of a received bit by sampling the serial data input signal line (CART IN) three times near the middle of a bit time (during the 5th, 7th, and 9th bit cycle clock



periods), and the majority logic level (high or low) detected during these sample times (hereinafter referred to as a majority vote result) is assigned to that bit time. For example, if two or three logic ones are detected during the sampling times, the bit time is assigned a logic one. Conversely, if two or three logic zeros are detected during the sampling times, the bit time is assigned a logic zero. The sixteen bit cycle clock periods are designated  $\emptyset$  through 15. One slot bit time is equal to one baud rate period.

### 7.1.2 CART FUNCTIONAL OPERATION

Figure 7-2 shows a functional flowchart overview of the CART mode of operation. Prior to all CART operations, the CART circuits must be initialized by either a hardware or software initiated reset (see CART "Reset Logic", paragraph 7-1.3.13 in this chapter).

The serial I/O port automatically enters the CART mode following a hardware initiated reset, or enters the CART mode following a software initiated reset only if the UART/CART Mode Select bit (bit 3) is " $\emptyset$ " in the CART control register (CCR). Following a reset, CART operations become cyclic with the reception of data for time slots  $\emptyset$  through E and the transmission of the frame's synchronization information (i.e., the 24-bit idle word and the 24-bit sync word).

For normal CART operations, software must configure the port for the system's data communications environment and for the frame length. This normally occurs at the start of a frame during the transmission of the idle word. The CART notifies software when a frame starts by the output of an interrupt which will only occur if the Interrupt Enable bit (bit 4) is set in the CCR. Software normally sets this bit at the beginning of the system program following a CART reset.

Upon servicing the CART interrupt, software loads the frame length register (FLR), transmit control register (TCR), and CCR with appropriate control information for the frame and the data communication environment, and loads the appropriate information word registers (IWRs) with data for serial transmission. Software should first write the CCR with the appropriate control information to configure the port, and then write the remaining port registers in any sequence with data for serial transmission. Software can configure the CART for the frame and the data communication environment in considerably less time than it takes to transmit a single bit of the idle word.

At the beginning of each frame, the CART transmits the frame synchronization information via the CART OUT signal line. Thereafter, the CART resets the slot counter (SC) to  $\sim 00$  and processes the information word (IW) slots of the frame. The number of IW slots per frame is software programmable and can vary between a minimum of zero and a maximum of fifteen. The slots are designated IW $\emptyset$  thru IWE and directly relate to IW registers  $\emptyset$  through E and bits  $\emptyset$  through E in the TCR, the transmit verify error status register (TVESR), and the receive error status register (RESR), respectively.

The state of each bit in the TCR determines whether the relating IW frame slot is for the transmission or reception of user data. When a TCR bit is " $1$ ", a slot is a transmit slot and its data is serially transmitted on the CART OUT signal line (see CART Transmit Mode, paragraph 7-1.2.1). When the bit is " $\emptyset$ ", the slot is a receive slot and serially receives data from the CART IN signal line (see CART Receive Mode, paragraph 7-1.2.2).

Upon completion of either a transmit or receive operation, the SC is incremented by one at the end of the slot (after the last bit cycle clock period of the last bit in the slot). The contents of the SC is then compared to the number of user's slots per frame specified in the FLR. If the contents of the SC is less than that of the FLR, the SC points to the next bit in the TCR for processing of the next slot. When the contents of the SC and FLR are equal, it denotes the end of a frame.

## CART

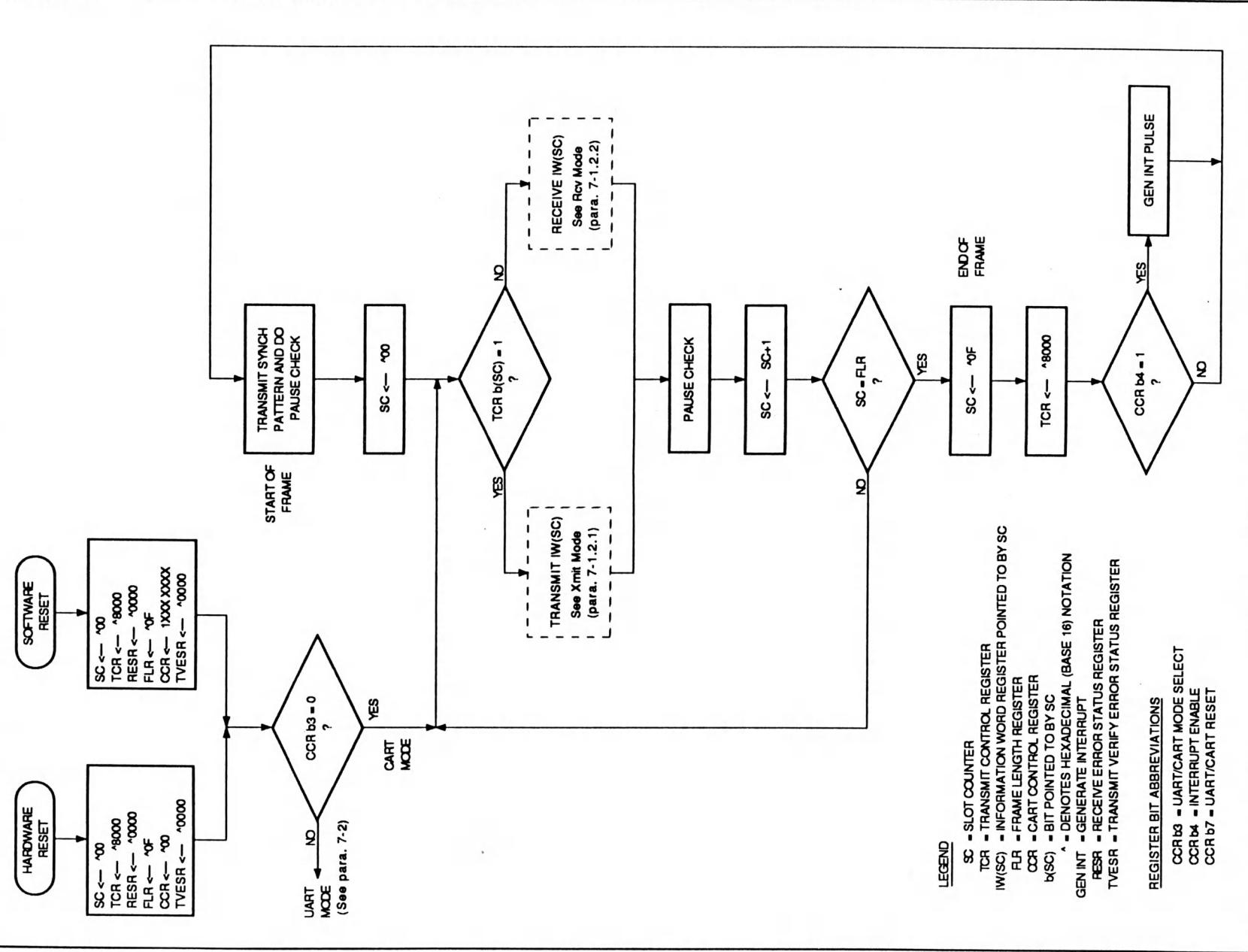


FIGURE 7-2. CART MODE FUNCTIONAL FLOWCHART - OVERVIEW

At the end of a frame, the SC is immediately loaded with ^0F and the TCR is reset to ^8000 to inhibit any further port transmissions until the port is reconfigured for the next frame. Also, it causes the port to output an INTERRUPT signal if CCR bit 4 is "1".

The state of Pause bit (bit 6) in the CCR is interrogated during the transmission of the sync pattern and after each information word slot. Depending upon when this bit is set determines port operations thereafter. See paragraph 7-1.4 for information on pause operations.

#### 7-1.2.1 CART TRANSMIT MODE

Figure 7-3 shows a functional flowchart of the CART transmit mode. The CART transmit mode is enabled when the bit pointed to by the slot counter (SC) is "1" in the TCR (see paragraph 7-1.2 for additional information).

When the port is set to the transmit mode, the serial transceiver immediately starts transmitting the dead bit of the serial message on the CART OUT signal line. In the second bit cycle clock period of the dead bit time, user data from the information word register (IWR) pointed to by the SC is transferred to the 21-bit serial transceiver buffer. At the end of the dead bit time, the transceiver then transmits the remaining bits (i.e., idle bits, start bits, user data bits, and stop bits) of the serial formatted message.

As each bit is transmitted, it is tested to verify its correct transmission over the data communication link. This is accomplished by the transceiver comparing the state of the bit prior to transmission to the majority vote result of the bit received on the CART IN signal line. If the bits do not match, the transceiver immediately sets the the IW Transmit Error bit (bit 4) in the CART status register (CSR) if the error occurred during an IW slot, or immediately sets the Sync Transmit Error bit (bit 3) in the CSR if the error occurred during the sync slot (see paragraph 7-1.2.3 for information on the updating of these status registers). A transmit verify is performed on all bits of a transmit slot except for the first bit (dead bit) and last bit (idle bit) of the slot.

There may be a short time delay between the transmission of the bit on the CART OUT signal line and the reception of the bit on the CART IN signal line due to signal propagation delays. This should not affect the data transmit verification process unless the propagation delay is greater than 0.45% of one baud rate period.

After all bits of a slot have been transmitted, the bit in the transmit verify error status register (TVESR) relating to the slot is updated with status by the transceiver four bit cycle clock periods before the SC is incremented by the CART control logic. If a transmit verify error was detected during the transmission of the slot, this bit is set; otherwise, it is cleared. Thereafter, the transmit mode ends and CART operations continue as described in the CART functional operation overview (paragraph 7-1.2).

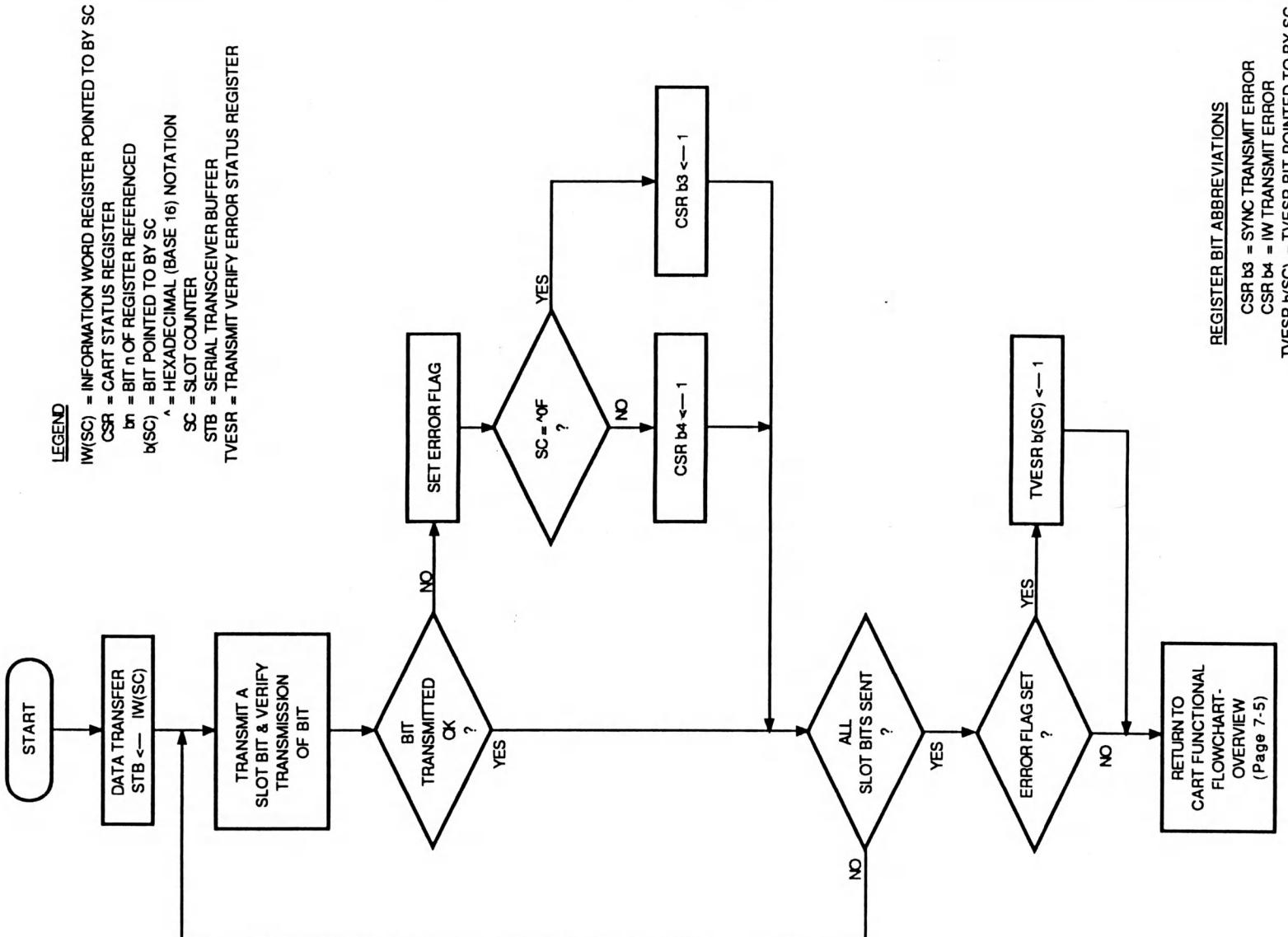


FIGURE 7-3. CART MODE TRANSMIT FLOWCHART



## CART

### 7.1.2.2 CART RECEIVE MODE

Figure 7-4 shows a functional flowchart of the CART receive mode. The CART receive mode is enabled when the bit pointed to by the slot counter (SC) is “0” in the TCR (see paragraph 7-1.2 for additional information).

At the beginning of the receive mode, the serial receiver resets an internal slot bit counter to zero and monitors the CART IN signal line for the start bit of a message. Depending upon the time the start bit was detected determines receiver operations thereafter. The receiver determines when the start bit occurred by the count (slot bit number) within the slot bit counter.

Ideally, the start bit should be detected any time during slot bit times 2, 3, 4, or 5 for proper data reception. If a start bit is detected during this time, the contents of the serial transceiver buffer (STB) is cleared to ^0000 and data reception follows. If a start bit is detected at any other time during a slot, the IW Receive Error bit (bit 5) in the CART status register (CSR) and the bit pointed to by the SC in the receive error status register (RESR) are set. Thereafter, the STB is cleared and data reception follows. If a start bit is not detected by the end of the slot, CSR bit 5 and the error bit in the RESR are set, and data ^FFFF is loaded into the STB. A slot in which no data is transmitted or received is referred to as an idle slot. See paragraph 7-1.2.3 for information on the updating of the status registers.

Whenever a start bit is detected, the serial transceiver determines the logic level of each following bit on the CART IN signal line by performing a majority vote. User data is received in the STB until the end of the slot, at which time data is transferred from the STB to the IW register pointed to by the SC. Following the transfer, the SC is incremented by one. If a receive error occurred during the slot time, data from the STB is transferred to the IW register right justified (i.e., upper bits of the IW data may be lost and filled with zeros). Thereafter, the receive mode ends and CART operations continue as described in the CART functional operation overview (paragraph 7-1.2).

## CART

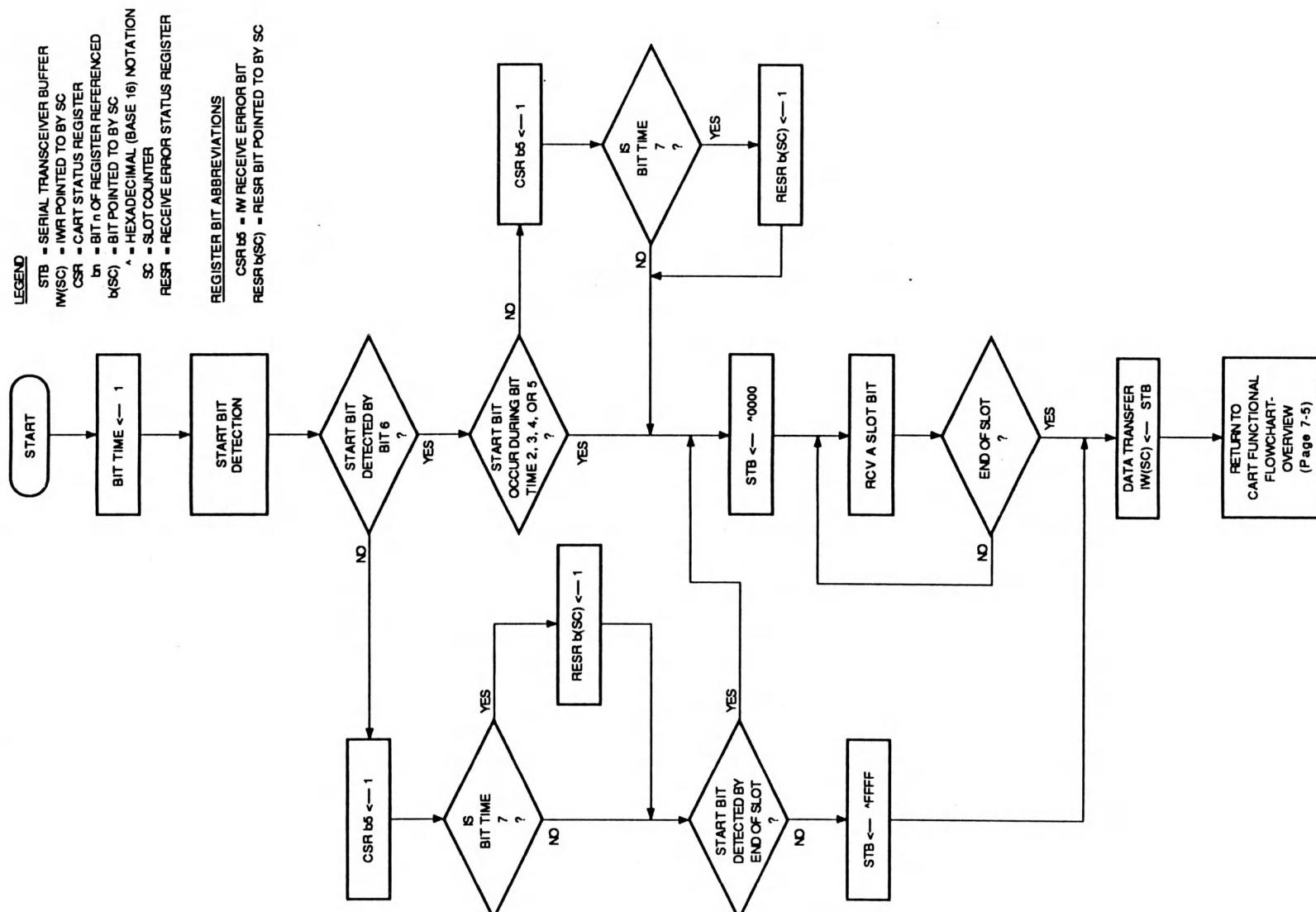


FIGURE 7-4. CART MODE RECEIVE FLOWCHART

## CART

### 7.1.2.3 CART STATUS REGISTERS UPDATE

Error status for a frame (i.e., sync and IW transmit verify errors, and IW receive errors) is constantly updated in the CART status register (CSR), the transmit verify error status register (TVESR), and the receive error status register (RESR) during the processing of the frame. Total status for a frame is available from these registers only upon completion of all frame activities. Total status for a frame remains valid in these registers until the end of slot "F" of the ensuing frame, at which time, the registers are cleared and updated with status of the ensuing frame. Reading status from these registers any time during the processing of a frame will not affect the status or the updating of the status in the registers. Figure 7-5 shows the update timing of the CART status registers for various error conditions.

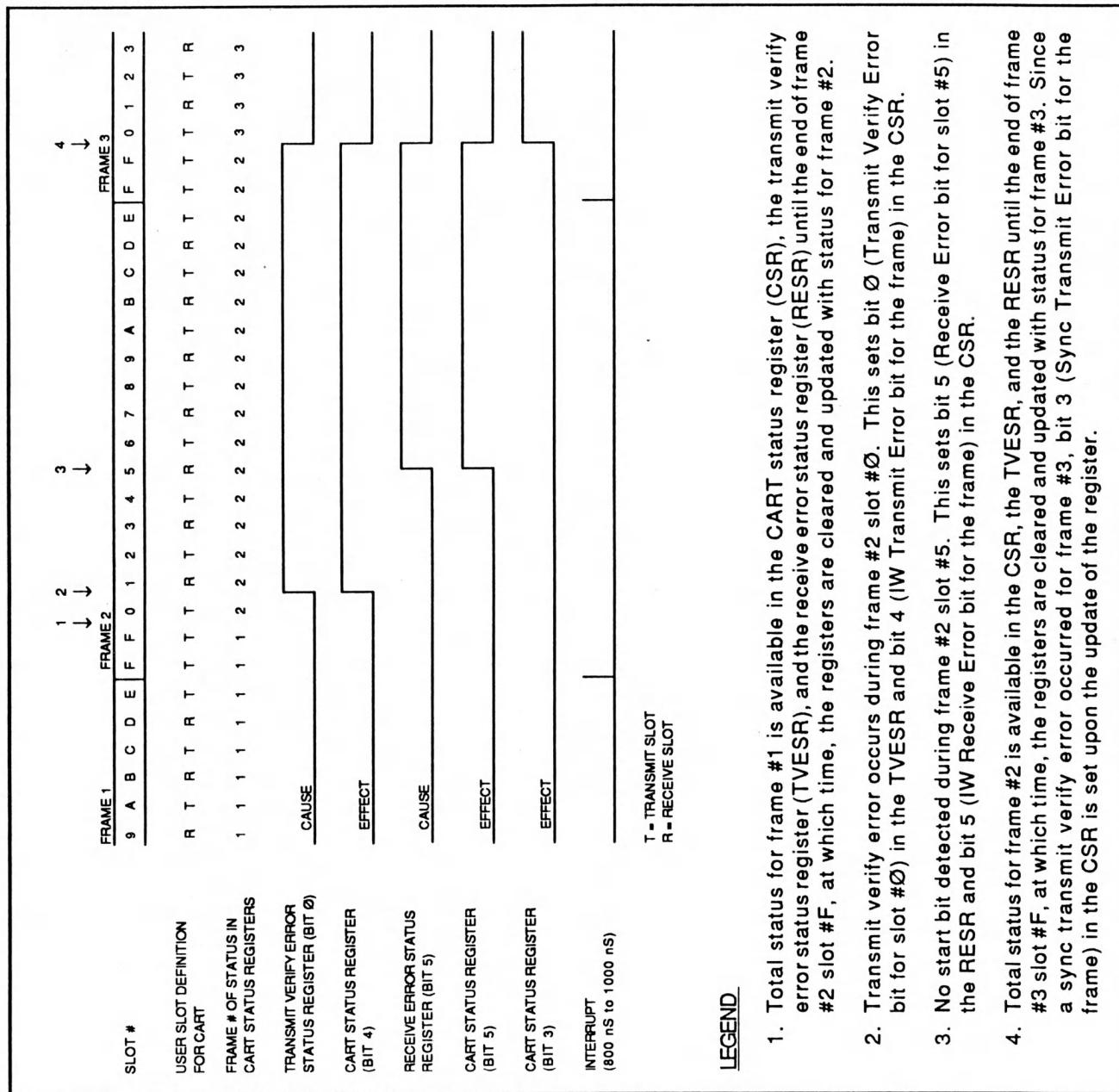


FIGURE 7-5. CART STATUS REGISTERS UPDATE TIMING EXAMPLE

### 7-1.3 CART ARCHITECTURE

Figure 7-6 shows how the CART internally interfaces to an EEC-IV device. Overall CART operation is controlled by the ENABLE (ENA) input signal to the device and by software. All CART circuits are addressed through the 16-bit data address register (DAR) on-board the device, and all data is transferred between an EEC-IV microprocessor and an addressed CART circuit via the device's MBus interface. Additional information on the CART and device interface is provided in the paragraphs that follow. Figure 7-7 (page 7-13) shows a simplified block diagram of the CART.

#### 7-1.3.1 CART REGISTER ADDRESS DECODER

The CART register address decoder is used to decode address bits A<sub>0</sub> through A<sub>7</sub> from the DAR to access any of the memory-mapped CART registers shown in Table 7-1 (page 7-12) when the address in the DAR is within the CART address range. The CART address ranges are  $\text{^nn}00\text{-}^{\text{nn}}1D$ ,  $\text{^nn}20\text{-}^{\text{nn}}2B$ , and  $\text{^nn}3A\text{-}^{\text{nn}}3D$  where nn is 09, 12, and 0F for EEC-IV device mask options "A", "C", and "D", respectively. The microprocessor has priority access to all IW registers and the slot count register.

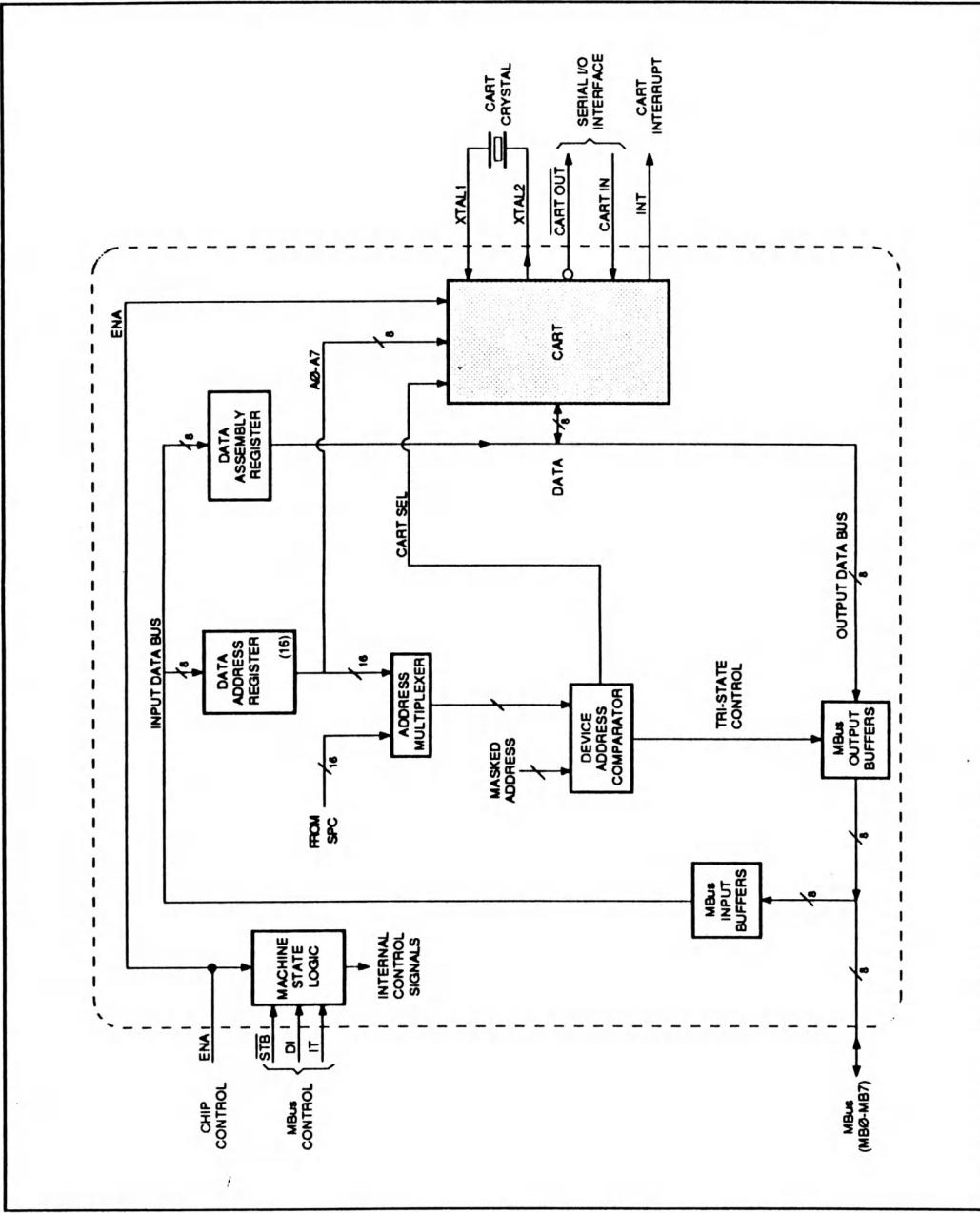


FIGURE 7-6. TYPICAL CART TO DEVICE INTERFACE

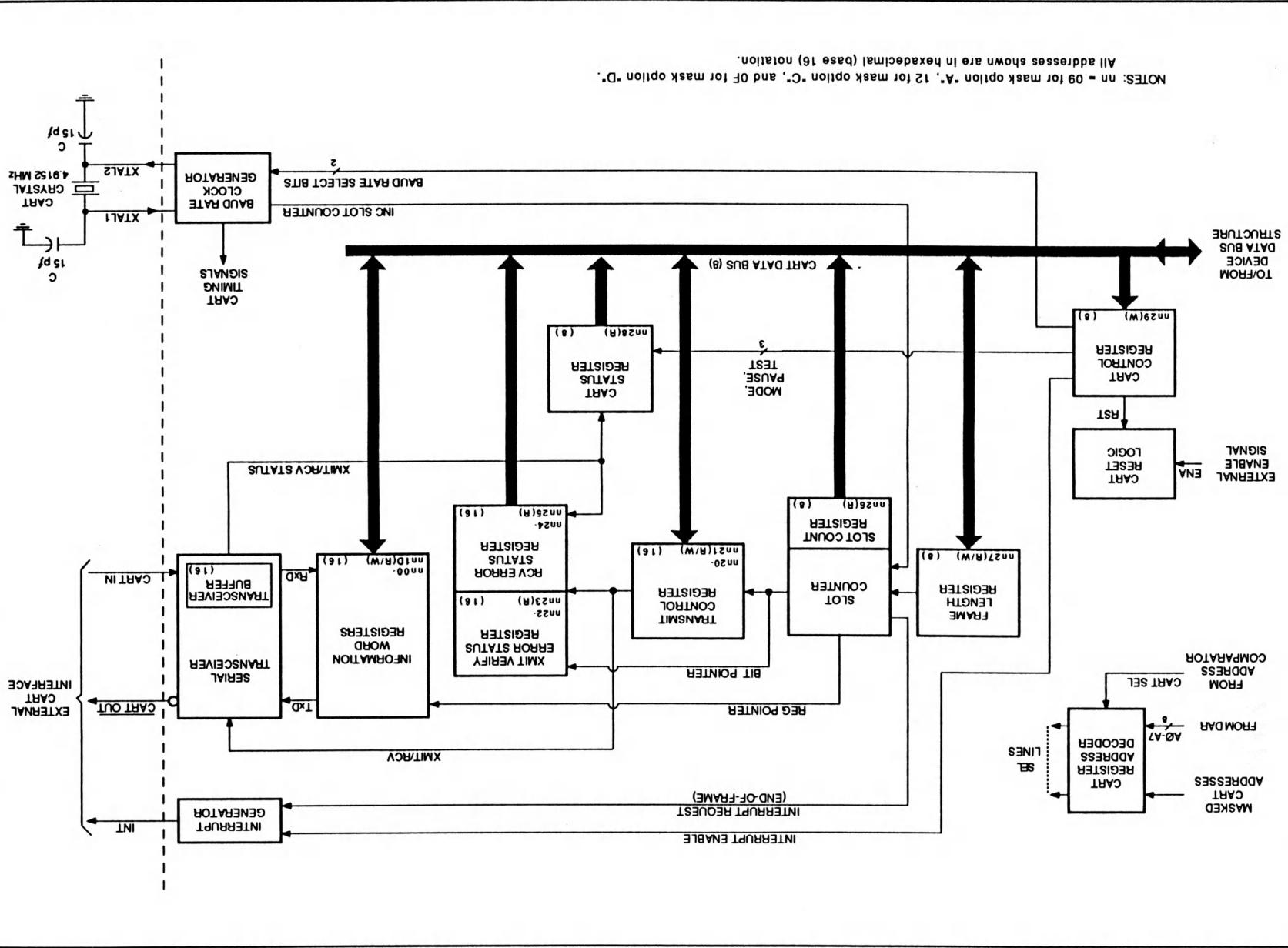
TABLE 7-1. CART MODE REGISTER ADDRESS MAP

ADDRESS <sup>③</sup>	READ			WRITE		
	- A -	- C -	- D -	-	-	-
0900 1200	0F00	Information Word Register #0 Low Byte		Information Word Register #0 Low Byte		
0901 1201	0F01			#0 High Byte		
0902 1202	0F02			#1 Low Byte		
0903 1203	0F03			#1 High Byte		
0904 1204	0F04			#2 Low Byte		
0905 1205	0F05			#2 High Byte		
0906 1206	0F06			#3 Low Byte		
0907 1207	0F07			#3 High Byte		
0908 1208	0F08			#4 Low Byte		
0909 1209	0F09			#4 High Byte		
090A 120A	0F0A			#5 Low Byte		
090B 120B	0F0B			#5 High Byte		
090C 120C	0F0C			#6 Low Byte		
090D 120D	0F0D			#6 High Byte		
090E 120E	0F0E			#7 Low Byte		
090F 120F	0F0F			#7 High Byte		
0910 1210	0F10			#8 Low Byte		
0911 1211	0F11			#8 High Byte		
0912 1212	0F12			#9 Low Byte		
0913 1213	0F13			#9 High Byte		
0914 1214	0F14			#A Low Byte		
0915 1215	0F15			#A High Byte		
0916 1216	0F16			#B Low Byte		
0917 1217	0F17			#B High Byte		
0918 1218	0F18			#C Low Byte		
0919 1219	0F19			#C High Byte		
091A 121A	0F1A			#D Low Byte		
091B 121B	0F1B			#D High Byte		
091C 121C	0F1C			#E Low Byte		
091D 121D	0F1D			#E High Byte		
0920 1220	0F20	Transmit Control Register Low Byte		Transmit Control Register Low Byte		
0921 1221	0F21	Transmit Control Register High Byte		Transmit Control Register High Byte		
0922 1222	0F22	Transmit Verify Error Status Register Low Byte		(2)		
0923 1223	0F23	Transmit Verify Error Status Register High Byte		(2)		
0924 1224	0F24	Receive Error Status Register Low Byte		(2)		
0925 1225	0F25	Receive Error Status Register High Byte		(2)		
0926 1226	0F26	Slot Count Register		(2)		
0927 1227	0F27	Frame Length Register		(2)		
0928 1228	0F28	CART Status Register		(2)		
0929 1229	0F29	(1)		(2)		
092A 122A	0F2A	(1)		(2)		
092B 122B	0F2B	(1)		(2)		
093A 123A	0F3A	Test Status Register #0 (4)		(2)		
093B 123B	0F3B	Test Status Register #1 (4)		(2)		
093C 123C	0F3C	Test Status Register #2 (4)		(2)		
093D 123D	0F3D	(1)		Test Node Register (4)		

## NOTES

1. Not used. An unpredictable value will be read.
2. Not used. Data written to this location is not stored.
3. Addresses in left column are for EEC-IV device mask option "A", middle column are for EEC-IV device mask option "C", and right column are for EEC-IV device mask option "D". All addresses shown are in hexadecimal notation.
4. Used for supplier part testing only. Do not read or write during normal CART operations.

FIGURE 7-7. CART MODE CIRCUITS SIMPLIFIED BLOCK DIAGRAM



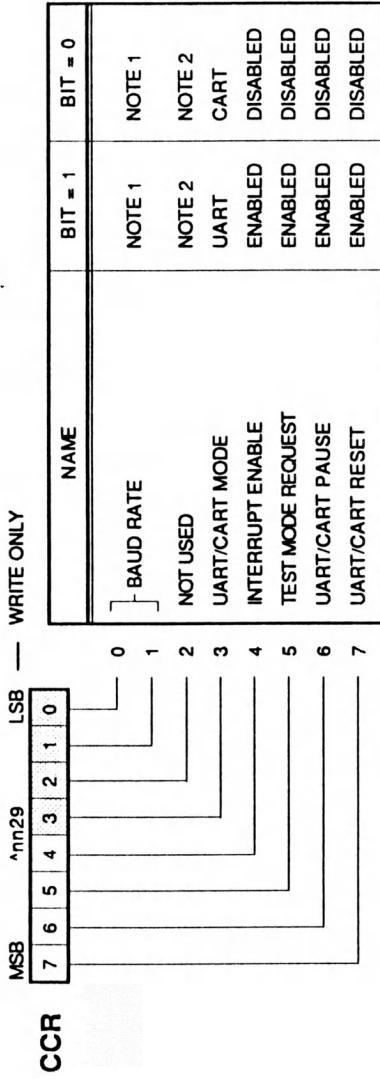
## CART

### 7-1.3.2 CART CONTROL REGISTER (CCR)

The 8-bit CCR is used for the following: to select the port operating mode (CART or UART); to select one-of-four different baud rates for serial I/O data communications; to enable and disable the output of the port's interrupt signal; to enable and disable the port's pause mode; to initiate a software reset for initializing all CART circuits except the CCR, and to enable and disable the CART/UART test mode and the writing of the test mode control register. Figure 7-8 shows the CCR bit format, and Table 7-2 defines each bit. On a hardware-initiated reset, the CCR is set to ^00, and on a software-initiated reset, it is set to 1XXX XXXX.

TABLE 7-2. CART CONTROL REGISTER BITS DESCRIPTION

BIT	NAME AND FUNCTION
0, 1	<b>BAUD RATE SELECT BITS:</b> These bits select the baud rate of the CART serial I/O data communications as shown in Table 7-3.
2	This bit is not used and has no affect on CART/UART operations.
3	<b>UART/CART MODE SELECT BIT:</b> This bit selects the port's operating mode. When set, it selects the UART mode; when cleared, it selects the CART mode. The UART mode can be selected only on a software reset. Any state change of this bit should be accompanied with a reset.
4	<b>INTERRUPT ENABLE BIT:</b> This bit, when set, enables the CART to output an active high INTERRUPT (INT) signal pulse at the beginning of each frame. When cleared, it inhibits the output of the interrupt signal by the CART.
5	<b>TEST MODE REQUEST BIT:</b> This bit is used for device manufacturer testing of the CART. Do not set this bit during normal device operation; otherwise, damage may result to the CART.
6	<b>UART/CART PAUSE BIT:</b> This bit, when set, pauses the operation of the CART upon completion of the current transmit or receive transaction. When this bit is cleared, normal CART operations resume. See paragraphs 7-1.4 and 7-2.4.
7	<b>UART/CART RESET BIT:</b> This bit, when set, initiates a software reset of the CART. This is a self-clearing bit which does not have to be cleared prior to a set to initiate a reset.



- NOTES: 1. See Tables 7-2 and 7-3 for bit definition.  
2. This bit is not used and has no effect on CART operations if set or cleared.  
3. nn = 09 for mask option "A", 12 for mask option "C", and 0F for mask option "D".

FIGURE 7-8. CART CONTROL REGISTER DATA FORMAT

### 7.1.3.3 BAUD RATE CLOCK GENERATOR

The baud rate clock generator is used to generate all internal CART timing signals as well as one-of-four program-selectable baud rates for serial I/O data communications. The baud rate clock generator consists of a crystal oscillator and a variable frequency-divider circuit. The baud rate clock generator is designed to operate using an external 4.91520 MHz  $\pm 200$  Hz crystal.

The variable frequency-divider circuit is controlled by the BAUD RATE SELECT bits (bits 0 and 1) of the CART control register. The logic state of these bits select the baud rate of the port as shown in Table 7-3. The table also shows the time periods produced by the baud rates for the CART serial data format.

Stabilization of the crystal oscillator at the proper operating frequency requires approximately 100 milliseconds after the ENABLE (ENA) signal is pulled high following a device power-up. When the ENA signal is pulled low, the oscillator is disabled, halting all CART operations.

TABLE 7-3. CART MODE SERIAL DATA FORMAT TIMING PERIODS VS BAUD RATE

CCR BITS		BAUD RATE	TIME PERIODS		
b1	b0		ONE BIT	ONE SLOT	ONE FRAME*
0	0	2,400	416.7 $\mu$ S	10.00 mS	170.00 mS
0	1	4,800	208.3 $\mu$ S	5.00 mS	85.00 mS
1	0	9,600	104.2 $\mu$ S	2.50 mS	42.50 mS
1	1	19,200	52.1 $\mu$ S	1.25 mS	21.25 mS

\* One frame time period is based upon 17 slots per frame, and that no interruptions occurred during the processing of the frame.

$\mu$ S = microseconds; mS = milliseconds

## CART

### 7.1.3.4 FRAME LENGTH REGISTER (FLR)

The 8-bit FLR is used to specify the number of user slots (0 to 15) per frame. The maximum number of user slots per frame is limited by the number of information word registers available in the CART, which is fifteen. The minimum number of user slots that can be specified for a frame is zero. The number of user slots per frame is contained in bits 0 through 3 of the register. Bits 4 through 7 of the register are not used and, when read, are read as "0's". Upon a CART reset, the FLR is set to  $\text{^OF}$ . Figure 7-9 shows the data format of the FLR.

### 7.1.3.5 TRANSMIT CONTROL REGISTER (TCR)

The programmable 16-bit TCR is used to specify which slots in a frame are for the transmission of user data and which slots are for the reception of user data. TCR bits 0 through 14 directly relate to frame slots 0 through E, respectively. When a TCR bit is set to "1", it enables the transmitter for the duration of the related slot time; when it is set to "0", it enables the receiver for the duration of the related slot time. TCR bit 15 is not used and is permanently fixed at "1". At the end of a frame or upon a CART reset, the TCR is reset to  $\text{^8000}$ . Figure 7-10 shows the data format of the register.

FLR	b7	$\text{^nn27}$	b0	- READ/WRITE
	0	0	0	D D D D
DDDD	= SLOTS/FRAME			
	= $\text{^0}$ TO $\text{^F}$			
VALUE WRITTEN TO FLR	IWs PER FRAME	DATA TRANSMITTED / RECEIVED		
$\text{^00}$	0	IDLE & SYNC WORDS ONLY		
$\text{^01}$	1	IDLE & SYNC WORDS, & IWD		
:	:	:		
$\text{^0E}$	14	IDLE & SYNC WORDS, & IWD - IWE		
$\text{^0F}$	15	IDLE & SYNC WORDS, & IWD - IWE		

#### NOTES

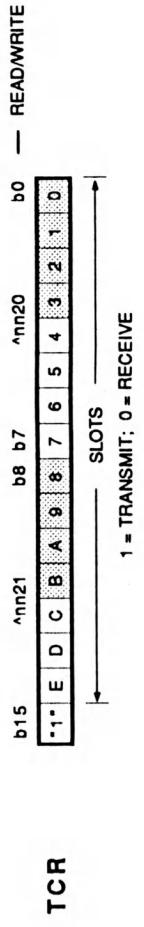
1. nn = 09 for mask option "A", 12 for mask option "C", and 0F for mask option "D".
2. The actual number of IWs transmitted and/or received within a frame is equal to the decimal value written to the FLR.
3. For 81C62 RAM/CART devices with Ford part number N7500020FSC111 (designated for the '88 model year), bit 3 in the register is permanently hardware fixed at '1' which sets a minimum of eight user slots per frame.

FIGURE 7-9. CART MODE FRAME LENGTH REGISTER DATA FORMAT

### 7-1.3.6 INFORMATION WORD REGISTERS (IWRs)

The 15x16-bit IWRs are used as transmit and receive registers for user data. These registers are made from standard RAM cells that are configured to perform as a time sliced direct memory access (DMA) dual ported RAM accessible by both the microprocessor and the CART circuits. The microprocessor has priority access over these registers. The IWRs are numbered from 0 through E and directly relate to frame slot numbers 0 through E, respectively. The IWRs are in an indefinite state following a CART reset. Figure 7-10 shows the data format of the IWRs.

#### TRANSMIT CONTROL REGISTER DATA FORMAT



#### INFORMATION WORD REGISTERS DATA FORMAT

WORD ADDR	IWR#	b15	b8 b7	b0 — READ/WRITE
^nn00	0	HIBYTE	*T LO BYTE	
^nn02	1	*	*R	
^nn04	2	*	*	
^nn06	3	*	*	
^nn08	4	*	*	
^nn0A	5	*	*	
^nn0C	6	*	*	
IWRs	7	*	*	
^nn0E	8	*	*	
^nn10	9	*	*	
^nn12	10	*	*	
^nn14	A	*	*	
^nn16	B	*	*	
^nn18	C	*	*	
^nn1A	D	*	*	
^nn1C	E	*	*	

\* T = UART Transmit Data Buffer and R = UART Receive Data Buffer (applicable to UART mode only).

#### NOTES

1. nn = 09 for mask option "A", 12 for mask option "C", and 0F for mask option "D".
2. For even addresses (A0 = 0), read/write b0 through b7; for odd addresses (A0 = 1), read/write b8 through b15.

FIGURE 7-10. CART MODE TCR AND IWRs DATA FORMATS

## CART

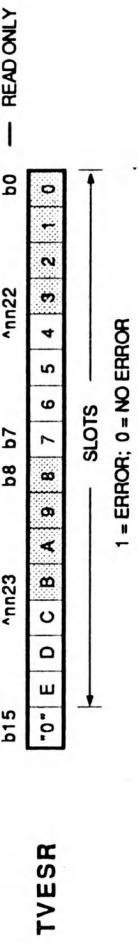
### 7.1.3.7 TRANSMIT VERIFY ERROR STATUS REGISTER (TVESR)

The 16-bit TVESR indicates which transmit slots of a frame had errors. The CART transceiver monitors the state of each bit as it is being transmitted on the CART OUT signal line by receiving the bit on the CART IN signal line. An error occurs when the state of a transmit bit does not match the majority vote result of the received bit. Each bit except the first and last bits of all transmit slots except the idle word of slot "F" are tested in a frame. If any bit does not compare, the TVESR bit relating to the slot is set during the last bit time of the slot. Bits  $\emptyset$  through 14 in the TVESR directly relate to frame slots  $\emptyset$  through E, respectively. Bit 15 of the TVESR is hardware fixed at " $\emptyset$ ". The transmit verify error status of the sync word of slot "F" is contained in bit 3 of the CART status register. Status in the TVESR remains valid for a frame until the end of slot "F" of the next frame, at which time, the register is cleared and then updated with status of the next frame. Following a reset, the TVESR is cleared. Figure 7-11 shows the data format of the register.

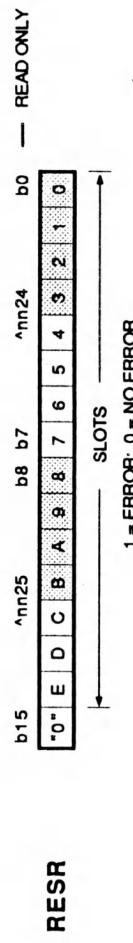
### 7.1.3.8 RECEIVE ERROR STATUS REGISTER (RESR)

The 16-bit RESR indicates which receive slots in a frame had errors. An error occurs if a start bit is not detected during a receive slot time, or if a valid start bit is not detected during slot bit times 2, 3, 4, or 5. When a receive error occurs, the receive error status bit relating to the slot is set in the RESR at the end of slot bit time 6. Bits  $\emptyset$  through 14 in the RESR directly relate to frame slots  $\emptyset$  through E, respectively. Bit 15 in the RESR is hardware fixed at " $\emptyset$ ". Status in the RESR remains valid for a frame until the end of slot "F" of the next frame, at which time, the register is cleared and then updated with status of the next frame. Following a reset, the RESR is cleared. Figure 7-11 shows the data format of the register.

#### TRANSMIT VERIFY ERROR STATUS REGISTER DATA FORMAT



#### RECEIVE ERROR STATUS REGISTER DATA FORMAT



NOTE: nn = 09 for mask option "A", 12 for mask option "C", and 0F for mask option "D".

FIGURE 7-11. CART MODE TVESR AND RESR DATA FORMATS

### 7-1-3.9 CART STATUS REGISTER (CSR)

The 8-bit CSR is used to accumulate and store the overall status of all CART operations. Figure 7-12 shows the CSR bit format, and Table 7-4 defines each status bit. The CSR is cleared following a CART reset.

TABLE 7-4. CART STATUS REGISTER BITS DESCRIPTION - CART MODE

BIT	NAME AND FUNCTION
0, 1	These bits are not used and are always read as "0's" in the CART mode. See Table 7-7.
2	<b>UART/CART MODE STATUS BIT:</b> This bit echoes the state of the UART/CART Mode Select bit (bit 3) in the CART control register. This bit is set when the port is in the UART mode, and it is cleared when the port is in the CART mode.
*3	<b>SYNC TRANSMIT ERROR BIT:</b> This bit is set when a transmit verify error occurs during the serial transmission of the sync word (slot #F). A transmit verify is performed on the sync word in the same manner as for an information word (see paragraph on transmit verify error status register for further information). The sync transmit error bit is set during the last bit time of the sync word slot if an error occurs.
*4	<b>IW TRANSMIT ERROR BIT:</b> This bit is the logical-OR of all bits in the transmit verify error status register. It is set whenever a transmit verify error occurs during the serial transmission of any information word (IW) in a frame.
*5	<b>IW RECEIVE ERROR BIT:</b> This bit is the logical-OR of all bits in the receive error status register. It is set whenever a receive error occurs during the serial reception of any information word (IW) in a frame.
6	<b>UART/CART PAUSE STATUS BIT:</b> This bit echoes the state of the UART/CART PAUSE bit (bit 6) in the CART control register. It is set when bit 6 is set in the CART control register even though the CART may not be in the pause mode. It is cleared when bit 6 is cleared in the CART control register.
7	<b>TEST MODE STATUS BIT:</b> This bit indicates when the CART is in the test mode. It is set when the test mode entry code is written into the test mode control register after the Test Mode Request bit (bit 5) is set in the CART control register. It is cleared when either bit 5 is cleared in the CART control register or any code other than the test mode entry code is written into the test mode control register.

- \* This bit retains status for a frame until the end of slot F of the ensuing frame, at which time, the bit is cleared and then updated with status of the ensuing frame.

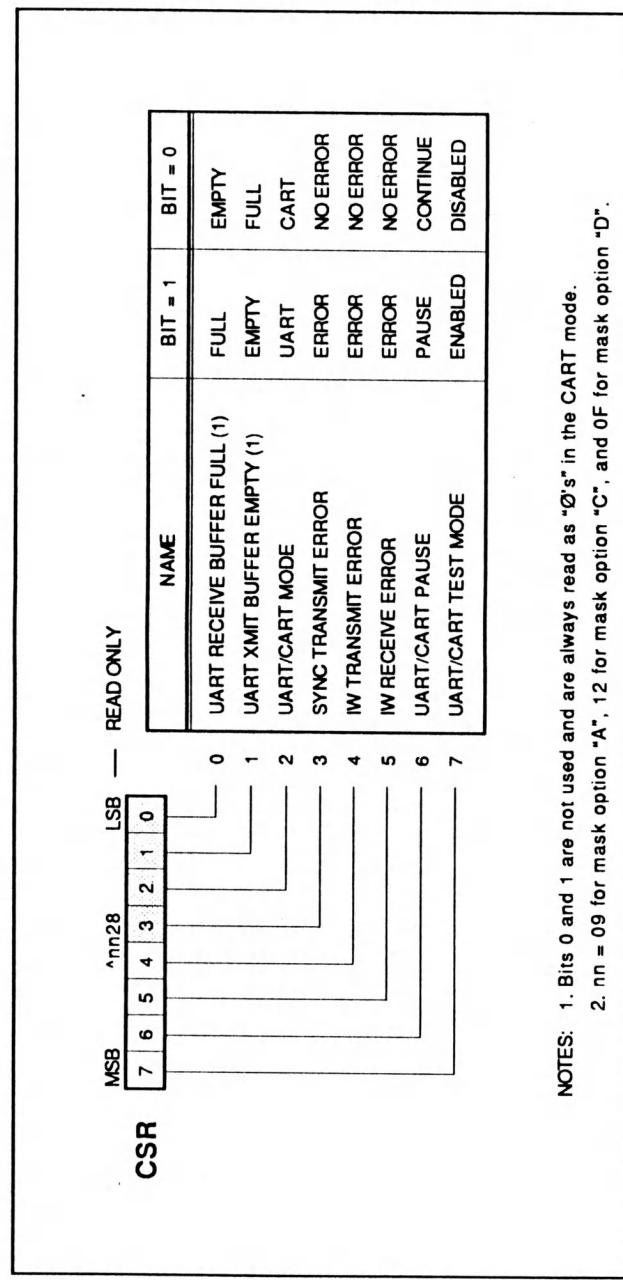


FIGURE 7-12. CART STATUS REGISTER DATA FORMAT

## CART

### 7-1.3.10 SLOT COUNTER (SC) AND SLOT COUNT REGISTER (SCR)

The SC is a 4-bit up-counter used as an address pointer to access the information word registers, and as a bit pointer to access the bits in the transmit control register (TCR), the transmit verify error status register (TVESR), and the receive error status register (RESR) during the processing of a frame. Also, the SC initiates an interrupt request at the start of a frame and resets the TCR at the end of a frame.

During the processing of a frame, the SC is incremented by one at the end of a slot by the baud rate clock generator. The value in the SC is then compared with the value in the frame length register (FLR). When a match occurs between these values denoting the end of a frame, the SC defaults to value  $\text{^OF}$ . This resets the TCR and enables the SC to initiate an interrupt request at the beginning of the next frame via the CART interrupt generator. When the values do not match, the next slot in the frame is processed.

The SC can be read via the SCR to determine which slot is being processed in a frame. When read, bits 0 through 3 in the SCR denote the slot number in-progress while bits 4 through 7 are read as "0's". Upon a CART reset, the SC and SCR are set to  $\text{^O0}$ . Figure 7-13 shows the data format of the SCR.

### 7-1.3.11 INTERRUPT GENERATOR

The interrupt generator is used to output a high INTERRUPT (INT) signal at the beginning of a CART frame during the processing of slot "F" if the Interrupt Enable bit (bit 4) in the CART control register is "1". The INT signal is output high for approximately 4 to 5 CART crystal cycles or approximately 800 to 1000 nanoseconds with a CART crystal frequency of 4.91520 MHz. Following a CART reset, the INT signal is set low.

### 7-1.3.12 SERIAL TRANSCEIVER

The serial transceiver is used to serially transmit data on the CART OUT signal line and serially receive data on the CART IN signal line. The transceiver operates in a half-duplex mode of operation only. Following is a summary of transceiver functions.

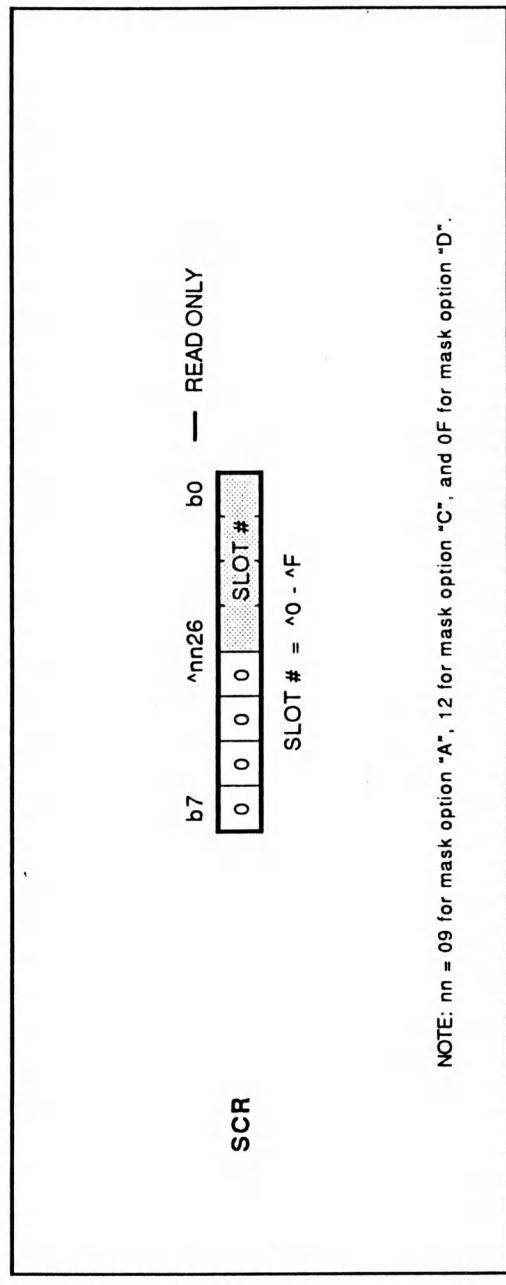


FIGURE 7-13. CART MODE SLOT COUNT REGISTER DATA FORMAT

**TRANSMITTER FUNCTIONS**

- holds the CART OUT signal line low for the duration of the idle word slot time (24 bits long),
- generates and transmits the sync pattern at the beginning of a frame,
- automatically transfers user data from the IW registers to the serial transceiver buffer for serial transmission,
- automatically serially formats user data with the proper idle bits, start bits, and stop bits,
- serially transmits the formatted data on the CART OUT signal line at the proper baud rate, and
- detects transmit verify errors during transmission of the data.

**RECEIVER FUNCTIONS**

- continuously monitors the CART IN signal line for the start bit of a received serial formatted message when the CART is not transmitting or receiving a message,
- detects slot bit timing errors during the reception of the start bit,
- automatically synchronizes the receiver circuits on the leading edge of a start bit to enable the reception of a message,
- determines the logic state of each received bit and removes user data from the serially received formatted message, and
- automatically transfers the user data from the serial transceiver to the IW registers.

**7-1.3.13 RESET LOGIC**

The reset logic is used to initialize the CART. Either hardware or software can initiate a reset. Hardware initiates a CART reset by momentarily pulsing the ENABLE (ENA) input signal line low to the device. Software initiates a CART reset by setting bit 7 (Reset bit) in the CART control register. When a reset is initiated, it triggers a one-shot in the reset logic which then initializes the port. A CART reset requires four CART crystal cycles to complete.

Table 7-5 shows the contents and/or conditions of the CART following a reset. It is important to note that some CART registers are not initialized and are in an indeterminate state following a reset. The information word registers (IWRs) are in an indeterminate state after a reset but can be cleared by software writing  $\text{^0000}$  to these registers. For a software reset, the value written into the CART control register to initiate the reset is unaffected by the reset.

TABLE 7-5. CART MODE RESET VALUES

CIRCUIT	RESET VALUES		COMMENTS
	HARDWARE	SOFTWARE	
CART Control Register	$\text{^00}$	$1\text{XXX XXXX}$	
Frame Length Register	$\text{^0F}$	$\text{^0F}$	$\text{"X" as embedded in software write cmd.}$
Slot Counter	$\text{^00}$	$\text{^00}$	
Slot Count Register	$\text{^00}$	$\text{^00}$	
Transmit Control Register	$\text{^8000}$	$\text{^8000}$	
Information Word Registers $\text{^0} \wedge \text{E}$	Indeterminate	Indeterminate	
Transmit Verify Error Status Register	$\text{^0000}$	$\text{^0000}$	
Receive Error Status Register	$\text{^0000}$	$\text{^0000}$	
CART Status Register	$\text{^00}$	Indeterminate	

#### 7-1.4 CART PAUSE MODE

The CART pause mode is used to halt all serial I/O port operations. In this mode, software may perform any of the following:

- read and/or write any or all information word registers (IWRs),
- read any port status register (i.e. CSR, TVESR, RESR),
- write any port control register (i.e. CCR, TCR, FLR),
- read the slot counter (SC), and/or
- initiate a software reset of the port via CCR Reset bit 7.

Software initiates the pause mode by setting the Pause bit (bit 6) in the CCR. If the Pause bit is set any time after the first half of the dead bit but before the end of a slot, the pause mode is not initiated until the following have occurred:

- all serial data transactions of the slot have been completed,
- all status flags pertaining to the current serial data transaction (receive or transmit) have been updated in the appropriate status registers,
- after the SC has been incremented to point to the next slot except when the Pause bit is set during the transmission of the 24-bit idle word, in which case, the SC retains the value ^0F.
- after an end-of-frame interrupt has been generated if the SC increments to ^0F at the end of the slot, and
- after the transmission of the 24-bit idle word but before the transmission of the sync word if the Pause bit was set before the end of the idle word slot.

If the Pause bit is set in the CCR during the first half of the dead bit for any slot and remains set thereafter, the port will pause at the end of the dead bit. When this occurs, the SC remains unchanged and all further port operations are inhibited for the slot.

Once in the pause mode, all port operations are inhibited until the Pause bit is cleared in the CCR. When software clears this bit, the port resumes operation based upon the time at which it paused, as follows:

- If the port paused at the end of the dead bit for an information word slot (i.e., slots ^0-^E), the port resumes normal operation with the dead bit of the same slot.
- If the port paused at the end of an information word slot, the port resumes normal operation with the dead bit of the next slot.
- If the port paused at the end of the dead bit for the idle word slot, the port resumes normal operation with the dead bit of the sync word slot.

## CART

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- If the port paused at the end of the dead bit for the sync word slot, the port resumes normal operation with the dead bit of the idle word slot.
- If the port paused at the end of the sync word slot, the port resumes normal operation with the dead bit of information word slot #0.
- If the port paused at the end of the idle word slot, the port resumes normal operation with the dead bit of the same slot.

If software initiates a port reset during the pause mode (i.e., software sets CCR Reset bit 7 to "1"), all port circuits are set to the conditions specified in Table 7-5 for a CART software reset. The port will be in the pause mode following a software-initiated reset only if the Pause bit was set in the software reset command.

If hardware initiates a CART reset during the pause mode, the Pause bit is cleared in the CCR and all port circuits are operational and set to the conditions specified in Table 7-5 for a hardware reset.

The CART pause mode is not initiated when the Pause bit is set and cleared after the first half of the dead bit but before the end of a slot, or when the Pause bit is set and cleared after the start but before the halfway point of the dead bit for a slot.

## 7-2 UART MODE

The following paragraphs describe the Universal Asynchronous Receiver/Transmitter (UART) mode of operation.

### 7-2.1 UART SERIAL DATA COMMUNICATIONS PROTOCOL

The UART uses an 11-bit serial data format for the transmission and reception of user data as shown in Figure 7-14. The format consists of one start bit, eight user data bits, and two stop bits which are transmitted and received by the UART in that order. The LSB of user data follows the start bit. When no transmitter is transmitting on the UART link, the data communication lines are considered idle. This idle time is referred to as dead bit time or dead bits.

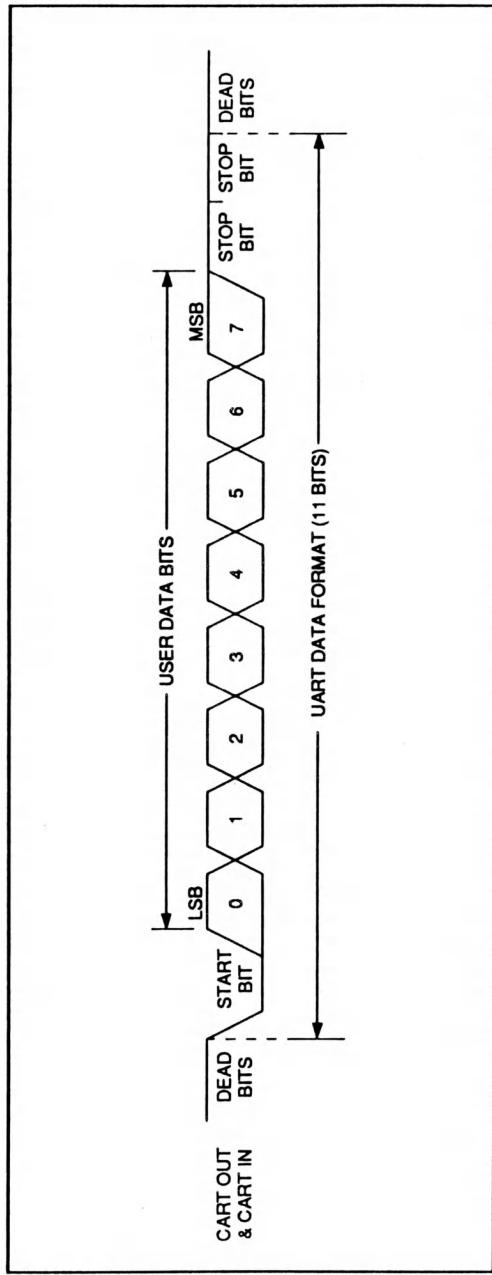


FIGURE 7-14. UART MODE SERIAL DATA FORMAT

### 7-2.2 UART FUNCTIONAL OPERATION

Figure 7-15 shows a functional flowchart of the UART mode of operation. The UART mode is selected when the UART/CART Mode Select bit (bit 3) and the Reset bit (bit 7) are simultaneously set to "1" along with all other control bits set for UART operations in the CART control register (CCR). Upon enabling the mode, the port (1) is configured as a double-buffered UART, (2) is reset, and (3) defaults to the UART receive mode. The port performs as a UART until the occurrence of either a hardware reset or a state change of the CCR bit 3.

In the receive mode, the port continuously monitors the CART IN signal line for a start bit until a start bit is detected or software loads a data byte into the UART transmit buffer (UTB). Upon detection of a start bit, the port serially receives the data message that is appended to the start bit (see UART Receive Mode, paragraph 7-2.2 for further information.). When the UTB is loaded with data, the port monitors the CART IN signal line for two more bit times following the load, and if a start bit is not detected during this time, the port serially transmits the data on the CART OUT signal line (See UART Transmit Mode, paragraph 7-2.2.1 for further information.).

At the end of serial data reception or transmission, the port performs a pause check by interrogating the PAUSE bit (bit 6) in the CCR. If this bit is "1", the pause mode is enabled (see paragraph 7-2.4). If it is "0", the port continues with the monitoring of the CART IN signal line for a start bit. The following paragraphs further describe the UART transmit and receive modes.

## CART

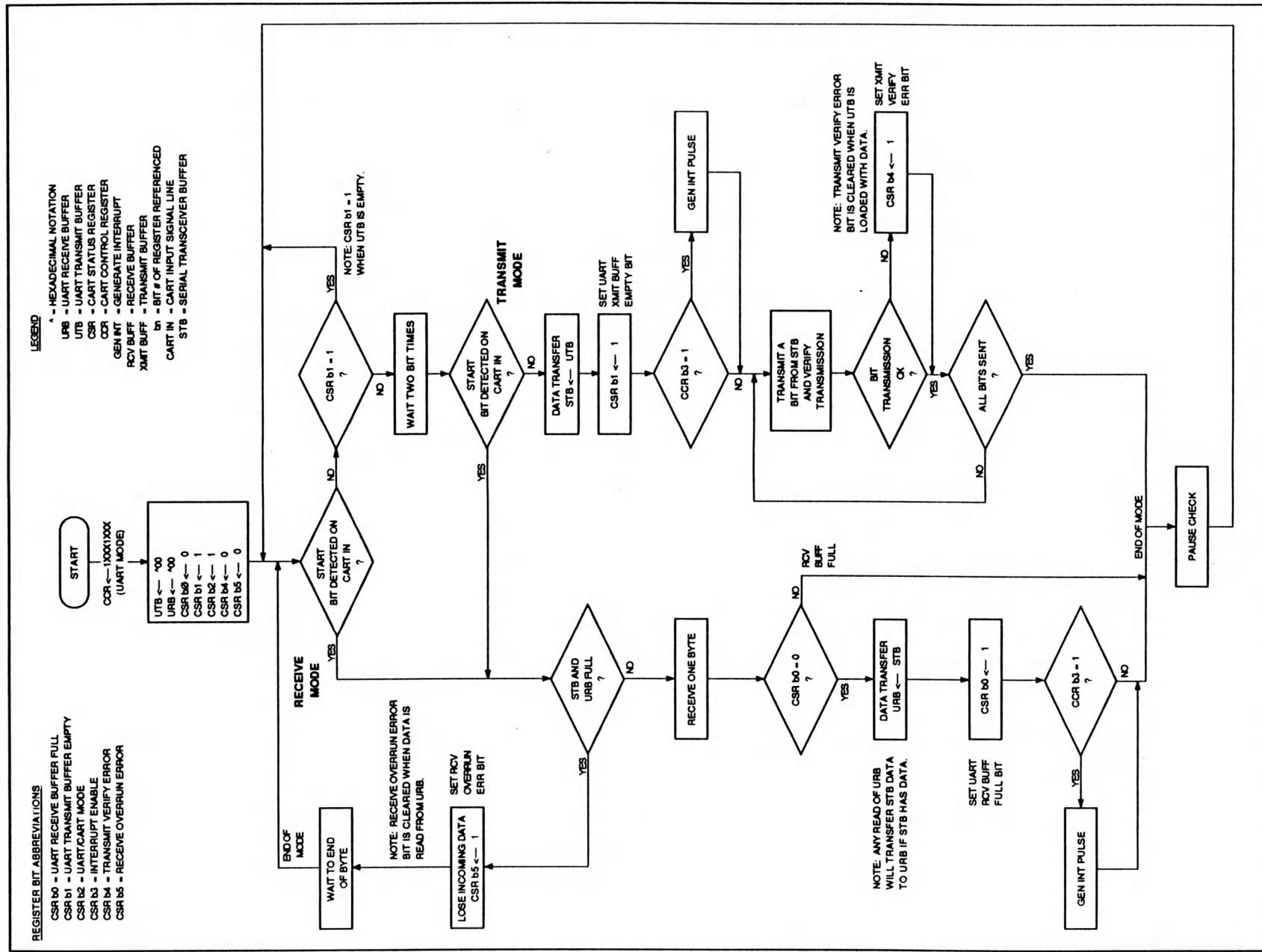


FIGURE 7-15. UART MODE FUNCTIONAL FLOWCHART

### 7-2.2.1 UART TRANSMIT MODE

UART transmit mode operations begin with a data transfer from the UTB to the serial transceiver buffer during the transmission of the start bit on the CART OUT signal line. The transceiver outputs the start bit by holding the CART OUT signal line high for one bit time. Thereafter, the transceiver outputs the eight user data bits in succession starting with the least significant bit. Immediately following the last user data bit (MSB), the transmitter outputs two stop bits by holding the CART OUT signal line low for two bit times.

During the serial transmission of the data, the serial transceiver verifies the correct transmission of each bit. Verification is accomplished by comparing the logic state of each transmitted bit with the majority vote result of the same bit received on the CART IN signal line. If any bit does not match, the transceiver sets the Transmit Verify Error status bit (bit 4) in the CART status register (CSR). If all bits match, the error bit is not set. The Transmit Verify Error bit is cleared on every load of the UTB.

Whenever data transfers from the UTB to the transceiver buffer, the UART Transmit Buffer Empty bit (bit 1) is set to "1" in the CSR to indicate an empty UTB. When software re-loads the UTB, CSR bit 1 is cleared to indicate a full buffer. Software can continuously send data via the data communication link by re-loading the UTB whenever the UTB is empty which can be determined through the interrogation of CSR bit 1 upon the servicing of a port interrupt. The port outputs an interrupt when the Interrupt Enable bit (bit 4) is "1" in the CCR and bit 1 is set in the CSR.

Between the transmission of consecutive UART messages, transmit operations are temporarily suspended for two bit times. During this time, the transceiver allows for the detection of a start bit on the data communication link. If a start bit is not detected within this time, transmit operations begin for the next data message. If a start bit is detected during this time, transmit operations remain suspended until the incoming message is received, at which time the transceiver again monitors the CART IN signal line for a start bit.

### 7-2.2.2 UART RECEIVE MODE

UART receive mode operations begin with the detection of a valid start bit on the CART IN signal line. Start bit detection for the UART mode is the same as for the CART mode. Upon detection of a valid start bit, the transceiver buffer serially receives the incoming data message. Upon reception of the last stop bit of the message, data in the transceiver buffer is transferred to the URB.

When data transfers into the URB, it sets the UART Receive Buffer Full bit (bit 0) in the CSR to indicate the buffer is full. If the URB is full of data when data is serially received in the transceiver buffer, data remains in the latter buffer until the URB is empty. When this occurs, further data reception is inhibited. If the URB and transceiver buffer are full of data upon detection of a valid start bit, incoming data on the CART IN signal line is not received and the UART sets an Overrun Error bit (bit 5) in the CSR to "1". The Overrun Error bit is cleared in the CSR upon a read of the URB.

Software can continuously receive data messages via the data communication link by reading the URB whenever it becomes full of data. Software can determine if the URB is full by interrogating the UART Receive Buffer Full bit in the CSR upon the servicing of the port interrupt. When the URB is full, this bit is "1". This bit is automatically cleared upon a read of the URB. When this bit is cleared, any data in the transceiver buffer is then transferred into the URB which re-sets the bit to "1". The port outputs an interrupt when the Interrupt Enable bit (bit 4) is set to "1" in the CCR and bit 0 is set in the CSR.

### 7-2-3 UART ARCHITECTURE

Figure 7-16 shows a simplified block diagram of the UART circuits. The UART mode utilizes many of the same circuits, circuit functions, and device interfaces as those used in the CART mode. In view of the similarities, coverage of the serial I/O port in the following paragraphs is mainly devoted to the circuit and operational differences between the UART mode and the CART mode.

#### 7-2-3.1 CART REGISTER ADDRESS DECODER

The CART register address decoder allows access to all memory-mapped UART registers for software operations. Table 7-6 (page 7-28) provides a memory address map of these registers, and Figure 7-17 (page 7-28) shows the data format of these registers.

The only difference between the UART address map and the CART address map is the assignments of addresses  $\text{^nn}00\text{-}^{\text{nn}}1D$  (where nn is 09, 12, and 0F for EEC-IV device mask options "A", "C", and "D", respectively). The microprocessor has priority access only to the UART transmit buffer (UTB) and the UART receive buffer (URB) which are both read and write. The microprocessor should not write the URB during normal operations; otherwise, an incoming message may be lost. Accessing a memory-mapped UART register is the same as accessing a CART memory-mapped register. Differences in the data format of the UART circuits with respect to the CART circuits is provided in the paragraphs that follow.

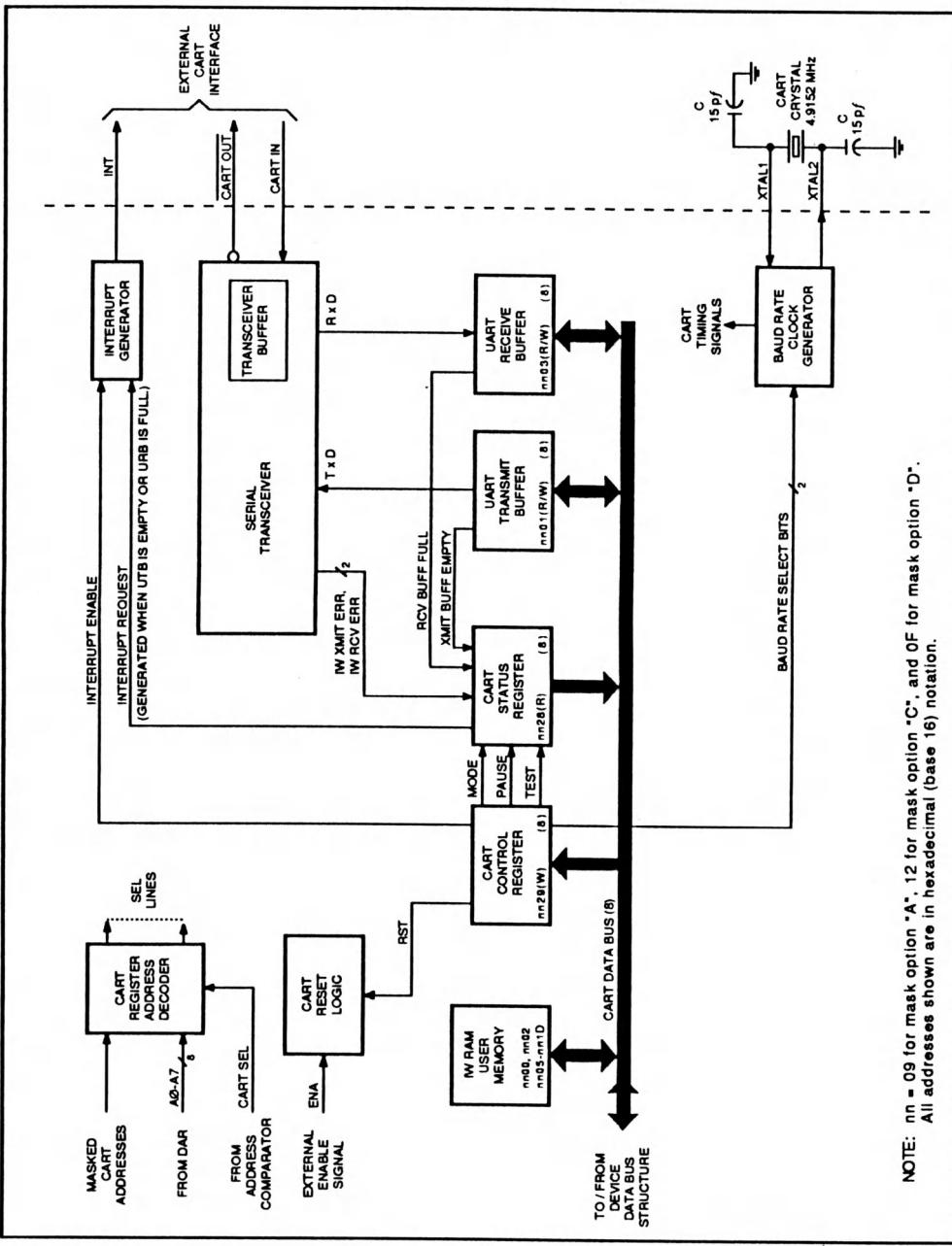


FIGURE 7-16. UART MODE CIRCUITS SIMPLIFIED BLOCK DIAGRAM

TABLE 7-6. UART MODE REGISTER ADDRESS MAP

ADDRESS <sup>①</sup>	• A •	• C •	• D •	READ	WRITE
0900	1200	0F00	(2)		(2) UART Transmit Buffer
0901	1201	0F01	UART Transmit Buffer		(2) UART Receive Buffer
0902	1202	0F02	(2)		(2) UART Receive Buffer
0903	1203	0F03	UART Receive Buffer		(2)
0904	1204	0F04	(2)		:
:	:	:	:		:
091D	121D	0F1D	(2)		(2)
0920	1220	0F20	:		
0928	1228	0F28			{ Same as CART Mode (See Table 7-1).
093A	123A	0F3A			
093D	123D	0F3D			

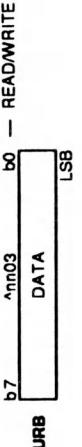
## NOTES:

1. Addresses in left column are for EEC-IV device mask option "A", middle column are for device mask option "C", and right column are for device mask option "D". All addresses shown are in hexadecimal (base 16) notation.
2. In the UART mode, these locations can be used as regular read/write RAM locations. In the CART mode, these locations are used for the IW registers.

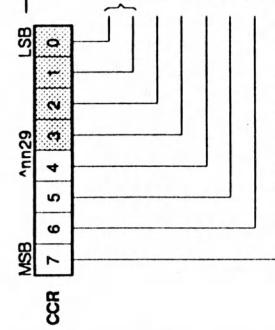
UART TRANSMIT BUFFER



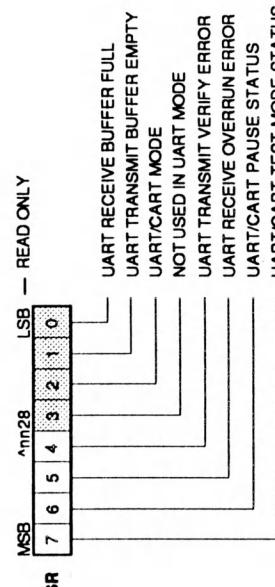
UART RECEIVE BUFFER



CART CONTROL REGISTER



CART STATUS REGISTER



NOTE: nn = 09 for mask option "A", 12 for mask option "C", and 0F for mask option "D".

FIGURE 7-17. UART MODE CIRCUITS DATA FORMAT

### 7-2-3.2 CCR UART/CART MODE SELECT BIT

The UART/CART Mode Select bit (bit 3) of the CCR must be set to select the UART mode. This bit must be simultaneously set with CCR bit 7 (Reset bit) to activate the mode. These two bits can be set in conjunction with other control bits to configure the port for UART operations. The name and function of all control bits, and the operation of the CCR is the same in both the UART mode and the CART mode.

### 7-2-3.3 CART STATUS REGISTER (CSR) IN UART MODE

The name and function of several status bits of the CSR change between the CART mode and the UART mode. Figure 7-17 shows the data format of the register, and Table 7-7 describes each register bit in the UART mode.

### 7-2-3.4 UART TRANSMIT BUFFER (UTB)

The UTB is used to temporarily hold user data for serial transmission. It is a read/write 8-bit register that is accessible in the UART mode only, and it resides in the same location as the high byte of I/W register #0 of the CART mode. Data loaded into the UTB transfers to the transceiver buffer in the serial transceiver when the buffer is empty during the UART transmit mode. Following the transfer, the UTB sets the UART Transmit Buffer Empty status bit (bit 1) in the CSR to indicate a cleared buffer. However, a software read of the UTB following a transfer will return previously written data. Bit 1 of the CSR is cleared when software loads data into the UTB. The UTB is empty following a UART reset. Figure 7-17 shows the data format of the UTB.

TABLE 7-7. CART STATUS REGISTER BITS DESCRIPTION - UART MODE

BIT	NAME AND FUNCTION
0	<b>UART RECEIVE BUFFER FULL BIT:</b> This bit indicates the status of the UART receive buffer (URB). It is set when serially received data is loaded into the URB by the serial transceiver, and it is cleared when software reads data from the URB. If interrupts are enabled in the UART, an interrupt will be generated on the setting of this bit.
1	<b>UART TRANSMIT BUFFER EMPTY BIT:</b> This bit indicates the status of the UART transmit buffer (UTB). It is set when the buffer is empty and can be loaded with data for serial transmission. It is cleared when software writes data into the UTB. It remains clear until data from the buffer is transferred to the serial transceiver, at which time the bit is set again. If interrupts are enabled in the UART, an interrupt will be generated on the setting of this bit.
2	<b>UART/CART MODE BIT:</b> This bit echoes bit 2 (UART/CART Mode Select bit) of the CCR which is used to select the CART or UART operating mode. It is set for the UART mode; and it is cleared for the CART mode.
3	This bit is not used and its logic state is indeterminate in the UART mode.
4	<b>UART TRANSMIT VERIFY ERROR BIT:</b> This bit is set if a transmit verify error is detected during the serial transmission of the start bit, user data bits, or first stop bit. A UART transmit verify error is determined in the same manner as for the CART mode. This bit is cleared when new data is loaded into the UTB.
5	<b>UART RECEIVE OVERRUN ERROR BIT:</b> This bit is set when both the URB and the transceiver buffer are full of data, and a start bit is detected on the CART IN signal line. When this occurs, the incoming data is lost.
6	<b>UART/CART PAUSE STATUS BIT:</b> Same as CART mode.
7	<b>UART/CART TEST MODE STATUS BIT:</b> Same as CART mode.

## CART

### 7-2.3.5 UART RECEIVE BUFFER (URB)

The URB is used to temporarily hold serially received user data until read by software. The URB is a read/write 8-bit register that is accessible in the UART mode only, and it resides in the same location as the high byte of IHW register #1 of the CART mode. When the URB has data available for a software read, it sets the UART Receive Buffer Full status bit (bit 0) in the CSR. The bit is cleared when the URB is read. The URB is loaded with data from the serial transceiver after the URB is read or cleared by a reset. The URB is empty following a UART reset. Figure 7-17 shows the data format of the URB.

### 7-2.3.6 INTERRUPT GENERATOR

The interrupt generator, when enabled by software, is used to output an active high external INTERRUPT (INT) signal when the UART is requesting service. The UART requests service whenever the UART transmit buffer is empty and can be loaded with new data for serial transmission, or when the UART receive buffer is full of data following the serial reception of data. Basic operation of the interrupt generator is the same in both the UART mode and the CART mode. Bit 4 of the CCR must be set to enable the UART's interrupt function.

### 7-2.3.7 BAUD RATE CLOCK GENERATOR, SERIAL TRANSCEIVER, AND CART RESET LOGIC

The baud rate clock generator, serial transceiver, and CART reset logic perform the same basic functions in the UART mode as in the CART mode. Table 7-8 shows the values and conditions of the UART circuits following a reset.

TABLE 7-8. UART MODE RESET VALUES

CIRCUIT	RESET VALUES	
	HARDWARE	SOFTWARE
CART Control Register	^00	1XXX XXXX
UART Transmit Buffer	Empty	Empty
UART Receive Buffer	Empty	Empty
CART Status Register	Cleared	Indeterminate
Serial Input Register	Empty	Empty
Serial Output Register	Empty	Empty

### 7-2.4 UART PAUSE MODE

The UART pause mode is used to halt all serial I/O port operations. It is enabled when software sets the Pause bit (bit 6) in the CCR. The port does not enter the pause mode until it detects the end of the data byte being transmitted or received. The port remains in the pause mode until CCR bit 6 is cleared, at which time, normal port operations resume. If software initiates a port reset followed by a pause request, the port will immediately enter the pause mode after the reset.

### 7-3 CART/UART SOFTWARE READ/WRITE OPERATIONS

The CART/UART port must be conditioned for the system's serial data communication environment following the stabilization of the port's crystal oscillator upon a device power-up and reset. Thereafter, software should normally read and write the port during the processing of frame slot #F for the CART mode, or read and write the port based upon the state of bits 0 (UART Receive Buffer Full bit) and 1 (UART Transmit Full Buffer bit) in the CART status register (CSR) for the UART mode. The port can be programmed to output an interrupt at the beginning of a frame (i.e., frame slot #F) or upon the update of UART CSR bits 0 and 1. Upon servicing the port interrupt, the external controller via the program can take the necessary steps, as required, to maintain serial I/O data communications and/or port operations for the CART or UART mode.

All software data written to or read from the CART/UART port is via the device's 8-bit wide MBus interface. MBus signal lines MB0 through MB7 directly correspond to bits 0 through 7 and 8 through 15 in all port circuits, respectively. MB0 is the MBus least significant bit line. Prior to any port software read or write operation, the address of the port circuit to be accessed must be loaded into the device's data address register (DAR). When a CART/UART address is in the DAR, it enables a handshake between the CART/UART circuits and the device's MBus interface.

## 7-4 CART/UART DATA PARITY GENERATOR/ERROR DETECTOR ALGORITHMS

The CART/UART port does not generate or detect parity on serial transacted data. Data parity generation and error detection can be easily implemented by software using the algorithms provided in the following paragraphs. The algorithms presented do not provide for data error correction.

The parity algorithms take advantage of the fact that the CART/UART port can serially transmit and receive a 16-bit data word in the CART mode, and two 8-bit data bytes in succession in the UART mode. Since the CART and UART serial data formats do not provide any extra bits for data parity implementation, the following algorithms require one 4-bit nibble of the 16-bit data word for a parity value. This leaves a maximum of twelve bits for user data. Figure 7-18 shows the data and parity format of the 16-bit word.

### Data Parity Generator Algorithm

The data parity generator algorithm is as follows:

$$\wedge A \oplus N\emptyset \oplus N1 \oplus N2 = N3$$

where:

$\wedge A$  = Fixed Algorithm Value,  
 $\oplus$  = Exclusive-Or Operation,  
 $N\emptyset-N2$  = User Data Nibbles, and  
 $N3$  = Parity Nibble.

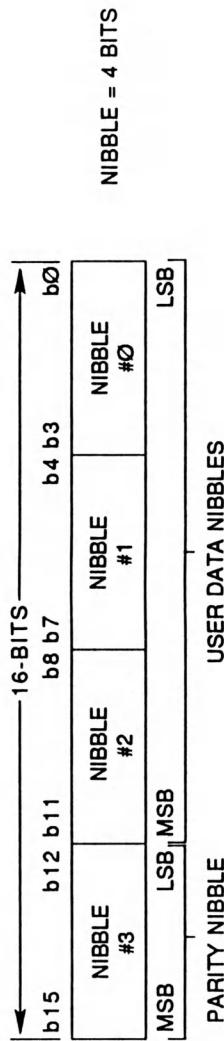
Nibbles  $N\emptyset$  thru  $N2$  can be Exclusively-OR'd in any sequence with the fixed algorithm value  $\wedge A$  to generate parity nibble  $N3$ . The parity nibble can be located anywhere within the 16-bit serial formatted word; however, it is recommended that it is located in the upper significant bits of the word following the user data bits. Figure 7-18 also shows an example of how data parity is generated using the algorithm.

### Data Parity Detector Algorithm

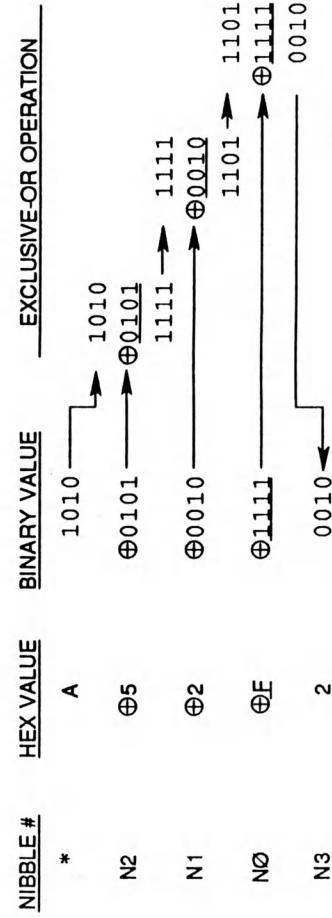
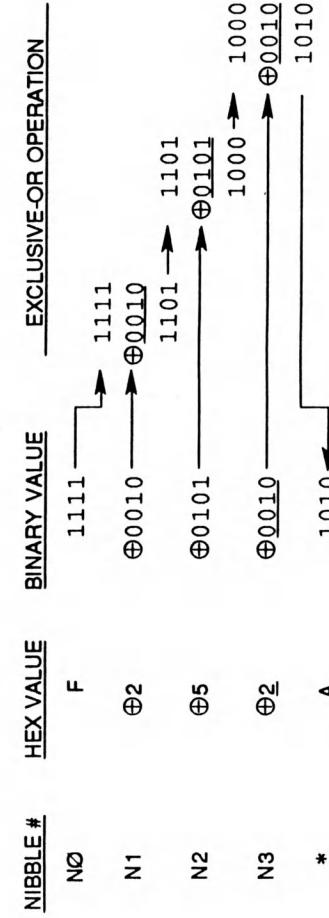
The data parity error detection algorithm is as follows:

$$N\emptyset \oplus N1 \oplus N2 \oplus N3 = \wedge A$$

where  $N\emptyset$  thru  $N3$  are data nibbles serially received via the data communication link. The nibbles can be Exclusively-OR'd in any sequence to obtain the fixed algorithm value  $\wedge A$  (1010). If the value obtained does not yield the fixed algorithm value, the received data is in error and should not be used. Figure 7-18 shows an example of how data parity is checked using the error detection algorithm.

DATA AND PARITY FORMATEXAMPLE

NIBBLE #	N3	N2	N1	N0
DATA NIBBLES	^2	^5	^2	^F
PARITY	MSB	MSB	MSB	LSB

PARITY GENERATIONPARITY ERROR DETECTION

\* FIXED ALGORITHM VALUE

FIGURE 7-18. CART/UART SERIAL DATA PARITY FORMAT AND EXAMPLE

