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RELAY CONTROL CHART

JUMPER TABLE

* SEE ASSEMBLY INSTRUCTIONS

REVISIONS		
OPTION	DATE	APPROVED

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P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

TEMPLATE ENGINEER -	DATE	SCHEMATIC						
HARDWARE SERVICES -								
HARDWARE SYSTEMS -		HW TYPE : Customer Evaluation						
TEST ENGINEER -		Product(s) : N/A : N/A						
COMPONENT ENGINEER -		PACKAGE : N/A-lead N/A N/A-family : Pitch-pitch Style Vendor Style						
TEST PROCESS -		<User Define> <User Define> <User Define>						
HARDWARE RELEASE -								
DESIGNER -		MASTER PROJECT TEMPLATE TBD	TESTER TEMPLATE no_template	DRAWING NO. 02_045361	REV. E			
PTD ENGINEER <PTD_ENGINEER>		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES						
CHECKER -		DECIMALS X.XX +-0.010 X XXXX +-0.005	FRACTIONS +1/32	ANGLES +2	SIZE D	SCALE 1:1	CODE ID NO. CodeID	SHEET 1 OF 52

SCHEMATIC



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REVISIONS

REV	DESCRIPTION	DATE	APPROVED

FMC+ HSPC CONNECTOR

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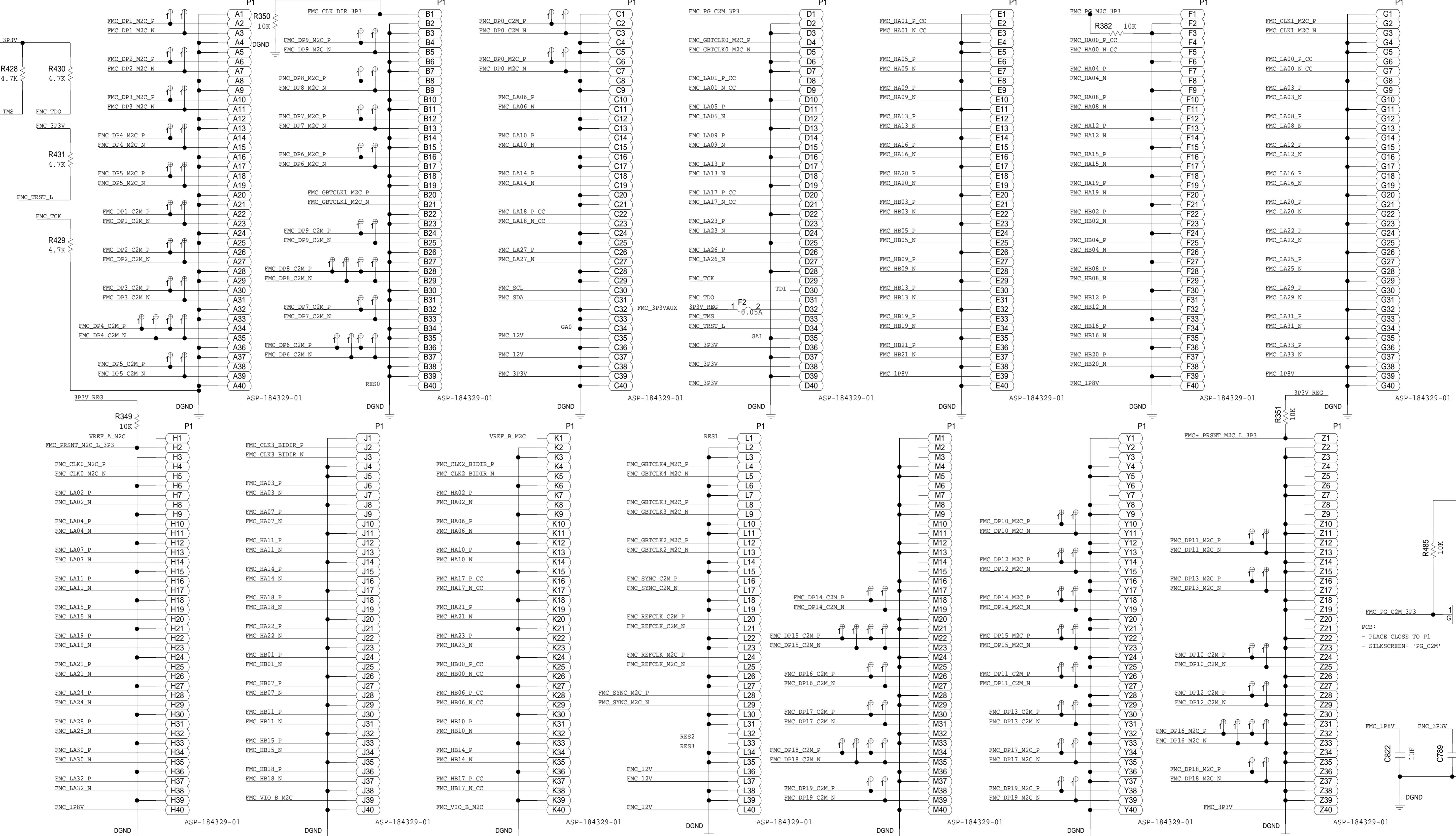
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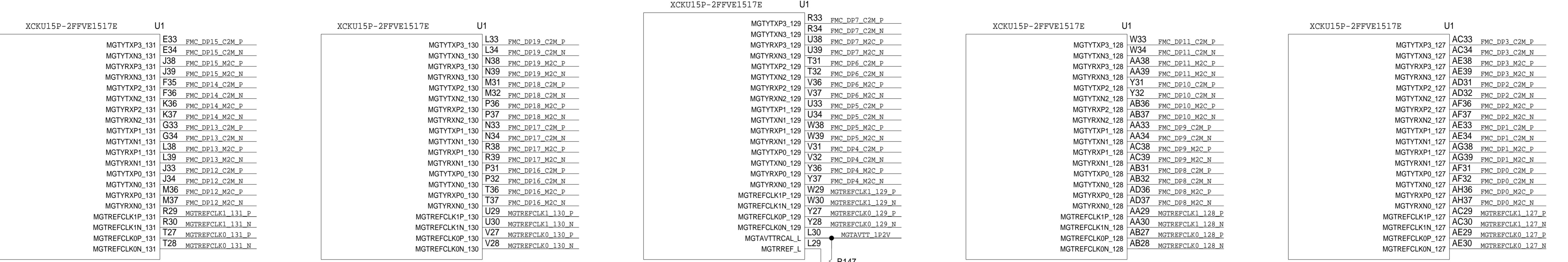
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ANALOG
DEVICESHW TYPE : Customer Evaluation
Product(s): N/A
: N/ADESIGN VIEW
<DESIGN_VIEW>DRAWING NO.
02_045361
REV
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<PTD_ENGINEER>SIZE
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SCALE
1:1
SHEET 2 OF 52

GTY TRANSCEIVERS

REVISIONS		
	DESCRIPTION	DATE



SCHEMATIC

W TYPE : Customer Evaluation
product(s): N/A
: N/A

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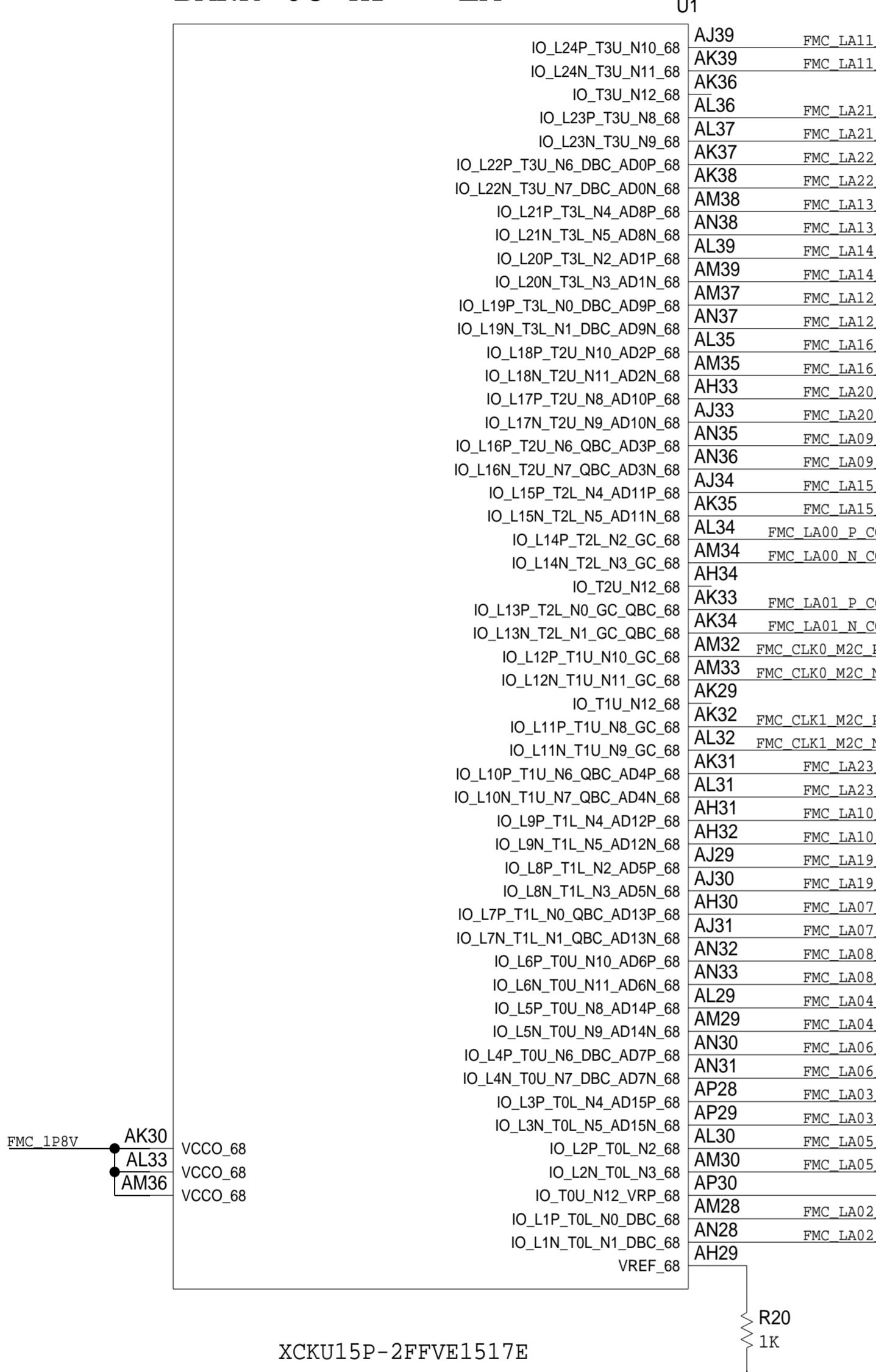
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SIZE D	SCALE 1:1

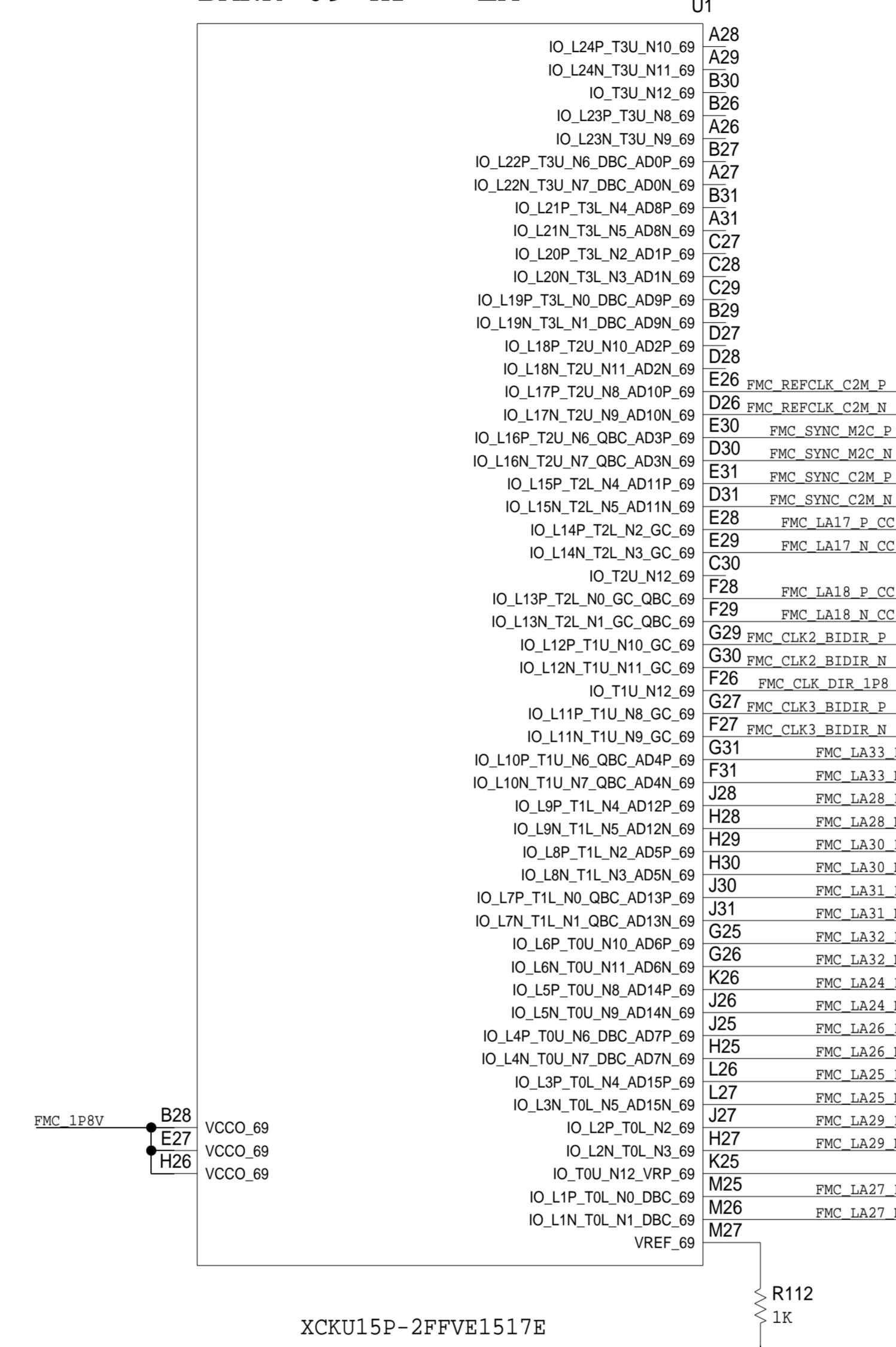
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REV	DESCRIPTION	DATE	APPROVED

FMC+ HSPC LA AND HA BANKS

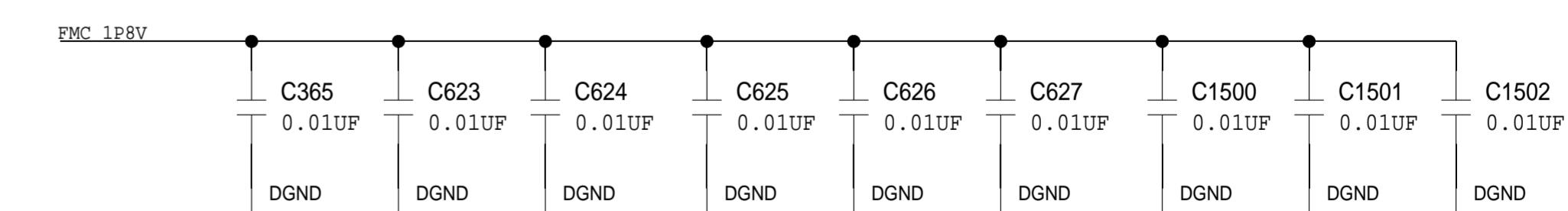
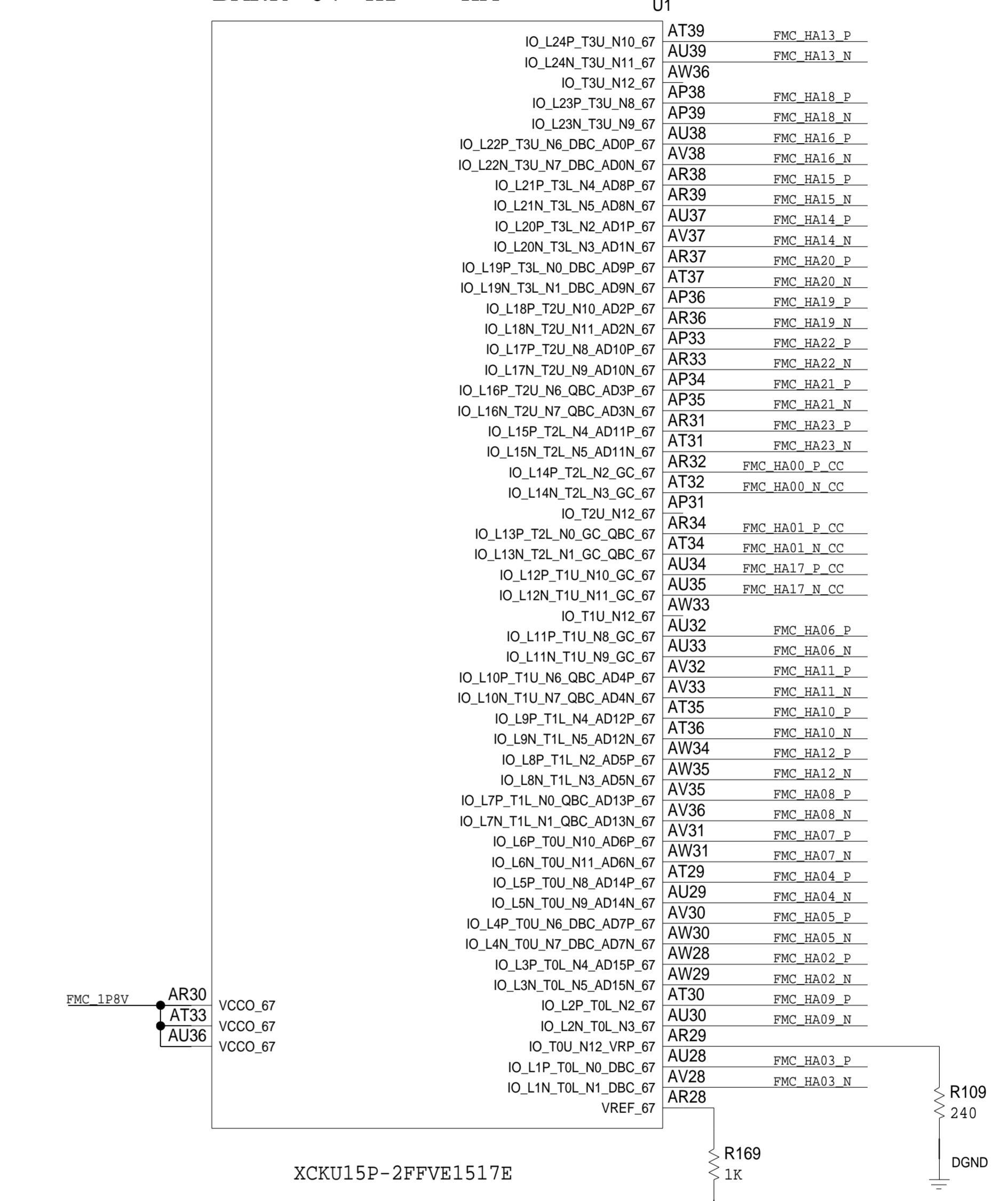
BANK 68 HP - LA



BANK 69 HP - LA



BANK 67 HP - HA



SCHEMATIC

HW TYPE : Customer Evaluation
Product(s) : N/A
: N/A

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DESIGN VIEW
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DRAWING NO.
02_045361

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SHEET 4 OF 52

MICROZED HEADERS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

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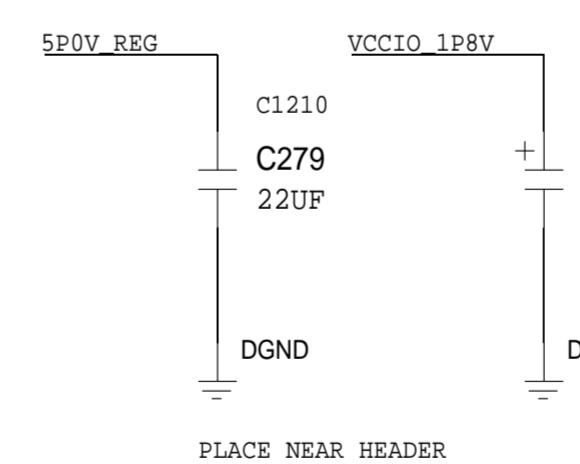
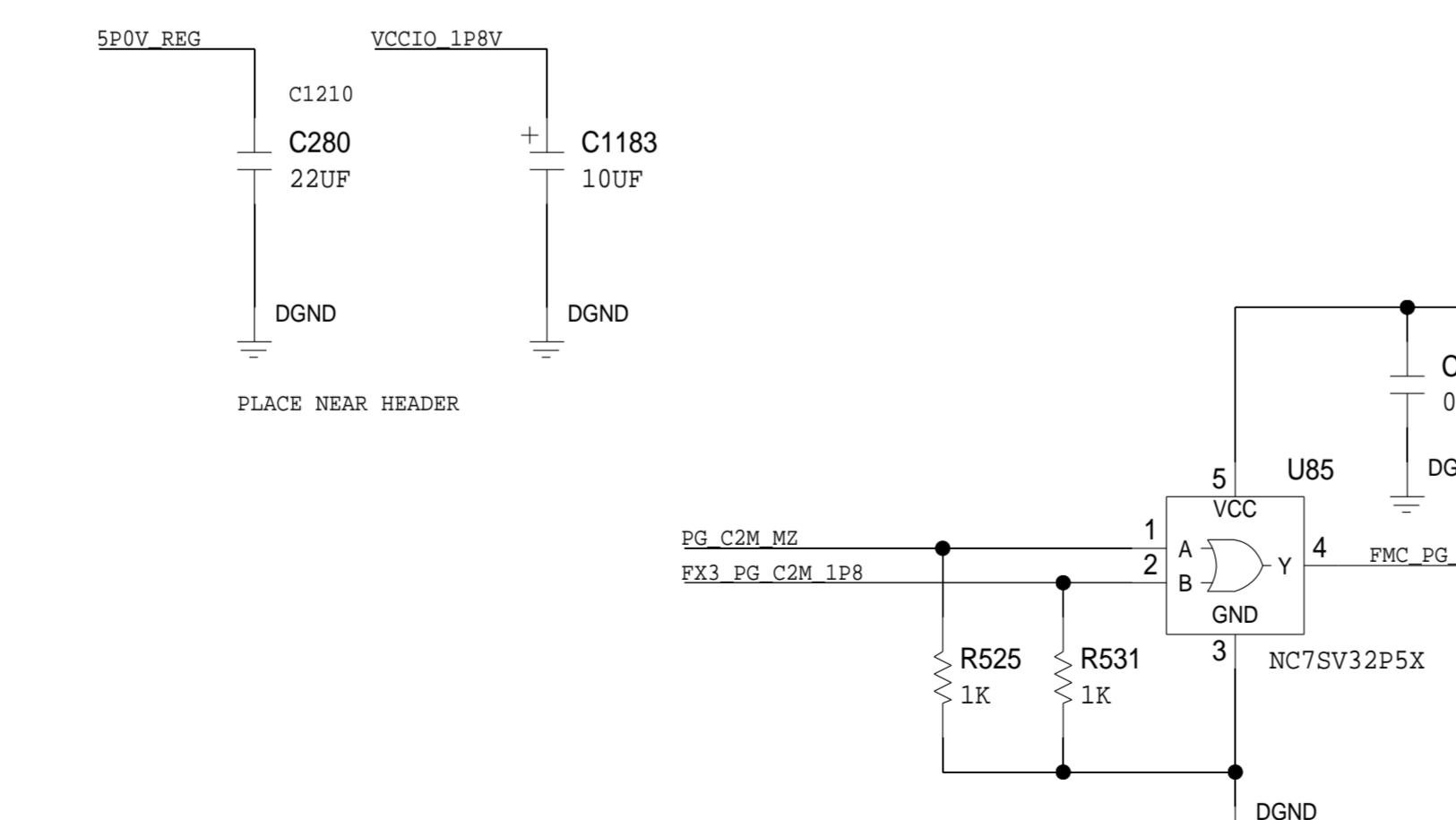
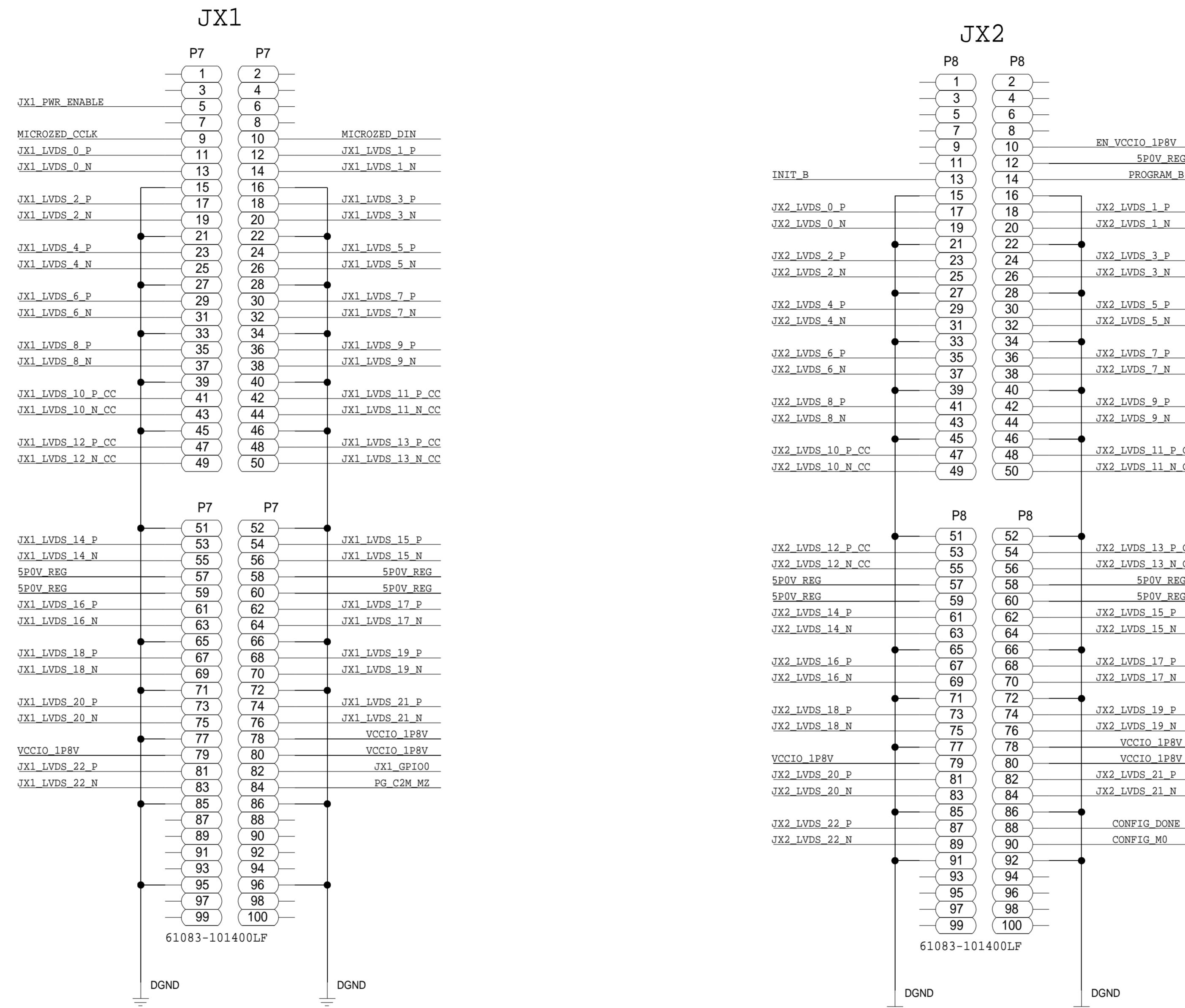
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SCHEMATIC			
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	Product(s): N/A : N/A		REV E
		PTD ENGINEER <PTD_ENGINEER>	SIZE D SCALE 1:1 SHEET 7 OF 52

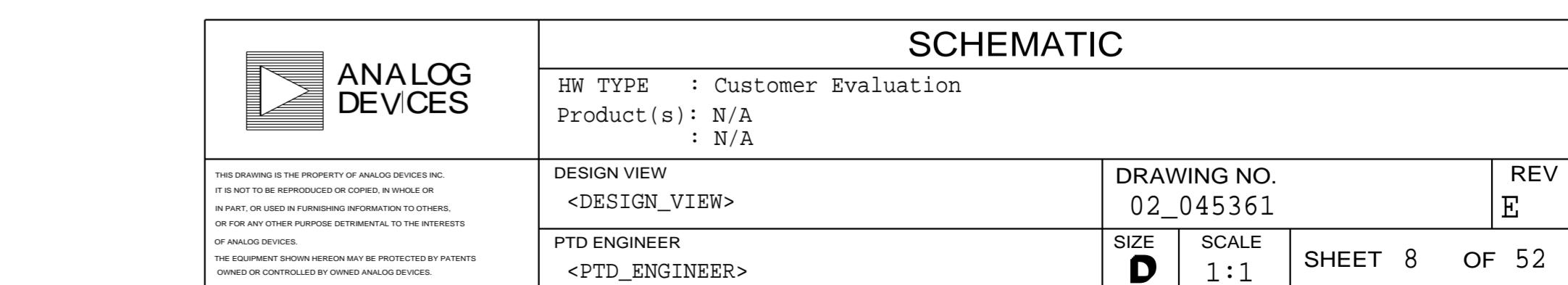
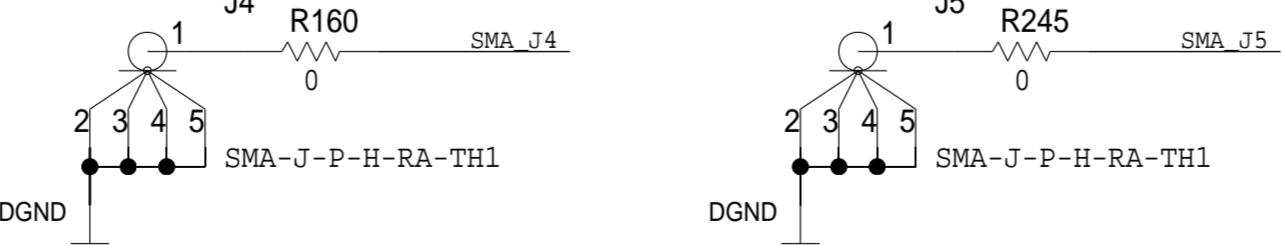
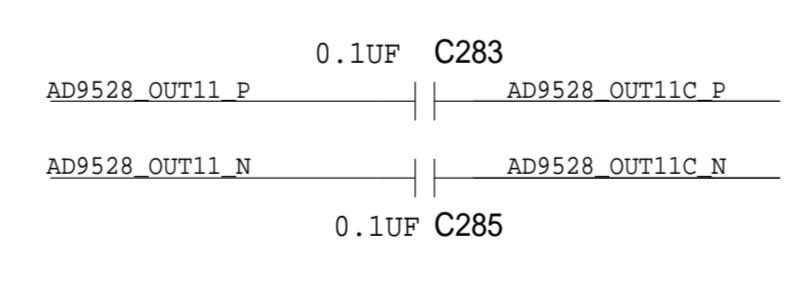
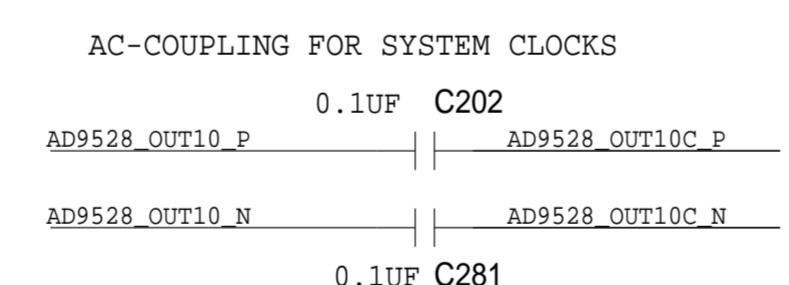
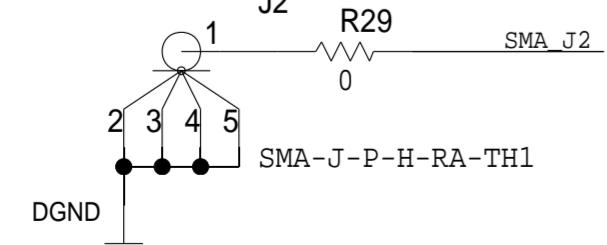
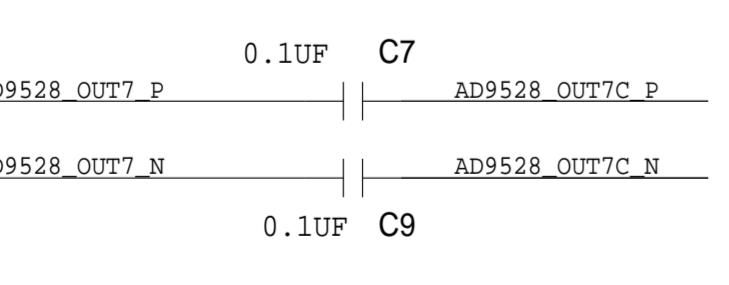
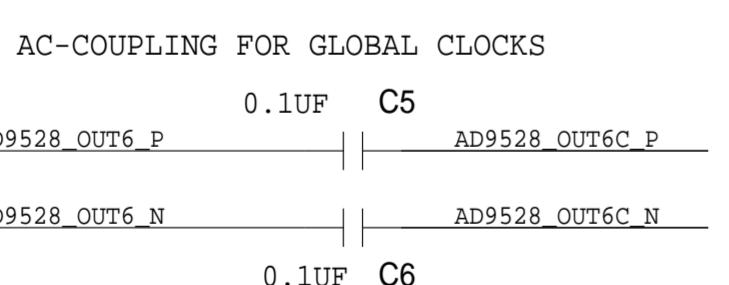
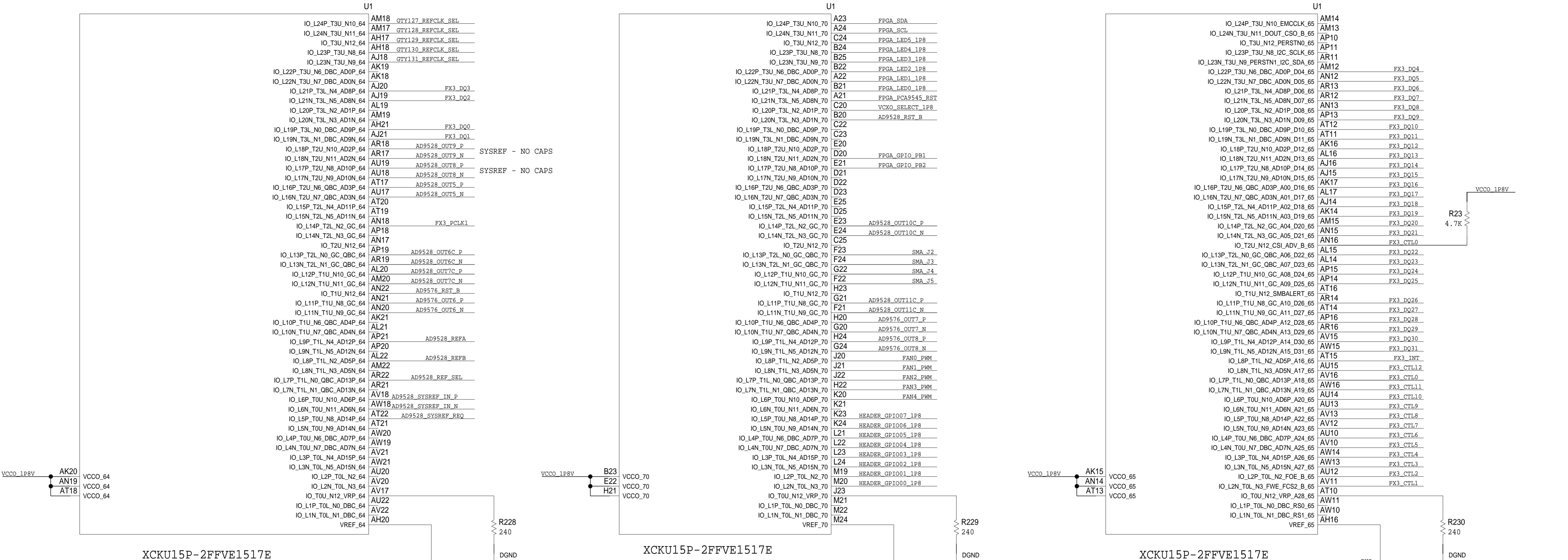
HP BANKS - FX3 AND MISC

REVISIONS		
DESCRIPTION	DATE	APPROVED

BANK 64 HP

BANK 70 HP

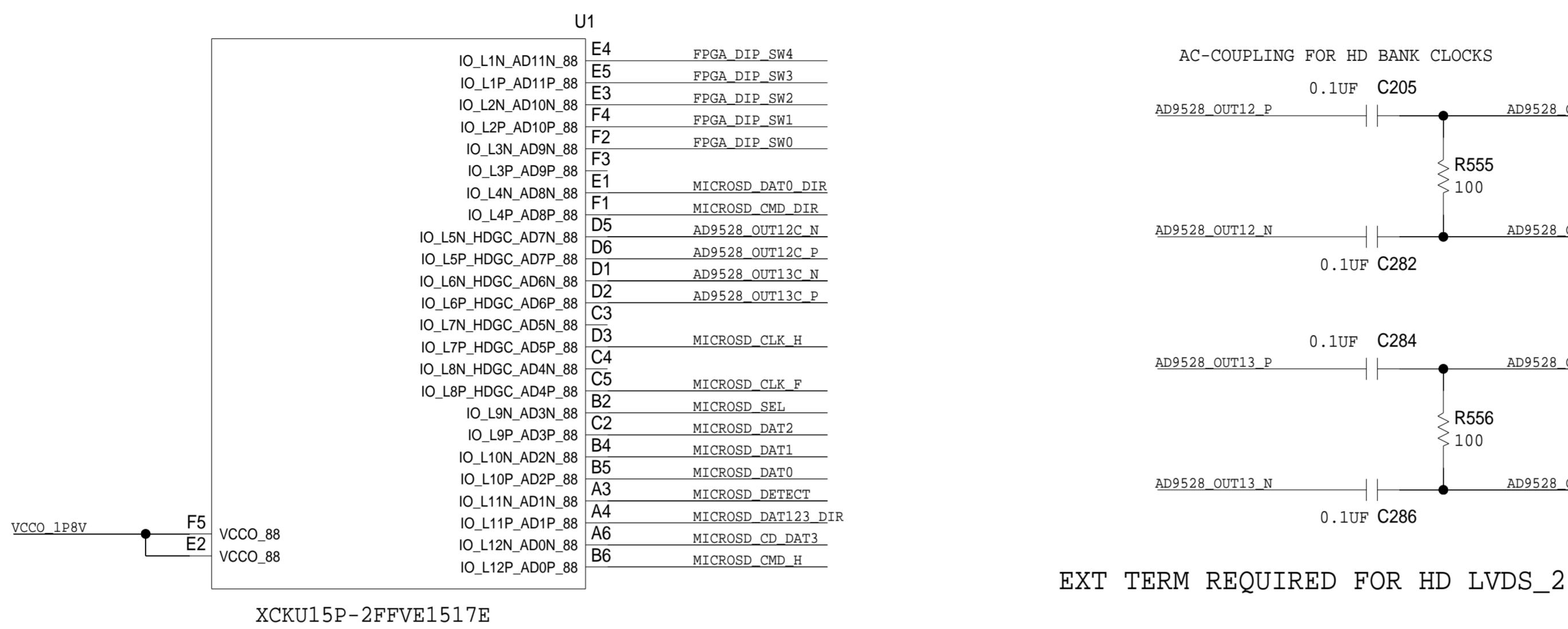
BANK 65 HP



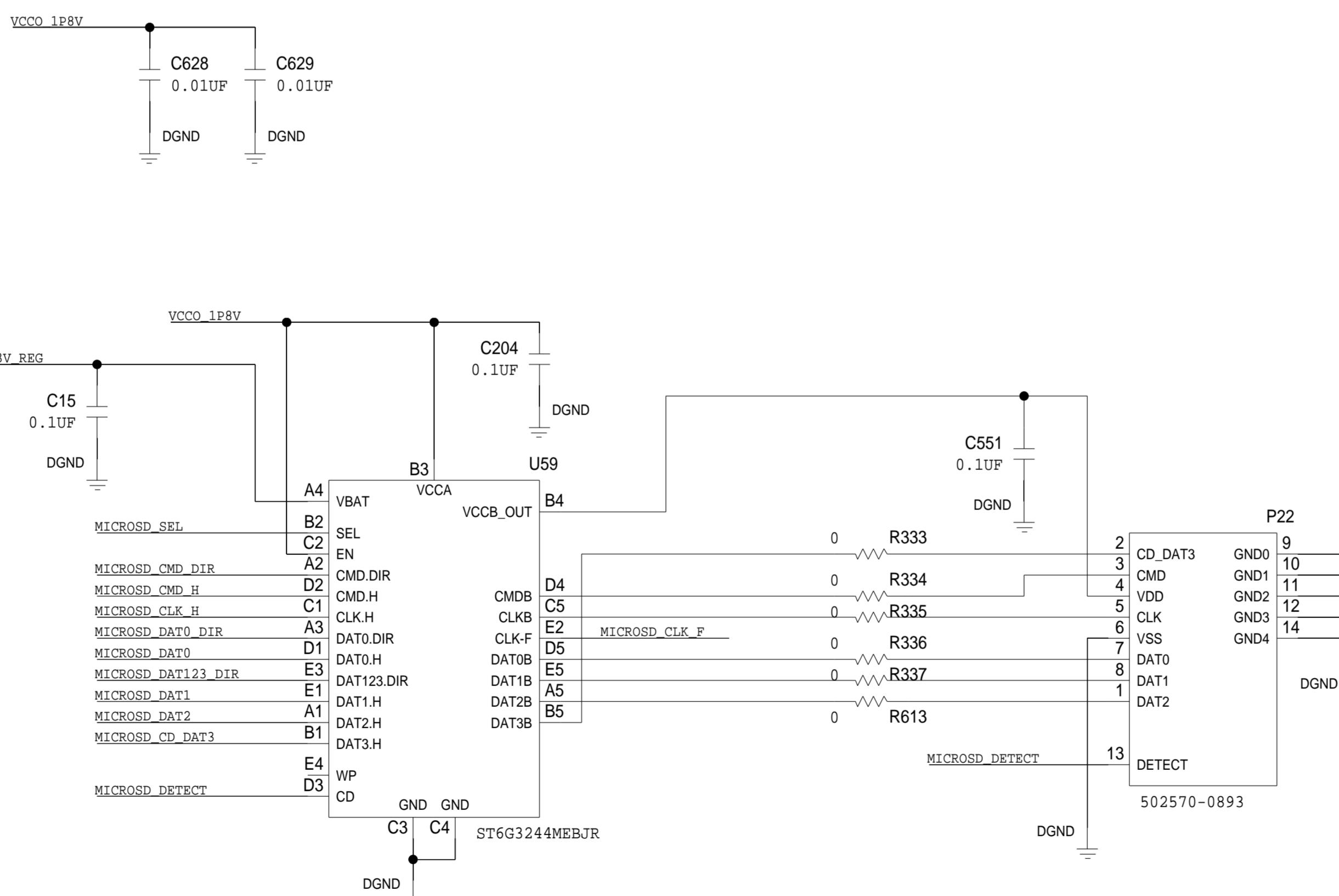
HD BANK - SD CARD, MISC

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

BANK 88 HD



EXT TERM REQUIRED FOR HD LVDS_25 WITH VCCO = 1.8V



SCHEMATIC

HW TYPE : Customer Evaluation
Product(s) : N/A
 : N/A

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DESIGN VIEW

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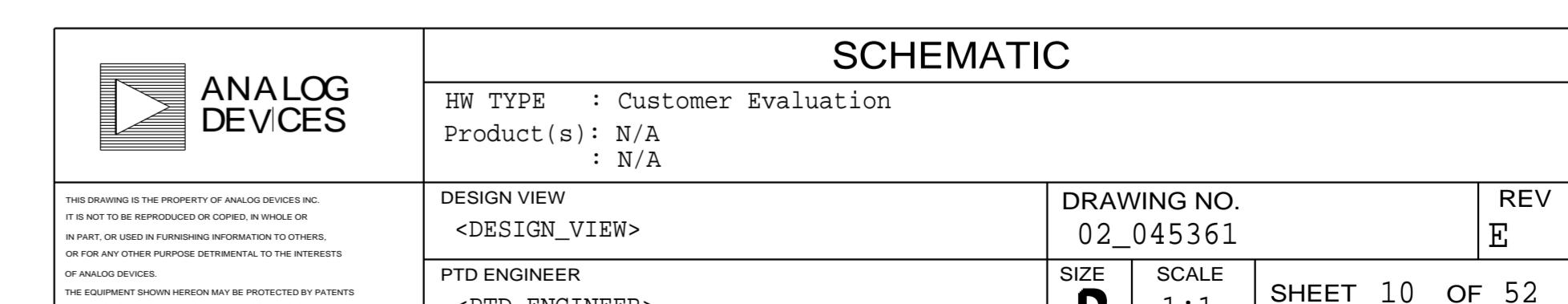
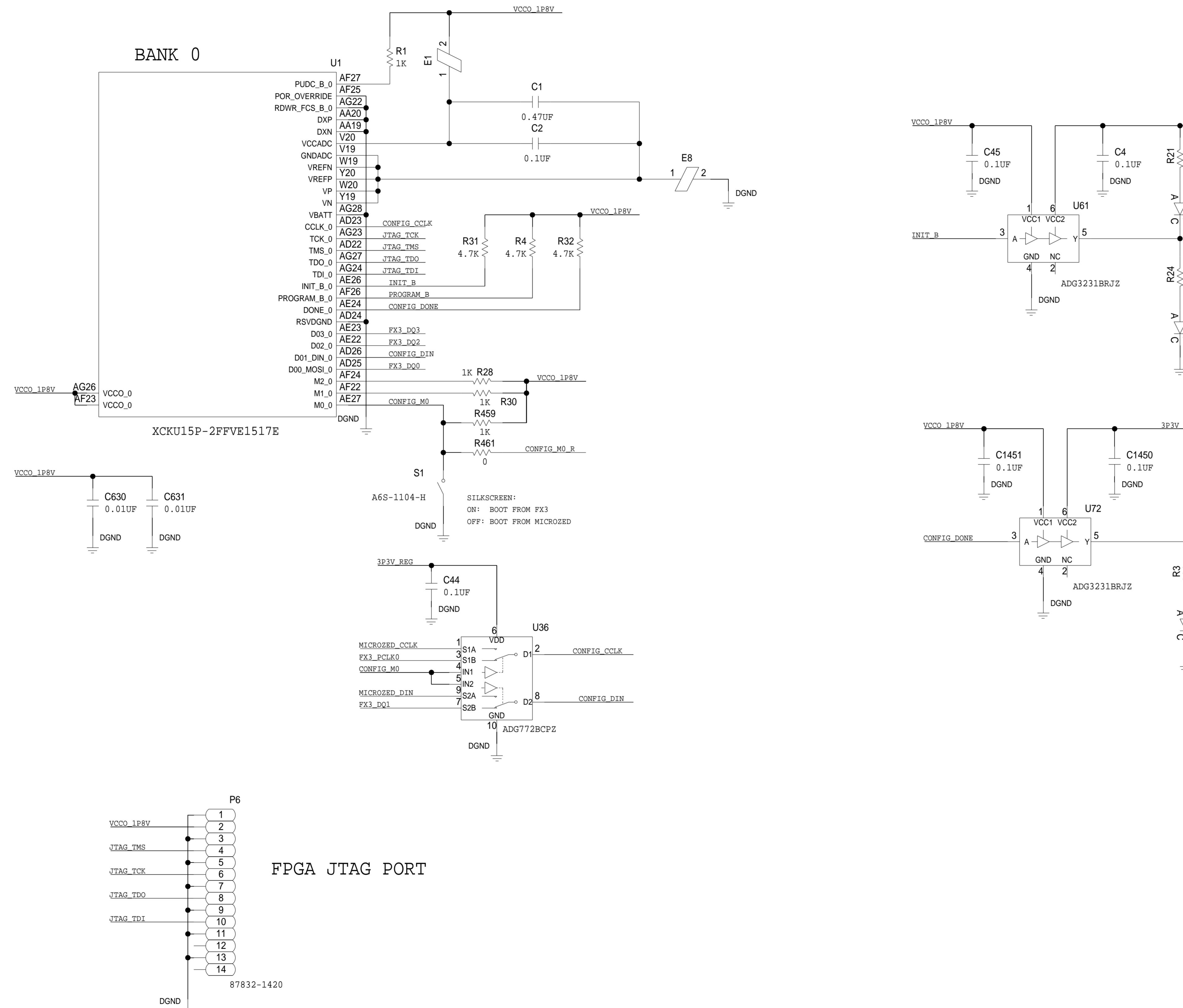
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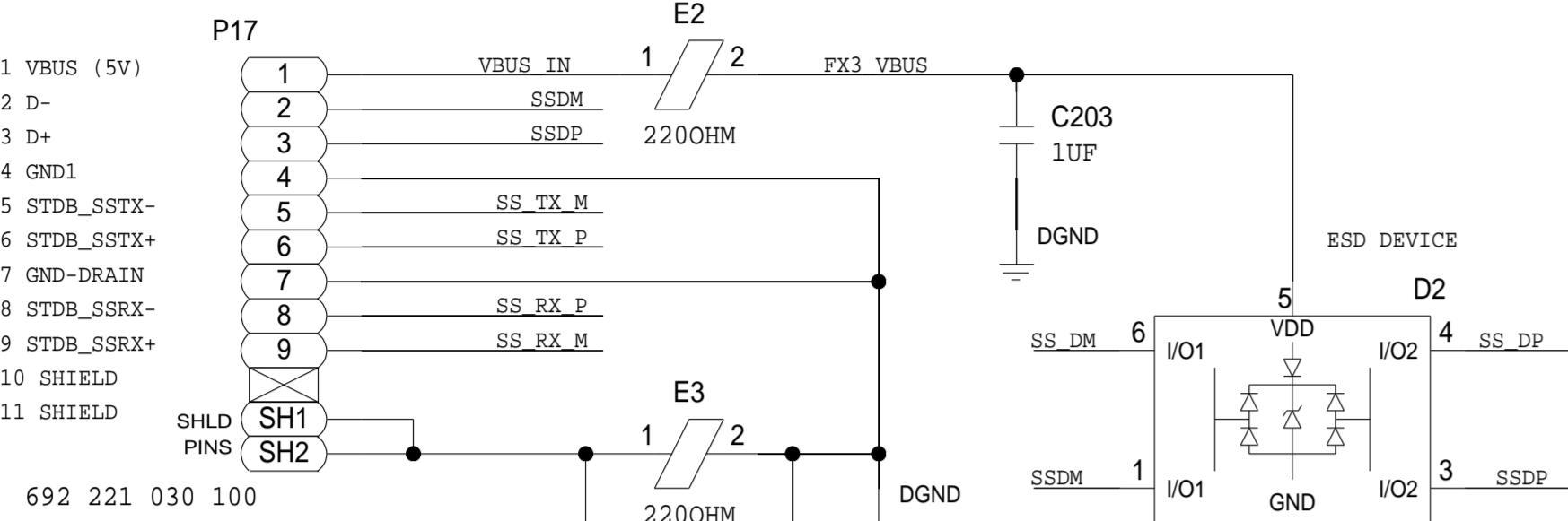
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FPGA CONFIGURATION

REVISIONS		
DESCRIPTION	DATE	APPROVED



FX3 USB CONTROLLER



NOTE:

SS_RX_P AND _M ARE INVERTED!

IDENTICAL TO FX3 BRD

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NOTE:

SS_RX_P AND _M ARE INVERTED!

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NOTE:

SS_RX_P AND _M ARE INVERTED!

IDENTICAL TO FX3 BRD

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CLOCKING - AD9528

REVISIONS		
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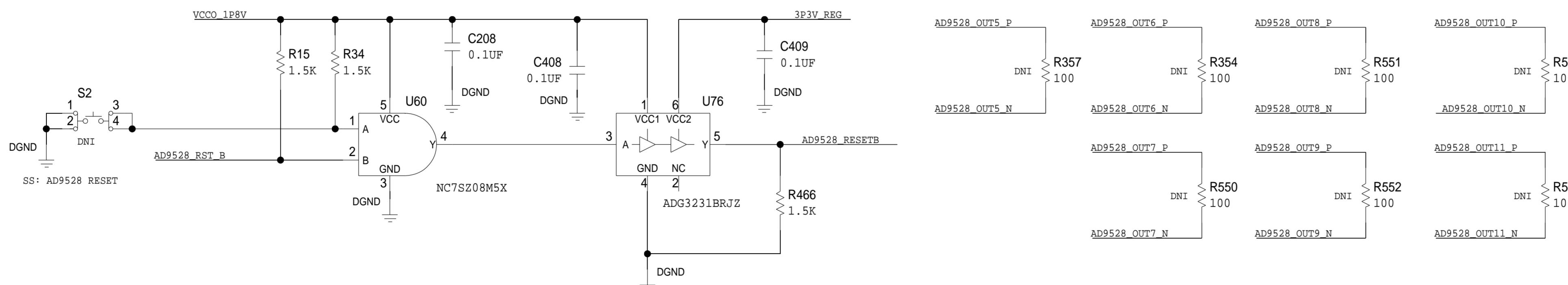
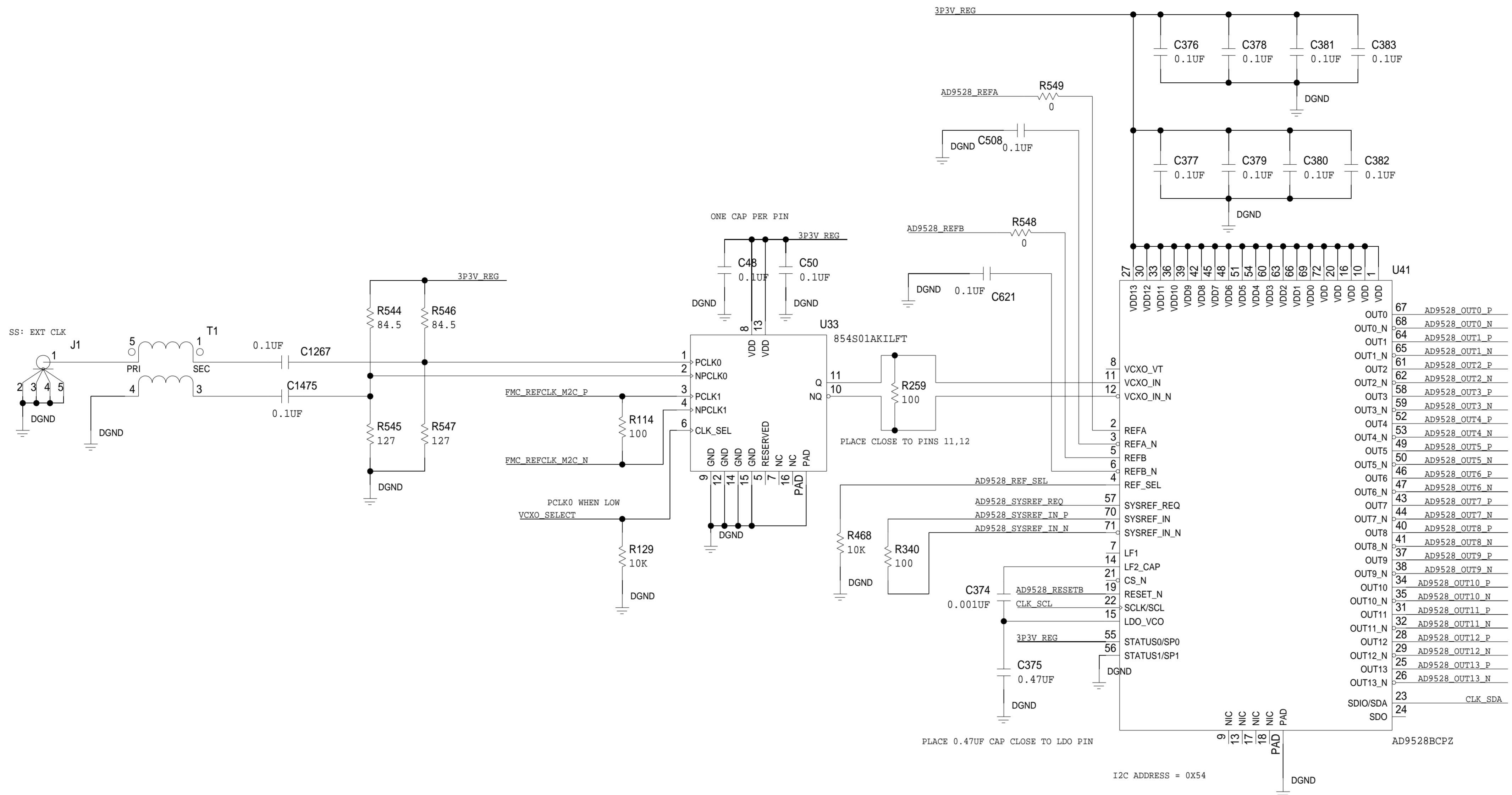
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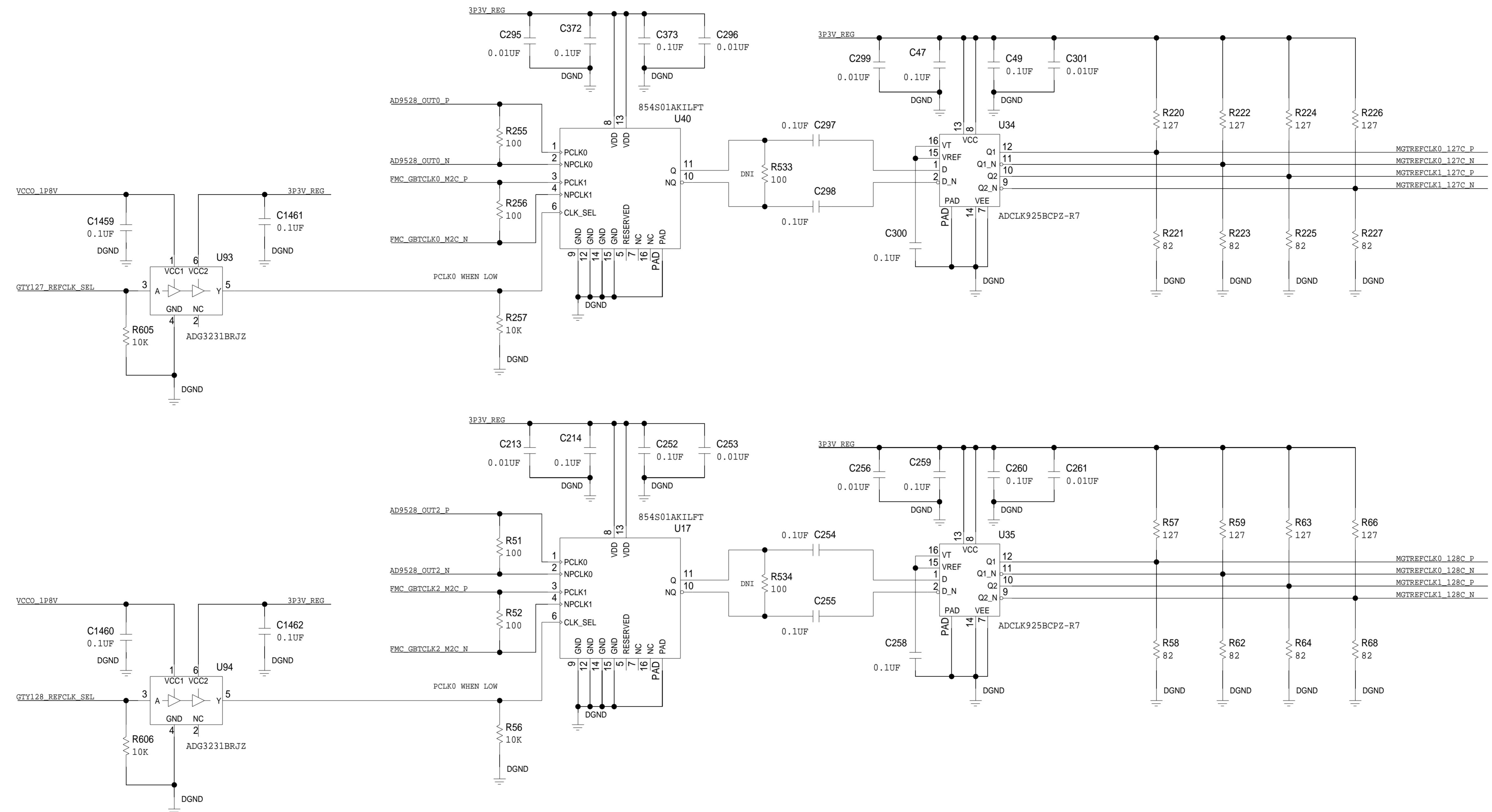


 ANALOG DEVICES	<h1>SCHEMATIC</h1>		
	HW TYPE : Customer Evaluation Product(s): N/A : N/A		
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	PTD ENGINEER <PTD_ENGINEER>	SIZE 	SCALE 1:1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

GTY REFCLK SWITCHING, BANKS 127 AND 128



SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s): N/A
 : N/A

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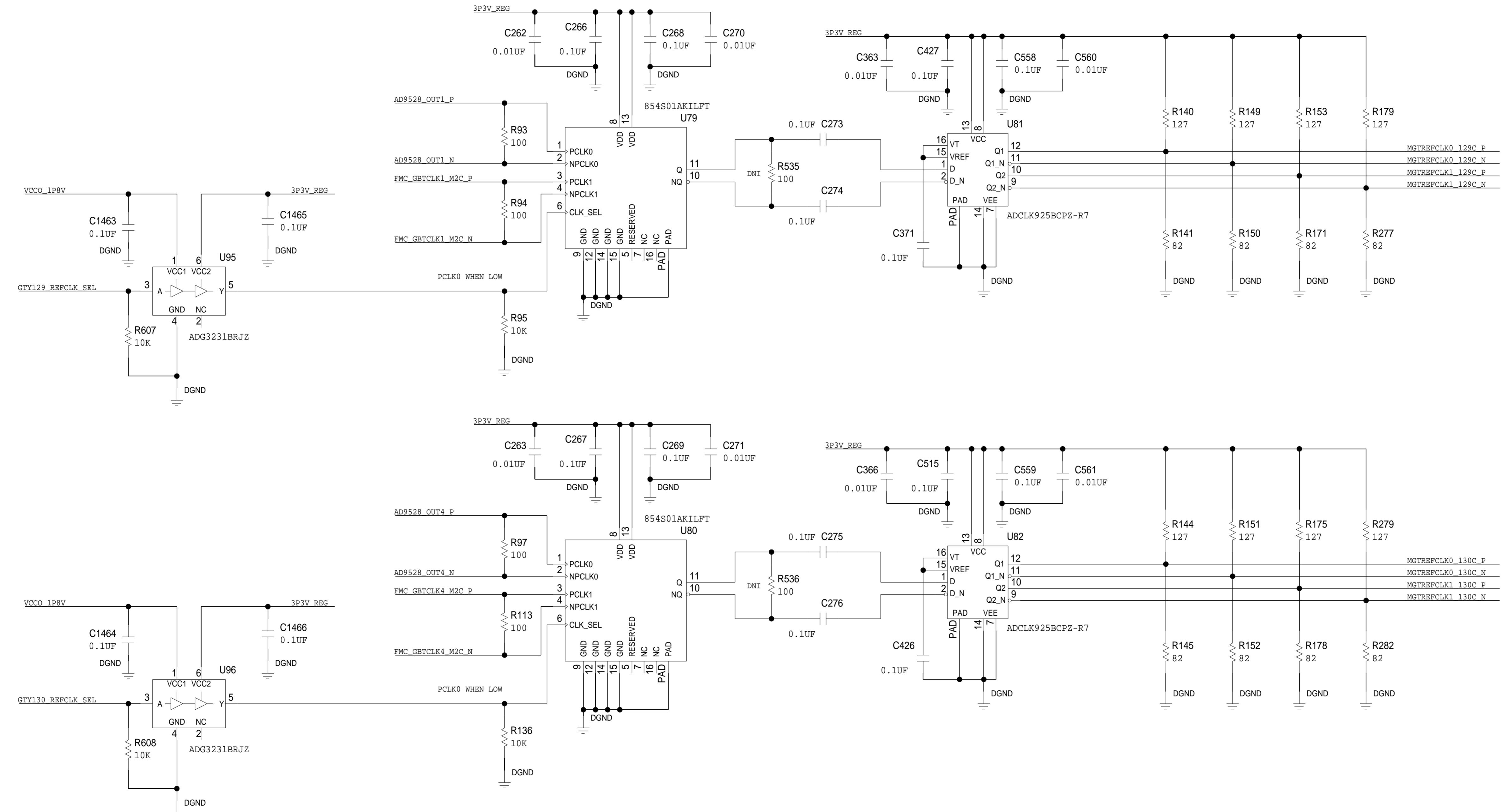
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SHEET

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REV	DESCRIPTION	DATE	APPROVED

GTY REFCLK SWITCHING, BANKS 129 AND 130



SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s): N/A
 : N/A

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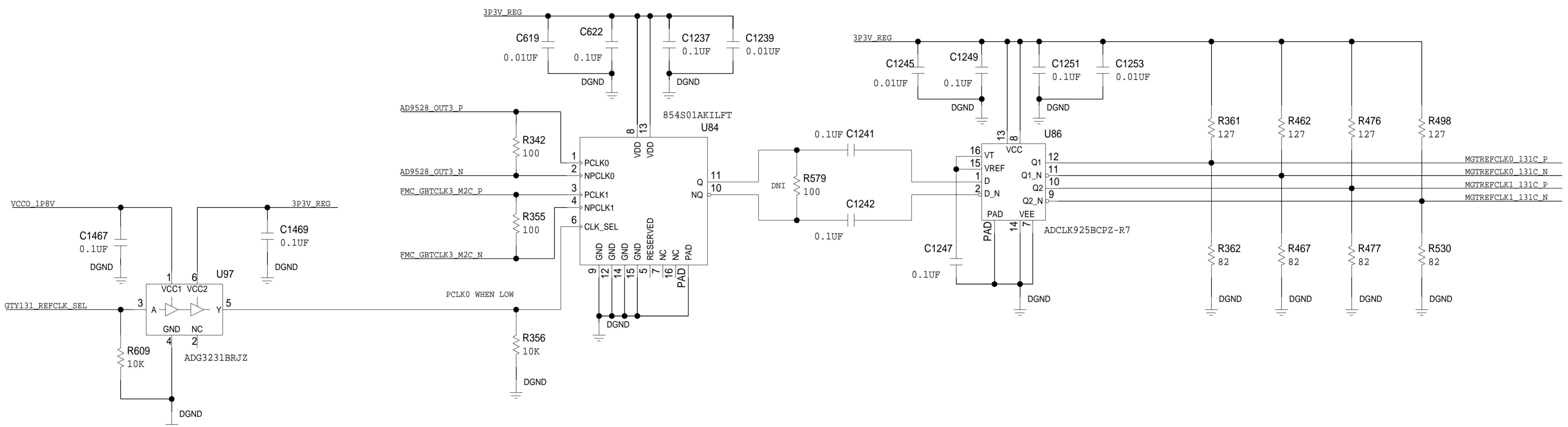
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 SHEET 14 OF 52

GTY REFCLK SWITCHING, BANK 131

REVISIONS

REV	DESCRIPTION	DATE	APPROVED



SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s): N/A
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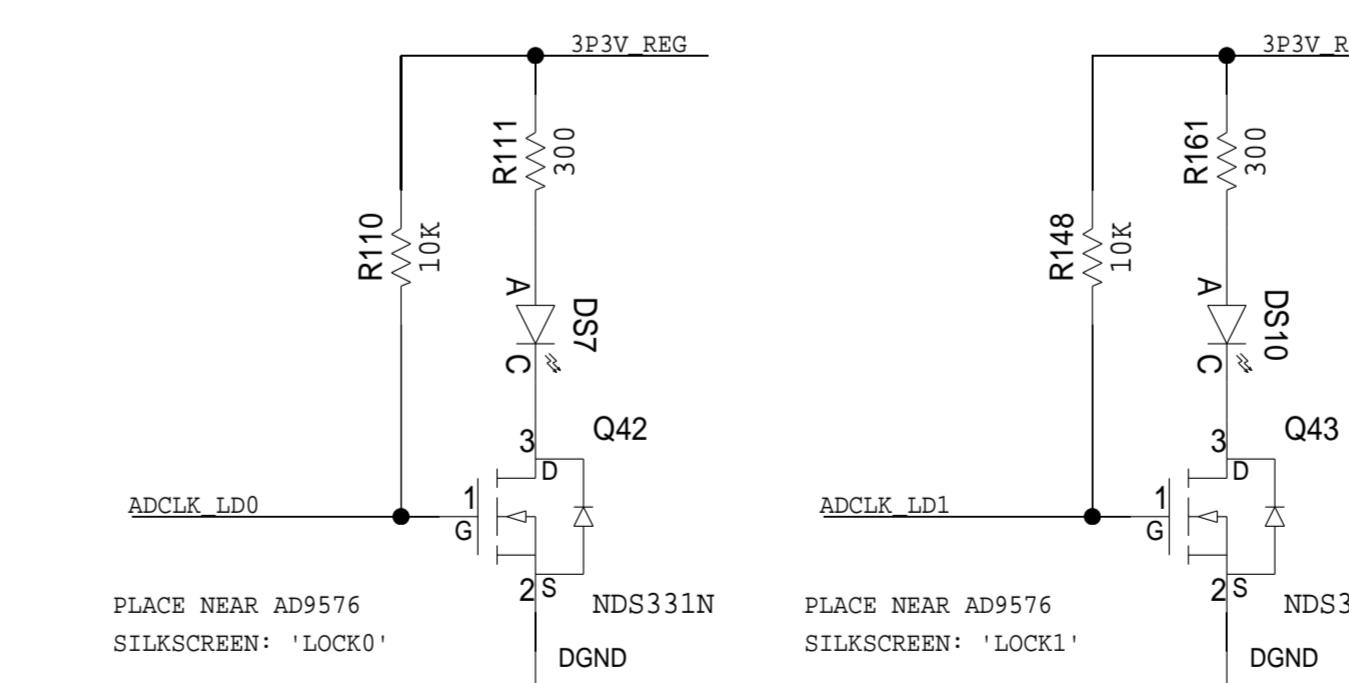
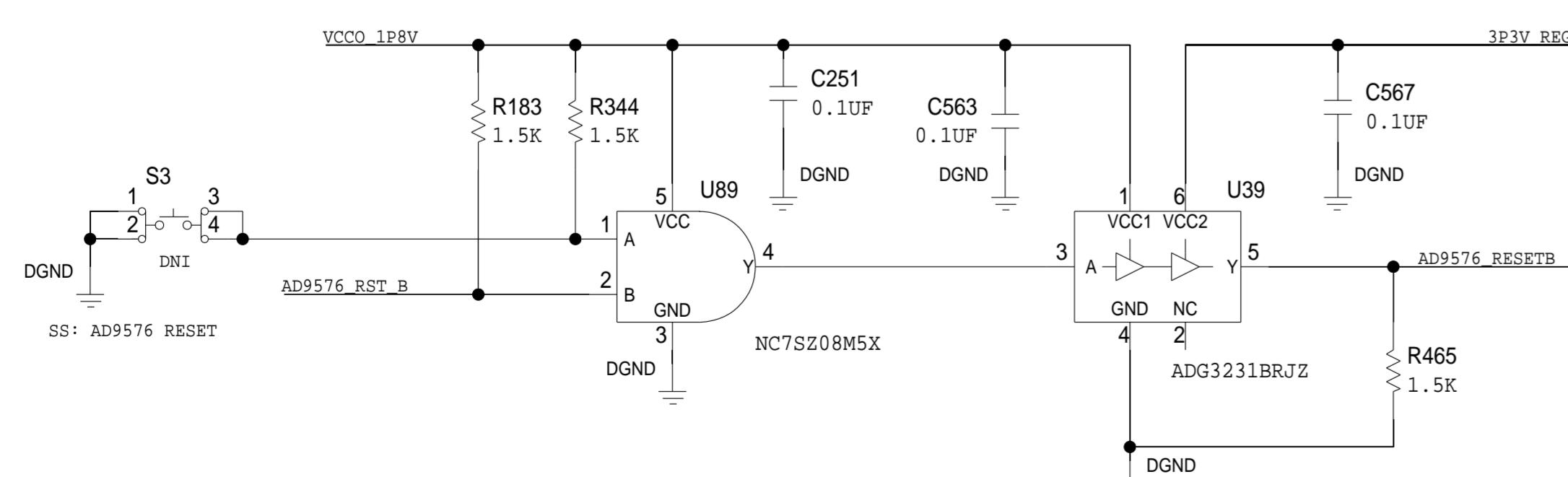
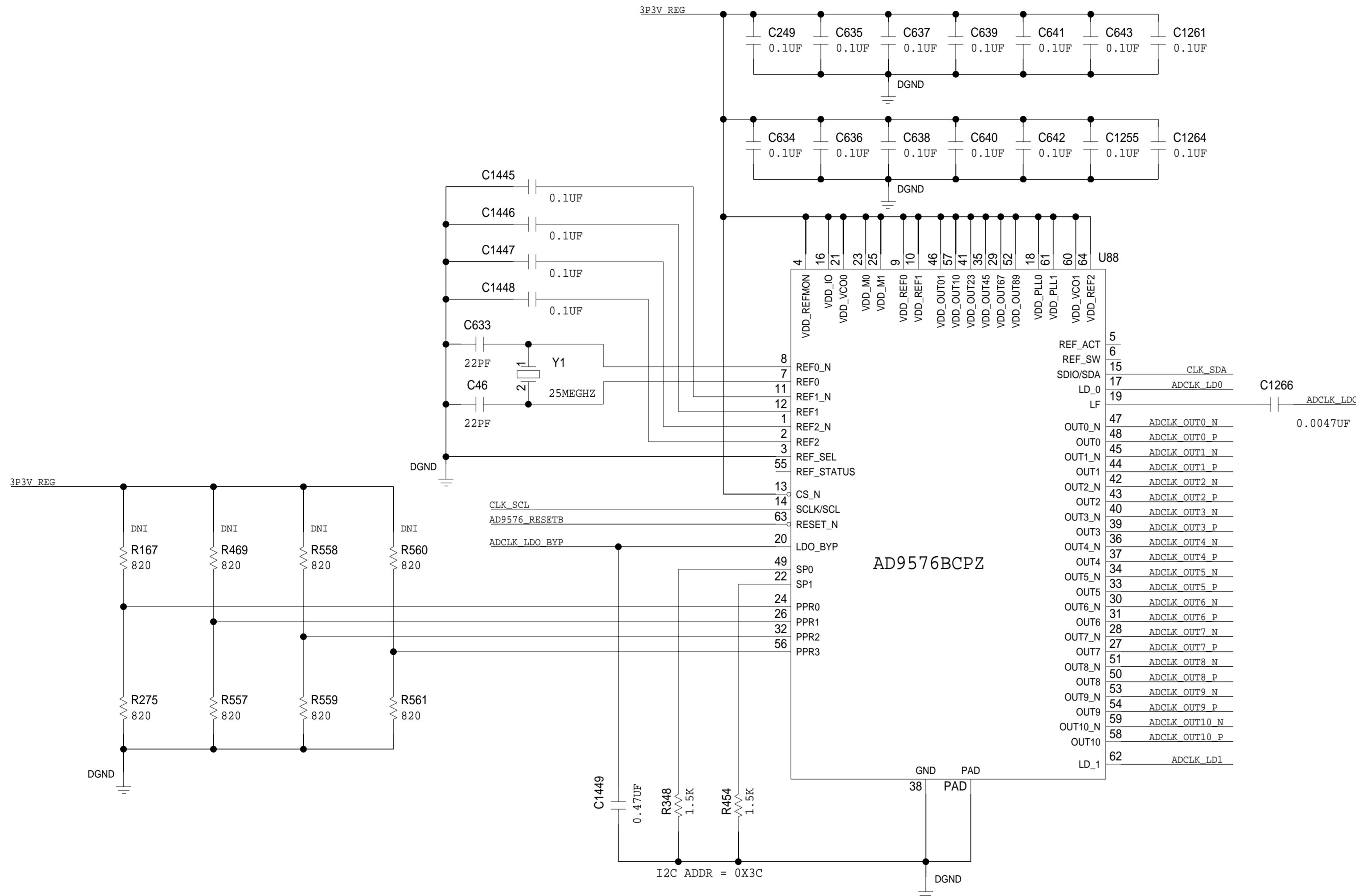
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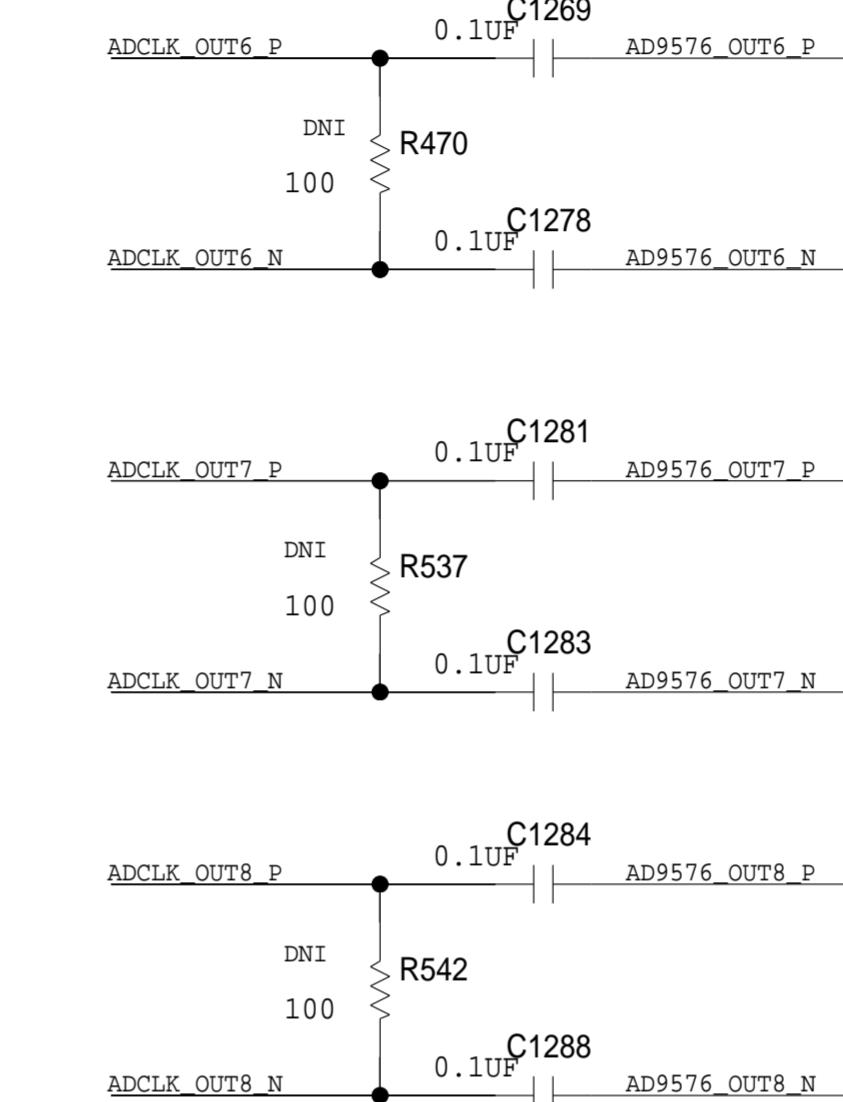
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CLOCKING - AD9576

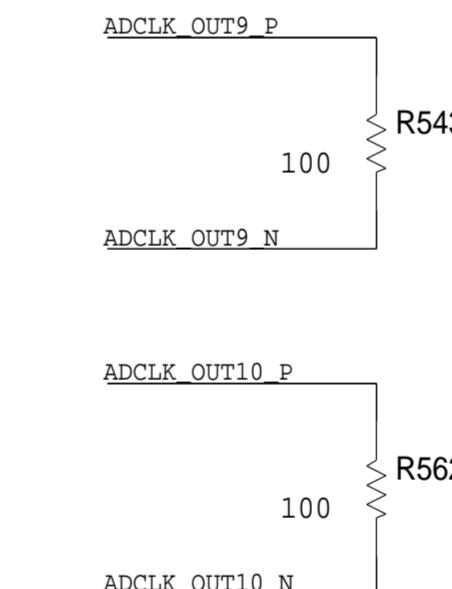


FPGA CLOCKS

PLACE NEAR LOADS



UNUSED OUTPUTS

ANALOG
DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): N/A
: N/A

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DRAWING NO.
02_045361

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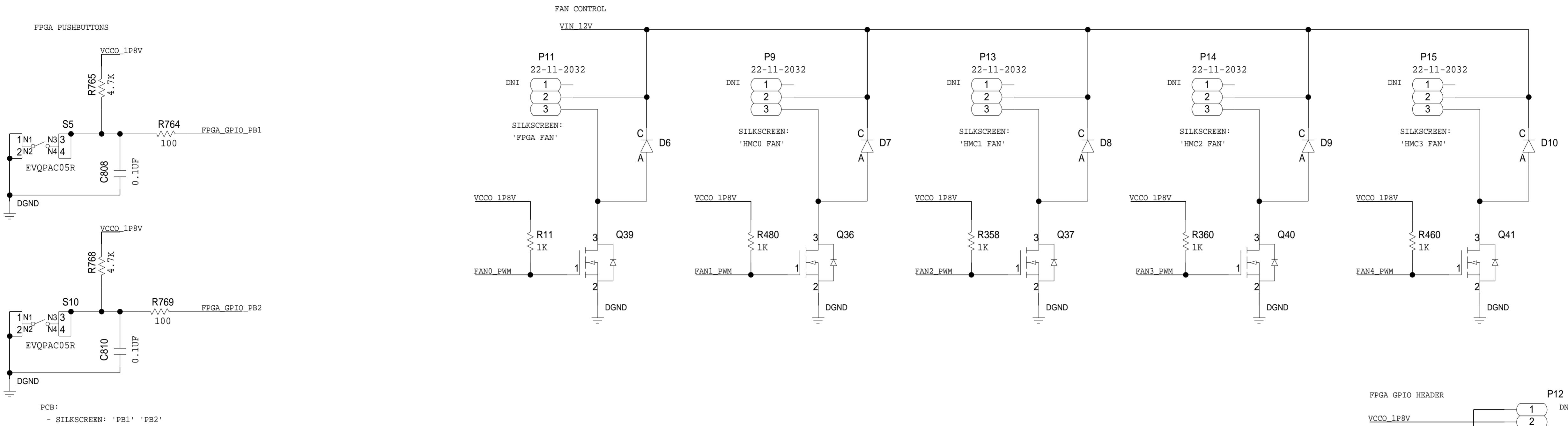
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SHEET 16 OF 52

FANS, GPIO, BUTTONS, ETC

REVISIONS		
DESCRIPTION	DATE	APPROVED

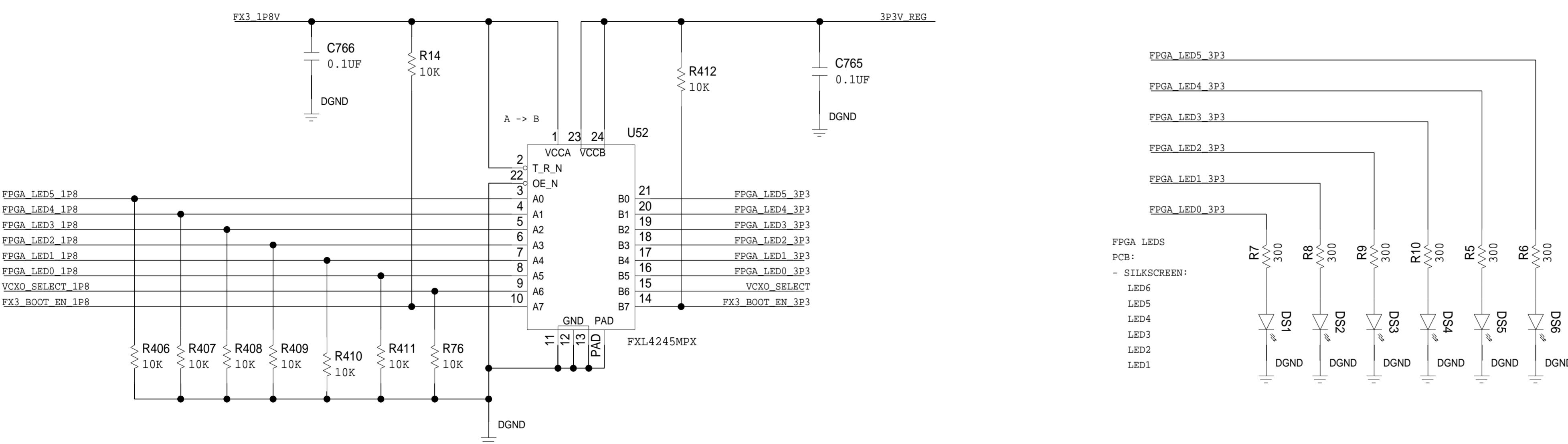
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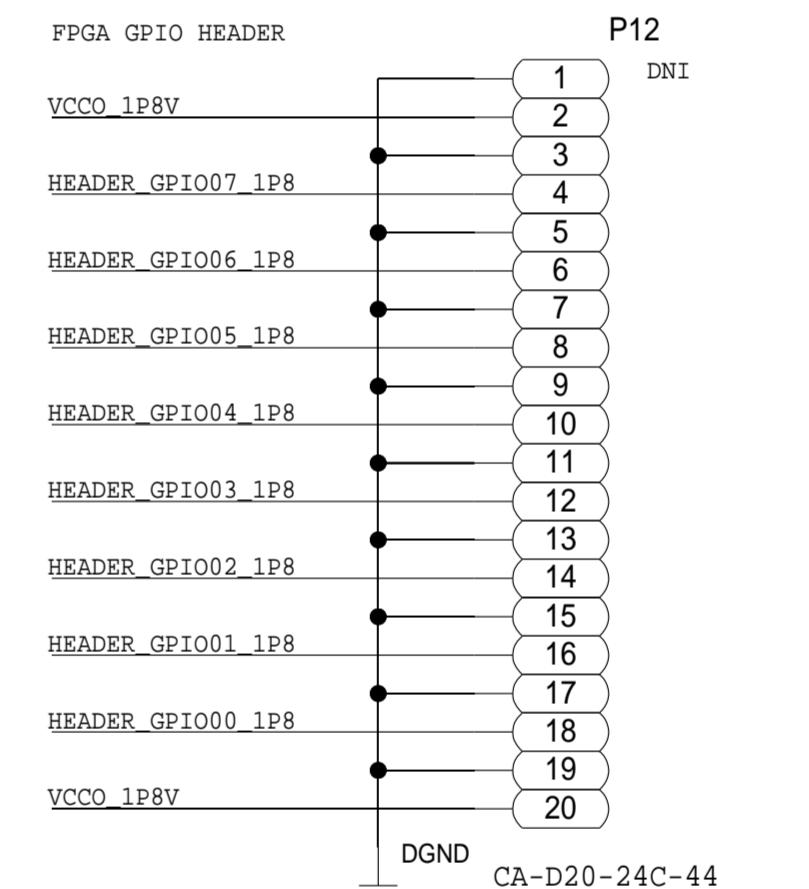
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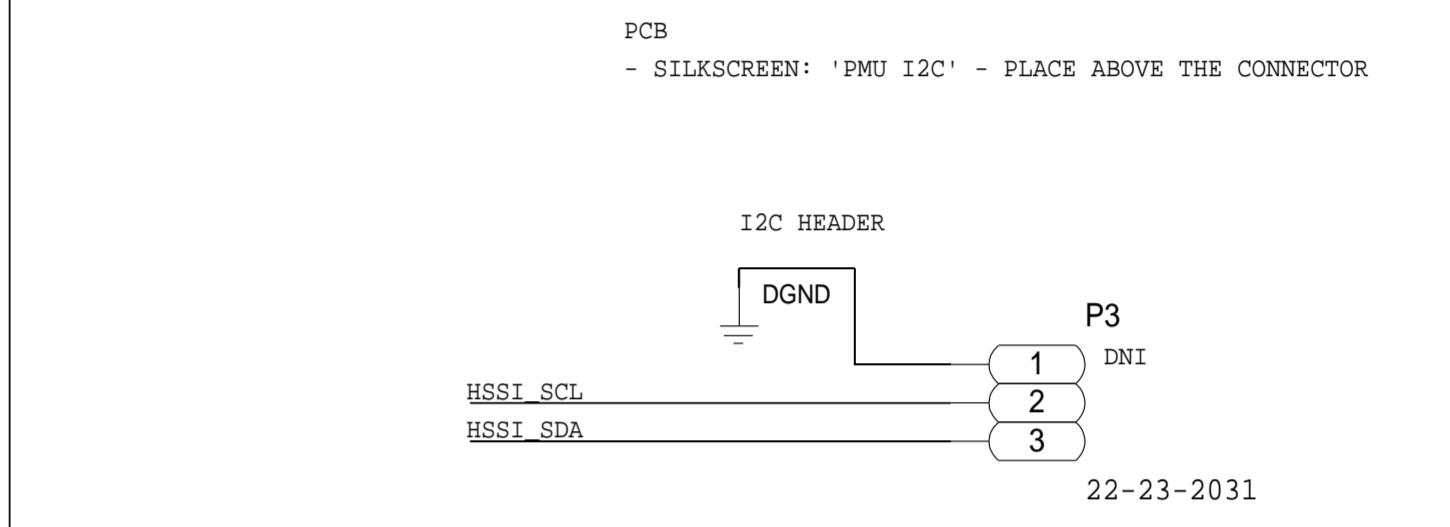
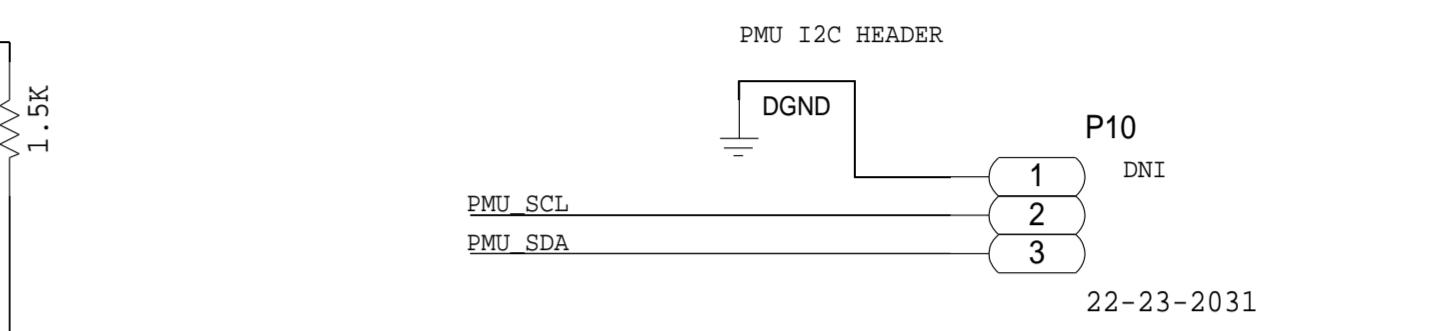
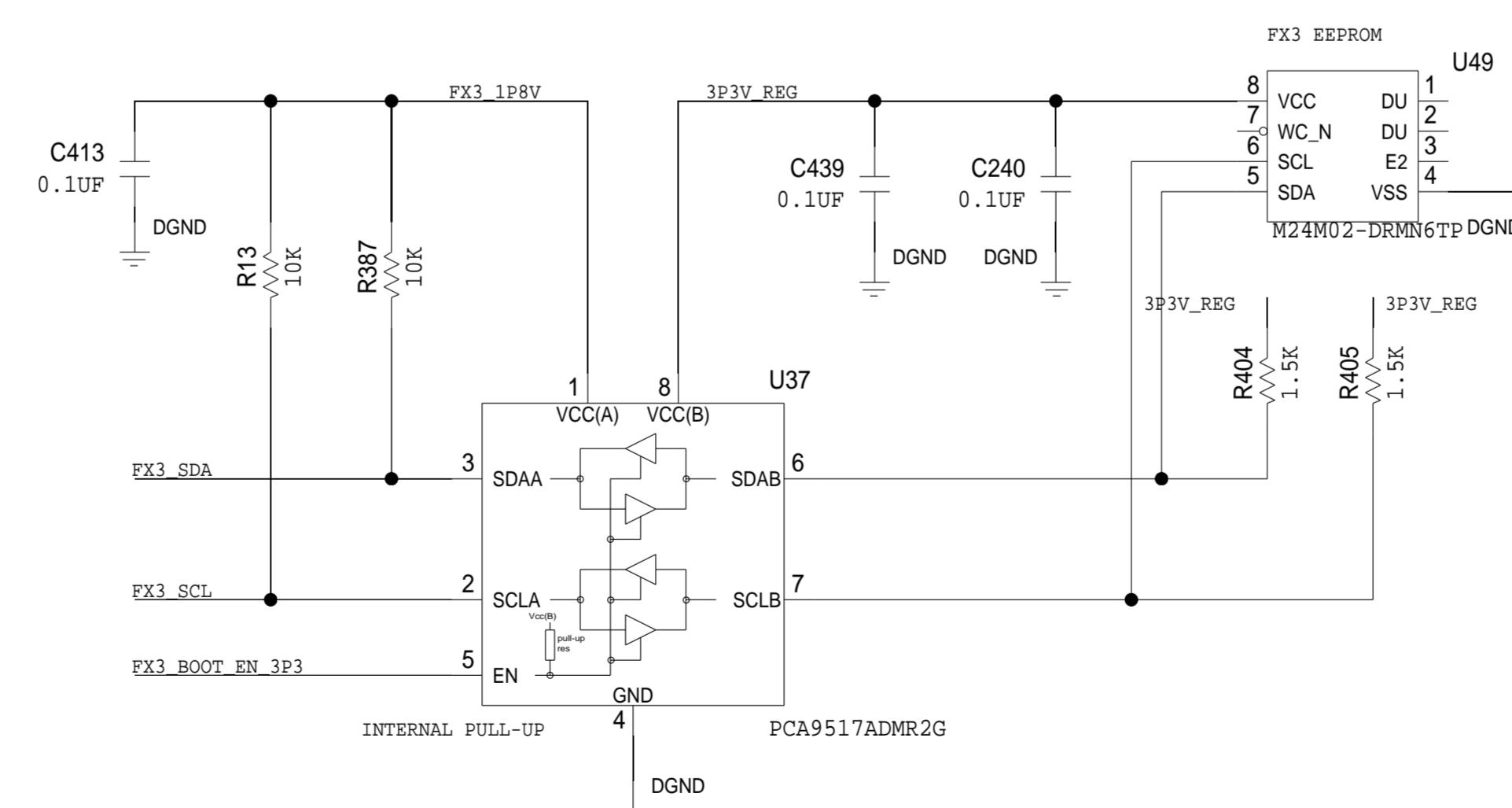
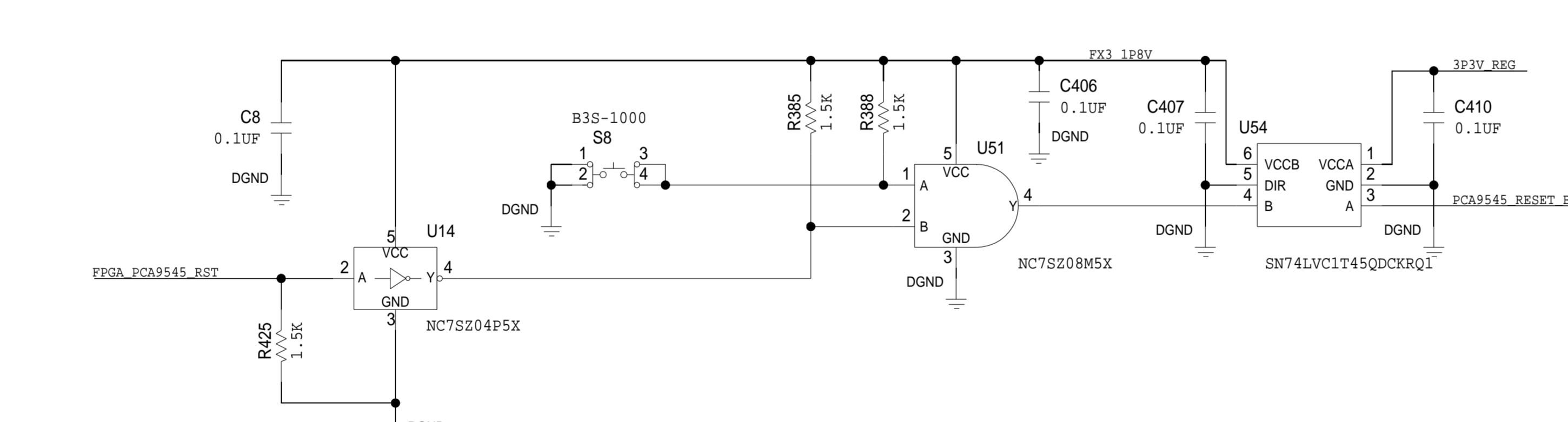
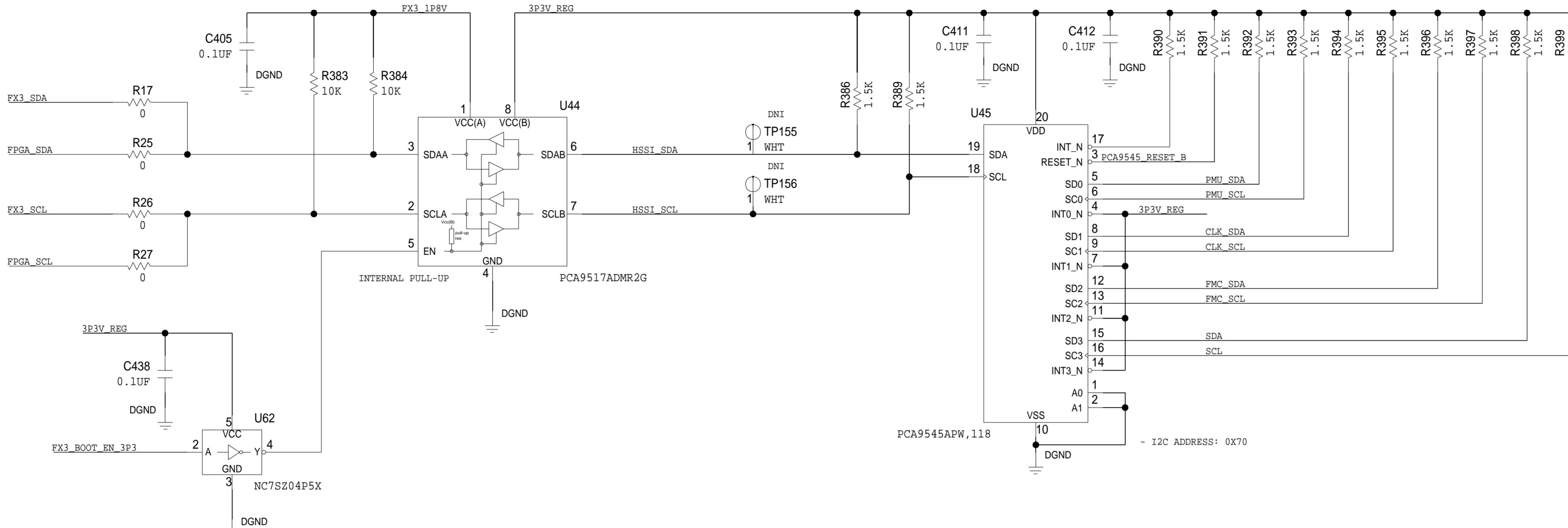
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 ANALOG DEVICES	<h1>SCHEMATIC</h1>		
	HW TYPE : Customer Evaluation Product(s): N/A : N/A		
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	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1
			SHEET 17 OF 52

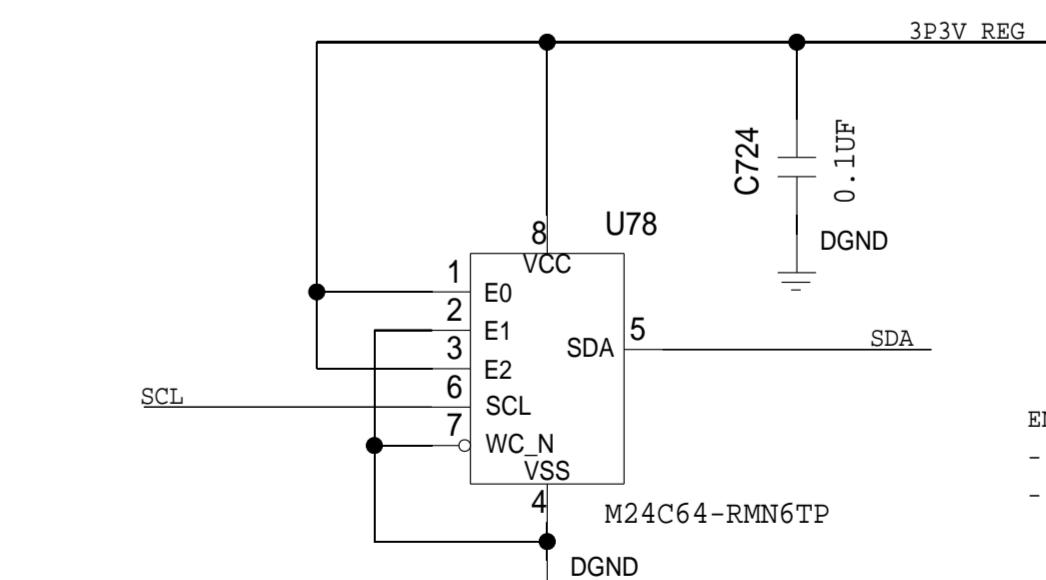
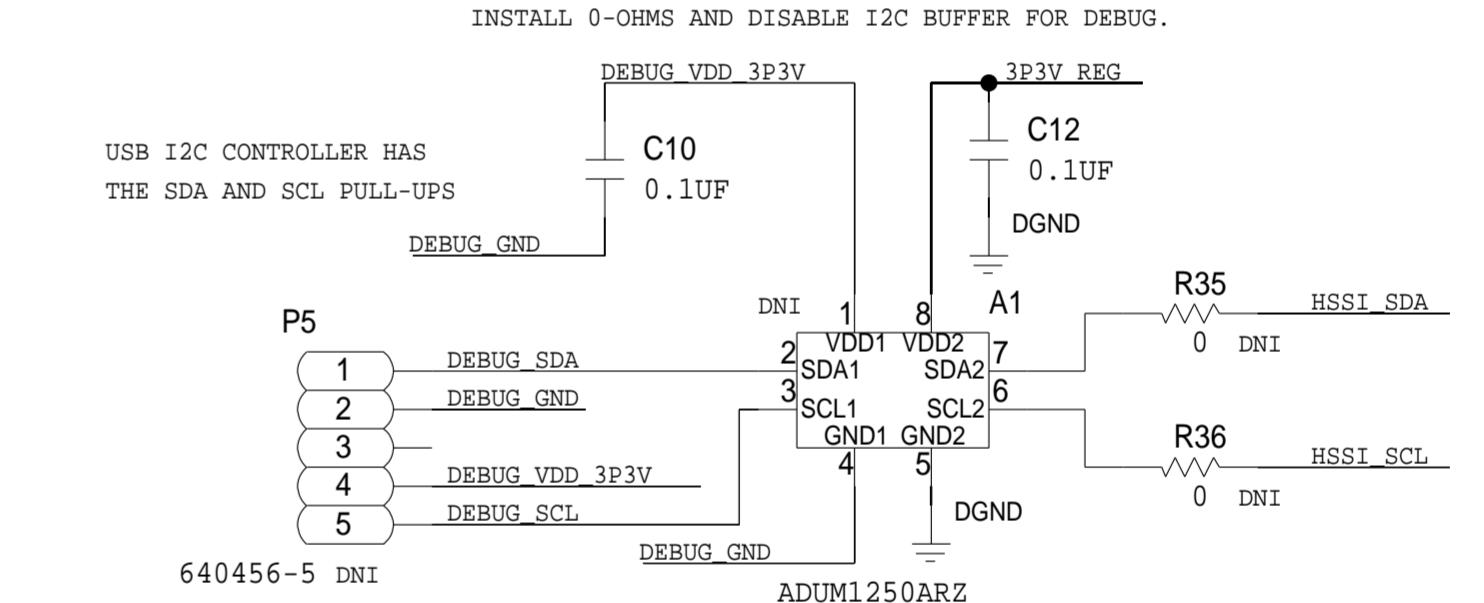
REVISIONS

REV	DESCRIPTION	DATE	APPROVED

I2C INTERFACE



I2C DEBUG INTERFACE



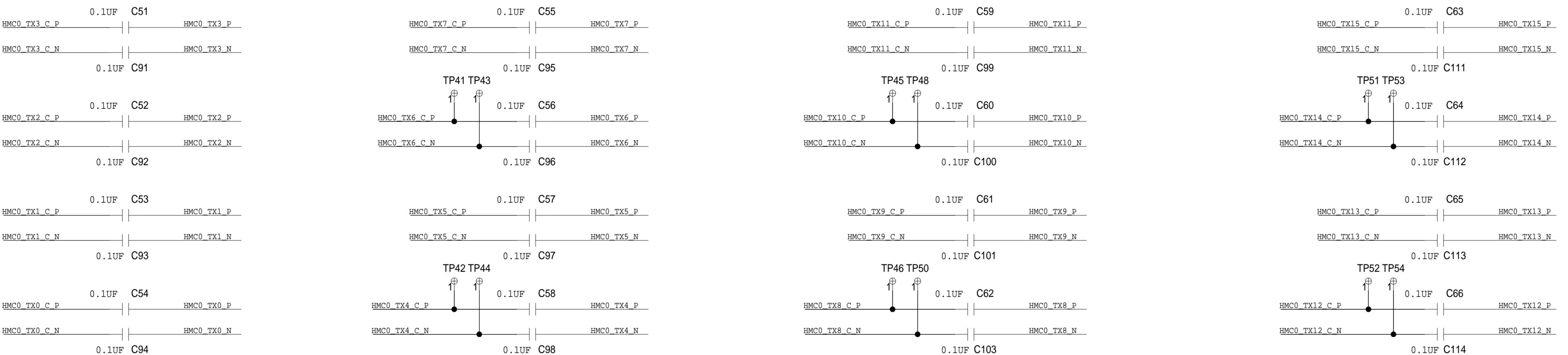
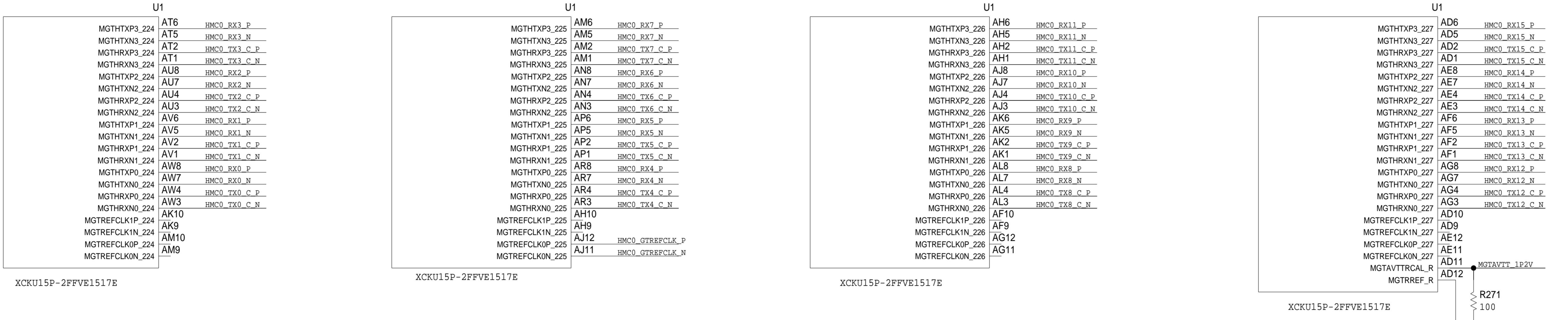
SCHEMATIC	
HW TYPE : Customer Evaluation	REV E
Product(s): N/A	
: N/A	
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DESIGN VIEW <DESIGN_VIEW>	
PTD ENGINEER <PTD_ENGINEER>	SIZE D SCALE 1:1 SHEET 18 OF 52

GTH TRANSCEIVERS HMC0

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

FPGA TX CONNECTS TO HMC RX
HMC TX CONNECTS TO FPGA RX THROUGH CAP



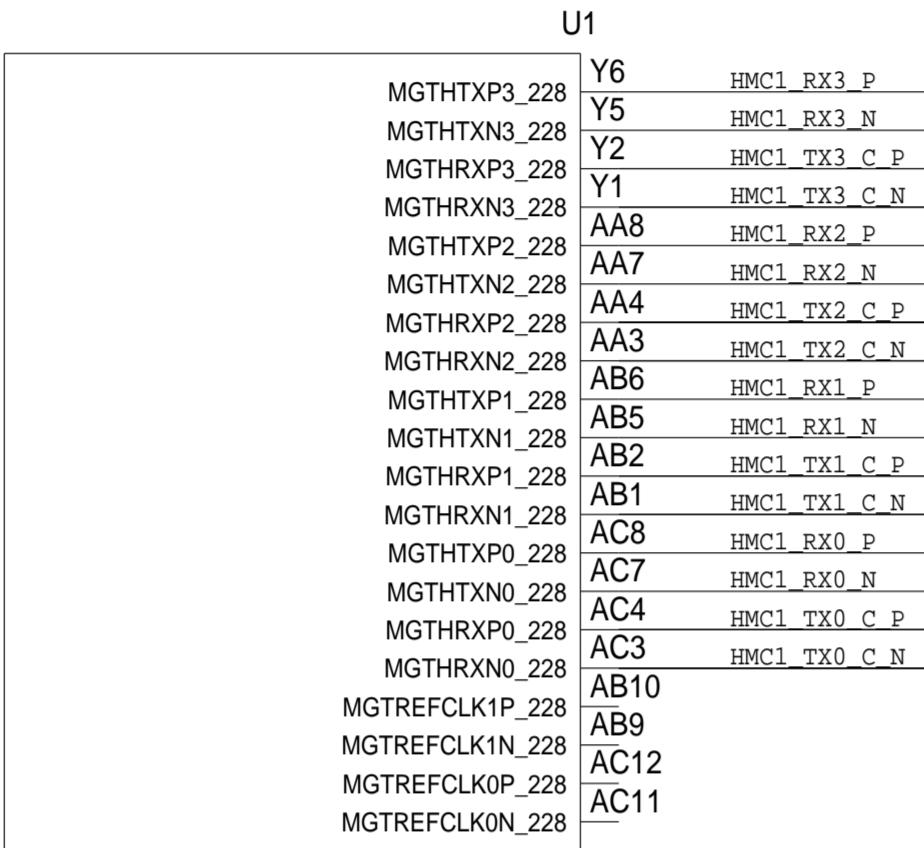
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HW TYPE : Customer Evaluation	Product(s) : N/A	SIZE D	REV E
IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED FOR FURNISHING INFORMATION TO OTHERS, EXCEPT AS AUTHORIZED BY WRITTEN AGREEMENT OF ANALOG DEVICES.			
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PTD ENGINEER	<PTD_ENGINEER>	SCALE 1:1	SHEET 19 OF 52

REVISIONS

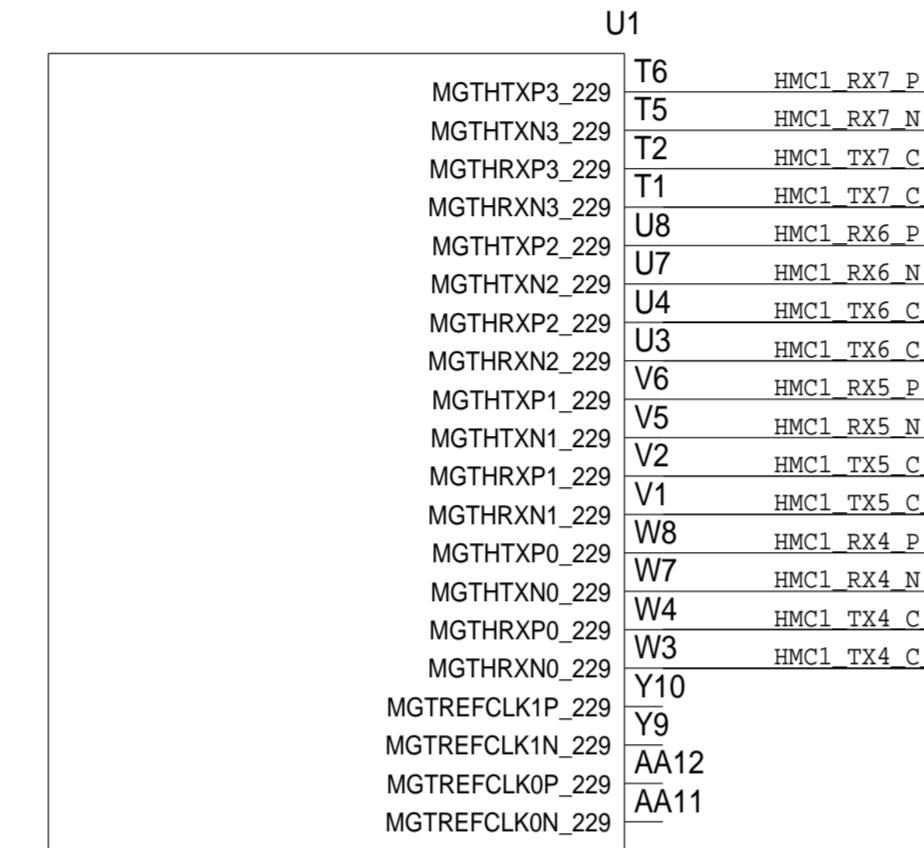
REV	DESCRIPTION	DATE	APPROVED

GTH TRANSCEIVERS HMC1

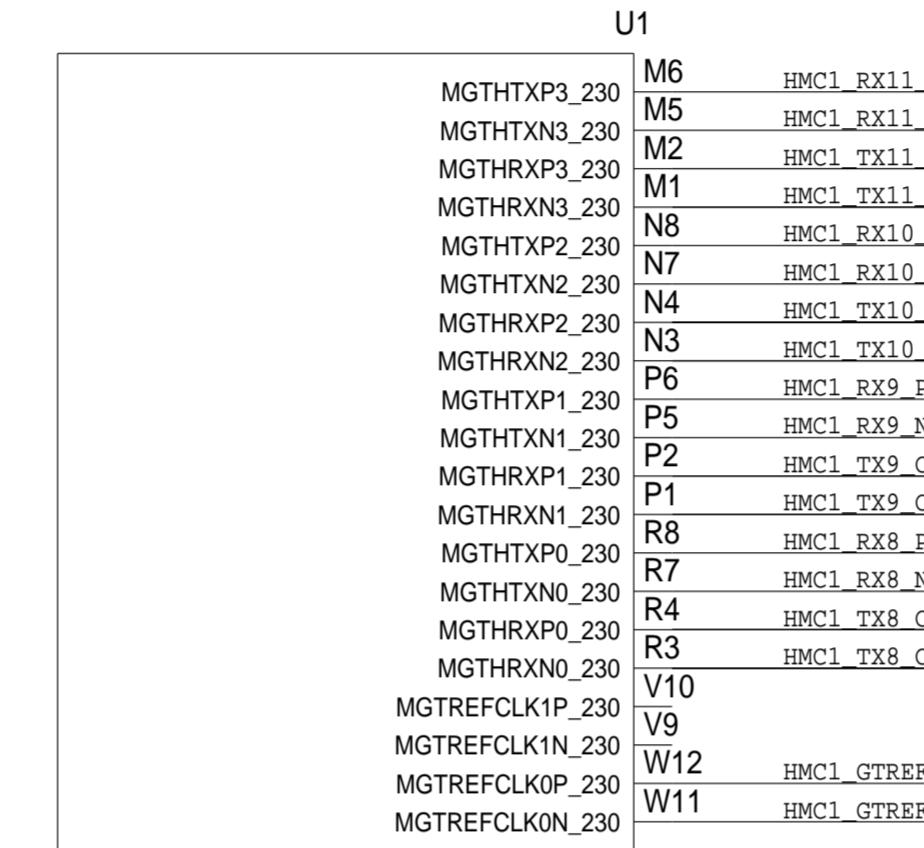
FPGA TX CONNECTS TO HMC RX
HMC TX CONNECTS TO FPGA RX THROUGH CAP



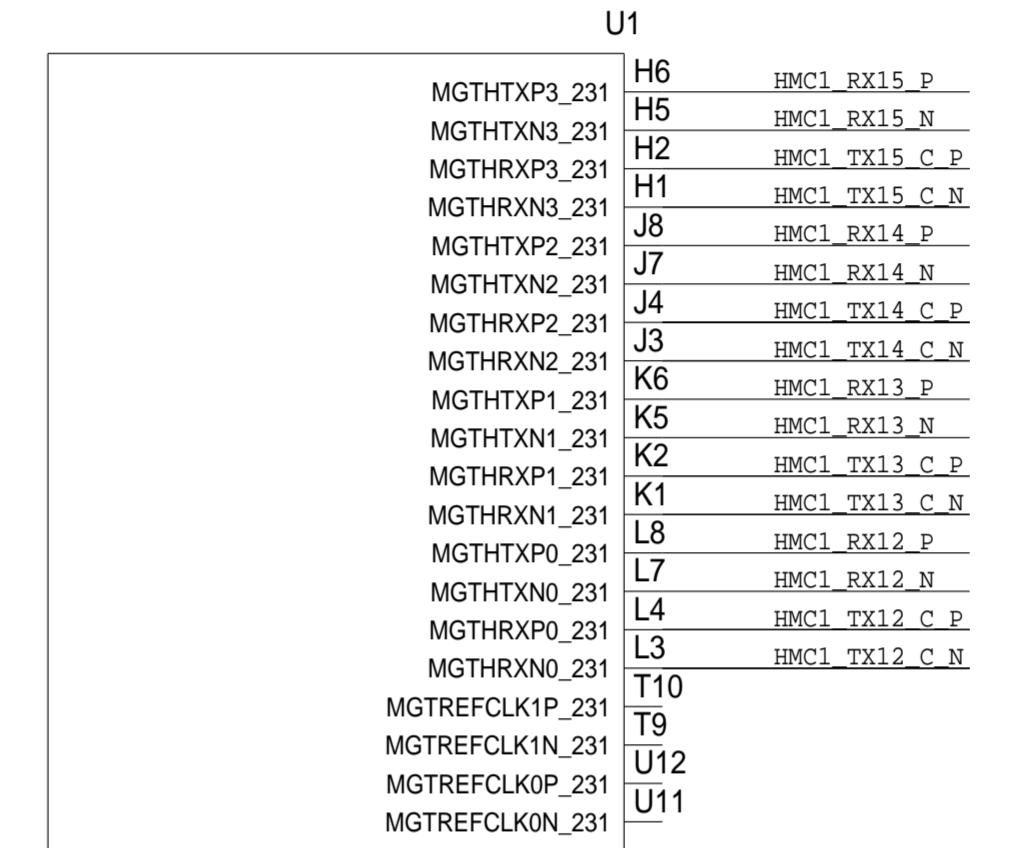
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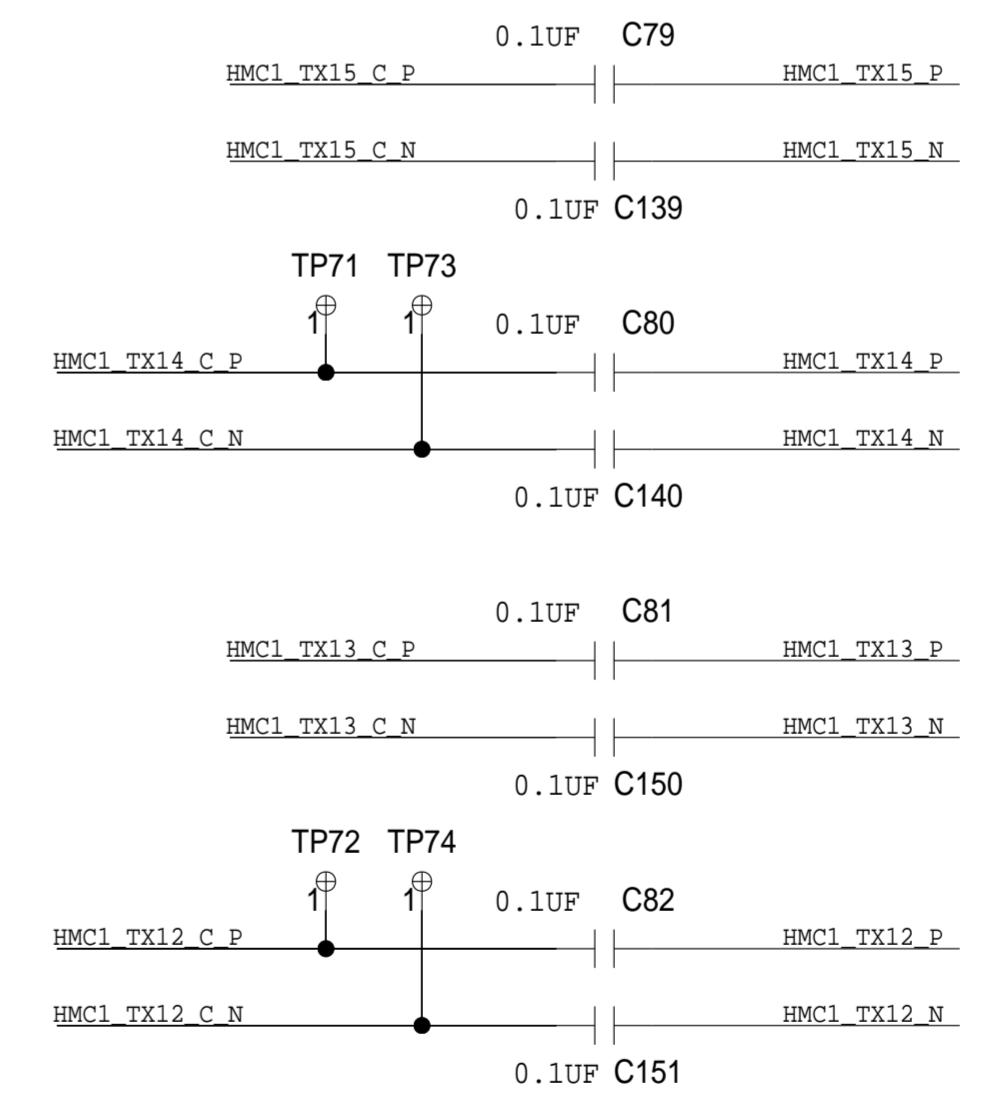
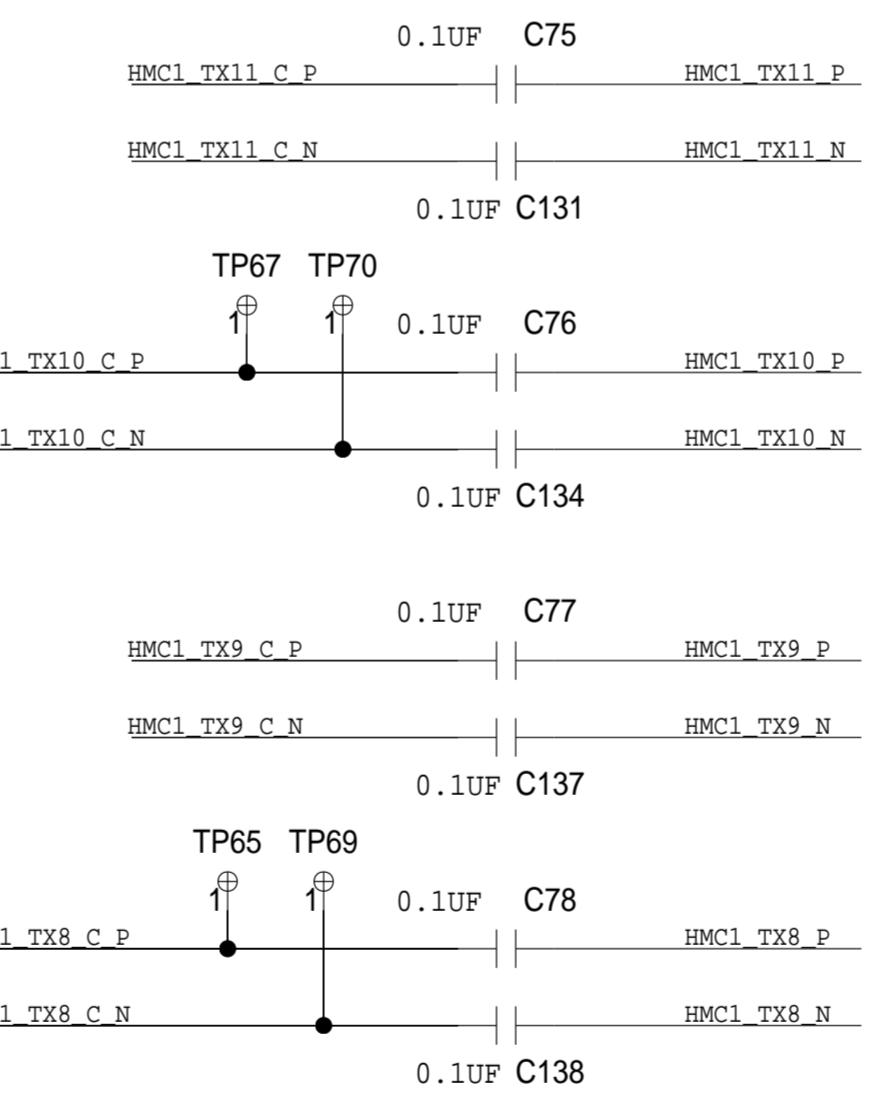
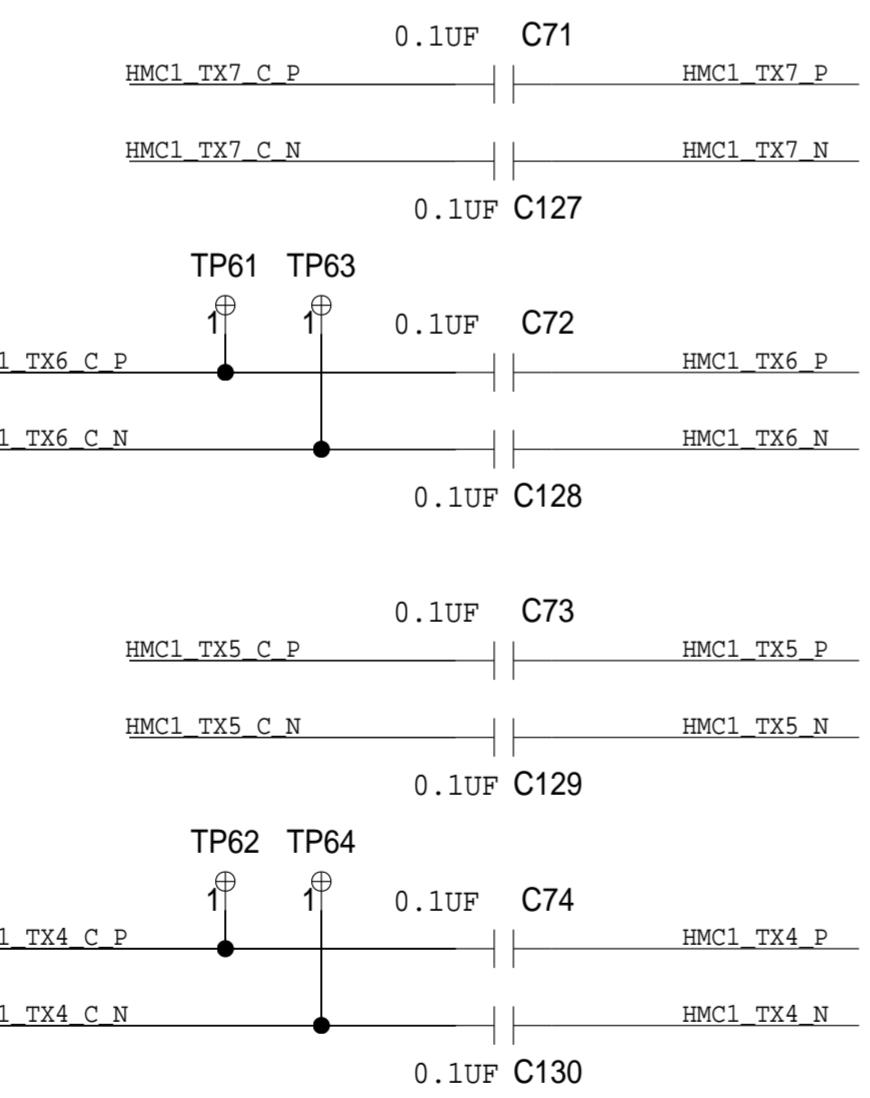
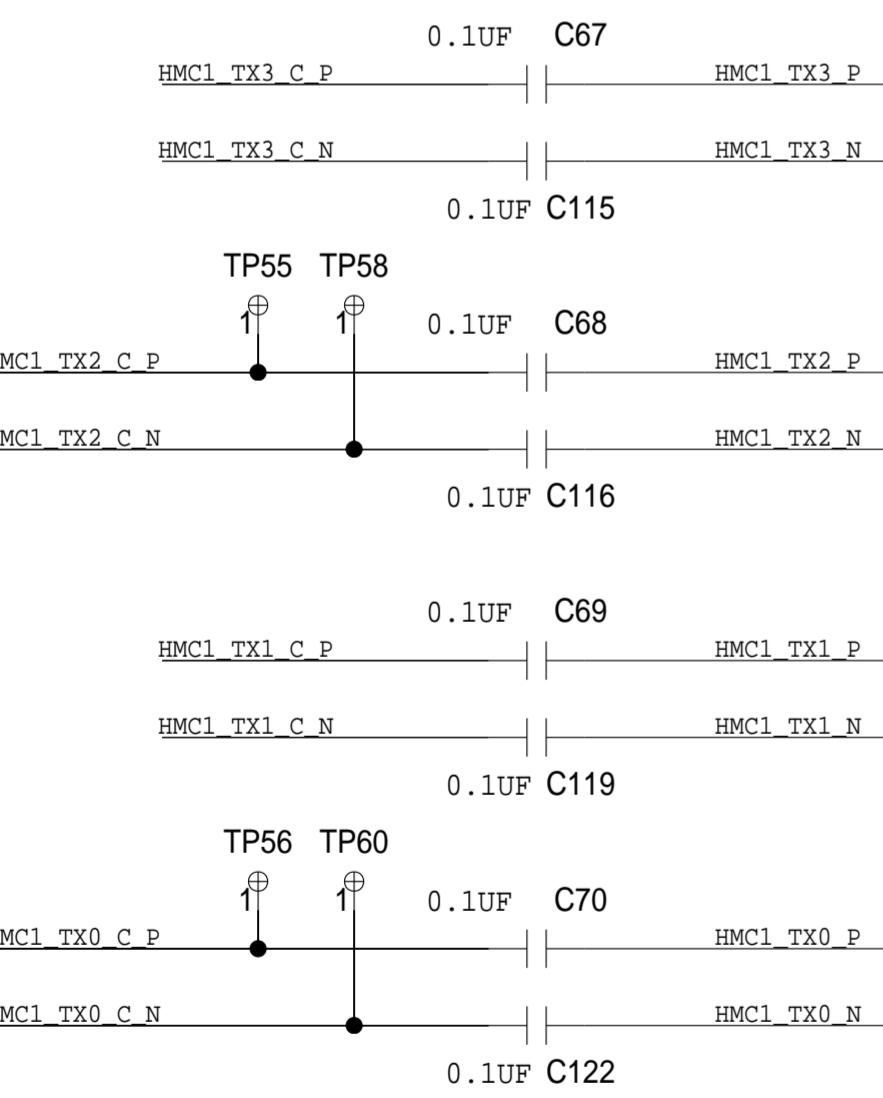
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XCKU15P-2FFVE1517E



XCKU15P-2FFVE1517E



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HW TYPE : Customer Evaluation
Product(s) : N/A
: N/A

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DRAWING NO.
02_045361

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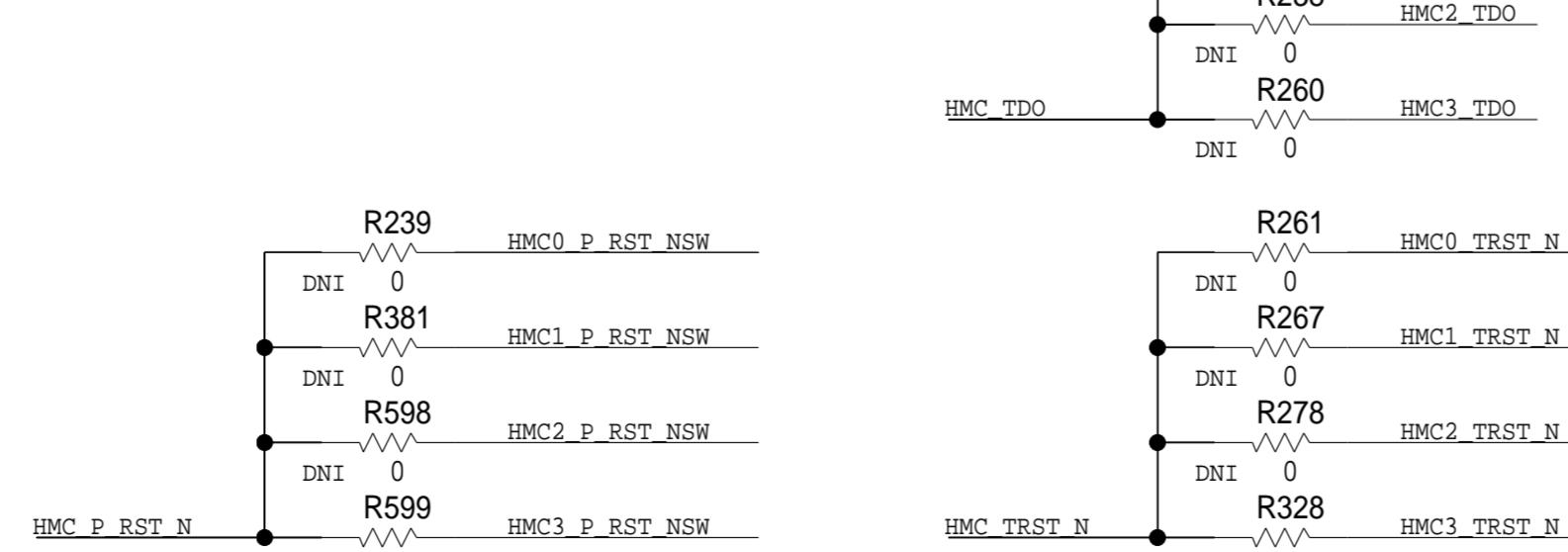
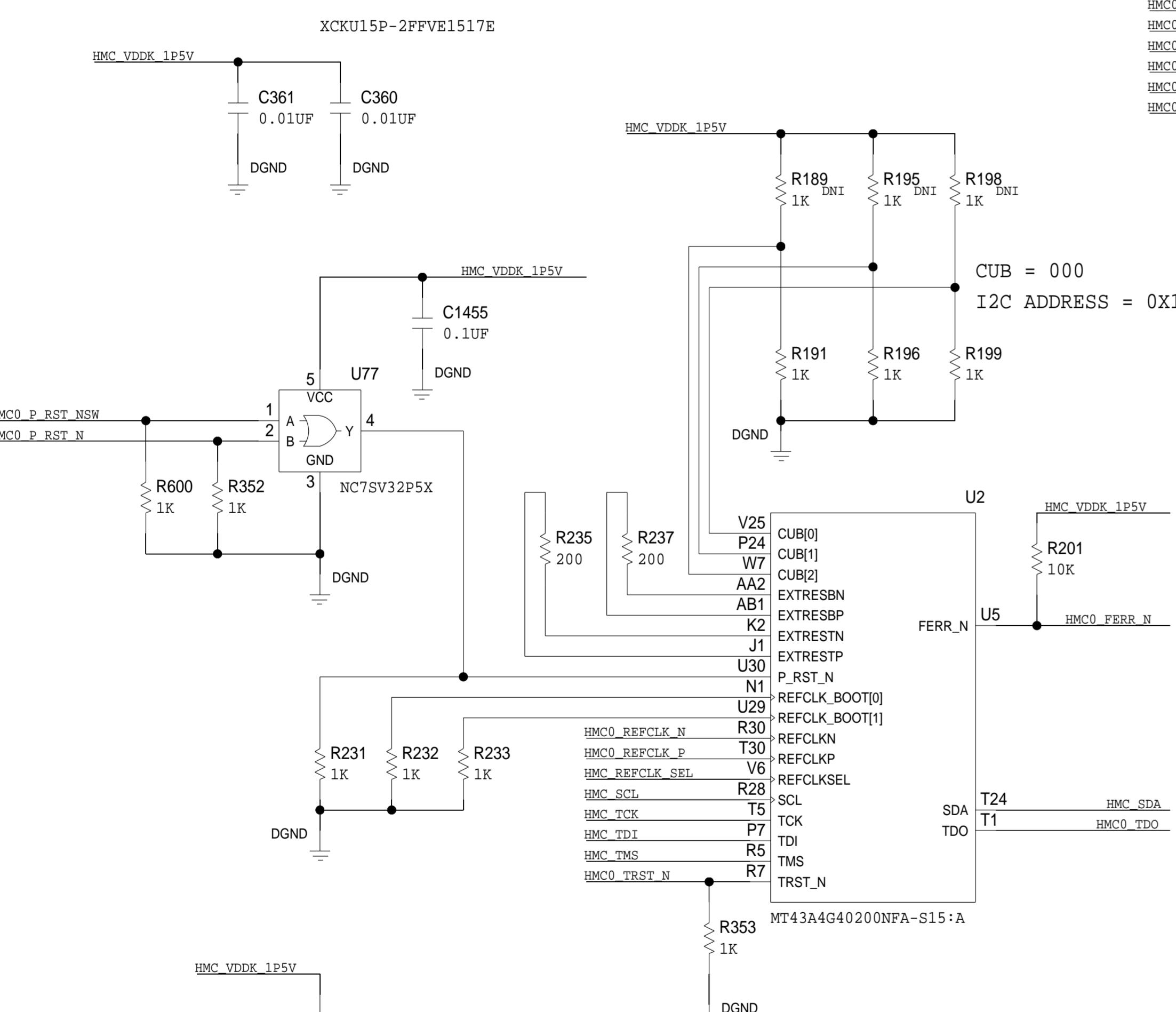
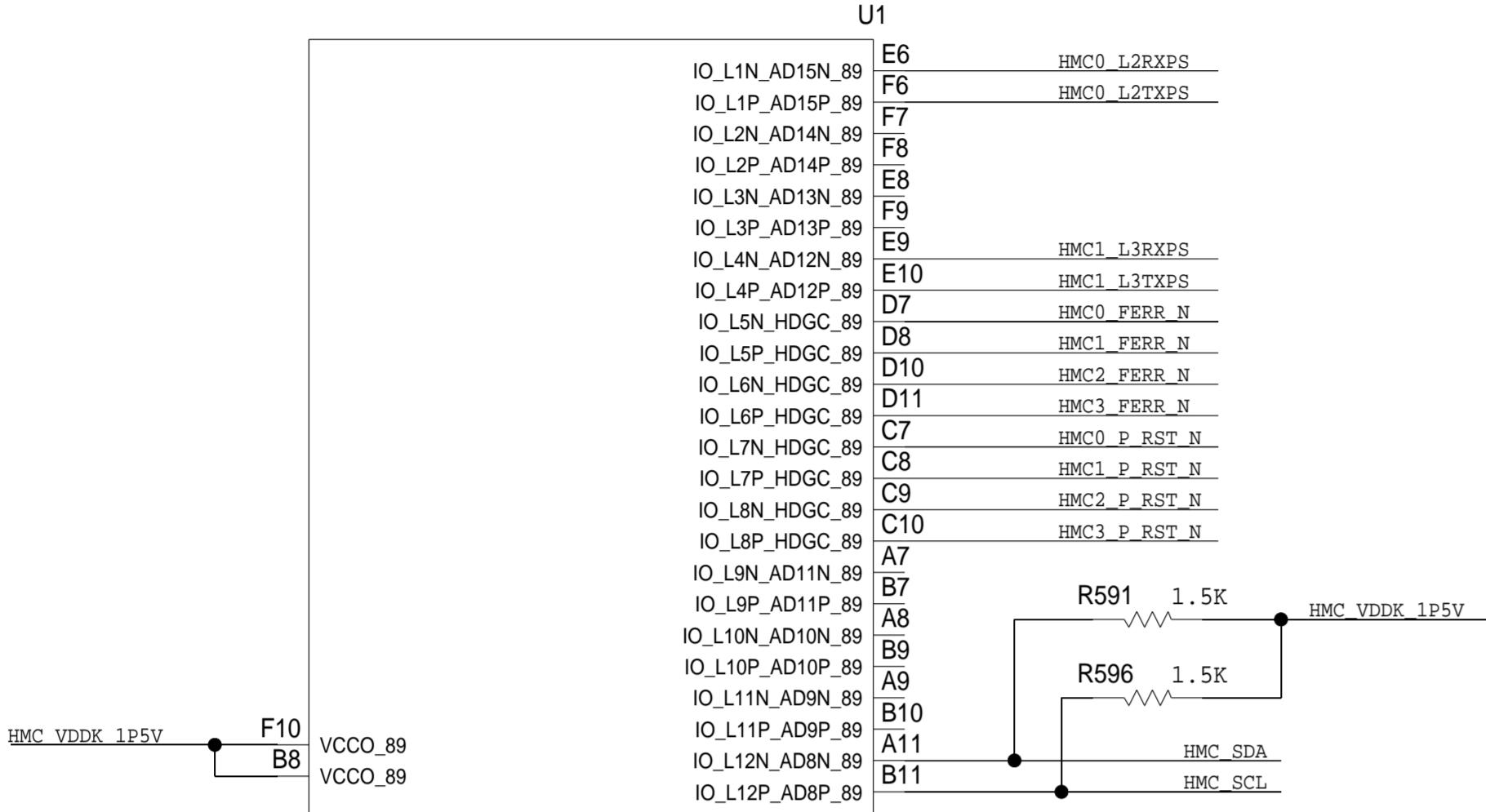
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SIZE
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1:1
SHEET 20 OF 52

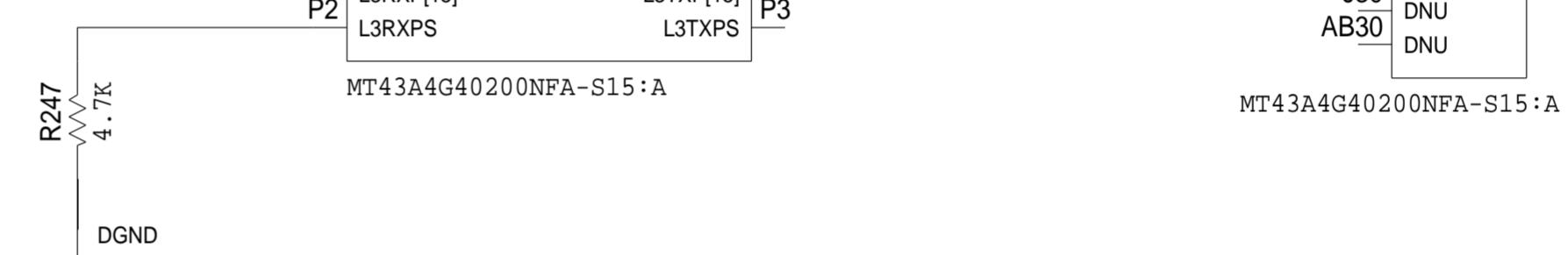
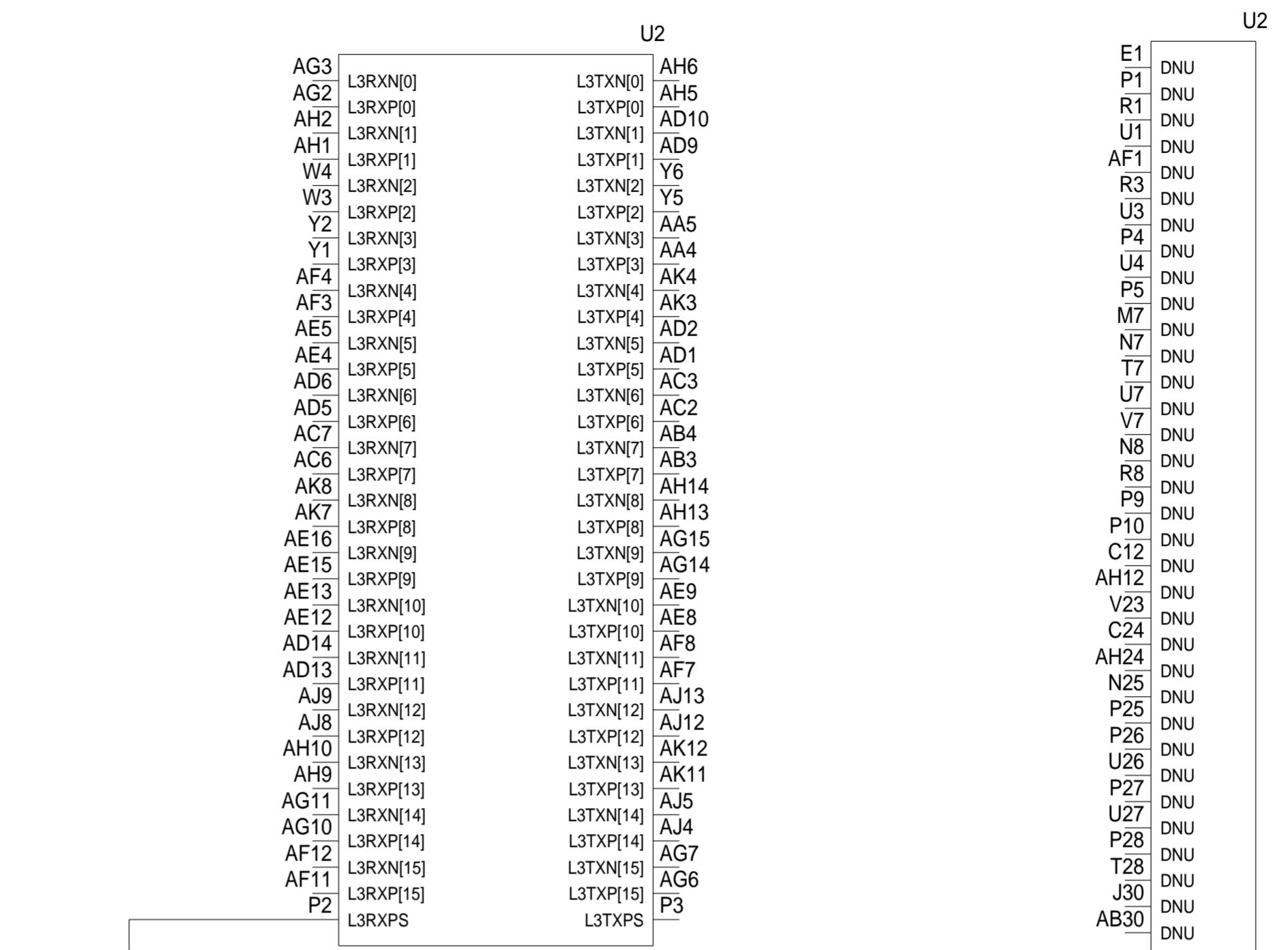
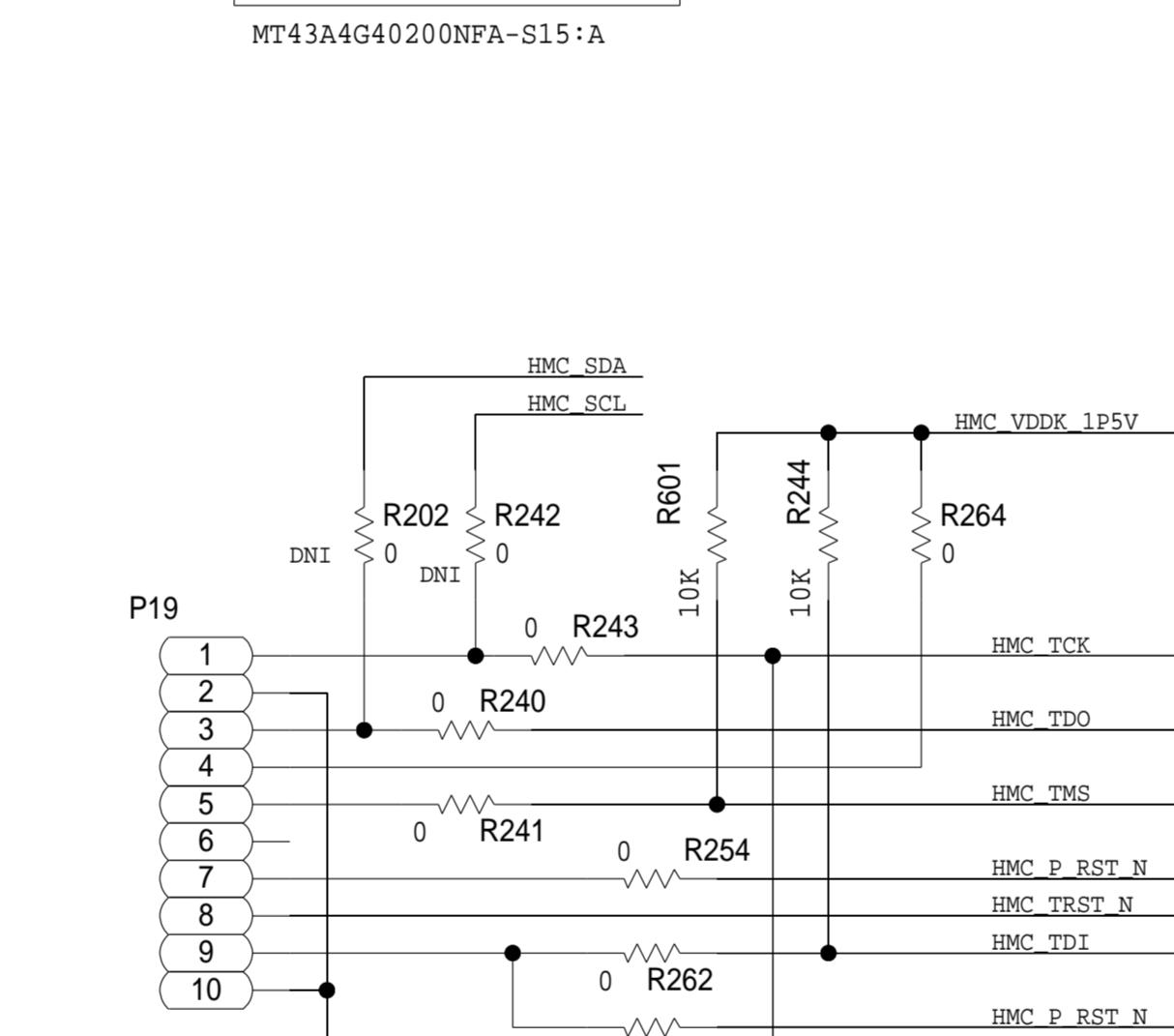
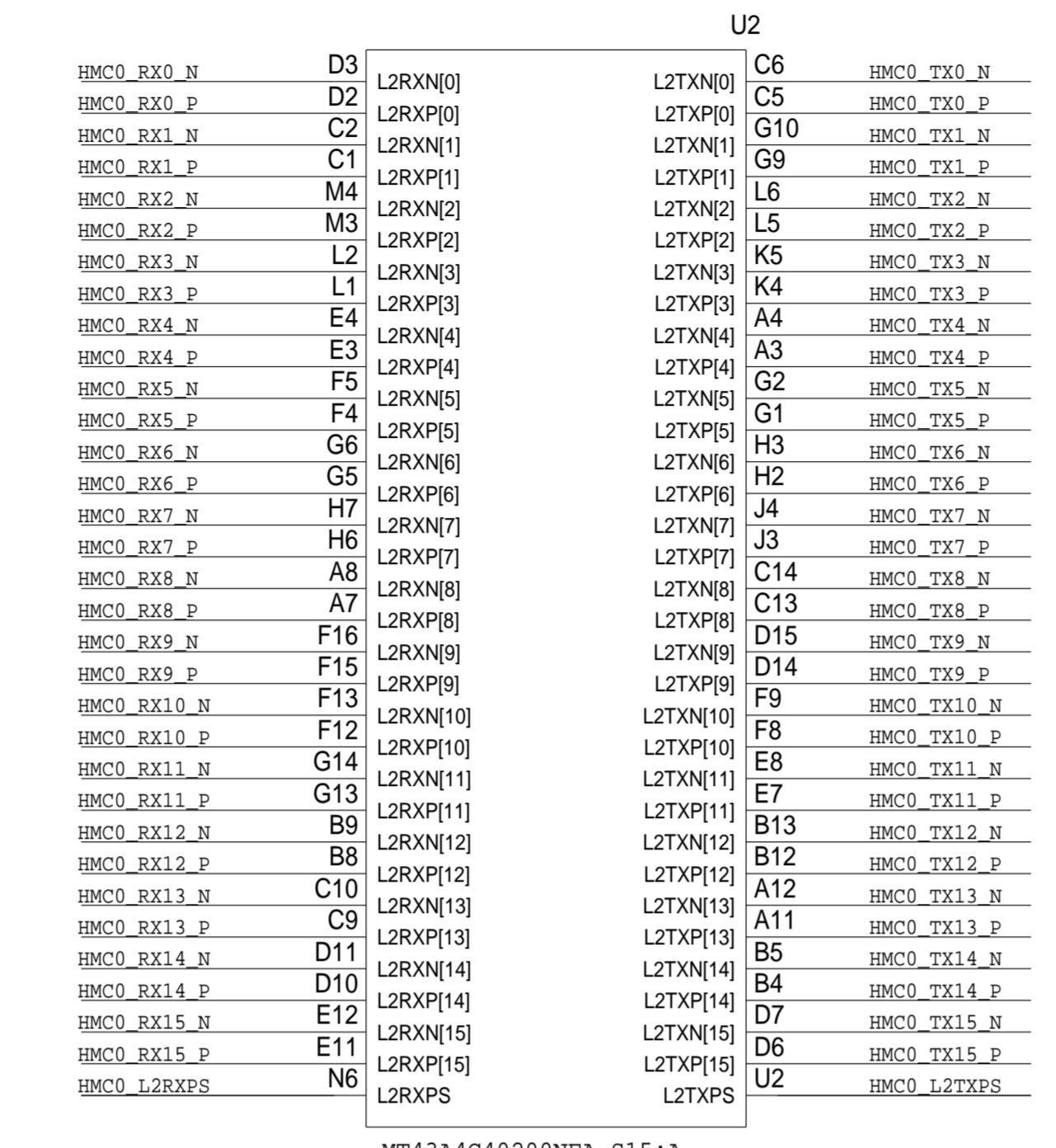
HMC0 DATA AND CONTROL

HMC LOW SPEED BANK

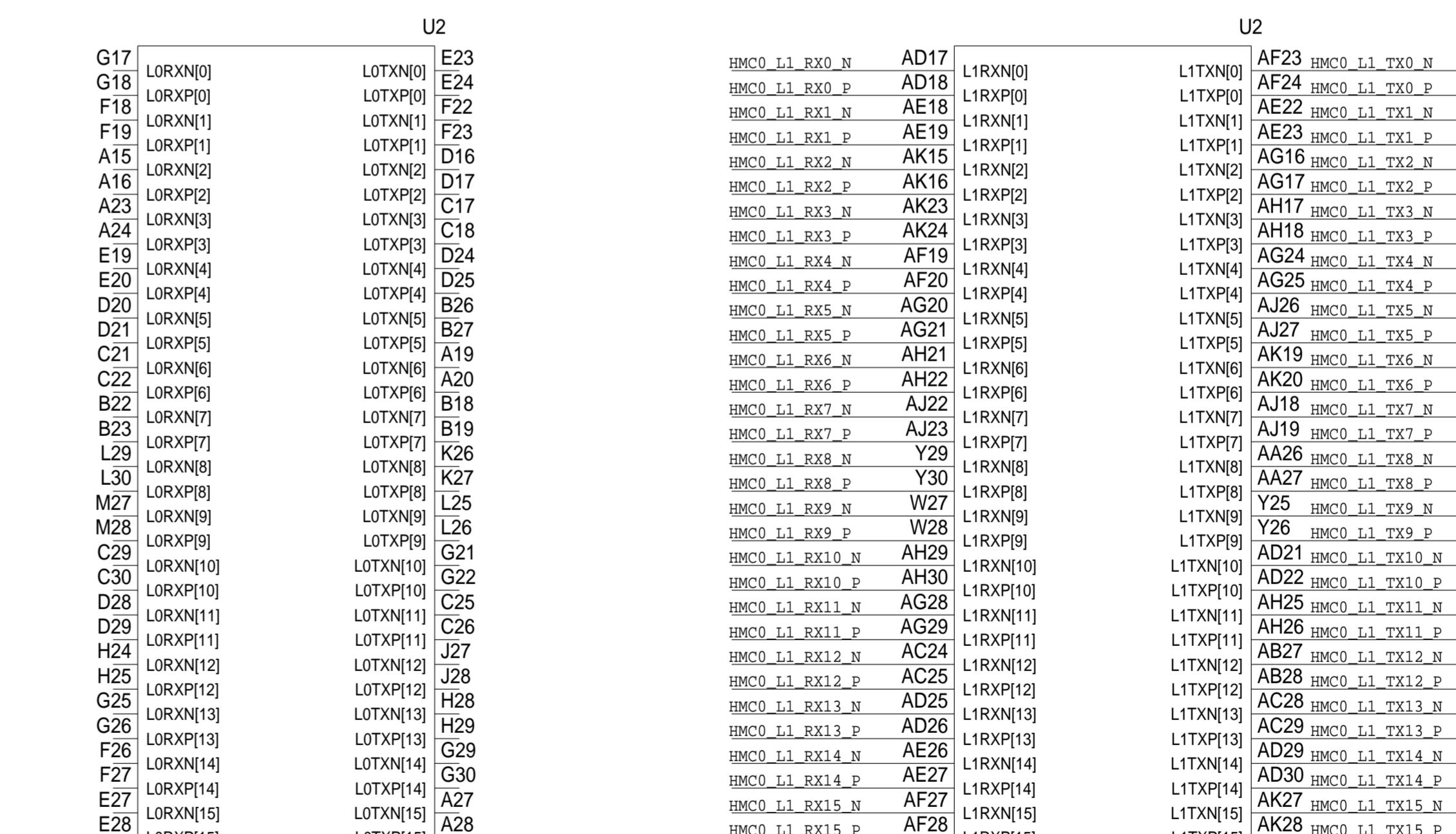
BANK 89 HD



FPGA LINK



CHAIN TO HMC2

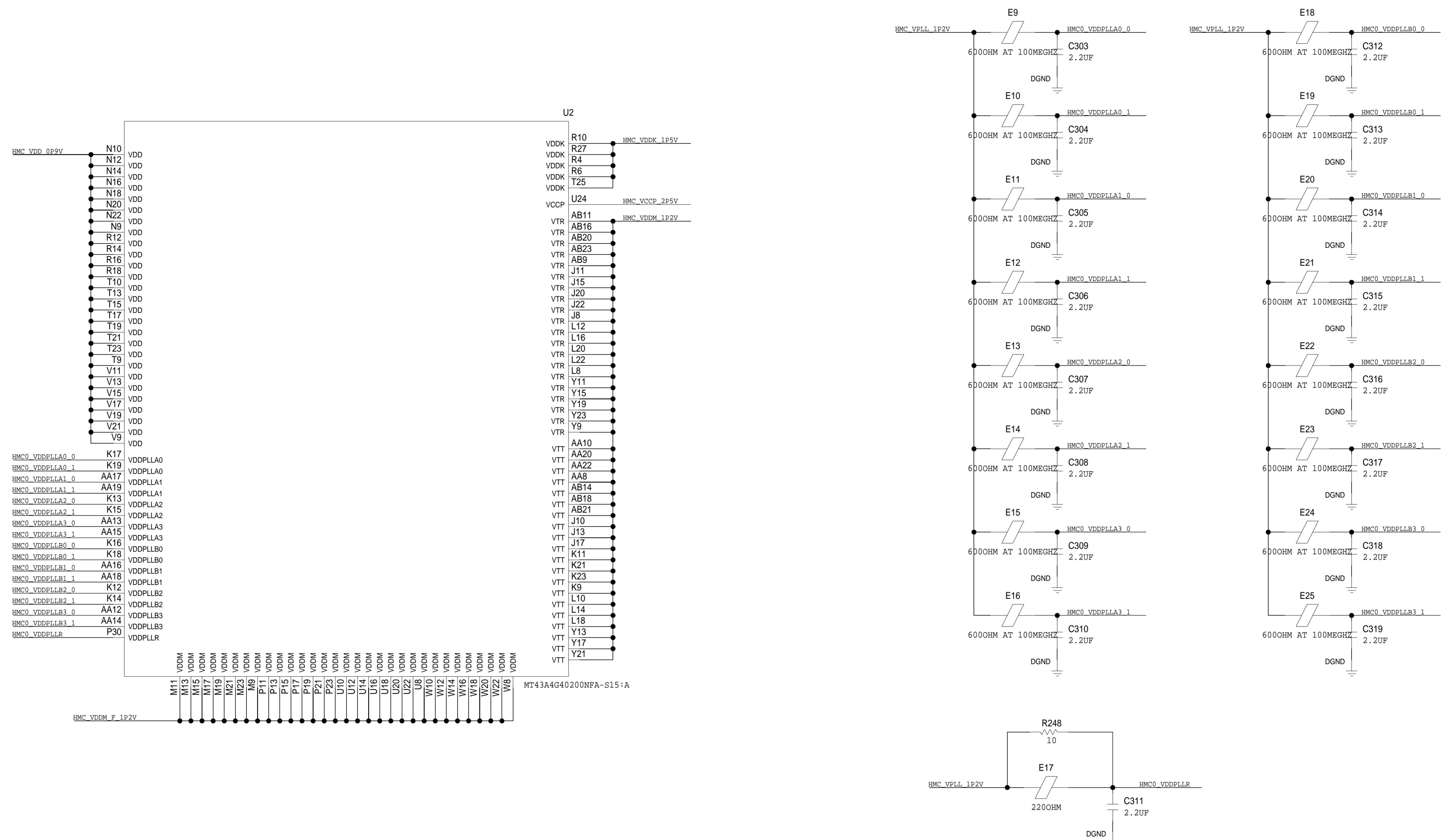


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S INC. OR OTHERS, INTERESTS	<p>DESIGN VIEW <DESIGN_VIEW></p>
BY PATENTS	<p>PTD ENGINEER <PTD_ENGINEER></p>

HMC0 POWER

REVISIONS		
	DESCRIPTION	DATE



SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): N/A
 : N/A

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	DRAWING NO. 02_045361	
SIZE		SCALE 1:1

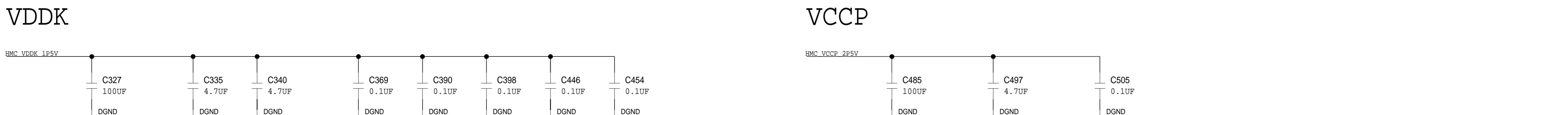
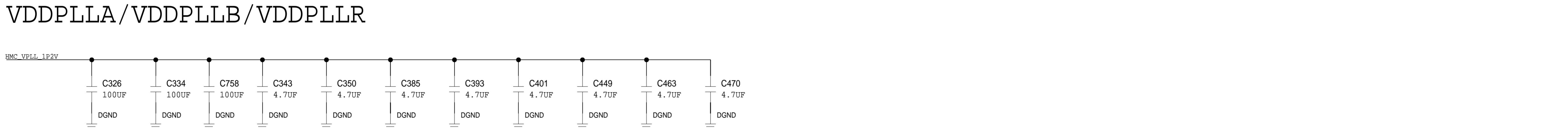
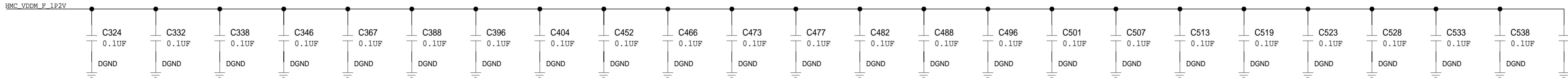
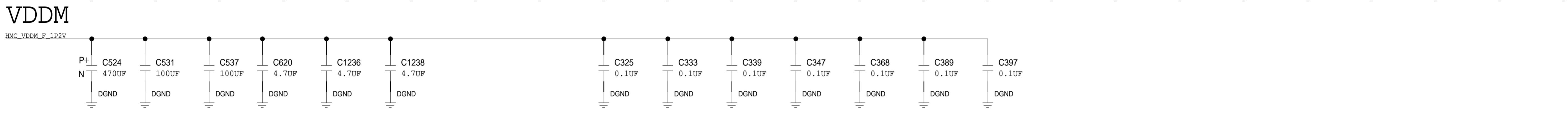
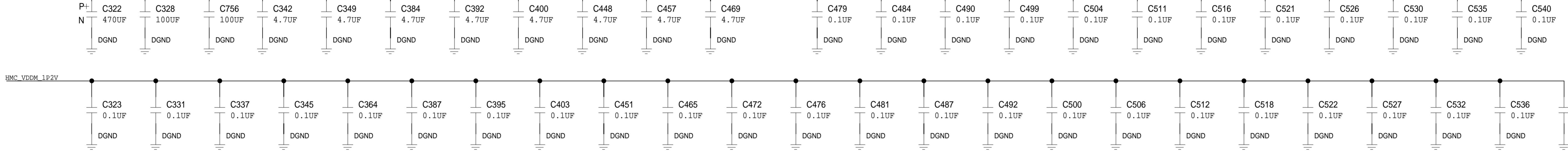
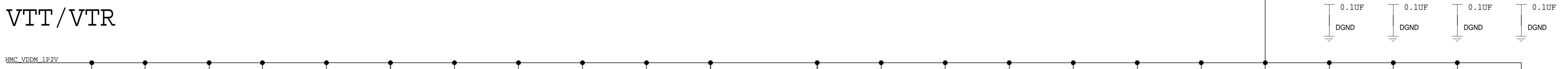
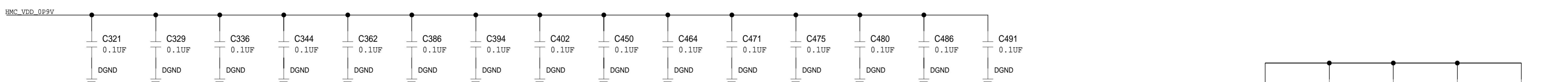
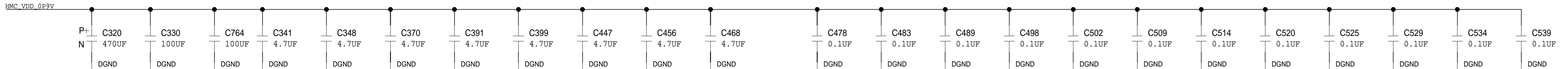
HEET 22 OF 52

REV	DESCRIPTION	DATE	APPROVED

HMC0 DECOUPLING

VDD

PLACE ALL CAPS AS CLOSE TO HMC0 PINS AS POSSIBLE



SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s): N/A
 : N/A

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DRAWING NO.
 02_045361

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SIZE
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 SHEET
 23 OF 52

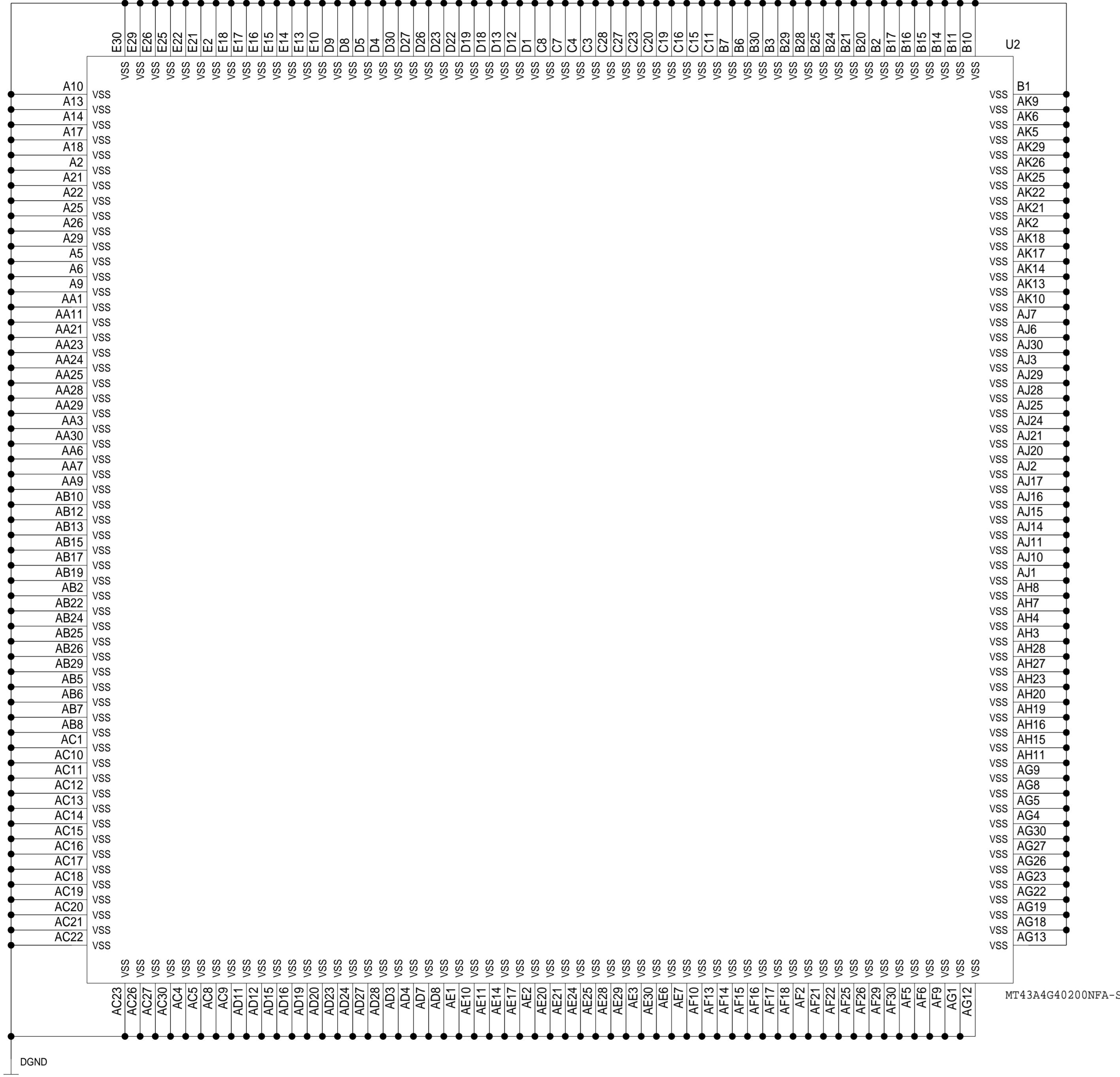
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REVISIONS

REV	DESCRIPTION	DATE	APPROVED

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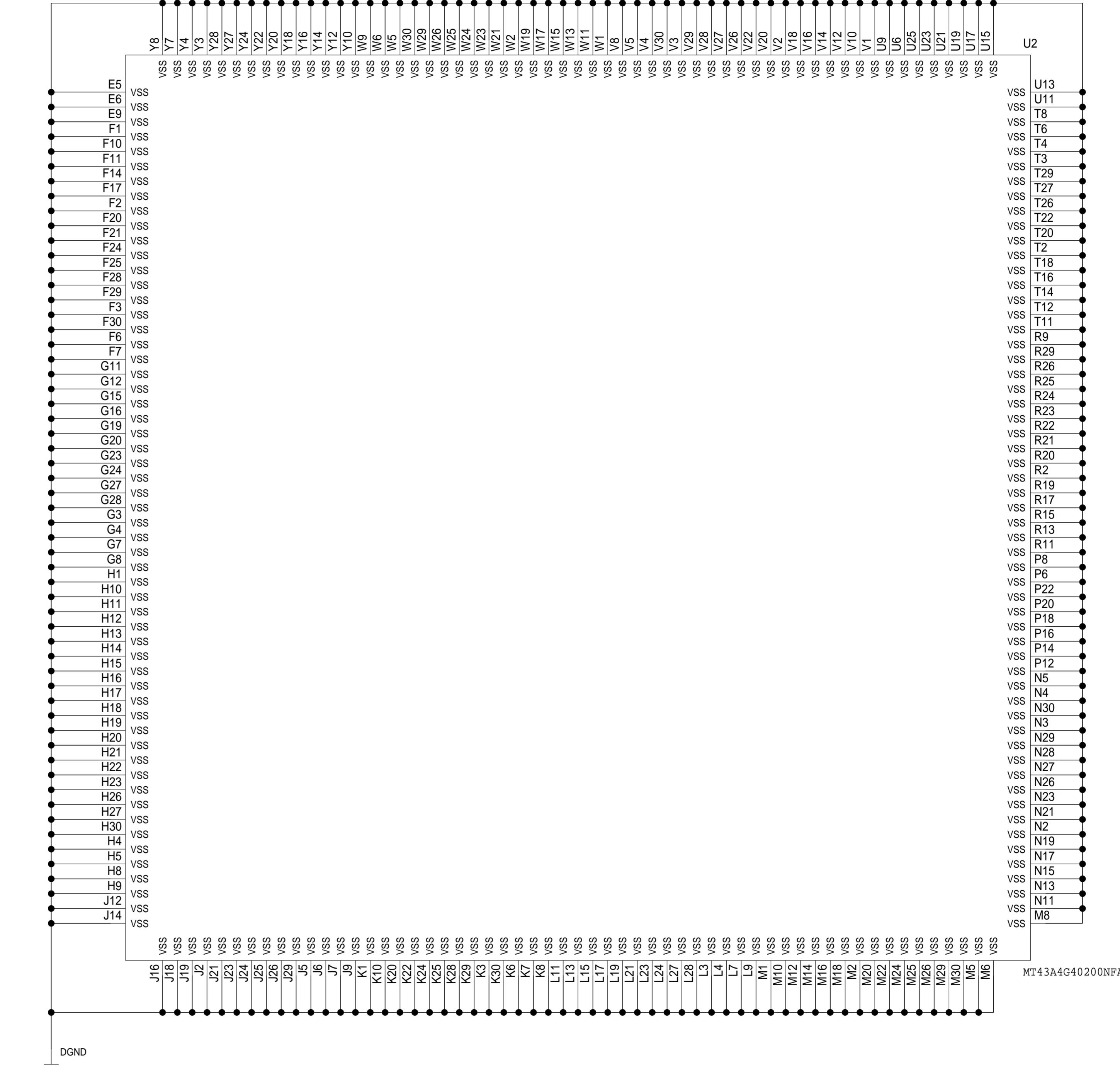
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D

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SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): N/A
: N/A

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PTD ENGINEER
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DRAWING NO.
02_045361
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SHEET
24 OF 52

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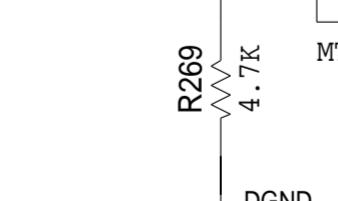
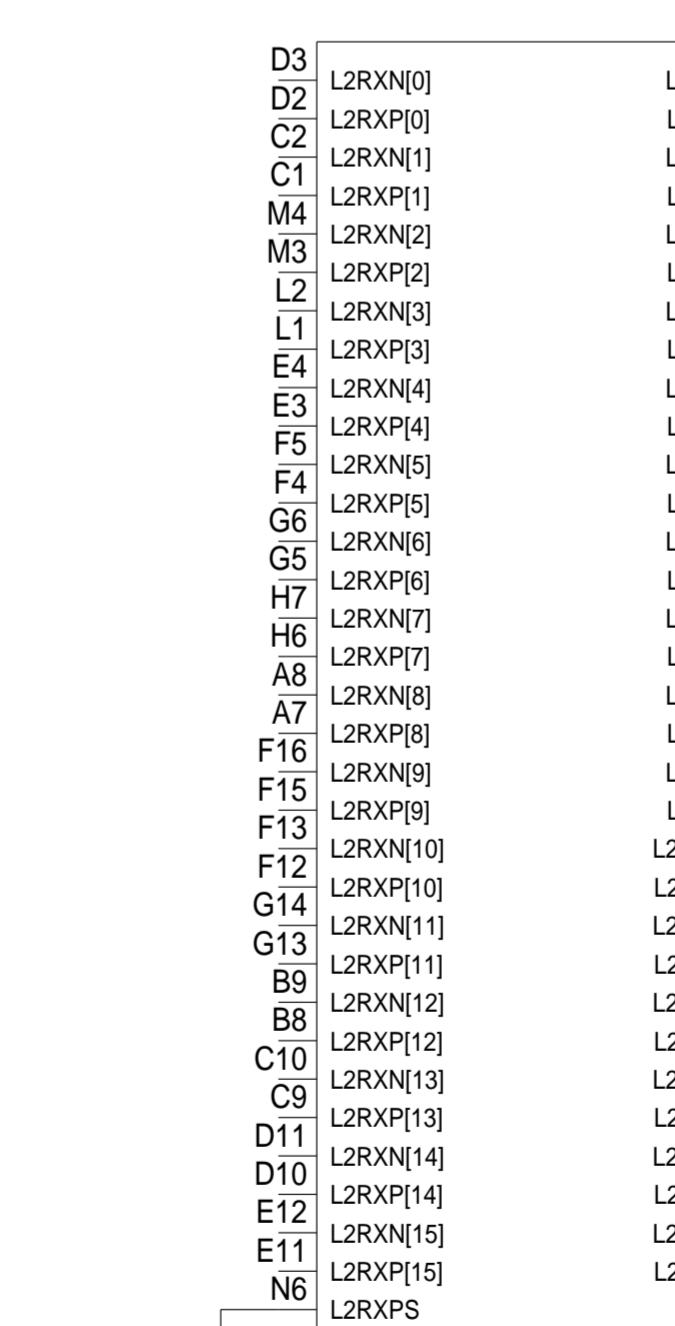
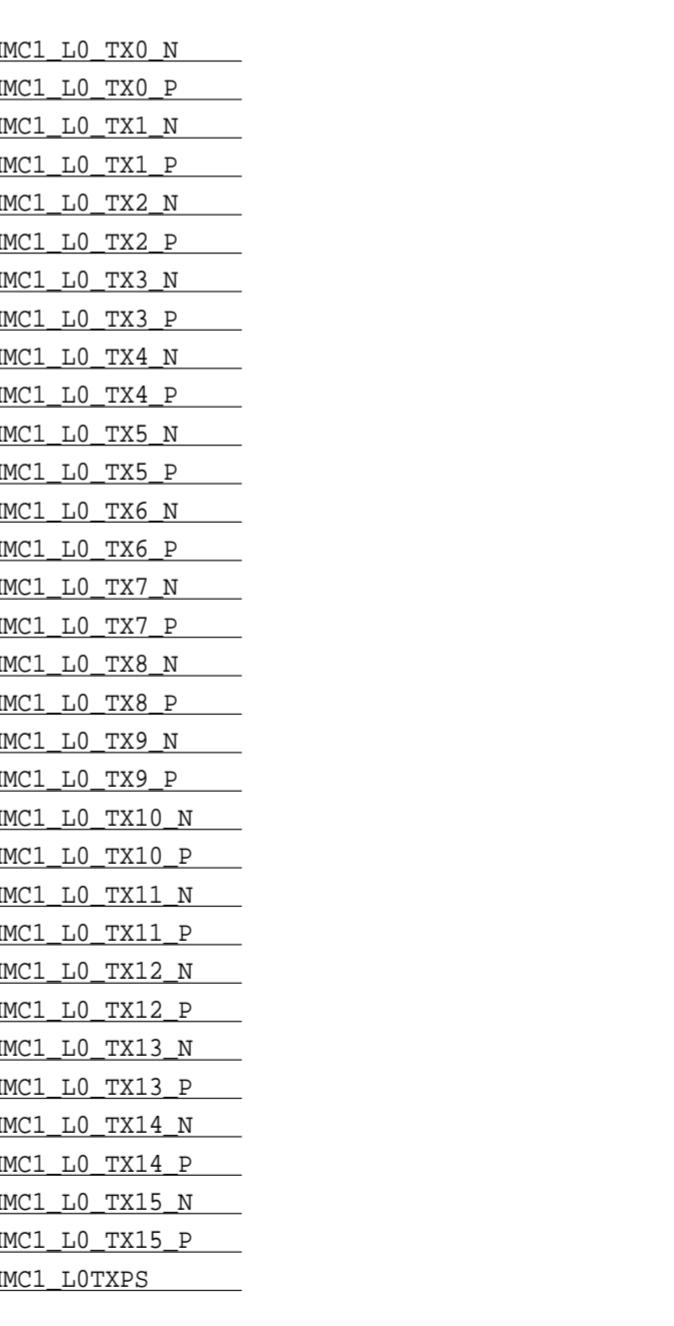
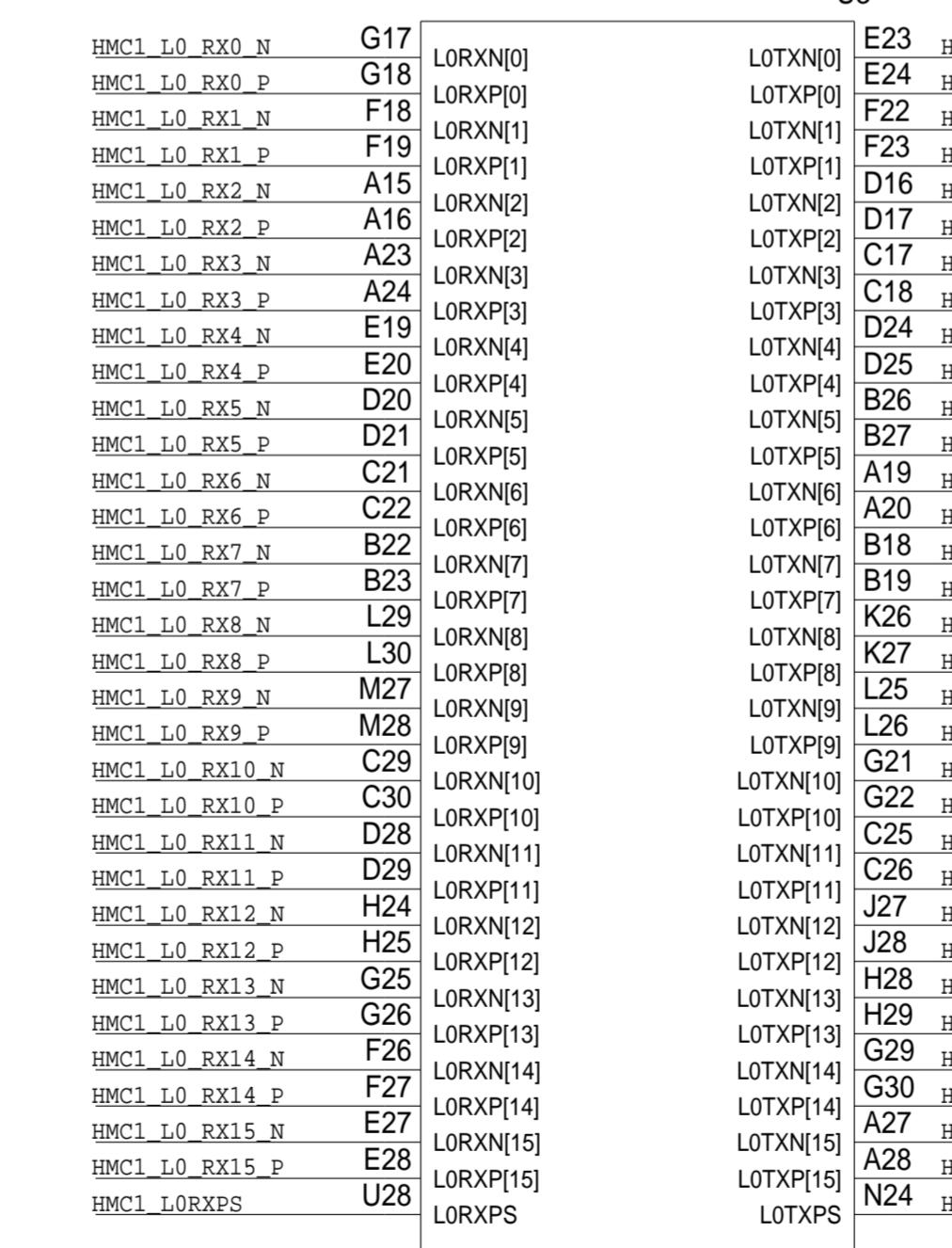
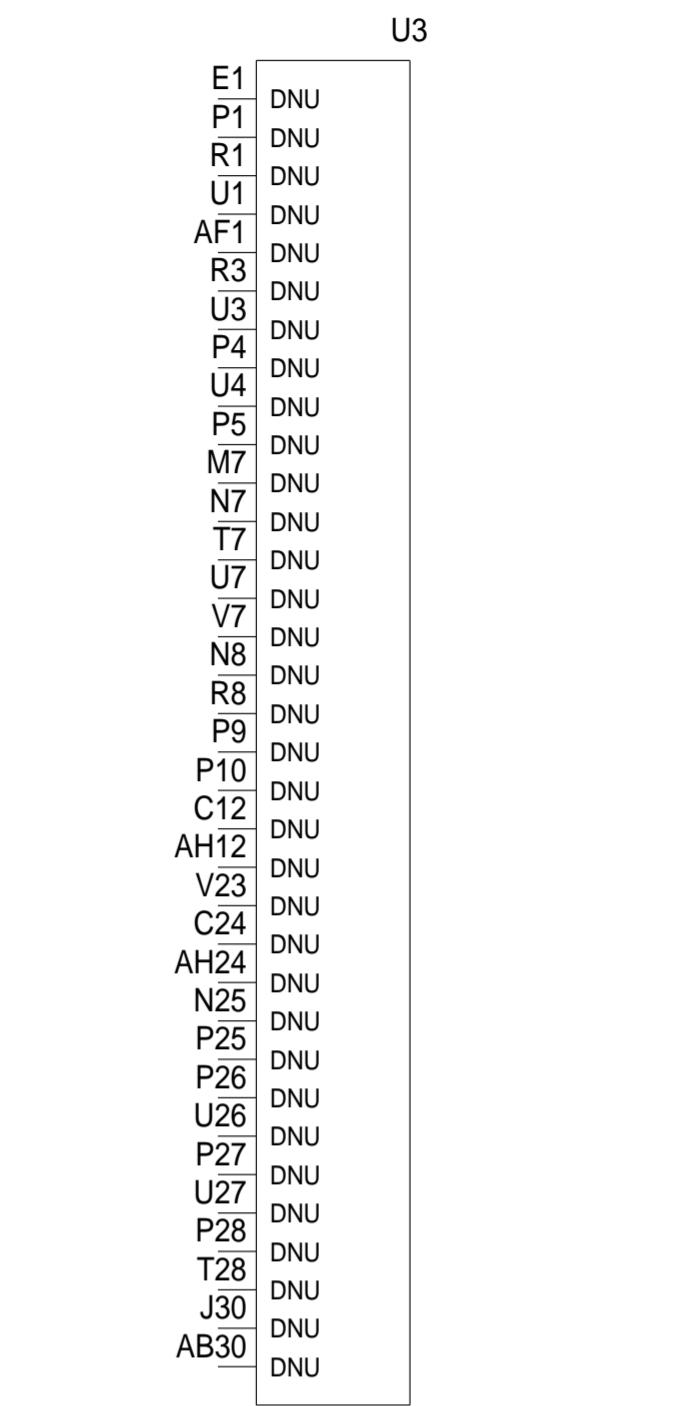
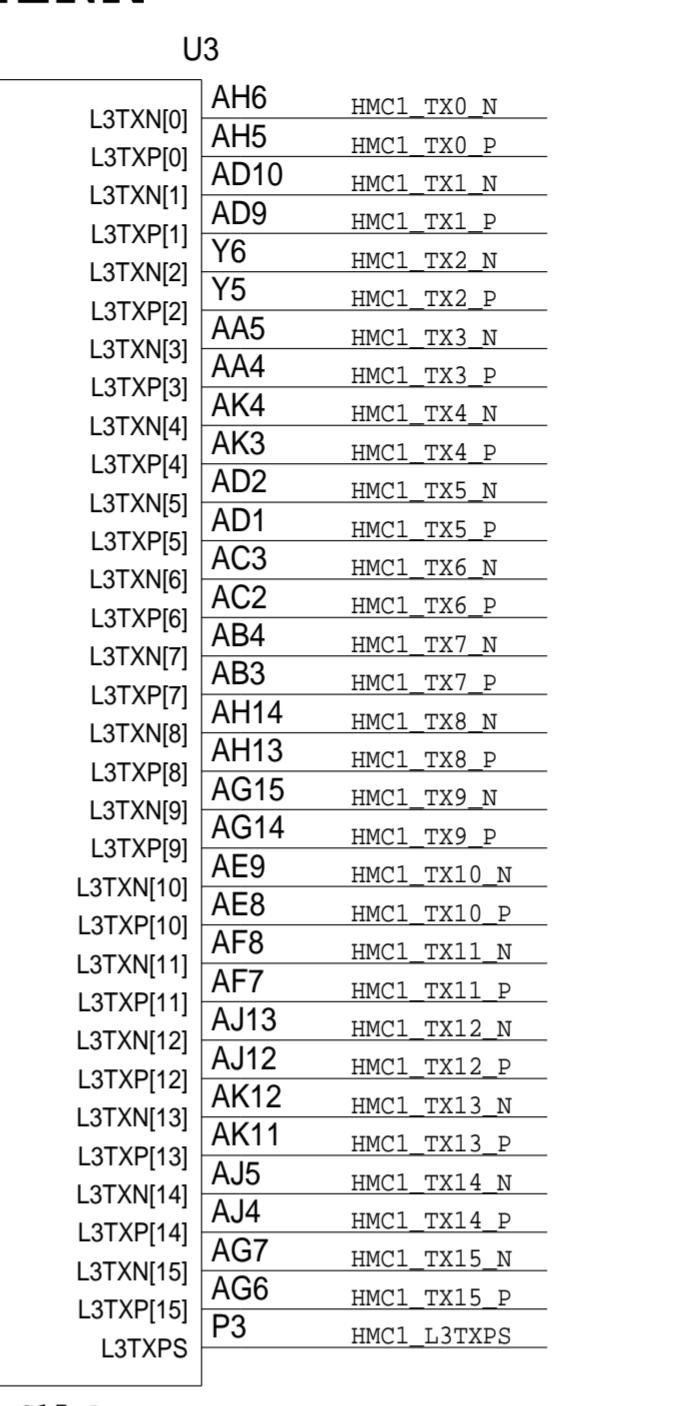
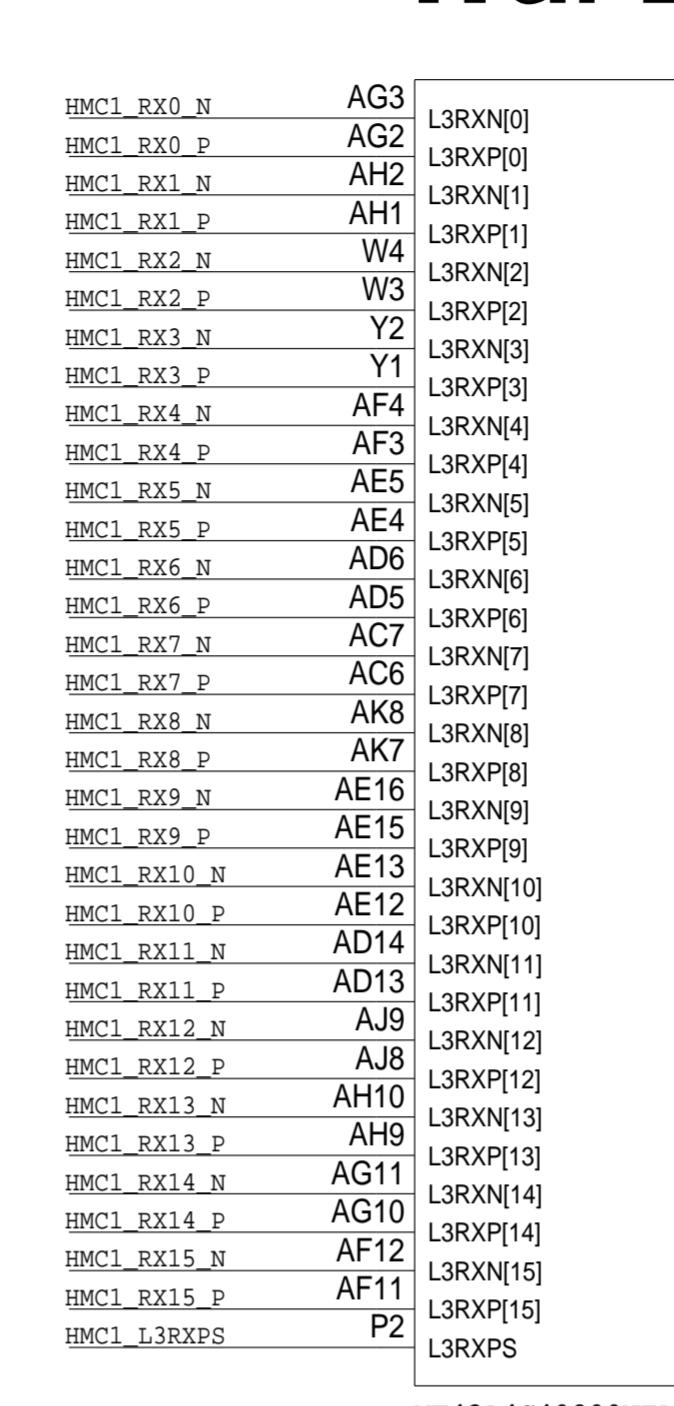
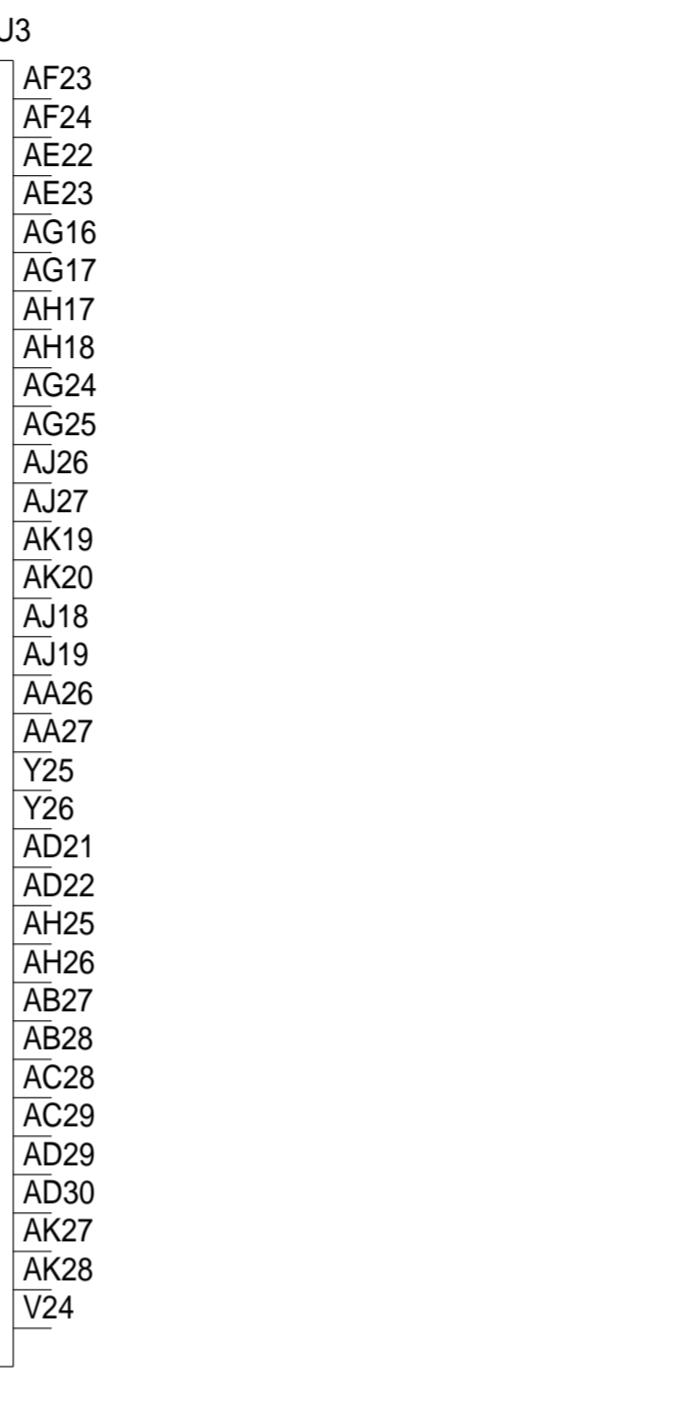
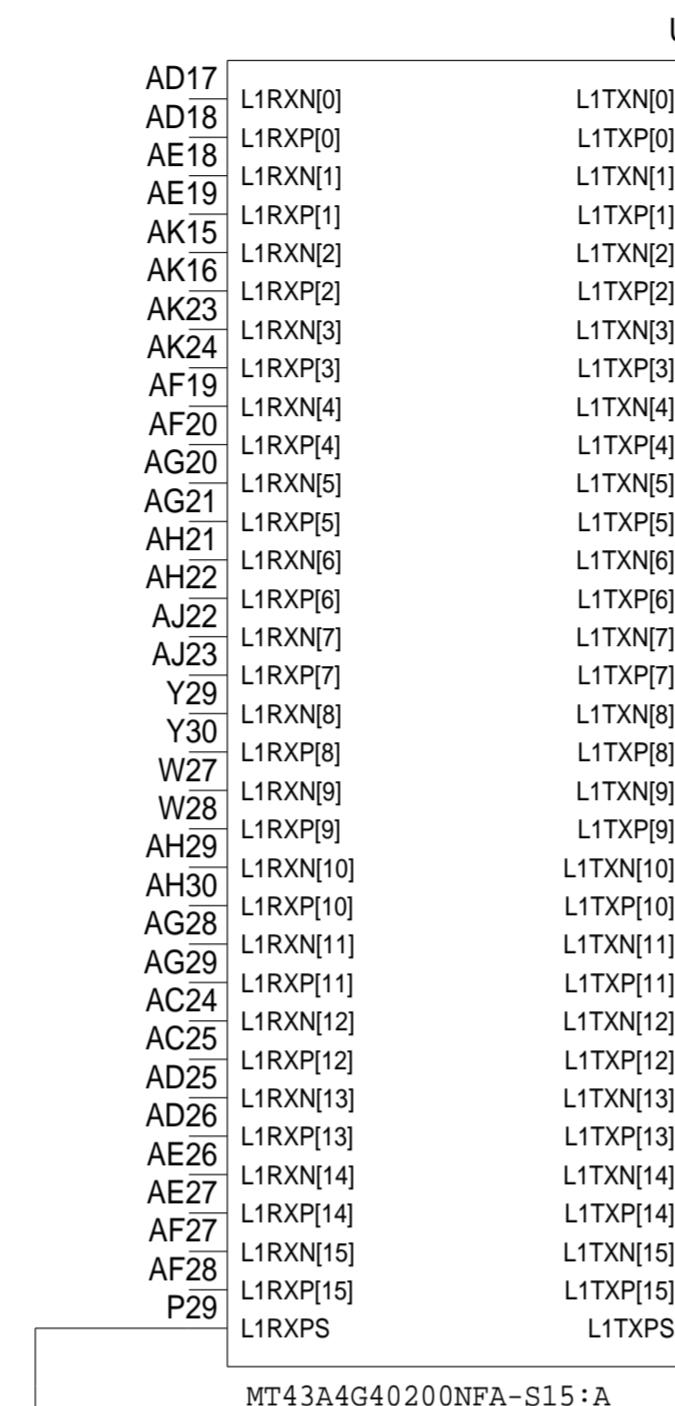
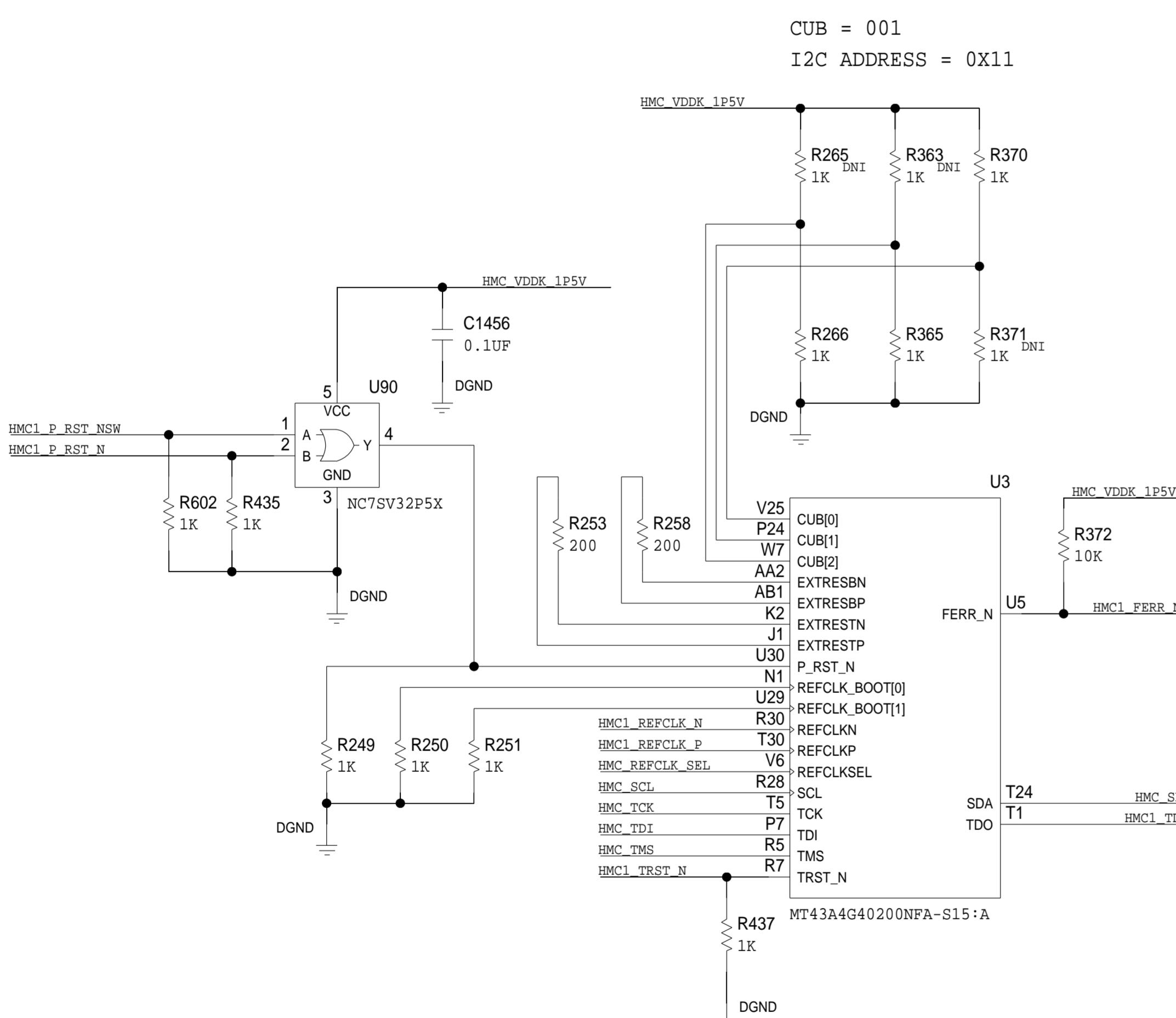
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HMC1 DATA AND CONTROL

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	DESCRIPTION	DATE

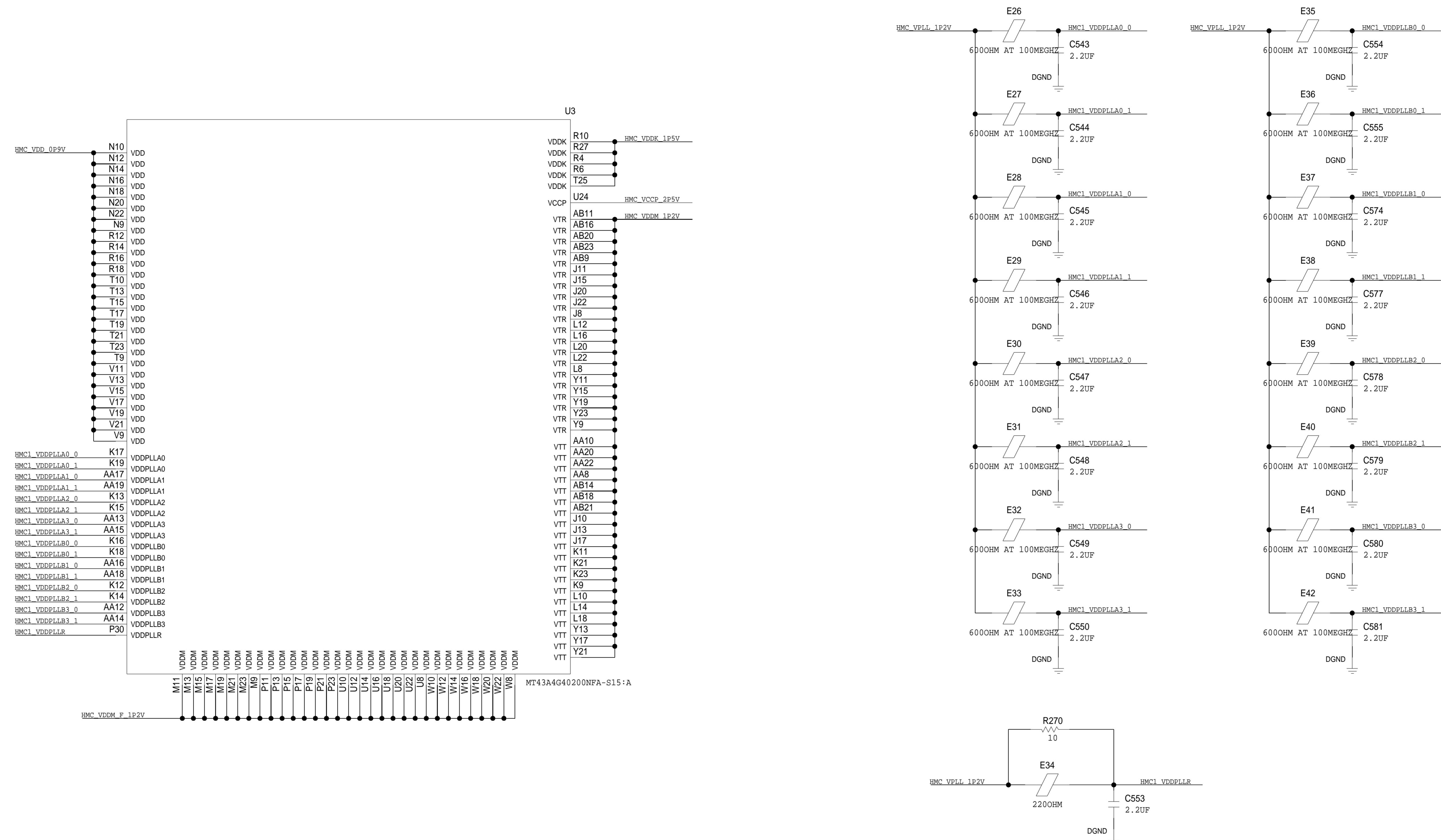


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Product(s)	: N/A		
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REVISIONS

REV	DESCRIPTION	DATE	APPROVED

HMC1 POWER



SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s): N/A
 : N/A

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DRAWING NO.
 02_045361

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PTD ENGINEER
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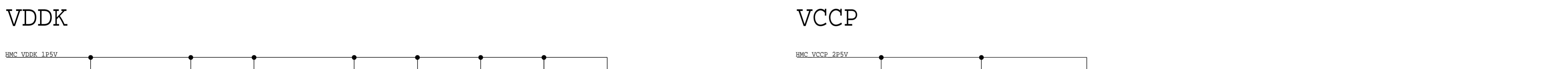
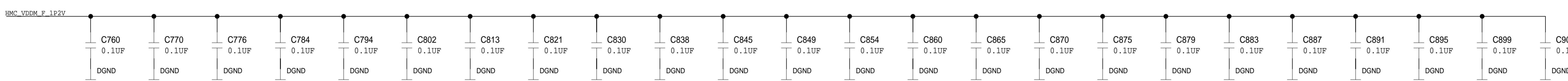
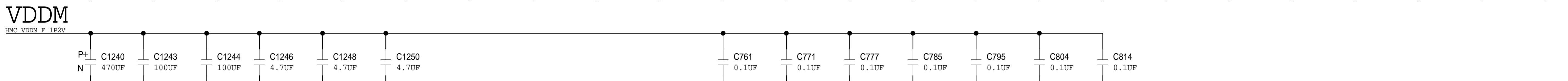
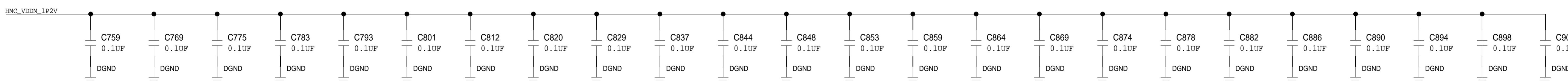
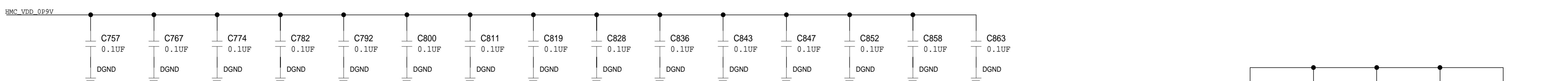
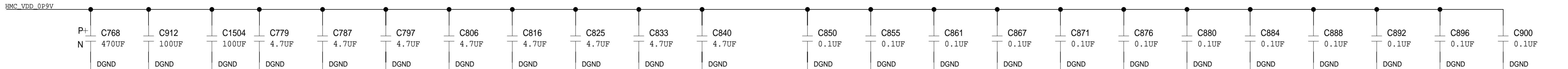
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REV	DESCRIPTION	DATE	APPROVED

HMC1 DECOUPLING

VDD

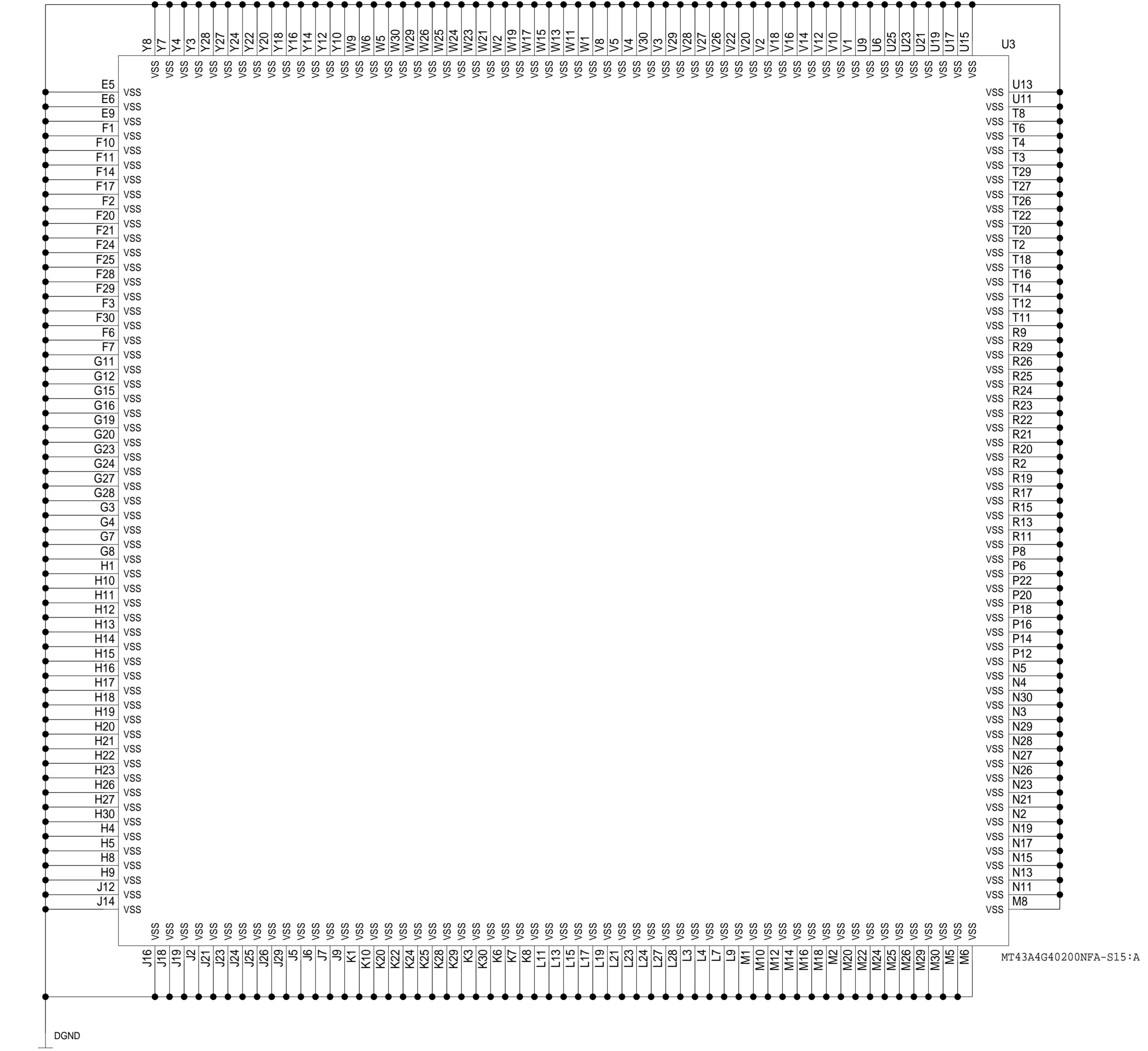
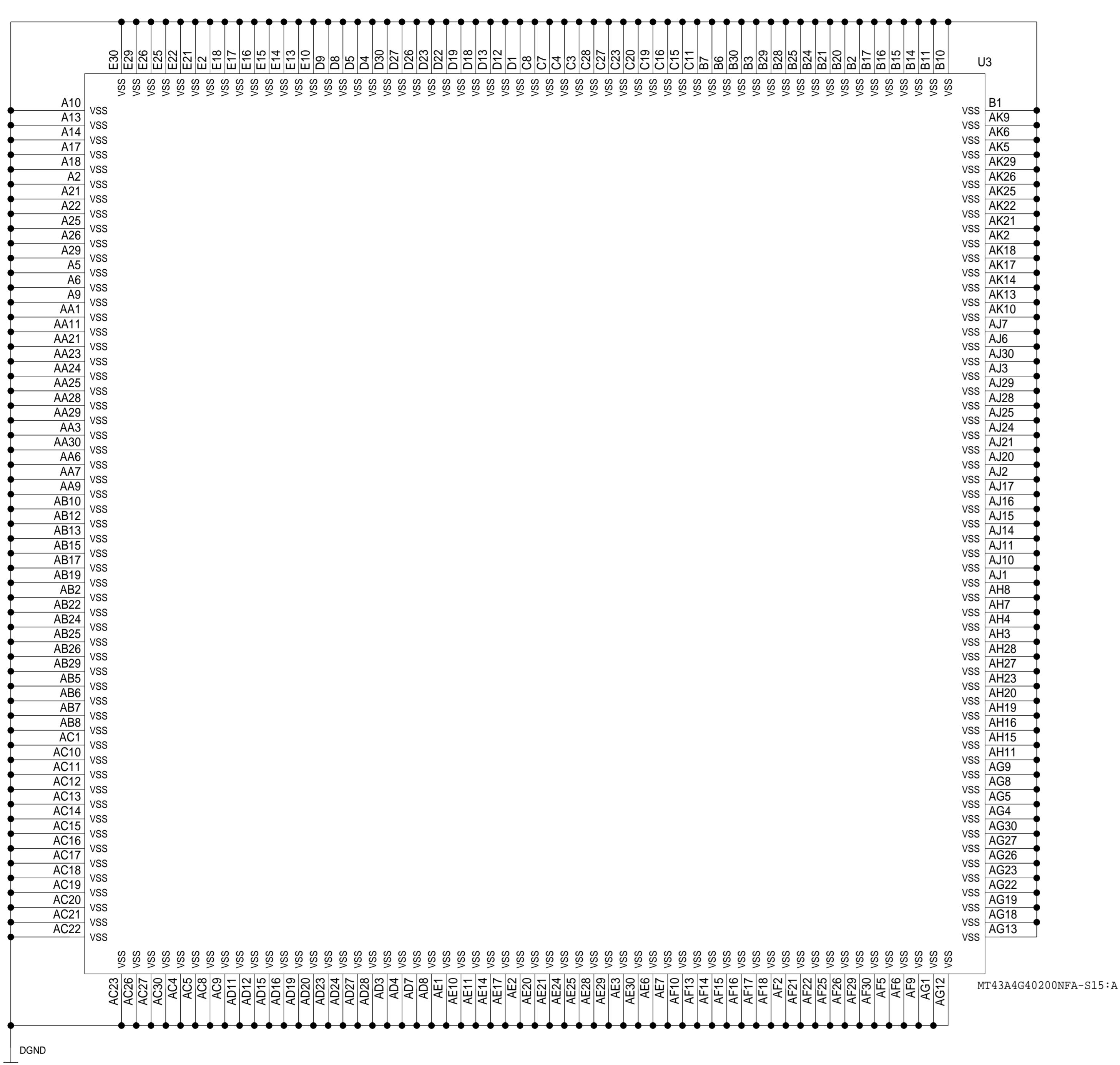
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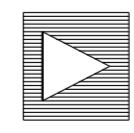


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Product(s): N/A		REV E	
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DESIGN VIEW <DESIGN_VIEW>			
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 27 OF 52

HMC1 GND

8	7	6	5	4	3	2	1
				REVISIONS			
REV	DESCRIPTION			DATE	APPROVED		



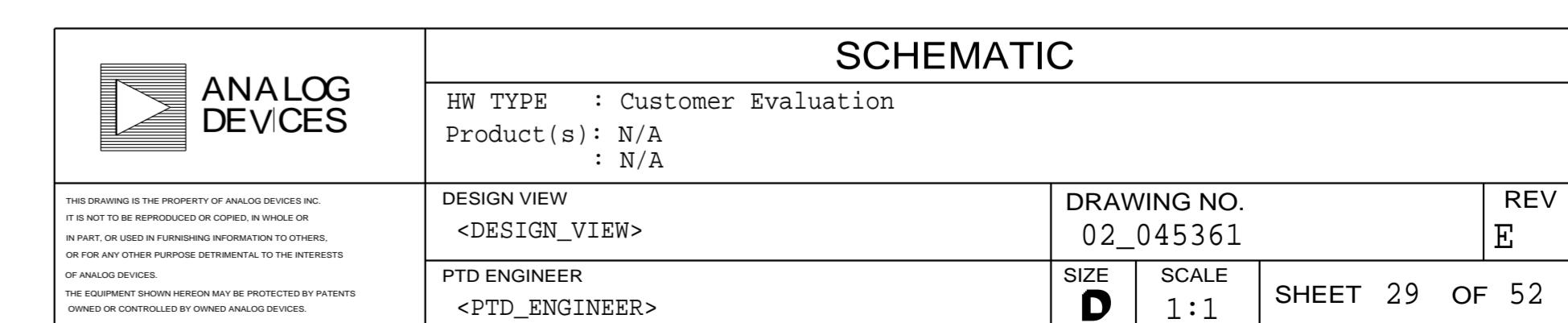
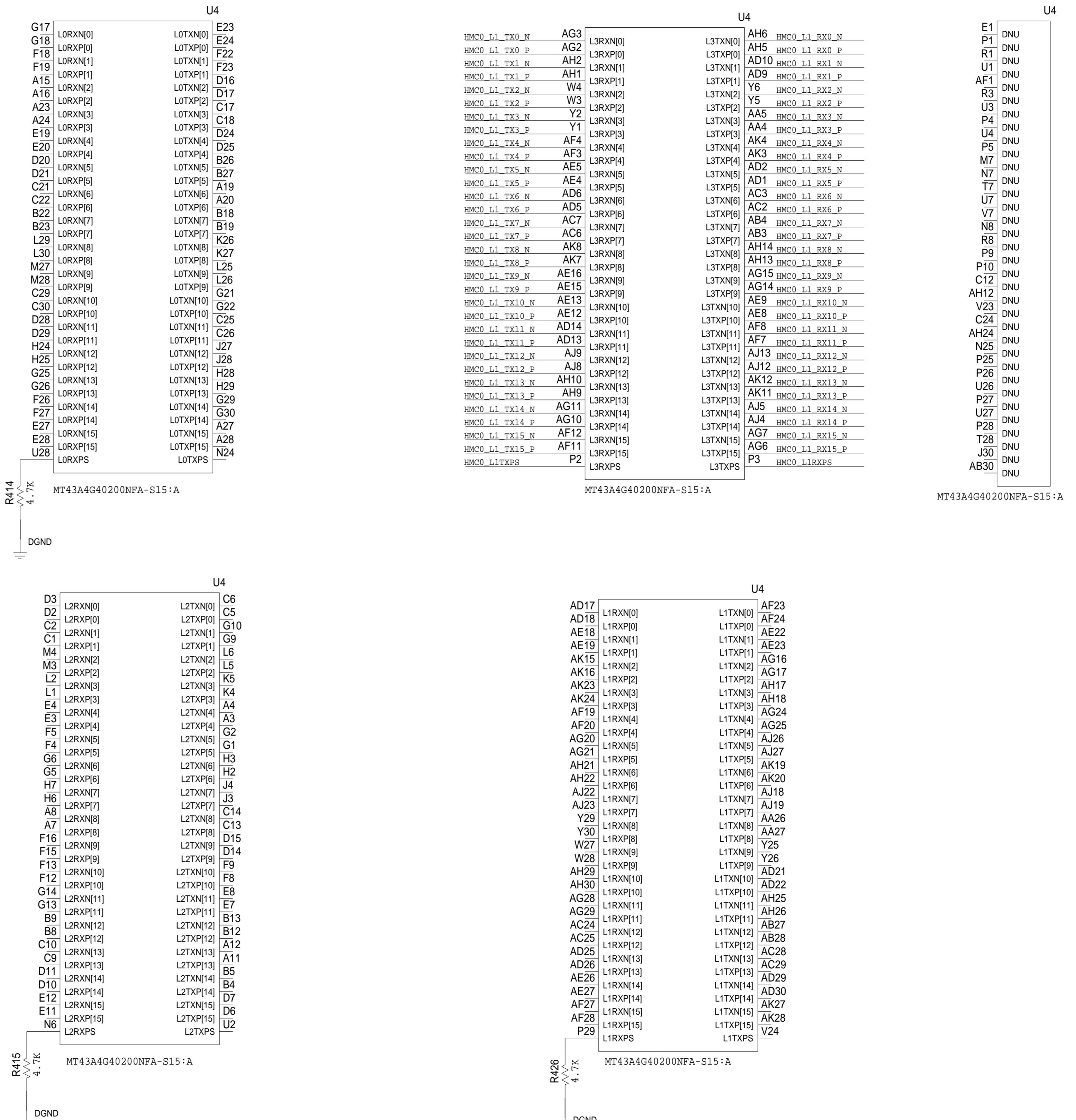
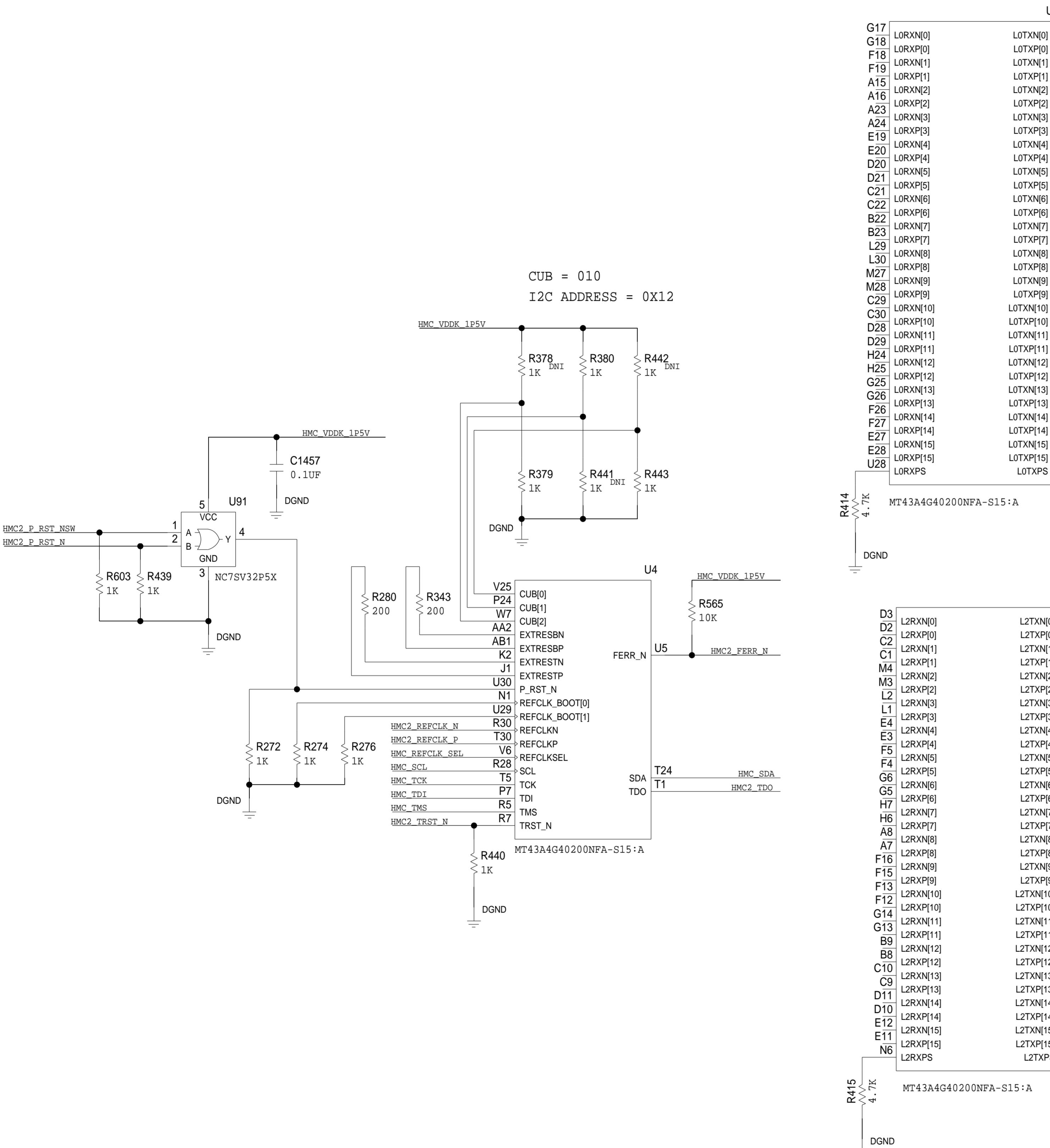
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	SIZE D SCALE 1:1 SHEET 28 OF 52

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HMC2 DATA AND CONTROL

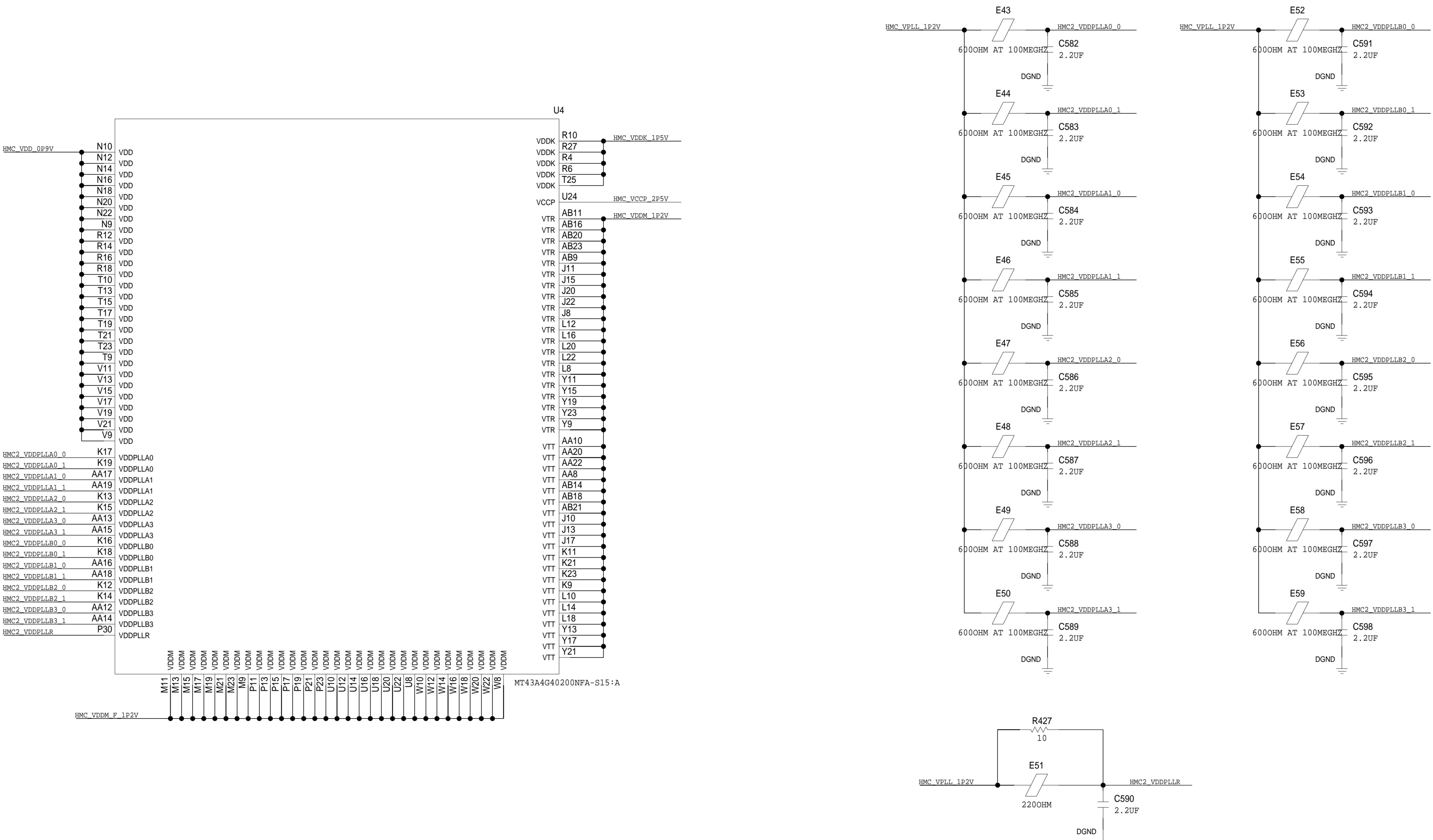
REVISIONS		
DESCRIPTION	DATE	APPROVED

CHAIN FROM HMC0



HMC2 POWER

REVISIONS		
	DESCRIPTION	DATE



SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): N/A
 : N/A

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DRAWING NO. REV

02_045361

SIZE — SCALE — SHEET — 30 OF — 52

D 1:1 SHEET 30 OF 52

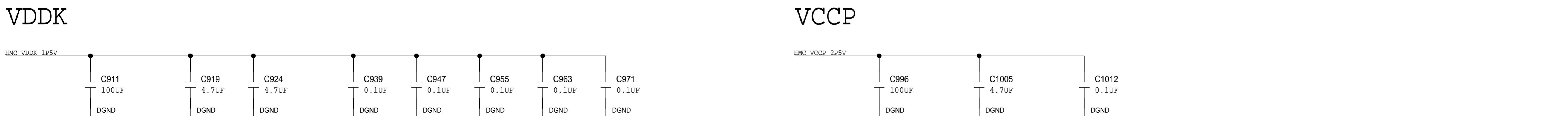
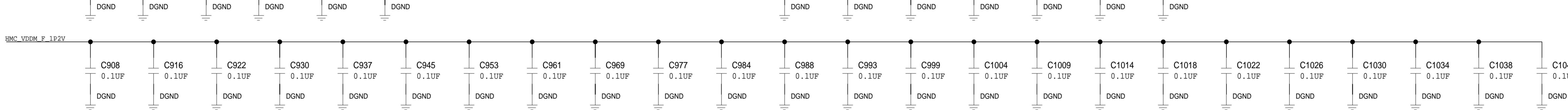
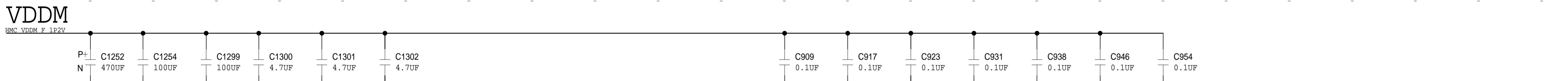
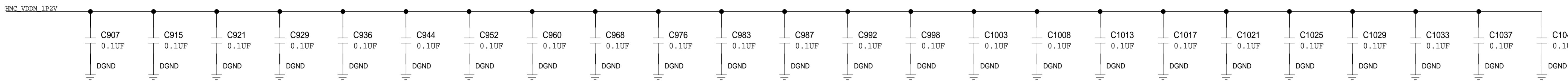
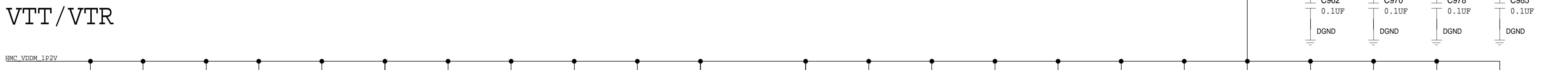
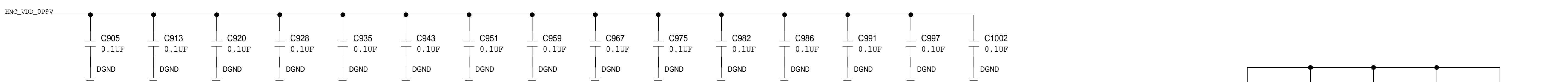
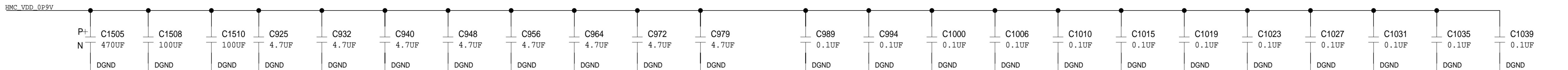
REVISIONS

REV	DESCRIPTION	DATE	APPROVED

HMC2 DECOUPLING

VDD

PLACE ALL CAPS AS CLOSE TO HMC2 PINS AS POSSIBLE



SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s): N/A
 : N/A

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DRAWING NO.
 02_045361

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PTD ENGINEER
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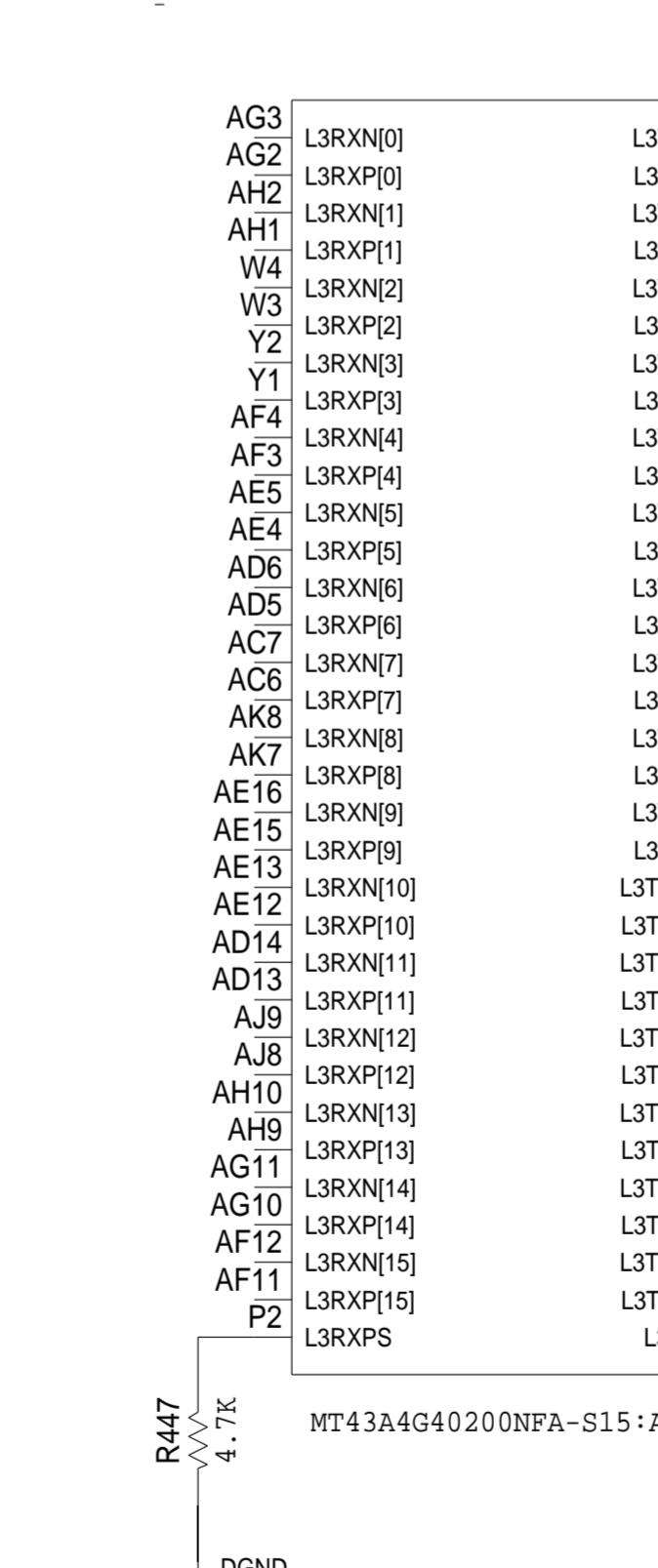
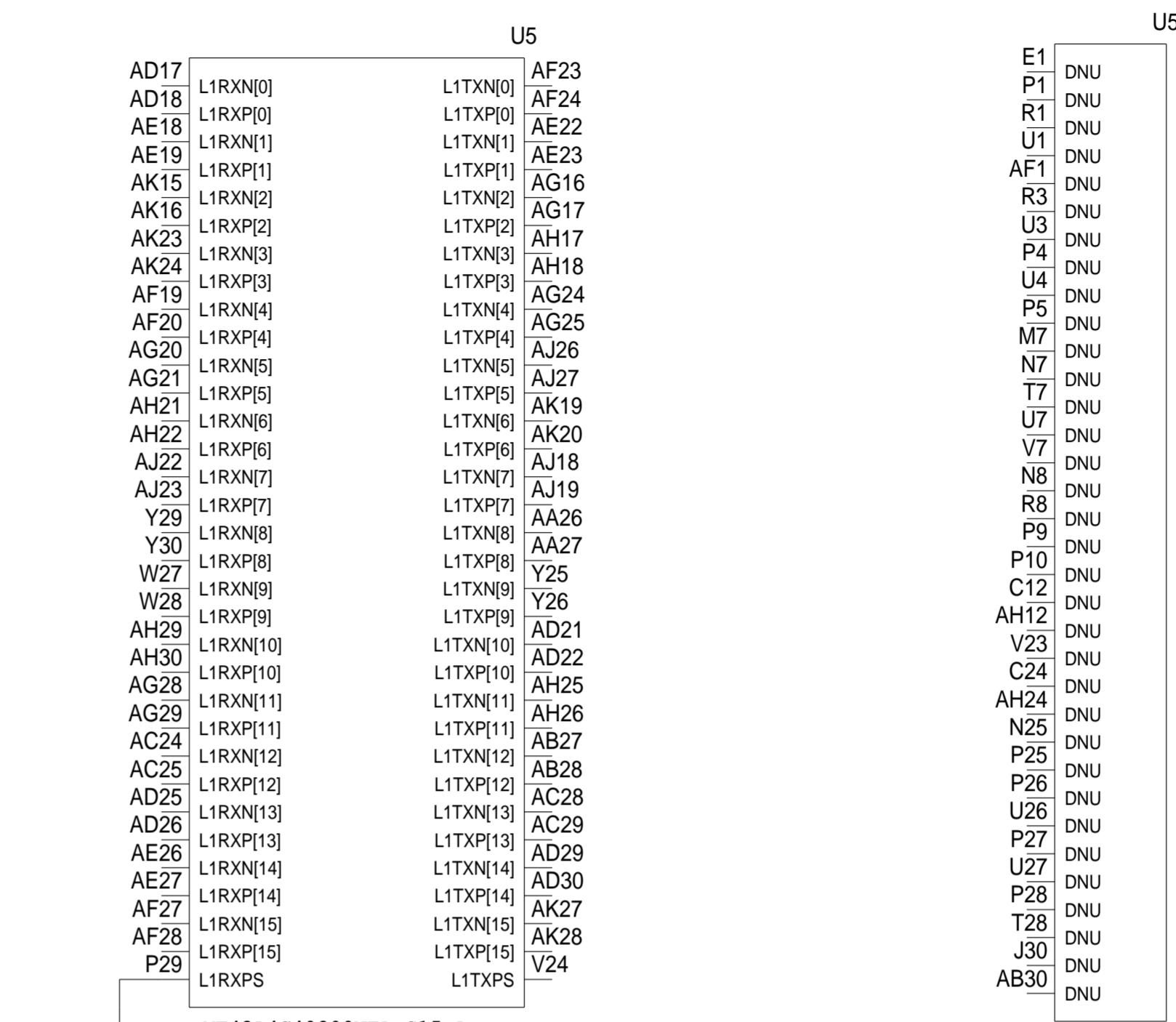
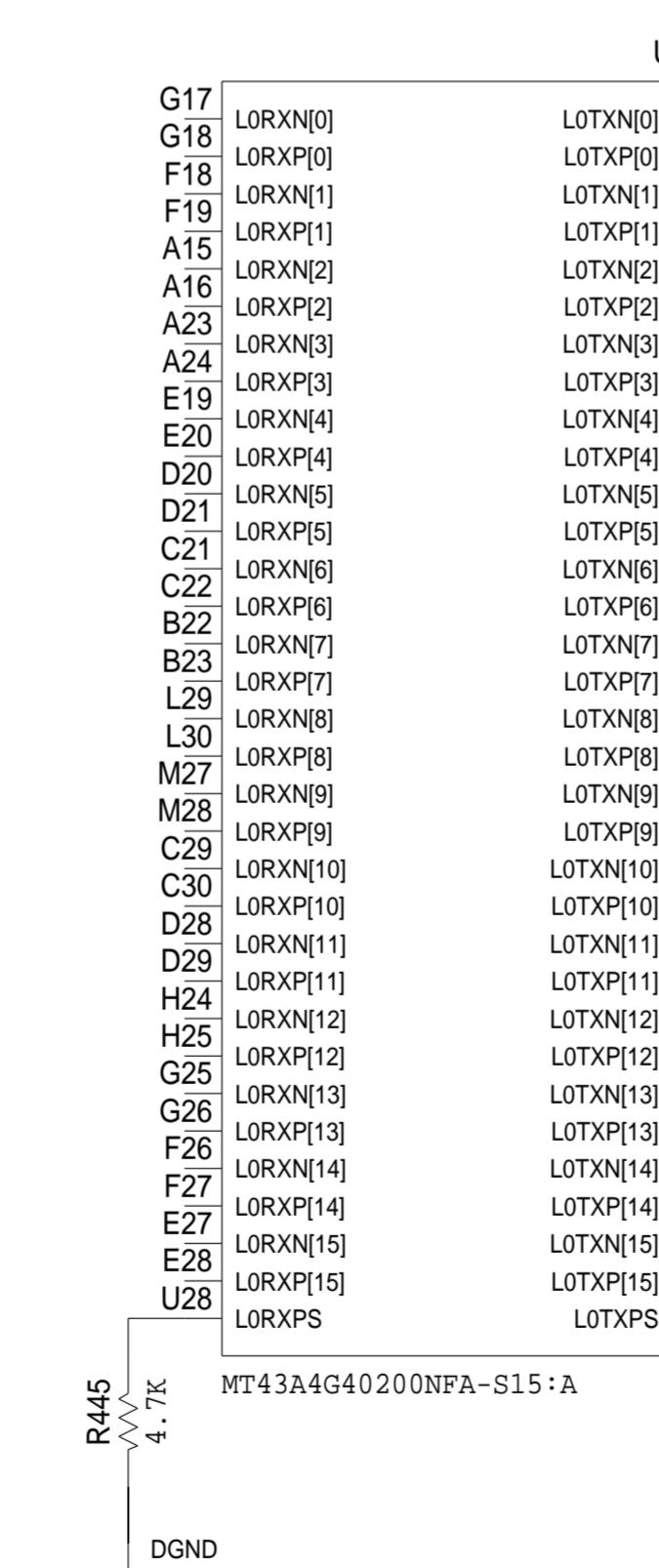
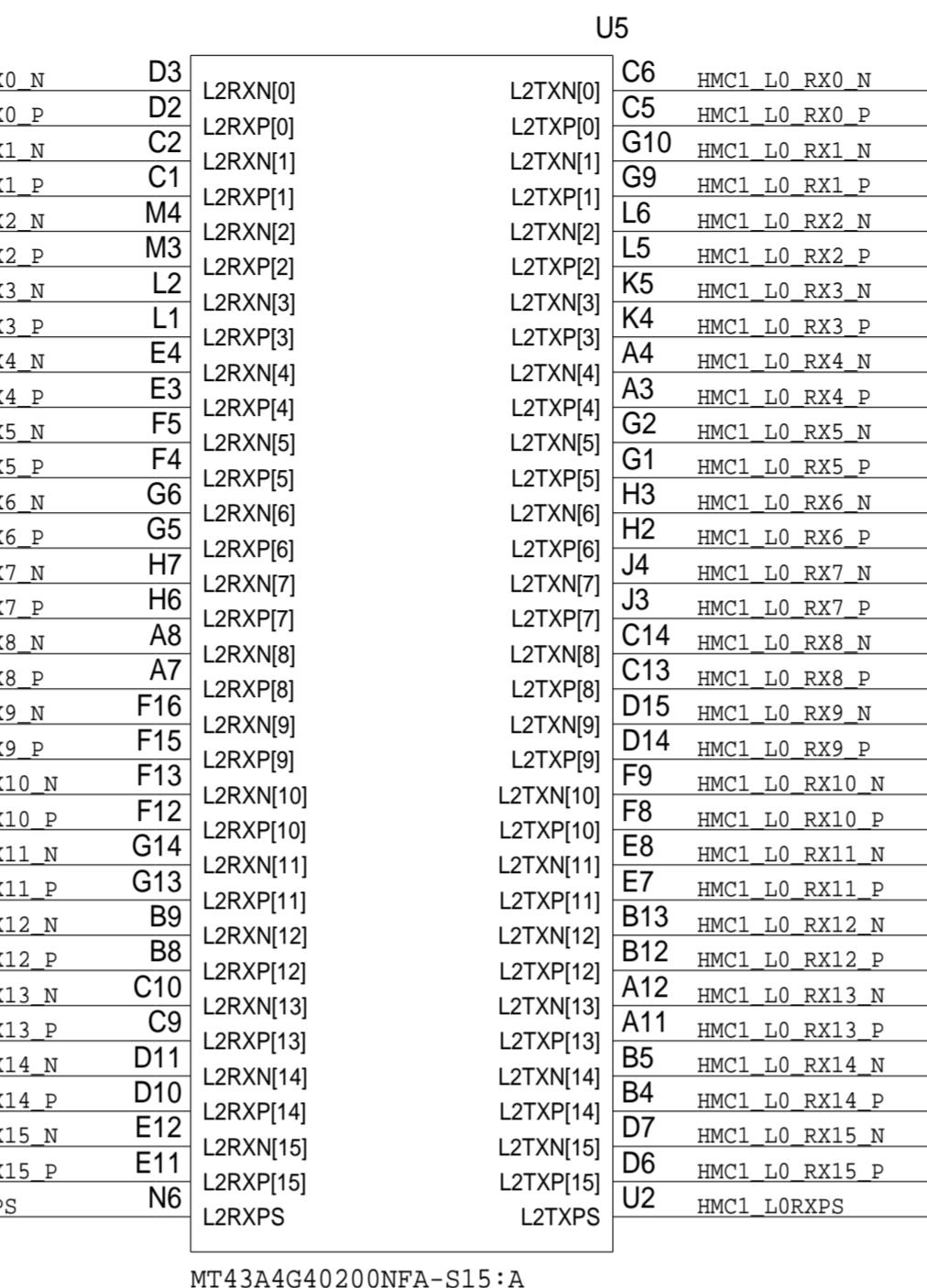
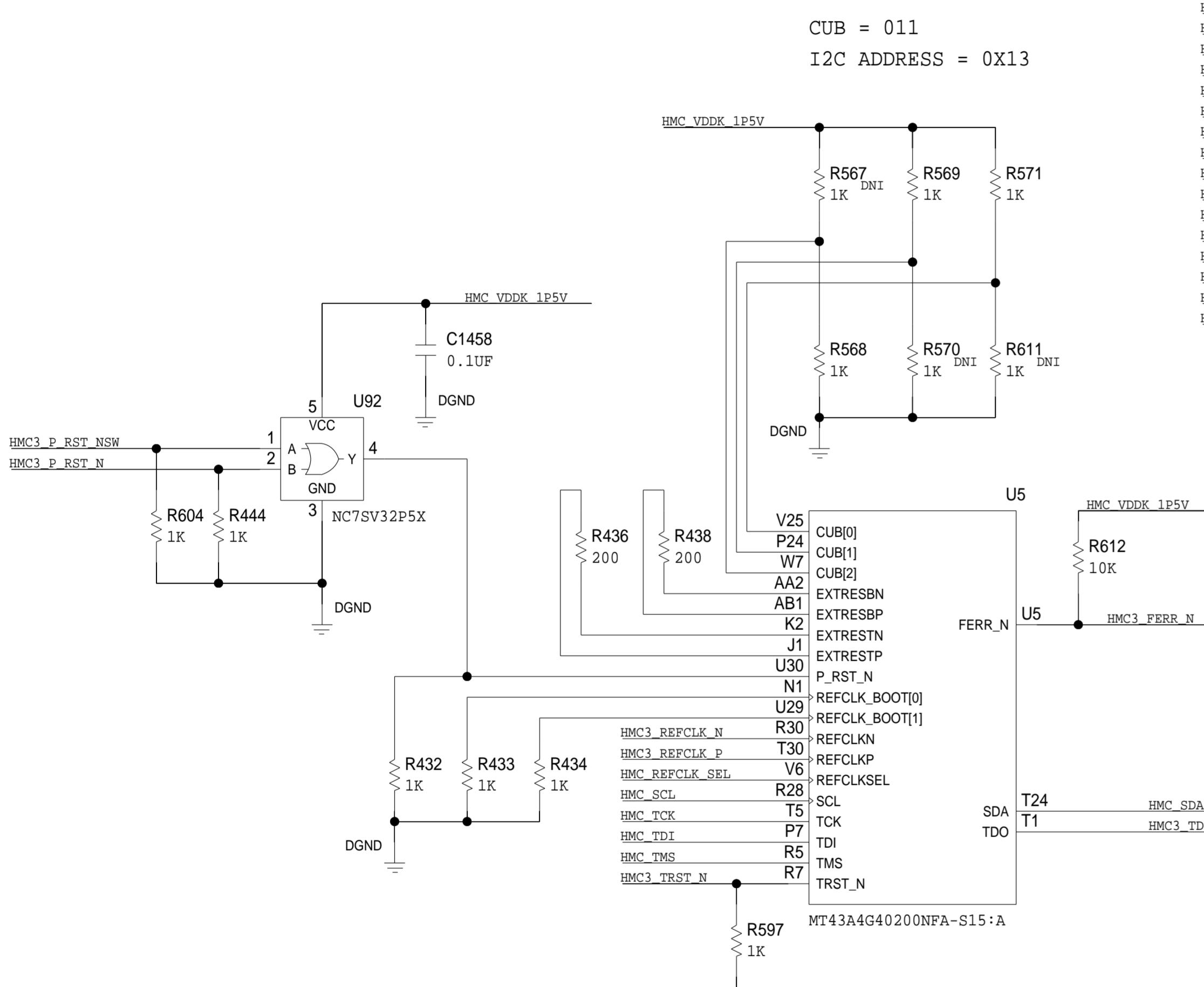
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SHEET 31 OF 52

HMC3 DATA AND CONTROL

CHAIN FROM HMC1

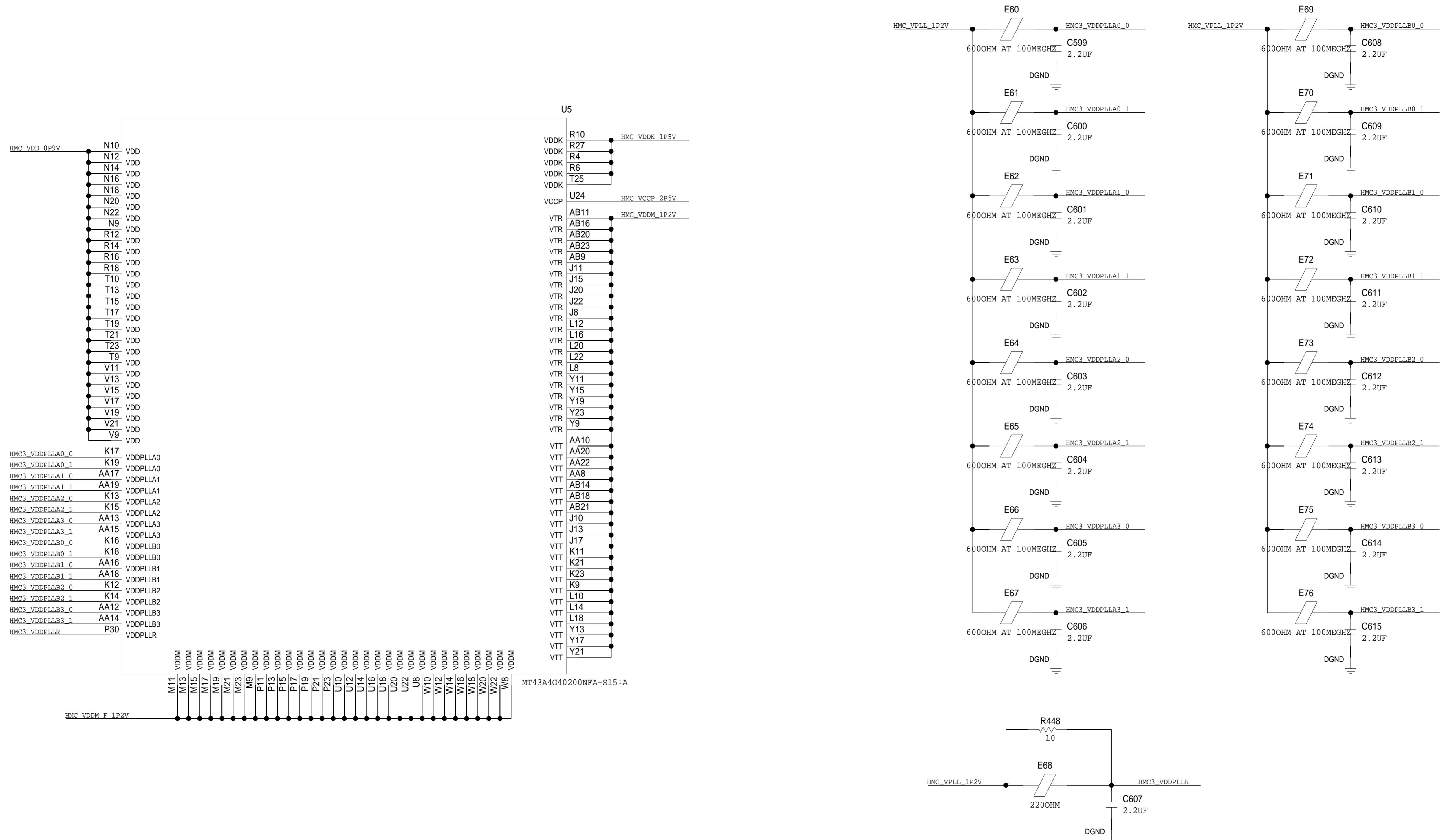


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	Product(s)	:	N/A	
		:	N/A	
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	PTD ENGINEER <PTD_ENGINEER>	SIZE P	SCALE 1:1	SHEET 33 OF 52

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

HMC3 POWER



SCHEMATIC	
HW TYPE : Customer Evaluation	REV E
Product(s): N/A	
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DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_045361
PTD ENGINEER <PTD_ENGINEER>	SIZE D SCALE 1:1 SHEET 34 OF 52

REV	DESCRIPTION	DATE	APPROVED

HMC3 DECOUPLING

VDD

PLACE ALL CAPS AS CLOSE TO HMC3 PINS AS POSSIBLE

D

HMC_VDD_0P9V

D

HMC_VDD_0P9V

D

VTT/VTR

HMC_VDDM_1P2V

C

HMC_VDDM_1P2V

C

VDDM

HMC_VDDM_F_1P2V

B

HMC_VDDM_F_1P2V

B

VDDPLLA/VDDPLL_B/VDDPLL_R

HMC_VPLL_1P2V

B

VDDK

HMC_VDDK_1P5V

A

VCCP

HMC_VCCP_2P5V



SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): N/A
: N/A

DESIGN VIEW
<DESIGN_VIEW>

DRAWING NO.
02_045361

REV
E

PTD ENGINEER
<PTD_ENGINEER>

SIZE
D
SCALE
1:1
SHEET 35 OF 52

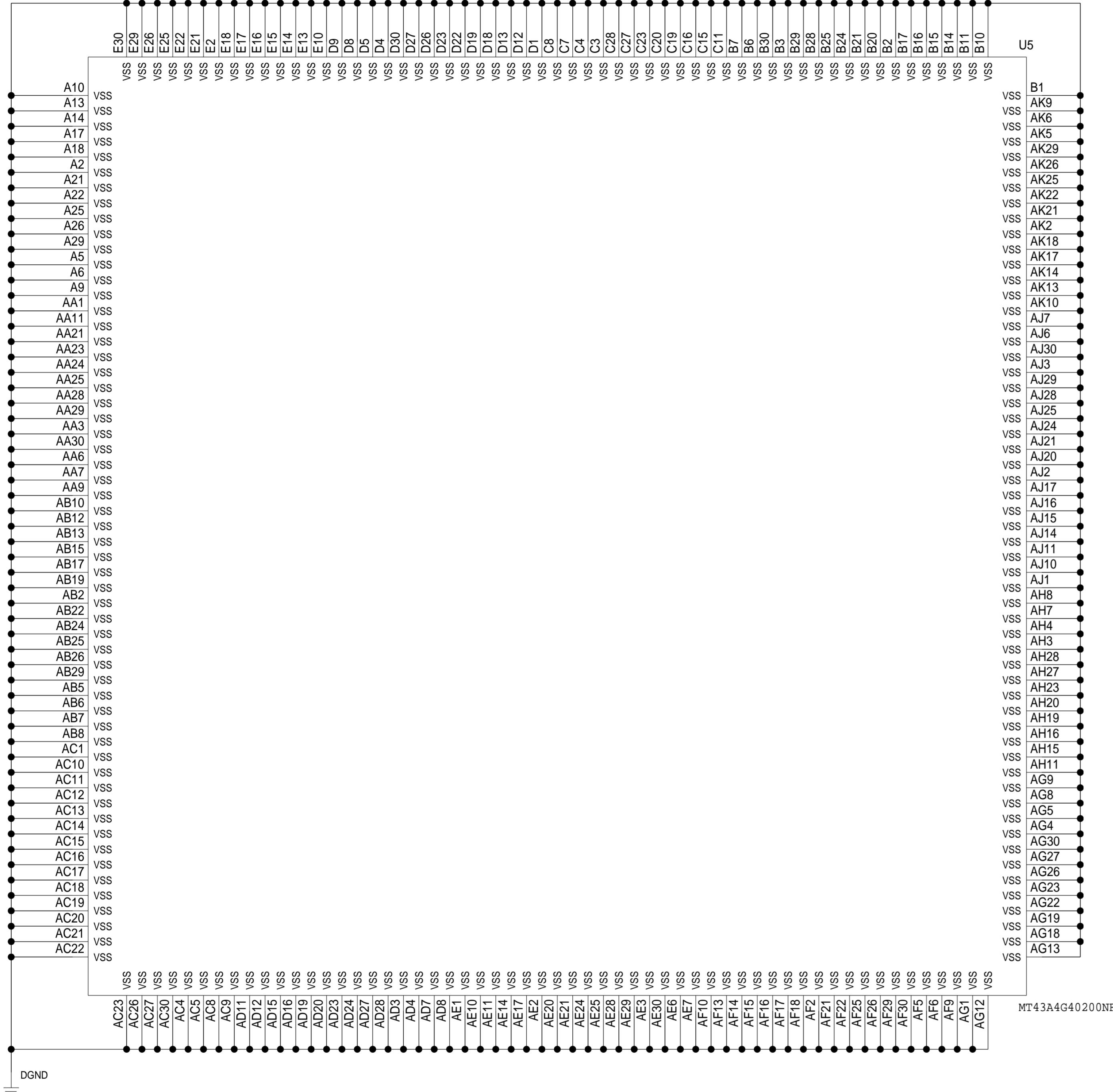
HMC3 GND

8 7 6 5 4 3 2 1

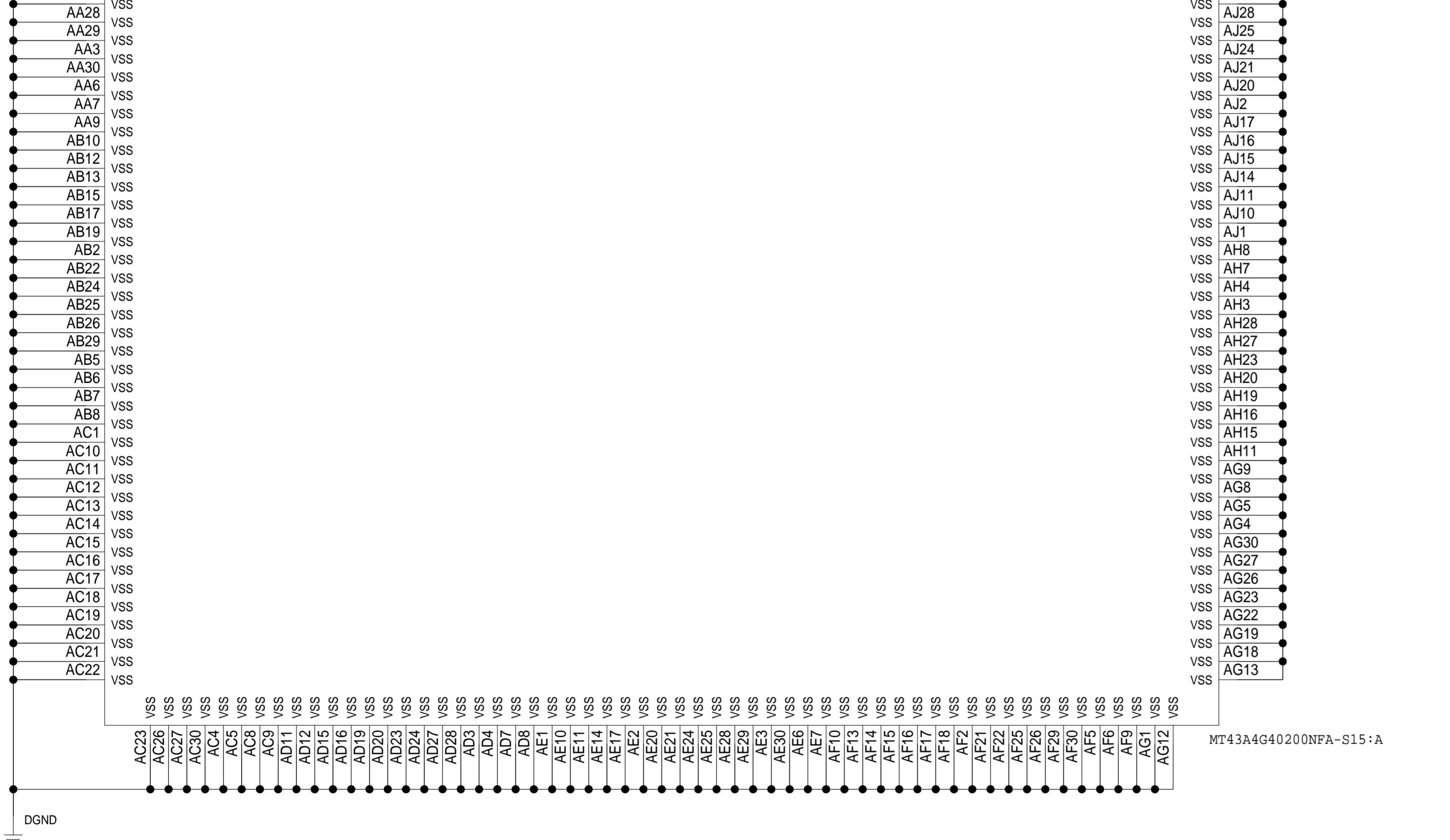
REVISIONS

REV	DESCRIPTION	DATE	APPROVED

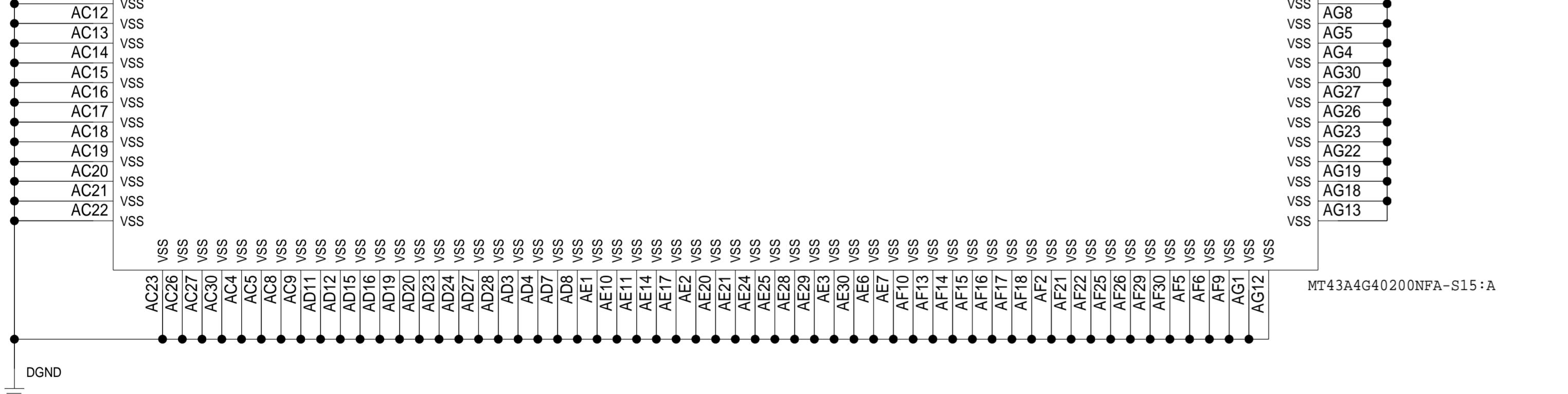
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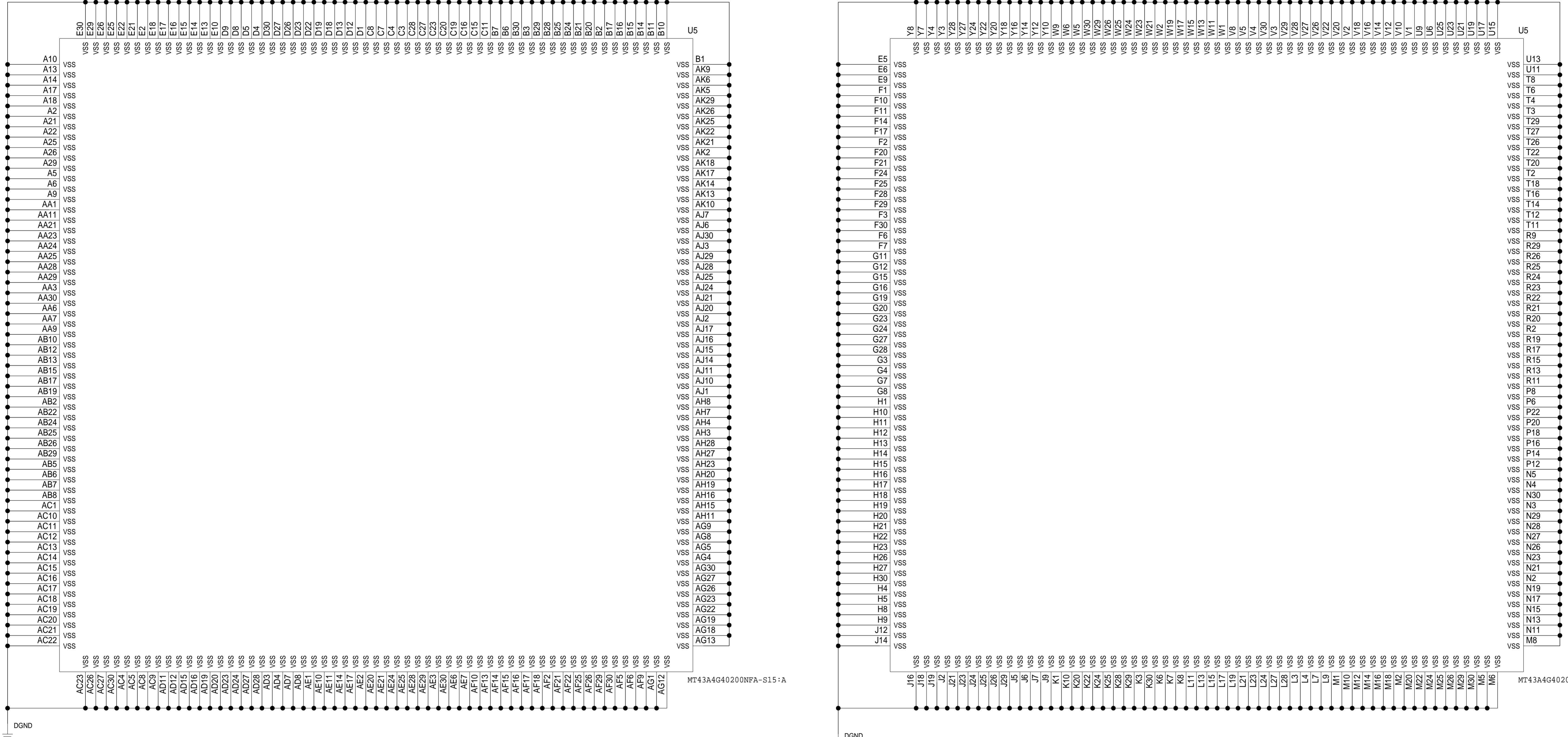


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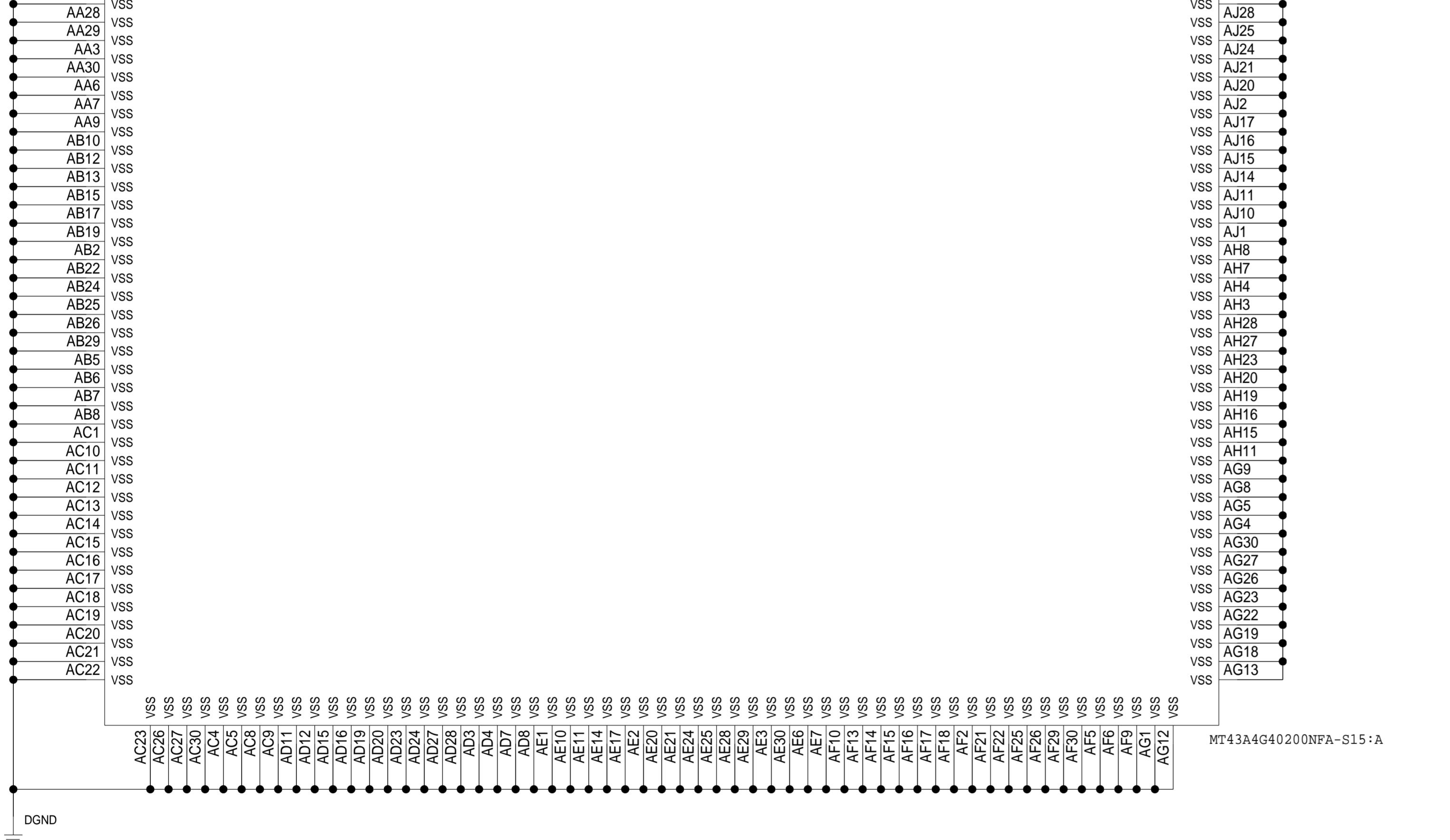


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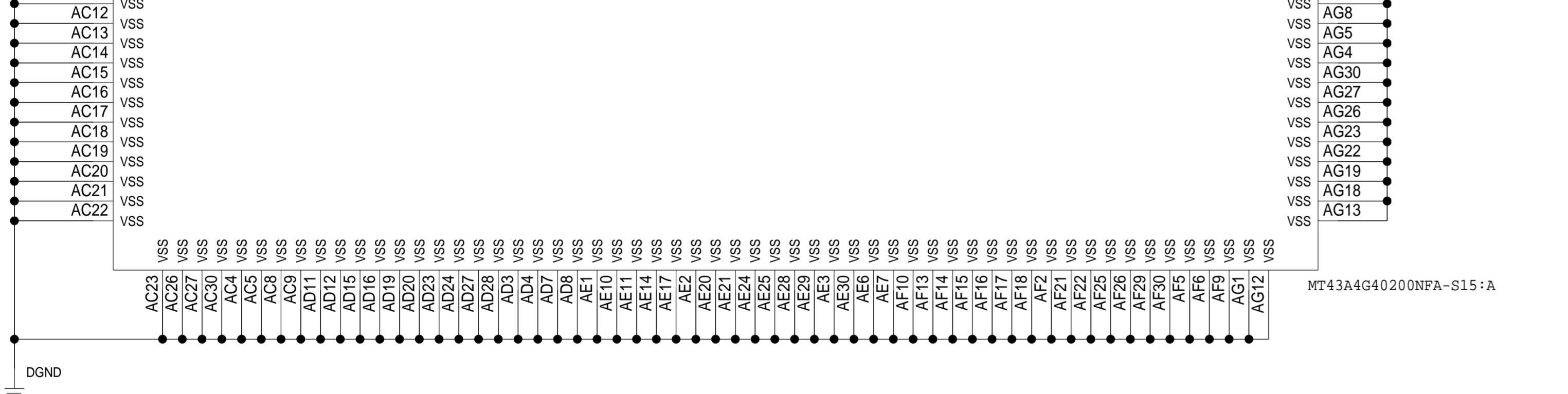
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C



B



ANALOG
DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): N/A
: N/A

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02_045361

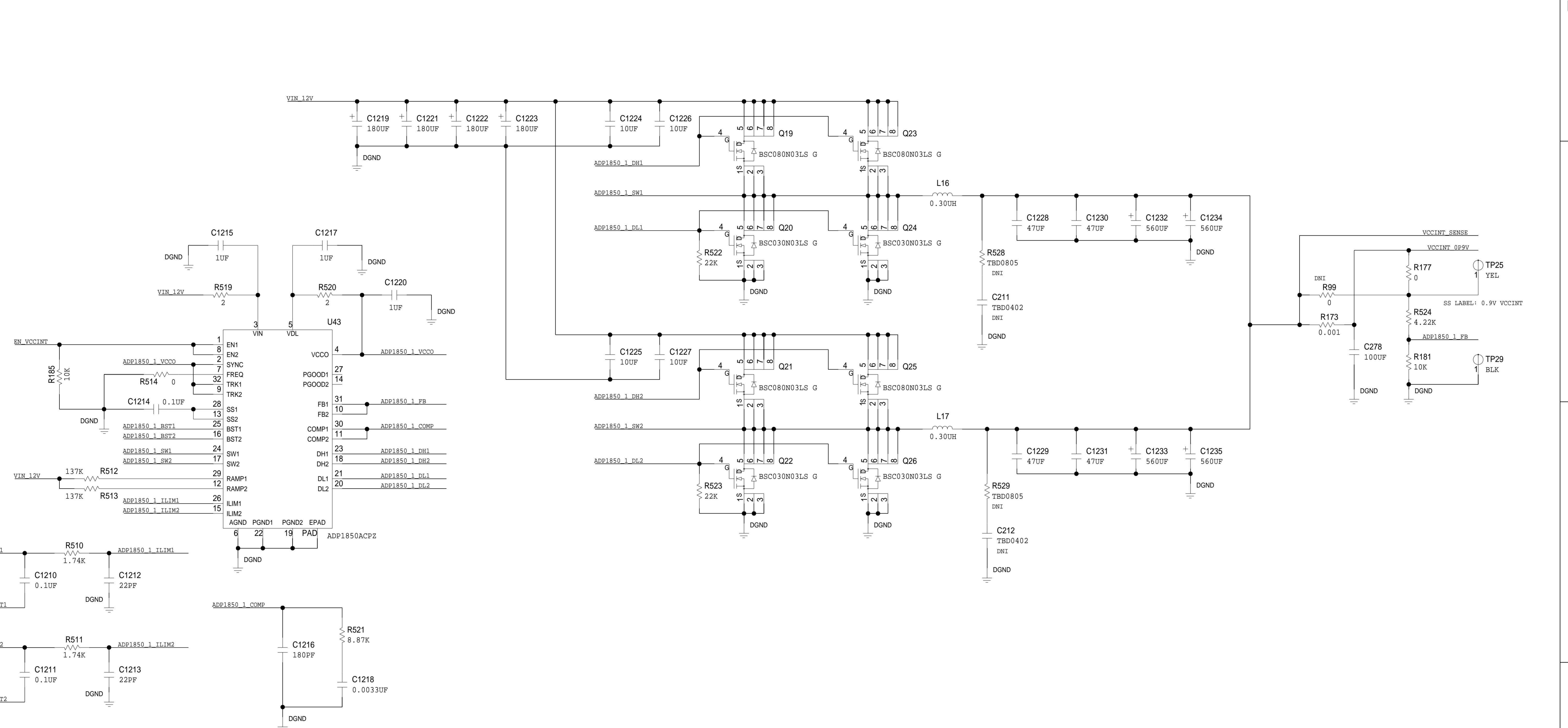
REV
E
SIZE
D
SCALE
1:1
SHEET 36 OF 52

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

POWER ADP1850 #1

VCCINT, 0.85V, 40A



SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s) : N/A
 : N/A

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DRAWING NO.
 02_045361

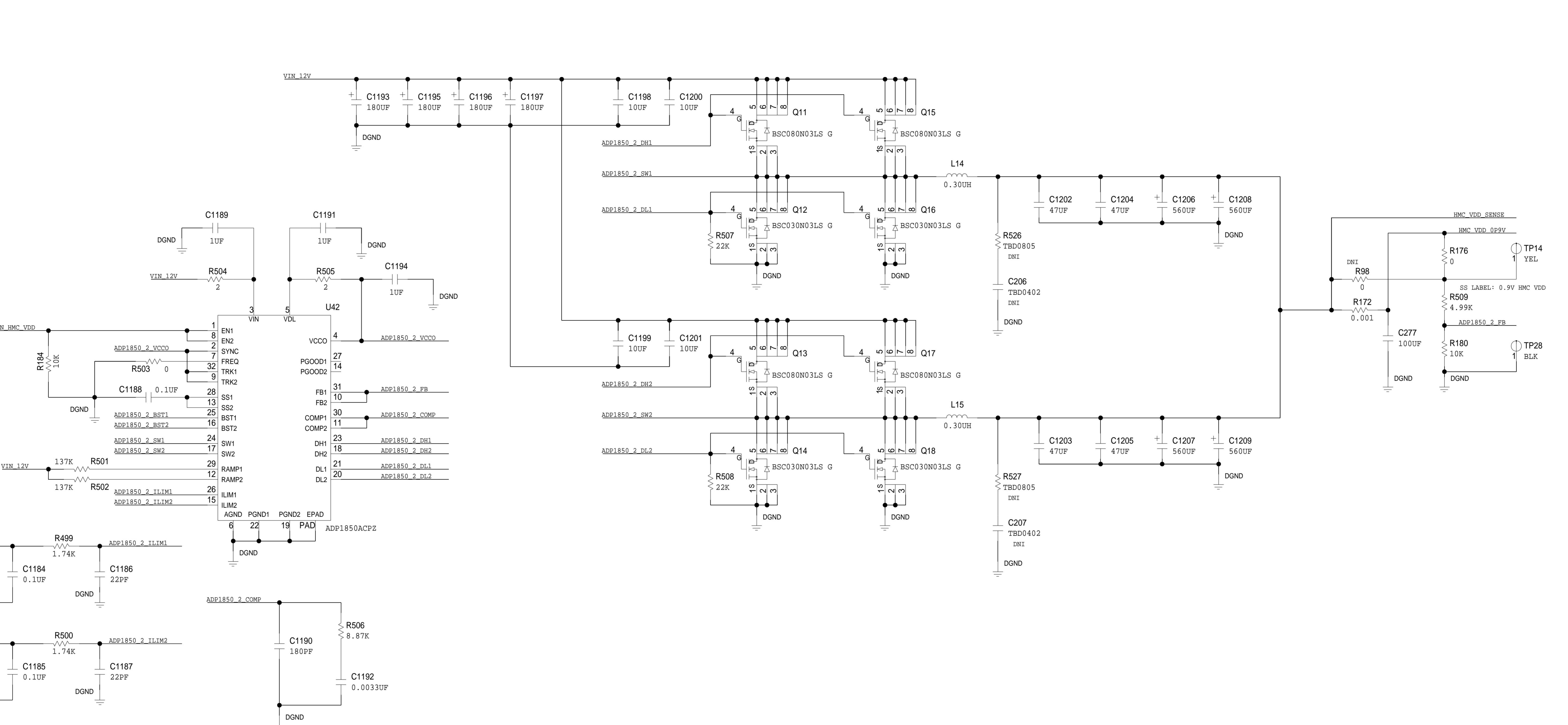
REV
 E
 SIZE
 D
 SCALE
 1:1
 SHEET 38 OF 52

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

POWER ADP1850 #2

HMC_VDD, 0.9V, 40A



SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s): N/A
 : N/A

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PTD ENGINEER

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DRAWING NO.

02_045361

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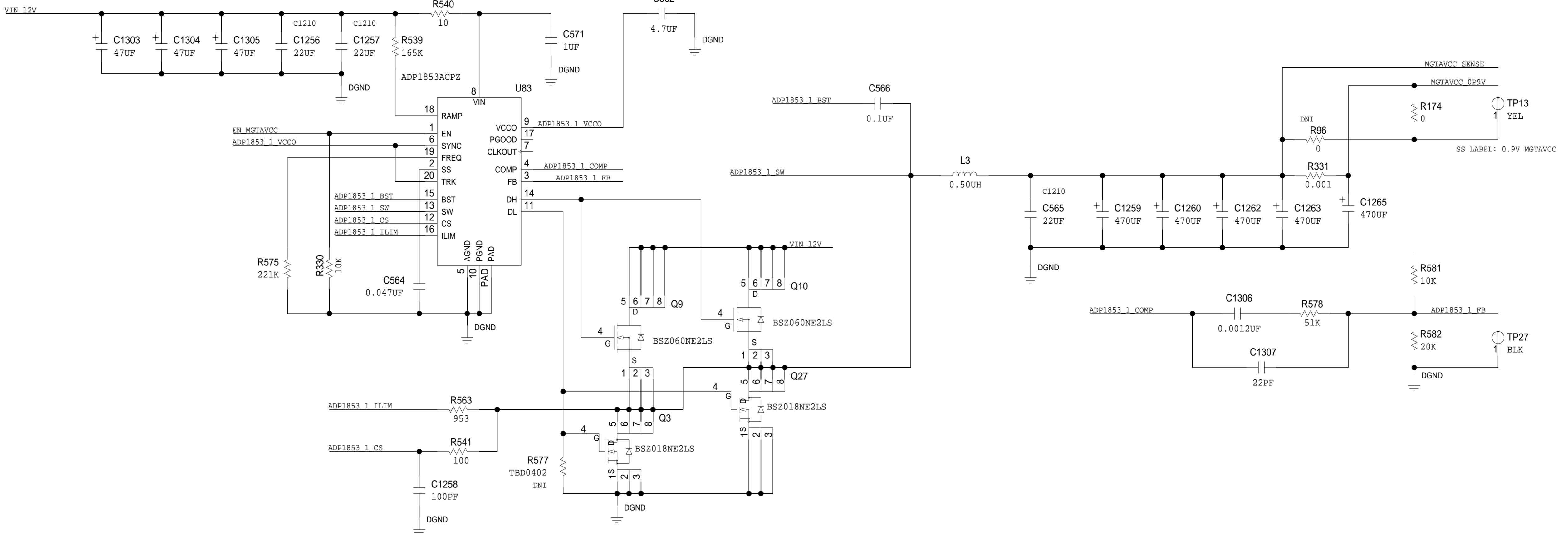
SIZE **D** SCALE 1:1 SHEET 39 OF 52

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

POWER ADP1853 #1

MGTAVCC, 0.9V, 18A



SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s) : N/A
 : N/A

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 02_045361
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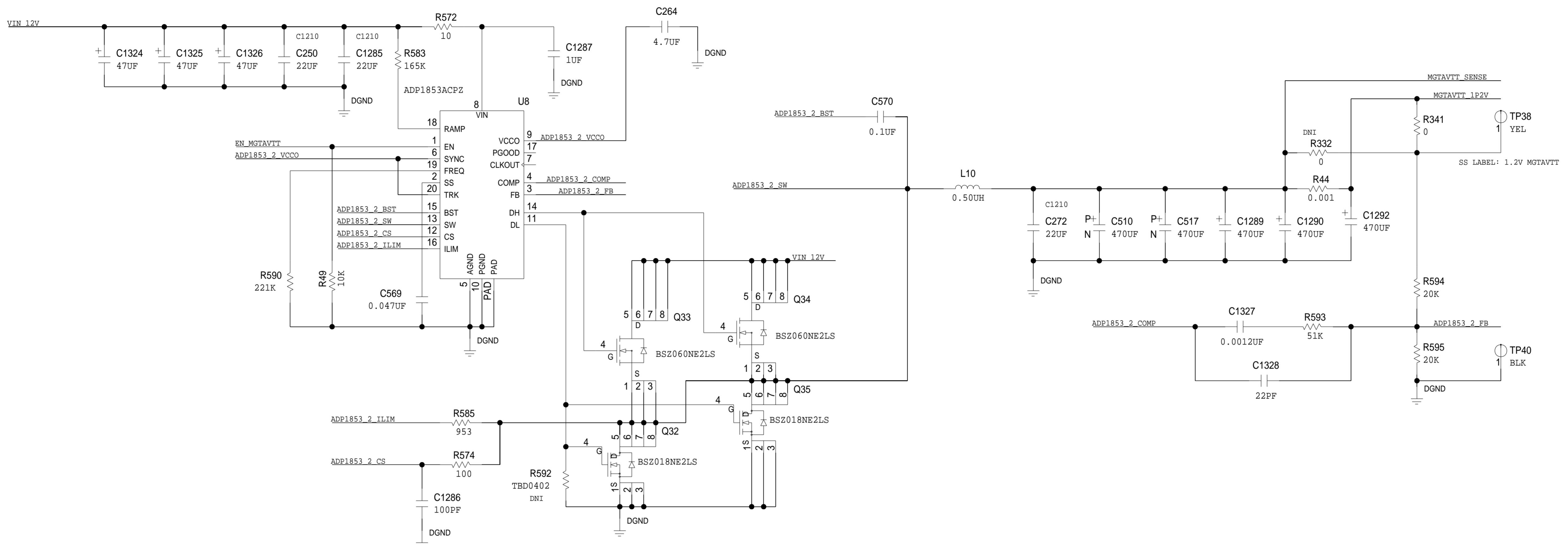
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SIZE
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 SCALE
 1:1
 SHEET 40 OF 52

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POWER ADP1853 #2

MGTAVTT, 1.2V, 18A



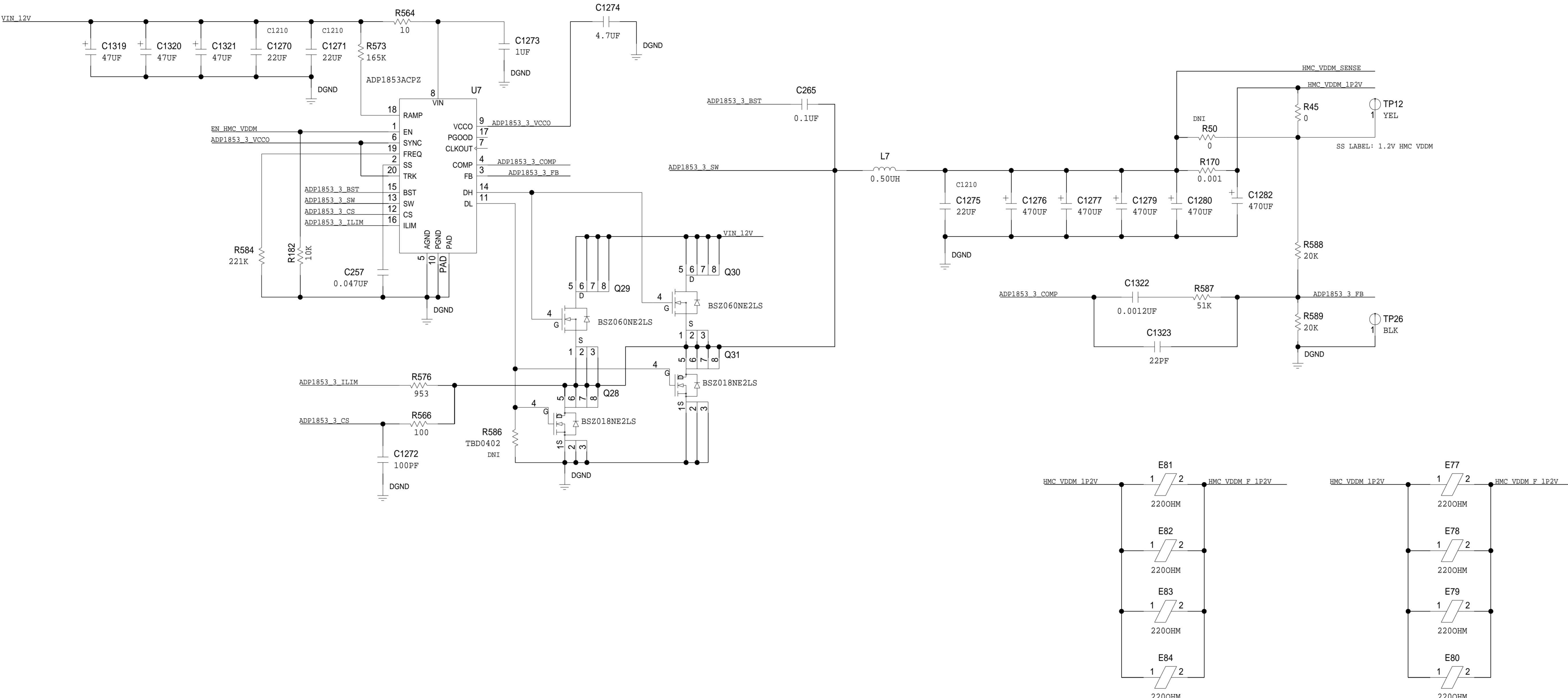
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HW TYPE : Customer Evaluation	Product(s) : N/A	REV E	
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THE EQUIPMENT SHOWN HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_045361	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 41 OF 52

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

POWER ADP1853 #3

HMC_VDDM, 1.2V, 20A



SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s): N/A
 : N/A

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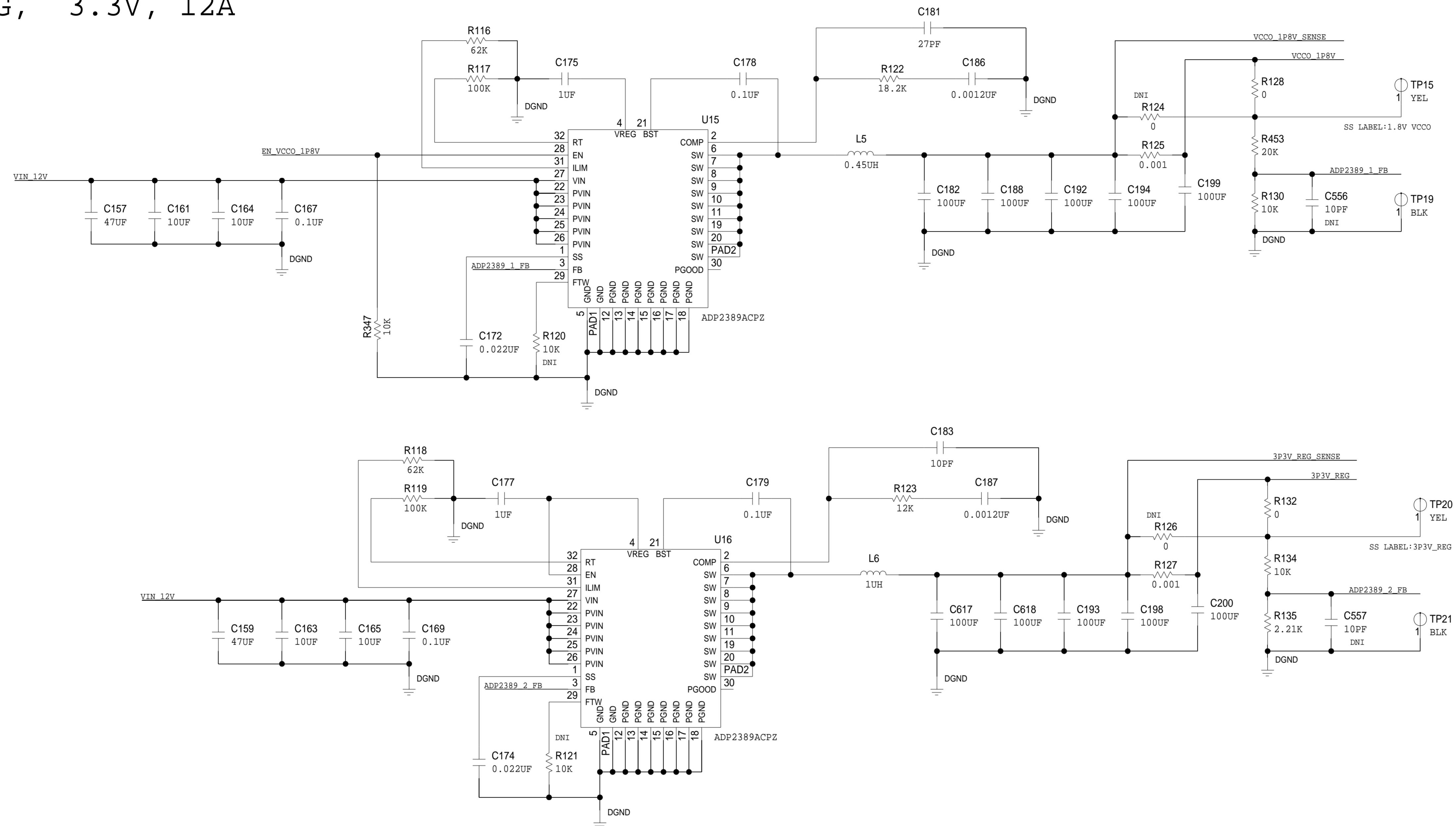
DRAWING NO.
 02_045361
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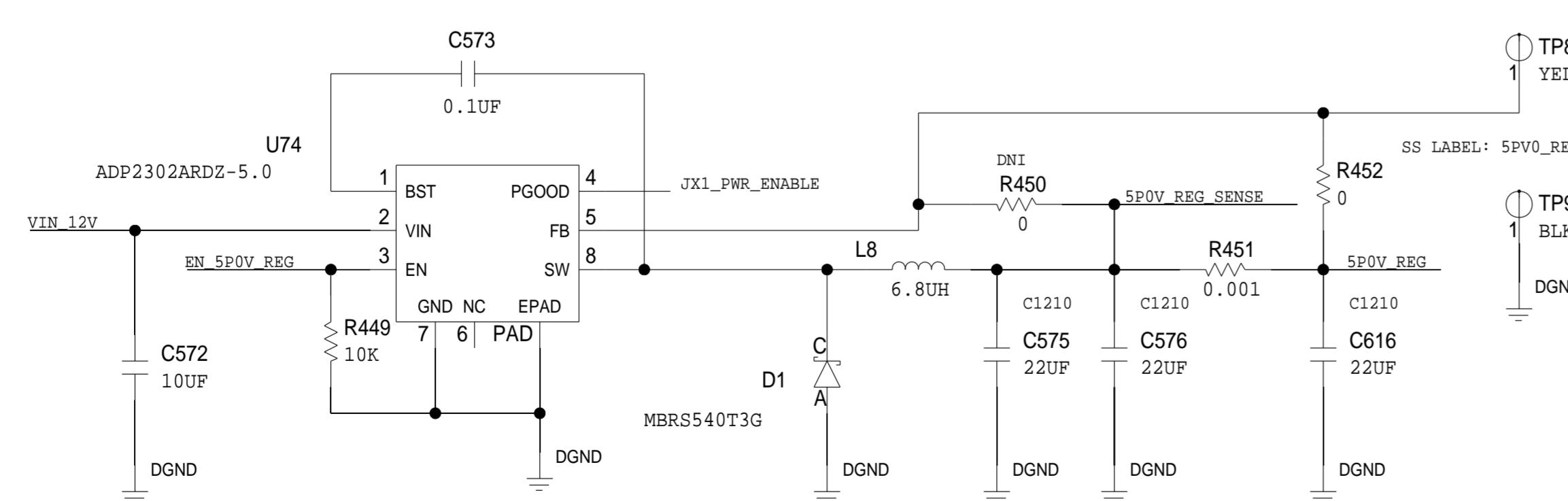
SIZE
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 SCALE
 1:1
 SHEET 42 OF 52

POWER ADP2389

VCCO_1P8V, 1.8V, 12A
3P3V_REG, 3.3V, 12A



MICROZED, 5.0V, 2A



SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): N/A
 : N/A

DESIGN
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	DRAWING NO.
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SIZE	SCALE

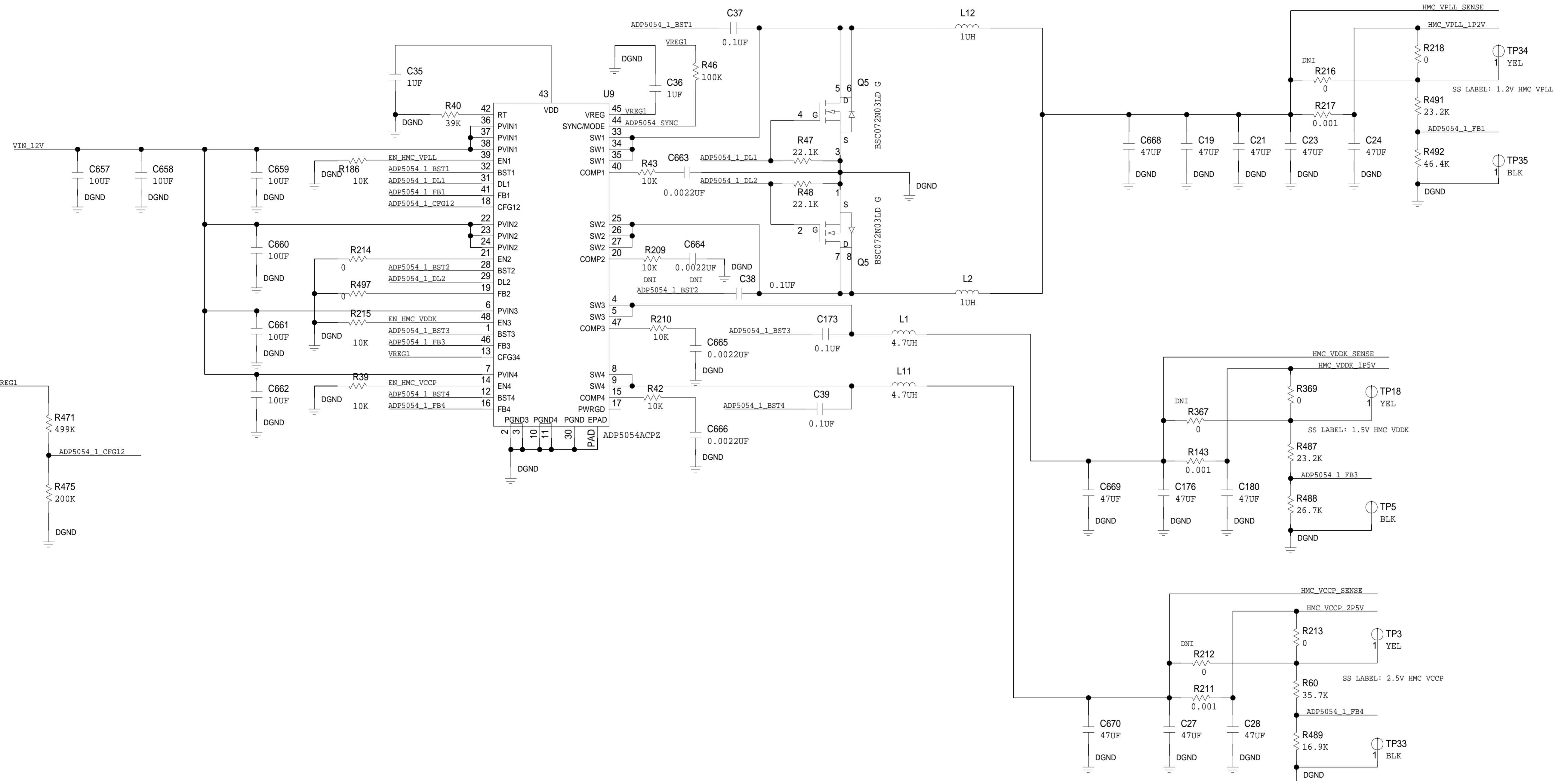
REV
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REVISIONS

REV	DESCRIPTION	DATE	APPROVED

POWER ADP5054 #1

HMC_VPLL, 1.2V, 10A
 HMC_VDDK, 1.5V, 1A
 HMC_VCCP, 2.5V, 1A



SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s) : N/A
 : N/A

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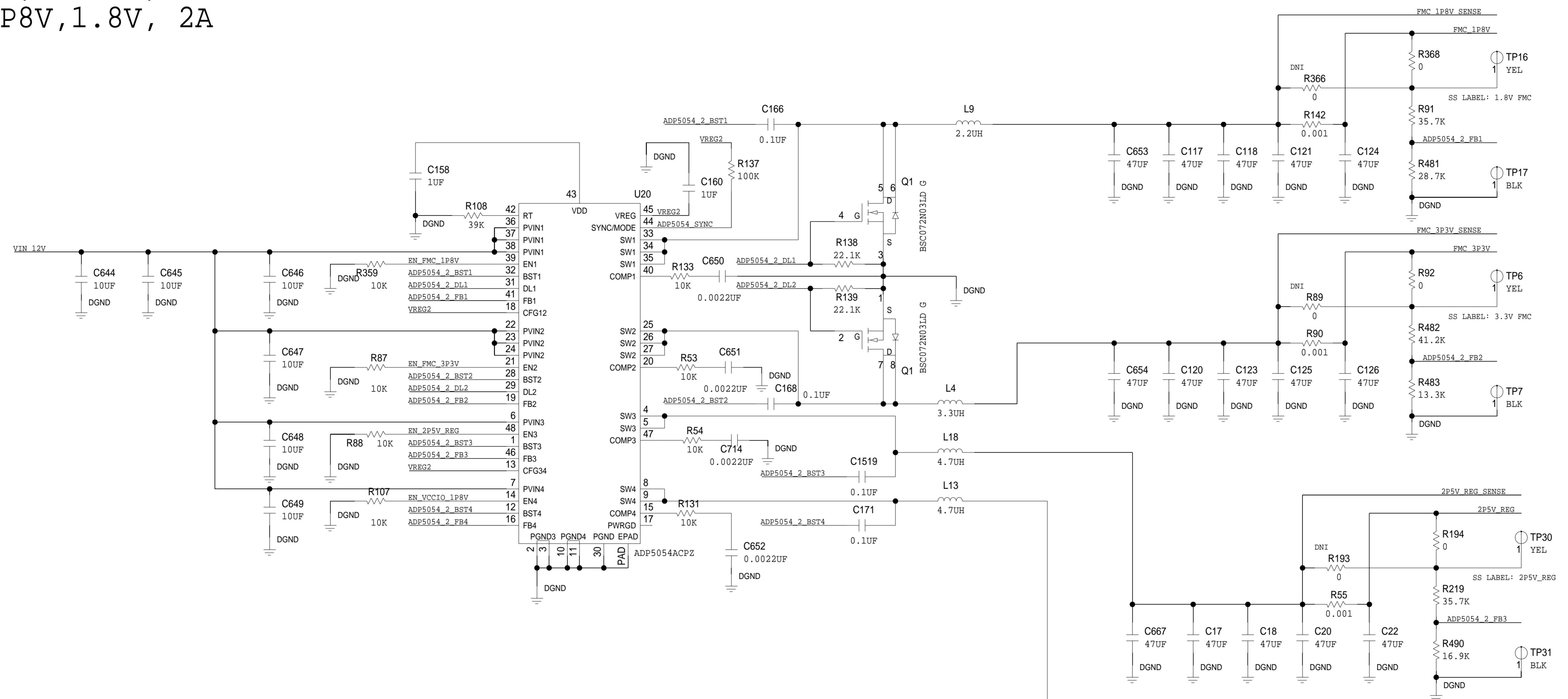
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SIZE
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 SHEET 44 OF 52

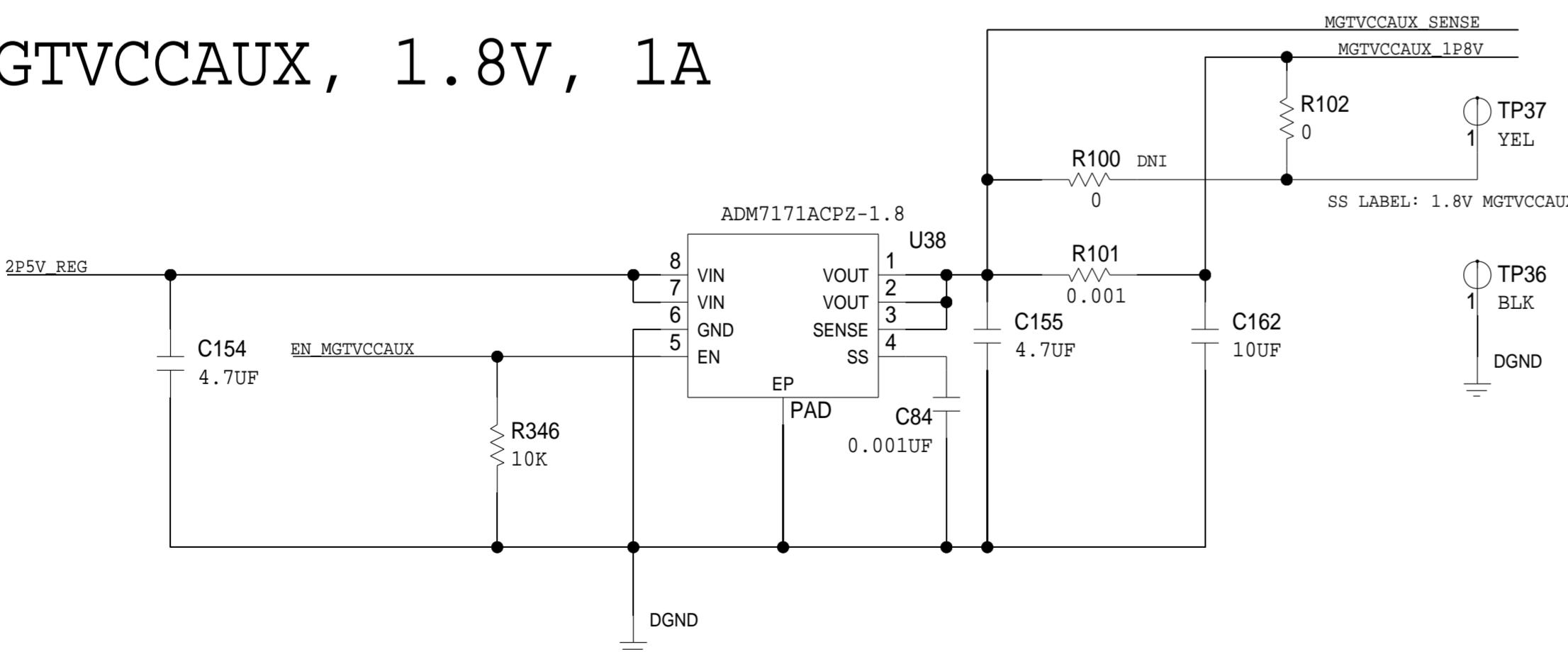
REV	DESCRIPTION	DATE	APPROVED

POWER ADP5054 #2

FMC_1P8V, 1.8V, 6A
 FMC_3P3V, 3.3V, 5A
 2P5V_REG, 2.5V, 1A
 VCCIO_1P8V, 1.8V, 2A



MGTVCVCAUX, 1.8V, 1A



SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s): N/A
 : N/A

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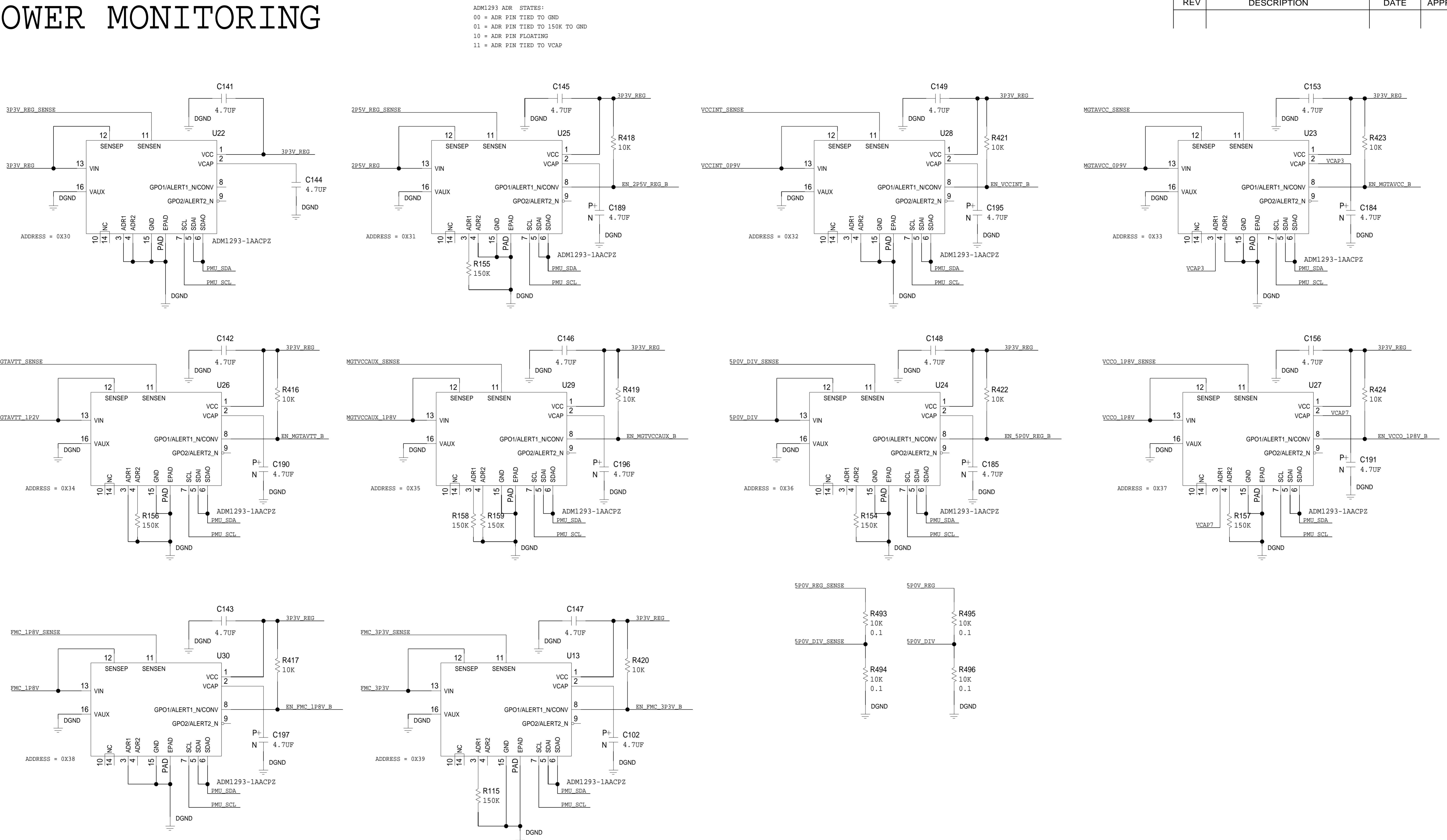
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SIZE
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 SCALE
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 SHEET 45 OF 52

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

POWER MONITORING



SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): N/A
: N/A

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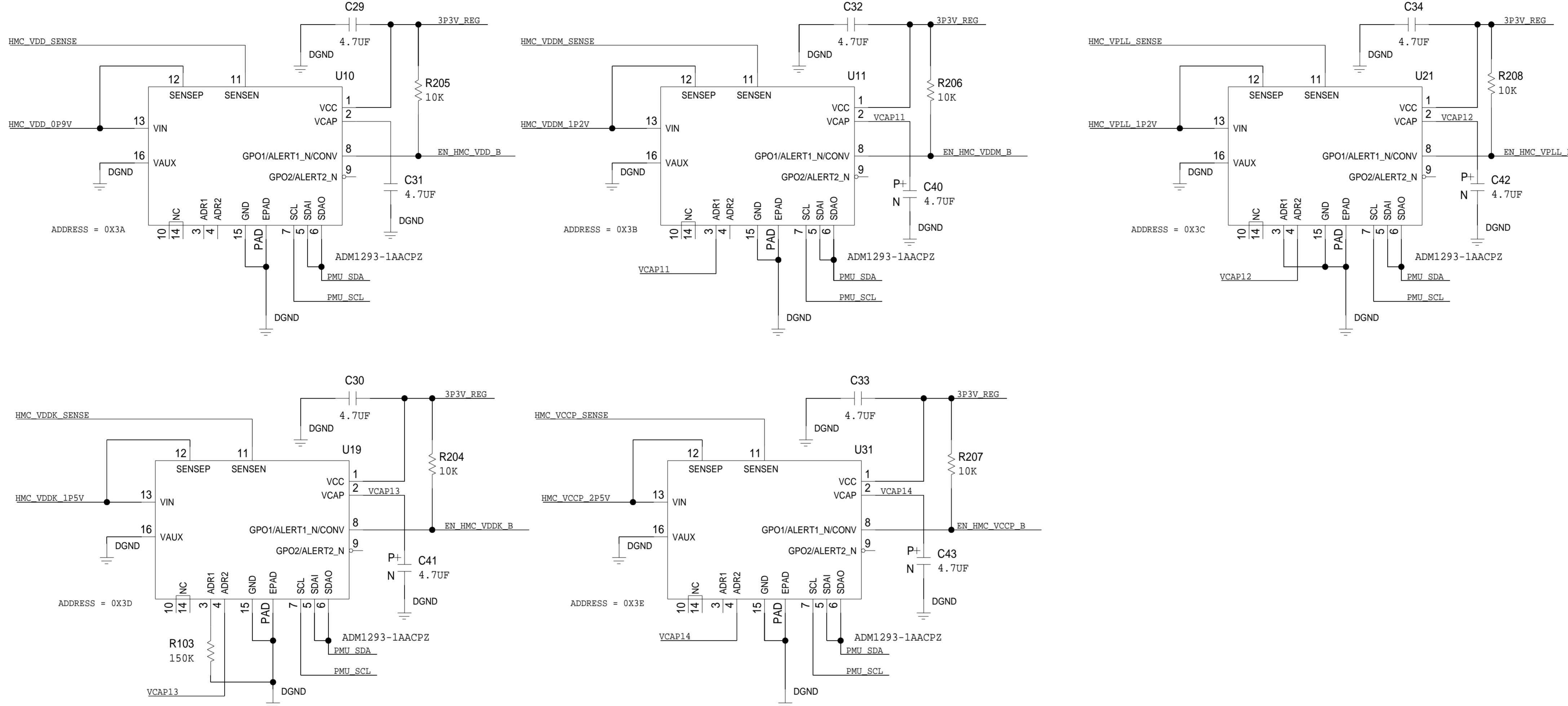
SIZE **D** SCALE 1:1 SHEET 46 OF 52

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

POWER MONITORING

ADM1293 ADR STATES:
 00 = ADR PIN TIED TO GND
 01 = ADR PIN TIED TO 150K TO GND
 10 = ADR PIN FLOATING
 11 = ADR PIN TIED TO VCAP



SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s): N/A
 : N/A

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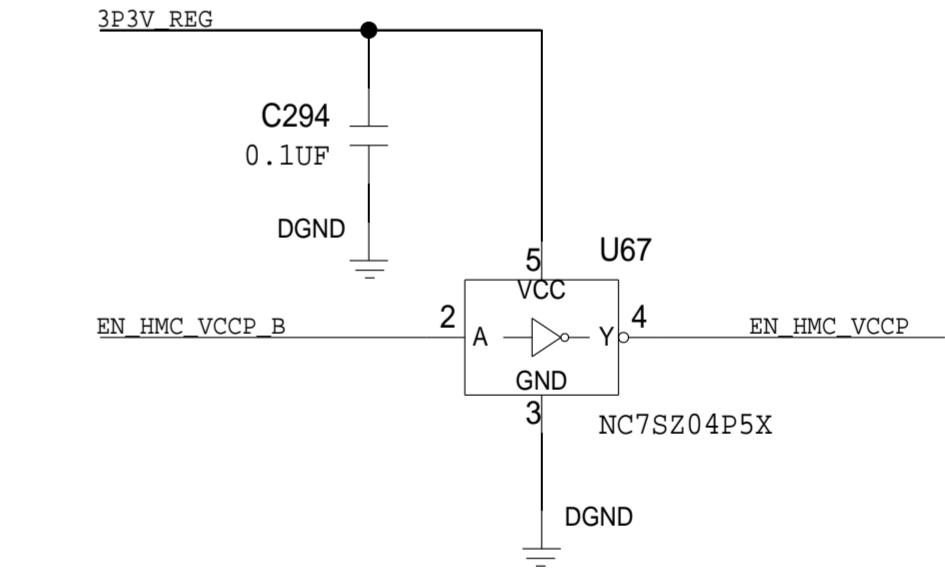
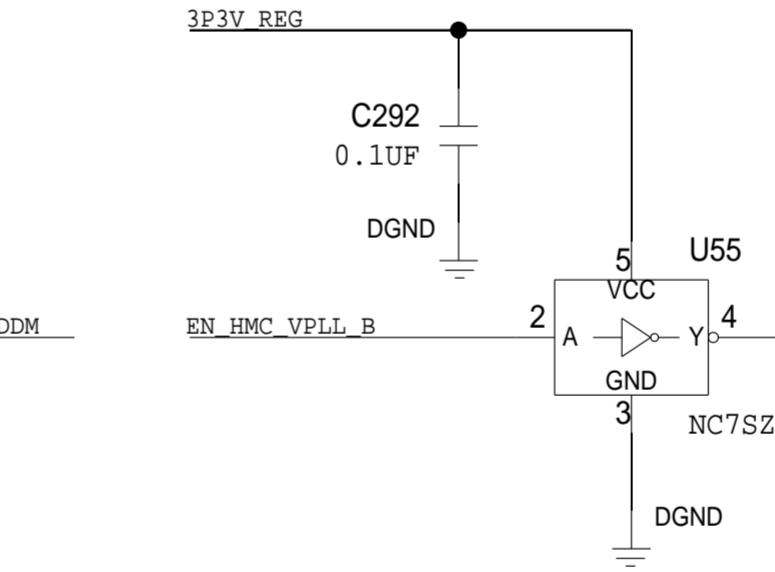
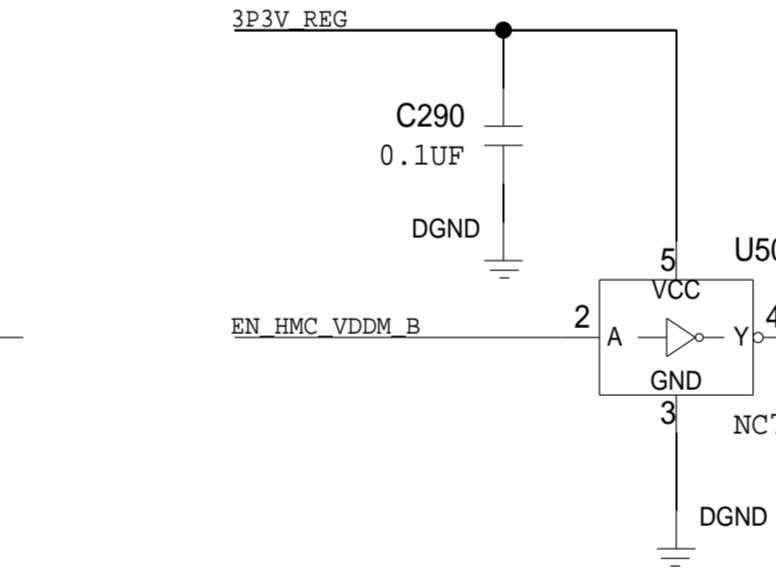
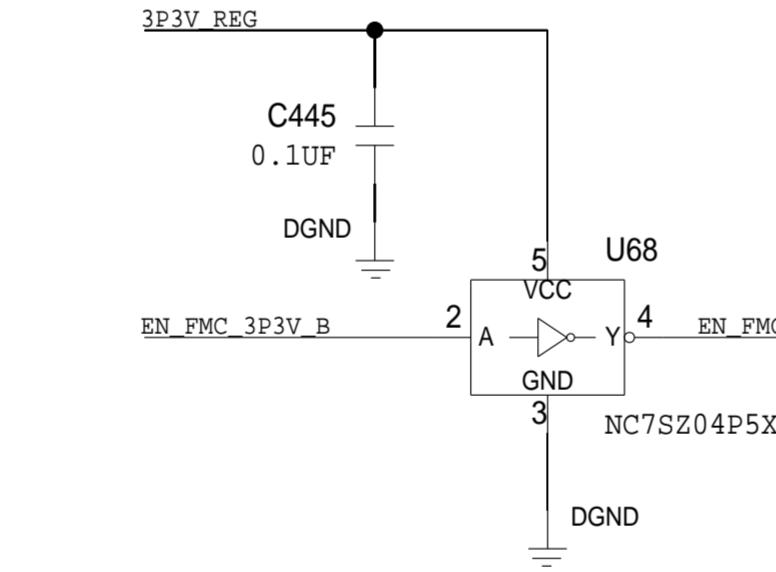
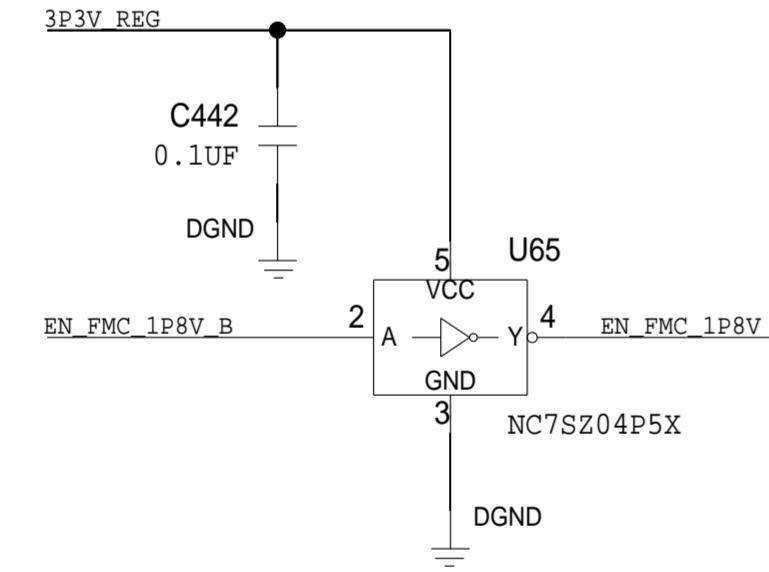
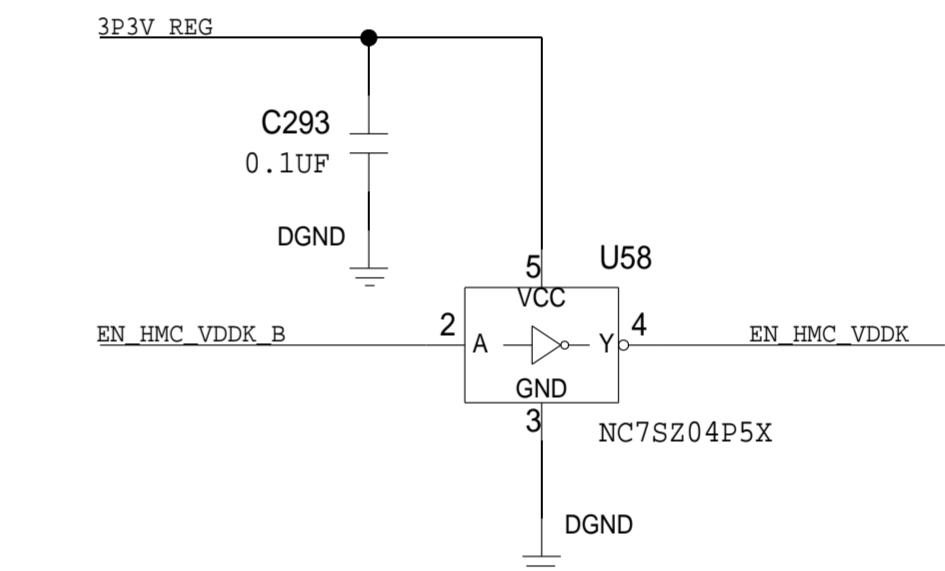
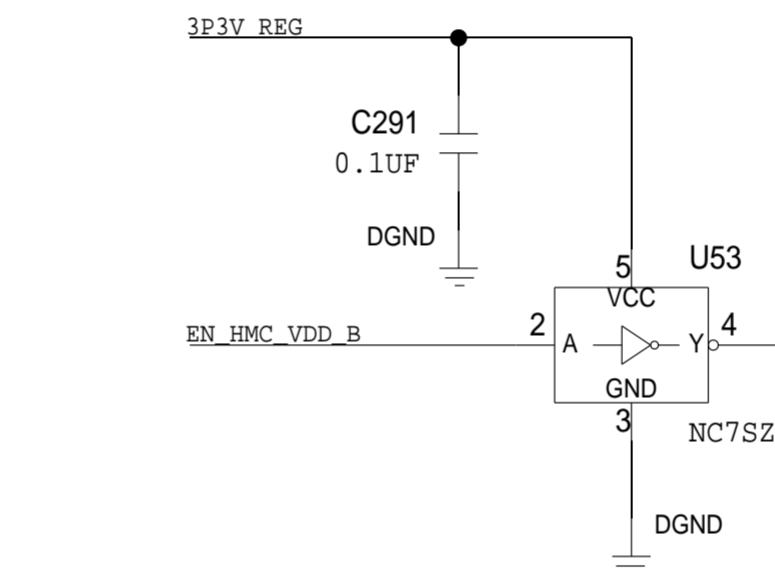
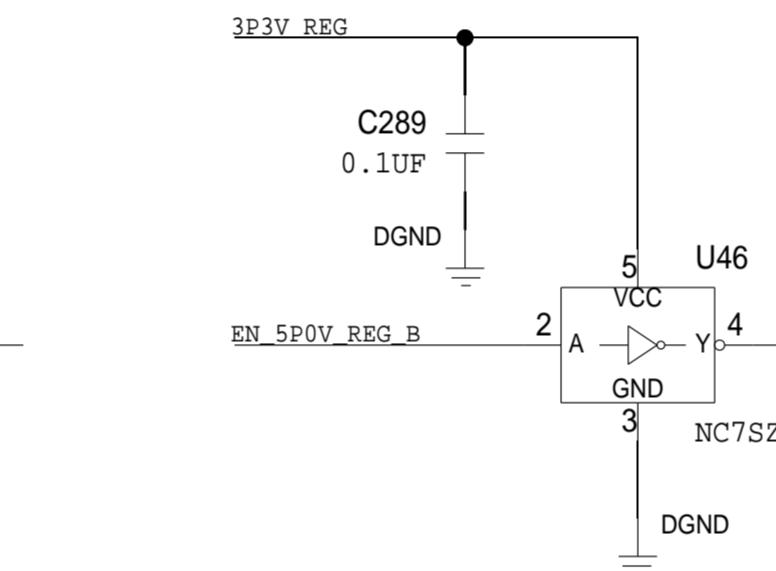
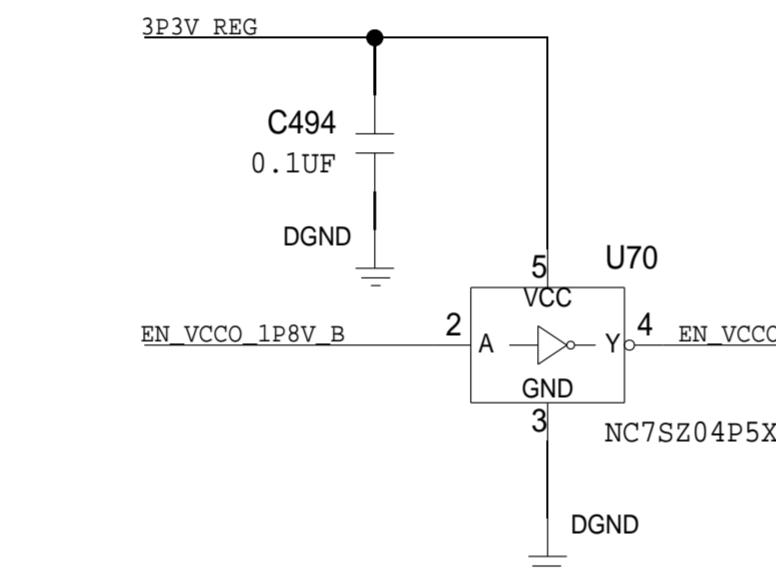
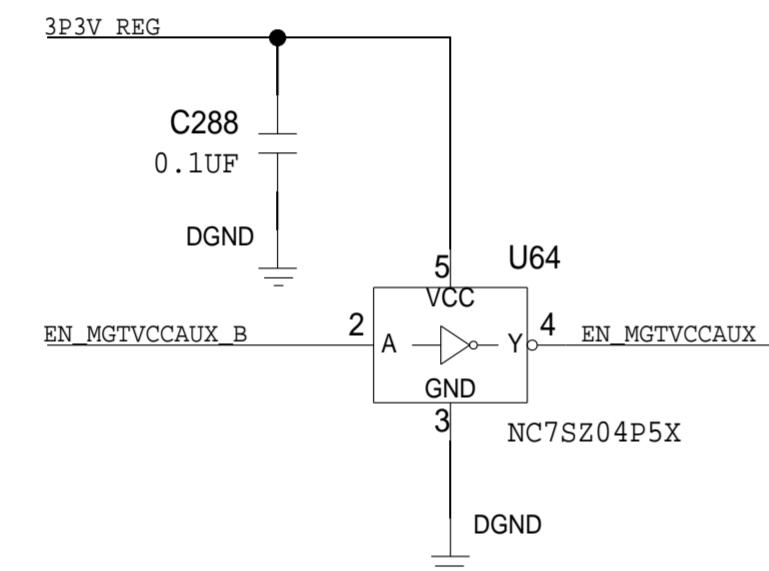
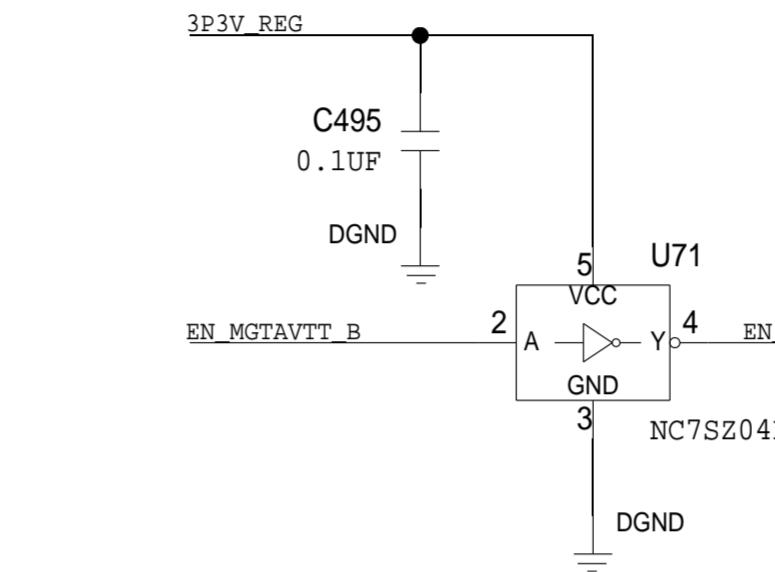
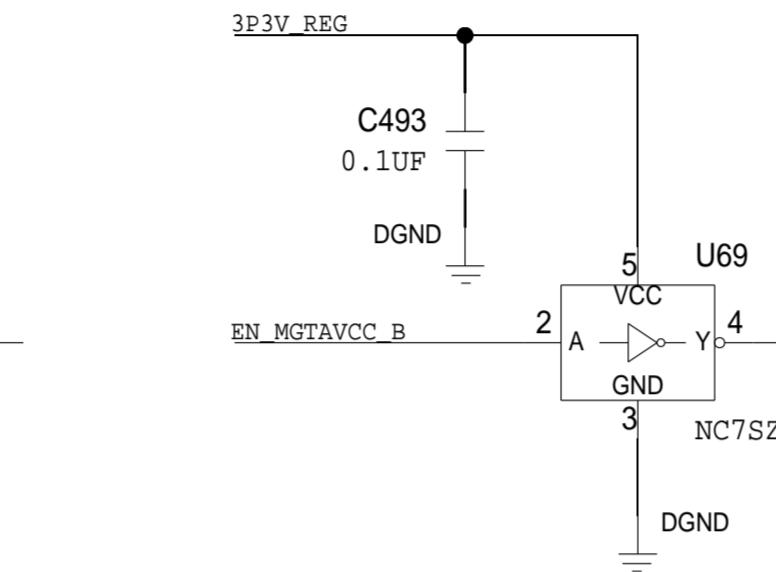
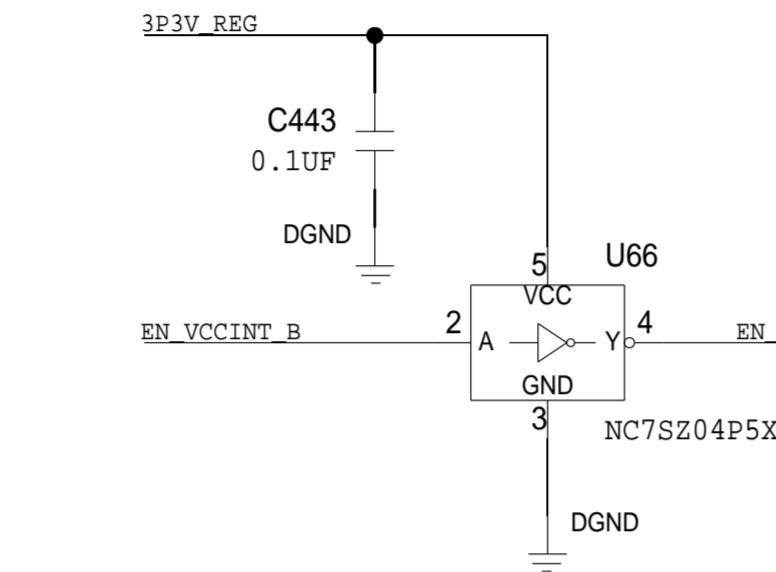
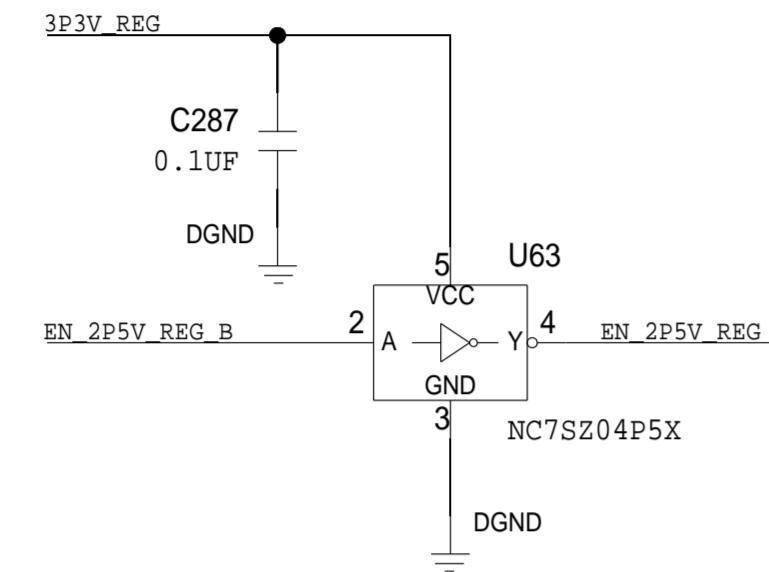
SIZE
 D
 SCALE
 1:1
 SHEET 47 OF 52

REVISI

REV	DESCRIPTION	DATE	APPROVED

POWER ENABLE INVERTERS

D



SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s): N/A
 : N/A

DESIGN VIEW
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DRAWING NO.
 02_045361

REV
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PTD ENGINEER
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SIZE
 D
 SCALE
 1:1
 SHEET 48 OF 52

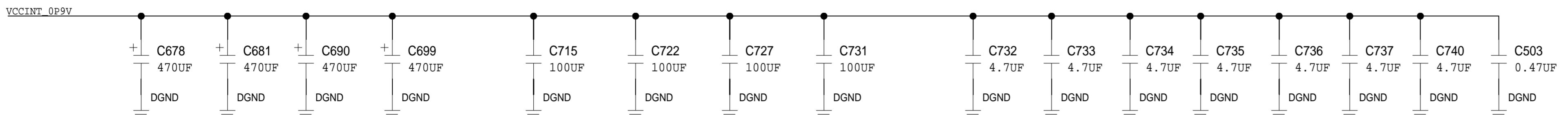
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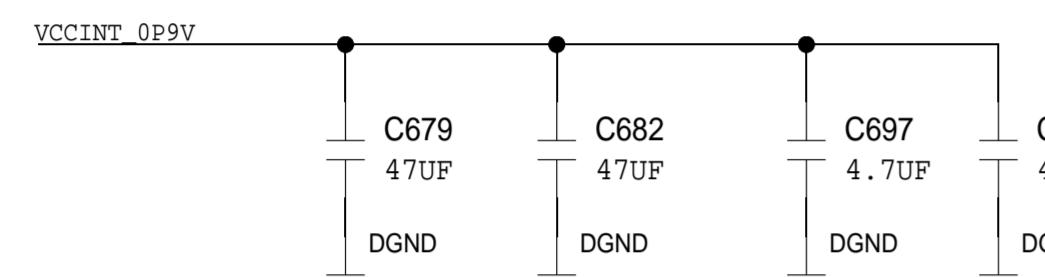
FPGA DECOUPLING

PLACE ALL CAPS AS CLOSE TO FPGA PINS AS POSSIBLE

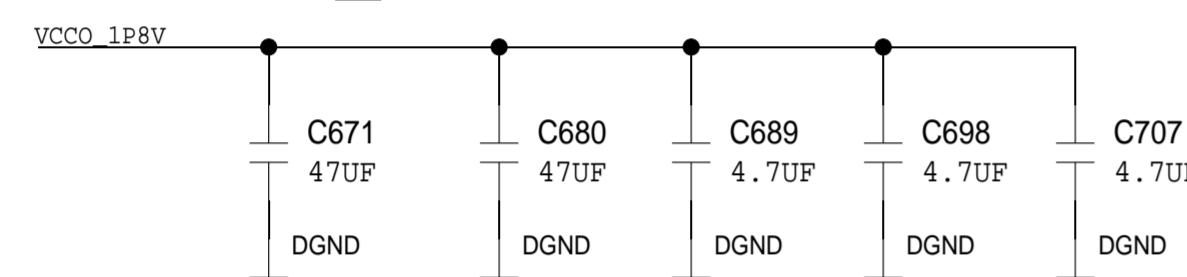
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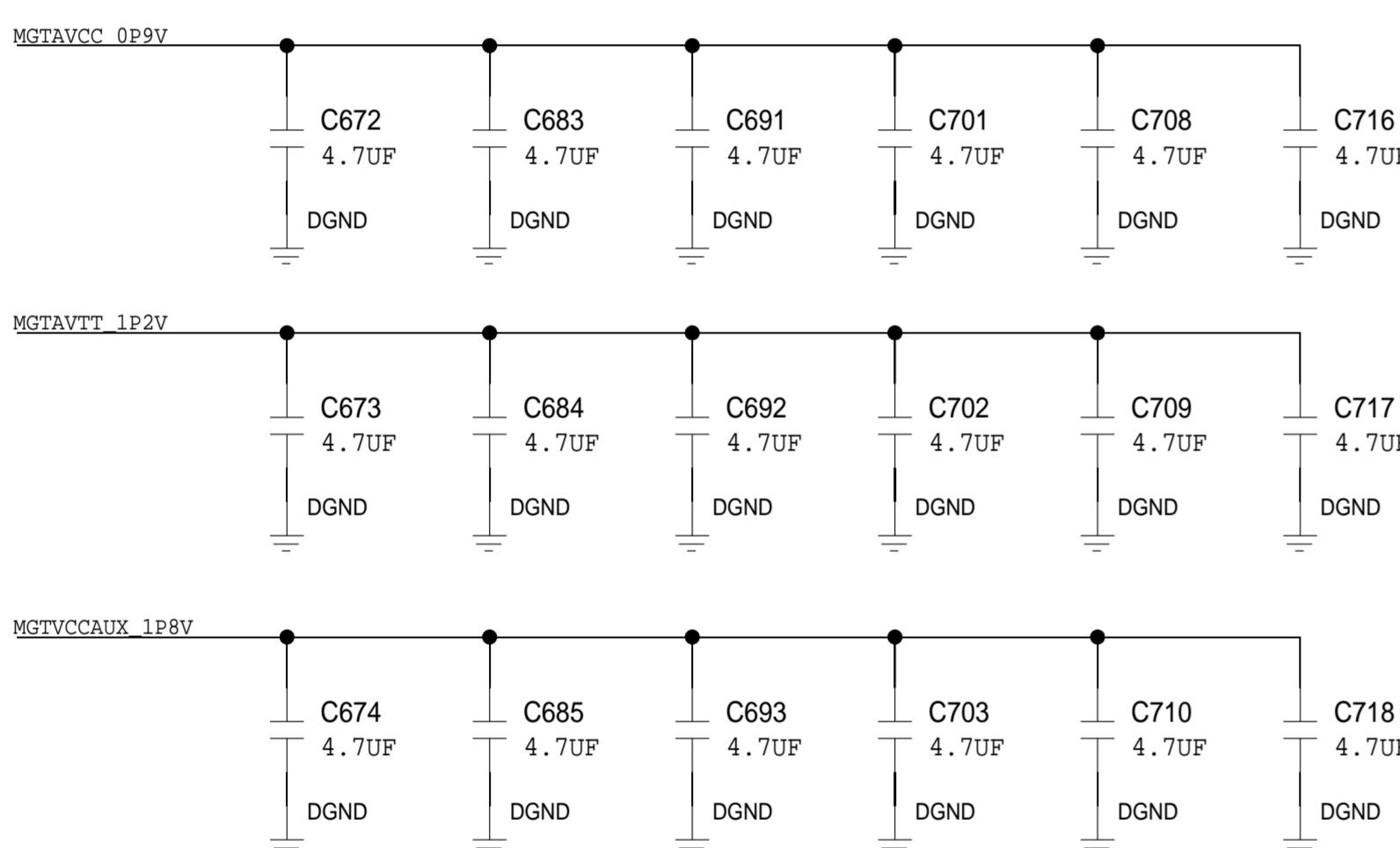
VCCBRAM



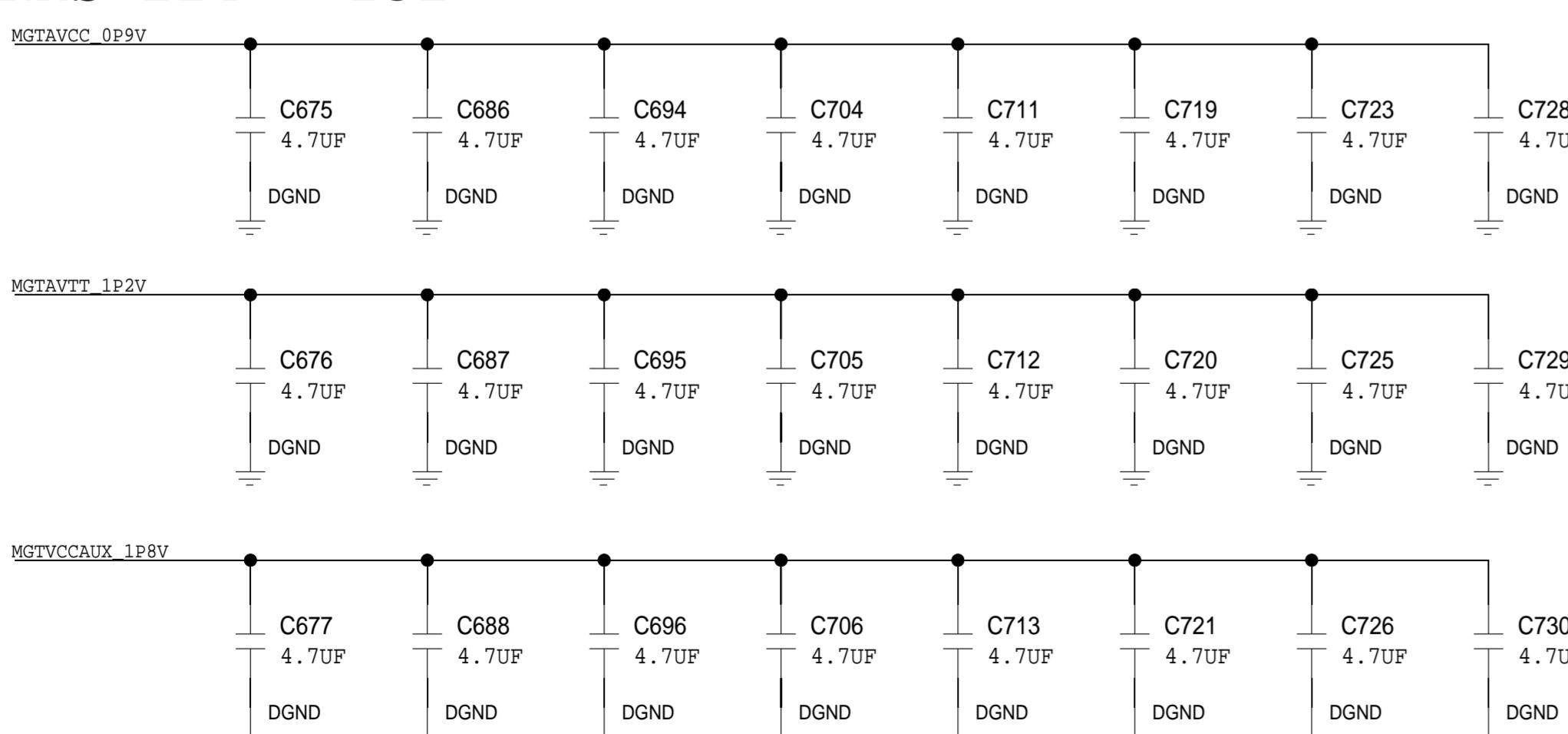
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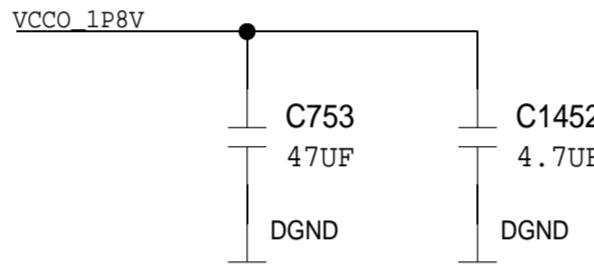
GTY BANKS 127 - 132



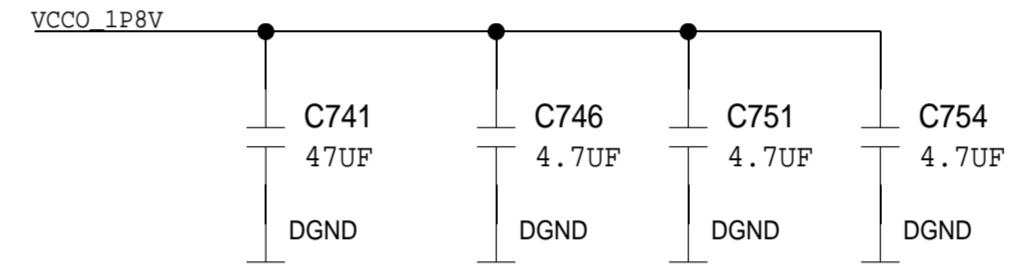
GTH BANKS 224 - 231



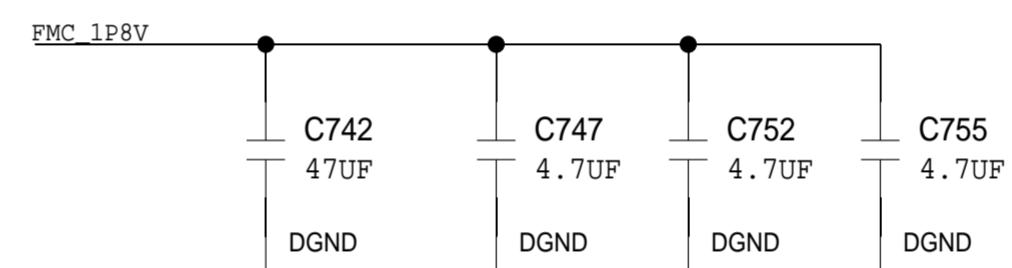
BANK 0



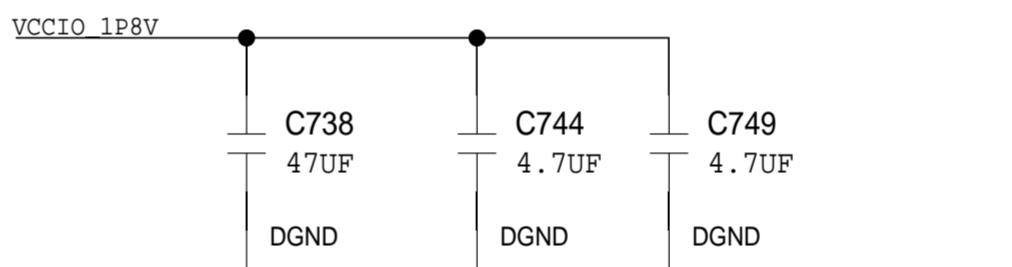
HP BANKS 64, 65, 70



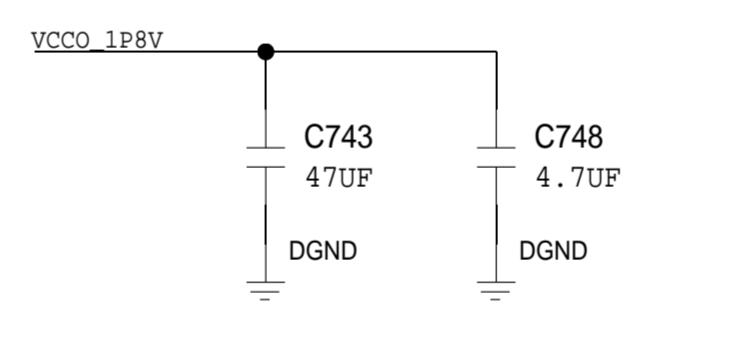
HP BANKS 67, 68, 69



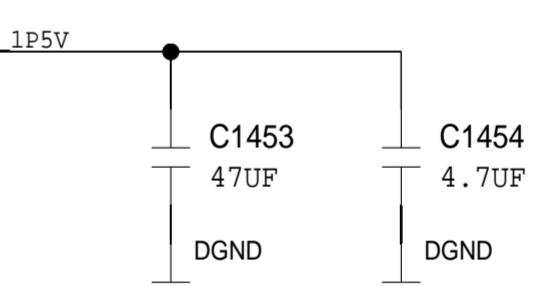
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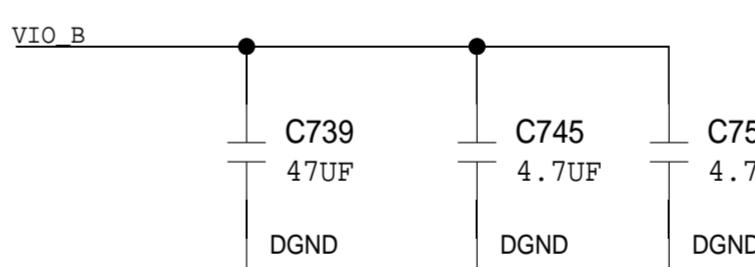
HD BANK 88



HD BANK 89



HD BANKS 90, 91

ANALOG
DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): N/A
: N/A

DESIGN VIEW
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DRAWING NO.
02_045361

REV
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PTD ENGINEER
<PTD_ENGINEER>

SIZE
D
SCALE
1:1
SHEET 49 OF 52

REVISI0NS

REV	DESCRIPTION	DATE	APPROVED

FPGA POWER AND DECOUPLING

D

D

C

C

→

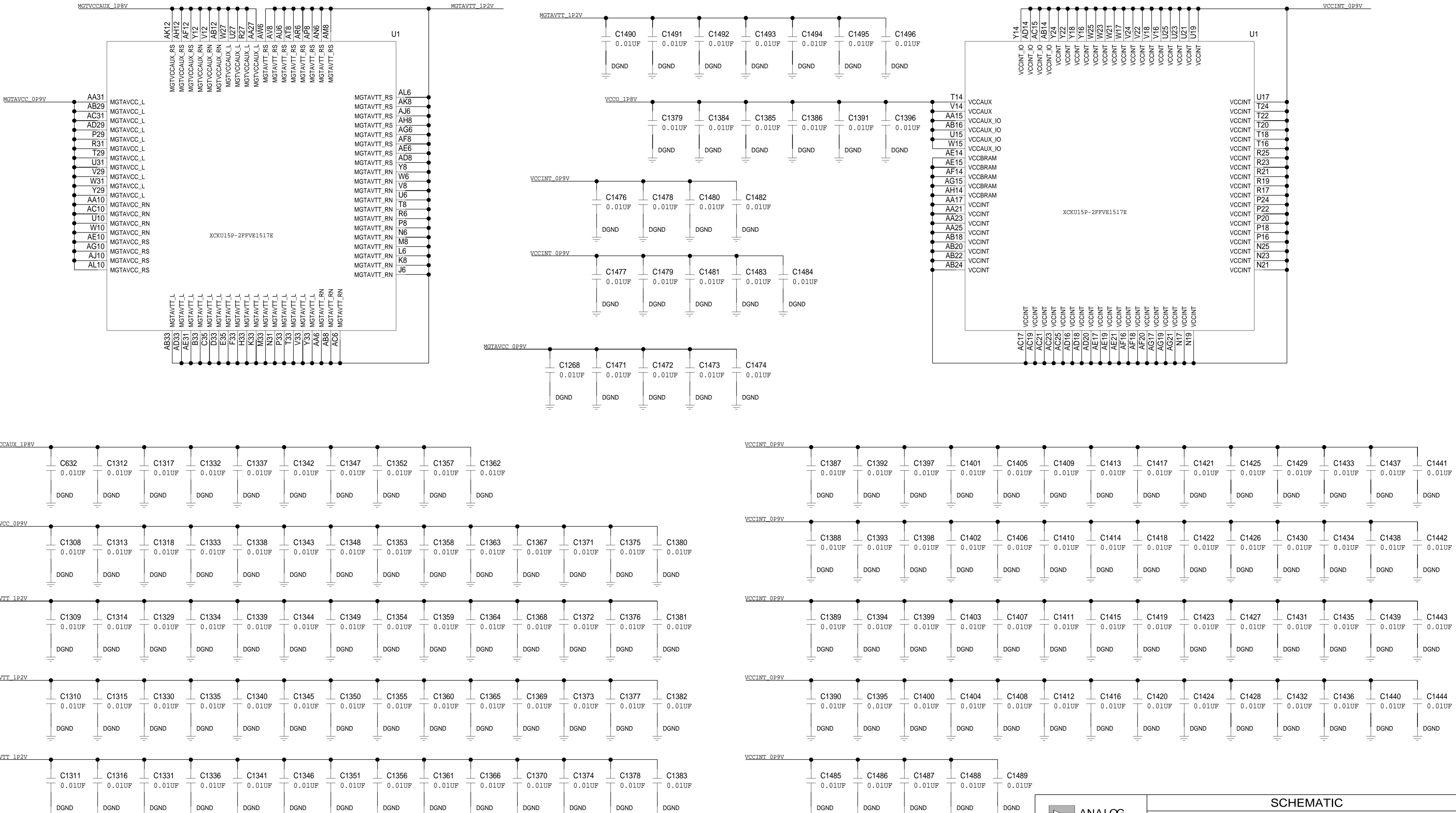
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B

B

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SCHEMATIC

HW TYPE : Customer Evaluation
 Product(s): N/A
 : N/A

DESIGN VIEW

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DRAWING NO.

02_045361

REV

E

PTD ENGINEER

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SIZE

1:1

SHEET

50 OF 52

FPGA GND

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

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D

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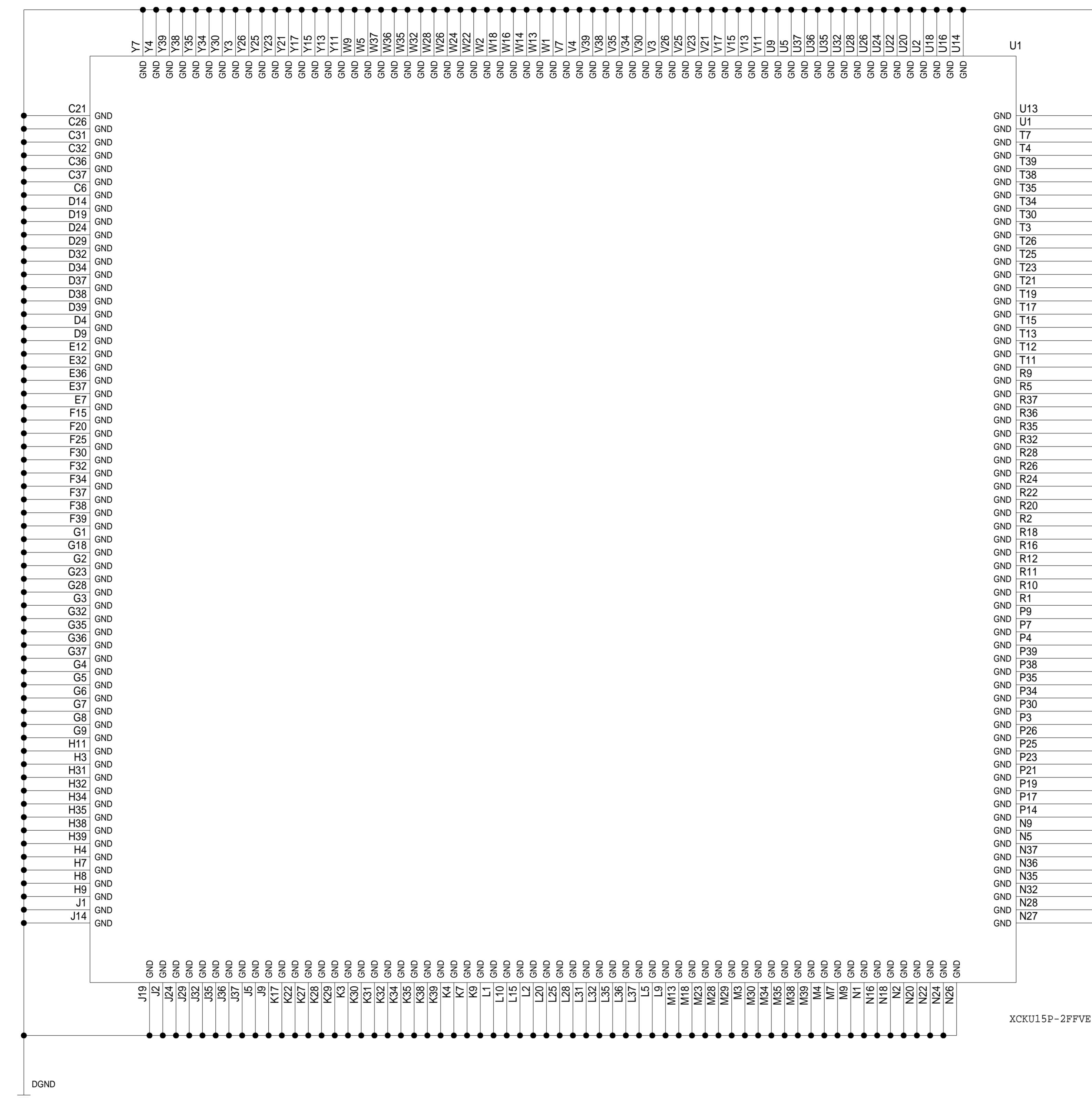
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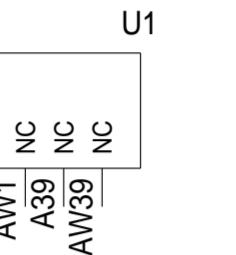
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FPGA SOCKET NC PINS



XCKU15P-2FFVE1517E

SCHEMATIC			
HW TYPE : Customer Evaluation	DESIGN VIEW	DRAWING NO.	REV
Product(s): N/A	<DESIGN_VIEW>	02_045361	E
: N/A			
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	<PTD_ENGINEER>	D	1:1
			SHEET 52 OF 52