European XFEL Cavity BPM plb46_to_iic_ mmap Data Sheet

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1 Introduction

For the European XFEL project a memory mapped IIC interface for the use with the 3.3 GHz cavity RFFE was developed. This board is controlled by two IIC buses available on the RFFE board. One is for the power management and identification of the board, the second for the RF functionality:

Power IIC:
The HotSwap controllers check the power consumption and the voltage levels on the RFFE, the adjacent EEPROM stores the identification of the board as well as the power on sequence.

RF IIC:
The second IIC bus controls the main functionality of the RFFE and the adjacent EEPROM is intended for calibration settings of the board.

The design shown here is used for both interfaces, but the first IIC is handled by the GPAC internally and not accessible directly through means of a memory mapped interface from the user. The second IIC however, is intended to be used by the control system and the GPAC internal processors. In order to allow several PLB masters access to the RFFE without interfering with a currently running request, a PLB component called PLB46_to_IIC_MMAP was placed in the BPM FPGAs.
This component provides a write FIFO interface to the IIC bus and a memory map of the data read from the IIC bus. The components can issue an individual interrupt for signaling completion of a particular request to a particular master. The component reads without master interaction after each bunch train particular IIC channels for quick access by the control system (e.g. temperatures, PLL lock indicators, etc.).

1.1 Purpose

The document here describes the firmware developed based on the schematic [2] of the RFFE.

1.2 Scope

This document provides a detailed overview of the firmware interface and specifies the user interface.

1.3 Definitions, acronyms, and abbreviations

This document is based on the “IEEE Recommended Practice for Software Requirements Specifications” [1].

ADC	Analog Digital Converter.
BPM	Beam Position Monitor
FPGA	Field Programmable Gate Array. Programmable logic device.

1.4 References

[1] IEEE Std 830-1998, Recommended Practice for Software Requirements Specifications.

[2] PSI 2012, RFFE schematic 3G3_Cavity_RFFE_V2R2prj.pdf
..\..\..\..\..\RFFE\04_Datasheet\01_Reference\EXFEL_Cavity_RFFE_120700B_r2.pdf

[3] Philips Semiconductors®, The I2C-bus specification Specification Version 2.1
01_Reference\I2C_Bus_specification.pdf

[4] Maxim Integrated® 2012, Datasheet MAX11617 and Texas Instruments® 2010, Datasheet LM62BIM3
..\..\..\..\..\RFFE\04_Datasheet\01_Reference\MAX11612-MAX11617.pdf
..\..\..\..\..\RFFE\04_Datasheet\01_Reference\lm62.pdf

[5] Texas Instruments® 2010, Datasheet DAC7678
..\..\..\..\..\RFFE\04_Datasheet\01_Reference\dac7678.pdf

[6] NXP® 2010, Datasheet SC18IS602/602B/603
..\..\..\..\..\RFFE\04_Datasheet\01_Reference\SC18IS602_602B_603.pdf

[7] Analog Devices® 2010, Datasheet AD9913
..\..\..\..\..\RFFE\04_Datasheet\01_Reference\AD9913.pdf

[8] Analog Devices® 2003, Datasheet ADF4001
..\..\..\..\..\RFFE\04_Datasheet\01_Reference\ADF4001.pdf

[9] Analog Devices® 2003, Datasheet ADF4107
..\..\..\..\..\RFFE\04_Datasheet\01_Reference\ADF4107.pdf

[10] NXP® 2010, Datasheet PCA9536
..\..\..\..\..\RFFE\04_Datasheet\01_Reference\PCA9536.pdf

[11] NXP® 2010, Datasheet PCA9555
..\..\..\..\..\RFFE\04_Datasheet\01_Reference\PCA9555.pdf

[12] Texas Instruments® 2005, Datasheet LM73
..\..\..\..\..\RFFE\04_Datasheet\01_Reference\lm73.pdf

[13] Microchip Technology Inc® 2005, Datasheet 24FC1025
..\..\..\..\..\RFFE\04_Datasheet\01_Reference\20001941L.pdf

1.5 Overview

Chapter 2 provides an overview and how the firmware is related to the other firmware used. Chapter 3 contains all the detail information on the interfaces.

2 Overall description

The RFFE [2] is a VME form factor board used for high frequency electronics for the cavity pickup.

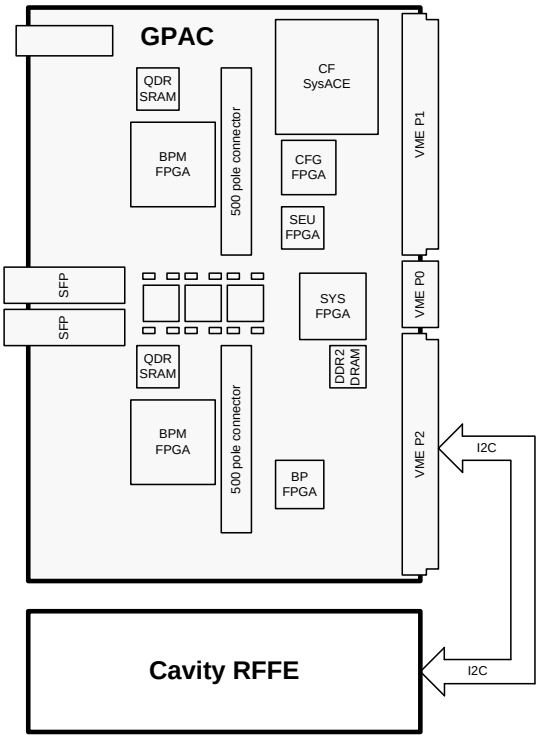

Figure 1: Board Overview

This board has a large variety of functions some of which are passive elements such as filters, splitters and amplifiers but also highly configurable components such as DACs (for phase shifting), PLLs, DDS, EEPROMs, switched attenuators (accounting for the beam charge), temperature sensors and feedback systems. The controllable chips are connected to one of the two IIC interfaces allowing the user to customize / adjust the board behavior. The advantage of the IIC bus is that the required clock for the chips is provided by the IIC master residing on the GPAC that is stopped during measurements of the beam data. There are also directly wired signals from the RFFE for intra-train control of the GPAC (e.g. a fast attenuator adjusts for high differences between set and measured beam charge) or power handling if a board is removed during operation.

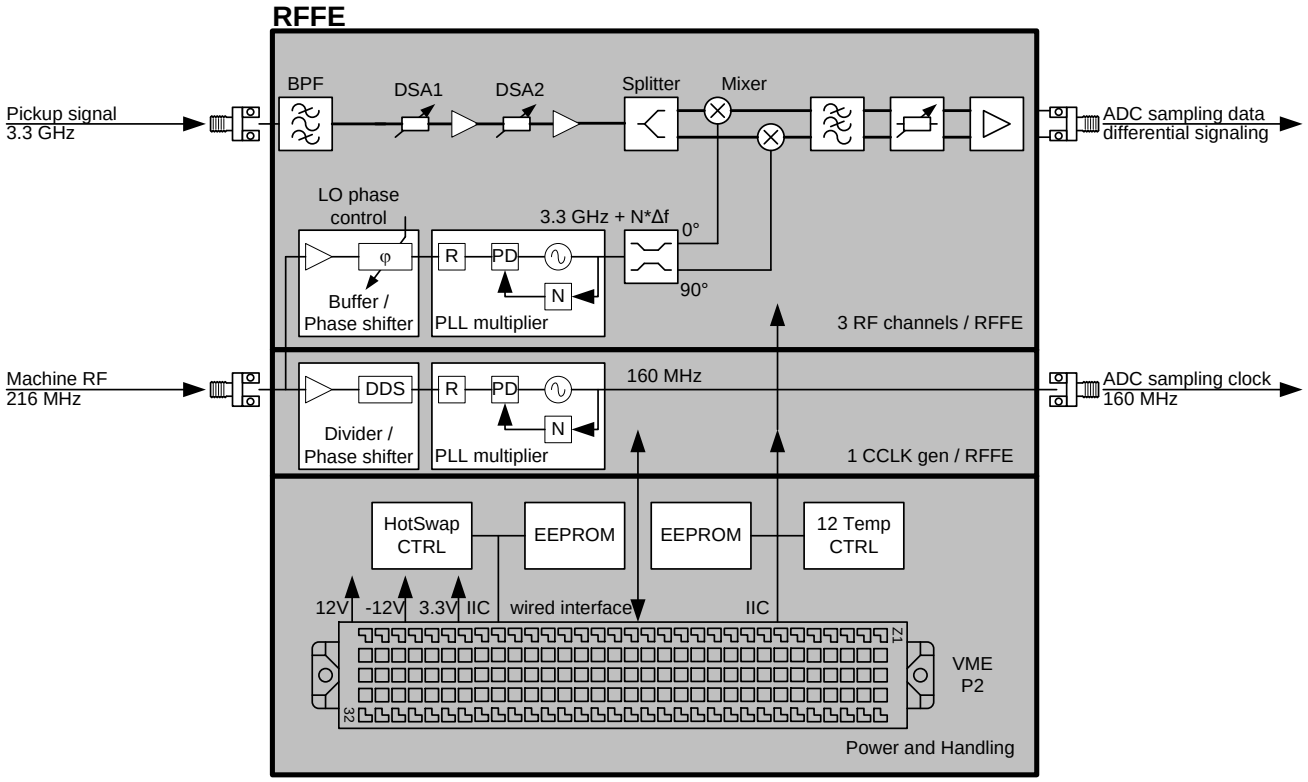

Figure 2: RFFE Board

The pickup signals (X, Y, REF) are attenuated and then mixed with a signal provided by a PLL that is locked to the machine RF (MREF). The ADC sampling clock is derived from the machine RF (MREF) by a DDS and cleaned by the PLL. Hence the ADC sampling clock and the position / reference signal are synchronized with each other. The IIC bus is used to setup the correct sampling frequency and to correct drifts by several feedback loops (temperature, sampling phase and I/Q phase feedbacks).

The PLB interface to the IIC is carried out in a generic way allowing several PLB masters to access the different functions independently i.e. providing the freedom to move the feedback loops locally or remotely in the BPM FPGA PPC, the SYS FPGA PPC or to the control system. Other features are: Keeping the request order (important for PLLs that require a specific register access order), requesting interrupts when IIC transfer has finished, local storing of the last access to a particular register on the RFFE and a feature to read specific functions (temperatures, status etc.) by an external trigger without software interaction.

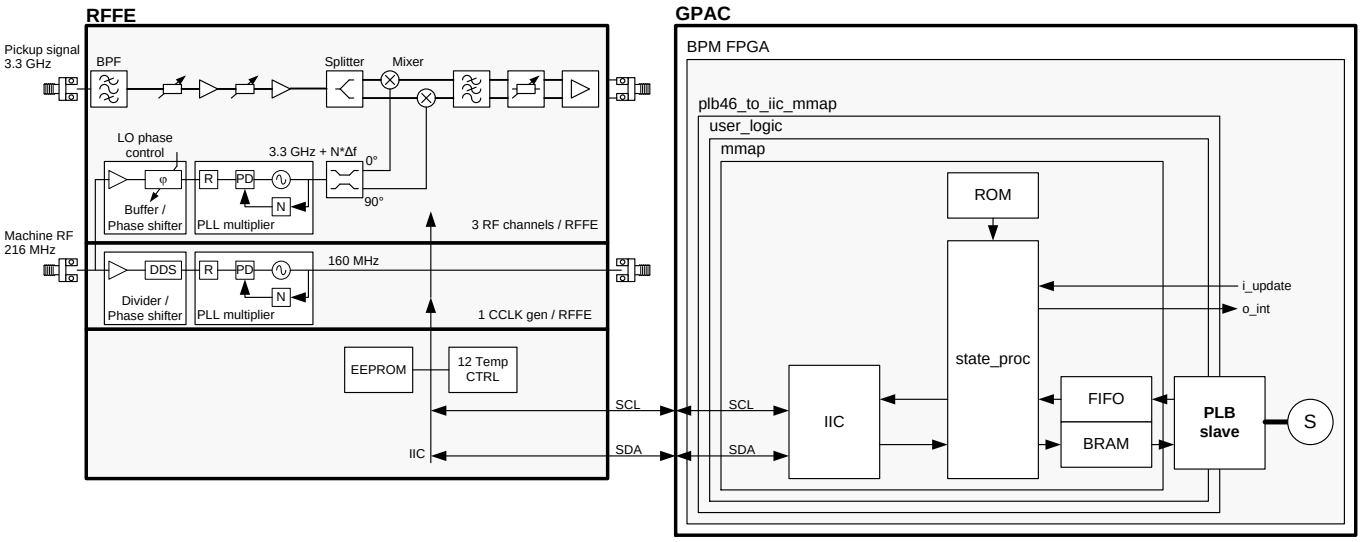

Figure 3: RFFE and GPAC Interconnect

If required, the user can write by PLB to a particular address (composed from interrupt request, read/write and index) into a FIFO. If the IIC is idle then the state machine reads the request from the FIFO (function address and eventually the data), obtains the access information from a ROM table (using the function address as index) and sends it over the IIC. On a read request the response from the RFFE is written into a BRAM showing to the user the last read access to the function address on the RFFE. If an interrupt was requested by the PLB master (also coded into the function address) then this interrupt is issued after the message was processed. If no further requests are in the FIFO then the IIC is idled until another request is found in the FIFO and the process repeats.
Another access to this firmware is by means of an external trigger (i_update). If an edge was found on this trigger then the state machine (state_proc) iterates trough the ROM searching for functions to be updated automatically and issues the needed IIC requests. Due to the storage of these requests the user benefits from not having to wait for completion of the individual requests but can access several function reads in a burst transfer.

3 Request composition

The PLB address, to which a user writes, forms the request on the IIC by looking up the IIC address and IIC Data Length by using the Index part of the PLB address in the ROM table. The read/write information is encoded into the PLB address and defines the read/write request bit of the IIC message [3].

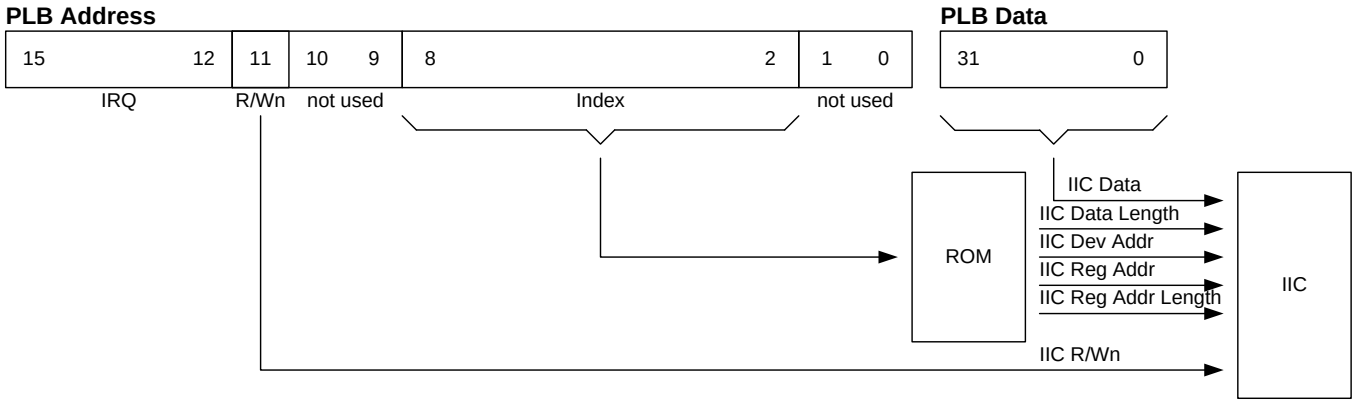

Figure 4: PLB Address Decomposition

A PLB read request reads from the BRAM, it does not issue an IIC message. Only a PLB write issues the forming of an IIC message and sends it over the bus to the RFFE.
This chapter is a summary and contains information from various datasheets [2…11]. For more information please refer to the schematic [2] of the RFFE and the relevant datasheets.

Address 8:0	R/W	Bit	Name	Description
0x000	R/W	7:0	TMP-CTRL	Temperature ADC MAX11617 [4] interface device address 0x35. Setup register, during initialization set to **0xA2**: BIT NAME DESCRIPTION 7 REG 1 = setup byte 6:4 SEL 010 = External reference and AIN11 is reference input 3 CLK 0 = internal clock 2 BIP/UNI 0 = unipolar. 1 RST 1 = no action 0 X 0 = Don't-care bit
0x004	R/W	15:0	R-MX-TMP-FBI	Mixer temperature measured by ADC MAX11617 [4] interface device address 0x35. Issue IIC request to read the R channel mixer temperature on AIN0 register address 0x61. The 16 bit value read has to be scaled by: (value – 61440)* 0.064103 - 30.769231 [degC]
0x008	R/W	15:0	R-RF-TMP-FBI	Attenuator temperature measured by ADC MAX11617 [4] interface device address 0x35. Issue IIC request to read the R channel attenuator temperature on AIN3 register address 0x67. The 16 bit value read has to be scaled by: (value – 61440)* 0.064103 - 30.769231 [degC]
0x00C	R/W	15:0	X-MX-TMP-FBI	Mixer temperature measured by ADC MAX11617 [4] interface device address 0x35. Issue IIC request to read the X channel mixer temperature on AIN1 register address 0x63. The 16 bit value read has to be scaled by:

				(value – 61440)* 0.064103 - 30.769231 [degC]
0x010	R/W	15:0	X-RF-TMP-FBI	Attenuator temperature measured by ADC MAX11617 [4] interface device address 0x35. Issue IIC request to read the X channel attenuator temperature on AIN4 register address 0x69. The 16 bit value read has to be scaled by: (value – 61440)* 0.064103 - 30.769231 [degC]
0x014	R/W	15:0	Y-MX-TMP-FBI	Mixer temperature measured by ADC MAX11617 [4] interface device address 0x35. Issue IIC request to read the Y channel mixer temperature on AIN2 register address 0x65. The 16 bit value read has to be scaled by: (value – 61440)* 0.064103 - 30.769231 [degC]
0x018	R/W	15:0	Y-RF-TMP-FBI	Attenuator temperature measured by ADC MAX11617 [4] interface device address 0x35. Issue IIC request to read the Y channel attenuator temperature on AIN5 register address 0x6B. The 16 bit value read has to be scaled by: (value – 61440)* 0.064103 - 30.769231 [degC]
0x01C	R/W	15:0	LO-TMP-FBI	Voltage ADC MAX11617 [4] interface device address 0x35. Issue IIC request to read the LO voltage on AIN6 register address 0x6D. The 16 bit value read has to be scaled by: (value – 61440)* 0.001 [V]
0x020	R/W	15:0	LO-PWR-I	Voltage ADC MAX11617 [4] interface device address 0x35. Issue IIC request to read the LO power proportional voltage on AIN7 register address 0x6F. The 16 bit value read has to be scaled by: (value – 61440)* 0.001 [V]
0x024	R/W	15:0	DET_DC	Voltage ADC MAX11617 [4] interface device address 0x35. Issue IIC request to read reference frequency voltage on AIN8 register address 0x71. The 16 bit value read has to be scaled by: (value – 61440)* 0.001 [V]
0x028	R/W	7:0	R-I-TMP-CFG	Temperature Sensor LM73 [12] configuration register address 0x01interface device address 0x4C. Issue IIC request to configure the R channel I component amplifier temperature. During initialization set to **0x40** BIT NAME DESCRIPTION 7 PD 0 = Power down not active 6 reserved 1 = recommended 5 ALERT Ena Don't-care because not used 4 ALERT Pol Don't-care because not used 3 One Shot Don't-care because not used 2:0 reserved 0 = recommended
0x02C	R/W	7:0	R-Q-TMP-CFG	Temperature Sensor LM73 [12] configuration register address 0x01interface device address 0x4A. Issue IIC request to configure the R channel Q component amplifier temperature. During initialization set to **0x40** BIT NAME DESCRIPTION 7 PD 0 = Power down not active 6 reserved 1 = recommended 5 ALERT Ena Don't-care because not used 4 ALERT Pol Don't-care because not used 3 One Shot Don't-care because not used

				2:0 reserved 0 = recommended
0x030	R/W	7:0	X-I-TMP-CFG	Temperature Sensor LM73 [12] configuration register address 0x01interface device address 0x49. Issue IIC request to configure the X channel I component amplifier temperature. During initialization set to **0x40** BIT NAME DESCRIPTION 7 PD 0 = Power down not active 6 reserved 1 = recommended 5 ALERT Ena Don't-care because not used 4 ALERT Pol Don't-care because not used 3 One Shot Don't-care because not used 2:0 reserved 0 = recommended
0x034	R/W	7:0	X-Q-TMP-CFG	Temperature Sensor LM73 [12] configuration register address 0x01interface device address 0x48. Issue IIC request to configure the X channel Q component amplifier temperature. During initialization set to **0x40** BIT NAME DESCRIPTION 7 PD 0 = Power down not active 6 reserved 1 = recommended 5 ALERT Ena Don't-care because not used 4 ALERT Pol Don't-care because not used 3 One Shot Don't-care because not used 2:0 reserved 0 = recommended
0x038	R/W	7:0	Y-I-TMP-CFG	Temperature Sensor LM73 [12] configuration register address 0x01interface device address 0x4D. Issue IIC request to configure the Y channel I component amplifier temperature. During initialization set to **0x40** BIT NAME DESCRIPTION 7 PD 0 = Power down not active 6 reserved 1 = recommended 5 ALERT Ena Don't-care because not used 4 ALERT Pol Don't-care because not used 3 One Shot Don't-care because not used 2:0 reserved 0 = recommended
0x03C	R/W	7:0	Y-Q-TMP-CFG	Temperature Sensor LM73 [12] configuration register address 0x01 interface device address 0x4E. Issue IIC request to configure the Y channel Q component amplifier temperature. During initialization set to **0x40** BIT NAME DESCRIPTION 7 PD 0 = Power down not active 6 reserved 1 = recommended 5 ALERT Ena Don't-care because not used 4 ALERT Pol Don't-care because not used 3 One Shot Don't-care because not used 2:0 reserved 0 = recommended
0x040	R/W	7:0	R-I-TMP-CTRL	Temperature Sensor LM73 [12] control/status register address 0x04 interface device address 0x4C. Issue IIC request to configure the R channel I component amplifier temperature. During initialization set to **0x60** BIT NAME DESCRIPTION 7 Time-Out 0 = Time-out not active 6:5 Resolution 11 = 0.03125°C/LSB 4 reserved 0 = recommended 3 ALERT Sta 0 = recommended 2 Temp Hi Don't-care because not used

				1 Temp Lo Don't-care because not used 0 Data avail 0 = recommended
0x044	R/W	7:0	R-Q-TMP-CTRL	Temperature Sensor LM73 [12] control/status register address 0x04 interface device address 0x4A. Issue IIC request to configure the R channel Q component amplifier temperature. During initialization set to **0x60** BIT NAME DESCRIPTION 7 Time-Out 0 = Time-out not active 6:5 Resolution 11 = 0.03125°C/LSB 4 reserved 0 = recommended 3 ALERT Sta 0 = recommended 2 Temp Hi Don't-care because not used 1 Temp Lo Don't-care because not used 0 Data avail 0 = recommended
0x048	R/W	7:0	X-I-TMP-CTRL	Temperature Sensor LM73 [12] control/status register address 0x04 interface device address 0x49. Issue IIC request to configure the X channel I component amplifier temperature. During initialization set to **0x60** BIT NAME DESCRIPTION 7 Time-Out 0 = Time-out not active 6:5 Resolution 11 = 0.03125°C/LSB 4 reserved 0 = recommended 3 ALERT Sta 0 = recommended 2 Temp Hi Don't-care because not used 1 Temp Lo Don't-care because not used 0 Data avail 0 = recommended
0x04C	R/W	7:0	X-Q-TMP-CTRL	Temperature Sensor LM73 [12] control/status register address 0x04 interface device address 0x48. Issue IIC request to configure the X channel Q component amplifier temperature. During initialization set to **0x60** BIT NAME DESCRIPTION 7 Time-Out 0 = Time-out not active 6:5 Resolution 11 = 0.03125°C/LSB 4 reserved 0 = recommended 3 ALERT Sta 0 = recommended 2 Temp Hi Don't-care because not used 1 Temp Lo Don't-care because not used 0 Data avail 0 = recommended
0x050	R/W	7:0	Y-I-TMP-CTRL	Temperature Sensor LM73 [12] control/status register address 0x04 interface device address 0x4D. Issue IIC request to configure the Y channel I component amplifier temperature. During initialization set to **0x60** BIT NAME DESCRIPTION 7 Time-Out 0 = Time-out not active 6:5 Resolution 11 = 0.03125°C/LSB 4 reserved 0 = recommended 3 ALERT Sta 0 = recommended 2 Temp Hi Don't-care because not used 1 Temp Lo Don't-care because not used 0 Data avail 0 = recommended
0x054	R/W	7:0	Y-Q-TMP-CTRL	Temperature Sensor LM73 [12] control/status register address 0x04 interface device address 0x4E. Issue IIC request to configure the Y channel Q component amplifier temperature. During initialization set to **0x60** BIT NAME DESCRIPTION

				7 Time-Out 0 = Time-out not active 6:5 Resolution 11 = 0.03125°C/LSB 4 reserved 0 = recommended 3 ALERT Sta 0 = recommended 2 Temp Hi Don't-care because not used 1 Temp Lo Don't-care because not used 0 Data avail 0 = recommended
0x058	R/W	7:0	R-I-TMP	Temperature Sensor LM73 [12] temperature register address 0x00 interface device address 0x4C. Issue IIC request to read the R channel I component amplifier temperature. The 16 bit value read has to be scaled by: value* 0.0078125 [°C]
0x05C	R/W	7:0	R-Q-TMP	Temperature Sensor LM73 [12] temperature register address 0x00 interface device address 0x4A. Issue IIC request to read the R channel Q component amplifier temperature. The 16 bit value read has to be scaled by: value* 0.0078125 [°C]
0x060	R/W	7:0	X-I-TMP	Temperature Sensor LM73 [12] temperature register address 0x00 interface device address 0x49. Issue IIC request to read the X channel I component amplifier temperature. The 16 bit value read has to be scaled by: value* 0.0078125 [°C]
0x064	R/W	7:0	X-Q-TMP	Temperature Sensor LM73 [12] temperature register address 0x00 interface device address 0x48. Issue IIC request to read the X channel Q component amplifier temperature. The 16 bit value read has to be scaled by: value* 0.0078125 [°C]
0x068	R/W	7:0	Y-I-TMP	Temperature Sensor LM73 [12] temperature register address 0x00 interface device address 0x4D. Issue IIC request to read the Y channel I component amplifier temperature. The 16 bit value read has to be scaled by: value* 0.0078125 [°C]
0x06C	R/W	7:0	Y-Q-TMP	Temperature Sensor LM73 [12] temperature register address 0x00 interface device address 0x4E. Issue IIC request to read the Y channel Q component amplifier temperature. The 16 bit value read has to be scaled by: value* 0.0078125 [°C]
0x080	R/W	15:0	DAC-INIT1	DAC 1 DAC7678 [5] Control register address 0x80 interface device address 0x4B. Issue IIC request to write to the Control register. During initialization set to **0x0000** BIT NAME DESCRIPTION 15:5 DB15:5 Don't-care bits 4 DB4 0 = Disable internal reference 3:0 DB3:0 Don't-care bits
0x084	R/W	15:0	DAC-INIT2	DAC 2 DAC7678 [5] Control register address 0x80 interface device address 0x4F. Issue IIC request to write to the Control register. During initialization set to **0x0000** BIT NAME DESCRIPTION 15:5 DB15:5 Don't-care bits 4 DB4 0 = Disable internal reference 3:0 DB3:0 Don't-care bits
0x088	R/W	15:0	R-MX-TMP-FBO	DAC 1 DAC7678 [5] interface device address 0x4B.

				Issue IIC request to access the R channel mixer temperature feedback set point by DAC channel A register address 0x30. The temperature (0…65 degC) has to be scaled to a 16 bit value by: (temperature + 30.7692) / 0.004006
0x08C	R/W	15:0	R-RF-TMP-FBO	DAC 1 DAC7678 [5] interface device address 0x4B. Issue IIC request to access the R channel attenuator temperature feedback set point by DAC channel D register address 0x33. The temperature (0…65 degC) has to be scaled to a 16 bit value by: (temperature + 30.7692) / 0.004006
0x090	R/W	15:0	X-MX-TMP-FBO	DAC 1 DAC7678 [5] interface device address 0x4B. Issue IIC request to access the X mixer temperature feedback set point by DAC channel B register address 0x31. The temperature (0…65 degC) has to be scaled to a 16 bit value by: (temperature + 30.7692) / 0.004006
0x094	R/W	15:0	X-RF-TMP-FBO	DAC 1 DAC7678 [5] interface device address 0x4B. Issue IIC request to access the X attenuator temperature feedback set point by DAC channel E register address 0x34. The temperature (0…65 degC) has to be scaled to a 16 bit value by: (temperature + 30.7692) / 0.004006
0x098	R/W	15:0	Y-MX-TMP-FBO	DAC 1 DAC7678 [5] interface device address 0x4B. Issue IIC request to access the Y channel mixer temperature feedback set point by DAC channel C register address 0x32. The temperature (0…65 degC) has to be scaled to a 16 bit value by: (temperature + 30.7692) / 0.004006
0x09C	R/W	15:0	Y-RF-TMP-FBO	DAC 1 DAC7678 [5] interface device address 0x4B. Issue IIC request to access the Y channel attenuator temperature feedback set point by DAC channel F register address 0x35. The temperature (0…65 degC) has to be scaled to a 16 bit value by: (temperature + 30.7692) / 0.004006
0x0A0	R/W	15:0	LO-TMP-FBO	DAC 1 DAC7678 [5] interface device address 0x4B. Issue IIC request to access the LO power feedback set point by DAC channel G register address 0x36. The voltage (0…3.3 V) has to be scaled to a 16 bit value by: voltage / 0.0000625
0x0A4	R/W	15:0	LO-PHASE	DAC 2 DAC7678 [5] interface device address 0x4F. Issue IIC request to access the LO phase shifter set point by DAC channel A register address 0x30. The voltage (0…4 V) has to be scaled to a 16 bit value by: voltage / 0.0000625
0x0A8	R/W	15:0	LO-PWR-O	DAC 2 DAC7678 [5] interface device address 0x4F. Issue IIC request to access the LO power set point by DAC channel B register address 0x31. The voltage (0…4 V) has to be scaled to a 16 bit value by: voltage / 0.0000625

0x0C8	R/W	7:0	R-ATT-O0	GPIO PCA9555 [11] output port 0 register address 0x02 interface device address 0x20. R channel R-DSA1 attenuator setting. The attenuator (0.5…31.5 dB) has to be scaled to a 8 bit value by: All bits inverted(attenuator * 4)
0x0CC	R/W	7:0	R-ATT-O1	GPIO PCA9555 [11] output port 1 register address 0x03 interface device address 0x20. R channel R-DSA2 attenuator setting. The attenuator (0.5…31.5 dB) has to be scaled to a 8 bit value by: All bits inverted(attenuator * 4)
0x0D0	R/W	7:0	R-ATT-P0	GPIO PCA9555 [11] input polarity port 0 register address 0x04 interface device address 0x20. R channel R-DSA1 attenuator polarity setting. During initialization set to **0x00** BIT NAME DESCRIPTION 7:0 N0.7:N0.0 0x00 = Input polarity retained
0x0D4	R/W	7:0	R-ATT-P1	GPIO PCA9555 [11] input polarity port 1 register address 0x05 interface device address 0x20. R channel R-DSA2 attenuator polarity setting. During initialization set to **0x00** BIT NAME DESCRIPTION 7:0 N1.7:N1.0 0x00 = Input polarity retained
0x0D8	R/W	7:0	R-ATT-C0	GPIO PCA9555 [11] configuration register port 0 register address 0x06 interface device address 0x20. R channel R-DSA1 attenuator configuration setting. During initialization set to **0x00** BIT NAME DESCRIPTION 7:0 C0.7:C0.0 0x00 = Output enabled
0x0DC	R/W	7:0	R-ATT-C1	GPIO PCA9555 [11] configuration register port 1 register address 0x07 interface device address 0x20. R channel R-DSA2 attenuator configuration setting. During initialization set to **0x00** BIT NAME DESCRIPTION 7:0 C1.7:C1.0 0x00 = Output enabled
0x0E8	R/W	7:0	X-ATT-O0	GPIO PCA9555 [11] output port 0 register address 0x02 interface device address 0x21. X channel X-DSA1 attenuator setting. The attenuator (0.5…31.5 dB) has to be scaled to a 8 bit value by: All bits inverted(attenuator * 4)
0x0EC	R/W	7:0	X-ATT-O1	GPIO PCA9555 [11] output port 1 register address 0x03 interface device address 0x21. X channel X-DSA2 attenuator setting. The attenuator (0.5…31.5 dB) has to be scaled to a 8 bit value by: All bits inverted(attenuator * 4)
0x0F0	R/W	7:0	X-ATT-P0	GPIO PCA9555 [11] input polarity port 0 register address 0x04 interface device address 0x21. X channel X-DSA1 attenuator polarity setting. During initialization set to **0x00** BIT NAME DESCRIPTION 7:0 N0.7:N0.0 0x00 = Input polarity retained
0x0F4	R/W	7:0	X-ATT-P1	GPIO PCA9555 [11] input polarity port 1 register address 0x05 interface device address 0x21. X channel X-DSA2 attenuator polarity setting. During initialization set to **0x00** BIT NAME DESCRIPTION 7:0 N1.7:N1.0 0x00 = Input polarity retained

0x0F8	R/W	7:0	X-ATT-C0	GPIO PCA9555 [11] configuration register port 0 register address 0x06 interface device address 0x21. X channel X-DSA1 attenuator configuration setting. During initialization set to **0x00** BIT NAME DESCRIPTION 7:0 C0.7:C0.0 0x00 = Output enabled
0x0FC	R/W	7:0	X-ATT-C1	GPIO PCA9555 [11] configuration register port 1 register address 0x07 interface device address 0x21. X channel X-DSA2 attenuator configuration setting. During initialization set to **0x00** BIT NAME DESCRIPTION 7:0 C1.7:C1.0 0x00 = Output enabled
0x108	R/W	7:0	Y-ATT-O0	GPIO PCA9555 [11] output port 0 register address 0x02 interface device address 0x21. Y channel Y-DSA1 attenuator setting. The attenuator (0.5…31.5 dB) has to be scaled to a 8 bit value by: All bits inverted(attenuator * 4)
0x10C	R/W	7:0	Y-ATT-O1	GPIO PCA9555 [11] output port 1 register address 0x03 interface device address 0x21. Y channel Y-DSA2 attenuator setting. The attenuator (0.5…31.5 dB) has to be scaled to a 8 bit value by: All bits inverted(attenuator * 4)
0x110	R/W	7:0	Y-ATT-P0	GPIO PCA9555 [11] input polarity port 0 register address 0x04 interface device address 0x21. Y channel Y-DSA1 attenuator polarity setting. During initialization set to **0x00** BIT NAME DESCRIPTION 7:0 N0.7:N0.0 0x00 = Input polarity retained
0x114	R/W	7:0	Y-ATT-P1	GPIO PCA9555 [11] input polarity port 1 register address 0x05 interface device address 0x21. Y channel Y-DSA2 attenuator polarity setting. During initialization set to **0x00** BIT NAME DESCRIPTION 7:0 N1.7:N1.0 0x00 = Input polarity retained
0x118	R/W	7:0	Y-ATT-C0	GPIO PCA9555 [11] configuration register port 0 register address 0x06 interface device address 0x21. Y channel Y-DSA1 attenuator configuration setting. During initialization set to **0x00** BIT NAME DESCRIPTION 7:0 C0.7:C0.0 0x00 = Output enabled
0x11C	R/W	7:0	Y-ATT-C1	GPIO PCA9555 [11] configuration register port 1 register address 0x07 interface device address 0x21. Y channel Y-DSA2 attenuator configuration setting. During initialization set to **0x00** BIT NAME DESCRIPTION 7:0 C1.7:C1.0 0x00 = Output enabled
0x120	R/W	23:0	LO-PLL-SPI-O	I2C/SPI bridge SC18IS602B [6] to PLL ADF4107 [9] interface device address 0x2A. Issue IIC request to access the I2C/SPI bridge device to send a SPI frame on interface 0 (register address 0x01) to the ADF4107 PLL registers for all channels (R, X and Y) at the same time.
0x128	R/W	7:0	LO-PLL-SPI-CFG	I2C/SPI bridge SC18IS602 [6] interface device address 0x2A. Issue IIC request to access the I2C/SPI bridge Configuration SPI register 0xF0. During initialization set to **0x01** BIT NAME DESCRIPTION

				7:6 reserved 00 = recommended 5 Order 0 = MSB first 4 reserved 0 = recommended 3:2 Mode 00 = CPOL = 0, CPHA = 0 1:0 Frequency 01 = 461 kHz
0x12C	R/W	7:0	LO-PLL-GPIO-ENA	I2C/SPI bridge SC18IS602 [6] interface device address 0x2A. Issue IIC request to access the I2C/SPI bridge GPIO Configuration GPIO register 0xF6. The data byte following the 0xF6 command byte will determine which pins can be used as GPIO. A logic 1 will enable the pin as a GPIO, while a logic 0 will disable GPIO control. During initialization set to **0x02** BIT NAME DESCRIPTION 7:4 X Don't-care bits 3 SS3 0 = Not used as GPIO 2 SS2 0 = Not used as GPIO 1 SS1 1 = Used as GPIO 0 SS0 0 = Not used as GPIO
0x130	R/W	7:0	LO-PLL-GPIO-CFG	I2C/SPI bridge SC18IS602 [6] interface device address 0x2A. Issue IIC request to access the I2C/SPI bridge GPIO Configuration register 0xF7. The pins defined as GPIO may be configured by software to one of four types on a pin-by-pin basis. These are: quasi-bidirectional, push-pull, open-drain, and input-only. During initialization set to **0xA9** BIT NAME DESCRIPTION 7:6 SS3 10 = input-only (high-impedance) 5:4 SS2 10 = input-only (high-impedance) 3:2 SS1 10 = input-only (high-impedance) 1:0 SS0 01 = push-pull
0x134	R/W	7:0	LO-PLL-GPIO-I	I2C/SPI bridge SC18IS602 [6] interface device address 0x2A. Issue IIC request to access the I2C/SPI bridge GPIO input register 0xF5. The register indicates the level on the pins BIT NAME DESCRIPTION 7:4 X Don't-care bits 3 SS3 Don't-care bit 2 SS2 Don't-care bit 1 SS1 ADF4107 MUXOUT 0 SS0 Don't-care bit
0x138	R/W	7:0	DIO-I	PCA9536 [10] interface device address 0x41. PIO input register 0x00. This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by configuration register 3. The register indicates the level on the pins BIT NAME DESCRIPTION 7:4 X 1111 = Given by chip 3 I3 Don't-care bit 2 I2 Int_Ref_ON 1 I1 Ext_Ref_Good 0 I0 I2C_Temp_Ctrl_ON
0x13C	R/W	7:0	DIO-O	PCA9536 [10] interface device address 0x41. PIO output register 0x01. This register reflects the outgoing logic levels of the pins defined as outputs by register 3. Bit values in this

				register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value. The register sets the level on the pins BIT NAME DESCRIPTION 7:4 X 1111 = Given by chip 3 I3 Don't-care bit 2 I2 Int_Ref_ON 1 I1 Don't-care bit 0 I0 I2C_Temp_Ctrl_ON
0x140	R/W	7:0	DIO-P	PCA9536 [10] interface device address 0x41. PIO polarity register 0x02. This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the corresponding input port data is inverted. If a bit in this register is cleared (written with a '0'), the input port data polarity is retained. During initialization set to **0x00** BIT NAME DESCRIPTION 7:4 X 0000 = Given by chip 3 P3 0 = Polarity retained 2 P2 0 = Polarity retained 1 P1 0 = Polarity retained 0 P0 0 = Polarity retained
0x144	R/W	7:0	DIO-C	GPIO PCA9536 [10] interface device address 0x41. PIO configuration register 0x03. This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. During initialization set to **0x02** BIT NAME DESCRIPTION 7:4 X 0000 = Given by chip 3 C3 0 = Output 2 C2 0 = Output 1 C1 1 = Input 0 C0 0 = Output
0x148	R/W	31:0	CCLK-DDS-CFR1	I2C/SPI bridge SC18IS602B [6] to DDS AD9913 [7] interface device address 0x2B. Issue IIC request to access the I2C/SPI bridge device to send a SPI frame on interface 0 (register address 0x01) to the AD9913 Control Function Register 1 (register address 0x00).
0x14C	R/W	15:0	CCLK-DDS-CFR2	I2C/SPI bridge SC18IS602B [6] to DDS AD9913 [7] interface device address 0x2B. Issue IIC request to access the I2C/SPI bridge device to send a SPI frame on interface 0 (register address 0x01) to the AD9913 Control Function Register 2 (register address 0x01).
0x150	R/W	31:0	CCLK-DDS-DAC	I2C/SPI bridge SC18IS602B [6] to DDS AD9913 [7] interface device address 0x2B. Issue IIC request to access the I2C/SPI bridge device to send a SPI frame on interface 0 (register address 0x01) to the AD9913 DAC Control Register (register address 0x02).
0x154	R/W	31:0	CCLK-DDS-FTW	I2C/SPI bridge SC18IS602B [6] to DDS AD9913 [7] interface device address 0x2B. Issue IIC request to access the I2C/SPI bridge device

				to send a SPI frame on interface 0 (register address 0x01) to the AD9913 FTW Register (register address 0x03).
0x158	R/W	15:0	DDS-POW	I2C/SPI bridge SC18IS602B [6] to DDS AD9913 [7] interface device address 0x2B. Issue IIC request to access the I2C/SPI bridge device to send a SPI frame on interface 0 (register address 0x01) to the AD9913 POW Register (register address 0x04).
0x168	R/W	7:0	CCLK-DDS-SPI-CFG	I2C/SPI bridge SC18IS602 [6] interface device address 0x2B. Issue IIC request to access the I2C/SPI bridge Configuration SPI register 0xF0. During initialization set to **0x00** BIT NAME DESCRIPTION 7:6 reserved 00 = recommended 5 Order 0 = MSB first 4 reserved 0 = recommended 3:2 Mode 00 = CPOL = 0, CPHA = 0 1:0 Frequency 00 = 1843 kHz
0x16C	R/W	7:0	CCLK-DDS-GPIO-ENA	I2C/SPI bridge SC18IS602 [6] interface device address 0x2B. Issue IIC request to access the I2C/SPI bridge GPIO Configuration GPIO register 0xF6. The data byte following the 0xF6 command byte will determine which pins can be used as GPIO. A logic 1 will enable the pin as a GPIO, while a logic 0 will disable GPIO control. During initialization set to **0x06** BIT NAME DESCRIPTION 7:4 X Don't-care bits 3 SS3 0 = Not used as GPIO 2 SS2 1 = Used as GPIO 1 SS1 1 = Used as GPIO 0 SS0 0 = Not used as GPIO
0x170	R/W	7:0	CCLK-DDS-GPIO-CFG	I2C/SPI bridge SC18IS602 [6] interface device address 0x2B. Issue IIC request to access the I2C/SPI bridge GPIO Configuration register 0xF7. The pins defined as GPIO may be configured by software to one of four types on a pin-by-pin basis. These are: quasi-bidirectional, push-pull, open-drain, and input-only. During initialization set to **0x95** BIT NAME DESCRIPTION 7:6 SS3 10 = input-only (high-impedance) 5:4 SS2 01 = push-pull 3:2 SS1 01 = push-pull 1:0 SS0 01 = push-pull
0x174	R/W	7:0	CCLK-DDS-GPIO-O	I2C/SPI bridge SC18IS602 [6] interface device address 0x2B. Issue IIC request to access the I2C/SPI bridge GPIO output register 0xF4. The register indicates the level on the pins BIT NAME DESCRIPTION 7:4 X Don't-care bits 3 SS3 Don't-care bit 2 SS2 DDS_RESET 1 SS1 DDS_IOUPDATE 0 SS0 DDS SPI CS_N
0x178	R/W	23:0	CCLK-PLL-SPI-O	I2C/SPI bridge SC18IS602B [6] to PLL ADF4001 [8] interface device address 0x28.

				Issue IIC request to access the I2C/SPI bridge device to send a SPI frame on interface 0 (register address 0x01) to the ADF4001 PLL registers for all channels (R, X and Y) at the same time.
0x180	R/W	7:0	CCLK-PLL-SPI-CFG	I2C/SPI bridge SC18IS602 [6] interface device address 0x28. Issue IIC request to access the I2C/SPI bridge Configuration SPI register 0xF0. During initialization set to **0x01** BIT NAME DESCRIPTION 7:6 reserved 00 = recommended 5 Order 0 = MSB first 4 reserved 0 = recommended 3:2 Mode 00 = CPOL = 0, CPHA = 0 1:0 Frequency 01 = 461 kHz
0x184	R/W	7:0	CCLK-PLL-GPIO-ENA	I2C/SPI bridge SC18IS602 [6] interface device address 0x28. Issue IIC request to access the I2C/SPI bridge GPIO Configuration GPIO register 0xF6. The data byte following the 0xF6 command byte will determine which pins can be used as GPIO. A logic 1 will enable the pin as a GPIO, while a logic 0 will disable GPIO control. During initialization set to **0x02** BIT NAME DESCRIPTION 7:4 X Don't-care bits 3 SS3 0 = Not used as GPIO 2 SS2 0 = Not used as GPIO 1 SS1 1 = Used as GPIO 0 SS0 0 = Not used as GPIO
0x188	R/W	7:0	CCLK-PLL-GPIO-CFG	I2C/SPI bridge SC18IS602 [6] interface device address 0x28. Issue IIC request to access the I2C/SPI bridge GPIO Configuration register 0xF7. The pins defined as GPIO may be configured by software to one of four types on a pin-by-pin basis. These are: quasi-bidirectional, push-pull, open-drain, and input-only. During initialization set to **0xA9** BIT NAME DESCRIPTION 7:6 SS3 10 = input-only (high-impedance) 5:4 SS2 10 = input-only (high-impedance) 3:2 SS1 10 = input-only (high-impedance) 1:0 SS0 01 = push-pull
0x18C	R/W	7:0	CCLK-PLL-GPIO-I	I2C/SPI bridge SC18IS602 [6] interface device address 0x28. Issue IIC request to access the I2C/SPI bridge GPIO input register 0xF5. The register indicates the level on the pins BIT NAME DESCRIPTION 7:4 X Don't-care bits 3 SS3 Don't-care bit 2 SS2 Don't-care bit 1 SS1 ADF4001 MUXOUT 0 SS0 Don't-care bit
0x190	R/W	31:0	Q-SCALE-EGU	EEPROM storing calibration data [13] interface device address 0x50. Stores the scaling for the charge to engineering units at memory address 0x0004. IEEE 754 single precision representation.
0x194	R/W	31:0	X-SCALE-EGU	EEPROM storing calibration data [13] interface device address 0x50.

				Stores the scaling for the X position to engineering units at memory address 0x0008. IEEE 754 single precision representation.
0x198	R/W	31:0	Y-SCALE-EGU	EEPROM storing calibration data [13] interface device address 0x50. Stores the scaling for the Y position to engineering units at memory address 0x000C. IEEE 754 single precision representation.
0x19C	R/W	31:0	Q-SCALE	EEPROM storing calibration data [13] interface device address 0x50. Stores the scaling for the charge for fine tuning at memory address 0x0010. IEEE 754 single precision representation.
0x1A0	R/W	31:0	X-SCALE	EEPROM storing calibration data [13] interface device address 0x50. Stores the scaling for the X position for fine tuning at memory address 0x0014. IEEE 754 single precision representation.
0x1A4	R/W	31:0	Y-SCALE	EEPROM storing calibration data [13] interface device address 0x50. Stores the scaling for the Y position for fine tuning at memory address 0x0018. IEEE 754 single precision representation.
0x1C0-0x2BC	R/W	31:0	AC-R-PHASE	EEPROM storing attenuator phase calibration data [13] interface device address 0x50. Stores the memory address 0x0034-0x0130. The 32 bit value representing [-360°:360°] has to be scaled by: angle / 0.015625 [°]
0x2C0-0x3BC	R/W	31:0	AC-R-AMPL	EEPROM storing attenuator amplitude calibration data [13] interface device address 0x50. Stores the memory address 0x0134-0x0230. IEEE 754 single precision representation [dB].
0x3C0-0x4BC	R/W	31:0	AC-X-PHASE	EEPROM storing attenuator phase calibration data [13] interface device address 0x50. Stores the memory address 0x0234-0x0330. The 32 bit value representing [-360°:360°] has to be scaled by: angle / 0.015625 [°]
0x4C0-0x5BC	R/W	31:0	AC-X-AMPL	EEPROM storing attenuator amplitude calibration data [13] interface device address 0x50. Stores the memory address 0x0334-0x0430. IEEE 754 single precision representation [dB].
0x5C0-0x6BC	R/W	31:0	AC-Y-PHASE	EEPROM storing attenuator phase calibration data [13] interface device address 0x50. Stores the memory address 0x0434-0x0530. The 32 bit value representing [-360°:360°] has to be scaled by: angle / 0.015625 [°]
0x6C0-0x7BC	R/W	31:0	AC-Y-AMPL	EEPROM storing attenuator amplitude calibration data [13] interface device address 0x50. Stores the memory address 0x0534-0x0630. IEEE 754 single precision representation [dB].
0x7C0-0x870	R/W	31:0	IB-R-PHASE	EEPROM storing I/Q imbalance phase calibration data [13] interface device address 0x50. Stores the memory address 0x0634-0x06E4. The 32 bit value representing [-360°:360°] has to be scaled by: angle / 0.015625 [°]
0x874-0x924	R/W	31:0	IB-R-AMPL	EEPROM storing I/Q imbalance amplitude calibration

				data [13] interface device address 0x50. Stores the memory address 0x06E8 -0x0798. IEEE 754 single precision representation [factor].
0x928-0x9D8	R/W	31:0	IB-X-PHASE	EEPROM storing I/Q imbalance phase calibration data [13] interface device address 0x50. Stores the memory address 0x079C-0x084C. The 32 bit value representing [-360°:360°] has to be scaled by: angle / 0.015625 [°]
0x9DC-0xA8C	R/W	31:0	IB-X-AMPL	EEPROM storing I/Q imbalance amplitude calibration data [13] interface device address 0x50. Stores the memory address 0x0850 -0x0900. IEEE 754 single precision representation [factor].
0xA90-0xB40	R/W	31:0	IB-Y-PHASE	EEPROM storing I/Q imbalance phase calibration data [13] interface device address 0x50. Stores the memory address 0x0904-0x09B4. The 32 bit value representing [-360°:360°] has to be scaled by: angle / 0.015625 [°]
0xB44-0xBF4	R/W	31:0	IB-Y-AMPL	EEPROM storing I/Q imbalance amplitude calibration data [13] interface device address 0x50. Stores the memory address 0x09B8 -0x0A68. IEEE 754 single precision representation [factor].

Table 1: PLB Memory Map

4 Appendix

None.