XFEL
GPAC
Clock Interface
Firmware
Data Sheet

Content

Table of Contents

Figures

Tables

1 Introduction

For the XFEL project a generic carrier called GPAC is designed. The GPAC contains several FPGAs of which one (BPM_FPGA) is responsible for the communication interface of the GPAC. The BPM_FPGA is set up as a System On Chip (SOC) containing several peripheral systems on the PLB 4.6 bus system. This document here describes one of these peripherals.
The basis for this document is the schematic of the GPAC [2].

1.1 Purpose

The intention is to get an introduction into the GPAC Clock Interface design which might be used in various firmware designs. This document explains the features provided and constraints implied onto a possible design needing/using the library module.

1.2 Scope

This document targets a system designer of a GPAC.

1.3 Definitions, acronyms, and abbreviations

This document is based on the “IEEE Recommended Practice for Software Requirements Specifications” [1].

BP_FPGA	Backplane FPGA on the GPAC
BPM1_FPGA	BPM 1 FPGA connected to the first 500 pole connector on the GPAC
BPM2_FPGA	BPM 2 FPGA connected to the second 500 pole connector on the GPAC
CFG_FPGA	Configuration FPGA on the GPAC
DCM	Digital Clock Manager, A Delay Locked Loop in the Xilinx FPGAs responsible for the clock generation and clock phases.
FPGA	Field Programmable Gate Array
Reg	Register. Mathematically z^-1
SEU	Single Event Upset FPGA on the GPAC
SOC	System On Chip. A processor with RAM and peripherals on the same FPGA
SYS_FPGA	System FPGA on the GPAC

1.4 References

[1] IEEE Std 830-1998, Recommended Practice for Software Requirements Specifications.
[2] PSI 2010, GPAC board, V1.00.
[3] Xilinx virtex5_hdl.pdf, Virtex-5 Libraries Guide for HDLDesigns

1.5 Overview

This document provides a detailed overview of the firmware interface and specifies the user interface.

2 Overall description

The system consists of a clock core connected to the 125 MHz, 200 MHz and 250 MHz clock system connected to all FPGAs for the fabric and the 125 MHZ and 150 MHz clock for the MGTs.
The aim of the component is to:

- Prepare the clocks in terms of phase, frequency and duty cycle for further use in the BPM_FPGA fabric.
- Generate the resets
- Provide mechanisms for distributing the clocks (for example sharing the reference clock between MGT tiles).

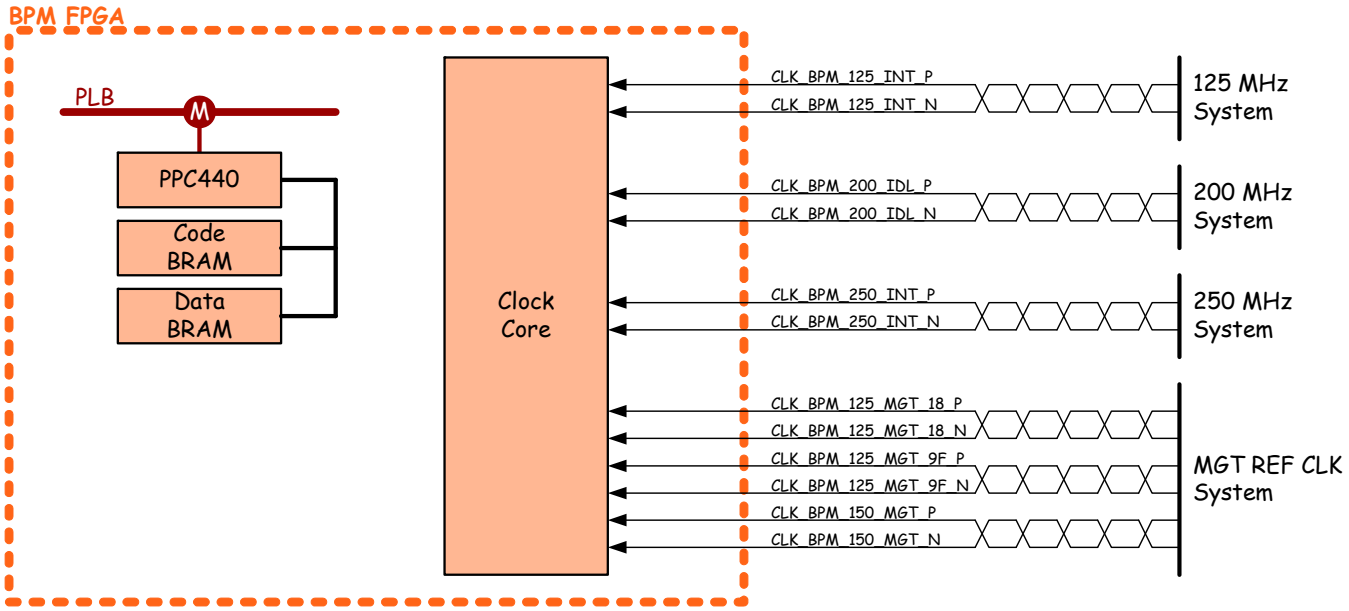

Figure 1: Overview

The clock core drives the various clocks in the BPM_FPGA firmware. Take particular care of the clocking scheme of the PPC440 hard ip which requires a phase offset (please check for CLKOUTx_DESKEW_ADJUST in the “Embedded Processor Block Reference Guide” (UG200) chapter “Clock Insertion Delays and PLL Usage”) compared to the other PLB cores on the bus.

2.1 User interfaces

2.1.1 Core Interface

Signal Name	Allowable Values	Description
System		
i_clk_125MHz_p		125 MHz differential-p system clock
i_clk_125MHz_n		125 MHz differential-n system clock
i_clk_200MHz_p		200 MHz differential-p system clock
i_clk_200MHz_n		200 MHz differential-n system clock
i_clk_250MHz_p		250 MHz differential-p system clock
i_clk_250MHz_n		250 MHz differential-n system clock
i_clk_125MHz_mgt_18_p		125 MHz differential-p reference clock for MGTs
i_clk_125MHz_mgt_18_n		125 MHz differential-n reference clock for MGTs
i_clk_125MHz_mgt_9f_p		125 MHz differential-p reference clock for MGTs
i_clk_125MHz_mgt_9f_n		125 MHz differential-n reference clock for MGTs
i_clk_150MHz_mgt_p		150 MHz differential-p reference clock for MGTs
i_clk_150MHz_mgt_n		150 MHz differential-n reference clock for MGTs
FPGA internal interface		
rst_125MHz		125 MHz reset
clk_125MHz_ppc		Global 125 MHz system clock with ppc skew adjustment for PPC440 cores
clk_125MHz		Global 125 MHz system clock
clk_125MHz_90		Global 125 MHz system clock with 90 degrees phase
clk_125MHz_180		Global 125 MHz system clock with 180 degrees phase
clk_125MHz_div2		Global 62.5 MHz system clock derived from the 125 MHz clock
rst_200MHz		200 MHz reset
clk_200MHz		Global 200 MHz system clock
clk_200MHz_div2		Global 100 MHz system clock derived from the 200 MHz clock
rst_250MHz		250 MHz reset
clk_250MHz		Global 250 MHz system clock
clk_250MHz_90		Global 250 MHz system clock with 90 degrees phase
clk_250MHz_180		Global 250 MHz system clock with 180 degrees phase
clk_250MHz_div2		Global 125 MHz system clock derived from the 250 MHz clock
clk_125MHz_mgt_18		Virtex-5 mgt clock distribution 125 MHz reference clock **Please note: Not all GTX tiles can be reached with this ref clock. Check in the datasheet which MGT tiles can be reached with this ref clock**
clk_125MHz_mgt_9f		Virtex-5 mgt clock distribution 125 MHz reference clock **Please note: Not all GTX tiles can be reached with this ref clock. Check in the**

		datasheet which MGT tiles can be reached with this ref clock
clk_150MHz_mgt		Virtex-5 mgt clock distribution 150 MHz reference clock
idelay_ctrl_rdy		RDY output from the IDELAYCTRL primitive used for the idelays of the Virtex-5

Table 1: Signal Description

2.1.2 Clock Core Interface

The core is embedded in a standalone interface without PLB access.

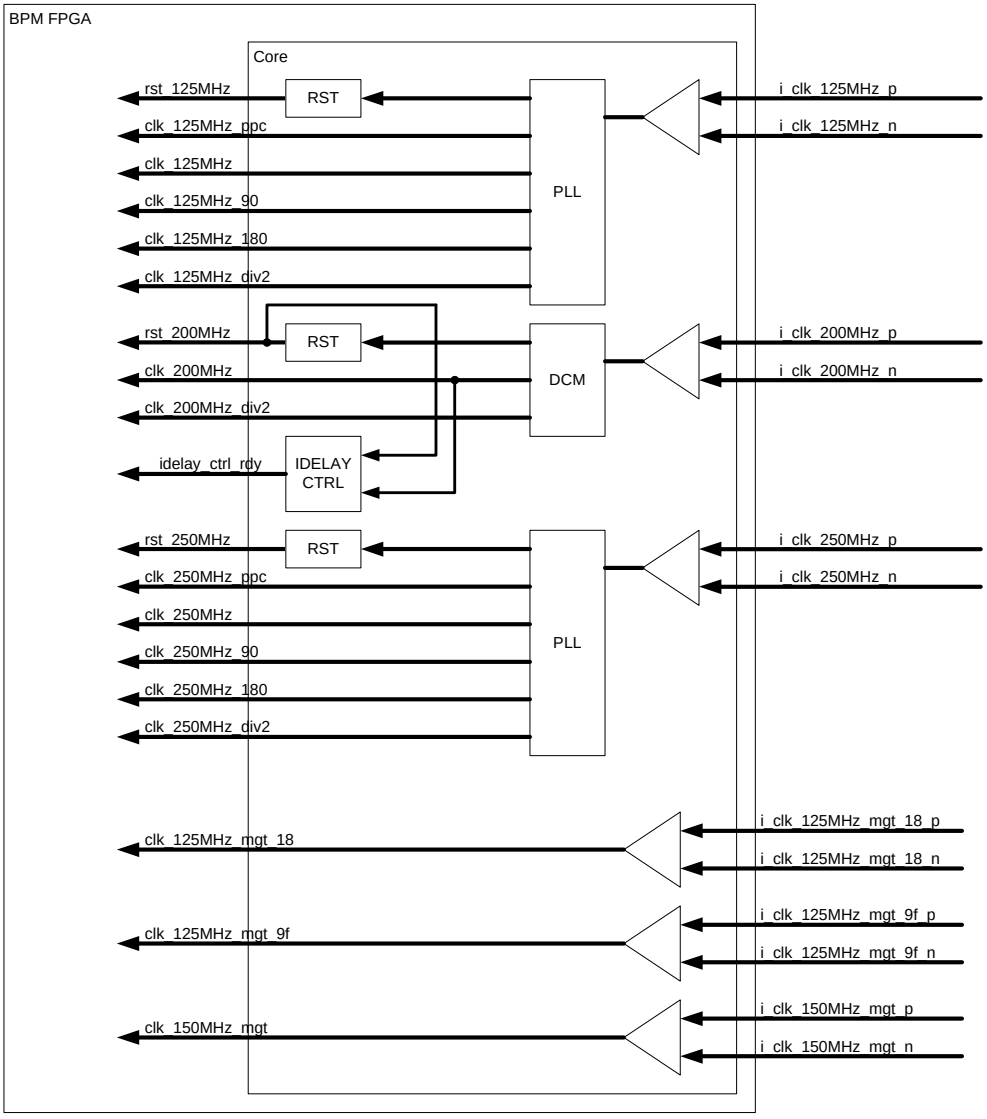

Figure 2: Clock Core Overview

The reset is released after the PLL/DCM has gained lock on the input clock.

The MGT clocks are routed though the dedicated reference clock lanes in the Virtex-5 FPGA.

Please note: If in a particular design the reference clock is not connected to a used GTX tile then this reference clock tile has to be instantiated as a dummy component in order to have the reference clock inputs being terminated correctly. If this dummy core is not implemented the clock will not be terminated properly and suffer from activity of nearby pins and occasionally cause the CDR to loose lock.

2.2 Performance

This chapter sums the tested static and dynamic requirements of the firmware. Used was a Virtex5 FPGA (for determining the values below an xc5fx70t speed grade 1 has been used)

Features of the receiver design	
Baud rate	
Max clock frequency	
Flip Flop used	
LUT used	

Table 2: Design Features

2.3 Design constraints

The design is in pure VHDL, however it contains primitive instantiations.

2.4 Software system attributes

The link design is implemented as a VHDL package.

3 Appendix

None.