European XFEL Cavity BPM plb46_to_fastlink_mmap Data Sheet

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1 Introduction

For the European XFEL project a fast 160 MSa/s ADC card with 6 channels for the use with cavity RFFEs was developed. This card contains temperature sensors, offset compensation circuits, clock distribution (delay and divider) and some other features of lesser importance.
The ADC16HL mezzanine board is a 6 channel ADC board with a resolution of 16 bit and a sampling rate of 160 MSa/s. The 500 pole mezzanine connector matches the PDC and GPAC carrier board pinning. All analog inputs are connected differentially to RADIALL connectors on the front. The sampling clock for the ADC's can be fed from an SMA connector, single ended or an internal free running 160 MHz quartz oscillator clock. The selection of the clock source/frequency/delay is controlled at runtime by software.

1.1 Purpose

The document here describes the firmware developed based on the schematic [2], hardware user document [3] and firmware interface datasheet [4].

1.2 Scope

This document specifies the firmware user interface and includes only selected information from the ADC16HL datasheet if considered helpful for the understanding.

1.3 Definitions, acronyms, and abbreviations

This document is based on the "IEEE Recommended Practice for Software Requirements Specifications" [1].

ADC	Analog Digital Converter.
BPM	Beam Position Monitor
FPGA	Field Programmable Gate Array. Programmable logic device.

1.4 References

[1] IEEE Std 830-1998, Recommended Practice for Software Requirements Specifications.
[2] PSI 2011, Schematic X-FEL BPM Electronics ADC16HL, ADC16HL_V2_Schematic.pdf
..\..\..\..\..\ADC16HL\04_Data_Sheet\01_Reference\ADC16HL_V2_Schematic.pdf and
..\..\..\..\..\ADC16HL\04_Data_Sheet\01_Reference\ADC16HL_V2_Assembly.pdf
[3] PSI 2009, User manual ADC16HL V2, Revision 1.0, ADC16HL_V2_Manual.pdf
..\..\..\..\..\ADC16HL\04_Data_Sheet\01_Reference\ADC16HL_V2_Manual.pdf
[4] PSI 2012, ADC16HL Firmware Interface Data Sheet ADC16HL_data_sheet.rtf
..\..\..\..\..\ADC16HL\04_Data_Sheet\ADC16HL_data_sheet.rtf
[5] PSI 2005, Fast Link Firmware Data Sheet fast_link_datasheet.rtf
..\..\..\..\..\ADC16HL\04_Data_Sheet\01_Reference\fast_link_data_sheet.pdf

1.5 Overview

This document provides an overview of the firmware interface and specifies the user interface.

2 Overall description

Up to two ADC16HL [2][3] boards can be connected to one GPAC. Each of the ADC16HL has a small FPGA controlling the features on the board and providing an abstract interface to these features.

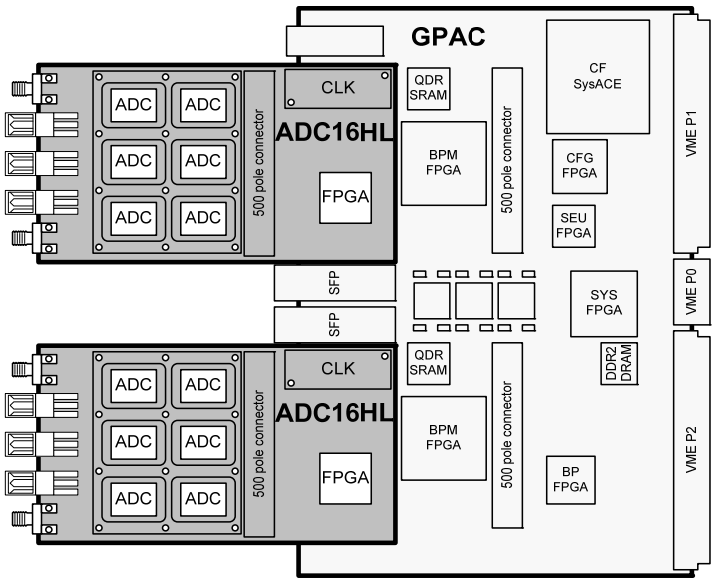

Figure 1: Board Overview

The mezzanine board ADC16HL contains a local oscillator 160 MHz (SL570), clock distribution chip (LMK01020), six 160 MSa/s 16 bit ADCs (LTC2209), temperature sensors (ADT7301), offset compensation circuitry DAC (DAC7512) and ADC (LTC2448) that are all connected to a Spartan-3AN FPGA. Each chip has different interfaces such as direct connections and serial protocols of varying bit length, phases and bit rates. The Spartan-3AN FPGA acts as an intermediate layer hiding parts of the framing and communication interfaces from the user and providing a common interface to access them all.
The main clock to the ADC16HL FPGA (FL_CLK) is provided by the GPAC and is switched off during measurement in order to prevent the clock of the FPGA to interfere with the ADC measurement data.
The ADC16HL provides to the GPAC information (FL_IDLE) whether the currently received request is still in progress or if a new request can be accepted.
The ADC16HL has differentially routed traces for the ADC data/clock and for the board settings. All signals are connected to the 500 pole connector matching the GPAC pinning. The board settings are carried out by means of a differentially routed serial protocol from the GPAC called FastLink [5]. The FastLink is a serial link which transmits four 16 bit words. After each 4 bits of data a stuffing bit (inverted preceding bit) is inserted for resynchronization purposes. The frame starts with a “start of frame” bit which is always “1”. The next 15bits form the address, indicating the recipient of the following 16 bit of data. The frame is protected by a 16 bit CRC checksum. The frame finishes with an inter-frame gap allowing the receiver of such a link to detect clearly the start of frame.

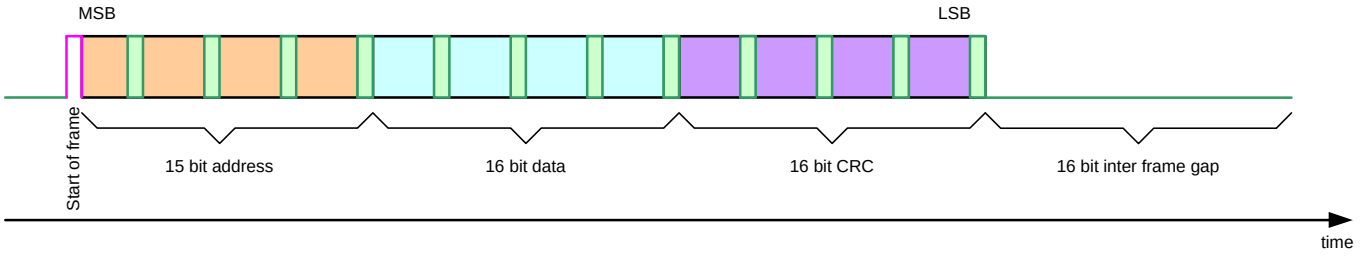

Figure 2: Frame Overview

In order to allow several PLB masters access to the ADC16HL without interfering with a currently running request a PLB component called PLB46_to_FASTLINK_MMAP was placed in the BPM FPGAs.
The PLB46_to_FASTLINK_MMAP component provides to the master an access to different functions independently, preserving the request order, issuing interrupts when the FastLink transfer has finished, local storage of the last access to a specific register on the ADC16HL and a feature to read defined functions (temperatures, status, firmware id etc.) triggered by an external signal without software interaction.

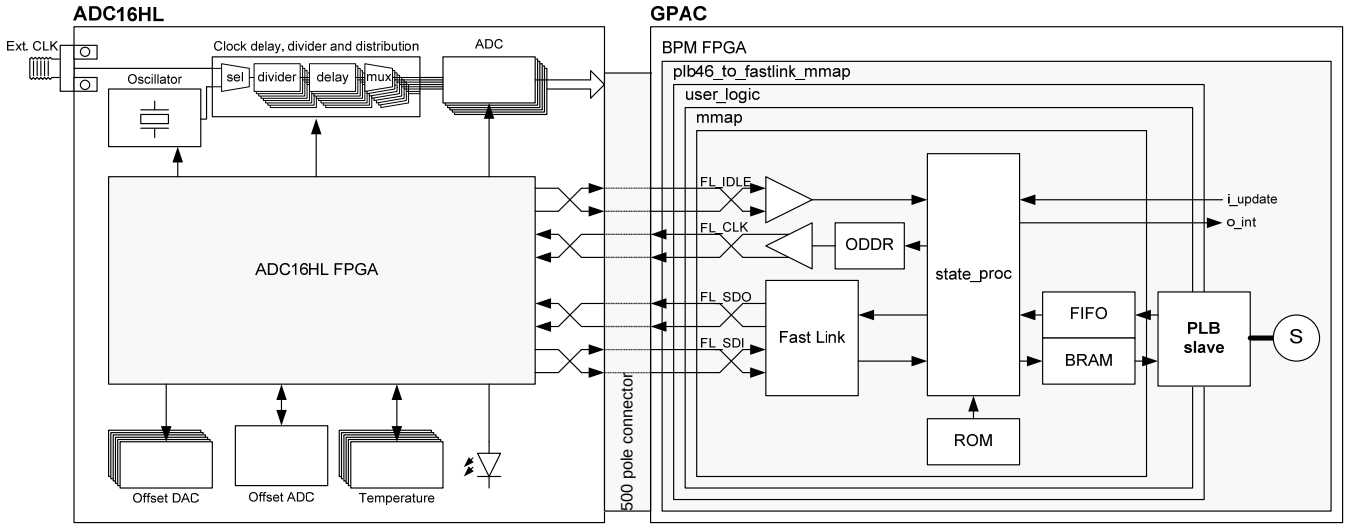

Figure 3: ADC16HL and GPAC Interconnect

If the user wants to write data by means of PLB then he writes to a specific address (which is composed from interrupt request and index) into a FIFO. Then the state machine (state_proc) enables the clock (FL_CLK). If the FastLink is idle and also the ADC16HL is idle then the state machine reads the request from the FIFO (function address and eventually the data), gets the access information from the ROM (using the function address as index) and sends it over the FastLink. The ADC16HL reacts on every FastLink frame with a response. On a write request it echoes this write request and on a read it attaches the data read from a particular function. The response from the ADC16HL is written into a BRAM showing to the user the last access to the function address on the ADC16HL. If an interrupt was requested by the PLB master (also coded into the function address) then this interrupt is issued after the response was received. If no further requests are in the FIFO then the clock (FL_CLK) is switched off until another request is found in the FIFO and the process described repeats.
Another access to this firmware is by means of an external trigger (i_update). If an edge is found on this trigger then the state machine (state_proc) iterates trough the ROM searching for

functions to be updated automatically and issues the necessary FastLink requests. Due to the storage of these requests the user benefits from not having to wait for completion of each of the individual requests but can access several function reads in a burst transfer.

3 Request composition

The PLB address, to which a user writes, forms the request on the FastLink by looking up the FastLink address and FastLink Data Length of the request by using the Index part of the PLB address in the ROM table.

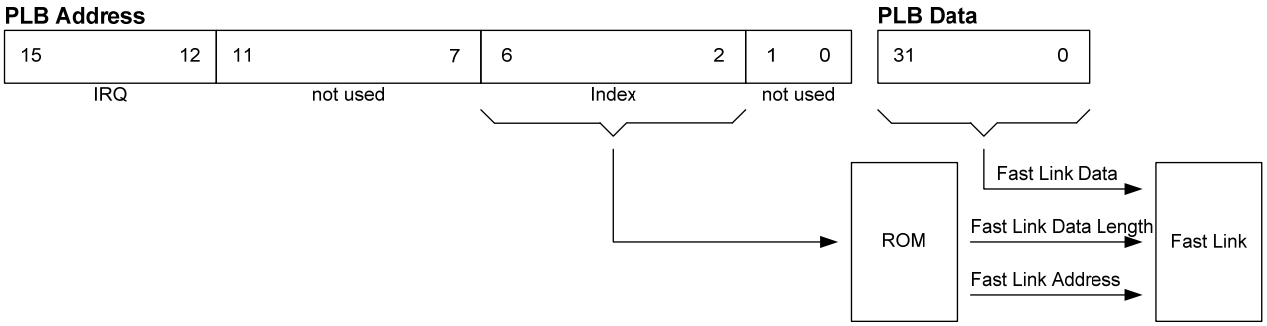

Figure 4: PLB Address Decomposition

A PLB read request always reads from the BRAM, it does not issue a FastLink message. Only a PLB write issues the forming of a FastLink message and sends it over the link to the ADC16HL.

Address [7:0]	R/W	Bit	Name	Description
0x00	R/W	15:0	ADC16HL_FW	ADC16HL Firmware version interface. Issue FastLink request to read the firmware version
0x04	R/W	15:0	ADT7301_0	ADC16HL temperature sensor ADT7301 interface. Issue FastLink request to read the Temperature 0
0x08	R/W	15:0	ADT7301_1	Issue FastLink request to read the Temperature 1
0x0C	R/W	15:0	ADT7301_2	Issue FastLink request to read the Temperature 2
0x10	R/W	15:0	ADT7301_3	Issue FastLink request to read the Temperature 3
0x14	R/W	15:0	ADT7301_4	Issue FastLink request to read the Temperature 4
0x18	R/W	15:0	ADT7301_5	Issue FastLink request to read the Temperature 5
0x1C	R/W	31:0	LMK010x0	ADC16HL clock distribution chip LMK010x0 interface. Issue FastLink request to write to the clock distribution chip
0x20	R/W	15:0	DAC7512_0	ADC16HL offset compensation DAC7512 interface. Issue FastLink request to write to the offset DAC 0
0x24	R/W	15:0	DAC7512_1	Issue FastLink request to write to the offset DAC 1
0x28	R/W	15:0	DAC7512_2	Issue FastLink request to write to the offset DAC 2
0x2C	R/W	15:0	DAC7512_3	Issue FastLink request to write to the offset DAC 3
0x30	R/W	15:0	DAC7512_4	Issue FastLink request to write to the offset DAC 4
0x34	R/W	15:0	DAC7512_5	Issue FastLink request to write to the offset DAC 5
0x38	R/W	15:0	DAC7512_ALL	Issue FastLink request to write to all offset DACs
0x3C	R/W	15:0	ADC16HL_CTRL	ADC16HL control and status interface. Issue FastLink request to write the control word
0x40	R/W	15:0	ADC16HL_STAT	ADC16HL control and status interface. Issue FastLink request to read the status word
0x44	R/W	31:0	LTC2448_WR	ADC16HL calibration ADC LTC2448 interface. Issue FastLink request to write to the calibration ADC
0x48	R/W	31:0	LTC2448_RD	Issue FastLink request to read from the calibration ADC

Table 1: PLB Memory Map

4 Appendix

None.