European XFEL Cavity BPM Software Data Sheet

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1 Introduction

For the E-XFEL a cavity BPM was designed consisting of the 3.3 GHz cavity pickup, RFFE board, ADC16HL sampling board, the GPAC carrier board and additional boards (transition cards, EVR) supporting the application. The aim is to measure sub um resolution of the beam position.
The software described here is using the hardware and firmware components implemented in the BPM FPGA for higher layer feedback systems and control simplification.

1.1 Purpose

The aim of this document is to provide a global overview of the software within the GPAC and describe the user interface of the BPM FPGAs on the GPAC.

1.2 Scope

This document provides a detailed overview of the software interface and specifies the user interface.

1.3 Definitions, acronyms, and abbreviations

This document is based on the “IEEE Recommended Practice for Software Requirements Specifications” [1].

ADC	Analog Digital Converter.
BPM	Beam Position Monitor
bunch train	All bunches belonging to one macro-pulse (macro-pulse as defined in the specification of DESY timing system)
EVR	EVent Receiver. Decoder of the Event Link at PSI. This is a standard PSI VME card used to decode event link messages for trigger generation.
FPGA	Field Programmable Gate Array. Programmable logic device.
MGT	Multi Gigabit Tranceiver. A component inside the FPGA which does serial bit streams including framing information running at more than a GBit/s
reg	Register. Mathematically z^-1
SOC	System on Chip. Basically a self-contained processor system in one chip, including processor, memory, and some peripherals.
TBD	To Be Defined. Means has to be defined by the user at setup of the FEL.

1.4 References

[1] IEEE Std 830-1998, Recommended Practice for Software Requirements Specifications.
[2] PSI 2012, Cavity BPM ADC Data Processing Ideas, Cavity_BPM_ADC_Data_Processing_Ideas_v1r4.pdf
..\..\..\..\..\04_Data_Sheet\01_Reference\Cavity_BPM_ADC_Data_Processing_Ideas_v1r4.pdf

[3] PSI 2014, European XFEL Cavity BPM bpm_cav_exfel Data Sheet, bpm_cav_exfel.pdf
..\..\pcores\bpm_cav_exfel_v1_00_a\doc\bpm_cav_exfel.pdf
[4] PSI 2013, European XFEL Cavity BPM plb46_to_fastlink_mmap Data Sheet, plb46_to_fastlink_mmap.pdf
..\..\pcores\plb46_to_fastlink_mmap_v1_00_a\doc\plb46_to_fastlink_mmap.pdf
[5] PSI 2013, European XFEL Cavity BPM plb46_to_iic_mmap Data Sheet, plb46_to_iic_mmap.pdf
..\..\pcores\plb46_to_iic_mmap_v1_00_a\doc\plb46_to_iic_mmap.pdf
[6] PSI 2013, European XFEL Cavity BPM sys_init Data Sheet, sys_init.pdf
..\..\pcores\sys_init_v1_00_a\doc\sys_init.pdf

1.5 Overview

Chapter 2 provides an overview and how the software is related to other components/functions implemented in firmware and hardware. The most important point to realize is that the BPM FPGAs are implementing a Sytem On Chip (SOC) design using the PLB as multi-master, random access memory map, which means that all accesses can be done by the processor and in parallel by the control-system. Chapter 3 contains all the detail information on the user interfaces.

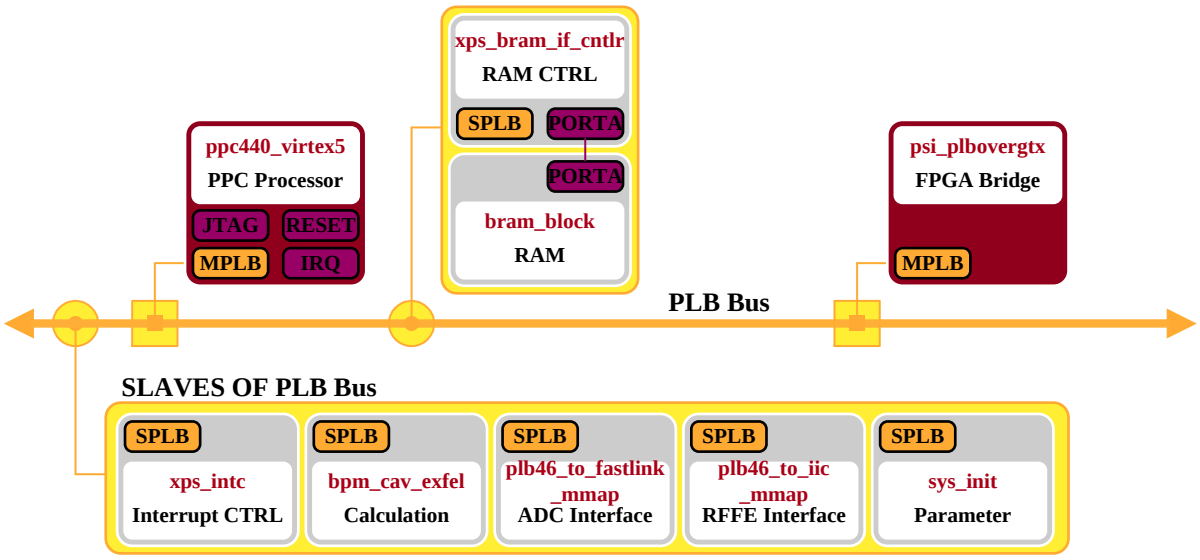

Figure 1: Cavity BPM SOC Firmware Overview (only a selection of used components)

The IBM® PLB is the backbone of the BPM FPGA firmware which allows connecting a PowerPC processor and a Multi Gigabit Tranceiver (MGT) based interface towards the control system as two independent masters on the bus. The PowerPC software is executed in a memory which is inside the FPGA and which is loaded together with the FPGA firmware. This means no additional loading of software is needed after the FPGA has got its firmware.
There are as well several slave components connected on the PLB. Some of these slave components are for organizing the processor like the interrupt controller (xps_intc), others are doing the interfacing to the cards (plb46_to_fastlink_mmap [4] and plb46_to_iic_mmap [5]), some implement a specialized storage for parameters (sys_init [6]) and the main number crunching and data processing is done in the bpm_cav_exfel [3] component. For more details please refer to the documentation of the individual firmware implementations.

2 Overall description

Figure 1 illustrates the main devices used in the BPM system. On the left hand side the pickups are drawn, which are connected to the RFFE by several meter long RF cables. Within the RFFEs the 3.3 GHz signals from the pickups are mixed with a machine RF derived frequency to obtain a pulse long enough to be measured with the six, 16 bit, 160 MSa/s ADC on the ADC16HL piggyback board. The ADC data is processed in the BPM FPGA on the GPAC and the results of the measurements and preprocessing calculations are finally provided to the control system.

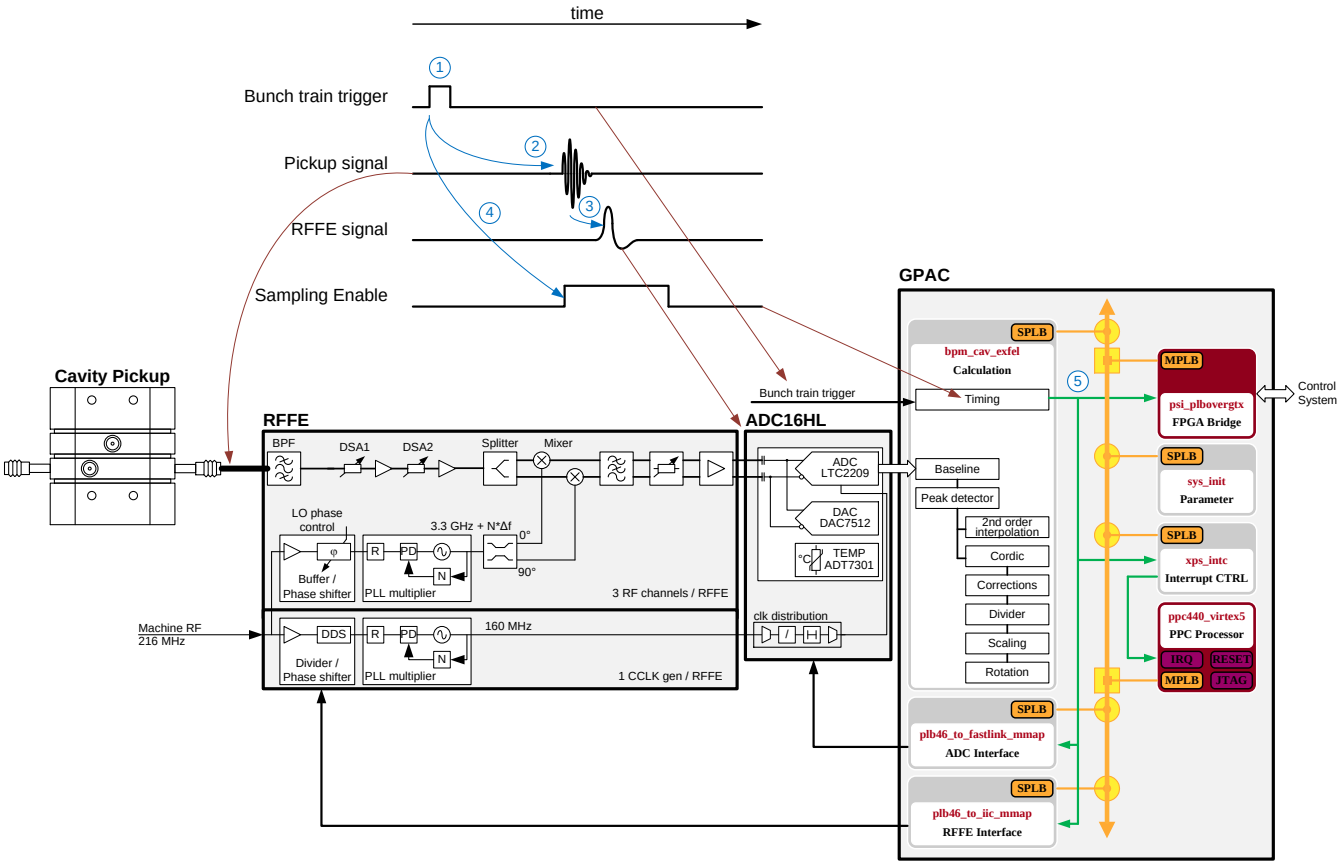

Figure 2: Cavity BPM Overview

The blue bullets in the figure above denote the following timing:

1.) The timing and event system of the machine provides a trigger pulse to the GPAC. In forming the GPAC that a new electron bunch is imminent.

2.) The electron bunch passing the pickup causes the pickup to generate a response oscillation (decaying 3.3 GHz oscillation).

3.) The RFFE down-converts the pickup response to a lower frequency (mixing the decaying pickup oscillation with a generated, stable, continuous 3.3 GHz signal)

4.) The GPAC opens a sampling window for the bunch to take measurements and do the beam parameter (position and charge) calculation. Basically sampling of ADC data and preprocessing the measurements.

5.) After completing the measurement/calculation an interrupt is issued to the control system to inform, that new data is available and ready to be picked up. At the same time it automatically triggers the read back of status information (temperatures, PLL lock status, …) from the ADC16HL board and the RFFE board.

The control system configures the BPM system by means of providing signals and information concerning the timing of the beam (a very stable machine RF and event system containing bunch train trigger, bunch number, etc.), the charge and filling pattern expected. This information has to be sent to the BPM system in advance, e.g. before the bunch train is fired.

3 Machine Interface Overview

The control (event) system of the E-XFEL machine will provide a signal denoted in this document as a bunch train trigger. This bunch train trigger informs the BPM that after a location dependent delay (B1.0) the bunch train will start; containing a predefined number of bunches (B0.0).

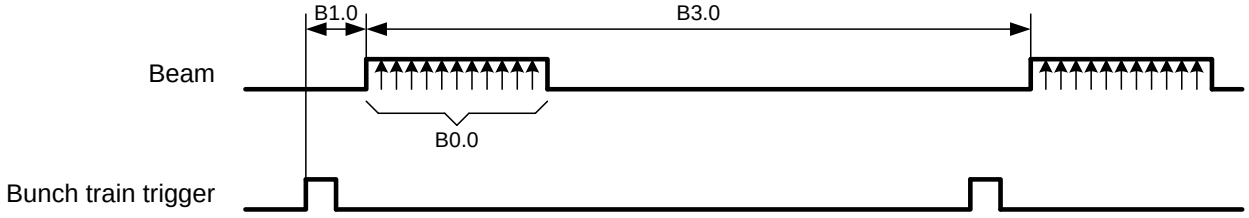

Figure 3: Machine Timing

Time	Value	Description
B0.0	1…3072	Number of bunches in the bunch train. The BPM electronics will measure and calculate this amount of positions.
B1.0	Location dependent	Delay between event transmitted on the event link cable (timing system of the machine) and the beam measured by a particular pickup. Stable delay, but depends on the position in the machine, hence different for each BPM
B3.0	max. 30 Hz	Bunch train repetition rate. This is a machine parameter, e.g. can be regarded as minimal delay between bunch trains.

Table 1: Machine Timing

The bunch train trigger is encoded in an event link frame of the E-XFEL.

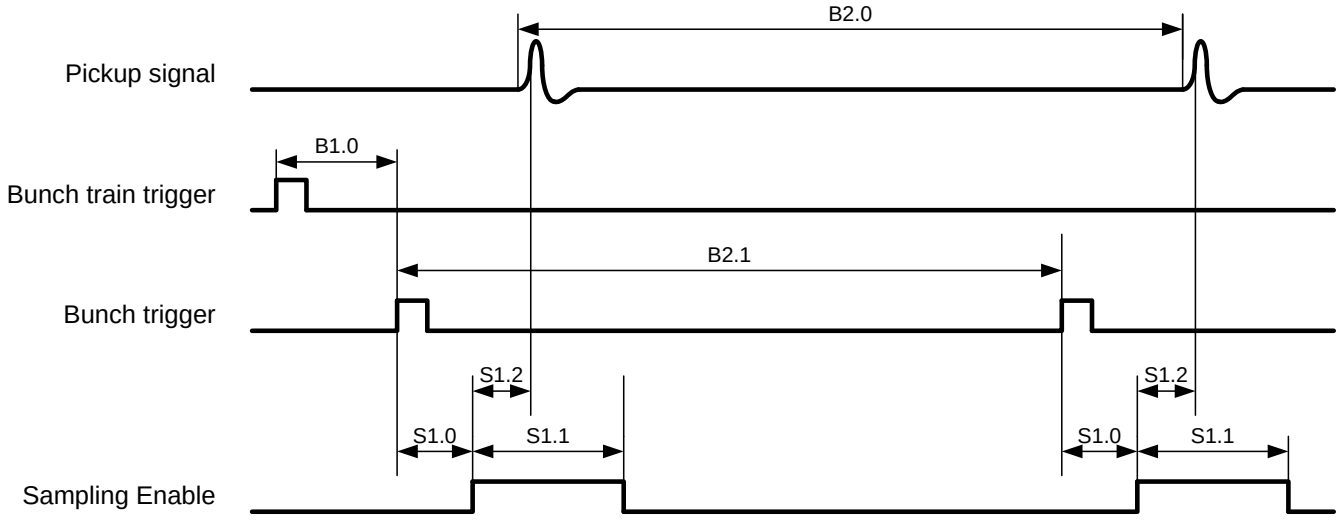

Figure 4: Beam Timing

Time	Value	Description

B1.0	Location dependent	Delay between event transmitted on the event link cable (timing system of the machine) and the beam measured by a particular pickup. Stable delay, but depends on the position in the machine, hence different for each BPM.
B2.0	200 ns … 1 ms	Bunch repetition rate. This is a machine setting carried out by the control system.
B2.1	200 ns … 1 ms in FPGA clock cycles	Basically the same as the bunch repetition rate but implemented as a counter in the BPM FPGA, hence the units are clock cycles. This is a machine setting carried out by the control system.
S1.0	TBD by the user	Sampling delay for the beam measurement.
S1.1	TBD by the user	Sampling duration for the beam measurement. In order to reduce the latency the user has to try to keep this window as short as possible.
S1.2	TBD by the user	Pre-samples of the beam measurement. This value is important if the bunch train trigger is missing and the FPGA needs to find the beam within the ADC data stream. The setting is only relevant in the signal (self) triggered mode.

Table 2: Beam Timing

3.1 Set values

There are several boards in a BPM system working together in order to measure the position and charge of the beam passing the pickup.
All these boards contain chips which have to be initialized or configured before they can contribute to the measurement. Because the interface to the boards (plb46_to_fastlink_mmap [4] and plb46_to_iic_mmap [5]) is reachable by memory access the user may choose to retrieve values directly from the hardware or write data directly to the hardware registers, however then the user has to construct the bit-patterns expected by the respective hardware chip. It turned out that this means a lot of bit arithmetic for the user which the user would like to avoid. For this feature a memory component was implemented (sys_init [6]) which is readable and writable by the user. This component separates each setting into an own memory address, which isolates the various settings for the user (no needed for bit arithmetic, shift, mask, ...). The local processor on the GPAC constructs the register word as needed by the hardware and writes this word to the interface.

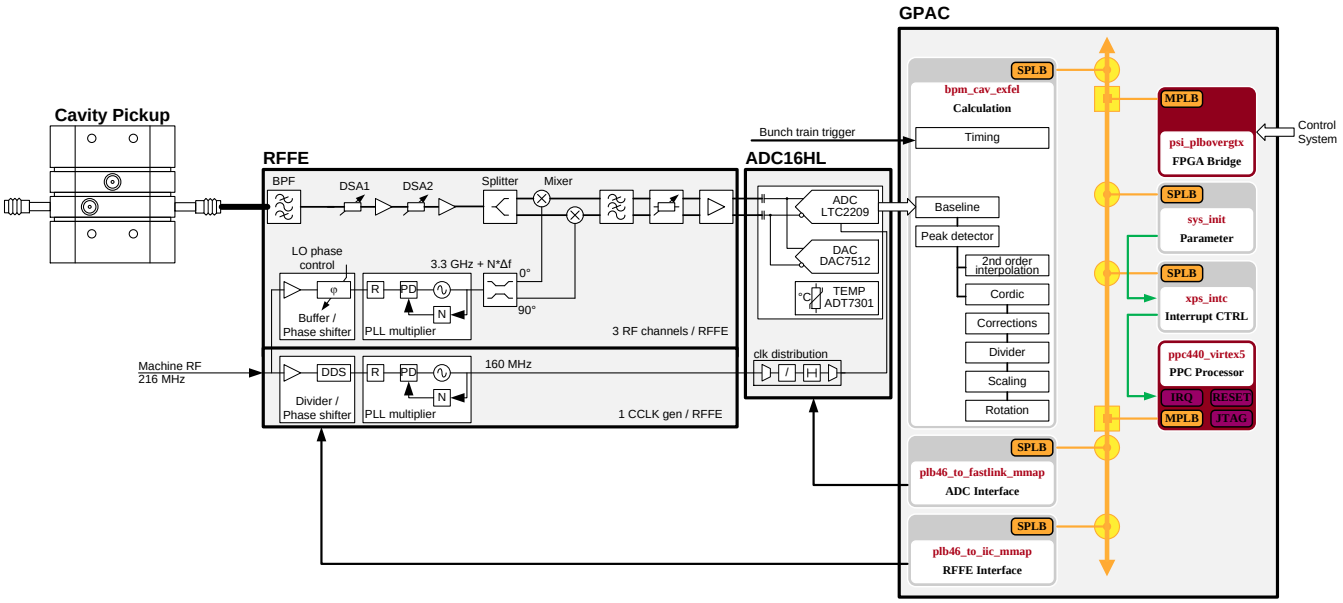

Figure 5: Set Values

The first board in the processing chain of the pickup signal is the RFFE board. This board is an analog high frequency board with many digitally controlled parameters to be set.

Address (SYS_INIT)	R/W	Bit	Name	Description
0x00000200	R/W	0	SYS_INIT_RFFE_INIT_IDX	Initializes the whole RFFE board in a sequence which allows all components to startup properly. '0' = Do not initialize. '1' = Start initialization.
0x00000204	R/W	0	SYS_INIT_RFFE_EEPROM_RD_IDX	Read configuration from EEPROM, located on the RFFE board and copy the parameters to the firmware calculation pipeline. '0' = Do not read. '1' = Start reading.
0x00000208	R/W	0	SYS_INIT_RFFE_EEPROM_WR_IDX	Read configuration data from the firmware calculation pipeline and write

				the parameters to EEPROM, located on the RFFE board. '0' = Do not write. '1' = Start writing.
0x00000210	R/W	0	SYS_INIT_DIO_TMP_FB_IDX	Switch between temperature feedback (analog feedback loop on the RFFE board) and temperature control (only set value without analog feedback). '0' = Analog temperature feedback. '1' = Set value, without feedback.
0x00000214	R/W	31:0	SYS_INIT_R_RF_TMP_FBO_IDX	Set temperature for the R channel attenuator : 0.0 °C… 60.0 °C IEEE 754 single precision representation.
0x00000218	R/W	31:0	SYS_INIT_R_MX_TMP_FBO_IDX	Set temperature for the R channel mixer : 0.0 °C… 60.0 °C IEEE 754 single precision representation.
0x0000021C	R/W	31:0	SYS_INIT_X_RF_TMP_FBO_IDX	Set temperature for the X channel attenuator : 0.0 °C… 60.0 °C IEEE 754 single precision representation.
0x00000220	R/W	31:0	SYS_INIT_X_MX_TMP_FBO_IDX	Set temperature for the X channel mixer : 0.0 °C… 60.0 °C IEEE 754 single precision representation.
0x00000224	R/W	31:0	SYS_INIT_Y_RF_TMP_FBO_IDX	Set temperature for the Y channel attenuator : 0.0 °C… 60.0 °C IEEE 754 single precision representation.
0x00000228	R/W	31:0	SYS_INIT_Y_MX_TMP_FBO_IDX	Set temperature for the Y channel mixer : 0.0 °C… 60.0 °C IEEE 754 single precision representation.
0x00000230	R/W	0	SYS_INIT_DIO_INT_REF_IDX	Use local oscillator for reference clock or external signal as reference clock. '0' = Local oscillator off. '1' = Local oscillator on.
0x00000240	R/W	0	SYS_INIT_CCLK_DDS_RESET_IDX	ADC clock path DDS chip AD9913, reset: '0' = Reset inactive. '1' = Reset active.
0x00000244	R/W	31:0	SYS_INIT_CCLK_DDS_CFR1_IDX	ADC clock path DDS chip AD9913, control function register 1
0x00000248	R/W	31:0	SYS_INIT_CCLK_DDS_CFR2_IDX	ADC clock path DDS chip AD9913, control function register 2
0x0000024C	R/W	31:0	SYS_INIT_CCLK_DDS_DAC_IDX	ADC clock path DDS chip AD9913, DAC register
0x00000250	R/W	31:0	SYS_INIT_CCLK_DDS_FTW_IDX	ADC clock path DDS chip AD9913, Frequency Tuning Word register
0x00000254	R/W	31:0	SYS_INIT_CCLK_DDS_PHASE_IDX	ADC clock path DDS chip AD9913, Phase offset register: 0.0 °… 360.0 ° IEEE 754 single precision representation.
0x00000260	R/W	13:0	SYS_INIT_CCLK_PLL_R_IDX	ADC clock path PLL chip ADF4001, R factor
0x00000264	R/W	12:0	SYS_INIT_CCLK_PLL_N_IDX	ADC clock path PLL chip ADF4001, N divider
0x00000268	R/W	0	SYS_INIT_CCLK_PLL_F2_IDX	ADC clock path PLL chip ADF4001, F2 selector: Phase detector polarity.

				'0' = Negative '1' = Positive
0x0000026C	R/W	0	SYS_INIT_CCLK_PLL_F3_IDX	ADC clock path PLL chip ADF4001, F3 selector: Charge pump output. '0' = Normal '1' = Tri stated
0x00000270	R/W	3:0	SYS_INIT_CCLK_PLL_MUX_IDX	ADC clock path PLL chip ADF4001, status pin selector: 0 Status pin = TRI-STATE 1 Status pin = LOCK DET 2 Status pin = N DIV 3 Status pin = DVDD 4 Status pin = R DIV 5 Status pin = N-CH. OD 6 Status pin = SDO 7 Status pin = DGND
0x00000280	R/W	31:0	SYS_INIT_LO_PHASE_IDX	LO phase shifter : 0.0 V… 4.0 V IEEE 754 single precision representation.
0x00000284	R/W	13:0	SYS_INIT_LO_PLL_R_IDX	LO PLL chip ADF4107, R factor
0x00000288	R/W	1:0	SYS_INIT_LO_PLL_P_IDX	LO PLL chip ADF4107, N divider part P 0 P = 8/9 1 P = 16/17 2 P = 32/33 3 P = 64/65
0x0000028C	R/W	12:0	SYS_INIT_LO_PLL_B_IDX	LO PLL chip ADF4107, N divider part B
0x00000290	R/W	5:0	SYS_INIT_LO_PLL_A_IDX	LO PLL chip ADF4107, N divider part A
0x00000294	R/W	0	SYS_INIT_LO_PLL_F2_IDX	LO PLL chip ADF4107, F2 selector: Phase detector polarity. '0' = Negative '1' = Positive
0x00000298	R/W	0	SYS_INIT_LO_PLL_F3_IDX	LO PLL chip ADF4107, F3 selector: Charge pump output. '0' = Normal '1' = Tri stated
0x0000029C	R/W	2:0	SYS_INIT_LO_PLL_MUX_IDX	LO PLL chip ADF4107, status pin selector: 0 Status pin = TRI-STATE 1 Status pin = LOCK DET 2 Status pin = N DIV 3 Status pin = DVDD 4 Status pin = R DIV 5 Status pin = N CH LOCK 6 Status pin = SDO 7 Status pin = DGND
0x000002B0	R/W	31:0	SYS_INIT_LO_PWR_O_IDX	Do not touch this parameter. This is an expert setting for the LO ouput: 0.0 V… 4.0 V IEEE 754 single precision representation.
0x000002B4	R/W	31:0	SYS_INIT_LO_TMP_FBO_IDX	Do not touch this parameter. This is an expert setting for the LO ouput : 0.0 V… 3.3 V IEEE 754 single precision representation.
0x000002C0	R/W	5:0	SYS_INIT_R_DSA_IDX	Attenuator setting in R path: 0 dB … 63 dB
0x000002C4	R/W	5:0	SYS_INIT_X_DSA_IDX	Attenuator setting in X path: 0 dB … 63 dB
0x000002C8	R/W	5:0	SYS_INIT_Y_DSA_IDX	Attenuator setting in Y path:

				0 dB … 63 dB

Table 3: SYS_INIT RFFE Board Register Map

The ADC16HL board is the next board in the processing chain turning the analog pulses into digital 16 bit words.

Address (SYS_INIT)	R/W	Bit	Name	Description
0x00000050	R/W	0	SYS_INIT_PB_INIT_IDX	Initializes the whole ADC16HL board in a sequence which allows all components to startup properly. '0' = Do not initialize. '1' = Start initialization.
0x00000060	R/W	0	SYS_INIT_GOE_IDX	Clock distribution chip LMK01020, Global output disable pin '0' = All the clock outputs are enabled. '1' = All the clock outputs are disabled.
0x00000064	R/W	0	SYS_INIT_SYNC_IDX	Global clock output synchronization pin '0' = All divided clocks are set to logic low. '1' = All divided clocks are activated and will transition to a high state simultaneously.
0x00000068	R/W	0	SYS_INIT_CLK_PD_IDX	Clock distribution chip LMK01020, Power Down command '0' = The chip is powered up. '1' = The chip is powered down.
0x0000006C	R/W	0	SYS_INIT_CLK_EN_IDX	Clock distribution chip LMK01020, output enable command '0' = The chip has outputs disabled. '1' = The chip has outputs enabled.
0x00000070	R/W	0	SYS_INIT_CLK_VBOOST_IDX	
0x00000074	R/W	0	SYS_INIT_CLK_SEL_IDX	Clock distribution chip LMK01020, input selector command '0' = Input is local oscillator. '1' = Input is SMA connector.
0x00000078	R/W	0	SYS_INIT_SCK_OE_IDX	Local oscillator SL570 clock output enable '0' = clock disable '1' = clock enable
0x00000080	R/W	0	SYS_INIT_ADC_SHDN_IDX	Power shutdown pin '0' = Normal operation '1' = Chip powered down
0x00000090	R/W	1:0	SYS_INIT_FPGA_CLK_MUX_IDX	Clock distribution chip LMK01020, output selector: 0 Bypassed 1 Divided 2 Delayed 3 Divided and Delayed
0x00000094	R/W	7:0	SYS_INIT_FPGA_CLK_DIV_IDX	Clock distribution chip LMK01020, output divider. (1 to 255) 0 Invalid 1 divide by 2 2 divide by 4 3 divide by 6 4 divide by 8 5 divide by 10 … … 255 divide by 510

0x00000098	R/W	3:0	SYS_INIT_FPGA_CLK_DLY_IDX	Clock distribution chip LMK01020, output delay in 150 ps steps. 0 0 ps 1 150 ps 2 300 ps 3 450 ps 4 600 ps 5 750 ps 6 900 ps 7 1050 ps 8 1200 ps 9 1350 ps 10 1500 ps 11 1650 ps 12 1800 ps 13 1950 ps 14 2100 ps 15 2250 ps
0x000000A0	R/W	1:0	SYS_INIT_PWR_CLK_MUX_IDX	Clock distribution chip LMK01020, output selector. For details please check SYS_INIT_FPGA_CLK_MUX_IDX
0x000000A4	R/W	7:0	SYS_INIT_PWR_CLK_DIV_IDX	Clock distribution chip LMK01020, output divider. (1 to 255). For details please check SYS_INIT_FPGA_CLK_DIV_IDX
0x000000A8	R/W	3:0	SYS_INIT_PWR_CLK_DLY_IDX	Clock distribution chip LMK01020, output delay in 150 ps steps. For details please check SYS_INIT_FPGA_CLK_DLY_IDX
0x000000B0	R/W	0	SYS_INIT_ADC0_PGA_IDX	Programmable gain amplifier control pin ‘0’ = Gain of 1, input range of 2.25 Vpp ‘1’ = Gain of 1.5, input range of 1.5 Vpp
0x000000B4	R/W	31:0	SYS_INIT_ADC0_DAC_OFS_IDX	Offset DAC chip DAC7512, output voltage: 0.25 V… 2 V IEEE 754 single precision representation.
0x000000B8	R/W	1:0	SYS_INIT_ADC0_DAC_MUX_IDX	Offset DAC chip DAC7512, output mux: “00” = Normal Operation “01” = Power down output 1 kΩ to GND “10” = Power down output 100 kΩ to GND “11” = Power down High-Z
0x000000BC	R/W	1:0	SYS_INIT_ADC0_CLK_MUX_IDX	Clock distribution chip LMK01020, output selector. For details please check SYS_INIT_FPGA_CLK_MUX_IDX
0x000000C0	R/W	7:0	SYS_INIT_ADC0_CLK_DIV_IDX	Clock distribution chip LMK01020, output divider. (1 to 255). For details please check SYS_INIT_FPGA_CLK_DIV_IDX
0x000000C4	R/W	3:0	SYS_INIT_ADC0_CLK_DLY_IDX	Clock distribution chip LMK01020, output delay in 150 ps steps. For details please check SYS_INIT_FPGA_CLK_DLY_IDX
0x000000D0	R/W	0	SYS_INIT_ADC1_PGA_IDX	Programmable gain amplifier control pin ‘0’ = Gain of 1, input range of 2.25 Vpp ‘1’ = Gain of 1.5, input range of 1.5 Vpp
0x000000D4	R/W	31:0	SYS_INIT_ADC1_DAC_OFS_IDX	Offset DAC chip DAC7512, output voltage: 0.25 V… 2 V IEEE 754 single precision representation.
0x000000D8	R/W	1:0	SYS_INIT_ADC1_DAC_MUX_IDX	Offset DAC chip DAC7512, output mux: “00” = Normal Operation “01” = Power down output 1 kΩ to GND “10” = Power down output 100 kΩ to GND “11” = Power down High-Z
0x000000DC	R/W	1:0	SYS_INIT_ADC1_CLK_MUX_IDX	Clock distribution chip LMK01020, output selector. For details please check

				SYS_INIT_FPGA_CLK_MUX_IDX
0x000000E0	R/W	7:0	SYS_INIT_ADC1_CLK_DIV_IDX	Clock distribution chip LMK01020, output divider. (1 to 255). For details please check SYS_INIT_FPGA_CLK_DIV_IDX
0x000000E4	R/W	3:0	SYS_INIT_ADC1_CLK_DLY_IDX	Clock distribution chip LMK01020, output delay in 150 ps steps. For details please check SYS_INIT_FPGA_CLK_DLY_IDX
0x000000F0	R/W	0	SYS_INIT_ADC2_PGA_IDX	Programmable gain amplifier control pin '0' = Gain of 1, input range of 2.25 Vpp '1' = Gain of 1.5, input range of 1.5 Vpp
0x000000F4	R/W	31:0	SYS_INIT_ADC2_DAC_OFS_IDX	Offset DAC chip DAC7512, output voltage: 0.25 V… 2 V IEEE 754 single precision representation.
0x000000F8	R/W	1:0	SYS_INIT_ADC2_DAC_MUX_IDX	Offset DAC chip DAC7512, output mux: "00" = Normal Operation "01" = Power down output 1 kΩ to GND "10" = Power down output 100 kΩ to GND "11" = Power down High-Z
0x000000FC	R/W	1:0	SYS_INIT_ADC2_CLK_MUX_IDX	Clock distribution chip LMK01020, output selector. For details please check SYS_INIT_FPGA_CLK_MUX_IDX
0x00000100	R/W	7:0	SYS_INIT_ADC2_CLK_DIV_IDX	Clock distribution chip LMK01020, output divider. (1 to 255). For details please check SYS_INIT_FPGA_CLK_DIV_IDX
0x00000104	R/W	3:0	SYS_INIT_ADC2_CLK_DLY_IDX	Clock distribution chip LMK01020, output delay in 150 ps steps. For details please check SYS_INIT_FPGA_CLK_DLY_IDX
0x00000110	R/W	0	SYS_INIT_ADC3_PGA_IDX	Programmable gain amplifier control pin '0' = Gain of 1, input range of 2.25 Vpp '1' = Gain of 1.5, input range of 1.5 Vpp
0x00000114	R/W	31:0	SYS_INIT_ADC3_DAC_OFS_IDX	Offset DAC chip DAC7512, output voltage: 0.25 V… 2 V IEEE 754 single precision representation.
0x00000118	R/W	1:0	SYS_INIT_ADC3_DAC_MUX_IDX	Offset DAC chip DAC7512, output mux: "00" = Normal Operation "01" = Power down output 1 kΩ to GND "10" = Power down output 100 kΩ to GND "11" = Power down High-Z
0x0000011C	R/W	1:0	SYS_INIT_ADC3_CLK_MUX_IDX	Clock distribution chip LMK01020, output selector. For details please check SYS_INIT_FPGA_CLK_MUX_IDX
0x00000120	R/W	7:0	SYS_INIT_ADC3_CLK_DIV_IDX	Clock distribution chip LMK01020, output divider. (1 to 255). For details please check SYS_INIT_FPGA_CLK_DIV_IDX
0x00000124	R/W	3:0	SYS_INIT_ADC3_CLK_DLY_IDX	Clock distribution chip LMK01020, output delay in 150 ps steps. For details please check SYS_INIT_FPGA_CLK_DLY_IDX
0x00000130	R/W	0	SYS_INIT_ADC4_PGA_IDX	Programmable gain amplifier control pin '0' = Gain of 1, input range of 2.25 Vpp '1' = Gain of 1.5, input range of 1.5 Vpp
0x00000134	R/W	31:0	SYS_INIT_ADC4_DAC_OFS_IDX	Offset DAC chip DAC7512, output voltage: 0.25 V… 2 V IEEE 754 single precision representation.
0x00000138	R/W	1:0	SYS_INIT_ADC4_DAC_MUX_IDX	Offset DAC chip DAC7512, output mux: "00" = Normal Operation "01" = Power down output 1 kΩ to GND "10" = Power down output 100 kΩ to GND "11" = Power down High-Z
0x0000013C	R/W	1:0	SYS_INIT_ADC4_CLK_MUX_IDX	Clock distribution chip LMK01020, output selector. For details please check

				SYS_INIT_FPGA_CLK_MUX_IDX
0x00000140	R/W	7:0	SYS_INIT_ADC4_CLK_DIV_IDX	Clock distribution chip LMK01020, output divider. (1 to 255). For details please check SYS_INIT_FPGA_CLK_DIV_IDX
0x00000144	R/W	3:0	SYS_INIT_ADC4_CLK_DLY_IDX	Clock distribution chip LMK01020, output delay in 150 ps steps. For details please check SYS_INIT_FPGA_CLK_DLY_IDX
0x00000150	R/W	0	SYS_INIT_ADC5_PGA_IDX	Programmable gain amplifier control pin '0' = Gain of 1, input range of 2.25 Vpp '1' = Gain of 1.5, input range of 1.5 Vpp
0x00000154	R/W	31:0	SYS_INIT_ADC5_DAC_OFS_IDX	Offset DAC chip DAC7512, output voltage: 0.25 V… 2 V IEEE 754 single precision representation.
0x00000158	R/W	1:0	SYS_INIT_ADC5_DAC_MUX_IDX	Offset DAC chip DAC7512, output mux: "00" = Normal Operation "01" = Power down output 1 kΩ to GND "10" = Power down output 100 kΩ to GND "11" = Power down High-Z
0x0000015C	R/W	1:0	SYS_INIT_ADC5_CLK_MUX_IDX	Clock distribution chip LMK01020, output selector. For details please check SYS_INIT_FPGA_CLK_MUX_IDX
0x00000160	R/W	7:0	SYS_INIT_ADC5_CLK_DIV_IDX	Clock distribution chip LMK01020, output divider. (1 to 255). For details please check SYS_INIT_FPGA_CLK_DIV_IDX
0x00000164	R/W	3:0	SYS_INIT_ADC5_CLK_DLY_IDX	Clock distribution chip LMK01020, output delay in 150 ps steps. For details please check SYS_INIT_FPGA_CLK_DLY_IDX

Table 4: SYS_INIT ADC16HL Board Register Map

The timing setting in the GPAC shall account for the relative position of the pulse to the event system of the machine. In addition the pulse measure duration and trigger mode are configurable.

Address (SYS_INIT)	**R/W**	**Bit**	**Name**	**Description**
0x00000000	R/W	0	SYS_INIT_SMP_INIT_IDX	Initializes the whole BPM system be individually calling the board init in a sequence which allows all components to startup properly. '0' = Do not initialize. '1' = Start initialization.
0x00000010	R/W	0	SYS_INIT_SMP_ENA_IDX	FSM enable. '0' = Put FSM to idle state. '1' = Start process of sampling data of a bunch train after triggering (external or signal trigger).
0x00000014	R/W	0	SYS_INIT_SMP_MODE_IDX	FSM mode 0 = External Trigger (which means external trigger connected to the GPAC BPM FPGA, this should be the bunch train trigger) 1 = Signal Trigger (Which means to trigger on a reference channel value threshold)
0x00000018	R/W	15:0	SYS_INIT_SMP_TRIG_VAL_IDX	Trigger value for self-triggered mode.
0x00000020	R/W	11:0	SYS_INIT_SMP_B0_0_IDX	Number of bunches expected. Corresponds

				to B0.0: 1 … 4'095 bunches
0x00000024	R/W	22:0	SYS_INIT_SMP_B1_0_IDX	Number of clock cycles delay if mode is in "External Trigger". Corresponds to B1.0: 1 … 8'000'000 clock cycles
0x00000028	R/W	11:0	SYS_INIT_SMP_B2_0_IDX	Clock cycles between bunches. Corresponds to B2.0: 1 … 4'095 clock cycles
0x0000002C	R/W	26:0	SYS_INIT_SMP_B3_0_IDX	Timeout for external trigger. After this time in units of clock cycles the trigger is issued and starts reading the samples. Corresponds to B3.0: 1 … 134'217'727 clock cycles
0x00000030	R/W	7:0	SYS_INIT_SMP_S1_0_IDX	Number of clock cycles delay between the internal bunch trigger (adc_trig) until start of processing the sampled data: 1 … 255 clock cycles
0x00000034	R/W	7:0	SYS_INIT_SMP_S1_1_IDX	Number of ADC samples requested per bunch: 1 … 255 samples
0x00000038	R/W	7:0	SYS_INIT_SMP_S1_2_IDX	Presamples. If SYS_INIT_SMP_MODE_IDX is set to mode "Signal Triggered" then this setting defines the number of samples priors the threshold. The sampling is triggered when a rising edge of the signal is detected (similar to an oscilloscope) with a predefined number of presamples. This setting here is basically the number of presamples required: 1 … 255 samples

Table 5: SYS_INIT GPAC Timing Register Map

3.2 Calculation Pipeline

The processing of the digitized data is carried out in the BPM FPGA of the GPAC in a firmware component called "bpm_cav_exfel" [3].
In a first step the peak of the reference I/Q ADC data has to be found inside the sampling window by the block called MAX.
After finding the I/Q peaks, a conversion from cartesian to polar coordinates are calculated (in the block CORDIC). The amplitudes (x_cd_amp, y_cd_amp and r_cd_amp) and phases (x_cd_phase, y_cd_phase and r_cd_phase) are stored for each bunch separately and can be retrieved by the control system. At the same time the Interpolation block calculates by means of a second order interpolation the top sample (s_top) and the deviation in degrees (t_top) from the peak is sampled. This information is important for a feedback which keeps the sampling point at the top of the analogue I/Q pulse.
The next calculation steps are performed for correcting various effects. First the I/Q imbalance is corrected, then a correction which accounts for the attenuator variation is done and finally a beam angle correction needs to be applied.
The next step is to divide the pickup position information with the charge in order to obtain the charge independent position information followed by scaling (x_egu, y_egu q_egu) to physical units [mm and pC].

To enable comparison of position information for several pickups, the mechanical shifts (rotation of the pickup compared to an arbitrary reference) have to be calculated. This is carried out by a rotation matrix (rot11…rot22) before the samples are stored in user accessible buffers.

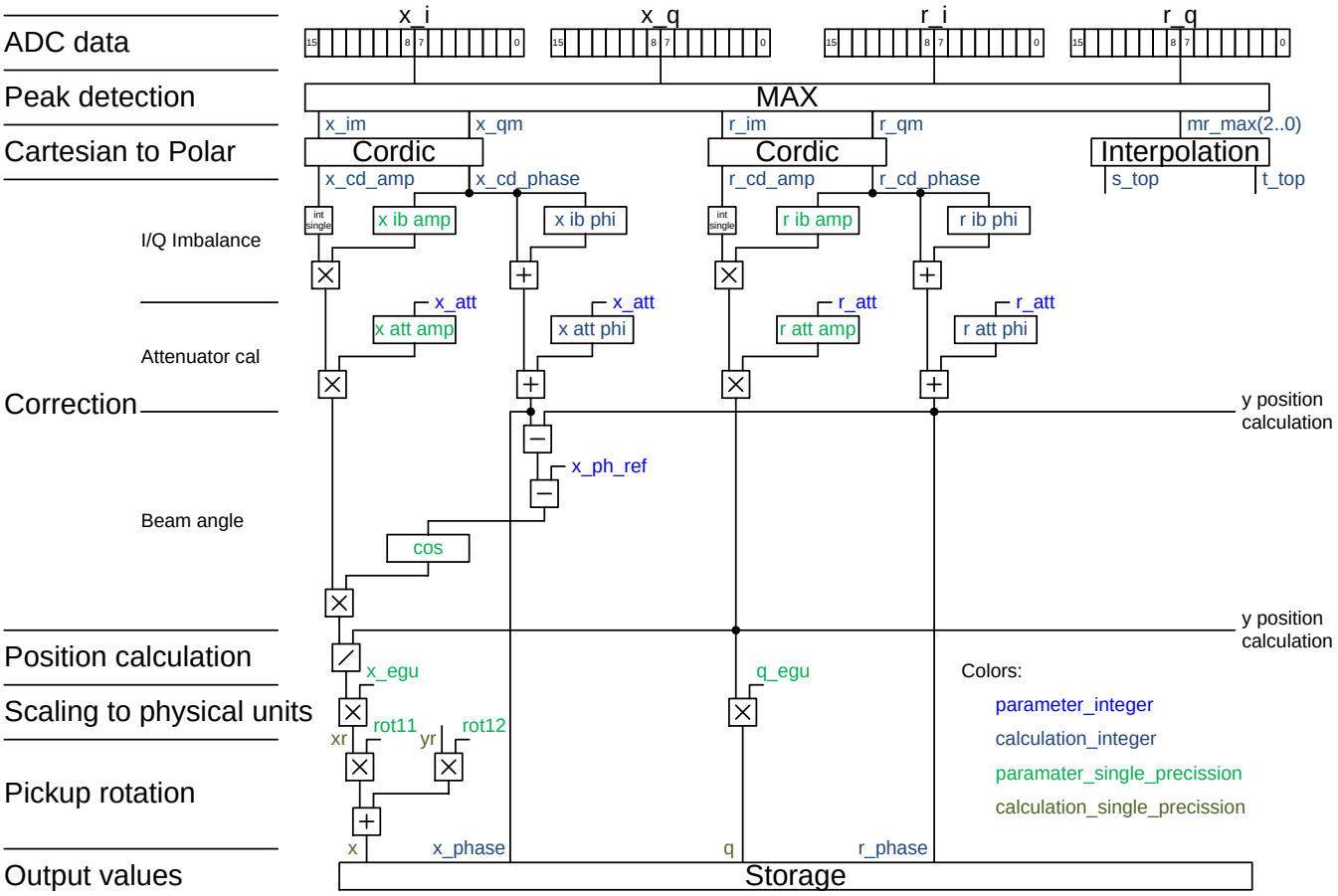

Figure 6: Calculation Pipeline

All the calculations so far are implemented in firmware due to performance reasons and to keep the latency as low as possible.
Please note: The BPM system is the base of many intra-train feedback systems and shall add only marginal latency to the feedback loop.

In addition there are slow drift effects which can influence the measurement and which are as well implemented on the GPAC. Because some effects are very slow we have implemented them in software instead of spending FPGA fabric resources.

For the sampling of the ADC data by means of the FPGA clock it is important to find a clean sampling position. This is as well important die to the individual delays of ADC clocks.

Address (SYS_INIT)	R/W	Bit	Name	Description
0x00000170	R/W	0	SYS_INIT_ADC_SYNC_IDX	Synchronize the ADC data streams arriving at the FPGA: ‘0’ = Sample ‘1’ = Synchronize

Table 6: SYS_INIT GPAC ADC Data Synchronization Register Map

The first correction to be applied is the baseline subtraction. After the baseline subtraction all ADC values are using a common 0 (common ground) value and the I and Q samples can be used in following calculations.

Address (SYS_INIT)	R/W	Bit	Name	Description
0x00000040	R/W	0	SYS_INIT_BL_ENA_IDX	Baseline enable '0' = Baseline calculation disabled '1' = Baseline calculation enables
0x00000044	R/W	3:0	SYS_INIT_BL_EXP_IDX	Baseline samples used for calculation set as 2^x 0 = 1 sample 1 = 2 samples 2 = 4 samples 3 = 8 samples 4 = 16 samples all other settings = 16 samples (same as setting 4)
0x00000048	R/W	9:0	SYS_INIT_BL_DEL_IDX	Baseline delay to the current measurement in number of clock cycles.

Table 7: SYS_INIT GPAC Baseline Calculation Register Map

The next correction to be applied is the I/Q imbalance correction. Due to analog tolerances the measured values have to be corrected with calibration factors in order to get rid of the tolerance effects.

Address (SYS_INIT)	R/W	Bit	Name	Description
0x00000370	R/W	0	SYS_INIT_IB_ENA_IDX	I/Q imbalance correction enable. '0' = I/Q calculation disabled. This means the amplitude is corrected by multiplying 1.0 and the phase by adding 0.0 °. '1' = I/Q calculation enabled. This means the amplitude is corrected by multiplying the value stored in the amplitude table and the phase by adding the value stored in the phase table
0x00000374	R/W	31:0	SYS_INIT_IB_R_INDEX_IDX	Index into the I/Q correction table for the R channel: 0 … 360
0x00000378	R/W	31:0	SYS_INIT_IB_R_PHASE_IDX	I/Q phase correction value on index SYS_INIT_IB_R_INDEX_IDX in 0.015625 ° steps for the R channel. Fix_point representation 10.6 [°]
0x0000037C	R/W	31:0	SYS_INIT_IB_R_AMPL_IDX	I/Q amplitude correction factor on index SYS_INIT_IB_R_INDEX_IDX for the R channel. IEEE 754 single precision representation.
0x00000384	R/W	31:0	SYS_INIT_IB_X_INDEX_IDX	Index into the I/Q correction table for the X channel:

				0 … 360
0x00000388	R/W	31:0	SYS_INIT_IB_X_PHASE_IDX	I/Q phase correction value on index SYS_INIT_IB_X_INDEX_IDX in 0.015625 ° steps for the X channel. Fix_point representation 10.6 [°]
0x0000038C	R/W	31:0	SYS_INIT_IB_X_AMPL_IDX	I/Q amplitude correction factor on index SYS_INIT_IB_X_INDEX_IDX for the X channel. IEEE 754 single precision representation.
0x00000394	R/W	31:0	SYS_INIT_IB_Y_INDEX_IDX	Index into the I/Q correction table for the Y channel: 0 … 360
0x00000398	R/W	31:0	SYS_INIT_IB_Y_PHASE_IDX	I/Q phase correction value on index SYS_INIT_IB_Y_INDEX_IDX in 0.015625 ° steps for the Y channel. Fix_point representation 10.6 [°]
0x0000039C	R/W	31:0	SYS_INIT_IB_Y_AMPL_IDX	I/Q amplitude correction factor on index SYS_INIT_IB_Y_INDEX_IDX for the Y channel. IEEE 754 single precision representation.

Table 8: SYS_INIT GPAC I/Q Imbalance Correction Register Map

One of the tolerance effects not corrected so far are the attenuator setting. It is clear that a set attenuation 15 dB is most likely not 15.000 dB but close to 15 dB. In addition the attenuator settings are changing as well the phase of the measurement which has to be calculated out by calibration values.

Address (SYS_INIT)	**R/W**	**Bit**	**Name**	**Description**
0x000003A0	R/W	0	SYS_INIT_AC_ENA_IDX	Attenuation calibration enable. '0' = Attenuation calibration disabled. This means the amplitude is corrected by multiplying $10^{\frac{attenautor\_in\_dB-63}{20}}$ and the phase by adding 0.0 °. '1' = Attenuation calibration enabled. This means the amplitude is corrected by multiplying the value stored in the amplitude table and the phase by adding the value stored in the phase table.
0x000003A8	R/W	31:0	SYS_INIT_AC_R_PHASE_IDX	Attenuator phase correction value on currently set attenuation in 0.015625 ° steps for the R channel Fix_point representation 10.6 [°]
0x000003AC	R/W	31:0	SYS_INIT_AC_R_AMPL_IDX	Attenuator amplitude correction factor on currently set attenuation for the R channel. IEEE 754 single precision representation.
0x000003B8	R/W	31:0	SYS_INIT_AC_X_PHASE_IDX	Attenuator phase correction value on currently set attenuation in 0.015625 ° steps for the X channel Fix_point representation 10.6 [°]

0x000003BC	R/W	31:0	SYS_INIT_AC_X_AMPL_IDX	Attenuator amplitude correction factor on currently set attenuation for the X channel. IEEE 754 single precision representation.
0x000003C8	R/W	31:0	SYS_INIT_AC_Y_PHASE_IDX	Attenuator phase correction value on currently set attenuation in 0.015625 ° steps for the Y channel Fix_point representation 10.6 [°]
0x000003CC	R/W	31:0	SYS_INIT_AC_Y_AMPL_IDX	Attenuator amplitude correction factor on currently set attenuation for the Y channel. IEEE 754 single precision representation.

Table 9: SYS_INIT GPAC I/Q Attenuator Calibration Register Map

There is as well an effect on the measurement if the beam passes the pickup in an angle. The error introduced is relatively getting bigger the closer the beam passes the electrical center of the pickup (the ADC values are very small and the beam angle component dominates the measurement).

Address (SMP_ADDR_REG)	R/W	Bit	Name	Description
0x000000B0	R/W	0	SYS_INIT_BA_ENA_IDX	Beam angle correction enable. '0' = Beam angle correction disabled. This means the amplitude is corrected by multiplying 1.0. '1' = Beam angle correction enabled. This means the amplitude is corrected by multiplying the cosine of the calculated projection angle.
0x000000B6	R/W	15:0	SYS_INIT_BA_X_IDX	Angle between reference channel and large X position channel amplitude. Fix_point representation 10.6 [°]
0x000000BA	R/W	15:0	SYS_INIT_BA_Y_IDX	Angle between reference channel and large Y position channel amplitude. Fix_point representation 10.6 [°]

Table 10: SYS_INIT GPAC Beam Angle Register Map

The scaling to engineering units is one of the final steps done by the calculation pipeline. This step is split into two scaling factors. The scaling factor containing "_EGU_" is the one which is calibrated in the lab with the expected beam response. The other scaling factor shall account for the cabling attenuation and pickup variation and has to be set when a beam based calibration is performed.

Address (SYS_INIT)	R/W	Bit	Name	Description
0x00000348	R/W	31:0	SYS_INIT_R_SCALE_EGU_IDX	A scaling factor which is used for the lab calibrated scaling. IEEE 754 single precision representation.
0x0000034C	R/W	31:0	SYS_INIT_X_SCALE_EGU_IDX	A scaling factor which is used for the lab calibrated scaling.

				IEEE 754 single precision representation.
0x00000350	R/W	31:0	SYS_INIT_Y_SCALE_EGU_IDX	A scaling factor which is used for the lab calibrated scaling. IEEE 754 single precision representation.
0x00000354	R/W	31:0	SYS_INIT_R_SCALE_IDX	A scaling factor which is used for the user calibrated scaling. IEEE 754 single precision representation.
0x00000358	R/W	31:0	SYS_INIT_X_SCALE_IDX	A scaling factor which is used for the user scaling. IEEE 754 single precision representation.
0x0000035C	R/W	31:0	SYS_INIT_Y_SCALE_IDX	A scaling factor which is used for the user scaling. IEEE 754 single precision representation.

Table 11: SYS_INIT GPAC Scaling Register Map

In order to correct the effects of the beam angle another measurement has to be done if high accuracy is required. The beam is set such that it passes the pickup at a high position offset and the angle between the reference channel and the position channels is recorded and used as a reference for the beam angle correction. This procedure can be automated by the following software task.

Address (SYS_INIT)	R/W	Bit	Name	Description
0x00000334	R/W	0	SYS_INIT_BA_FB_ENA_IDX	Beam angle feedback enable: '0' = Feedback disable '1' = Feedback enable
0x00000338	R/W	31:0	SYS_INIT_BA_FB_THR_IDX	Position threshold from which value on to retrieve a new angle and write it to the beam angle correction register [mm]. IEEE 754 single precision representation

Table 12: SYS_INIT GPAC Beam Angle Feedback Register Map

For the user it might be interesting to know what the average charge of a longer bunch-train was and the average positions X and Y of the bunch train. Of course the user has to avoid to interpret gaps in the bunch train as charge and position, hence only bunches which are bigger than a charge threshold are considered in the average.

Address (SYS_INIT)	R/W	Bit	Name	Description
0x000003D0	R/W	31:0	SYS_INIT_Q_FB_THR_IDX	Charge threshold needed for various calculations [pC]. IEEE 754 single precision representation
0x000003E0	R/W	31:0	SYS_INIT_Q_TRAIN_AVG_IDX	Average of the bunch train charge for each bunch which is charge is bigger than the threshold defined by

				SYS_INIT_Q_FB_THR_IDX. IEEE 754 single precision representation
0x000003E4	R/W	31:0	SYS_INIT_X_TRAIN_AVG_IDX	Average of the bunch train X position for each bunch which is charge is bigger than the threshold defined by SYS_INIT_Q_FB_THR_IDX. IEEE 754 single precision representation
0x000003E8	R/W	31:0	SYS_INIT_Y_TRAIN_AVG_IDX	Average of the bunch train Y position for each bunch which is charge is bigger than the threshold defined by SYS_INIT_Q_FB_THR_IDX. IEEE 754 single precision representation

Table 13: SYS_INIT GPAC Train Average Register Map

3.3 Sampling Time Feedback (DDS Feedback)

The sampling clock used by the ADCs is as well generated in the RFFE board. In order to minimize effects caused by the sampling clock jitter, the ADC sampling point shall be at the top of the I and Q pulse. Due to the same source of LO path and ADC clock generation in the RFFE board the sampling will have a fixed phase. The clock generation contains a DDS (Direct Digital Synthesis) chip which is basically a phase counter, phase offset register, phase-to-amplitude lookup table and a DAC. The phase offset register in the DDS chip is hence a simple way to move the ADC sampling clock in time (phase difference to the pickup signal)

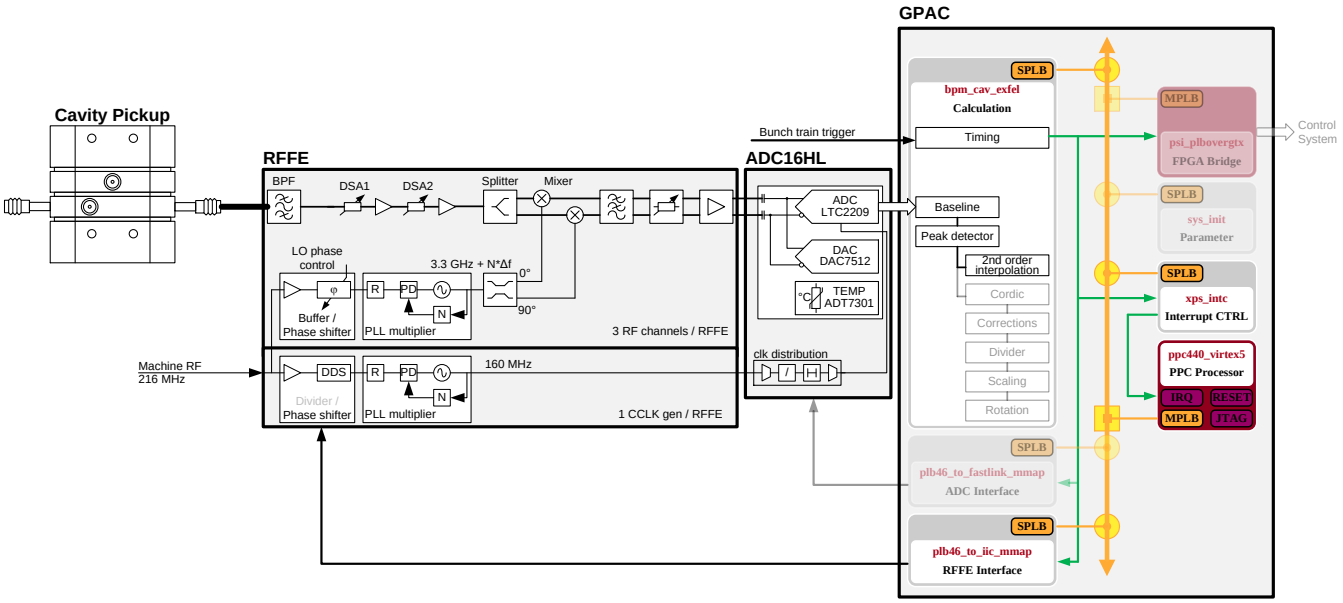

Figure 7: Sampling Time Feedback

The GPAC calculates from the 3 top samples of the pulse by means of a second order interpolation the top sample amplitude and the top sample phase. The top sample phase in turn is used in a software implemented PI feedback loop to control the DDS phase offset register.

In order to keep the ADC sampling of the I/Q pulse at the top, a feedback is implemented in the GPAC varying the DDS phase such that the desired second interpolation top phase is met. The feedback is basically a PI controller and due to its nature to correct slow drifts not a very performant implementation. This PI controller runs slowly in a software interrupt context.

Address (SYS_INIT)	R/W	Bit	Name	Description
0x000002E0	R/W	0	SYS_INIT_PHASE_FB_ON_IDX	Sampling point feedback enable: '0' = Feedback disable '1' = Feedback enable
0x000002E4	R/W	31:0	SYS_INIT_PHASE_FB_REF_IDX	The reference angle which shall be regulated to [°]. IEEE 754 single precision representation
0x000002E8	R/W	31:0	SYS_INIT_PHASE_FB_KP_IDX	The proportional factor for the PI controller. IEEE 754 single precision representation
0x000002EC	R/W	31:0	SYS_INIT_PHASE_FB_KI_IDX	The integral factor for the PI controller. IEEE 754 single precision representation
0x000003D0	R/W	31:0	SYS_INIT_Q_FB_THR_IDX	Charge threshold needed for various calculations [pC]. IEEE 754 single precision representation

Table 14: SYS_INIT GPAC Sampling Phase Feedback Register Map

3.4 I/Q Phase Feedback

For the measurement accuracy it makes sense if the two ADC channels I and Q are both at full range. If the I and Q channel have the same amplitude then this leads to a 45° angle between I and Q value which in turn is the output of the CORDIC calculation. All we need to do, is to keep the I/Q phase of the reference channel at 45° by means of the LO phase shifter. This calculation is done as well in software with a simple PI feedback controller.

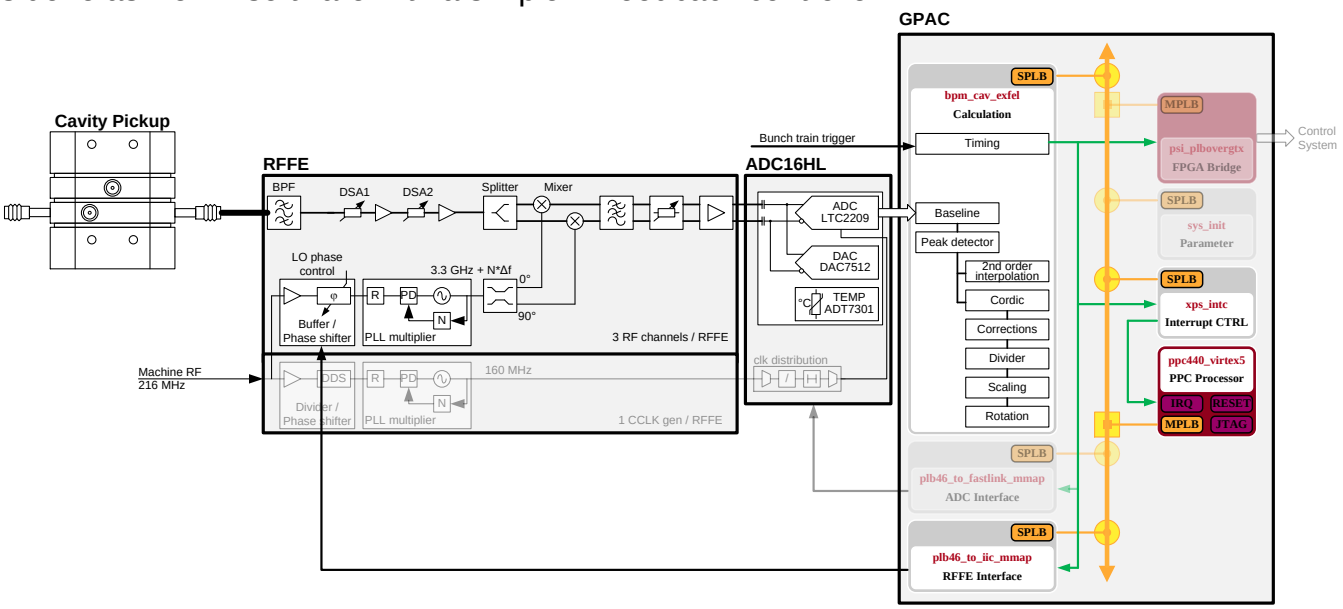

Figure 8: I/Q Phase Feedback

In order to minimize the sample to noise ratio both (I and Q) ADC samples are used at a high value. For this a feedback is implemented in the GPAC varying the LO phase such that the desired angle between I and Q is close to 45°. The feedback is basically a PI controller and due to its nature to correct slow drifts not a very performant implementation. This PI controller runs slowly in a software interrupt context.

Address (SYS_INIT)	R/W	Bit	Name	Description
0x00000300	R/W	0	SYS_INIT_PH_REF_FB_ON_IDX	I/Q phase feedback enable: '0' = Feedback disable '1' = Feedback enable
0x00000304	R/W	31:0	SYS_INIT_PH_REF_FB_REF_IDX	The reference angle which shall be regulated to [°]. IEEE 754 single precision representation
0x00000308	R/W	31:0	SYS_INIT_PH_REF_FB_KP_IDX	The proportional factor for the PI controller. IEEE 754 single precision representation
0x0000030C	R/W	31:0	SYS_INIT_PH_REF_FB_KI_IDX	The integral factor for the PI controller. IEEE 754 single precision representation
0x000003D0	R/W	31:0	SYS_INIT_Q_FB_THR_IDX	Charge threshold needed for various calculations [pC]. IEEE 754 single precision representation

Table 15: SYS_INIT GPAC I/Q Phase Feedback Register Map

3.5 Attenuator Feedback

The charge of the beam can be changed over a wide range. In order to adjust for high beam currents attenuators are included in the RFFE board. These attenuators are automatically driven by the GPAC in a feedback in order to use the full range of the ADC independently from the beam charge set.

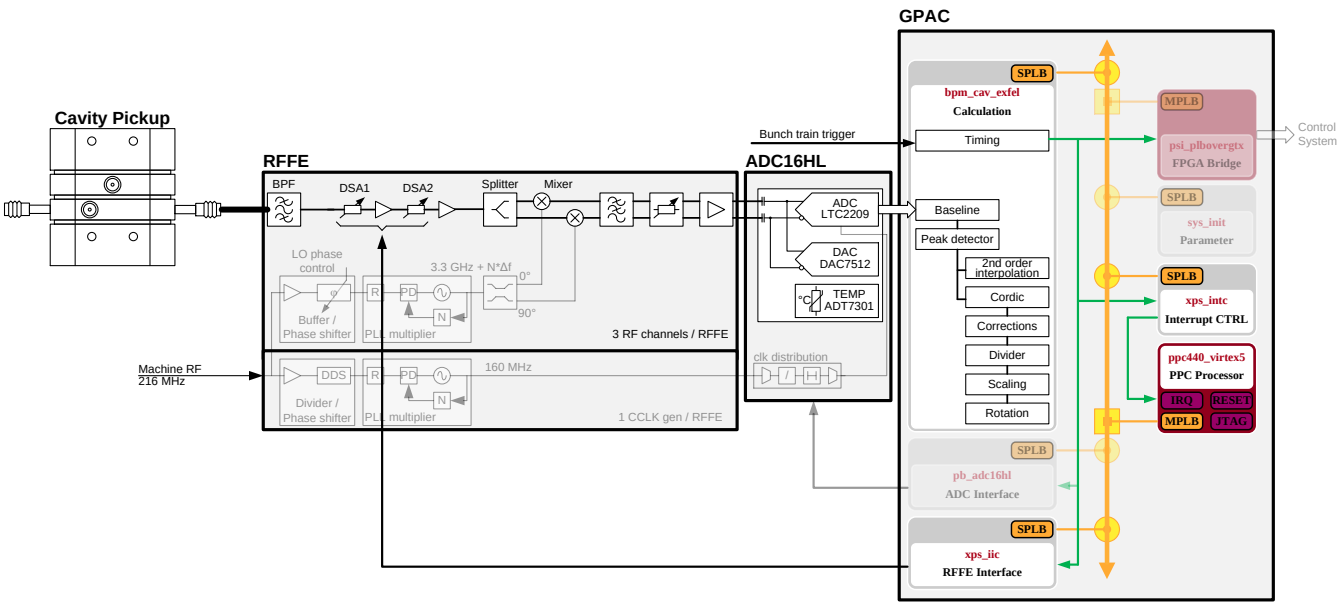

Figure 9: Attenuator Feedback

The attenuation feedback is an advanced feedback based on the experience and not a purely mathematical model of a simple feedback controller. Hence the following figures are added to explain the behavior requested in the project.

Assume first the cases where the attenuators are kept as they are. The aim was that if even one bunch of a longer train of bunches is in a valid range to prevent switching.

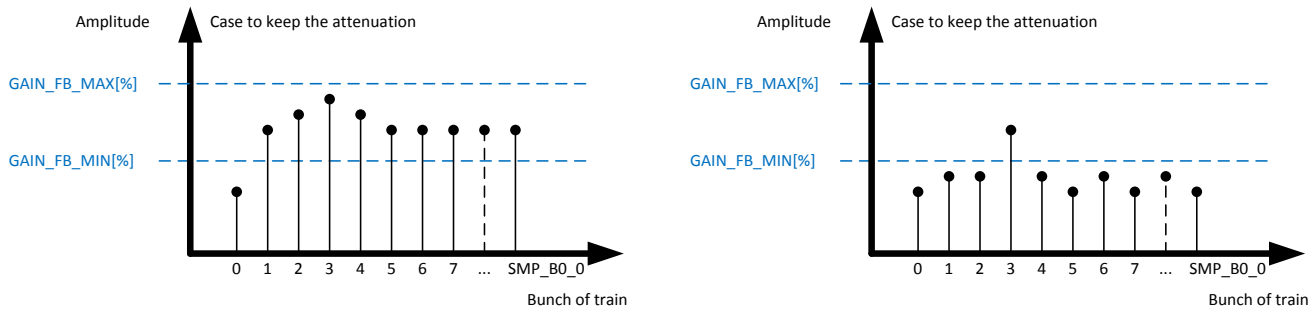

Figure 10: Attenuator Feedback Unchanged Value

If at least one measurement is above the upper limit then the attenuation is increased my GAIN_FB_ATT_INC. This attenuation increment value is set by the user to adapt how fast the range of the measured properties (charge or position) will be increased.

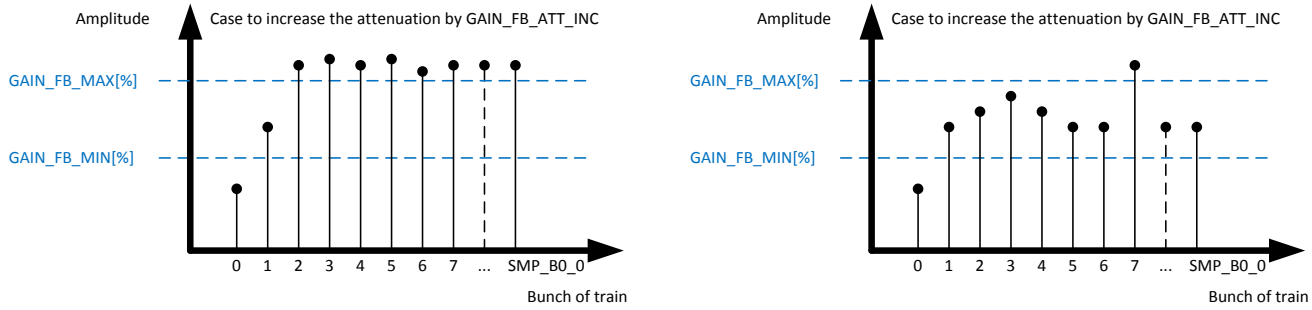

Figure 11: Attenuator Feedback Increased Value

One special case is to note: If the ADCs are driven to the max then the increase will be at least 6 dB (doubling the measurement range).

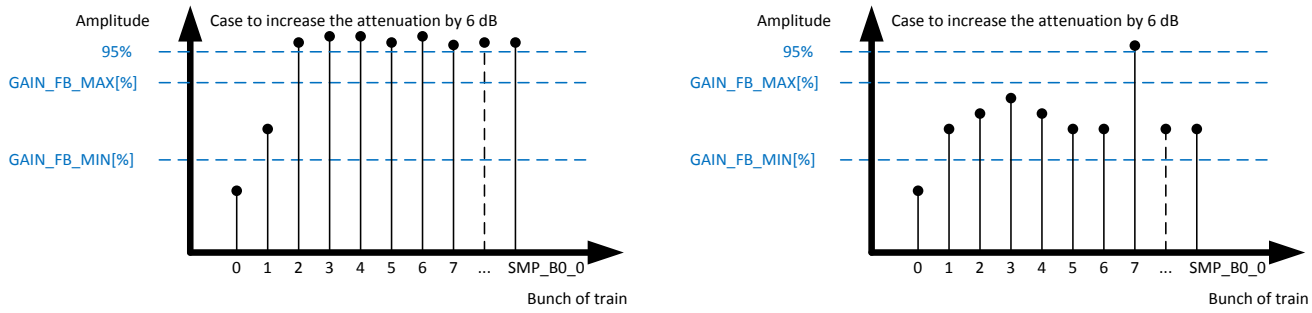

Figure 12: Attenuator Feedback Increased Value

If the measured property is lower than the limit, then the attenuation is decreased after a user settable, consecutive occurrence of the detected decrease.
Please note: The attenuator is only decreased if GAIN_FB_MIN_CNT number of consecutive low bunches are detected. This means: If at least one bunch is considered ok then then again a whole set of GAIN_FB_MIN_CNT consecutive bunches are needed to decrease attenuation.

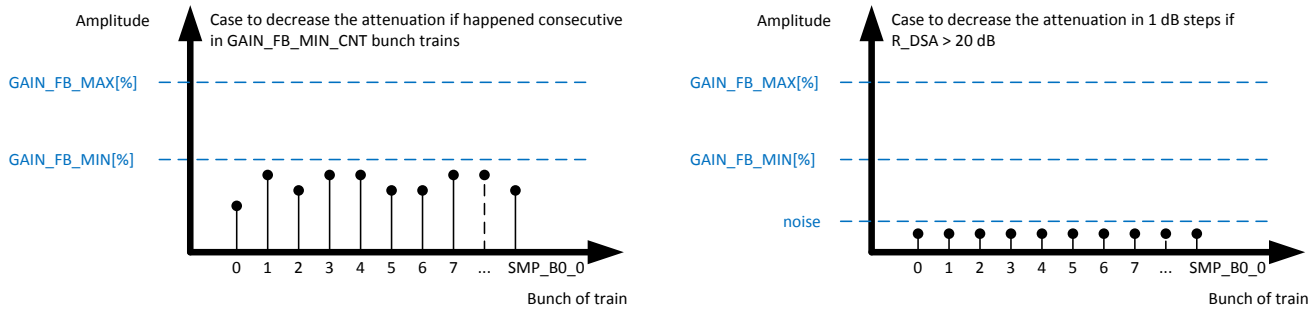

Figure 13: Attenuator Feedback Decreased Value

As well here one special case is if the measurement is hidden in the noise floor due to high attenuation set. In such a case the attenuation is decreased down to 20 dB in order to search for the beam.

Address (SYS_INIT)	R/W	Bit	Name	Description
0x00000320	R/W	0	SYS_INIT_REF_GAIN_FB_ON_IDX	Attenuator feedback enable for R channel: '0' = Feedback disable '1' = Feedback enable
0x00000324	R/W	0	SYS_INIT_X_GAIN_FB_ON_IDX	Attenuator feedback enable for X channel: '0' = Feedback disable '1' = Feedback enable
0x00000328	R/W	0	SYS_INIT_Y_GAIN_FB_ON_IDX	Attenuator feedback enable for Y channel: '0' = Feedback disable '1' = Feedback enable
0x00000400	R/W	6:0	SYS_INIT_REF_GAIN_FB_MAX_IDX	Upper limit in [%] to increase attenuation. Naturally the range is from 0% to 100% In addition the upper limit has to be 10% bigger than the lower range.
0x00000404	R/W	6:0	SYS_INIT_REF_GAIN_FB_MIN_IDX	Lower limit in [%] to decrease attenuation. Naturally the range is from 0% to 100% In addition the upper limit has to be 10% bigger than the lower range.
0x00000408	R/W	31:0	SYS_INIT_REF_GAIN_FB_MIN_CNT_IDX	Consecutive occurrences needed in order to decrease attenuation. This is basically a delay when to react or better to say how long to tolerate a too small signal before decreasing

				the attenuation to prevent the attenuators to switch too often.
0x0000040C	R/W	5:0	SYS_INIT_REF_GAIN_FB_ATT_INC_IDX	Value to increase attenuation if at upper limit. Range 1 to 63 [dB]
0x00000420	R/W	6:0	SYS_INIT_X_GAIN_FB_MAX_IDX	Upper limit in [%] to increase attenuation. Naturally the range is from 0% to 100% In addition the upper limit has to be 10% bigger than the lower range.
0x00000424	R/W	6:0	SYS_INIT_X_GAIN_FB_MIN_IDX	Lower limit in [%] to decrease attenuation. Naturally the range is from 0% to 100% In addition the upper limit has to be 10% bigger than the lower range.
0x00000428	R/W	31:0	SYS_INIT_X_GAIN_FB_MIN_CNT_IDX	Consecutive occurrences needed in order to decrease attenuation. This is basically a delay when to react or better to say how long to tolerate a too small signal before decreasing the attenuation to prevent the attenuators to switch too often.
0x0000042C	R/W	5:0	SYS_INIT_X_GAIN_FB_ATT_INC_IDX	Value to increase attenuation if at upper limit. Range 1 to 63 [dB]
0x00000440	R/W	6:0	SYS_INIT_Y_GAIN_FB_MAX_IDX	Upper limit in [%] to increase attenuation. Naturally the range is from 0% to 100% In addition the upper limit has to be 10% bigger than the lower range.
0x00000444	R/W	6:0	SYS_INIT_Y_GAIN_FB_MIN_IDX	Lower limit in [%] to decrease attenuation. Naturally the range is from 0% to 100% In addition the upper limit has to be 10% bigger than the lower range.
0x00000448	R/W	31:0	SYS_INIT_Y_GAIN_FB_MIN_CNT_IDX	Consecutive occurrences needed in order to decrease attenuation. This is basically a delay when to react or better to say how long to tolerate a too small signal before decreasing the attenuation to prevent the attenuators to switch too often.
0x0000044C	R/W	5:0	SYS_INIT_Y_GAIN_FB_ATT_INC_IDX	Value to increase attenuation if at upper limit. Range 1 to 63 [dB]

Table 16: SYS_INIT GPAC Attenuator Feedback Register Map

4 Appendix

None.