R61526

262,144–Color, 240x320-Dot Graphics LCD Controller Driver for a-Si TFT Panel

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Rev.1.10a
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Description

The R61526 is a single-chip liquid crystal controller driver LSI for a-Si TFT panel, incorporating frame memory for a maximum 240RGB x 320-dot graphics display, source driver, gate driver and a power supply circuit. For efficient data transfer, it supports high-speed interface via 8-/9-/16-/18-bit ports as system interface to the host processor. The R61526 supports also RGB interface compliant with MIPI DPI (VSYNC, HSYNC, PCLK, DE and DB[17:0]) to display moving images.

The power supply circuit incorporates step-up circuits and voltage follower circuits to generate voltage levels to drive TFT liquid crystal panel.

The R61526's power management functions including 8-color display and the sleep mode make this LSI an ideal driver for the med and small sized portable devices with color display systems such as digital cellular phones or small PDAs, where long battery life is a major concern.

Features

- A single-chip controller driver incorporating gate and a power supply circuits for a maximum 240RGB x 320-dot graphics display on amorphous TFT panel
  - System interface
    MIPI DBI (Compliant with MIPI DBI Version 2.00)
    Type B: 16/18 bits, 8/9 bits
    Type C: 4 lines, 9 bits (Option 1), 8 bits (Option 3)
  - MIPI DPI(VSYNC, HSYNC, PCLK, DE, DB[17:0])
  - TE-I/F (MIPI DBI + TE synchronization signal output)
- Window address function to specify a rectangular area in the internal frame memory to write data
- Write data in a rectangular area in the internal frame memory via moving picture display interface Note
  - Reduce data transfer by specifying the area in the frame memory to rewrite data
  - Enable displaying the data in the still picture frame memory area with a moving picture simultaneously
- Abundant color display and drawing functions
  - Programmable γ-correction function for 262,144-color display
  - Partial display function
- Low power consumption architecture (enables to supply power directly to interface I/O)
  - Sleep function
  - Low power consumption 8-color display function
  - Input power supply voltages: IOVCC1, IOVCC2 (power supply for interface I/O)
    VCI (power supply for liquid crystal analog circuit)
- Incorporates a liquid crystal drive power supply circuit
  - Source driver liquid crystal drive/VCOM power supply: DDVDH, VREG, VCL
  - Gate drive power supply: VGH, VGL
  - VCOM drive (VCOM power supply): VCOMH, VCOML
- Liquid crystal power supply startup sequencer
- TFT storage capacitance: Cst only (common VCOM formula)
- 172,800-byte internal frame memory
- Internal 720-channel source driver and 320-channel gate driver
- Single-chip solution for COG module with the arrangement of gate circuits on both sides of the glass substrate
- Internal NVM: User identification code (24 bits). VCOM level adjustment (14 bits). NVM (896 bits) to enable data for automatic load to registers. Write/erase sequencer and write/erase power supply circuit are supported.
- Internal reference voltage

Note: Patent of moving picture display interface is granted.

United States Patent	No. 7,176,870
Japanese Patent	No. 3,826,159
Korean Patent	No.747,636

Power Supply Specifications

Table 1

No.	Item		R61526
1	TFT data lines		720
2	TFT gate lines		320
3	TFT display storage capacitance		Cst only (Common VCOM formula)
4	Liquid crystal drive output	S[1:720]	Grayscale levels V0 ~ V63
		G[1:320]	VGH-VGL
		VCOM	VCOMH=3.0 ~ (DDVDH-0.5)V VCOML=(VCL+0.5) ~ 0V VCOMH-VCOML amplitude = max. 6V Change VCOMH with electronic volume. Change VCOMH-VCOML amplitude with electronic volume
5	Input voltage	IOVCC1 (interface voltage)	1.65V ~ 3.30V Power supply to IM[3:0], RESETX, DB[17:0], RDX, SDA, SDO, WRX/SCL, DCX, CSX, VSYNC, HSYNC, DOTCLK, ENABLE, TE
		IOVCC2 (LED interface voltage)	1.65V ~ 3.30V Power supply to LEDPWM
		VCI (liquid crystal drive power supply voltage)	2.5V ~ 3.3V
6	Liquid crystal drive voltages	DDVDH	5.0V ~ 5.8V
		VGH	10.0V ~ 18.0V
		VGL	-7.1V ~ -14.9V
		VGH-VGL	Max. 28.0V
		VCL	-1.9V ~ -3.3V
		VCI-VCL	Max. 6.6V
7	Internal step-up circuits	DDVDH	VCI x 2
		VGH	VCI + VCI2 x 2, VCI2 x 3
		VGL	-VCI + VCI2 x -1, VCI2 x -2, -VCI + VCI2 x -2
		VCL	VCI x –1

Block Diagram

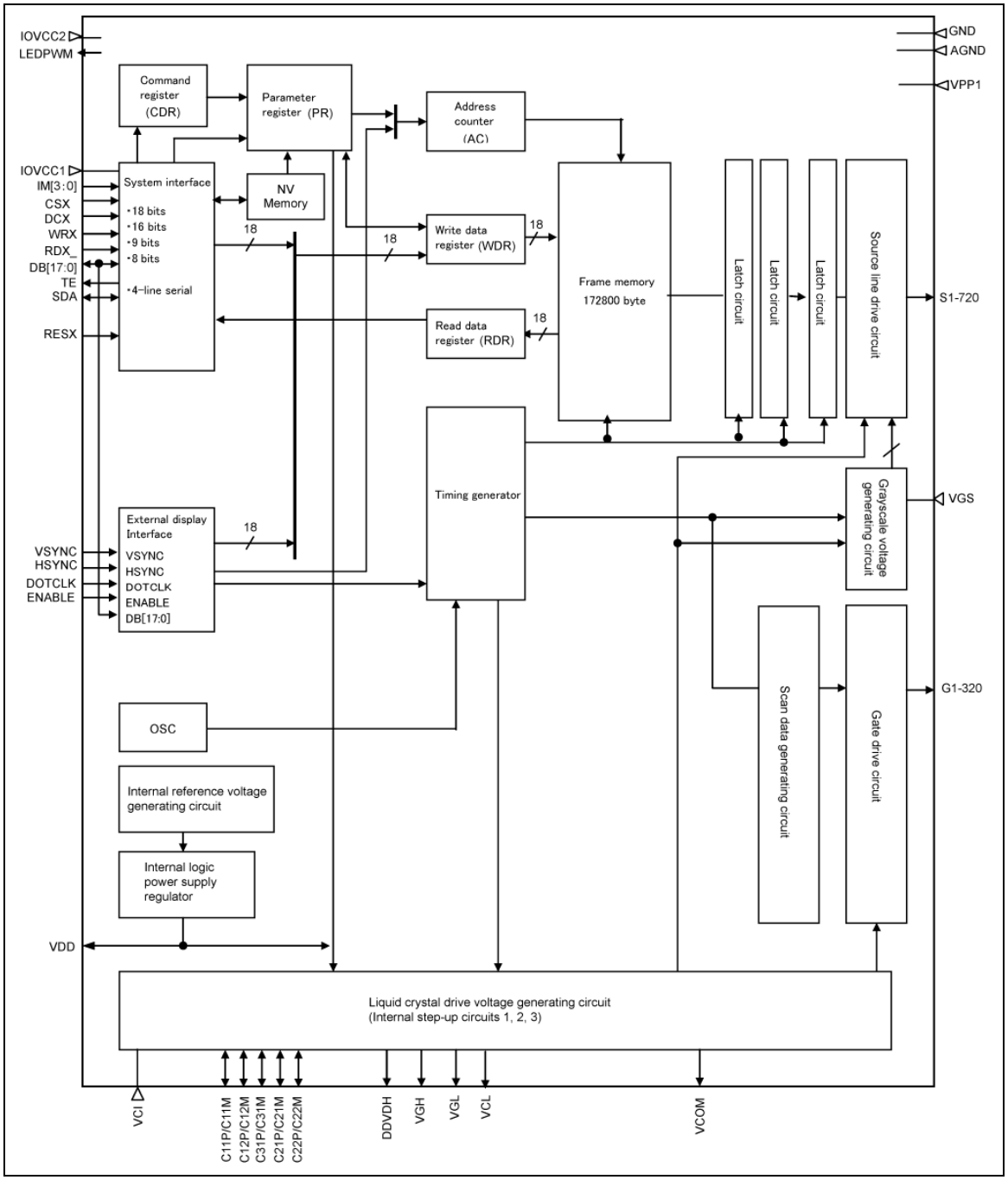


Figure 1

Block Function

1. System Interface

The R61526 supports MIPI DBI TypeB (18/16/9/8 bits) and MIPI DBI TypeC (Option 1, 3). The interface is selected by setting IM[3:0] pins.

Table 2

IM3	IM2	IM1	IM0	Interface	Pin	Colors
0	0	0	0	MIPI DBI Type B 8 bits	DB[7:0]	65,536 / 262,144
0	0	0	1	MIPI DBI Type B 16 bits	DB[15:0]	65,536 / 262,144
0	0	1	0	MIPI DBI Type B 9 bits	DB[8:0]	262,144
0	0	1	1	MIPI DBI Type B 18bits	DB[17:0]	65,536 / 262,144
0	1	0	1	DBI Type C 9 bits (Option 1)	SDA	8 / 262,144
0	1	1	0	DBI Type C 8 bits (Option 3)	SDA	8 / 262,144
1	1	1	1	DBI Type B 8 bits	DB[7:0]	65,536 / 262,144

Set number of colors using set_pixel_format: 3Ah.

Pins IM[3:0] are connected to IOVCC1 via a pull-up resistor. Ground to obtain a “Low” level. The above settings can be realized. The R61526 can support MIPI DBI Type B (8 bits) by setting IM[3:0] pins to 0000 or 1111.

(a) MIPI DBI Type B (18/16/9/8 Bits)

The R61526 supports MIPI DBI TypeB (18/16/9/8 bits). It supports command method with 8-bit command registers and 8-bit parameter registers. The LSI also has an 18-bit write/read register (WDR/RDR). The WDR is used to temporarily store data that is automatically written to the internal frame memory in internal operation of the chip.

The WDR is used to temporarily store the data read out from the frame memory. When reading data from the frame memory, the R61526 first stores the data in the RDR. For this reason, invalid data is sent to the data bus at first and valid data is sent as the R61526 reads second and subsequent data from the frame memory.

Table 3

DCX	RDX	WRX	Operation
0	1	↑	Command
1	↑	1	Read parameter
1	1	↑	Write parameter

(b) MIPI DBI Type C (Option 1, 3)

The R61526 supports 9-bit (Option 1) and 8-bit (Option 3) serial interfaces that use signals CSX, DCX, SCL, SDA, and SDO.

2. External Display Interface (TE-Signal, DPI and VSYNC Interface)

The R61526 supports TE signal, a synchronous signal, DPI and VSYNC interface as external display interface for moving image.

When DBI is selected, display data is written in synchronization with TE, generated by using internal clock output from the R61526, enabling updating image data without flicker on the panel.

When DPI is selected, externally supplied VSYNC, HSYNC, and PCLK signals drive the chip. Display data (DB[17:0]) is written in synchronization with those synchronous signals following data enable signal (DE). This enables updating image data without flicker on the panel.

When VSYNC interface is selected, the entire operation, except for synchronization with synchronous signal VSYNC, is in synchronization with internal clock. System interface is used when display data is written to the frame memory via the system interface DBI.

3. Address Counter (AC)

The address counter (AC) gives an address to the frame memory. Address information defined by CDR and PR is transferred to the AC. The AC is automatically updated plus or minus 1 as the R61526 writes/reads data to/from the frame memory. Display data is written to the frame memory via conventional system interface.

4. Frame Memory

The frame memory is graphics frame memory, which can store bit-pattern data of 172,800 (240RGB x 320 (dots) x 18(bits)) bytes at maximum, using 18 bits per pixel.

5. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltage according to the grayscale setting value in the γ-correction register, enabling display in 262,144 colors.

6. Liquid Crystal Drive Power Supply Circuit

The liquid crystal drive power supply circuit generates VREG, VGH, VGL and VCOM levels to drive liquid crystal.

7. Timing Generator

The timing generator generates a timing signal for the operation of internal circuit such as the internal frame memory. The timing signal for display operation such as frame memory read operation and the timing signal for internal operation such as frame memory access from the host processor are generated separately in order to avoid mutual interference.

8. Oscillator (OSC)

The R61526 incorporates internal oscillator. The frame frequency is adjusted by using a command.

9. Liquid Crystal Driver Circuit

The liquid crystal driver circuit of the R61526 consists of a 720-output source driver (S[1:720]) and a 320-output gate driver (G[1:320]). The display pattern data is latched when 720 bits of data are inputted. The latched data control the source driver and output drive waveforms. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720-bit source output from the source driver can be changed by setting the SS bit (C0h) and the shift direction of gate output from the gate driver can be changed by setting the GS bit (C0h). The scan mode by the gate driver can be changed by setting the SM bit (C0h) enabling to select an optimal scan mode for the module.

10. Internal Logic Power Supply Regulator

The internal logic power supply regulator generates an internal logic power supply.

Pin Function

Table 4 External Power Supply

Signal	I/O	Connect to	Function	Unused pin
IOVCC1	I	Power supply	Power supply to interface pins and the logic.	—
IOVCC2	I	Power supply	Power supply to LEDPWM. This should be connected to Power supply pin.	IOVCC1
GND	I	Power supply	GND for internal logic and interface pin. Set GND=0V.	—
VCI	I	Power supply	Power supply to liquid crystal power supply analog circuit.	—
AGND	I	Power supply	Analog GND (logic regulator, LCD power supply circuit). AGND=0V. Connect to GND on the FPC to prevent noise in case of COG.	—

Note 1: GND and AGND pins are located on several places on the chip. Make sure to connect electrical potential to all of them as “Connection Example” instructs.

Table 5 Bus Interface (Amplitude: IOVCC1-GND)

Signal	I/O	Connect to	Function	Unused pin
CSX	I	Host Processor	System bus select signal. Low: Select (Accessible) High: Not select (Inaccessible) Make sure to connect to host processor. Follow AC timing to control the signal. Chip enable signal in DBI Type C operation (Option 3).	-
DCX	I	Host Processor	Command/data select signal Low: Command High: Data Command/data select signal in DBI Type C operation (Option 3).	-
WRX/SCL	I	Host Processor	Write strobe signal in DBI Type B operation. Data are written when WRX is Low. Synchronous clock signal in DBI Type C operation.	-
RDX	I	Host Processor	Read strobe signal. Data are read when RDX is low.	IOVCC1
SDA	I/O	Host Processor	Serial data input/output pin in DBI Type C operation. Data is input on the rising edge of signal SCL. Data is output on the falling edge of SCL when serial data output pin is selected.	IOVCC1 or GND
SDO	O	Host Processor	This pin is enabled when SDOE=1 and DBI Type C is used. With this setting, SDA can be used as an input pin and SDO pin can be used as an output pin without bidirectional bus to execute serial communication.	OPEN
DB[17:0]	I/O	Host Processor	18-bit bi-directional data bus in DBI Type B operation. 8-bit interface: Use DB[7:0] 9-bit interface: Use DB[8:0] 16-bit interface: Use DB[15:0] 18-bit interface: Use DB[17:0] Abnormal current (through current) is not conducted when CSX is High and the data bus is Hi-z. 18-bit input data bus in DPI operation. 16-bit interface: Use DB[15:0] 18-bit interface: Use DB[17:0] The unused DB pins (DB[17:16]) must be fixed at IOVCC1 or GND level when DPI 16-bit interface is selected.	IOVCC1 or GND or OPEN
ENABLE	I	Host Processor	Data enable signal in DPI operation. Low: Select (Accessible) High: Not select (Inaccessible) Connect to IOVCC1 or GND when DPI is not selected. Connect to host processor and input an IOVCC1/GND signal always when DPI is selected.	IOVCC1 or GND

VSYNC	I	Host Processor	Frame synchronous signal. Low active. Connect to IOVCC1 or GND when DPI is not selected. Connect to host processor and input an IOVCC1/GND signal always when DPI is selected.	IOVCC1 or GND
HSYNC	I	Host Processor	Line synchronous signal. Low active. Connect to IOVCC1 or GND when DPI is not selected. Connect to host processor and input an IOVCC1/GND signal always when DPI is selected.	IOVCC1 or GND
DOTCLK	I	Host Processor	Pixel clock signal. The data input timing is set on the rising edge. Connect to IOVCC1 or GND when DPI is not selected. Connect to host processor and input an IOVCC1/GND signal always when DPI is selected.	IOVCC1 or GND
TE	O	Host Processor	Tearing Effect output signal. It can be used as signal to verify NVM write operation depending on register setting. Leave open when not used.	OPEN
RESX	I	Host Processor or external RC oscillator	Reset pin. The R61526 is initialized when RESX is Low. Make sure to execute power-on reset when turning the power supply on.	-

Table 6 Mode Select Pin (Amplitude: IOVCC1-GND)

Signal	I/O	Connect to	Function	Unused pin
IM[3:0]	I	GND or OPEN	Interface selecting signal. Used to switch DBI Type B (18/16/9/8 bits) and Type C (Option1/Option3). Internally connected to a pull-up resistor. Ground if necessary.	—

Table 7 Internal Power Supply Circuit

Signal	I/O	Connect to	Function	Unused pin
VDD	O	Stabilizing capacitor	Output from internal logic regulator. Connect to stabilizing capacitor.	-
DDVDH	O	Stabilizing capacitor	Source driver liquid crystal and VCOM drive power supply. The output level from the step-up circuit 1 using VCI. The step-up factor is 2. Make sure to connect a stabilizing capacitor.	-
VGH	O	Stabilizing capacitor LCD panel	Liquid crystal drive power supply. The output level form the step-up circuit 2, generated from VCI and VCI2. The output level is determined by the step-up factor, which is set by instruction (BT). Connect a stabilizing capacitor.	-
VGL	O	Stabilizing capacitor LCD panel	Liquid crystal drive power supply. The output level form the step-up circuit 2, generated from VCI and VCI2. The output level is determined by the step-up factor, which is set by instruction (BT). Connect a stabilizing capacitor.	-
VCL	O	Stabilizing capacitor	VCOML drive power supply. Make sure to connect a stabilizing capacitor.	-
C11P, C11M C12P, C12M	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.	-
C21P, C21M, C22P, C22M	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.	-
C31P, C31M	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 3.	

Table 8 LCD Drive Power Supply

Signal	I/O	Connect to	Function	Unused pin
VREG	O	Stabilizing capacitor	Outputs voltage level defined by VRH bit. The level is used as reference level for 1. source driver grayscale, 2. VCOMH level or 3. VCOM amplitude.	-
VCOM	O	TFT panel's common electrode	Power supply to TFT panel's common electrode. VCOM output level alternates between VCOMH and VCOML. The alternating cycle is set by a register. Also, the VCOM output can be started and halted by register setting.	-
VGS	I	GND	Reference level for the grayscale voltage generating circuit.	-
S[1:720]	O	LCD panel	Liquid crystal application voltages.	OPEN
G[1:320]	O	LCD panel	Gate line output signals. VGH: gate line is selected VGL: gate line is not selected	OPEN

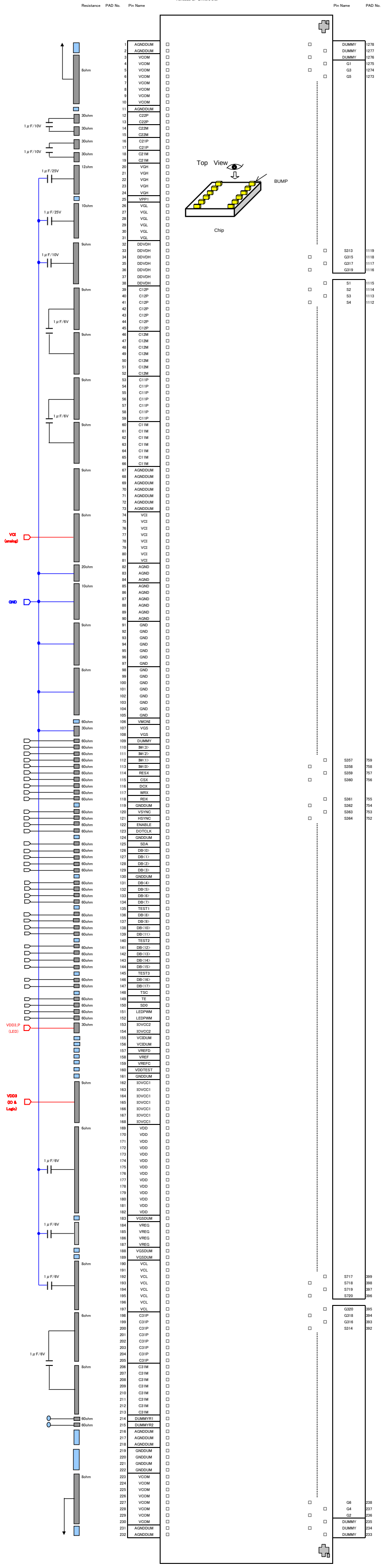
Table 9 Other pins (Test, Dummy)

Signal	I/O	Connect to	Function	Unused pin
VREFC	I	OPEN	Test pin. Leave open or connect to GND.	OPEN or GND
VREFD	O	OPEN	Test pin. Leave open.	OPEN
VREF	O	OPEN	Test pin. Leave open.	OPEN
VDDTEST	I	OPEN	Test pin. Leave open or connect to GND.	OPEN or GND
VMONI	O	OPEN	Test pin. Leave open or connect to GND.	OPEN or GND
AGNDDUM GNDDUM VCIDUM VGSDUM Note	O	-	Used to fix electrical potential by connecting unused I/F and test pins on the glass. Leave open when the dummy pins are not used.	OPEN
DUMMYR[1:2]	O	OPEN	Dummy pins to measure contact resistance. Short-circuited to AGND in the R61526. Leave all power supplies including GND open to measure contact resistance.	OPEN
TEST1	I	OPEN	Test pin. Leave open or connect to GND.	OPEN or GND
TEST2	I	OPEN	Test pin. Leave open or connect to GND.	OPEN or GND
TEST3	I	OPEN	Test pin. Leave open or connect to GND.	OPEN or GND
TSC	I	OPEN	Test pin. Leave open or connect to GND.	OPEN or GND
VPP1	I	-	Test pin. Leave open or connect to GND=0V. Do not draw ITO line when leaving VPP1 open.	OPEN or GND
DUMMY	O	-	Dummy pins to support the LSI when mounted onto a glass substrate.	OPEN
LEDPWM	O	OPEN	Test pin. Leave open.	OPEN

PATENT ISSUED: Japanese Patent No. 3,980,066
Korean Patent No. 401,270
Taiwanese Patent No. 175,413
United States Patent No. 6,323,930, No. 6,924,868

R61526 Wiring Example

Rev 0.1 '09/7/31
Rev 0.2 '09/7/31 Number miss correction
Rev 0.3 '09/9/7 Output PADs Added
Rev 0.4 '09/10/27 VMONI GND→OPEN, add VREG 1uF
Renesas SP Drivers Inc.



●Chip size: 15.26mm x 0.65mm

●Chip thickness: 280μm (typ)

●Pad coordinate: Pad center

●Pad origin: Chip center

●Au bump size:

1. 40μm x 56μm (I/O side, No.1-232)
2. 14μm x 104μm (Output to LCD, No 233-1278)

●Au bump pitch: See BUMP Arrangement.

●Au bump height: 12μm

●Alignment Mark

Alignment mark shape	X	Y
(1-a)	-7480	225
(1-b)	7480	225

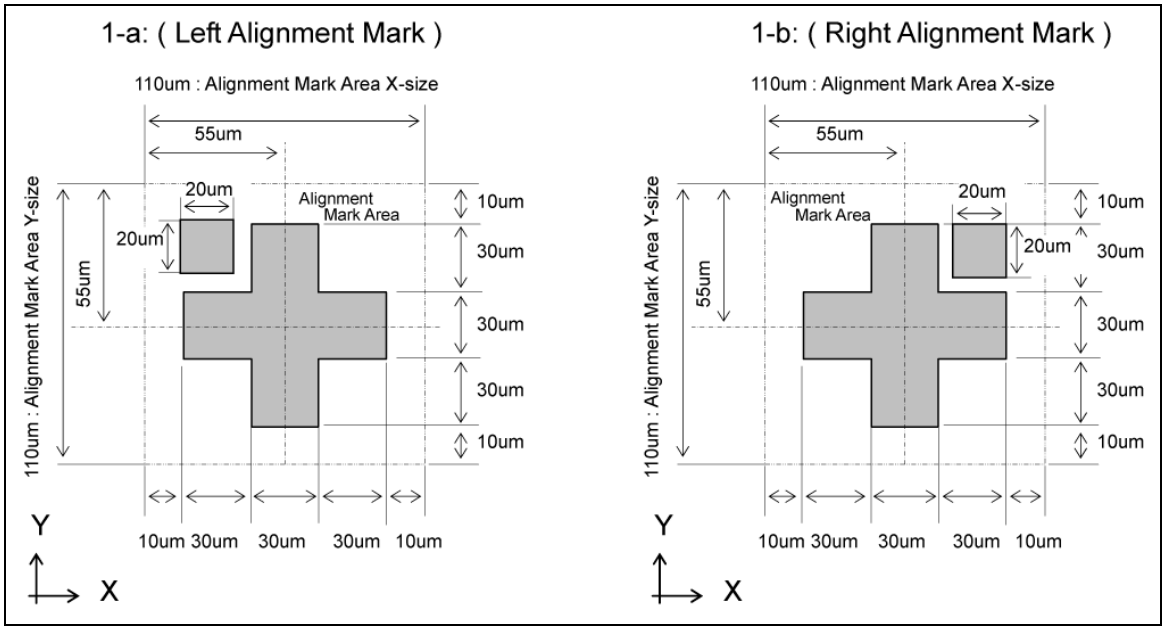


Figure 2

R61526 Pad Coordinates (No.1) (Unit: um) 2009.9.14 rev1.0a

pad No	pad name	X	ΔX	Y	ΔY
1	AGNDDUM	−7292.5	−60.0	−250.0	0.0
2	AGNDDUM	−7232.5	−60.0	−250.0	0.0
3	VCOM	−7172.5	−60.0	−250.0	0.0
4	VCOM	−7112.5	−60.0	−250.0	0.0
5	VCOM	−7052.5	−60.0	−250.0	0.0
6	VCOM	−6992.5	−60.0	−250.0	0.0
7	VCOM	−6932.5	−60.0	−250.0	0.0
8	VCOM	−6872.5	−60.0	−250.0	0.0
9	VCOM	−6812.5	−60.0	−250.0	0.0
10	VCOM	−6752.5	−60.0	−250.0	0.0
11	AGNDDUM	−6692.5	−60.0	−250.0	0.0
12	C22P	−6632.5	−60.0	−250.0	0.0
13	C22P	−6572.5	−60.0	−250.0	0.0
14	C22M	−6512.5	−60.0	−250.0	0.0
15	C22M	−6452.5	−60.0	−250.0	0.0
16	C21P	−6392.5	−60.0	−250.0	0.0
17	C21P	−6332.5	−60.0	−250.0	0.0
18	C21M	−6272.5	−60.0	−250.0	0.0
19	C21M	−6212.5	−60.0	−250.0	0.0
20	VGH	−6152.5	−60.0	−250.0	0.0
21	VGH	−6092.5	−60.0	−250.0	0.0
22	VGH	−6032.5	−60.0	−250.0	0.0
23	VGH	−5972.5	−60.0	−250.0	0.0
24	VGH	−5912.5	−60.0	−250.0	0.0
25	VPP1	−5852.5	−60.0	−250.0	0.0
26	VGL	−5792.5	−60.0	−250.0	0.0
27	VGL	−5732.5	−60.0	−250.0	0.0
28	VGL	−5672.5	−60.0	−250.0	0.0
29	VGL	−5612.5	−60.0	−250.0	0.0
30	VGL	−5552.5	−60.0	−250.0	0.0
31	VGL	−5492.5	−60.0	−250.0	0.0
32	DDVDH	−5432.5	−60.0	−250.0	0.0
33	DDVDH	−5372.5	−60.0	−250.0	0.0
34	DDVDH	−5312.5	−60.0	−250.0	0.0
35	DDVDH	−5252.5	−60.0	−250.0	0.0
36	DDVDH	−5192.5	−60.0	−250.0	0.0
37	DDVDH	−5132.5	−60.0	−250.0	0.0
38	DDVDH	−5072.5	−60.0	−250.0	0.0
39	C12P	−5012.5	−60.0	−250.0	0.0
40	C12P	−4952.5	−60.0	−250.0	0.0
41	C12P	−4892.5	−60.0	−250.0	0.0
42	C12P	−4832.5	−60.0	−250.0	0.0
43	C12P	−4772.5	−60.0	−250.0	0.0
44	C12P	−4712.5	−60.0	−250.0	0.0
45	C12P	−4652.5	−60.0	−250.0	0.0
46	C12M	−4592.5	−60.0	−250.0	0.0
47	C12M	−4532.5	−60.0	−250.0	0.0
48	C12M	−4472.5	−60.0	−250.0	0.0
49	C12M	−4412.5	−60.0	−250.0	0.0
50	C12M	−4352.5	−60.0	−250.0	0.0
51	C12M	−4292.5	−60.0	−250.0	0.0
52	C12M	−4232.5	−60.0	−250.0	0.0
53	C11P	−4172.5	−60.0	−250.0	0.0
54	C11P	−4112.5	−60.0	−250.0	0.0
55	C11P	−4052.5	−60.0	−250.0	0.0
56	C11P	−3992.5	−60.0	−250.0	0.0
57	C11P	−3932.5	−60.0	−250.0	0.0
58	C11P	−3872.5	−60.0	−250.0	0.0
59	C11P	−3812.5	−60.0	−250.0	0.0
60	C11M	−3752.5	−60.0	−250.0	0.0
61	C11M	−3692.5	−60.0	−250.0	0.0
62	C11M	−3632.5	−60.0	−250.0	0.0
63	C11M	−3572.5	−60.0	−250.0	0.0
64	C11M	−3512.5	−60.0	−250.0	0.0
65	C11M	−3452.5	−60.0	−250.0	0.0
66	C11M	−3392.5	−60.0	−250.0	0.0
67	AGNDDUM	−3332.5	−60.0	−250.0	0.0
68	AGNDDUM	−3272.5	−60.0	−250.0	0.0
69	AGNDDUM	−3212.5	−60.0	−250.0	0.0
70	AGNDDUM	−3152.5	−60.0	−250.0	0.0
71	AGNDDUM	−3092.5	−60.0	−250.0	0.0
72	AGNDDUM	−3032.5	−60.0	−250.0	0.0
73	AGNDDUM	−2972.5	−60.0	−250.0	0.0
74	VCI	−2912.5	−60.0	−250.0	0.0
75	VCI	−2852.5	−60.0	−250.0	0.0
76	VCI	−2792.5	−60.0	−250.0	0.0
77	VCI	−2732.5	−60.0	−250.0	0.0
78	VCI	−2672.5	−60.0	−250.0	0.0
79	VCI	−2612.5	−60.0	−250.0	0.0
80	VCI	−2552.5	−60.0	−250.0	0.0
81	VCI	−2492.5	−60.0	−250.0	0.0
82	AGND	−2432.5	−60.0	−250.0	0.0
83	AGND	−2372.5	−60.0	−250.0	0.0
84	AGND	−2312.5	−60.0	−250.0	0.0
85	AGND	−2252.5	−60.0	−250.0	0.0
86	AGND	−2192.5	−60.0	−250.0	0.0
87	AGND	−2132.5	−60.0	−250.0	0.0
88	AGND	−2072.5	−60.0	−250.0	0.0
89	AGND	−2012.5	−60.0	−250.0	0.0
90	AGND	−1952.5	−60.0	−250.0	0.0
91	GND	−1892.5	−60.0	−250.0	0.0
92	GND	−1832.5	−60.0	−250.0	0.0
93	GND	−1772.5	−60.0	−250.0	0.0
94	GND	−1712.5	−60.0	−250.0	0.0
95	GND	−1652.5	−60.0	−250.0	0.0
96	GND	−1592.5	−60.0	−250.0	0.0
97	GND	−1532.5	−60.0	−250.0	0.0
98	GND	−1472.5	−60.0	−250.0	0.0
99	GND	−1412.5	−60.0	−250.0	0.0
100	GND	−1352.5	−60.0	−250.0	0.0

R61526 Pad Coordinates (No.2) (Unit: um)

pad No	pad name	X	ΔX	Y	ΔY
101	GND	-1292.5	-60.0	-250.0	0.0
102	GND	-1232.5	-60.0	-250.0	0.0
103	GND	-1172.5	-60.0	-250.0	0.0
104	GND	-1112.5	-60.0	-250.0	0.0
105	GND	-1052.5	-60.0	-250.0	0.0
106	VMONI	-992.5	-60.0	-250.0	0.0
107	VGS	-932.5	-60.0	-250.0	0.0
108	VGS	-872.5	-60.0	-250.0	0.0
109	DUMMY	-812.5	-60.0	-250.0	0.0
110	IM<3>	-752.5	-60.0	-250.0	0.0
111	IM<2>	-692.5	-60.0	-250.0	0.0
112	IM<1>	-632.5	-60.0	-250.0	0.0
113	IM<0>	-572.5	-60.0	-250.0	0.0
114	RESX	-512.5	-60.0	-250.0	0.0
115	CSX	-452.5	-60.0	-250.0	0.0
116	DCX	-392.5	-60.0	-250.0	0.0
117	WRX	-332.5	-60.0	-250.0	0.0
118	RDX	-272.5	-60.0	-250.0	0.0
119	GNDDUM	-212.5	-60.0	-250.0	0.0
120	VSYNC	-152.5	-60.0	-250.0	0.0
121	HSYNC	-92.5	-60.0	-250.0	0.0
122	ENABLE	-32.5	-60.0	-250.0	0.0
123	DOTCLK	27.5	-60.0	-250.0	0.0
124	GNDDUM	87.5	-72.5	-250.0	0.0
125	SDA	160.0	-85.0	-250.0	0.0
126	DB<0>	245.0	-85.0	-250.0	0.0
127	DB<1>	330.0	-85.0	-250.0	0.0
128	DB<2>	415.0	-85.0	-250.0	0.0
129	DB<3>	500.0	-72.5	-250.0	0.0
130	GNDDUM	572.5	-72.5	-250.0	0.0
131	DB<4>	645.0	-85.0	-250.0	0.0
132	DB<5>	730.0	-85.0	-250.0	0.0
133	DB<6>	815.0	-85.0	-250.0	0.0
134	DB<7>	900.0	-72.5	-250.0	0.0
135	TEST1	972.5	-72.5	-250.0	0.0
136	DB<8>	1045.0	-85.0	-250.0	0.0
137	DB<9>	1130.0	-85.0	-250.0	0.0
138	DB<10>	1215.0	-85.0	-250.0	0.0
139	DB<11>	1300.0	-72.5	-250.0	0.0
140	TEST2	1372.5	-72.5	-250.0	0.0
141	DB<12>	1445.0	-85.0	-250.0	0.0
142	DB<13>	1530.0	-85.0	-250.0	0.0
143	DB<14>	1615.0	-85.0	-250.0	0.0
144	DB<15>	1700.0	-72.5	-250.0	0.0
145	TEST3	1772.5	-72.5	-250.0	0.0
146	DB<16>	1845.0	-85.0	-250.0	0.0
147	DB<17>	1930.0	-72.5	-250.0	0.0
148	TSC	2002.5	-72.5	-250.0	0.0
149	TE	2075.0	-85.0	-250.0	0.0
150	SD0	2160.0	-85.0	-250.0	0.0
151	LEDPWM	2245.0	-85.0	-250.0	0.0
152	LEDPWM	2330.0	-72.5	-250.0	0.0
153	IOVCC2	2402.5	-60.0	-250.0	0.0
154	IOVCC2	2462.5	-72.5	-250.0	0.0
155	VCIDUM	2535.0	-85.0	-250.0	0.0
156	VCIDUM	2620.0	-85.0	-250.0	0.0
157	VREFD	2705.0	-85.0	-250.0	0.0
158	VREF	2790.0	-85.0	-250.0	0.0
159	VREFC	2875.0	-85.0	-250.0	0.0
160	VDDTEST	2960.0	-72.5	-250.0	0.0
161	GNDDUM	3032.5	-60.0	-250.0	0.0
162	IOVCC1	3092.5	-60.0	-250.0	0.0
163	IOVCC1	3152.5	-60.0	-250.0	0.0
164	IOVCC1	3212.5	-60.0	-250.0	0.0
165	IOVCC1	3272.5	-60.0	-250.0	0.0
166	IOVCC1	3332.5	-60.0	-250.0	0.0
167	IOVCC1	3392.5	-60.0	-250.0	0.0
168	IOVCC1	3452.5	-60.0	-250.0	0.0
169	VDD	3512.5	-60.0	-250.0	0.0
170	VDD	3572.5	-60.0	-250.0	0.0
171	VDD	3632.5	-60.0	-250.0	0.0
172	VDD	3692.5	-60.0	-250.0	0.0
173	VDD	3752.5	-60.0	-250.0	0.0
174	VDD	3812.5	-60.0	-250.0	0.0
175	VDD	3872.5	-60.0	-250.0	0.0
176	VDD	3932.5	-60.0	-250.0	0.0
177	VDD	3992.5	-60.0	-250.0	0.0
178	VDD	4052.5	-60.0	-250.0	0.0
179	VDD	4112.5	-60.0	-250.0	0.0
180	VDD	4172.5	-60.0	-250.0	0.0
181	VDD	4232.5	-60.0	-250.0	0.0
182	VDD	4292.5	-60.0	-250.0	0.0
183	VGSDUM	4352.5	-60.0	-250.0	0.0
184	VREG	4412.5	-60.0	-250.0	0.0
185	VREG	4472.5	-60.0	-250.0	0.0
186	VREG	4532.5	-60.0	-250.0	0.0
187	VREG	4592.5	-60.0	-250.0	0.0
188	VGSDUM	4652.5	-60.0	-250.0	0.0
189	VGSDUM	4712.5	-60.0	-250.0	0.0
190	VCL	4772.5	-60.0	-250.0	0.0
191	VCL	4832.5	-60.0	-250.0	0.0
192	VCL	4892.5	-60.0	-250.0	0.0
193	VCL	4952.5	-60.0	-250.0	0.0
194	VCL	5012.5	-60.0	-250.0	0.0
195	VCL	5072.5	-60.0	-250.0	0.0
196	VCL	5132.5	-60.0	-250.0	0.0
197	VCL	5192.5	-60.0	-250.0	0.0
198	C31P	5252.5	-60.0	-250.0	0.0
199	C31P	5312.5	-60.0	-250.0	0.0
200	C31P	5372.5	-60.0	-250.0	0.0

R61526 Pad Coordinates (No.3) (Unit: um)

pad No	pad name	X	ΔX	Y	ΔY
201	C31P	5432.5	−60.0	−250.0	0.0
202	C31P	5492.5	−60.0	−250.0	0.0
203	C31P	5552.5	−60.0	−250.0	0.0
204	C31P	5612.5	−60.0	−250.0	0.0
205	C31P	5672.5	−60.0	−250.0	0.0
206	C31M	5732.5	−60.0	−250.0	0.0
207	C31M	5792.5	−60.0	−250.0	0.0
208	C31M	5852.5	−60.0	−250.0	0.0
209	C31M	5912.5	−60.0	−250.0	0.0
210	C31M	5972.5	−60.0	−250.0	0.0
211	C31M	6032.5	−60.0	−250.0	0.0
212	C31M	6092.5	−60.0	−250.0	0.0
213	C31M	6152.5	−60.0	−250.0	0.0
214	DUMMYR1	6212.5	−60.0	−250.0	0.0
215	DUMMYR2	6272.5	−60.0	−250.0	0.0
216	AGNDDUM	6332.5	−60.0	−250.0	0.0
217	AGNDDUM	6392.5	−60.0	−250.0	0.0
218	AGNDDUM	6452.5	−60.0	−250.0	0.0
219	GNDDUM	6512.5	−60.0	−250.0	0.0
220	GNDDUM	6572.5	−60.0	−250.0	0.0
221	GNDDUM	6632.5	−60.0	−250.0	0.0
222	GNDDUM	6692.5	−60.0	−250.0	0.0
223	VCOM	6752.5	−60.0	−250.0	0.0
224	VCOM	6812.5	−60.0	−250.0	0.0
225	VCOM	6872.5	−60.0	−250.0	0.0
226	VCOM	6932.5	−60.0	−250.0	0.0
227	VCOM	6992.5	−60.0	−250.0	0.0
228	VCOM	7052.5	−60.0	−250.0	0.0
229	VCOM	7112.5	−60.0	−250.0	0.0
230	VCOM	7172.5	−60.0	−250.0	0.0
231	AGNDDUM	7232.5	−60.0	−250.0	0.0
232	AGNDDUM	7292.5	−	−250.0	−
233	DUMMY	7399.0	14.0	226.0	135.0
234	DUMMY	7385.0	14.0	91.0	−135.0
235	DUMMY	7371.0	14.0	226.0	135.0
236	G2	7357.0	14.0	91.0	−135.0
237	G4	7343.0	14.0	226.0	135.0
238	G6	7329.0	14.0	91.0	−135.0
239	G8	7315.0	14.0	226.0	135.0
240	G10	7301.0	14.0	91.0	−135.0
241	G12	7287.0	14.0	226.0	135.0
242	G14	7273.0	14.0	91.0	−135.0
243	G16	7259.0	14.0	226.0	135.0
244	G18	7245.0	14.0	91.0	−135.0
245	G20	7231.0	14.0	226.0	135.0
246	G22	7217.0	14.0	91.0	−135.0
247	G24	7203.0	14.0	226.0	135.0
248	G26	7189.0	14.0	91.0	−135.0
249	G28	7175.0	14.0	226.0	135.0
250	G30	7161.0	14.0	91.0	−135.0

pad No	pad name	X	ΔX	Y	ΔY
251	G32	7147.0	14.0	226.0	135.0
252	G34	7133.0	14.0	91.0	−135.0
253	G36	7119.0	14.0	226.0	135.0
254	G38	7105.0	14.0	91.0	−135.0
255	G40	7091.0	14.0	226.0	135.0
256	G42	7077.0	14.0	91.0	−135.0
257	G44	7063.0	14.0	226.0	135.0
258	G46	7049.0	14.0	91.0	−135.0
259	G48	7035.0	14.0	226.0	135.0
260	G50	7021.0	14.0	91.0	−135.0
261	G52	7007.0	14.0	226.0	135.0
262	G54	6993.0	14.0	91.0	−135.0
263	G56	6979.0	14.0	226.0	135.0
264	G58	6965.0	14.0	91.0	−135.0
265	G60	6951.0	14.0	226.0	135.0
266	G62	6937.0	14.0	91.0	−135.0
267	G64	6923.0	14.0	226.0	135.0
268	G66	6909.0	14.0	91.0	−135.0
269	G68	6895.0	14.0	226.0	135.0
270	G70	6881.0	14.0	91.0	−135.0
271	G72	6867.0	14.0	226.0	135.0
272	G74	6853.0	14.0	91.0	−135.0
273	G76	6839.0	14.0	226.0	135.0
274	G78	6825.0	14.0	91.0	−135.0
275	G80	6811.0	14.0	226.0	135.0
276	G82	6797.0	14.0	91.0	−135.0
277	G84	6783.0	14.0	226.0	135.0
278	G86	6769.0	14.0	91.0	−135.0
279	G88	6755.0	14.0	226.0	135.0
280	G90	6741.0	14.0	91.0	−135.0
281	G92	6727.0	14.0	226.0	135.0
282	G94	6713.0	14.0	91.0	−135.0
283	G96	6699.0	14.0	226.0	135.0
284	G98	6685.0	14.0	91.0	−135.0
285	G100	6671.0	14.0	226.0	135.0
286	G102	6657.0	14.0	91.0	−135.0
287	G104	6643.0	14.0	226.0	135.0
288	G106	6629.0	14.0	91.0	−135.0
289	G108	6615.0	14.0	226.0	135.0
290	G110	6601.0	14.0	91.0	−135.0
291	G112	6587.0	14.0	226.0	135.0
292	G114	6573.0	14.0	91.0	−135.0
293	G116	6559.0	14.0	226.0	135.0
294	G118	6545.0	14.0	91.0	−135.0
295	G120	6531.0	14.0	226.0	135.0
296	G122	6517.0	14.0	91.0	−135.0
297	G124	6503.0	14.0	226.0	135.0
298	G126	6489.0	14.0	91.0	−135.0
299	G128	6475.0	14.0	226.0	135.0
300	G130	6461.0	14.0	91.0	−135.0

R61526 Pad Coordinates (No.4) (Unit: um)

pad No	pad name	X	ΔX	Y	ΔY
301	G132	6447.0	14.0	226.0	135.0
302	G134	6433.0	14.0	91.0	−135.0
303	G136	6419.0	14.0	226.0	135.0
304	G138	6405.0	14.0	91.0	−135.0
305	G140	6391.0	14.0	226.0	135.0
306	G142	6377.0	14.0	91.0	−135.0
307	G144	6363.0	14.0	226.0	135.0
308	G146	6349.0	14.0	91.0	−135.0
309	G148	6335.0	14.0	226.0	135.0
310	G150	6321.0	14.0	91.0	−135.0
311	G152	6307.0	14.0	226.0	135.0
312	G154	6293.0	14.0	91.0	−135.0
313	G156	6279.0	14.0	226.0	135.0
314	G158	6265.0	14.0	91.0	−135.0
315	G160	6251.0	14.0	226.0	135.0
316	G162	6237.0	14.0	91.0	−135.0
317	G164	6223.0	14.0	226.0	135.0
318	G166	6209.0	14.0	91.0	−135.0
319	G168	6195.0	14.0	226.0	135.0
320	G170	6181.0	14.0	91.0	−135.0
321	G172	6167.0	14.0	226.0	135.0
322	G174	6153.0	14.0	91.0	−135.0
323	G176	6139.0	14.0	226.0	135.0
324	G178	6125.0	14.0	91.0	−135.0
325	G180	6111.0	14.0	226.0	135.0
326	G182	6097.0	14.0	91.0	−135.0
327	G184	6083.0	14.0	226.0	135.0
328	G186	6069.0	14.0	91.0	−135.0
329	G188	6055.0	14.0	226.0	135.0
330	G190	6041.0	14.0	91.0	−135.0
331	G192	6027.0	14.0	226.0	135.0
332	G194	6013.0	14.0	91.0	−135.0
333	G196	5999.0	14.0	226.0	135.0
334	G198	5985.0	14.0	91.0	−135.0
335	G200	5971.0	14.0	226.0	135.0
336	G202	5957.0	14.0	91.0	−135.0
337	G204	5943.0	14.0	226.0	135.0
338	G206	5929.0	14.0	91.0	−135.0
339	G208	5915.0	14.0	226.0	135.0
340	G210	5901.0	14.0	91.0	−135.0
341	G212	5887.0	14.0	226.0	135.0
342	G214	5873.0	14.0	91.0	−135.0
343	G216	5859.0	14.0	226.0	135.0
344	G218	5845.0	14.0	91.0	−135.0
345	G220	5831.0	14.0	226.0	135.0
346	G222	5817.0	14.0	91.0	−135.0
347	G224	5803.0	14.0	226.0	135.0
348	G226	5789.0	14.0	91.0	−135.0
349	G228	5775.0	14.0	226.0	135.0
350	G230	5761.0	14.0	91.0	−135.0

pad No	pad name	X	ΔX	Y	ΔY
351	G232	5747.0	14.0	226.0	135.0
352	G234	5733.0	14.0	91.0	−135.0
353	G236	5719.0	14.0	226.0	135.0
354	G238	5705.0	14.0	91.0	−135.0
355	G240	5691.0	14.0	226.0	135.0
356	G242	5677.0	14.0	91.0	−135.0
357	G244	5663.0	14.0	226.0	135.0
358	G246	5649.0	14.0	91.0	−135.0
359	G248	5635.0	14.0	226.0	135.0
360	G250	5621.0	14.0	91.0	−135.0
361	G252	5607.0	14.0	226.0	135.0
362	G254	5593.0	14.0	91.0	−135.0
363	G256	5579.0	14.0	226.0	135.0
364	G258	5565.0	14.0	91.0	−135.0
365	G260	5551.0	14.0	226.0	135.0
366	G262	5537.0	14.0	91.0	−135.0
367	G264	5523.0	14.0	226.0	135.0
368	G266	5509.0	14.0	91.0	−135.0
369	G268	5495.0	14.0	226.0	135.0
370	G270	5481.0	14.0	91.0	−135.0
371	G272	5467.0	14.0	226.0	135.0
372	G274	5453.0	14.0	91.0	−135.0
373	G276	5439.0	14.0	226.0	135.0
374	G278	5425.0	14.0	91.0	−135.0
375	G280	5411.0	14.0	226.0	135.0
376	G282	5397.0	14.0	91.0	−135.0
377	G284	5383.0	14.0	226.0	135.0
378	G286	5369.0	14.0	91.0	−135.0
379	G288	5355.0	14.0	226.0	135.0
380	G290	5341.0	14.0	91.0	−135.0
381	G292	5327.0	14.0	226.0	135.0
382	G294	5313.0	14.0	91.0	−135.0
383	G296	5299.0	14.0	226.0	135.0
384	G298	5285.0	14.0	91.0	−135.0
385	G300	5271.0	14.0	226.0	135.0
386	G302	5257.0	14.0	91.0	−135.0
387	G304	5243.0	14.0	226.0	135.0
388	G306	5229.0	14.0	91.0	−135.0
389	G308	5215.0	14.0	226.0	135.0
390	G310	5201.0	14.0	91.0	−135.0
391	G312	5187.0	14.0	226.0	135.0
392	G314	5173.0	14.0	91.0	−135.0
393	G316	5159.0	14.0	226.0	135.0
394	G318	5145.0	14.0	91.0	−135.0
395	G320	5131.0	56.0	226.0	135.0
396	S720	5075.0	14.0	91.0	−135.0
397	S719	5061.0	14.0	226.0	135.0
398	S718	5047.0	14.0	91.0	−135.0
399	S717	5033.0	14.0	226.0	135.0
400	S716	5019.0	14.0	91.0	−135.0

R61526 Pad Coordinates (No.5) (Unit: um)

pad No	pad name	X	ΔX	Y	ΔY
401	S715	5005.0	14.0	226.0	135.0
402	S714	4991.0	14.0	91.0	−135.0
403	S713	4977.0	14.0	226.0	135.0
404	S712	4963.0	14.0	91.0	−135.0
405	S711	4949.0	14.0	226.0	135.0
406	S710	4935.0	14.0	91.0	−135.0
407	S709	4921.0	14.0	226.0	135.0
408	S708	4907.0	14.0	91.0	−135.0
409	S707	4893.0	14.0	226.0	135.0
410	S706	4879.0	14.0	91.0	−135.0
411	S705	4865.0	14.0	226.0	135.0
412	S704	4851.0	14.0	91.0	−135.0
413	S703	4837.0	14.0	226.0	135.0
414	S702	4823.0	14.0	91.0	−135.0
415	S701	4809.0	14.0	226.0	135.0
416	S700	4795.0	14.0	91.0	−135.0
417	S699	4781.0	14.0	226.0	135.0
418	S698	4767.0	14.0	91.0	−135.0
419	S697	4753.0	14.0	226.0	135.0
420	S696	4739.0	14.0	91.0	−135.0
421	S695	4725.0	14.0	226.0	135.0
422	S694	4711.0	14.0	91.0	−135.0
423	S693	4697.0	14.0	226.0	135.0
424	S692	4683.0	14.0	91.0	−135.0
425	S691	4669.0	14.0	226.0	135.0
426	S690	4655.0	14.0	91.0	−135.0
427	S689	4641.0	14.0	226.0	135.0
428	S688	4627.0	14.0	91.0	−135.0
429	S687	4613.0	14.0	226.0	135.0
430	S686	4599.0	14.0	91.0	−135.0
431	S685	4585.0	14.0	226.0	135.0
432	S684	4571.0	14.0	91.0	−135.0
433	S683	4557.0	14.0	226.0	135.0
434	S682	4543.0	14.0	91.0	−135.0
435	S681	4529.0	14.0	226.0	135.0
436	S680	4515.0	14.0	91.0	−135.0
437	S679	4501.0	14.0	226.0	135.0
438	S678	4487.0	14.0	91.0	−135.0
439	S677	4473.0	14.0	226.0	135.0
440	S676	4459.0	14.0	91.0	−135.0
441	S675	4445.0	14.0	226.0	135.0
442	S674	4431.0	14.0	91.0	−135.0
443	S673	4417.0	14.0	226.0	135.0
444	S672	4403.0	14.0	91.0	−135.0
445	S671	4389.0	14.0	226.0	135.0
446	S670	4375.0	14.0	91.0	−135.0
447	S669	4361.0	14.0	226.0	135.0
448	S668	4347.0	14.0	91.0	−135.0
449	S667	4333.0	14.0	226.0	135.0
450	S666	4319.0	14.0	91.0	−135.0

pad No	pad name	X	ΔX	Y	ΔY
451	S665	4305.0	14.0	226.0	135.0
452	S664	4291.0	14.0	91.0	−135.0
453	S663	4277.0	14.0	226.0	135.0
454	S662	4263.0	14.0	91.0	−135.0
455	S661	4249.0	14.0	226.0	135.0
456	S660	4235.0	14.0	91.0	−135.0
457	S659	4221.0	14.0	226.0	135.0
458	S658	4207.0	14.0	91.0	−135.0
459	S657	4193.0	14.0	226.0	135.0
460	S656	4179.0	14.0	91.0	−135.0
461	S655	4165.0	14.0	226.0	135.0
462	S654	4151.0	14.0	91.0	−135.0
463	S653	4137.0	14.0	226.0	135.0
464	S652	4123.0	14.0	91.0	−135.0
465	S651	4109.0	14.0	226.0	135.0
466	S650	4095.0	14.0	91.0	−135.0
467	S649	4081.0	14.0	226.0	135.0
468	S648	4067.0	14.0	91.0	−135.0
469	S647	4053.0	14.0	226.0	135.0
470	S646	4039.0	14.0	91.0	−135.0
471	S645	4025.0	14.0	226.0	135.0
472	S644	4011.0	14.0	91.0	−135.0
473	S643	3997.0	14.0	226.0	135.0
474	S642	3983.0	14.0	91.0	−135.0
475	S641	3969.0	14.0	226.0	135.0
476	S640	3955.0	14.0	91.0	−135.0
477	S639	3941.0	14.0	226.0	135.0
478	S638	3927.0	14.0	91.0	−135.0
479	S637	3913.0	14.0	226.0	135.0
480	S636	3899.0	14.0	91.0	−135.0
481	S635	3885.0	14.0	226.0	135.0
482	S634	3871.0	14.0	91.0	−135.0
483	S633	3857.0	14.0	226.0	135.0
484	S632	3843.0	14.0	91.0	−135.0
485	S631	3829.0	14.0	226.0	135.0
486	S630	3815.0	14.0	91.0	−135.0
487	S629	3801.0	14.0	226.0	135.0
488	S628	3787.0	14.0	91.0	−135.0
489	S627	3773.0	14.0	226.0	135.0
490	S626	3759.0	14.0	91.0	−135.0
491	S625	3745.0	14.0	226.0	135.0
492	S624	3731.0	14.0	91.0	−135.0
493	S623	3717.0	14.0	226.0	135.0
494	S622	3703.0	14.0	91.0	−135.0
495	S621	3689.0	14.0	226.0	135.0
496	S620	3675.0	14.0	91.0	−135.0
497	S619	3661.0	14.0	226.0	135.0
498	S618	3647.0	14.0	91.0	−135.0
499	S617	3633.0	14.0	226.0	135.0
500	S616	3619.0	14.0	91.0	−135.0

R61526 Pad Coordinates (No.6) (Unit: um)

pad No	pad name	X	ΔX	Y	ΔY
501	S615	3605.0	14.0	226.0	135.0
502	S614	3591.0	14.0	91.0	−135.0
503	S613	3577.0	14.0	226.0	135.0
504	S612	3563.0	14.0	91.0	−135.0
505	S611	3549.0	14.0	226.0	135.0
506	S610	3535.0	14.0	91.0	−135.0
507	S609	3521.0	14.0	226.0	135.0
508	S608	3507.0	14.0	91.0	−135.0
509	S607	3493.0	14.0	226.0	135.0
510	S606	3479.0	14.0	91.0	−135.0
511	S605	3465.0	14.0	226.0	135.0
512	S604	3451.0	14.0	91.0	−135.0
513	S603	3437.0	14.0	226.0	135.0
514	S602	3423.0	14.0	91.0	−135.0
515	S601	3409.0	14.0	226.0	135.0
516	S600	3395.0	14.0	91.0	−135.0
517	S599	3381.0	14.0	226.0	135.0
518	S598	3367.0	14.0	91.0	−135.0
519	S597	3353.0	14.0	226.0	135.0
520	S596	3339.0	14.0	91.0	−135.0
521	S595	3325.0	14.0	226.0	135.0
522	S594	3311.0	14.0	91.0	−135.0
523	S593	3297.0	14.0	226.0	135.0
524	S592	3283.0	14.0	91.0	−135.0
525	S591	3269.0	14.0	226.0	135.0
526	S590	3255.0	14.0	91.0	−135.0
527	S589	3241.0	14.0	226.0	135.0
528	S588	3227.0	14.0	91.0	−135.0
529	S587	3213.0	14.0	226.0	135.0
530	S586	3199.0	14.0	91.0	−135.0
531	S585	3185.0	14.0	226.0	135.0
532	S584	3171.0	14.0	91.0	−135.0
533	S583	3157.0	14.0	226.0	135.0
534	S582	3143.0	14.0	91.0	−135.0
535	S581	3129.0	14.0	226.0	135.0
536	S580	3115.0	14.0	91.0	−135.0
537	S579	3101.0	14.0	226.0	135.0
538	S578	3087.0	14.0	91.0	−135.0
539	S577	3073.0	14.0	226.0	135.0
540	S576	3059.0	14.0	91.0	−135.0
541	S575	3045.0	14.0	226.0	135.0
542	S574	3031.0	14.0	91.0	−135.0
543	S573	3017.0	14.0	226.0	135.0
544	S572	3003.0	14.0	91.0	−135.0
545	S571	2989.0	14.0	226.0	135.0
546	S570	2975.0	14.0	91.0	−135.0
547	S569	2961.0	14.0	226.0	135.0
548	S568	2947.0	14.0	91.0	−135.0
549	S567	2933.0	14.0	226.0	135.0
550	S566	2919.0	14.0	91.0	−135.0

pad No	pad name	X	ΔX	Y	ΔY
551	S565	2905.0	14.0	226.0	135.0
552	S564	2891.0	14.0	91.0	−135.0
553	S563	2877.0	14.0	226.0	135.0
554	S562	2863.0	14.0	91.0	−135.0
555	S561	2849.0	14.0	226.0	135.0
556	S560	2835.0	14.0	91.0	−135.0
557	S559	2821.0	14.0	226.0	135.0
558	S558	2807.0	14.0	91.0	−135.0
559	S557	2793.0	14.0	226.0	135.0
560	S556	2779.0	14.0	91.0	−135.0
561	S555	2765.0	14.0	226.0	135.0
562	S554	2751.0	14.0	91.0	−135.0
563	S553	2737.0	14.0	226.0	135.0
564	S552	2723.0	14.0	91.0	−135.0
565	S551	2709.0	14.0	226.0	135.0
566	S550	2695.0	14.0	91.0	−135.0
567	S549	2681.0	14.0	226.0	135.0
568	S548	2667.0	14.0	91.0	−135.0
569	S547	2653.0	14.0	226.0	135.0
570	S546	2639.0	14.0	91.0	−135.0
571	S545	2625.0	14.0	226.0	135.0
572	S544	2611.0	14.0	91.0	−135.0
573	S543	2597.0	14.0	226.0	135.0
574	S542	2583.0	14.0	91.0	−135.0
575	S541	2569.0	14.0	226.0	135.0
576	S540	2555.0	14.0	91.0	−135.0
577	S539	2541.0	14.0	226.0	135.0
578	S538	2527.0	14.0	91.0	−135.0
579	S537	2513.0	14.0	226.0	135.0
580	S536	2499.0	14.0	91.0	−135.0
581	S535	2485.0	14.0	226.0	135.0
582	S534	2471.0	14.0	91.0	−135.0
583	S533	2457.0	14.0	226.0	135.0
584	S532	2443.0	14.0	91.0	−135.0
585	S531	2429.0	14.0	226.0	135.0
586	S530	2415.0	14.0	91.0	−135.0
587	S529	2401.0	14.0	226.0	135.0
588	S528	2387.0	14.0	91.0	−135.0
589	S527	2373.0	14.0	226.0	135.0
590	S526	2359.0	14.0	91.0	−135.0
591	S525	2345.0	14.0	226.0	135.0
592	S524	2331.0	14.0	91.0	−135.0
593	S523	2317.0	14.0	226.0	135.0
594	S522	2303.0	14.0	91.0	−135.0
595	S521	2289.0	14.0	226.0	135.0
596	S520	2275.0	14.0	91.0	−135.0
597	S519	2261.0	14.0	226.0	135.0
598	S518	2247.0	14.0	91.0	−135.0
599	S517	2233.0	14.0	226.0	135.0
600	S516	2219.0	14.0	91.0	−135.0

R61526 Pad Coordinates (No.7) (Unit: um)

pad No	pad name	X	ΔX	Y	ΔY
601	S515	2205.0	14.0	226.0	135.0
602	S514	2191.0	14.0	91.0	−135.0
603	S513	2177.0	14.0	226.0	135.0
604	S512	2163.0	14.0	91.0	−135.0
605	S511	2149.0	14.0	226.0	135.0
606	S510	2135.0	14.0	91.0	−135.0
607	S509	2121.0	14.0	226.0	135.0
608	S508	2107.0	14.0	91.0	−135.0
609	S507	2093.0	14.0	226.0	135.0
610	S506	2079.0	14.0	91.0	−135.0
611	S505	2065.0	14.0	226.0	135.0
612	S504	2051.0	14.0	91.0	−135.0
613	S503	2037.0	14.0	226.0	135.0
614	S502	2023.0	14.0	91.0	−135.0
615	S501	2009.0	14.0	226.0	135.0
616	S500	1995.0	14.0	91.0	−135.0
617	S499	1981.0	14.0	226.0	135.0
618	S498	1967.0	14.0	91.0	−135.0
619	S497	1953.0	14.0	226.0	135.0
620	S496	1939.0	14.0	91.0	−135.0
621	S495	1925.0	14.0	226.0	135.0
622	S494	1911.0	14.0	91.0	−135.0
623	S493	1897.0	14.0	226.0	135.0
624	S492	1883.0	14.0	91.0	−135.0
625	S491	1869.0	14.0	226.0	135.0
626	S490	1855.0	14.0	91.0	−135.0
627	S489	1841.0	14.0	226.0	135.0
628	S488	1827.0	14.0	91.0	−135.0
629	S487	1813.0	14.0	226.0	135.0
630	S486	1799.0	14.0	91.0	−135.0
631	S485	1785.0	14.0	226.0	135.0
632	S484	1771.0	14.0	91.0	−135.0
633	S483	1757.0	14.0	226.0	135.0
634	S482	1743.0	14.0	91.0	−135.0
635	S481	1729.0	14.0	226.0	135.0
636	S480	1715.0	14.0	91.0	−135.0
637	S479	1701.0	14.0	226.0	135.0
638	S478	1687.0	14.0	91.0	−135.0
639	S477	1673.0	14.0	226.0	135.0
640	S476	1659.0	14.0	91.0	−135.0
641	S475	1645.0	14.0	226.0	135.0
642	S474	1631.0	14.0	91.0	−135.0
643	S473	1617.0	14.0	226.0	135.0
644	S472	1603.0	14.0	91.0	−135.0
645	S471	1589.0	14.0	226.0	135.0
646	S470	1575.0	14.0	91.0	−135.0
647	S469	1561.0	14.0	226.0	135.0
648	S468	1547.0	14.0	91.0	−135.0
649	S467	1533.0	14.0	226.0	135.0
650	S466	1519.0	14.0	91.0	−135.0
651	S465	1505.0	14.0	226.0	135.0
652	S464	1491.0	14.0	91.0	−135.0
653	S463	1477.0	14.0	226.0	135.0
654	S462	1463.0	14.0	91.0	−135.0
655	S461	1449.0	14.0	226.0	135.0
656	S460	1435.0	14.0	91.0	−135.0
657	S459	1421.0	14.0	226.0	135.0
658	S458	1407.0	14.0	91.0	−135.0
659	S457	1393.0	14.0	226.0	135.0
660	S456	1379.0	14.0	91.0	−135.0
661	S455	1365.0	14.0	226.0	135.0
662	S454	1351.0	14.0	91.0	−135.0
663	S453	1337.0	14.0	226.0	135.0
664	S452	1323.0	14.0	91.0	−135.0
665	S451	1309.0	14.0	226.0	135.0
666	S450	1295.0	14.0	91.0	−135.0
667	S449	1281.0	14.0	226.0	135.0
668	S448	1267.0	14.0	91.0	−135.0
669	S447	1253.0	14.0	226.0	135.0
670	S446	1239.0	14.0	91.0	−135.0
671	S445	1225.0	14.0	226.0	135.0
672	S444	1211.0	14.0	91.0	−135.0
673	S443	1197.0	14.0	226.0	135.0
674	S442	1183.0	14.0	91.0	−135.0
675	S441	1169.0	14.0	226.0	135.0
676	S440	1155.0	14.0	91.0	−135.0
677	S439	1141.0	14.0	226.0	135.0
678	S438	1127.0	14.0	91.0	−135.0
679	S437	1113.0	14.0	226.0	135.0
680	S436	1099.0	14.0	91.0	−135.0
681	S435	1085.0	14.0	226.0	135.0
682	S434	1071.0	14.0	91.0	−135.0
683	S433	1057.0	14.0	226.0	135.0
684	S432	1043.0	14.0	91.0	−135.0
685	S431	1029.0	14.0	226.0	135.0
686	S430	1015.0	14.0	91.0	−135.0
687	S429	1001.0	14.0	226.0	135.0
688	S428	987.0	14.0	91.0	−135.0
689	S427	973.0	14.0	226.0	135.0
690	S426	959.0	14.0	91.0	−135.0
691	S425	945.0	14.0	226.0	135.0
692	S424	931.0	14.0	91.0	−135.0
693	S423	917.0	14.0	226.0	135.0
694	S422	903.0	14.0	91.0	−135.0
695	S421	889.0	14.0	226.0	135.0
696	S420	875.0	14.0	91.0	−135.0
697	S419	861.0	14.0	226.0	135.0
698	S418	847.0	14.0	91.0	−135.0
699	S417	833.0	14.0	226.0	135.0
700	S416	819.0	14.0	91.0	−135.0

R61526 Pad Coordinates (No.8) (Unit: um)

pad No	pad name	X	ΔX	Y	ΔY
701	S415	805.0	14.0	226.0	135.0
702	S414	791.0	14.0	91.0	−135.0
703	S413	777.0	14.0	226.0	135.0
704	S412	763.0	14.0	91.0	−135.0
705	S411	749.0	14.0	226.0	135.0
706	S410	735.0	14.0	91.0	−135.0
707	S409	721.0	14.0	226.0	135.0
708	S408	707.0	14.0	91.0	−135.0
709	S407	693.0	14.0	226.0	135.0
710	S406	679.0	14.0	91.0	−135.0
711	S405	665.0	14.0	226.0	135.0
712	S404	651.0	14.0	91.0	−135.0
713	S403	637.0	14.0	226.0	135.0
714	S402	623.0	14.0	91.0	−135.0
715	S401	609.0	14.0	226.0	135.0
716	S400	595.0	14.0	91.0	−135.0
717	S399	581.0	14.0	226.0	135.0
718	S398	567.0	14.0	91.0	−135.0
719	S397	553.0	14.0	226.0	135.0
720	S396	539.0	14.0	91.0	−135.0
721	S395	525.0	14.0	226.0	135.0
722	S394	511.0	14.0	91.0	−135.0
723	S393	497.0	14.0	226.0	135.0
724	S392	483.0	14.0	91.0	−135.0
725	S391	469.0	14.0	226.0	135.0
726	S390	455.0	14.0	91.0	−135.0
727	S389	441.0	14.0	226.0	135.0
728	S388	427.0	14.0	91.0	−135.0
729	S387	413.0	14.0	226.0	135.0
730	S386	399.0	14.0	91.0	−135.0
731	S385	385.0	14.0	226.0	135.0
732	S384	371.0	14.0	91.0	−135.0
733	S383	357.0	14.0	226.0	135.0
734	S382	343.0	14.0	91.0	−135.0
735	S381	329.0	14.0	226.0	135.0
736	S380	315.0	14.0	91.0	−135.0
737	S379	301.0	14.0	226.0	135.0
738	S378	287.0	14.0	91.0	−135.0
739	S377	273.0	14.0	226.0	135.0
740	S376	259.0	14.0	91.0	−135.0
741	S375	245.0	14.0	226.0	135.0
742	S374	231.0	14.0	91.0	−135.0
743	S373	217.0	14.0	226.0	135.0
744	S372	203.0	14.0	91.0	−135.0
745	S371	189.0	14.0	226.0	135.0
746	S370	175.0	14.0	91.0	−135.0
747	S369	161.0	14.0	226.0	135.0
748	S368	147.0	14.0	91.0	−135.0
749	S367	133.0	14.0	226.0	135.0
750	S366	119.0	14.0	91.0	−135.0

pad No	pad name	X	ΔX	Y	ΔY
751	S365	105.0	14.0	226.0	135.0
752	S364	91.0	14.0	91.0	−135.0
753	S363	77.0	14.0	226.0	135.0
754	S362	63.0	14.0	91.0	−135.0
755	S361	49.0	98.0	226.0	135.0
756	S360	−49.0	14.0	91.0	−135.0
757	S359	−63.0	14.0	226.0	135.0
758	S358	−77.0	14.0	91.0	−135.0
759	S357	−91.0	14.0	226.0	135.0
760	S356	−105.0	14.0	91.0	−135.0
761	S355	−119.0	14.0	226.0	135.0
762	S354	−133.0	14.0	91.0	−135.0
763	S353	−147.0	14.0	226.0	135.0
764	S352	−161.0	14.0	91.0	−135.0
765	S351	−175.0	14.0	226.0	135.0
766	S350	−189.0	14.0	91.0	−135.0
767	S349	−203.0	14.0	226.0	135.0
768	S348	−217.0	14.0	91.0	−135.0
769	S347	−231.0	14.0	226.0	135.0
770	S346	−245.0	14.0	91.0	−135.0
771	S345	−259.0	14.0	226.0	135.0
772	S344	−273.0	14.0	91.0	−135.0
773	S343	−287.0	14.0	226.0	135.0
774	S342	−301.0	14.0	91.0	−135.0
775	S341	−315.0	14.0	226.0	135.0
776	S340	−329.0	14.0	91.0	−135.0
777	S339	−343.0	14.0	226.0	135.0
778	S338	−357.0	14.0	91.0	−135.0
779	S337	−371.0	14.0	226.0	135.0
780	S336	−385.0	14.0	91.0	−135.0
781	S335	−399.0	14.0	226.0	135.0
782	S334	−413.0	14.0	91.0	−135.0
783	S333	−427.0	14.0	226.0	135.0
784	S332	−441.0	14.0	91.0	−135.0
785	S331	−455.0	14.0	226.0	135.0
786	S330	−469.0	14.0	91.0	−135.0
787	S329	−483.0	14.0	226.0	135.0
788	S328	−497.0	14.0	91.0	−135.0
789	S327	−511.0	14.0	226.0	135.0
790	S326	−525.0	14.0	91.0	−135.0
791	S325	−539.0	14.0	226.0	135.0
792	S324	−553.0	14.0	91.0	−135.0
793	S323	−567.0	14.0	226.0	135.0
794	S322	−581.0	14.0	91.0	−135.0
795	S321	−595.0	14.0	226.0	135.0
796	S320	−609.0	14.0	91.0	−135.0
797	S319	−623.0	14.0	226.0	135.0
798	S318	−637.0	14.0	91.0	−135.0
799	S317	−651.0	14.0	226.0	135.0
800	S316	−665.0	14.0	91.0	−135.0

R61526 Pad Coordinates (No.9) (Unit: um)

pad No	pad name	X	ΔX	Y	ΔY
801	S315	−679.0	14.0	226.0	135.0
802	S314	−693.0	14.0	91.0	−135.0
803	S313	−707.0	14.0	226.0	135.0
804	S312	−721.0	14.0	91.0	−135.0
805	S311	−735.0	14.0	226.0	135.0
806	S310	−749.0	14.0	91.0	−135.0
807	S309	−763.0	14.0	226.0	135.0
808	S308	−777.0	14.0	91.0	−135.0
809	S307	−791.0	14.0	226.0	135.0
810	S306	−805.0	14.0	91.0	−135.0
811	S305	−819.0	14.0	226.0	135.0
812	S304	−833.0	14.0	91.0	−135.0
813	S303	−847.0	14.0	226.0	135.0
814	S302	−861.0	14.0	91.0	−135.0
815	S301	−875.0	14.0	226.0	135.0
816	S300	−889.0	14.0	91.0	−135.0
817	S299	−903.0	14.0	226.0	135.0
818	S298	−917.0	14.0	91.0	−135.0
819	S297	−931.0	14.0	226.0	135.0
820	S296	−945.0	14.0	91.0	−135.0
821	S295	−959.0	14.0	226.0	135.0
822	S294	−973.0	14.0	91.0	−135.0
823	S293	−987.0	14.0	226.0	135.0
824	S292	−1001.0	14.0	91.0	−135.0
825	S291	−1015.0	14.0	226.0	135.0
826	S290	−1029.0	14.0	91.0	−135.0
827	S289	−1043.0	14.0	226.0	135.0
828	S288	−1057.0	14.0	91.0	−135.0
829	S287	−1071.0	14.0	226.0	135.0
830	S286	−1085.0	14.0	91.0	−135.0
831	S285	−1099.0	14.0	226.0	135.0
832	S284	−1113.0	14.0	91.0	−135.0
833	S283	−1127.0	14.0	226.0	135.0
834	S282	−1141.0	14.0	91.0	−135.0
835	S281	−1155.0	14.0	226.0	135.0
836	S280	−1169.0	14.0	91.0	−135.0
837	S279	−1183.0	14.0	226.0	135.0
838	S278	−1197.0	14.0	91.0	−135.0
839	S277	−1211.0	14.0	226.0	135.0
840	S276	−1225.0	14.0	91.0	−135.0
841	S275	−1239.0	14.0	226.0	135.0
842	S274	−1253.0	14.0	91.0	−135.0
843	S273	−1267.0	14.0	226.0	135.0
844	S272	−1281.0	14.0	91.0	−135.0
845	S271	−1295.0	14.0	226.0	135.0
846	S270	−1309.0	14.0	91.0	−135.0
847	S269	−1323.0	14.0	226.0	135.0
848	S268	−1337.0	14.0	91.0	−135.0
849	S267	−1351.0	14.0	226.0	135.0
850	S266	−1365.0	14.0	91.0	−135.0

pad No	pad name	X	ΔX	Y	ΔY
851	S265	−1379.0	14.0	226.0	135.0
852	S264	−1393.0	14.0	91.0	−135.0
853	S263	−1407.0	14.0	226.0	135.0
854	S262	−1421.0	14.0	91.0	−135.0
855	S261	−1435.0	14.0	226.0	135.0
856	S260	−1449.0	14.0	91.0	−135.0
857	S259	−1463.0	14.0	226.0	135.0
858	S258	−1477.0	14.0	91.0	−135.0
859	S257	−1491.0	14.0	226.0	135.0
860	S256	−1505.0	14.0	91.0	−135.0
861	S255	−1519.0	14.0	226.0	135.0
862	S254	−1533.0	14.0	91.0	−135.0
863	S253	−1547.0	14.0	226.0	135.0
864	S252	−1561.0	14.0	91.0	−135.0
865	S251	−1575.0	14.0	226.0	135.0
866	S250	−1589.0	14.0	91.0	−135.0
867	S249	−1603.0	14.0	226.0	135.0
868	S248	−1617.0	14.0	91.0	−135.0
869	S247	−1631.0	14.0	226.0	135.0
870	S246	−1645.0	14.0	91.0	−135.0
871	S245	−1659.0	14.0	226.0	135.0
872	S244	−1673.0	14.0	91.0	−135.0
873	S243	−1687.0	14.0	226.0	135.0
874	S242	−1701.0	14.0	91.0	−135.0
875	S241	−1715.0	14.0	226.0	135.0
876	S240	−1729.0	14.0	91.0	−135.0
877	S239	−1743.0	14.0	226.0	135.0
878	S238	−1757.0	14.0	91.0	−135.0
879	S237	−1771.0	14.0	226.0	135.0
880	S236	−1785.0	14.0	91.0	−135.0
881	S235	−1799.0	14.0	226.0	135.0
882	S234	−1813.0	14.0	91.0	−135.0
883	S233	−1827.0	14.0	226.0	135.0
884	S232	−1841.0	14.0	91.0	−135.0
885	S231	−1855.0	14.0	226.0	135.0
886	S230	−1869.0	14.0	91.0	−135.0
887	S229	−1883.0	14.0	226.0	135.0
888	S228	−1897.0	14.0	91.0	−135.0
889	S227	−1911.0	14.0	226.0	135.0
890	S226	−1925.0	14.0	91.0	−135.0
891	S225	−1939.0	14.0	226.0	135.0
892	S224	−1953.0	14.0	91.0	−135.0
893	S223	−1967.0	14.0	226.0	135.0
894	S222	−1981.0	14.0	91.0	−135.0
895	S221	−1995.0	14.0	226.0	135.0
896	S220	−2009.0	14.0	91.0	−135.0
897	S219	−2023.0	14.0	226.0	135.0
898	S218	−2037.0	14.0	91.0	−135.0
899	S217	−2051.0	14.0	226.0	135.0
900	S216	−2065.0	14.0	91.0	−135.0

R61526 Pad Coordinates (No.10) (Unit: um)

pad No	pad name	X	ΔX	Y	ΔY
901	S215	−2079.0	14.0	226.0	135.0
902	S214	−2093.0	14.0	91.0	−135.0
903	S213	−2107.0	14.0	226.0	135.0
904	S212	−2121.0	14.0	91.0	−135.0
905	S211	−2135.0	14.0	226.0	135.0
906	S210	−2149.0	14.0	91.0	−135.0
907	S209	−2163.0	14.0	226.0	135.0
908	S208	−2177.0	14.0	91.0	−135.0
909	S207	−2191.0	14.0	226.0	135.0
910	S206	−2205.0	14.0	91.0	−135.0
911	S205	−2219.0	14.0	226.0	135.0
912	S204	−2233.0	14.0	91.0	−135.0
913	S203	−2247.0	14.0	226.0	135.0
914	S202	−2261.0	14.0	91.0	−135.0
915	S201	−2275.0	14.0	226.0	135.0
916	S200	−2289.0	14.0	91.0	−135.0
917	S199	−2303.0	14.0	226.0	135.0
918	S198	−2317.0	14.0	91.0	−135.0
919	S197	−2331.0	14.0	226.0	135.0
920	S196	−2345.0	14.0	91.0	−135.0
921	S195	−2359.0	14.0	226.0	135.0
922	S194	−2373.0	14.0	91.0	−135.0
923	S193	−2387.0	14.0	226.0	135.0
924	S192	−2401.0	14.0	91.0	−135.0
925	S191	−2415.0	14.0	226.0	135.0
926	S190	−2429.0	14.0	91.0	−135.0
927	S189	−2443.0	14.0	226.0	135.0
928	S188	−2457.0	14.0	91.0	−135.0
929	S187	−2471.0	14.0	226.0	135.0
930	S186	−2485.0	14.0	91.0	−135.0
931	S185	−2499.0	14.0	226.0	135.0
932	S184	−2513.0	14.0	91.0	−135.0
933	S183	−2527.0	14.0	226.0	135.0
934	S182	−2541.0	14.0	91.0	−135.0
935	S181	−2555.0	14.0	226.0	135.0
936	S180	−2569.0	14.0	91.0	−135.0
937	S179	−2583.0	14.0	226.0	135.0
938	S178	−2597.0	14.0	91.0	−135.0
939	S177	−2611.0	14.0	226.0	135.0
940	S176	−2625.0	14.0	91.0	−135.0
941	S175	−2639.0	14.0	226.0	135.0
942	S174	−2653.0	14.0	91.0	−135.0
943	S173	−2667.0	14.0	226.0	135.0
944	S172	−2681.0	14.0	91.0	−135.0
945	S171	−2695.0	14.0	226.0	135.0
946	S170	−2709.0	14.0	91.0	−135.0
947	S169	−2723.0	14.0	226.0	135.0
948	S168	−2737.0	14.0	91.0	−135.0
949	S167	−2751.0	14.0	226.0	135.0
950	S166	−2765.0	14.0	91.0	−135.0

pad No	pad name	X	ΔX	Y	ΔY
951	S165	−2779.0	14.0	226.0	135.0
952	S164	−2793.0	14.0	91.0	−135.0
953	S163	−2807.0	14.0	226.0	135.0
954	S162	−2821.0	14.0	91.0	−135.0
955	S161	−2835.0	14.0	226.0	135.0
956	S160	−2849.0	14.0	91.0	−135.0
957	S159	−2863.0	14.0	226.0	135.0
958	S158	−2877.0	14.0	91.0	−135.0
959	S157	−2891.0	14.0	226.0	135.0
960	S156	−2905.0	14.0	91.0	−135.0
961	S155	−2919.0	14.0	226.0	135.0
962	S154	−2933.0	14.0	91.0	−135.0
963	S153	−2947.0	14.0	226.0	135.0
964	S152	−2961.0	14.0	91.0	−135.0
965	S151	−2975.0	14.0	226.0	135.0
966	S150	−2989.0	14.0	91.0	−135.0
967	S149	−3003.0	14.0	226.0	135.0
968	S148	−3017.0	14.0	91.0	−135.0
969	S147	−3031.0	14.0	226.0	135.0
970	S146	−3045.0	14.0	91.0	−135.0
971	S145	−3059.0	14.0	226.0	135.0
972	S144	−3073.0	14.0	91.0	−135.0
973	S143	−3087.0	14.0	226.0	135.0
974	S142	−3101.0	14.0	91.0	−135.0
975	S141	−3115.0	14.0	226.0	135.0
976	S140	−3129.0	14.0	91.0	−135.0
977	S139	−3143.0	14.0	226.0	135.0
978	S138	−3157.0	14.0	91.0	−135.0
979	S137	−3171.0	14.0	226.0	135.0
980	S136	−3185.0	14.0	91.0	−135.0
981	S135	−3199.0	14.0	226.0	135.0
982	S134	−3213.0	14.0	91.0	−135.0
983	S133	−3227.0	14.0	226.0	135.0
984	S132	−3241.0	14.0	91.0	−135.0
985	S131	−3255.0	14.0	226.0	135.0
986	S130	−3269.0	14.0	91.0	−135.0
987	S129	−3283.0	14.0	226.0	135.0
988	S128	−3297.0	14.0	91.0	−135.0
989	S127	−3311.0	14.0	226.0	135.0
990	S126	−3325.0	14.0	91.0	−135.0
991	S125	−3339.0	14.0	226.0	135.0
992	S124	−3353.0	14.0	91.0	−135.0
993	S123	−3367.0	14.0	226.0	135.0
994	S122	−3381.0	14.0	91.0	−135.0
995	S121	−3395.0	14.0	226.0	135.0
996	S120	−3409.0	14.0	91.0	−135.0
997	S119	−3423.0	14.0	226.0	135.0
998	S118	−3437.0	14.0	91.0	−135.0
999	S117	−3451.0	14.0	226.0	135.0
1000	S116	−3465.0	14.0	91.0	−135.0

R61526 Pad Coordinates (No.11) (Unit: um)

pad No	pad name	X	ΔX	Y	ΔY
1001	S115	−3479.0	14.0	226.0	135.0
1002	S114	−3493.0	14.0	91.0	−135.0
1003	S113	−3507.0	14.0	226.0	135.0
1004	S112	−3521.0	14.0	91.0	−135.0
1005	S111	−3535.0	14.0	226.0	135.0
1006	S110	−3549.0	14.0	91.0	−135.0
1007	S109	−3563.0	14.0	226.0	135.0
1008	S108	−3577.0	14.0	91.0	−135.0
1009	S107	−3591.0	14.0	226.0	135.0
1010	S106	−3605.0	14.0	91.0	−135.0
1011	S105	−3619.0	14.0	226.0	135.0
1012	S104	−3633.0	14.0	91.0	−135.0
1013	S103	−3647.0	14.0	226.0	135.0
1014	S102	−3661.0	14.0	91.0	−135.0
1015	S101	−3675.0	14.0	226.0	135.0
1016	S100	−3689.0	14.0	91.0	−135.0
1017	S99	−3703.0	14.0	226.0	135.0
1018	S98	−3717.0	14.0	91.0	−135.0
1019	S97	−3731.0	14.0	226.0	135.0
1020	S96	−3745.0	14.0	91.0	−135.0
1021	S95	−3759.0	14.0	226.0	135.0
1022	S94	−3773.0	14.0	91.0	−135.0
1023	S93	−3787.0	14.0	226.0	135.0
1024	S92	−3801.0	14.0	91.0	−135.0
1025	S91	−3815.0	14.0	226.0	135.0
1026	S90	−3829.0	14.0	91.0	−135.0
1027	S89	−3843.0	14.0	226.0	135.0
1028	S88	−3857.0	14.0	91.0	−135.0
1029	S87	−3871.0	14.0	226.0	135.0
1030	S86	−3885.0	14.0	91.0	−135.0
1031	S85	−3899.0	14.0	226.0	135.0
1032	S84	−3913.0	14.0	91.0	−135.0
1033	S83	−3927.0	14.0	226.0	135.0
1034	S82	−3941.0	14.0	91.0	−135.0
1035	S81	−3955.0	14.0	226.0	135.0
1036	S80	−3969.0	14.0	91.0	−135.0
1037	S79	−3983.0	14.0	226.0	135.0
1038	S78	−3997.0	14.0	91.0	−135.0
1039	S77	−4011.0	14.0	226.0	135.0
1040	S76	−4025.0	14.0	91.0	−135.0
1041	S75	−4039.0	14.0	226.0	135.0
1042	S74	−4053.0	14.0	91.0	−135.0
1043	S73	−4067.0	14.0	226.0	135.0
1044	S72	−4081.0	14.0	91.0	−135.0
1045	S71	−4095.0	14.0	226.0	135.0
1046	S70	−4109.0	14.0	91.0	−135.0
1047	S69	−4123.0	14.0	226.0	135.0
1048	S68	−4137.0	14.0	91.0	−135.0
1049	S67	−4151.0	14.0	226.0	135.0
1050	S66	−4165.0	14.0	91.0	−135.0

pad No	pad name	X	ΔX	Y	ΔY
1051	S65	−4179.0	14.0	226.0	135.0
1052	S64	−4193.0	14.0	91.0	−135.0
1053	S63	−4207.0	14.0	226.0	135.0
1054	S62	−4221.0	14.0	91.0	−135.0
1055	S61	−4235.0	14.0	226.0	135.0
1056	S60	−4249.0	14.0	91.0	−135.0
1057	S59	−4263.0	14.0	226.0	135.0
1058	S58	−4277.0	14.0	91.0	−135.0
1059	S57	−4291.0	14.0	226.0	135.0
1060	S56	−4305.0	14.0	91.0	−135.0
1061	S55	−4319.0	14.0	226.0	135.0
1062	S54	−4333.0	14.0	91.0	−135.0
1063	S53	−4347.0	14.0	226.0	135.0
1064	S52	−4361.0	14.0	91.0	−135.0
1065	S51	−4375.0	14.0	226.0	135.0
1066	S50	−4389.0	14.0	91.0	−135.0
1067	S49	−4403.0	14.0	226.0	135.0
1068	S48	−4417.0	14.0	91.0	−135.0
1069	S47	−4431.0	14.0	226.0	135.0
1070	S46	−4445.0	14.0	91.0	−135.0
1071	S45	−4459.0	14.0	226.0	135.0
1072	S44	−4473.0	14.0	91.0	−135.0
1073	S43	−4487.0	14.0	226.0	135.0
1074	S42	−4501.0	14.0	91.0	−135.0
1075	S41	−4515.0	14.0	226.0	135.0
1076	S40	−4529.0	14.0	91.0	−135.0
1077	S39	−4543.0	14.0	226.0	135.0
1078	S38	−4557.0	14.0	91.0	−135.0
1079	S37	−4571.0	14.0	226.0	135.0
1080	S36	−4585.0	14.0	91.0	−135.0
1081	S35	−4599.0	14.0	226.0	135.0
1082	S34	−4613.0	14.0	91.0	−135.0
1083	S33	−4627.0	14.0	226.0	135.0
1084	S32	−4641.0	14.0	91.0	−135.0
1085	S31	−4655.0	14.0	226.0	135.0
1086	S30	−4669.0	14.0	91.0	−135.0
1087	S29	−4683.0	14.0	226.0	135.0
1088	S28	−4697.0	14.0	91.0	−135.0
1089	S27	−4711.0	14.0	226.0	135.0
1090	S26	−4725.0	14.0	91.0	−135.0
1091	S25	−4739.0	14.0	226.0	135.0
1092	S24	−4753.0	14.0	91.0	−135.0
1093	S23	−4767.0	14.0	226.0	135.0
1094	S22	−4781.0	14.0	91.0	−135.0
1095	S21	−4795.0	14.0	226.0	135.0
1096	S20	−4809.0	14.0	91.0	−135.0
1097	S19	−4823.0	14.0	226.0	135.0
1098	S18	−4837.0	14.0	91.0	−135.0
1099	S17	−4851.0	14.0	226.0	135.0
1100	S16	−4865.0	14.0	91.0	−135.0

R61526 Pad Coordinates (No.12) (Unit: um)

pad No	pad name	X	ΔX	Y	ΔY
1101	S15	−4879.0	14.0	226.0	135.0
1102	S14	−4893.0	14.0	91.0	−135.0
1103	S13	−4907.0	14.0	226.0	135.0
1104	S12	−4921.0	14.0	91.0	−135.0
1105	S11	−4935.0	14.0	226.0	135.0
1106	S10	−4949.0	14.0	91.0	−135.0
1107	S9	−4963.0	14.0	226.0	135.0
1108	S8	−4977.0	14.0	91.0	−135.0
1109	S7	−4991.0	14.0	226.0	135.0
1110	S6	−5005.0	14.0	91.0	−135.0
1111	S5	−5019.0	14.0	226.0	135.0
1112	S4	−5033.0	14.0	91.0	−135.0
1113	S3	−5047.0	14.0	226.0	135.0
1114	S2	−5061.0	14.0	91.0	−135.0
1115	S1	−5075.0	56.0	226.0	135.0
1116	G319	−5131.0	14.0	91.0	−135.0
1117	G317	−5145.0	14.0	226.0	135.0
1118	G315	−5159.0	14.0	91.0	−135.0
1119	G313	−5173.0	14.0	226.0	135.0
1120	G311	−5187.0	14.0	91.0	−135.0
1121	G309	−5201.0	14.0	226.0	135.0
1122	G307	−5215.0	14.0	91.0	−135.0
1123	G305	−5229.0	14.0	226.0	135.0
1124	G303	−5243.0	14.0	91.0	−135.0
1125	G301	−5257.0	14.0	226.0	135.0
1126	G299	−5271.0	14.0	91.0	−135.0
1127	G297	−5285.0	14.0	226.0	135.0
1128	G295	−5299.0	14.0	91.0	−135.0
1129	G293	−5313.0	14.0	226.0	135.0
1130	G291	−5327.0	14.0	91.0	−135.0
1131	G289	−5341.0	14.0	226.0	135.0
1132	G287	−5355.0	14.0	91.0	−135.0
1133	G285	−5369.0	14.0	226.0	135.0
1134	G283	−5383.0	14.0	91.0	−135.0
1135	G281	−5397.0	14.0	226.0	135.0
1136	G279	−5411.0	14.0	91.0	−135.0
1137	G277	−5425.0	14.0	226.0	135.0
1138	G275	−5439.0	14.0	91.0	−135.0
1139	G273	−5453.0	14.0	226.0	135.0
1140	G271	−5467.0	14.0	91.0	−135.0
1141	G269	−5481.0	14.0	226.0	135.0
1142	G267	−5495.0	14.0	91.0	−135.0
1143	G265	−5509.0	14.0	226.0	135.0
1144	G263	−5523.0	14.0	91.0	−135.0
1145	G261	−5537.0	14.0	226.0	135.0
1146	G259	−5551.0	14.0	91.0	−135.0
1147	G257	−5565.0	14.0	226.0	135.0
1148	G255	−5579.0	14.0	91.0	−135.0
1149	G253	−5593.0	14.0	226.0	135.0
1150	G251	−5607.0	14.0	91.0	−135.0

pad No	pad name	X	ΔX	Y	ΔY
1151	G249	−5621.0	14.0	226.0	135.0
1152	G247	−5635.0	14.0	91.0	−135.0
1153	G245	−5649.0	14.0	226.0	135.0
1154	G243	−5663.0	14.0	91.0	−135.0
1155	G241	−5677.0	14.0	226.0	135.0
1156	G239	−5691.0	14.0	91.0	−135.0
1157	G237	−5705.0	14.0	226.0	135.0
1158	G235	−5719.0	14.0	91.0	−135.0
1159	G233	−5733.0	14.0	226.0	135.0
1160	G231	−5747.0	14.0	91.0	−135.0
1161	G229	−5761.0	14.0	226.0	135.0
1162	G227	−5775.0	14.0	91.0	−135.0
1163	G225	−5789.0	14.0	226.0	135.0
1164	G223	−5803.0	14.0	91.0	−135.0
1165	G221	−5817.0	14.0	226.0	135.0
1166	G219	−5831.0	14.0	91.0	−135.0
1167	G217	−5845.0	14.0	226.0	135.0
1168	G215	−5859.0	14.0	91.0	−135.0
1169	G213	−5873.0	14.0	226.0	135.0
1170	G211	−5887.0	14.0	91.0	−135.0
1171	G209	−5901.0	14.0	226.0	135.0
1172	G207	−5915.0	14.0	91.0	−135.0
1173	G205	−5929.0	14.0	226.0	135.0
1174	G203	−5943.0	14.0	91.0	−135.0
1175	G201	−5957.0	14.0	226.0	135.0
1176	G199	−5971.0	14.0	91.0	−135.0
1177	G197	−5985.0	14.0	226.0	135.0
1178	G195	−5999.0	14.0	91.0	−135.0
1179	G193	−6013.0	14.0	226.0	135.0
1180	G191	−6027.0	14.0	91.0	−135.0
1181	G189	−6041.0	14.0	226.0	135.0
1182	G187	−6055.0	14.0	91.0	−135.0
1183	G185	−6069.0	14.0	226.0	135.0
1184	G183	−6083.0	14.0	91.0	−135.0
1185	G181	−6097.0	14.0	226.0	135.0
1186	G179	−6111.0	14.0	91.0	−135.0
1187	G177	−6125.0	14.0	226.0	135.0
1188	G175	−6139.0	14.0	91.0	−135.0
1189	G173	−6153.0	14.0	226.0	135.0
1190	G171	−6167.0	14.0	91.0	−135.0
1191	G169	−6181.0	14.0	226.0	135.0
1192	G167	−6195.0	14.0	91.0	−135.0
1193	G165	−6209.0	14.0	226.0	135.0
1194	G163	−6223.0	14.0	91.0	−135.0
1195	G161	−6237.0	14.0	226.0	135.0
1196	G159	−6251.0	14.0	91.0	−135.0
1197	G157	−6265.0	14.0	226.0	135.0
1198	G155	−6279.0	14.0	91.0	−135.0
1199	G153	−6293.0	14.0	226.0	135.0
1200	G151	−6307.0	14.0	91.0	−135.0

R61526 Pad Coordinates (No.13) (Unit: um)

pad No	pad name	X	ΔX	Y	ΔY
1201	G149	−6321.0	14.0	226.0	135.0
1202	G147	−6335.0	14.0	91.0	−135.0
1203	G145	−6349.0	14.0	226.0	135.0
1204	G143	−6363.0	14.0	91.0	−135.0
1205	G141	−6377.0	14.0	226.0	135.0
1206	G139	−6391.0	14.0	91.0	−135.0
1207	G137	−6405.0	14.0	226.0	135.0
1208	G135	−6419.0	14.0	91.0	−135.0
1209	G133	−6433.0	14.0	226.0	135.0
1210	G131	−6447.0	14.0	91.0	−135.0
1211	G129	−6461.0	14.0	226.0	135.0
1212	G127	−6475.0	14.0	91.0	−135.0
1213	G125	−6489.0	14.0	226.0	135.0
1214	G123	−6503.0	14.0	91.0	−135.0
1215	G121	−6517.0	14.0	226.0	135.0
1216	G119	−6531.0	14.0	91.0	−135.0
1217	G117	−6545.0	14.0	226.0	135.0
1218	G115	−6559.0	14.0	91.0	−135.0
1219	G113	−6573.0	14.0	226.0	135.0
1220	G111	−6587.0	14.0	91.0	−135.0
1221	G109	−6601.0	14.0	226.0	135.0
1222	G107	−6615.0	14.0	91.0	−135.0
1223	G105	−6629.0	14.0	226.0	135.0
1224	G103	−6643.0	14.0	91.0	−135.0
1225	G101	−6657.0	14.0	226.0	135.0
1226	G99	−6671.0	14.0	91.0	−135.0
1227	G97	−6685.0	14.0	226.0	135.0
1228	G95	−6699.0	14.0	91.0	−135.0
1229	G93	−6713.0	14.0	226.0	135.0
1230	G91	−6727.0	14.0	91.0	−135.0
1231	G89	−6741.0	14.0	226.0	135.0
1232	G87	−6755.0	14.0	91.0	−135.0
1233	G85	−6769.0	14.0	226.0	135.0
1234	G83	−6783.0	14.0	91.0	−135.0
1235	G81	−6797.0	14.0	226.0	135.0
1236	G79	−6811.0	14.0	91.0	−135.0
1237	G77	−6825.0	14.0	226.0	135.0
1238	G75	−6839.0	14.0	91.0	−135.0
1239	G73	−6853.0	14.0	226.0	135.0
1240	G71	−6867.0	14.0	91.0	−135.0
1241	G69	−6881.0	14.0	226.0	135.0
1242	G67	−6895.0	14.0	91.0	−135.0
1243	G65	−6909.0	14.0	226.0	135.0
1244	G63	−6923.0	14.0	91.0	−135.0
1245	G61	−6937.0	14.0	226.0	135.0
1246	G59	−6951.0	14.0	91.0	−135.0
1247	G57	−6965.0	14.0	226.0	135.0
1248	G55	−6979.0	14.0	91.0	−135.0
1249	G53	−6993.0	14.0	226.0	135.0
1250	G51	−7007.0	14.0	91.0	−135.0

pad No	pad name	X	ΔX	Y	ΔY
1251	G49	−7021.0	14.0	226.0	135.0
1252	G47	−7035.0	14.0	91.0	−135.0
1253	G45	−7049.0	14.0	226.0	135.0
1254	G43	−7063.0	14.0	91.0	−135.0
1255	G41	−7077.0	14.0	226.0	135.0
1256	G39	−7091.0	14.0	91.0	−135.0
1257	G37	−7105.0	14.0	226.0	135.0
1258	G35	−7119.0	14.0	91.0	−135.0
1259	G33	−7133.0	14.0	226.0	135.0
1260	G31	−7147.0	14.0	91.0	−135.0
1261	G29	−7161.0	14.0	226.0	135.0
1262	G27	−7175.0	14.0	91.0	−135.0
1263	G25	−7189.0	14.0	226.0	135.0
1264	G23	−7203.0	14.0	91.0	−135.0
1265	G21	−7217.0	14.0	226.0	135.0
1266	G19	−7231.0	14.0	91.0	−135.0
1267	G17	−7245.0	14.0	226.0	135.0
1268	G15	−7259.0	14.0	91.0	−135.0
1269	G13	−7273.0	14.0	226.0	135.0
1270	G11	−7287.0	14.0	91.0	−135.0
1271	G9	−7301.0	14.0	226.0	135.0
1272	G7	−7315.0	14.0	91.0	−135.0
1273	G5	−7329.0	14.0	226.0	135.0
1274	G3	−7343.0	14.0	91.0	−135.0
1275	G1	−7357.0	14.0	226.0	135.0
1276	DUMMY	−7371.0	14.0	91.0	−135.0
1277	DUMMY	−7385.0	14.0	226.0	135.0
1278	DUMMY	−7399.0	−	91.0	−

Alignment mark		X	Y
Cross	(1−a)	−7480.0	225.0
	(1−b)	7480.0	225.0

BUMP Arrangement

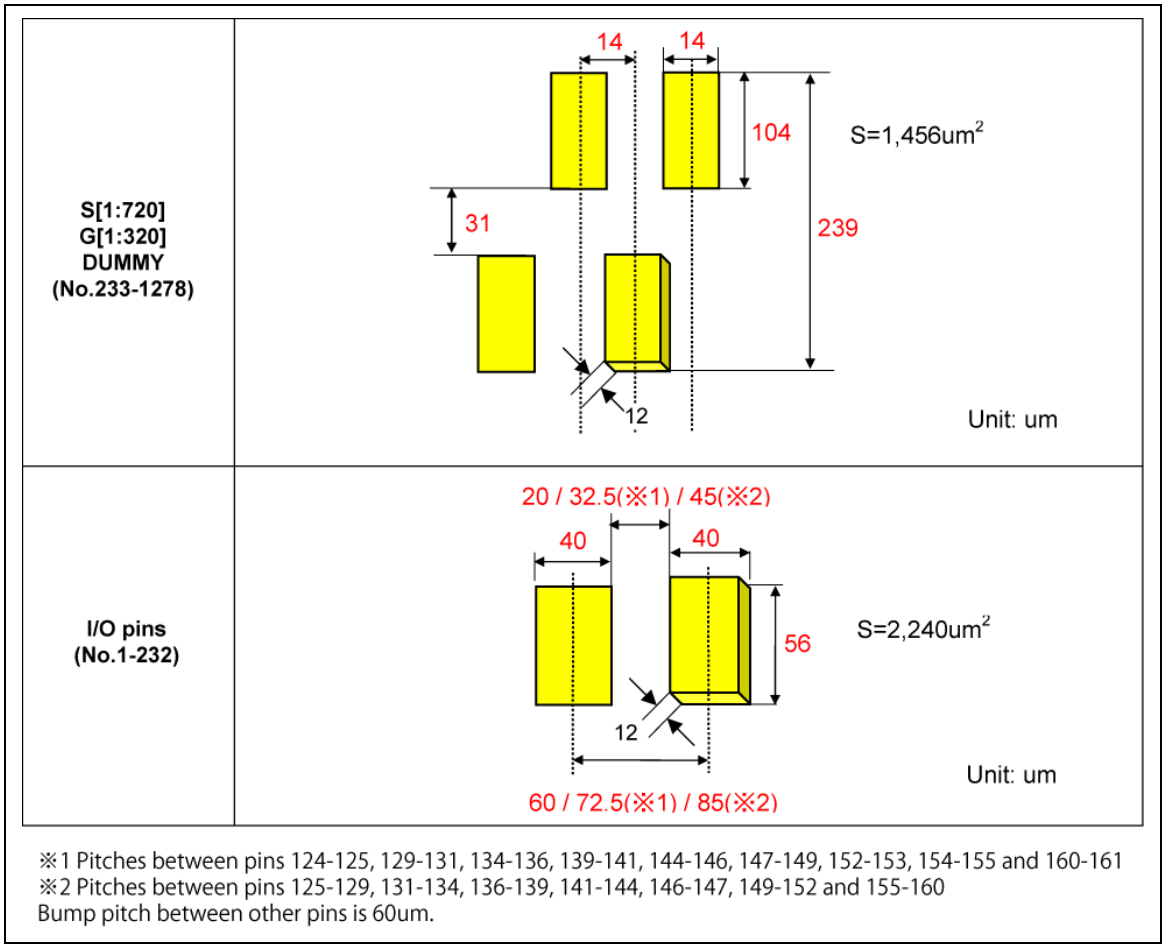


Figure 3

System Interface

From here on, only one function that is related to the interface referred to is mentioned if there is more than two functions assigned to a pin.

DBI Type B

Outline

The R61526 adopts 18-/16-/9-/8-bit bus display command to interface to high-performance host processor. The R61526 starts internal processing after storing control information of externally sent 18-/16-/9-/8-bit data in the command register (CDR) and the parameter register (PR). Since the internal operation of the R61526 is determined by signals sent from the host processor, command/parameter signal, read/write status signal (RDX/WRX), and internal 18-bit data bus signals (DB[17:0]) are called command.

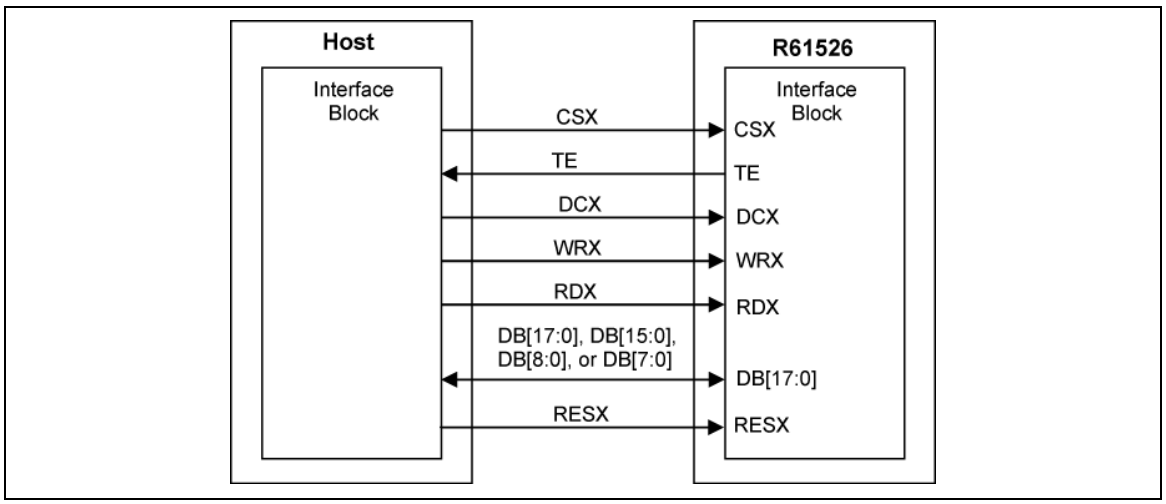


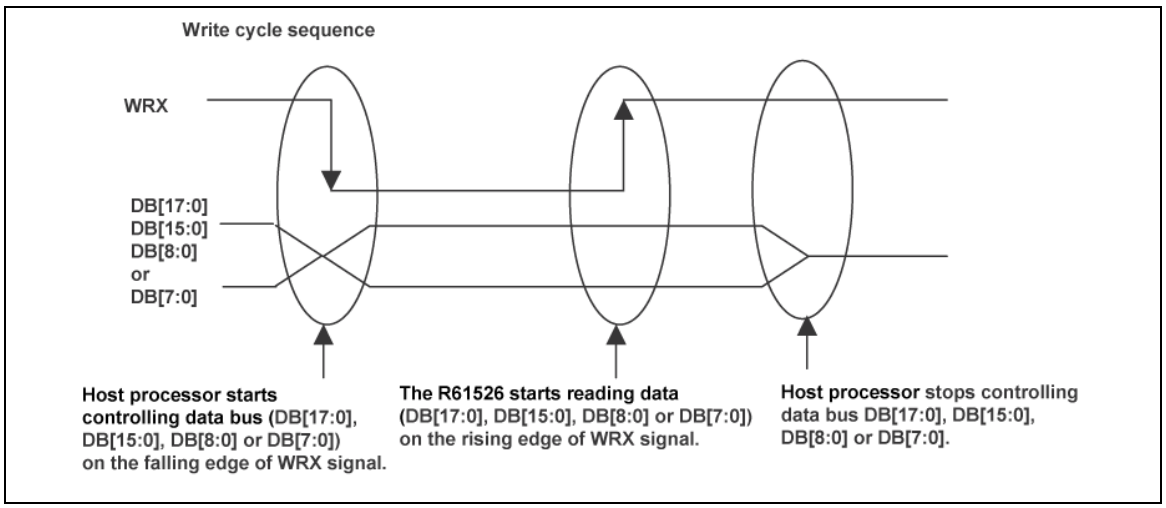
Figure 4 Example: DBI Type B

Write Cycle Sequence

In write cycle, data and/or command are written to the R61526 via the interface between the R61526 and the host processor. Each step of write cycle sequence (WRX high, WRX low, WRX high) comprises three control signals (DCX, RDX, WRX) and 8(DB[7:0]), 9(DB[8:0]), 16(DB[15:0]), or 18(DB[17:0]) bit data. The DCX bit indicates signal that is used to select command or data sent on the data bus.

When DCX="1", data on DB[17:0], DB[15:0], DB[8:0] or DB[7:0] is image data or command parameter. When DCX = 0, data on DB[7:0] is command.

Setting RDX and WRX to "Low" simultaneously is prohibited. See the figure below for the write cycle sequence. G



Note: WRX is not synchronous signal (can be halted).

Figure 5 Write Cycle Sequence

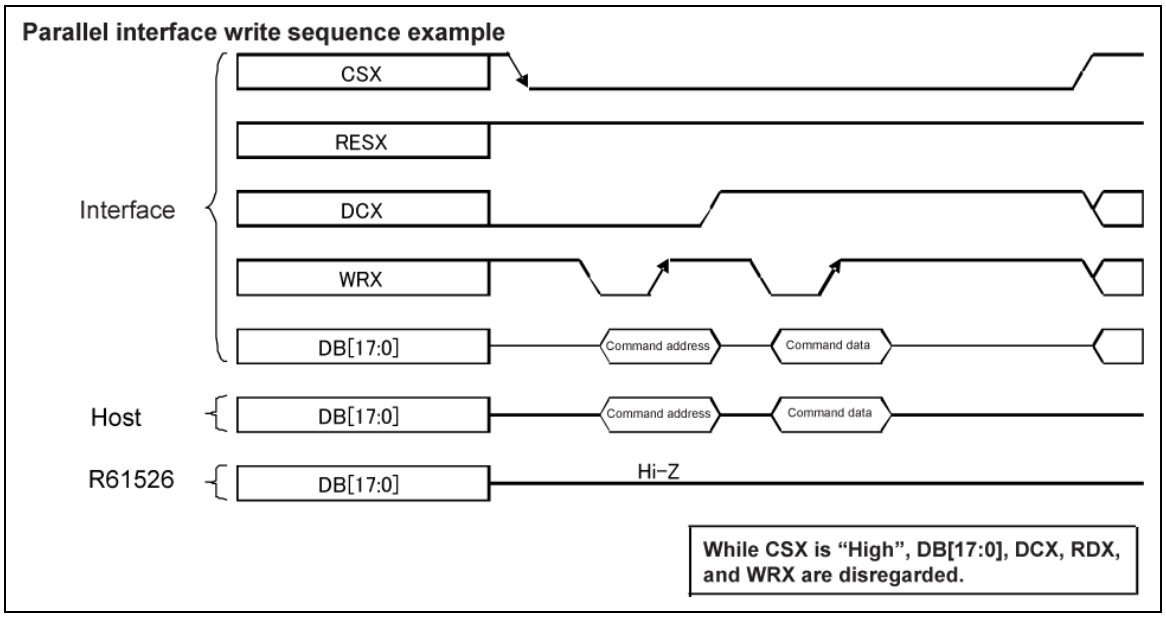
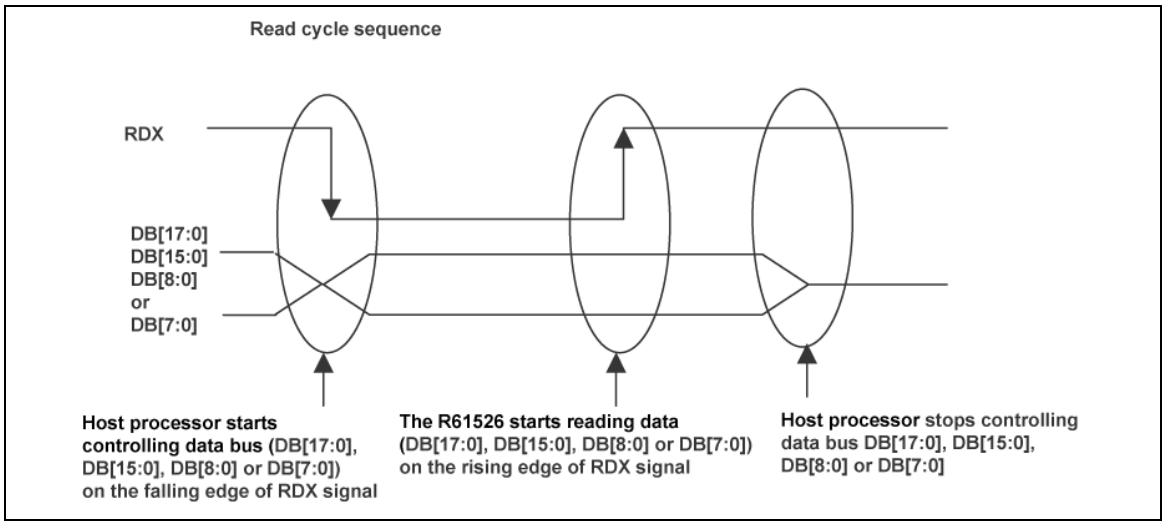


Figure 6

Read Cycle Sequence

In read cycle, data are read from the R61526 via the interface between the R61526 and the host processor. The data (DB[17:0], [15:0], [8:0] or [7:0]) is transmitted from the R61526 to the host processor on the falling edge of RDX. The host processor reads the data on the rising edge of RDX. It is prohibited to set both RDX and WRX low at the same time. See below for the read cycle sequence.



Note: RDX is not synchronous signal (can be halted).

Figure 7 Read Cycle Sequence

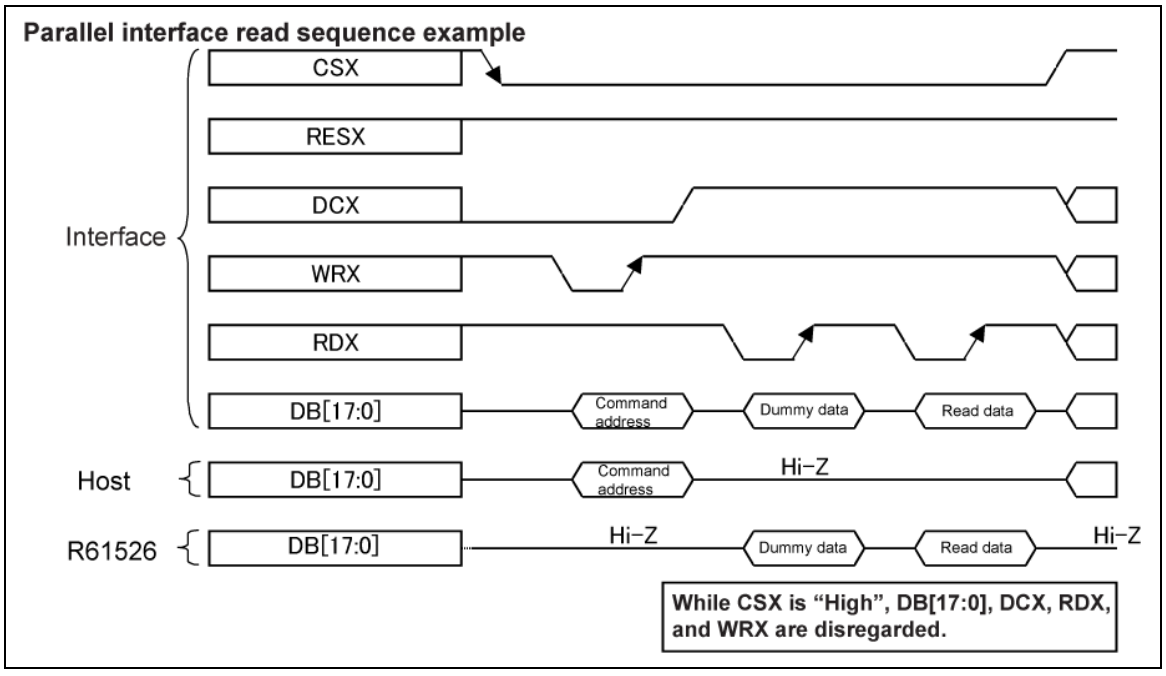


Figure 8

Data Transfer Break

When a break occurs in the transmission of parameter for command from the host processor to the R61526 before the last parameter of the command is sent to the R61526 and the host processor transmits the parameter(s) of a new command rather than the parameters of the interrupted command, the R61526 rejects the parameters of the new command following the break. The command parameters sent to the R61526 before the break occurs are stored in the register of the R61526. However those parameters sent after the break are disregarded, and the data in the register is not overwritten.

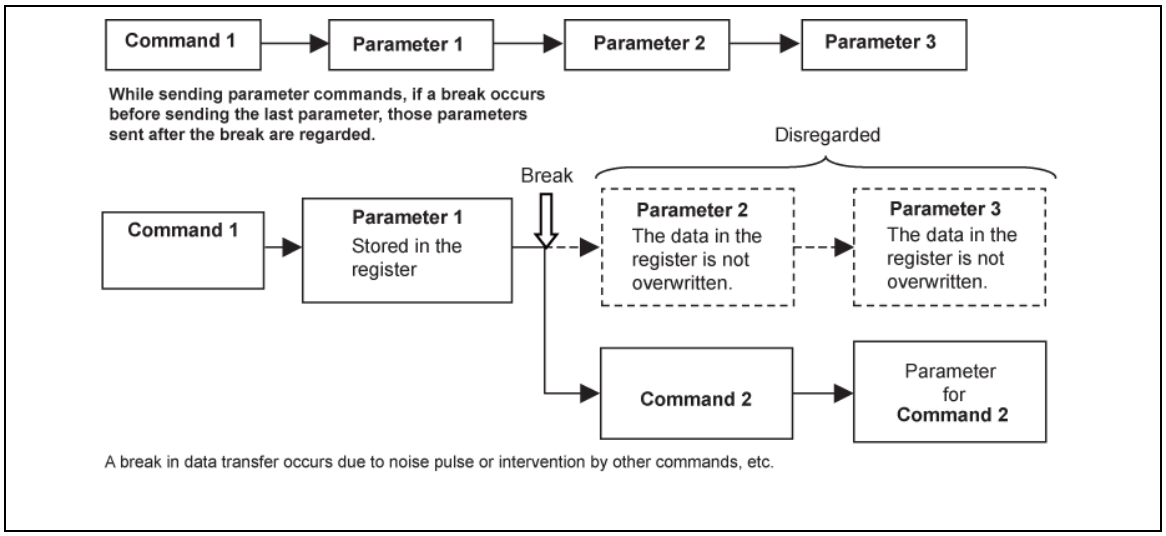


Figure 9

Data Transfer Pause (Command/Pause/Command)

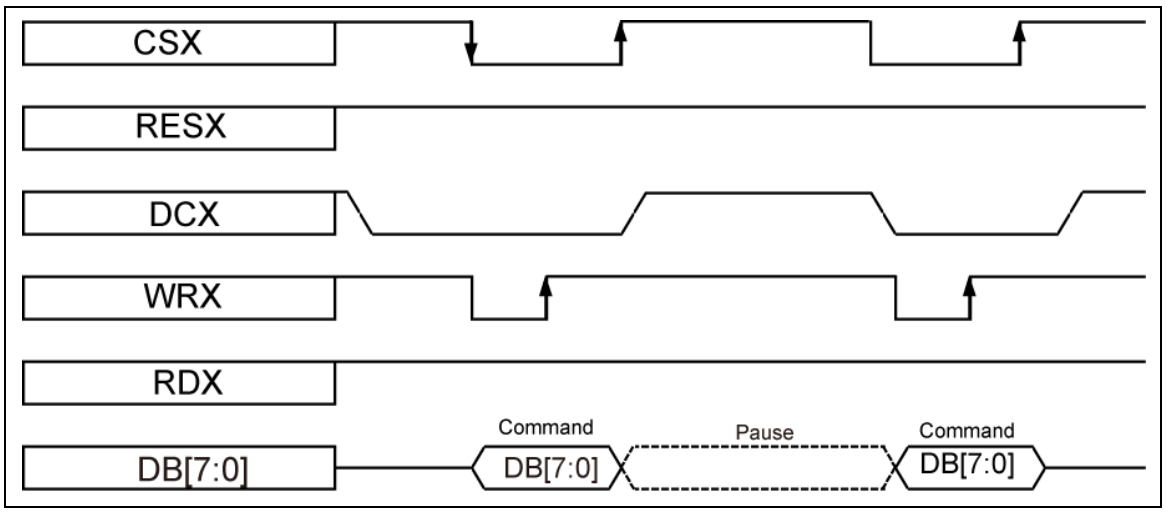


Figure 10

Data Transfer Pause (Command/Pause/Parameter)

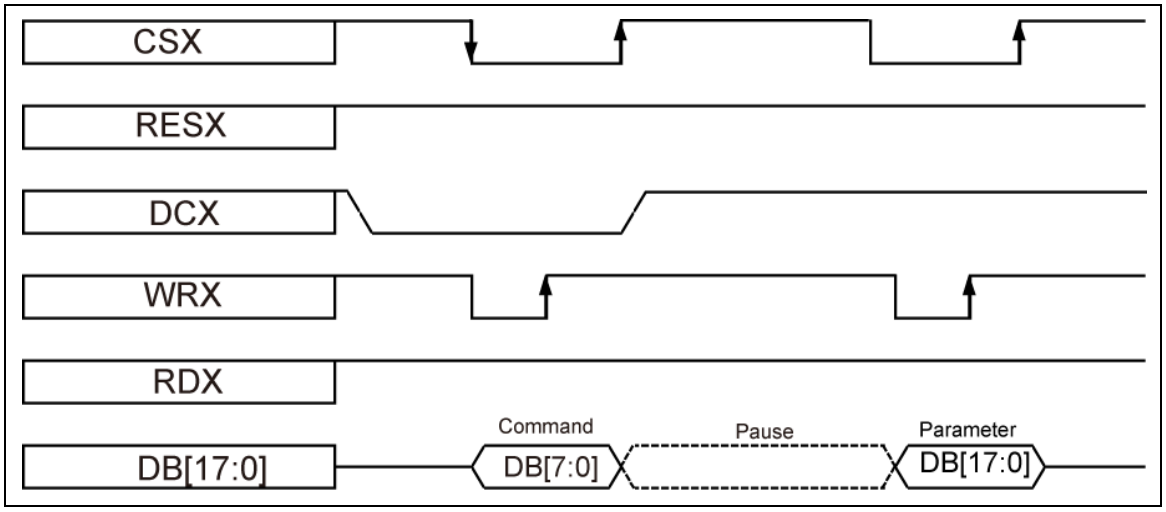


Figure 11

Data Transfer Pause (Parameter/Pause/Command)

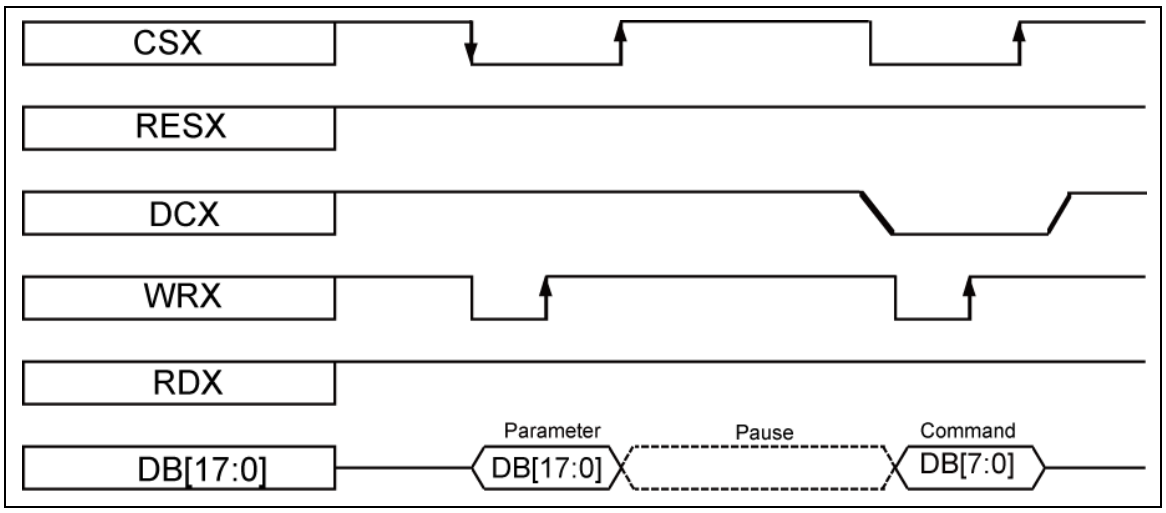


Figure 12

Data Transfer Pause (Parameter/Pause/Parameter)

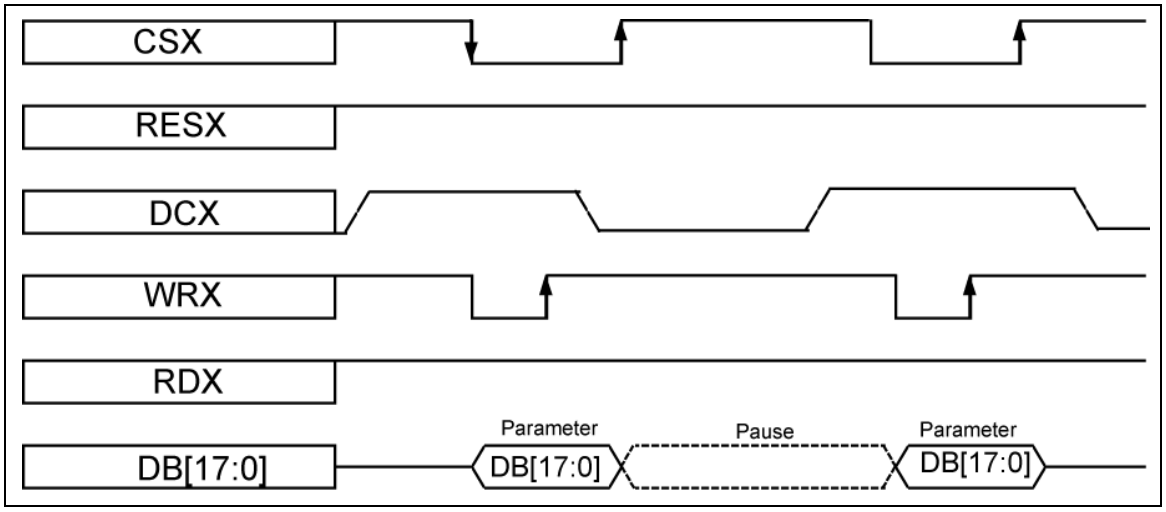


Figure 13

Data Transfer Mode

Two methods are available for writing data to the frame memory in the R61526.

(1) Write Method 1 (Default)

One frame of image data is written to the frame memory. If the amount of data transmitted is more than 1 frame, the data is disregarded. The write operation of the data to the frame memory is terminated when a command intervenes in the middle of the course. The R61526 writes the image data to the next frame when a command to start data write (2Ch) is written. Set WEMODE =0 (Frame Memory Access and Interface setting (B3h)).

Start writing data to the frame memory (2Ch)	Image data for Frame 1	Any command	Start writing data to the frame memory (2Ch)	Image data for Frame 2	Any command

…… Any command

Figure 14

(2) Write Method 2

The image data is written consecutively to the frame memory. The frame memory pointer is reset to the start point when the frame memory becomes full and the driver starts writing the image data of the next frame. Set WEMODE =1 (Frame Memory Access and Interface setting (B3h)).

Start Stop

Start writing data to the frame memory (2Ch)	Image data for Frame 1	Image data for Frame 2	Image data for Frame 3	……	Any command

Figure 15

Notes: 1. Two write methods are available for all data transfer color modes in 18-/ 16-/ 9-/ 8- bit bus display command I/F.
2. The number of pixel in one frame can be odd or even in both download methods. Only complete data sets are retained in the frame memory.
3. The data write operation to the frame memory is terminated when a command intervenes in the middle of the course. In this case, if write_memory_continue (3Ch) is executed, the write operation can be started again from the address where the write operation is halted.

DBI Type C

The R61526 supports serial interface DBI Type C (Options 1 and 3).

Nine / Eight bit data, transmitted from the R61526 to the host processor, is stored in command register (CDR) or parameter register (PR) to start internal operation which is determined by signals from the host processor.

The R61526 does not support “pause” in write and read operations when DBI Type C.

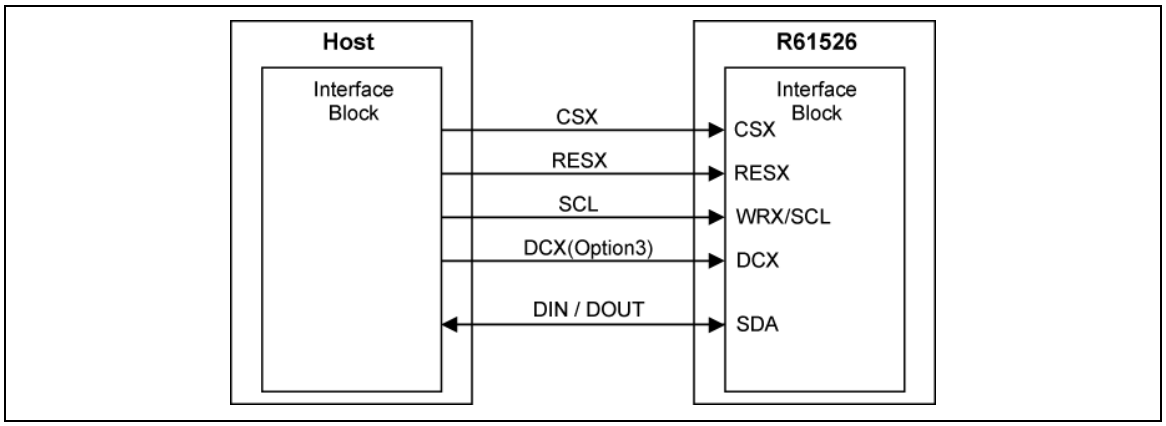
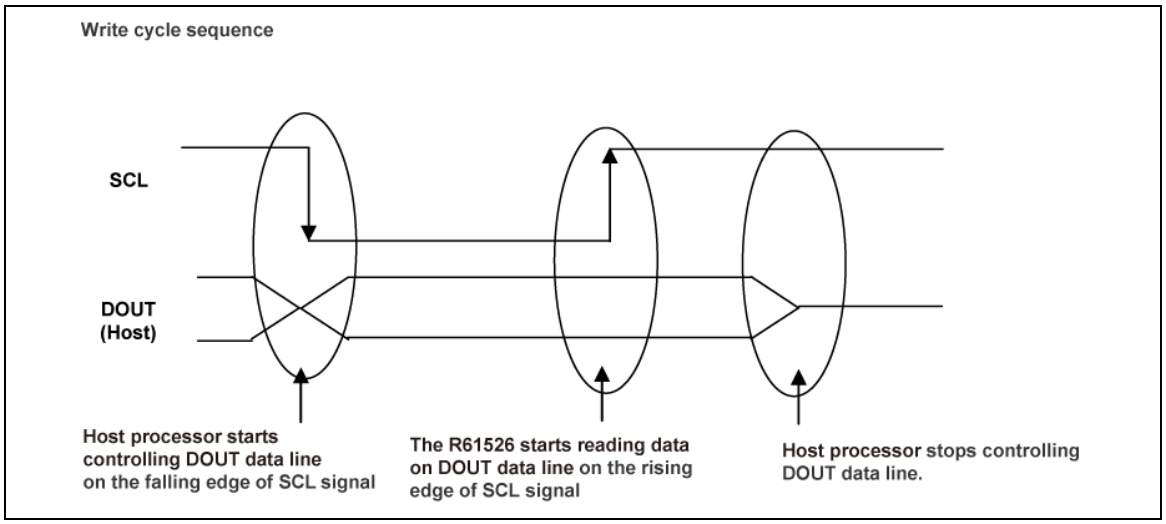


Figure 16 Example: DBI TypeC

Write Cycle Sequence

In write cycle, data and/or command are written to the R61526 via the interface between the R61526 and the host processor. Each step of write cycle sequence (SCL High Low High) has two or three control signals (CSX, SCL, (DCX)) and data output from DOUT. During Write Cycle Sequence, the host processor outputs data while the R61526 accepts data at the rising edge of SCL.

If DCX is used in DBI Type C Option 3 operation, data on DOUT is command when DCX=”0”. When DCX = 1, data on DOUT is image data or command parameter. See next figure for Write Cycle Sequence.



Note: SCL is not synchronous signal (can be halted).

Figure 17 Write Cycle Sequence

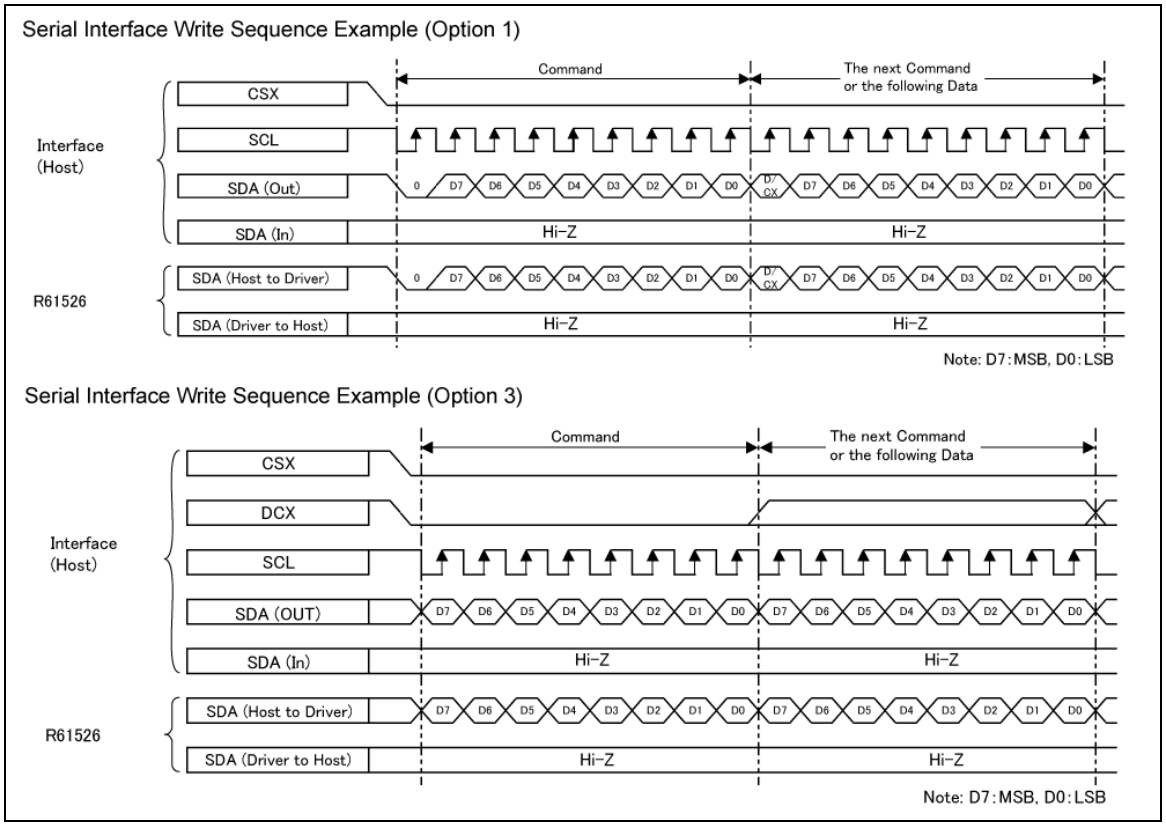
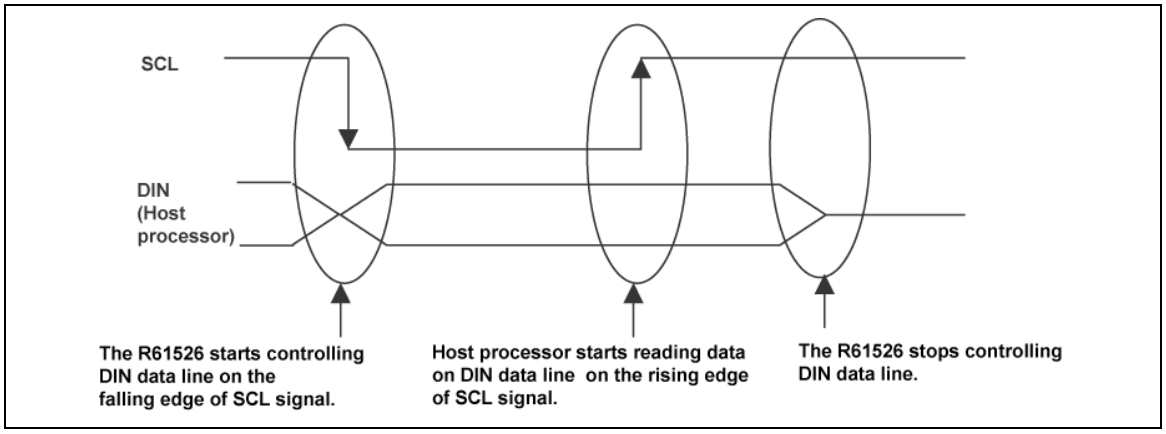


Figure 18 Write Sequence Example (Option 1)

Read Cycle Sequence

In read cycle, data and/or commands are read from the R61526 via the interface between the R61526 and the host processor. Data is transmitted from the R61526 to the host processor via DIN on the falling edge of WRX/SCL. The host processor reads the data on the rising edge of SCL. See next figure for the read cycle sequence.



Note: SCL is not a synchronous signal (can be halted).

Figure 19 Read Cycle Sequence

(2-1) Read Operation by Read Command 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 2Eh, 45h, A1h, and BFh

First byte of read data, after a read command is dummy data regardless of whether it is a parameter or frame memory data.

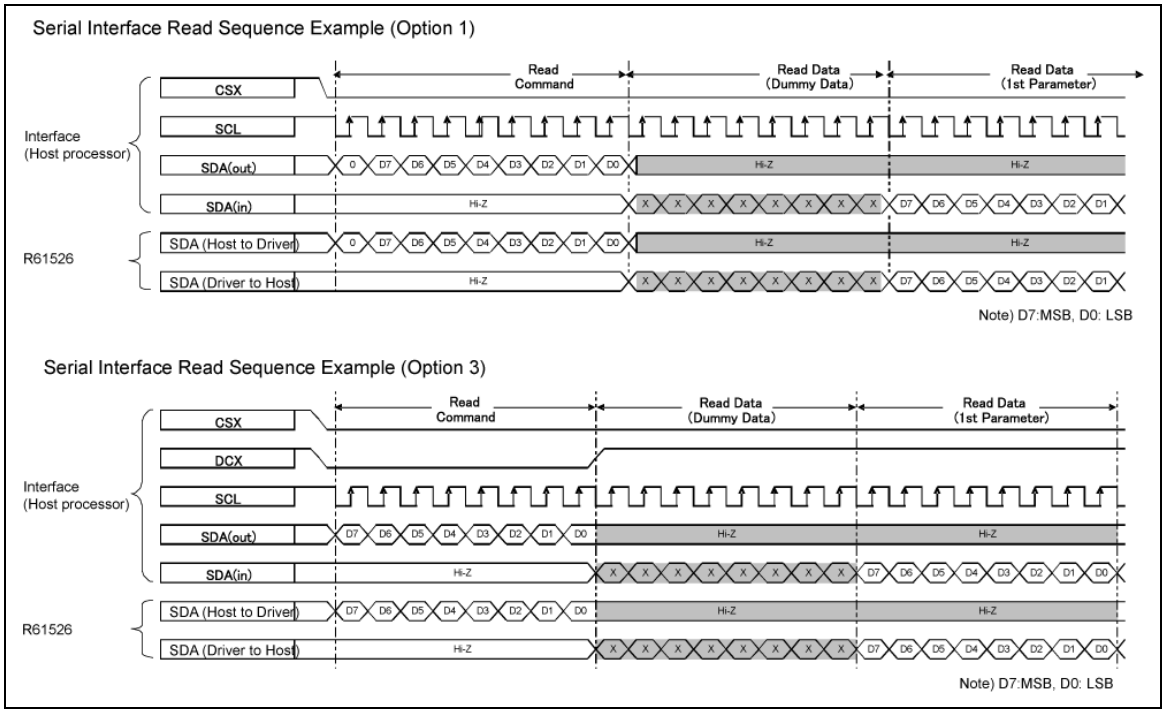


Figure 20 DBI Type C Read Operation by Read Command (Option 1, 3)

(2-2) Read Operation by Read Mode In Command (B0h, B1h, B3h, B4h, C0h, C1h, C3h, C4h, C8h, C9h, CAh, D0h, D1h, D2h, D4h, E0h, E1h, E2h)

The first byte after Read Mode In Command is dummy data.

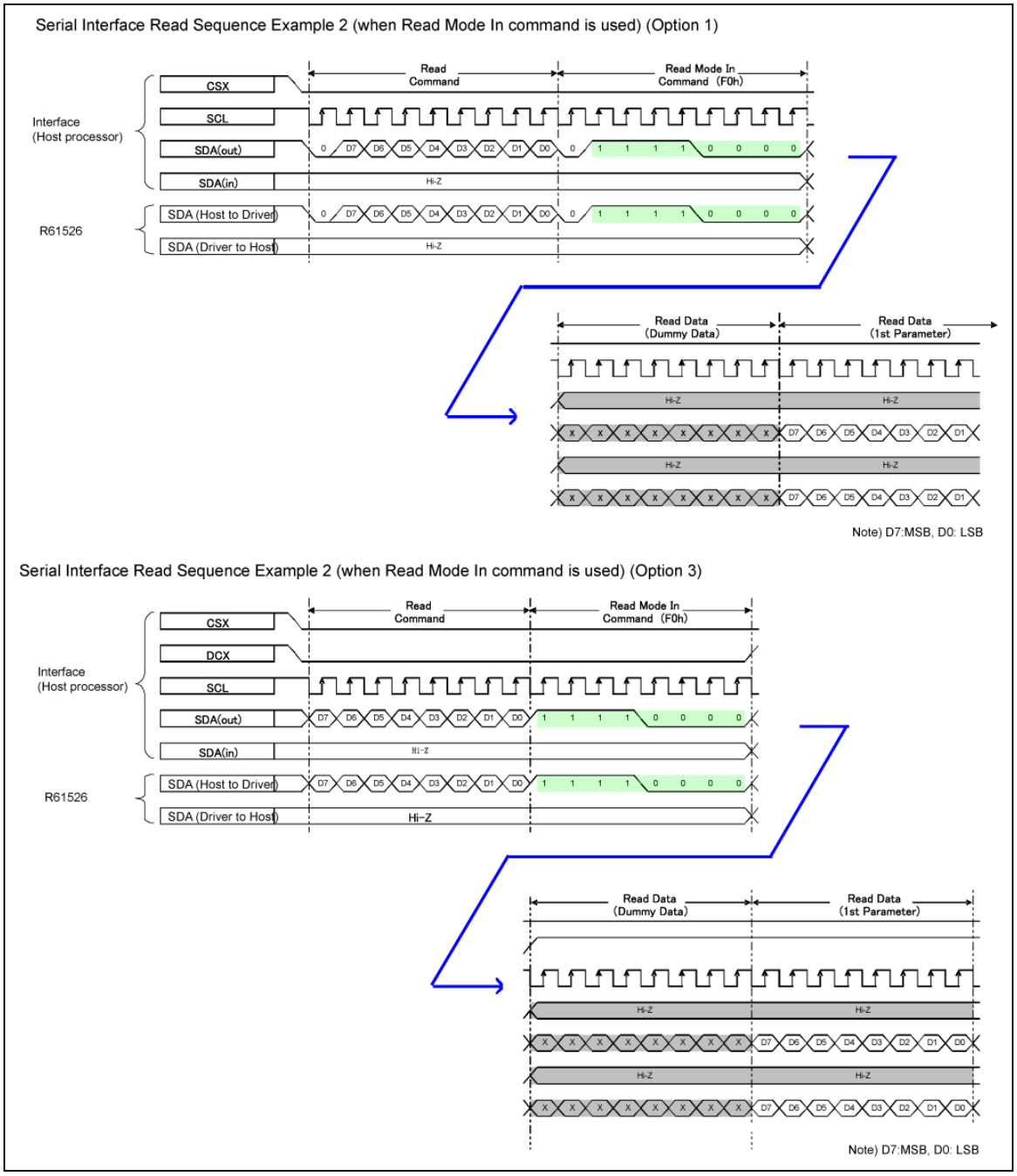


Figure 21 DBI Type C Read Operation by Read Mode In Command

Data Transfer Break

When a break occurs in the transmission of parameter for command from the host processor to the R61526 before the last parameter of the command is sent to the R61526 and the host processor transmits the parameter(s) of a new command rather than the parameters of the interrupted command, the R61526 rejects the parameters of the new command following the break. The command parameters sent to the R61526 before the break occurs are stored in the register of the R61526. However those parameters sent after the break are disregarded, and the data in the register is not overwritten.

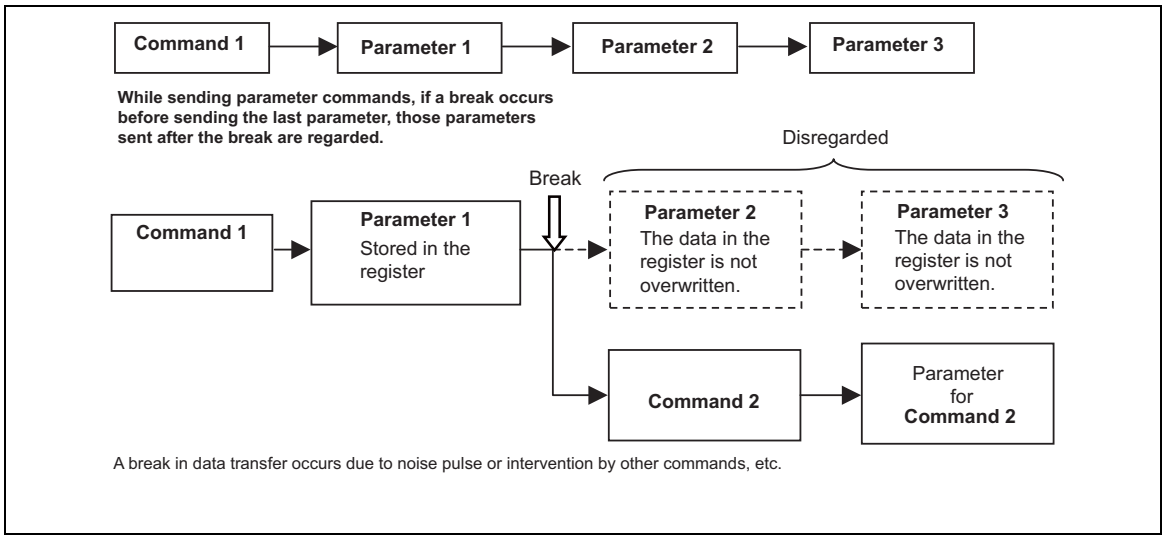


Figure 22

Data Transfer Pause

The R61526 does not support pause during Type C write/read operation.

After transferring command /parameter, if transfer is halt by setting CSX=High, start transfer (CSX=Low) from a command.

DBI Data Format

The R61526 supports color formats shown in the table below. At least one color format is supported by each of Type B 18-/16-/9-/8-bit and Type C interface.

Table 10

Type	IM[0:3]	Data Pin	Color format	MIPI Spec	R61526
MIPI	0011	DB[17:0]	18bpp	Not defined	Yes
Type B	0001	DB[15:0]	8bpp	Yes	No
			12bpp	Yes	No
			16bpp	Yes	Yes
			18bpp (262,144-color Option 1)	Yes	Yes
			18bpp (262,144-color Option 2)	Yes	Yes
			24bpp (16,776,216-color Option 1)	Yes	No
			24bpp (16,776,216-color Option 2)	Yes	No
	0010	DB[8:0]	18bpp	Yes	Yes
	0000 1111	DB[7:0]	8bpp	Yes	No
			12bpp	Yes	No
			16bpp	Yes	Yes
			18bpp	Yes	Yes
			24bpp	Yes	No
MIPI	0101	SDA	3bpp (8-color Option 1)	Yes	Yes
Type C			3bpp (8-color Option 2)	Yes	Yes
			18bpp	Not defined	Yes
	0110	SDA	3bpp (8-color Option 1)	Yes	Yes
			3bpp (8-color Option 2)	Yes	Yes
			18bpp	Not defined	Yes

Yes: Supported.
No: Not supported.

■DBI Type B Data Format

●Data Format for 18-Bit Interface (DB[17:0] is used)

	set_pixel_format	DFM	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*											D7	D6	D5	D4	D3	D2	D1	D0
Command Parameter Read	*	*											D7	D6	D5	D4	D3	D2	D1	D0

	set_pixel_format	DFM	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

●Pin Connection for 16-Bit Bus Interface (DB[15:0] is used)

	set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*									D7	D6	D5	D4	D3	D2	D1	D0
Command Parameter Read	*	*									D7	D6	D5	D4	D3	D2	D1	D0

			First Transmission																Second Transmission														Third Transmission													
	set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	*	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]																																		
18bpp Frame Memory Write	3'h6	0	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]			G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]			B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]			R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]			G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]			B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]		
		1									R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]																		
18bpp Frame Memory Read	*	0	r1[5]	r1[4]	r1[3]	r1[2]	r1[1]	r1[0]			g1[5]	g1[4]	g1[3]	g1[2]	g1[1]	g1[0]			b1[5]	b1[4]	b1[3]	b1[2]	b1[1]	b1[0]			r2[5]	r2[4]	r2[3]	r2[2]	r2[1]	r2[0]			g2[5]	g2[4]	g2[3]	g2[2]	g2[1]	g2[0]			b2[5]	b2[4]	b2[3]	b2[2]	b2[1]	b2[0]		
		1									r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]																		

●Data Format for 9-Bit Interface (DB[17:0] is used)

	set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*		D7	D6	D5	D4	D3	D2	D1	D0
Command Parameter Read	*	*		D7	D6	D5	D4	D3	D2	D1	D0

			First Transmission									Second Transmission								
	set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

●Data Format for 8-Bit Interface (DB[7:0] is used)

	set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*	D7	D6	D5	D4	D3	D2	D1	D0
Command Parameter Read	*	*	D7	D6	D5	D4	D3	D2	D1	D0

			First Transmission								Second Transmission								Third Transmission							
	set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	*	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]								
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]		

●Extended Format for 18bpp Data

		Frame Memory Data (18bpp)																
set_pixel_format	EPF	r5	r4	r3	r2	r1	r0	g5	g4	g3	g2	g1	g0	b5	b4	b3	b2	b1	b0
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
16bpp	2'h0	R[4]	R[3]	R[2]	R[1]	R[0]	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	0
	2'h1	R[4]	R[3]	R[2]	R[1]	R[0]	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	1
	2'h2	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]

R[4:0], B[4:0] = 5'h1F → r[5:0], b[5:0] = 6'h3F
R[4:0], B[4:0] = 5'h00 → r[5:0], b[5:0] = 6'h00

Note 1: The first Command Parameter Read and Frame Memory Read after read command is issued is invalid (dummy read).
Note 2: Data are written to the Frame Memory when data for one pixel are input. In 2-pixel 3- transfer operation (16-bit I/F 18bpp Option1), the first and second pixels are written in the 2nd and 3rd transfers respectively.
Note 3: If data transfer stops after 2nd transfer in 2-pixel 3-transfer operation, the first pixel data are written normally. This applies to the last address when number of pixel is odd according to window setting.
Note 4: This page shows example with BGR=0. If BGR=1, allocation of R and B in the frame memory is swapped.

BGR Register Setting and Write/Read Data in Frame Memory

System interface outputs write and read data in the same RGB order regardless of BGR register setting.

Example: 18-Bit Interface

●BGR=0

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Write data	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

↓

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Frame memory	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

↓

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Read data	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

●BGR=1

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Write data	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

↓

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Frame memory	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]

↓

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Read data	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

■DBI Type C Data Format

●Data Format for Serial Interface Option1/Option3

	set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*	D7	D6	D5	D4	D3	D2	D1	D0
Command Parameter Read	*	*	D7	D6	D5	D4	D3	D2	D1	D0

			First Transmission								Second Transmission								Third Transmission							
	set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
3bpp Frame Memory Write	3'h1	0			R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]																
		1		R1[0]	G1[0]	B1[0]		R2[0]	G2[0]	B2[0]																
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]		

●Extended Format for 18 bpp Data

		Frame Memory Data (18bpp)																	
set_pixel_format	EPF	r5	r4	r3	r2	r1	r0	g5	g4	g3	g2	g1	g0	b5	b4	b3	b2	b1	b0
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
3pbb	*	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	G[0]	G[0]	G[0]	G[0]	G[0]	G[0]	B[0]	B[0]	B[0]	B[0]	B[0]	B[0]

Note 1: The first Command Parameter Read and Frame Memory Read after read command issued are invalid (dummy read).
Note 2: This page shows example with BGR=0. If BGR=1, allocation of R and B in the frame memory are swapped.

Display Pixel Interface (DPI)

Display Pixel Interface (DPI)

In Display Pixel Interface (DPI) operation, display operation is in synchronization with synchronization signals VSYNC, HSYNC and DOTCLK (PCLK). If window address function and frame memory rewrite cycle setting are used together, the data is transferred only to the video image area so that the R61526 consumes only a small amount of power according to a frequency of rewrite operation. Front and back porch periods must be made before and after the display period. In DPI operation, commands must be transferred via DBI Type C serial interface. DPI and DBI Type B cannot be used simultaneously.

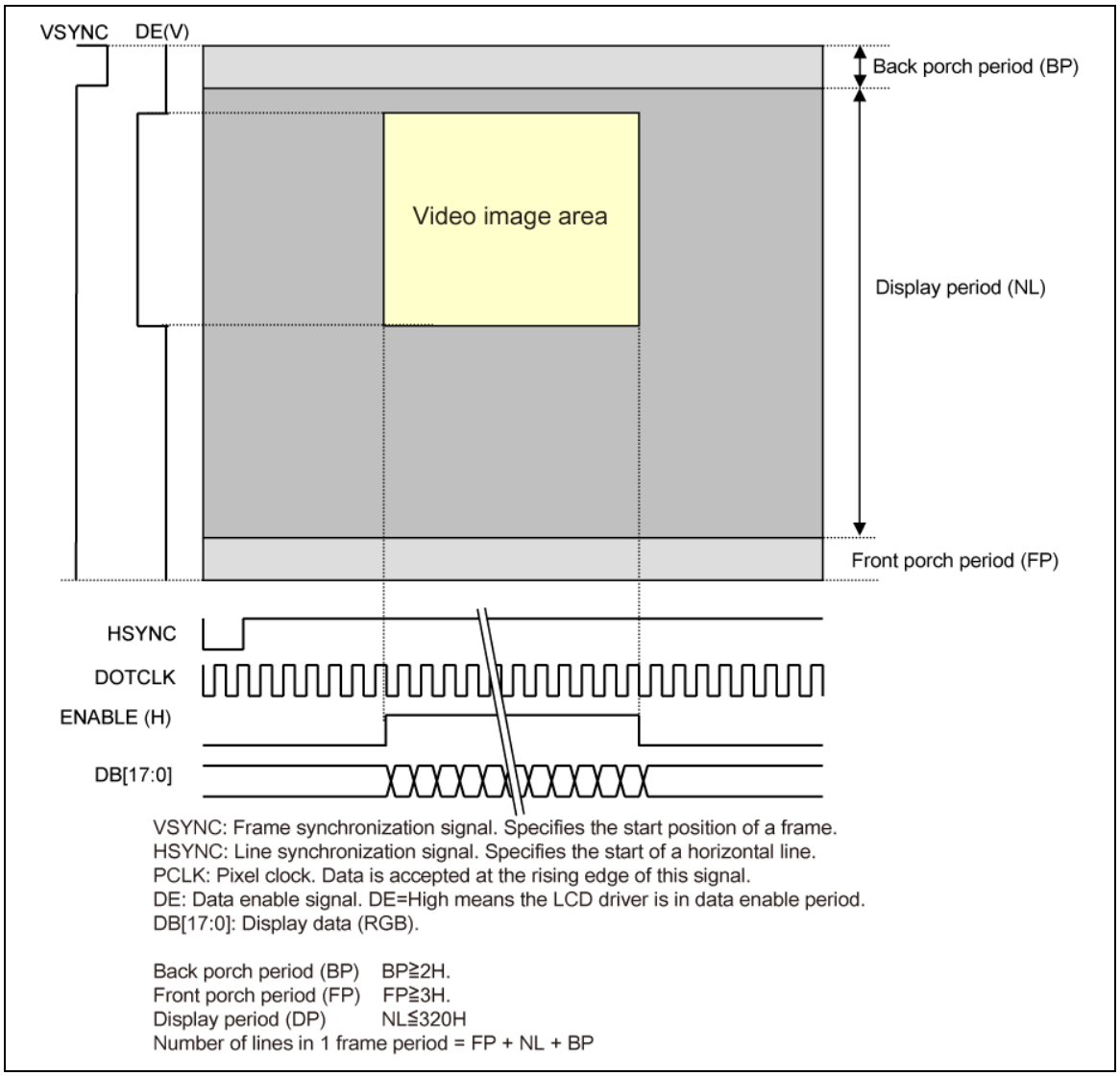


Figure 23

DPI Timing

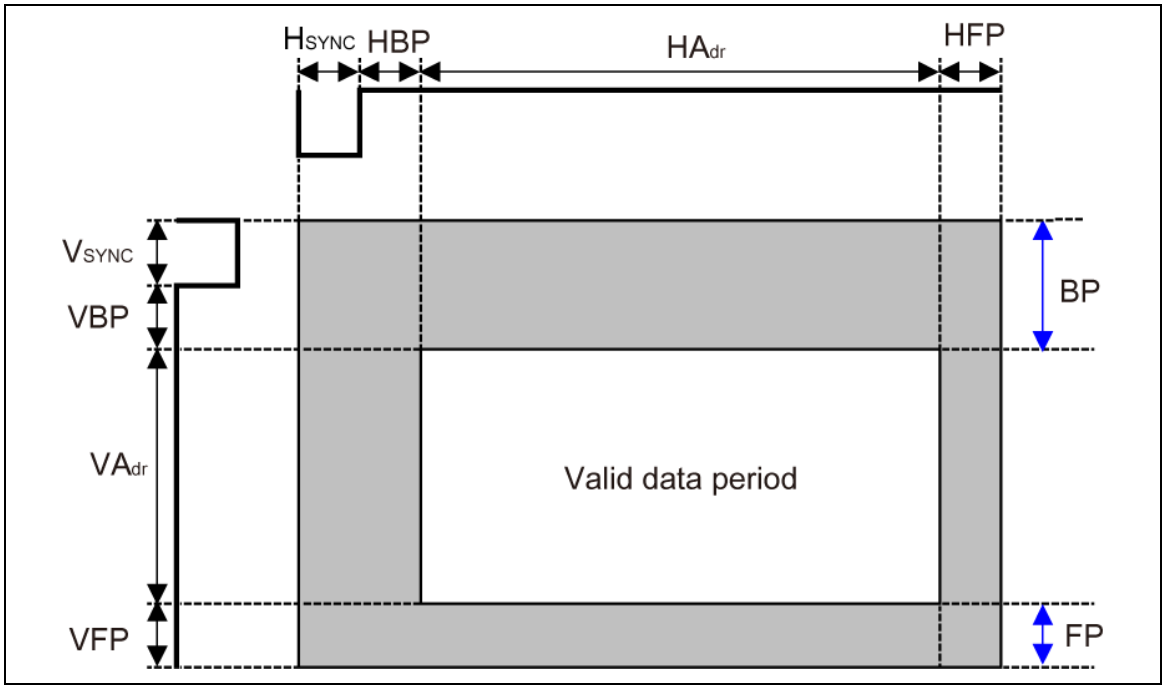


Figure 24

Table 11

Parameters	Symbols	Min.	Typ.	Max.	Step	Unit
Horizontal Synchronization	Hsync	2	10	16	1	PCLKCYC
Horizontal Back Porch	HBP	2	20	24	1	PCLKCYC
Horizontal Address	HAdr	–	240	–	1	PCLKCYC
Horizontal Front Porch	HFP	2	10	16	1	PCLKCYC
Vertical Synchronization	Vsync	1	2	4	1	Line
Vertical Back Porch	VBP	1	2	–	1	Line
Vertical Address	VAdr	–	320	–	1	Line
Vertical Front Porch	VFP	3	4	–	1	Line

Typical values are setting example when used with panel resolution QVGA (240 x 320), clock frequency 5.65MHz and frame frequency about 60Hz.

Note: Make sure that Vsync+VBP = BP, VFP = FP and VAdr＝line number specified by NL.

Also make sure that
(Number of DOTCLK per 1 line) ≥ (Number of RTN clock) × (PCDIVL+PCDIVH)

Video Image Display via DPI

The R61526 supports video image capable DPI and frame memory to store display data so that the driver has strong points such as

1. Window address function enabling data transfer for only video image area.
2. Data only for video image display area can be transferred.
3. Reduced amount of data transfer enables low power consumption operation as the system as a whole.
4. Still picture area (icon mark, etc.) is rewritten even in video image display period by using system interface together with DPI.

To access Frame Memory via System Interface (DBI) in DPI operation

Frame memory can be accessed via system interface in DPI operation as well. However in DPI operation, the frame memory is always written in synchronization with DOTCLK when ENABLE=”High”. Therefore, make sure to stop display data write operation via DPI by setting ENABLE = “Low” to write data to frame memory via system interface. If RM=0, the frame memory is accessed via system interface. To return to DPI operation, make write/read bus cycle time and then set RM=1 and execute a write_memory_start command (2Ch) and then start frame memory access. If both interfaces are used to access the frame memory, write data is not guaranteed.

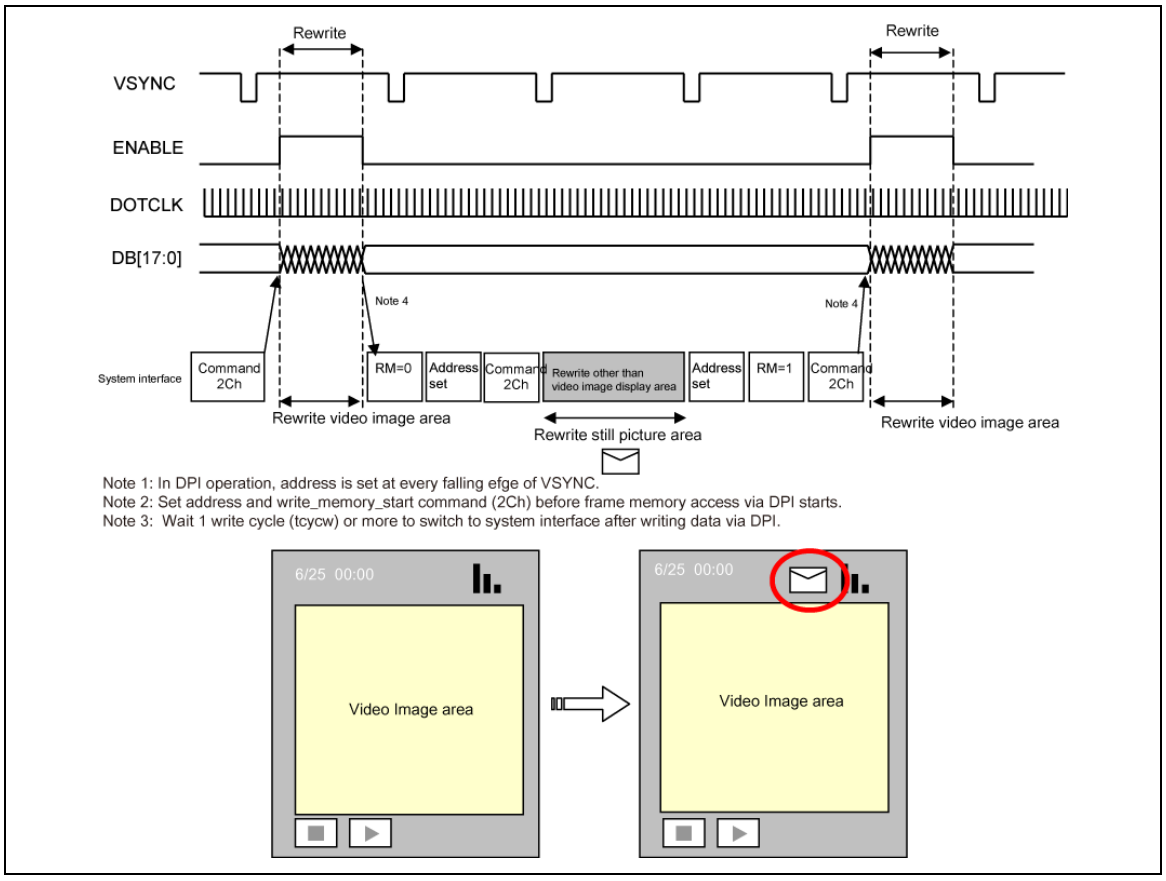


Figure 25

DPI

16-Bit DPI

16-bit DPI can be used when set_pixel_format (3Ah) D[6:4]=3'h5.

Images are displayed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. Data transfer to internal frame memory is in synchronization with display operation. 16-bit RGB data (DB[15:0]) and data enable signal (ENABLE) are used.

Only system interface (DBI Type C) can be used to set commands.

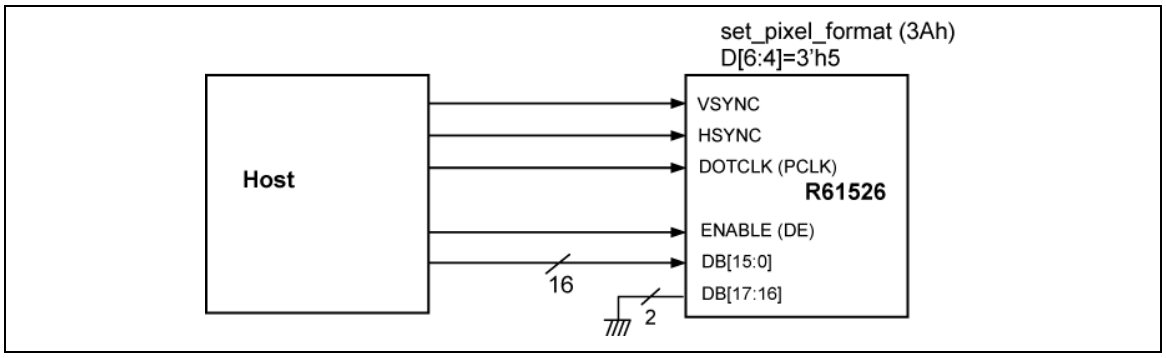


Figure 26 Example

18-Bit DPI

18-bit DPI can be used when set_pixel_format (3Ah) D[6:4]=3'h6.

Images are displayed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK.

Data transfer to internal frame memory is in synchronization with display operation. 18-bit RGB data (DB[17:0]) and data enable signal (ENABLE) are used.

Only system interface (DBI Type C) can be used to set commands.

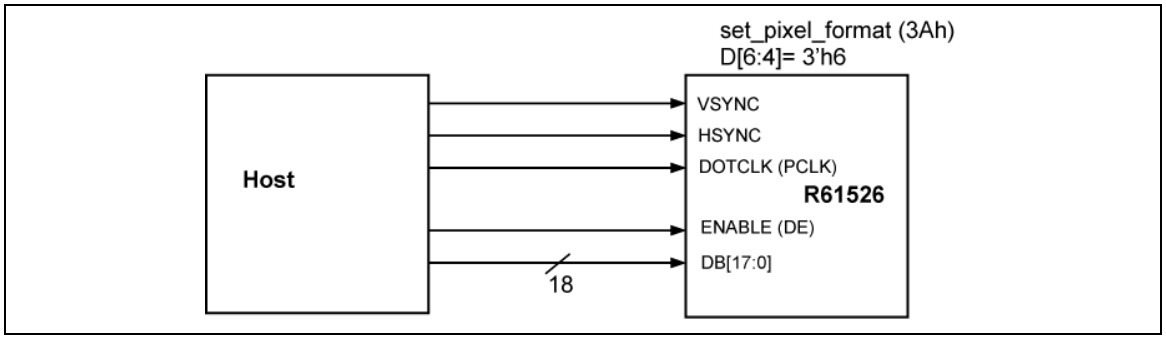


Figure 27 Example

Notes to Usage of DPI

a. In DPI operation, functions noted “disabled” in the table below are invalid.

Table 12

Function	External Display Interface	Internal Display Operation
Partial Display Function	Disabled	Enabled
Idle Mode	Disabled	Enabled

b. It is necessary to supply VSYNC, HSYNC and PCLK all the time during DPI operation.

c. Panel control signal reference clock is PCLK in DPI operation, not usual internal oscillation clock.

d. Make sure to follow “Internal Clock Operation Transition Sequence” in switching sequence to transit from/to display by internal operation mode to/from display via DPI.

e. Address is set every frame on the falling edge of VSYNC during DPI operation.

f. Make sure that ENABLE = Low, when commands are input via DBI TypeC.

DPI Data Format

The R61526 supports color formats as below:

Table 13

set_pixel_format (3Ah) D[6:4]	Data pin	Color format	MIPI Spec.	R61526
—	—	24bpp	Yes	No
3’h6	DB[17:0]	18bpp	Yes	Yes
3’h5	DB[15:0]	16bpp	Yes	Yes

Yes: Supported
No: Unsupported

See next figure for connection of host professor and the R61526’s pins.

■DPI Data Format

●Pin Connection for 18-Bit Interface (DB[17:0] is used. set pixel format D[6:4]=3'h6. 18bpp)

Configuration1

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
R61526 pin							DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Configuration2

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			R5	R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0			B5	B4	B3	B2	B1	B0
R61526 pin			DB17	DB16	DB15	DB14	DB13	DB12			DB11	DB10	DB9	DB8	DB7	DB6			DB5	DB4	DB3	DB2	DB1	DB0
			R5	R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0			B5	B4	B3	B2	B1	B0

●Pin Connection for 16-Bit Interface (DB[15:0] is used. set pixel format D[6:4]=3'h5. 16bpp)

Configuration1

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
									R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
R61526 pin									DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
									R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Configuration2

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0				B4	B3	B2	B1	B0
R61526 pin				DB15	DB14	DB13	DB12	DB11			DB10	DB9	DB8	DB7	DB6	DB5				DB4	DB3	DB2	DB1	DB0
				R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0				B4	B3	B2	B1	B0

Configuration3

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			R4	R3	R2	R1	R0				G5	G4	G3	G2	G1	G0			B4	B3	B2	B1	B0	
R61526 pin			DB15	DB14	DB13	DB12	DB11				DB10	DB9	DB8	DB7	DB6	DB5			DB4	DB3	DB2	DB1	DB0	
			R4	R3	R2	R1	R0				G5	G4	G3	G2	G1	G0			B4	B3	B2	B1	B0	

●Extended Format for 18 bpp Data

		Frame Memory Data (18bpp)																		
set_pixel_format	EPF	r5	r4	r3	r2	r1	r0	g5	g4	g3	g2	g1	g0	b5	b4	b3	b2	b1	b0
18bpp	*	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16bpp	2'h0	R4	R3	R2	R1	R0	0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0
	2'h1	R4	R3	R2	R1	R0	1	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1
	2'h2	R4	R3	R2	R1	R0	R4	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	B4

R[4:0], B[4:0] = 5'h1F → r[5:0], b[5:0] = 6'h3F
R[4:0], B[4:0] = 5'h00 → r[5:0], b[5:0] = 6'h00

Note: This page shows example with BGR=0. If BGR=1, allocation of R and B in the frame memory is swapped.

Command Description

Table 14 User Command

Operational Code (Hex)	Command	Command (C) /Read(R) /Write(W)	Number Of Parameter	MIPI DCS Type1 Requirement	R61526 Implementation	Note
00h	nop	C	0	Yes	Yes	
01h	soft_reset	C	0	Yes	Yes	
04h	Read Display Identification Information	R	3	No	Yes	
0Ah	get_power_mode	R	1	Yes	Yes	
0Bh	get_address_mode	R	1	Yes (Bits [7:0])	Yes (Bits 7/6/5/4/0 Only)	
0Ch	get_pixel_format	R	1	Yes	Yes	
0Dh	get_display_mode	R	1	Yes	Yes	
0Eh	get_signal_mode	R	1	Yes	Yes	
0Fh	get_diagnostic _result	R	1	Bits 7/6: Yes Bits 5/4: Optional	Yes (Bits 7/6 Only)	
10h	enter_sleep_mode	C	0	Yes	Yes	
11h	exit_sleep_mode	C	0	Yes	Yes	
12h	enter_partial_mode	C	0	Yes	Yes	
13h	enter_normal_ mode	C	0	Yes	Yes	
28h	set_display_off	C	0	Yes	Yes	
29h	set_display_on	C	0	Yes	Yes	
2Ah	set_column_ address	W	4	Yes	Yes	
2Bh	set_page_address	W	4	Yes	Yes	

Table 15 User Command (continued)

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter	MIPI DCS Type1 Requirement	R61526 Implementation	Note
2Ch	write_memory_start	W	Variable	Yes	Yes	Note 1
2Dh	write_LUT	W	Variable	Optional	No	
2Eh	read_memory_start	R	Variable	Yes	Yes	Note 1
30h	set_partial_area	W	4	Yes	Yes	
33h	set_scroll_area	W	6	Yes	No	
34h	set_tear_off	C	0	Yes	Yes	
35h	set_tear_on	W	1	Yes	Yes	
36h	set_address_mode	W	1	Yes (Bits [7:0])	Yes (Bits 7/6/5/4/0 Only)	
37h	set_scroll_start	W	2	Yes	No	
38h	exit_idle_mode	C	0	Yes	Yes	
39h	enter_idle_mode	C	0	Yes	Yes	
3Ah	set_pixel_format	W	1	Yes	Yes	
3Ch	write_memory _continue	W	Variable	Yes	Yes	Note 1
3Eh	read_memory _continue	R	Variable	Yes	Yes	Note 1
44h	set_tear_scanline	W	2	Yes	Yes	
45h	get_scanline	R	2	Yes	Yes	

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter	MIPI DCS Type1 Requirement	R61526 Implementation	Note
51h	Write_ Display_ Brightness	W	1	No	Yes	
52h	Read_Display_ Brightness_Value	R	2	No	Yes	
53h	Write_ Control_Display	W	1	No	Yes	
54h	Read_CTRL_ Value_ Display	R	2	No	Yes	
55h	Write_Content_ Adaptive_Brightness_ Control	W	1	No	Yes	
56h	Read_Content_ Adaptive_Brightness_ Control	R	2	No	Yes	
68h	Read_Automatic_ Brightness_Control_ Self-Diagnostic_Result	R	1	No	Yes	
A1h	read_DDB_start	R	3	Yes	Yes	

Note 1: See “DBI Data Format” and “DPI Data Format” for Frame Memory write/read formats.

Table 16 Manufacturer Command

Operational Code (Hex)	Function	Command (C) /Read(R) /Write(W)	Number Of Parameter	Category
B0h	Manufacturer Command Access Protect	W / R	2	Additional User Command
B1h	Low Power Mode Control	W / R	1	Additional User Command
B3h	Frame Memory Access and Interface Setting	W / R	5	Additional User Command
B4h	Display Mode and Frame Memory Write Mode Setting	W / R	1	Additional User Command
BFh	Device code Read	R	5	
C0h	Panel Driving Setting	W / R	8	
C1h	Display Timing Setting for Normal / Partial Mode	W / R	5	
C3h	Display Timing Setting for Idle Mode	W / R	5	
C4h	Source/VCOM/Gate Driving Timing Setting	W / R	5	
C8h ~ CAh	Gamma Set A ~ C	W	22	
D0h	Power Setting (Common Setting)	W / R	6	
D1h	VCOM Setting	W / R	3	
D2h	Power Setting for Normal / Partial Mode	W / R	2	
D4h	Power Setting for Idle Mode	W / R	2	
E0h	NVM Access Control	W / R	3	
E1h	set_DDB_write_control	W / R	1	
E2h	NVM Load Control	W / R	1	
F0h	Read Mode In	C	0	Note 2
B0～FF Except above command	LSI TEST Registers	W / R	Variable	

Note 2: This command can be used only for DBI Type C.

Command Accessibility

In initial state (an access level is 0), only User Command and B0h Manufacturer Command Access Protect command (B0h) are accessible. Other commands are treated as nop.

Of Manufacturer Command (B0h-ECh) defined in the table below, additional user commands (B1h-B4h) are accessible only when an access level is 1.

Other Manufacturer Commands (C0h-F4h) are accessible only when an access level is 2. See MCAP command (B0h) description for detail.

Table 17 User Command

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
00h	nop	Yes	Yes	Yes	Yes	Yes
01h	soft_reset	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
04h	Read Display Identification Information	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
0Ah	get_power_mode	Yes	Yes	Yes	Yes	Yes
0Bh	get_address_mode	Yes	Yes	Yes	Yes	Yes
0Ch	get_pixel_format	Yes	Yes	Yes	Yes	Yes
0Dh	get_display_mode	Yes	Yes	Yes	Yes	Yes
0Eh	get_signal_mode	Yes	Yes	Yes	Yes	Yes
0Fh	get_diagnostic _result	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
10h	enter_sleep_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
11h	exit_sleep_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
12h	enter_partial_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
13h	enter_normal_mod e	Yes	Yes	Yes	Yes	Yes
28h	set_display_off	Yes	Yes	Yes	Yes	Yes
29h	set_display_on	Yes	Yes	Yes	Yes	Yes
2Ah	set_column_addres s	Yes	Yes	Yes	Yes	Yes
2Bh	set_page_address	Yes	Yes	Yes	Yes	Yes
2Ch	write_memory_start	Yes	Yes	Yes	Yes	Yes
2Eh	read_memory_start	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
30h	set_partial_area	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
34h	set_tear_off	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
35h	set_tear_on	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes

Table 18 User Command (continued)

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
36h	set_address_mode	Yes	Yes	Yes	Yes	Yes
38h	exit_idle_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
39h	enter_idle_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
3Ah	set_pixel_format	Yes	Yes	Yes	Yes	Yes
3Ch	write_memory _continue	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
3Eh	read_memory _continue	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
44h	set_tear_scanline	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
45h	get_scanline	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	No
51h	Write_Display_ Brightness	No	No	No	No	No
52h	Read_Display_ Brightness_Value	No	No	No	No	No
53h	Write_Control_Disp lay	No	No	No	No	No
54h	Read_CTRL_Value _ Display	No	No	No	No	No
55h	Write_Content_ Adaptive_Brightnes s_ Control	No	No	No	No	No
56h	Write_Content_ Adaptive_Brightnes s_ Control	No	No	No	No	No
68h	Read_Automatic_ Brightness_Control _ Self-Diagnostic_Result	No	No	No	No	No
A1h	read_DDB_start	Yes	Yes	Yes	Yes	Yes

Note: Command may be accessed only when DM=0 (display operation is in synchronization with internal oscillation clock). Access to these commands is disabled when DM=1 and DPI is selected.

Table 19 Manufacturer Command

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
B0h	Manufacturer Command Access Protect	Yes	Yes	Yes	Yes	Yes
B1h	Low Power Mode Control	Yes	Yes	Yes	Yes	Yes
B3h	Frame Memory Access and Interface Setting	Yes	Yes	Yes	Yes	Yes
B4h	Display Mode and Frame Memory Write Mode Setting	Yes	Yes	Yes	Yes	Yes
BFh	Device Code Read	Yes	Yes	Yes	Yes	Yes
C0h	Panel Driving Setting	Yes	Yes	Yes	Yes	Yes
C1h	Display Timing Setting for Normal / Partial Mode	Yes	Yes	Yes	Yes	Yes
C3h	Display Timing Setting for Idle Mode	Yes	Yes	Yes	Yes	Yes
C4h	Source/VCOM/ Gate Driving Timing Setting	Yes	Yes	Yes	Yes	Yes
C8h ~ CAh	Gamma Set A ~ C	Yes	Yes	Yes	Yes	Yes
D0h	Power Setting (Common Setting)	Yes	Yes	Yes	Yes	Yes
D1h	VCOM Setting	Yes	Yes	Yes	Yes	Yes
D2h	Power Setting for Normal / Partial Mode	Yes	Yes	Yes	Yes	Yes
D4h	Power Setting for Idle Mode	Yes	Yes	Yes	Yes	Yes

Table 20 Manufacturer Command (continued)

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
E0h	NVM Access Control	No	No	No	No	Yes
E1h	set_DDB_write_control	No	No	No	No	Yes
E2h	NVM Load Control	No	No	No	No	Yes
F0h	Read Mode In	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
B0～FF Except above commands	LSI TEST Registers	No	No	No	No	No

Notes: 1. Command may be accessed only when DM=0 (display operation is in synchronization with internal oscillation clock). To access these commands is disabled when DM=1 and DPI is selected.

2. F0h Read Mode In command can be used only for DBI Type C.

Default Modes and Values

Table 21 User Command

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
00h	nop	None	N/A	N/A	N/A
01h	soft_reset	None	N/A	N/A	N/A
04h	Read Display Identification Information	1st	LCMID (Note2)	LCMID (Note2)	LCMID (Note2)
		2nd	LCDVr (Note2)	LCDVr (Note2)	LCDVr (Note2)
		3rd	PRJID (Note2)	PRJID (Note2)	PRJID (Note2)
0Ah	get_power_mode	1st	08h	08h	08h
0Bh	get_address_mode	1st	00h	No Change (Note1)	00h
0Ch	get_pixel_format	1st	66h	66h	66h
0Dh	get_display_mode	1st	00h	00h	00h
0Eh	get_signal_mode	1st	00h	00h	00h
0Fh	get_diagnostic _result	1st	00h	00h	00h
10h	enter_sleep_mode	None	Sleep Mode On	Sleep Mode On	Sleep Mode On
11h	exit_sleep_mode	None	Sleep Mode On	Sleep Mode On	Sleep Mode On
12h	enter_partial_mode	None	Normal Display Mode On	Normal Display Mode On	Normal Display Mode On
13h	enter_normal_mod e	None	Normal Display Mode On	Normal Display Mode On	Normal Display Mode On
28h	set_display_off	None	Display Off	Display Off	Display Off
29h	set_display_on	None	Display Off	Display Off	Display Off
2Ah	set_column_addre ss	1st/2nd SC[8:0]	000h	000h	000h
		3rd/4th EC[8:0]	0EFh	If set_address_mod e B5=0 : 0EFh B5=1 : 13Fh	0EFh

Table 22 User Command (continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
2Bh	set_page_address	1st/2nd SP[8:0]	000h	000h	000h
		3rd/4th EP[8:0]	13Fh	If set_address_mode B5=0: 13Fh B5=1: 0EFh	13Fh
2Ch	write_memory_start	all	Random Values	Not Cleared	Not Cleared
2Eh	read_memory_start	all	Random Values	Not Cleared	Not Cleared
30h	set_partial_area	1st/2nd SR[8:0]	000h	000h	000h
		3rd/4th ER[8:0]	13Fh	13Fh	13Fh
34h	set_tear_off	None	TE line output Off	TE line output Off	TE line output Off
35h	set_tear_on	1st	TE line output Off	TE line output Off	TE line output Off
36h	set_address_mode	1st	00h	No Change (Note1)	00h
38h	exit_idle_mode	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
39h	enter_idle_mode	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
3Ah	set_pixel_format	1st	66h	66h	66h
3Ch	write_memory_continue	all	Random Values	Not Cleared	Not Cleared
3Eh	read_memory_continue	all	Random Values	Not Cleared	Not Cleared
44h	set_tear_scanline	1st/2nd STS[8:0]	000h	000h	000h
45h	get_scanline	1st/2nd GTS[9:0]	000h (invalid)	000h (invalid)	000h (invalid)

Table 23 User Command (continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
51h / 52h	(Write/Read)_Display_ Brightness	1st/2nd	00h	00h	00h
53h / 54h	(Write/Read)_Control_Display	1st/2nd	00h	00h	00h
55h / 56h	(Write/Read)_Content_Adaptive_ Brightness_Control	1st/2nd	00h	00h	00h
68h	Read_Automatic_ Brightness_Control _ Self-Diagnostic_Result	2nd	00h	00h	00h
A1h	read_DDB_start	1st	LCMID (Note2)	LCMID (Note2)	LCMID (Note2)
		2nd	LCDVr (Note2)	LCDVr (Note2)	LCDVr (Note2)
		3rd	PRJID (Note2)	PRJID (Note2)	PRJID (Note2)

Notes: 1. No Change from the value before soft_reset command.
2. Data is loaded from internal NVM. The supplier ID written to NVM is set as default.

Table 24 Manufacturer Command

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
B0h	Manufacturer Command Access Protect	1st	MCAP=2'h0 MCAPB=4'h0	No Change (Note1)	MCAP=2'h0 MCAPB=4'h0
		2nd	MCAPC=6'h00	No Change (Note1)	MCAPC=6'h00
B1h	Low Power Mode Control	1st	STB=2'h0	No Change (Note 1)	STB=2'h0
B3h	Frame Memory Access and Interface Setting	1st	WEMODE=0	No Change (Note1)	WEMODE=0
		2nd	TEI[2:0]=3'h0	No Change (Note1)	TEI[2:0]=3'h0
		3rd	DENC[2:0]=3'h0	No Change (Note1)	DENC[2:0]=3'h0
		4th	EPF[1:0]=2'h0 DFM=0	No Change (Note1)	EPF[1:0]=2'h0 DFM=0
		5th	00h	No Change (Note 1)	00h
B4h	Display Mode and Frame Memory Write Mode Setting	1st	SDOE=0, RM=0 DM[1:0]=2'h0	No Change (Note1)	SDOE=0, RM=0 DM[1:0]=2'h0

Table 25 Manufacturer Command (continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
BFh	Device Code Read	1st	8'h01	8'h01	8'h01
		2nd	8'h22	8'h22	8'h22
		3rd	8'h15	8'h15	8'h15
		4th	8'h26	8'h26	8'h26
C0h	Panel Driving Setting	1st	GIP=0 REV=0 SM=0 GS=0 BGR=0 SS=0	No Change (Note1)	GIP=0 REV=0 SM=0 GS=0 BGR=0 SS=0
		2nd	NL[6:0]=7'h4F	No Change (Note1)	NL[6:0]=7'h4F
		3rd	SCN[6:0]=7'h00	No Change (Note1)	SCN[6:0]=7'h00
		4th	00h	No Change (Note1)	00h
		5th	BLV=1 PTV=0	No Change (Note1)	BLV=1 PTV=0
		6th	BLS=0 NDL=0 PTS[2:0]=3'h0 PTDC=0	No Change (Note1)	BLS=0 NDL=0 PTS[2:0]=3'h0 PTDC=0
		7th	PTG=0 ISC[3:0]=4'h1	No Change (Note1)	PTG=0 ISC[3:0]=4'h1
		8th	PCDIVH[2:0]=3'h0 PCDIVL[2:0]=3'h0	No Change (Note1)	PCDIVH[2:0]=3'h0 PCDIVL[2:0]=3'h0
C1h,C3h	Display Timing Setting for Normal / Partial Mode Display Timing Setting for Idle Mode	1st	BCx=1	No Change (Note1)	BCx=1
		2nd	DIVx[1:0]=2'h2	No Change (Note1)	DIVx[1:0]=2'h2
		3rd	RTNx[5:0]=6'h28	No Change (Note1)	RTNx[5:0]=6'h28
		4th	BPx[7:0]=8'h08	No Change (Note1)	BPx[7:0]=8'h08
		5th	FPx[7:0]=8'h08	No Change (Note1)	FPx[7:0]=8'h08

C4h	Source/VCOM/Gate Driving Timing Setting	1st	SDT[2:0]=3'h1 NOW[2:0]=3'h1	No Change (Note1)	SDT[2:0]=3'h1 NOW[2:0]=3'h1
		2nd	MCP[2:0]=3'h1	No Change (Note1)	MCP[2:0]=3'h1
		3rd	VEQW[3:0]=4'h0 VEM[1:0]=2'h0	No Change (Note1)	VEQW[3:0]=4'h0 VEM[1:0]=2'h0
		4th	SPCW[3:0]=4'h0	No Change (Note1)	SPCW[3:0]=4'h0
		5th	00h	No Change (Note 1)	00h

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
C8h ~ CAh	Gamma Set A ~ C	1st-18th	All “0”	No Change (Note1)	All “0”
D0h	Power Setting (Common Setting)	1st	BT[2:0]=3’h6	No Change (Note1)	BT[2:0]=3’h6
		2nd	53h	No Change (Note1)	53h
		3rd	VC2[2:0]=3’h2	No Change (Note1)	VC2[2:0]=3’h2
		4th	VRH[5:0]=6’h3F	No Change (Note1)	VRH[5:0]=6’h3F
		5th	DCT=3’h7	No Change (Note1)	DCT=3’h7
		6th	00h	No Change (Note1)	00h
D1h	VCOM Setting	1st	VCM[6:0]=7’h7F	No Change (Note1)	VCM[6:0]=7’h7F
		2nd	VDV[6:0]=7’h00	No Change (Note1)	VDV[6:0]=7’h00
		3rd	10h	No Change (Note1)	10h
D2h,D4h	Power Setting -for Normal / Partial Mode -for Idle Mode	1st	8’h1	No Change (Note1)	8’h1
		2nd	DC1x[2:0]=3’h2 DC0x[2:0]=3’h4	No Change (Note1)	DC1x[2:0]=3’h2 DC0x[2:0]=3’h4
E0h	NVM Access Control	1st	NVAE =0	No Change	NVAE =0
		2nd	FTT=0	No Change	FTT=0
		3rd	TEM=0 VERIFLGWR=0 VERIFLGER=0	No Change	TEM=0 VERIFLGWR=0 VERIFLGER=0
E1h	set_DDB_write_control	1st	WCDDB=0	No Change	WCDDB=0
E2h	NVM Load Control	1st	LD[6:0]=7’h00	No Change	LD[6:0]=7’h00
F0h	Read Mode In	None	Read Mode Off	Read Mode Off	Read Mode Off

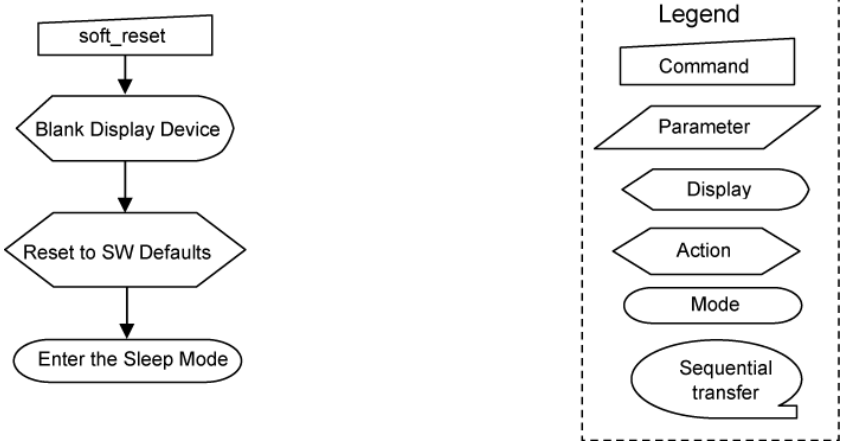
Note: No Change from the value before soft_reset command.

User Command

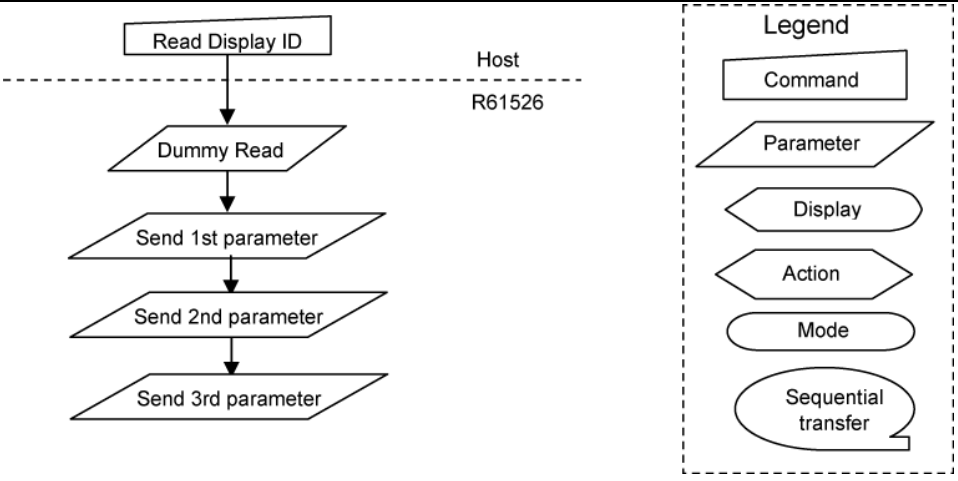
nop: 00h

00h	nop												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	0	0	0	0	00h
Parameter	None												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read. X = Don't Care												
Restriction	-												
Flow Chart	-												

soft_reset: 01h

01h	soft_reset												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	0	0	0	1	01h
Parameter	None												
Description	The display module performs a software reset. Commands and parameters are written with their SW Reset default values. (See “Default Modes and Values”.) Note: The Frame Memory contents are unaffected by this command. X = Don’t care												
Restriction	If a soft_reset is sent when the display module is not in the Sleep Mode, the host processor must wait 120 ms before sending an exit_sleep_mode command. soft_reset should not be sent during exit_sleep_mode sequence. No new command setting is allowed until the R61526 enters the Sleep Mode. See “State & Command sequence” for sequence to enter the Sleep Mode. If a soft_reset is sent when in the Sleep Mode, data in NVM and EEPROM are read. No new command setting is inhibited when data is read (5ms).												
Flow Chart													

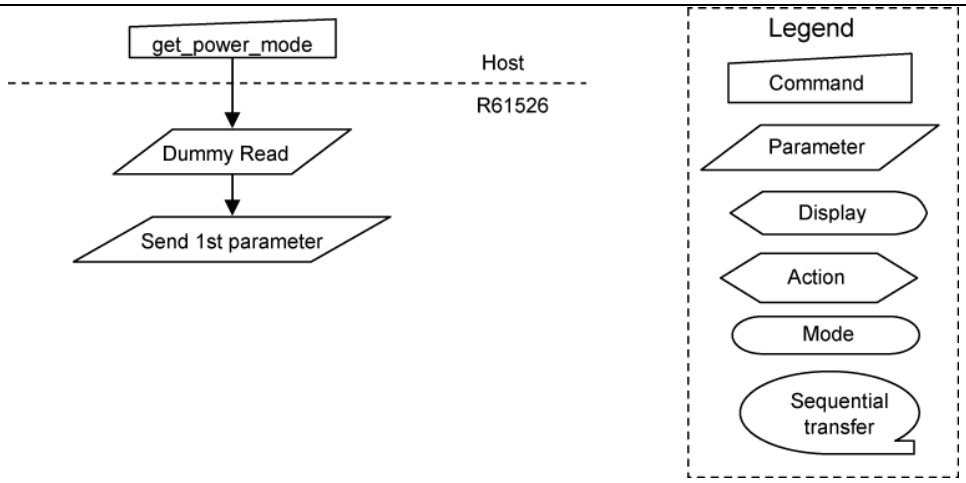
Read Display ID Information: 04h

04h	get_power_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	0	0	0	0	1	0	0	04h
Dummy Parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
1st Parameter	1	↑	1	X	LC MID [7]	LC MID [6]	LC MID [5]	LC MID [4]	LC MID [3]	LC MID [2]	LC MID [1]	LC MID [0]	XXh
2nd parameter	1	↑	1	X	LCD V[7]	LCD V[6]	LCD V[5]	LCD V[4]	LCD V[3]	LCD V[2]	LCD V[1]	LCD V[0]	80-FFh
3rd Parameter	1	↑	1	X	PRJ ID [7]	PRJ ID [7]	PRJ ID [7]	PRJ ID [7]	PRJ ID [7]	PRJ ID [7]	PRJ ID [7]	PRJ ID [7]	XXh
Description	This is a read only command to read the display's identification number. The 1st parameter is dummy read parameter. **LCMID** LCMID is a number to identify module manufacturer of LCM. **LCDV** LCDV is to record versions of the module and the driver. **PRJID** PRJID is to record the project and the product numbers. The above numbers and version are stored in NVM. The numbers and versions can be changed by writing data to NVM. For details, see description of NVM write operation. Values of 04h are the same as those of A1h commands. x = Don't care												
Restriction	-												
Flow Chart													

get_power_mode: 0Ah

0Ah	get_power_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	0	1	0	1	0	0Ah
1st parameter	1	↑	1	x	0	IDM ON	PTL ON	SLP OUT	NOR ON	DSP ON	0	0	XXh
Description	The display module returns the current power mode.												

Bit	Description	Comment	Command list Symbol
D7	Reserved	Set to “0”	-
D6	Idle Mode On/Off		IDMON
D5	Partial Mode On/Off		PTLON
D4	Sleep Mode On/Off		SLPOUT
D3	Display Normal Mode On/Off		NORON
D2	Display On/Off		DSPON
D1	Reserved	Set to “0”	-
D0	Reserved	Set to “0”	-

0Ah	get_power_mode
	• Bit D7 – Not defined This bit is not applicable. Set to “0”. • Bit D6 – Idle Mode On/Off ‘0’ = Idle Mode Off. ‘1’ = Idle Mode On. • Bit D5 – Partial Mode On/Off ‘0’ = Partial Mode Off. ‘1’ = Partial Mode On. • Bit D4 – Sleep Mode On/Off ‘0’ = Sleep Mode On ‘1’ = Sleep Mode Off • Bit D3 – Display Normal Mode On/Off ‘0’ = Display Normal Mode Off ‘1’ = Display Normal Mode On • Bit D2 – Display On/Off ‘0’ = Display is Off ‘1’ = Display is On • Bit D1 – Reserved This bit is not applicable. Set to “0”. • Bit D0 – Reserved This bit is not applicable. Set to “0”. X = Don’t care.
Restriction	-
Flow chart	

get_address_mode: 0Bh

<table>
<tr><td>0Bh</td><td colspan="13">get_address_mode</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB [17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0Bh</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>x</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>0</td><td>0</td><td>0</td><td>B0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">The display module returns the current status of the display as described in the table below. This command setting depends on set_address_mode (36h).
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command list symbol</th></tr>
<tr><td>D7</td><td>Page Address Order</td><td></td><td>B7</td></tr>
<tr><td>D6</td><td>Column Address Order</td><td></td><td>B6</td></tr>
<tr><td>D5</td><td>Page/column Order</td><td></td><td>B5</td></tr>
<tr><td>D4</td><td>Line Address Order</td><td></td><td>B4</td></tr>
<tr><td>D3</td><td>RGB/BGR Order</td><td>Set to “0”</td><td></td></tr>
<tr><td>D2</td><td>Display Data Latch Order</td><td>Set to “0”</td><td></td></tr>
<tr><td>D1</td><td>Reserved</td><td>Set to “0”</td><td></td></tr>
<tr><td>D0</td><td>Switching between Common outputs and Frame Memory</td><td></td><td>B0</td></tr>
</table>

Bit D7 - Page Address Order

‘0’ = Top to Bottom (When set_address_mode D7 = ’0’)
‘1’ = Bottom to Top (When set_address_mode D7 = ‘1’)

Bit D6 – Column Address Order

‘0’ = Left to Right (When set_address_mode D6 = ‘0’)
‘1’ = Right to Left (When set_address_mode D6 = ‘1’)

Bit D5 – Page/column Order

‘0’ = Normal Mode (When set_address_mode D5 = ‘0’)
‘1’ = Reverse Mode (When set_address_mode D5 = ‘1’)
Note: See “Host Processor to Memory Write/Read Direction” and “Memory Access Control” for D7 to D5 bits.

Bit D4 – Line Address Order

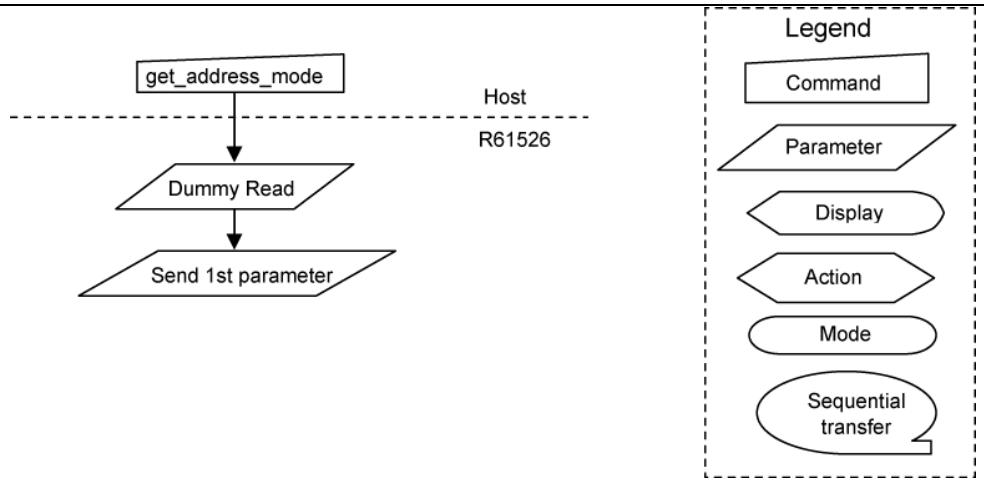
‘0’ = LCD Refresh Top to Bottom (When set_address_mode = ‘0’ (D4))
‘1’ = LCD Refresh Bottom to Top (When set_address_mode = ‘1’ (D4))
Note: See “Memory Access Control (36h)” for D4 bit.

Bit D3 – RGB/BGR Order

This bit is not applicable. Set to “0” (Not supported).

Bit D2 – Display Data latch Data Order

This bit is not applicable. Set to “0” (Not supported).</td></tr>
</table>

0Bh	get_address_mode
Description	• Bit D1 – Reserved This bit is not applicable. Set to “0” (Not supported). • Bit D0 – Switching between Common outputs and Frame Memory ‘0’ = Reading direction from Frame Memory to Common Outputs is identical with writing direction. ‘1’ = Reading direction from Frame Memory to Common Outputs is reverse of writing direction. X = Don’t care.
Restriction	-
Flow Chart	

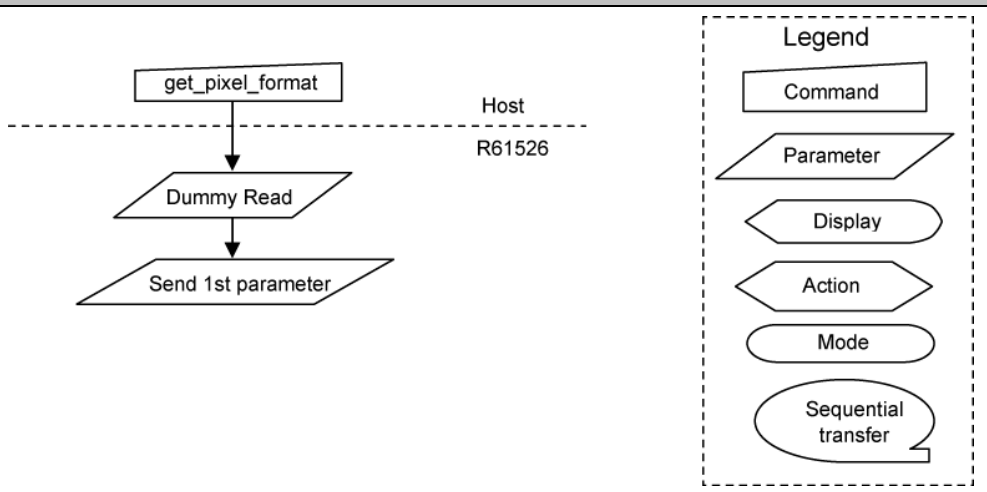
Note: See “”State Transition Diagram” for display mode transition.

get_pixel_format: 0Ch

<table>
<tr><td>0Ch</td><td colspan="13">get_pixel_format</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB [17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0Ch</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>x</td><td>0</td><td>D6</td><td>D5</td><td>D4</td><td>0</td><td>D2</td><td>D1</td><td>D0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below. This command setting depends on set_pixel_format (3Ah).
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th></tr>
<tr><td>D7</td><td rowspan="4">DPI Pixel format
(RGB Interface Color Format)</td><td>Set to “0”</td></tr>
<tr><td>D6</td><td>D6</td></tr>
<tr><td>D5</td><td>D5</td></tr>
<tr><td>D4</td><td>D4</td></tr>
<tr><td>D3</td><td rowspan="4">DBI Pixel Format
(Control Interface Color Format)</td><td>Set to “0”</td></tr>
<tr><td>D2</td><td>D2</td></tr>
<tr><td>D1</td><td>D1</td></tr>
<tr><td>D0</td><td>D0</td></tr>
</table>

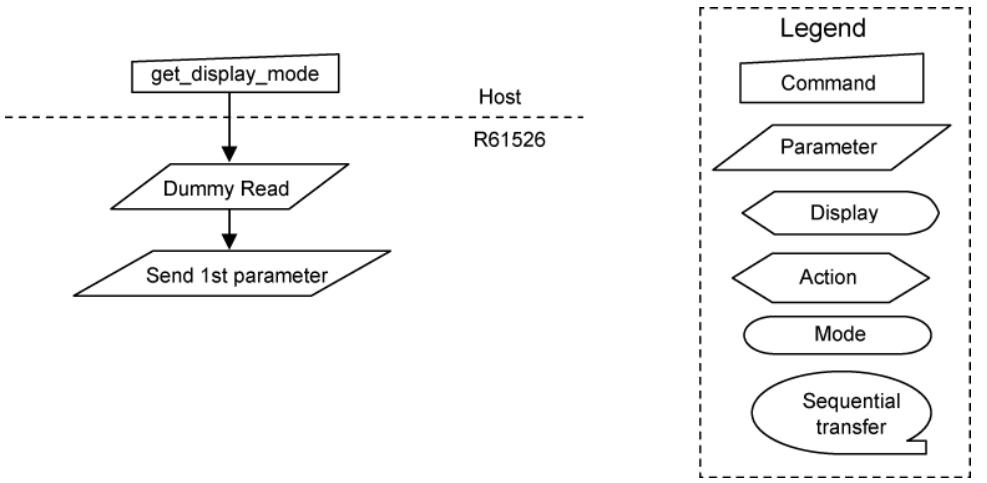
Bit D[6:4] – DPI Pixel Format (RGB Interface Color Format Selection)
Bit D[2:0] – DBI Pixel Format (Control Interface Color Format Selection)
Bit D7 and D3 - These bits are not applicable. Set to “0”.
See description of command set_pixel_format (3Ah).

<table>
<tr><th>Control Interface Color Format</th><th>D6/D2</th><th>D5/D1</th><th>D4/D0</th></tr>
<tr><td>Setting inhibited</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>3 bits/pixel (8 colors)</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Setting inhibited</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Setting inhibited</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Setting inhibited</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>16 bits/pixel (65,536 colors)</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>18 bits/pixel (262,1444 colors)</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Setting inhibited</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Note 1: Abnormal image will be on the display when “setting inhibited“ bit is used.
Note 2: In DBI type B operation, set only D[2:0]=5 (16 bits/pixel) or 6(18 bits/pixel).
Note 3: In DBI type C serial interface operation, set only D[2:0]=1(3 bits/pixel) or 6(18 bits/pixel).
Note 4: In DPI operation, set only D[6:4]=5(16 bits/pixel) or 6(18 bits/pixel)
x = Don’t care</td></tr>
</table>

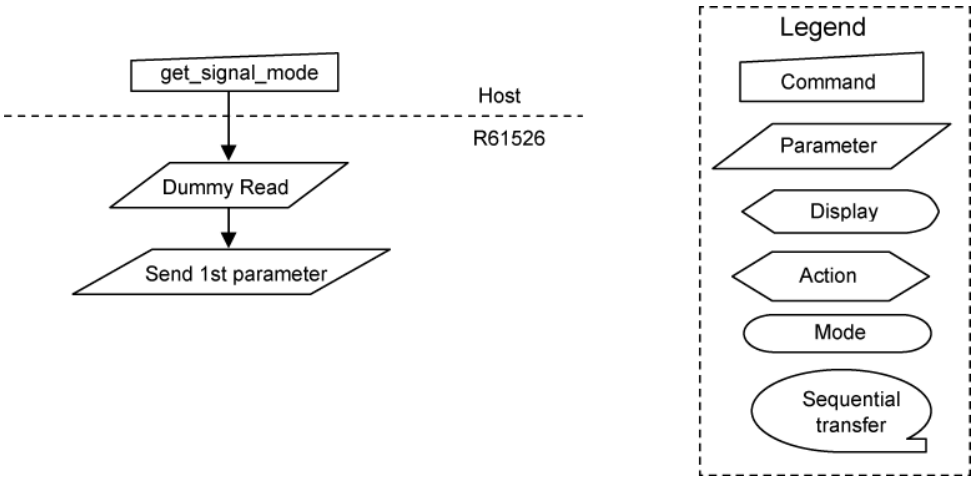
0Ch	get_pixel_format
Flow chart	

get_display_mode: 0Dh

<table>
<tr><td>0Dh</td><td colspan="13">get_display_mode</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB [17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0Dh</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">The display module returns the current status of the display as described in the table below.
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command list symbol</th></tr>
<tr><td>D7</td><td>Reserved</td><td>Set to “0”</td><td></td></tr>
<tr><td>D6</td><td>Reserved</td><td>Set to “0”</td><td></td></tr>
<tr><td>D5</td><td>Inversion ON/OFF</td><td>Set to “0”</td><td></td></tr>
<tr><td>D4</td><td>Reserved</td><td>Set to “0”</td><td></td></tr>
<tr><td>D3</td><td>Reserved</td><td>Set to “0”</td><td></td></tr>
<tr><td>D2</td><td>Gamma Curve Selection</td><td>Set to “0”</td><td></td></tr>
<tr><td>D1</td><td>Gamma Curve Selection</td><td>Set to “0”</td><td></td></tr>
<tr><td>D0</td><td>Gamma Curve Selection</td><td>Set to “0”</td><td></td></tr>
</table>
• Bit D7 — Reserved
This bit is not applicable. Set to “0”.
• Bit D6 – Reserved
This bit is not applicable. Set to “0”.
• Bit D5 – Inversion On/Off
This bit is not applicable. Set to “0”.
• Bit D4, D3 – Reserved
These bits are not applicable. Set to “0”.
• Bit D2, D1, D0 – Gamma Curve Selection
These bits are not applicable. Set to “0”.
x = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
</table>

0Dh	get_display_mode
Flow Chart	

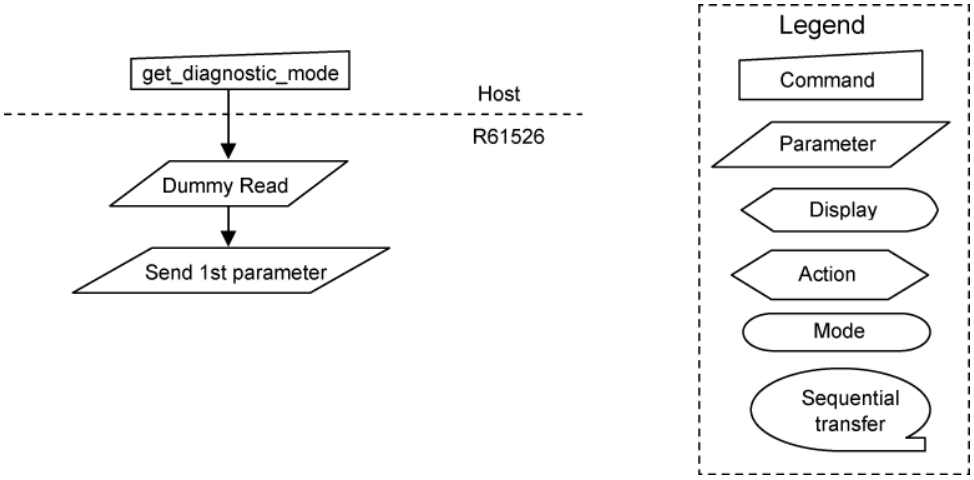
get_signal_mode: 0Eh

<table>
<tr><td>0Eh</td><td colspan="13">get_signal_mode</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB [17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0Eh</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>x</td><td>TEON</td><td>TELOM</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">The display module returns the Display Signal Mode as described in the table below.
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command list symbol</th></tr>
<tr><td>D7</td><td>Tearing Effect line ON/OFF</td><td></td><td>TEON</td></tr>
<tr><td>D6</td><td>Tearing Effect line Output Mode</td><td></td><td>TELOM</td></tr>
<tr><td>D5</td><td>Reserved</td><td>Set to “0”</td><td>-</td></tr>
<tr><td>D4</td><td>Reserved</td><td>Set to “0”</td><td>-</td></tr>
<tr><td>D3</td><td>Reserved</td><td>Set to “0”</td><td>-</td></tr>
<tr><td>D2</td><td>Reserved</td><td>Set to “0”</td><td>-</td></tr>
<tr><td>D1</td><td>Reserved</td><td>Set to “0”</td><td>-</td></tr>
<tr><td>D0</td><td>Reserved</td><td>Set to “0”</td><td>-</td></tr>
</table>
• Bit D7 – Tearing Effect Line On/Off
‘0’ = Tearing Effect Line Off
‘1’ = Tearing Effect On
• Bit D6 – Tearing Effect Line Output Mode (See “set_tear_on: 35h”).
‘0’ = Mode1
‘1’ = Mode2
• Bit D[5:0] – Reserved
These bits are not applicable. Set to “0”.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

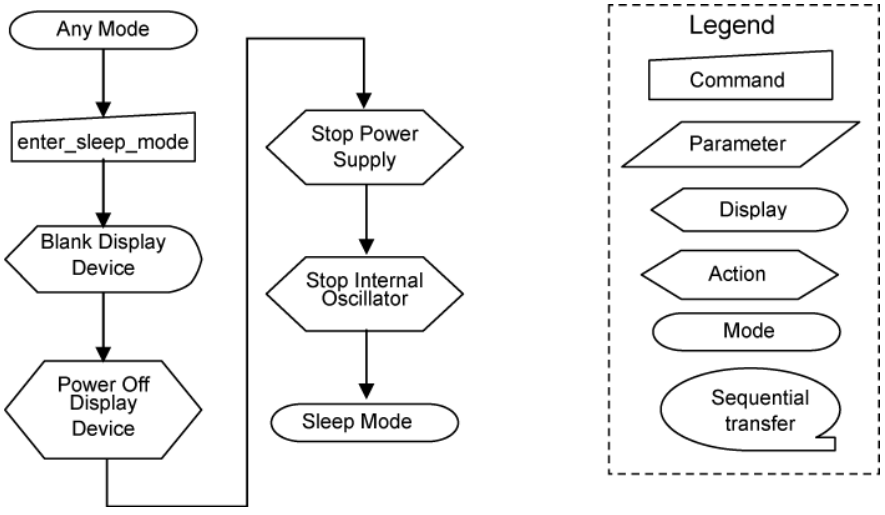
get_diagnostic_result:0Fh

<table>
<tr><td>0Fh</td><td colspan="13">get_diagnostic_result</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB [17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0Fh</td></tr>
<tr><td>1st Parameter</td><td>0</td><td>↑</td><td>1</td><td>x</td><td>FUN CL</td><td>FUN CD</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command List Symbol</th></tr>
<tr><td>D7</td><td>Register Loading Detection</td><td></td><td>FUNCL</td></tr>
<tr><td>D6</td><td>Functionality Detection</td><td></td><td>FUNCD</td></tr>
<tr><td>D5</td><td>Chip Attachment Detection</td><td>Set to “0”</td><td>-</td></tr>
<tr><td>D4</td><td>Display Glass Break Detection</td><td>Set to “0”</td><td>-</td></tr>
<tr><td>D3</td><td>Reserved</td><td>Set to “0”</td><td>-</td></tr>
<tr><td>D2</td><td>Reserved</td><td>Set to “0”</td><td>-</td></tr>
<tr><td>D1</td><td>Reserved</td><td>Set to “0”</td><td>-</td></tr>
<tr><td>D0</td><td>Reserved</td><td>Set to “0”</td><td>-</td></tr>
</table>
The display module returns the self-diagnostic results following a Sleep Out command as shown in the table above.
・ Bit D7 – Register Loading Detection
This bit shows a result after a register value is loaded. If the value is successfully loaded, the value is inverted.
・ Bit D6 – Functionality Detection
Note: See Self Diagnostic Function for D6.
・ Bit D5 – Chip Attachment Detection
This bit is not applicable. Set to “0”.
・Bit D4 –Display Glass Break Detection
This bit is not applicable. Set to “0”.
・Bits D3, D2, D1, D0 – Reserved. Set to 0.

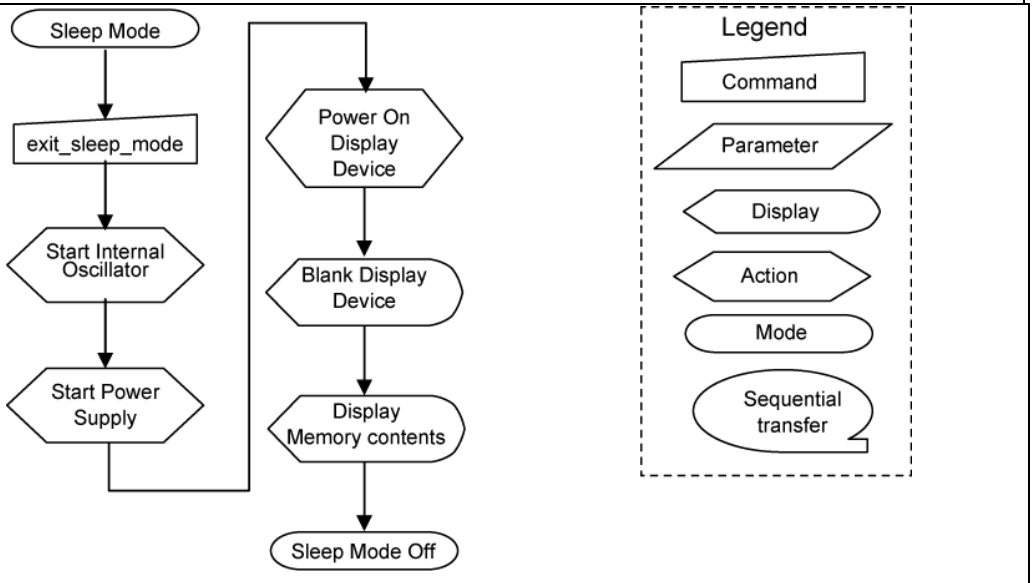
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
</table>

0Fh	get_diagnostic_result
Flow Chart	

enter_sleep_mode: 10h

10h	enter_sleep_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	1	0	0	0	0	10h
Parameter	None												
Description	This command causes the LCD module to enter the Sleep mode. In this mode, the DC/DC converter, internal oscillator and panel scanning stop. See “State & Command sequence” for Sleep In sequence. DBI remains operational and the memory maintains its contents when in the Sleep mode. See State Transition Diagram for each stage of transition. X = Don’t care												
Restriction	This command has no effect when the module is already in the Sleep mode. Sleep mode can be exited only when the exit_sleep_mode (11h) is transmitted. Sending a new command is prohibited while the R61526 performs either power supply OFF sequencer or blank scan.												
Flow Chart													

exit_sleep_mode: 11h

11h	exit_sleep_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	1	0	0	0	1	11h
Parameter	None												
Description	This command causes the display module to exit Sleep mode. DC/DC converter, internal oscillation and panel scanning start. See “State & Command sequence” for exit_sleep_mode. See State Transition Diagram for each stage of transition. X = Don’t care												
Restriction	This command shall not cause any visual effect on display device when the display module is not in Sleep mode. No new command setting is allowed during power supply ON sequence. The power supply ON sequencer operates for a period of ”NVM data load time (5ms) + 7 frames.” The host processor must wait 7 frames after sending an enter_sleep_mode command before sending an exit_sleep_mode command. The display runs the self-diagnostic function after this command is received. NVM data read is performed when an exit_sleep_mode command is written. Do not send any command during data read (5ms).												
Flow Chart													

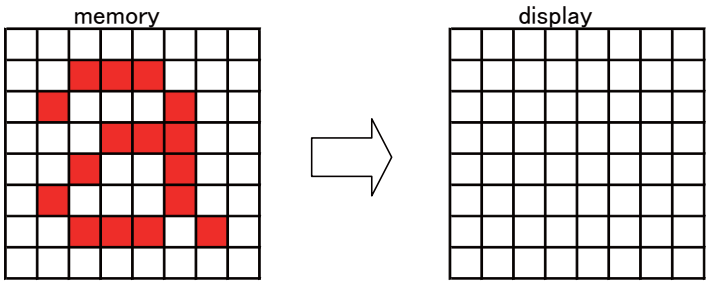
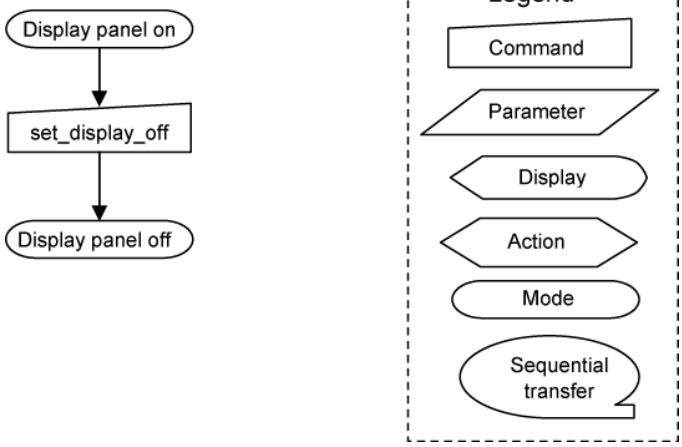
enter_partial_mode: 12h

12h	enter_partial_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	1	0	0	1	0	12h
Parameter	None												
Description	This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the set_partial_area command (30h). To leave Partial Display Mode, the enter_normal_mode (13h) has to be written. X=Don't care Note: When a command breaks in the middle of frame period in Normal mode, the command is enabled from the next frame period.												
Restriction	This command has no effect when the module is already in Partial mode.												
Flow Chart	See set_partial_area (30h).												

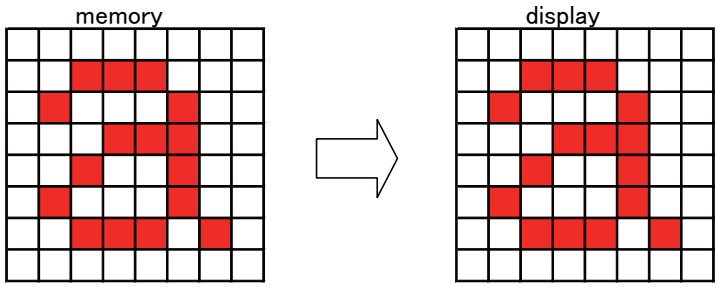
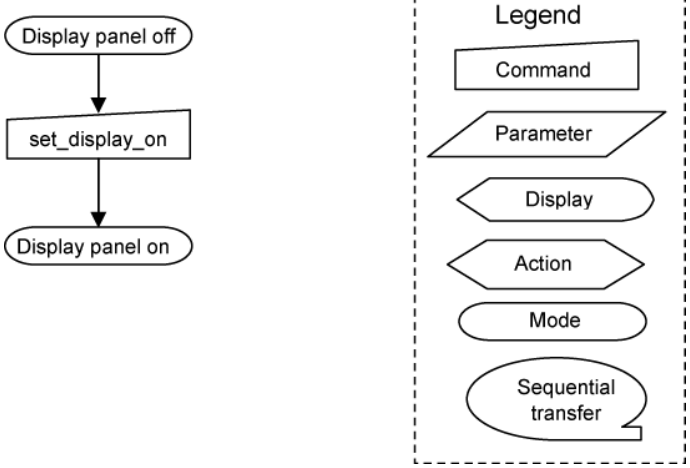
enter_normal_mode: 13h

13h	enter_normal_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	1	0	0	1	1	13h
Parameter	None												
Description	This command causes the display module to enter the Normal mode. Partial mode is off when in the Normal mode. X = Don't care Note: When a command breaks in the middle of frame period in Partial mode, that command becomes valid from the next frame period.												
Restriction	This command has no effect when Normal mode is already active.												
Flow Chart	See the description of command set_partial_area (30h) when using this command.												

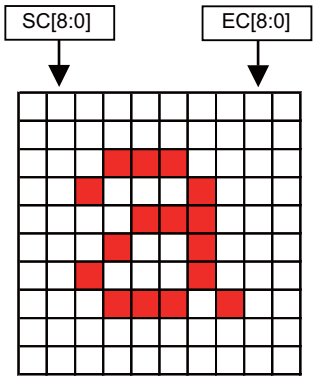
set_display_off: 28h

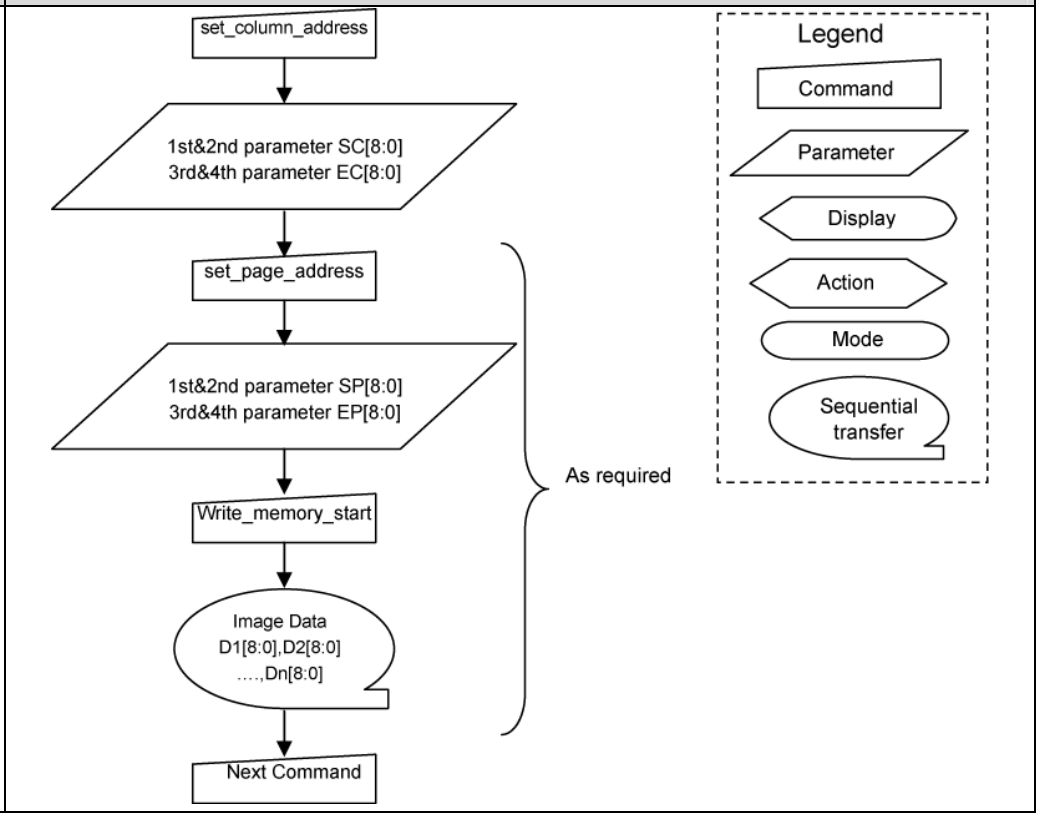
28h	Set_display_off												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	0	1	0	0	0	28h
Parameter	None												
Description	This command causes the display module to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. (Example)  See Panel Driving Setting (C0h) for mode setting when DISPOFF. X = Don't care												
Restriction	This command has no effect when the display panel is already off.												
Flow Chart													

set_display_on: 29h

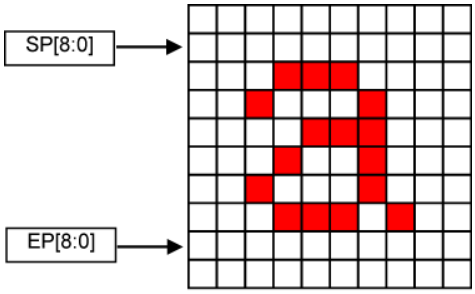
29h	**set_display_on**												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	0	1	0	1	0	0	1	29h
Parameter	None												
Description	This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. (Example) memory display  X = Don't care												
Restriction	This command has no effect when the display panel is already on.												
Flow Chart													

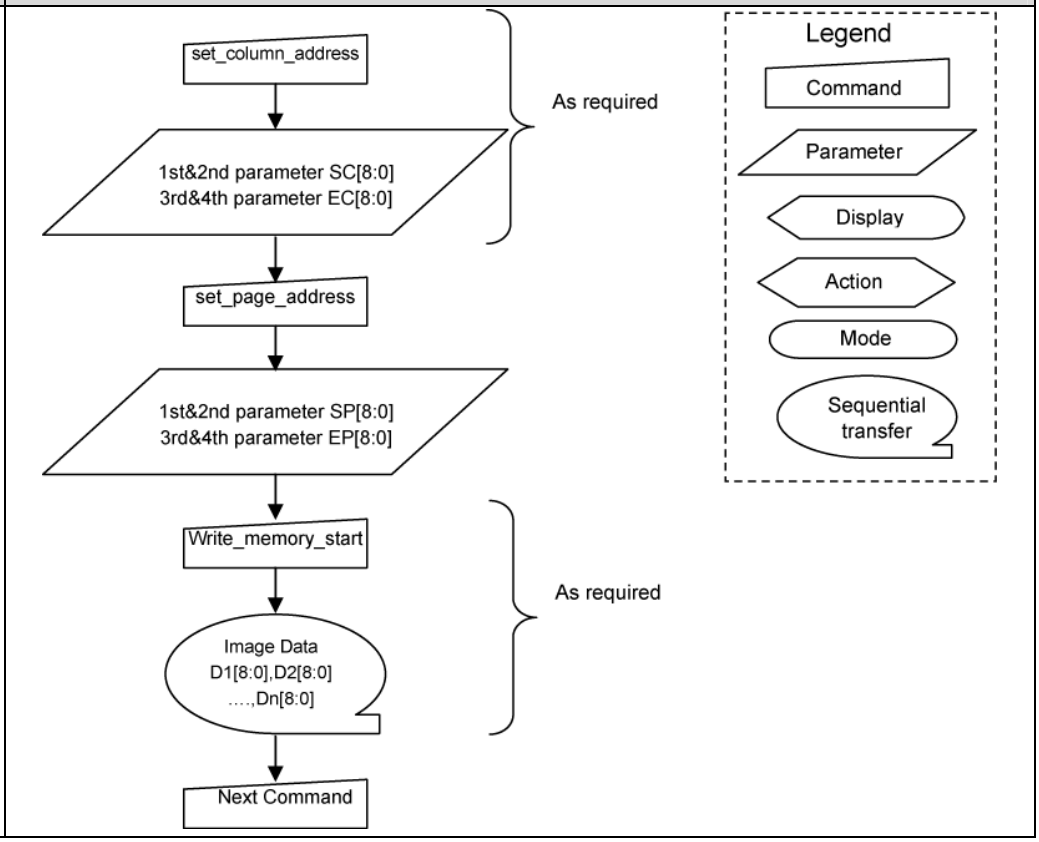
set_column_address: 2Ah

2Ah	set_column_address												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	0	1	0	1	0	2Ah
1st parameter	1	1	↑	x	0	0	0	0	0	0	0	SC[8]	XXh
2nd parameter	1	1	↑	x	SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]	XXh
3rd parameter	1	1	↑	x	0	0	0	0	0	0	0	EC[8]	XXh
4th parameter	1	1	↑	x	EC[7]	EC[6]	EC[5]	EC[4]	EC[3]	EC[2]	EC[1]	EC[0]	XXh
Description	This command defines the column an area on the frame memory that can be accessed by the host processor. The values of SC[8:0] and EC[8:0] are referred to when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written. No status bits are changed. Example  X=Don't care.												
Restriction	SC [8:0] must not be equal to EC[8:0], it must be less than EC[8:0]. Set the 1st parameter B5 in set_address_mode (36h) in advance. Note: The parameters are disregarded in following cases: • If set_address_mode B5 = 0: SC[8:0] or EC[8:0] > 0EFh • If set_address_mode B5 = 1: SC[8:0] or EC[8:0] > 13Fh												

2Ah	set_column_address
Flow Chart	

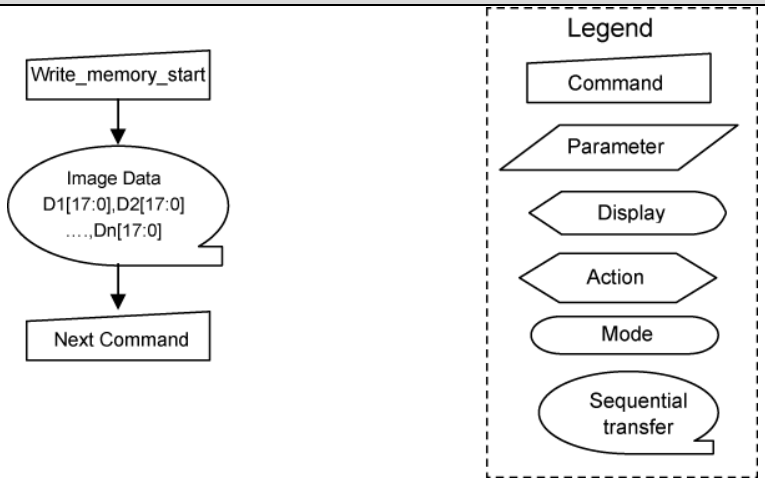
set_page_address: 2Bh

2Bh	set_page_address												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	0	1	0	1	1	2Bh
1st parameter	1	1	↑	x	0	0	0	0	0	0	0	SP[8]	XXh
2nd parameter	1	1	↑	x	SP[7]	SP[6]	SP[5]	SP[4]	SP[3]	SP[2]	SP[1]	SP[0]	XXh
3rd parameter	1	1	↑	x	0	0	0	0	0	0	0	EP[8]	XXh
4th parameter	1	1	↑	x	EP[7]	EP[6]	EP[5]	EP[4]	EP[3]	EP[2]	EP[1]	EP[0]	XXh
Description	This command defines the page extent of the frame memory accessed by the host processor. No status bits are changed. The values of SP[8:0] and EP[8:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written. Example  X=Don't care												
Restriction	SC [8:0] must not be equal to EC[8:0], it must be less than EC[8:0]. Set the 1st parameter B5 in set_address_mode (36h) in advance. Note: The parameters are disregarded in following cases. • If set_address_mode B5 = 0: SP[8:0] or EP[8:0] > 13Fh • If set_address_mode B5 = 1: SP[8:0] or EP[8:0] > 0EFh												

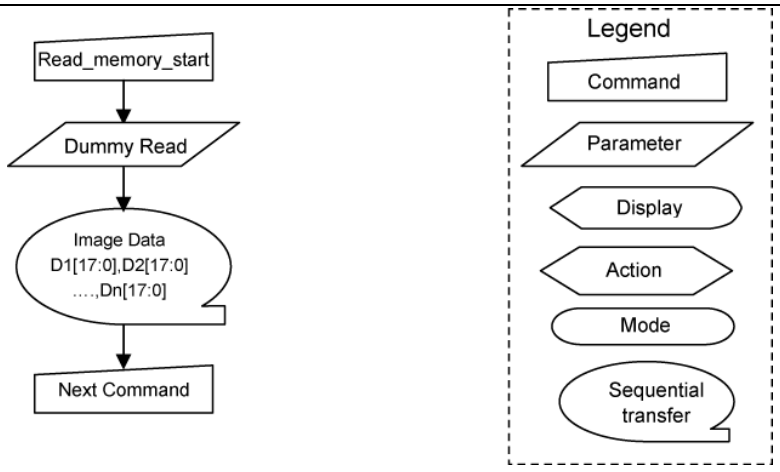
2Bh	set_page_address
Flow Chart	

write_memory_start: 2Ch

2Ch	write_memory_start												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	0	1	1	0	0	2Ch
1st parameter	1	1	↑	D1 [17:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000… 3FF
: :	1	1	↑	Dx [17:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000… 3FF
Nth parameter	1	1	↑	Dn [17:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000… 3FF
Description	This command transfers image data from the host processor to the display module's frame memory. No status bits are changed. If this command is received, the column and page registers are set to the Start Column (SC) and Start Page (SP) respectively. After pixel data 1 is stored in frame memory at (SC, SP), address counter's direction differs depending on Bits 5, 6, 7 of set_address_mode (36h). See "Host Processor to Memory Write/Read Direction". If Frame Memory Access and Interface setting (B3h) WEMODE = 0: If the number of pixels in transfer data exceeds (EC-SC+1)x(EP-SP+1), the extra pixels are ignored. If Frame Memory Access and Interface setting (B3h) WEMODE = 1 When the number of pixels in transfer data exceeds (EC-SC+1)x(EP-SP+1), the column register and the page register are set to the Start Column and Start Page respectively. Then subsequent data is written to the frame memory. Sending any other command will stop writing to the frame memory. See DBI Data Format and DPI Data Format for write data formats in DBI Type B 18-/16-/9-/8-bit bus interface, Type C serial interface, and DPI. X=Don't care.												
Restriction	In all color modes, there are no restrictions on the length of parameters. To execute 2Eh or 3Eh (read_memory) command, wait for 8 write cycles (66ns × 8 cycles) or more after transferring pixel data by 2Ch or 3Ch (write_memory) command. If a write cycle is 180ns or more, wait time is unnecessary. To issue 2Ah command, 2Bh command, 36h command, or B3h command (WEMODE) after executing 2Ch command or 3Ch command, transfer pixel data of 10 words or more by 2Ch or 3Ch command or wait for 10 cycles (66ns × 10 cycles). If a write cycle is 180ns or more, wait time is unnecessary.												

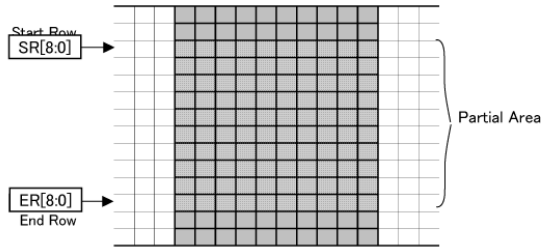
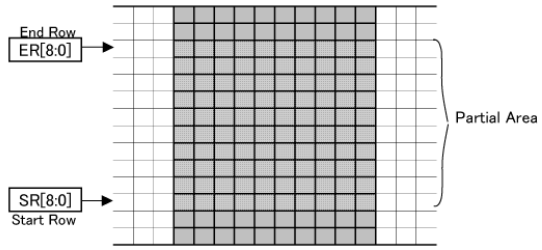
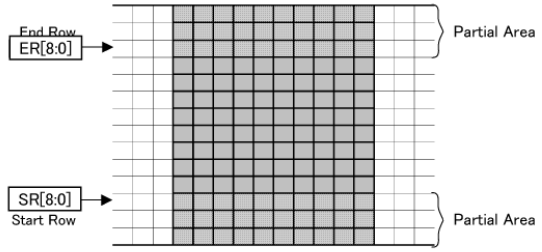
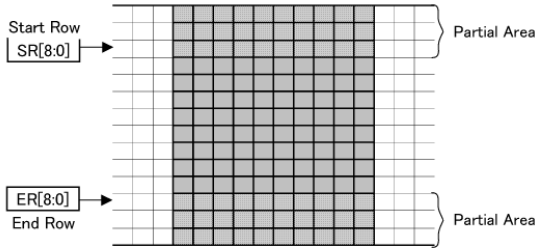
2Ch	write_memory_start
Flow Chart	

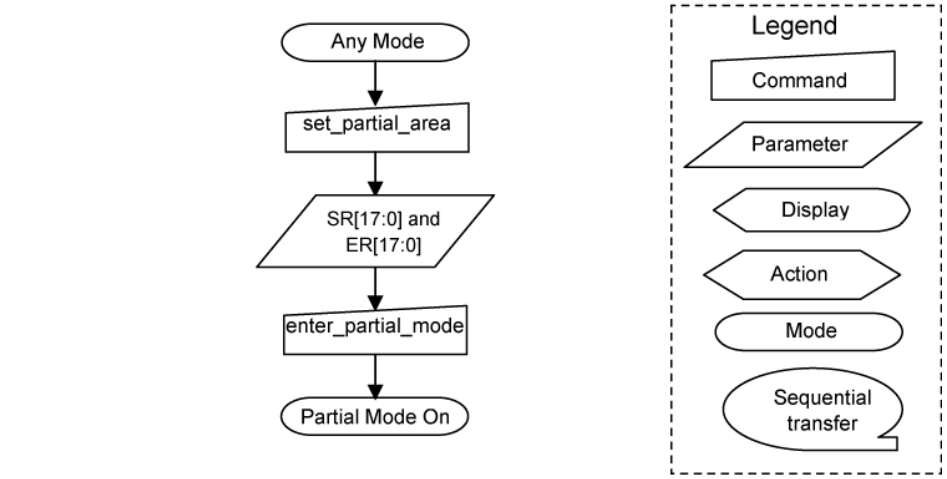
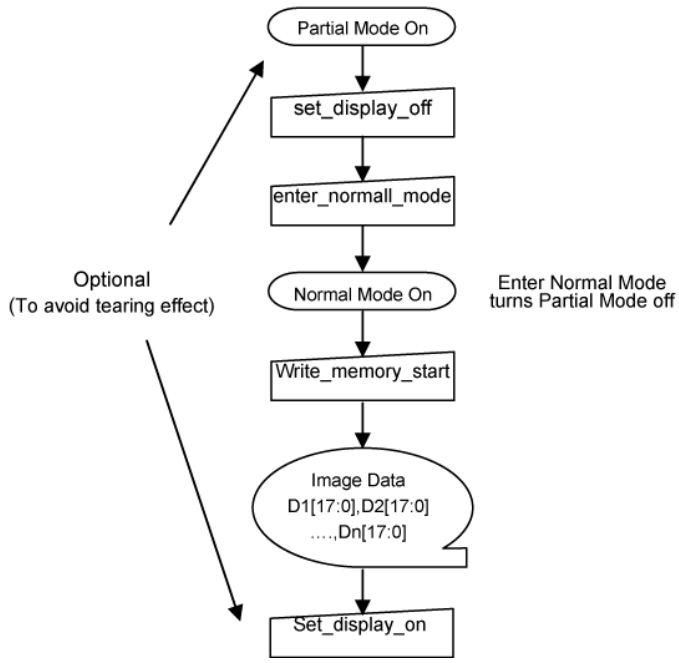
read_memory_start: 2Eh

2Eh	read_memory_start												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	0	1	1	1	0	2Eh
1st parameter	1	↑	1	D1 [17:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000… 3FF
:	1	↑	1	Dx [17:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000… 3FF
Nth parameter	1	↑	1	Dn [17:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000… 3FF
Description	This command transfers image data from the frame memory to the host processor. No status bits are changed. If this command is received, the column and page registers are set to the Start Column (SC) and Start Page (SP) respectively. After pixel data 1 is read from the frame memory at (SC, SP), address counter's direction differs depending on Bits 5, 6, 7 of set_address_mode (36h). See "Host Processor to Memory Write/Read Direction". If read operation continued after (EP, EC) data is read, the last data (EP, EC) continues to be read. Frame memory read is stopped when any other command is written. See DBI Data Format for write data formats in DBI Type B 18-/ 16-/ 9- /8- bit bus interface and Type C serial interface. X = Don't care.												
Restriction	In all color modes, the Frame read is always 18 bits so there is no restriction on the length of parameters. To execute 2Eh or 3Eh (read_memory) command, wait for 8 write cycles (66ns × 8 cycles) or more after transferring pixel data by 2Ch or 3Ch (write_memory) command. If a write cycle is 180ns or more, wait time is unnecessary.												
Flow Chart													

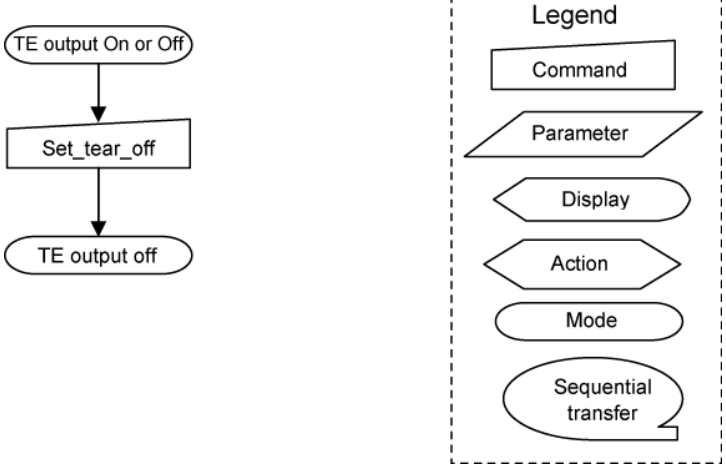
set_partial_area: 30h

30h	set_partial_area												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	0	0	0	0	30h
1st parameter	1	1	↑	x	0	0	0	0	0	0	0	SR[8]	000… 1AF
2nd parameter	1	1	↑	x	SR[7]	SR[6]	SR[5]	SR[4]	SR[3]	SR[2]	SR[1]	SR[0]	
3rd parameter	1	1	↑	x	0	0	0	0	0	0	0	ER[8]	000… 1AF
4th parameter	1	1	↑	x	ER[7]	ER[6]	ER[5]	ER[4]	ER[3]	ER[2]	ER[1]	ER[0]	

30h	set_partial_area
Description	This command defines the partial mode's display area. There are 2 commands associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. End Row > Start Row (set_address_mode(36h) B4=0)  End Row > Start Row(set_address_mode(36h) B4=1)  End Row < Start Row (set_address_mode(36h) B4=0)  End Row < Start Row (set_address_mode(36h) B4=1)  If End Row = Start Row, the partial area will be one row deep. X = Don't care.
Restriction	SR[8:0] and ER[8:0] must not be greater than 13Fh. The bits other than SR[8:0] and ER[8:0] are "Don't care".

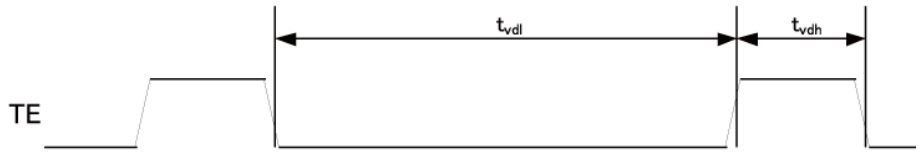
30h	set_partial_area
Flow Chart	1. To enter Partial mode  2.To exit Partial mode 

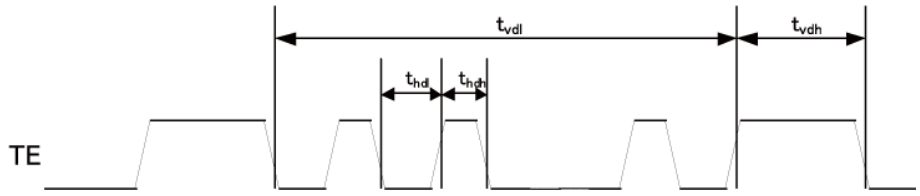
set_tear_off: 34h

34h	set_tear_off												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	0	1	0	0	34h
Parameter	None												
Description	This command turns off the Tearing Effect output signal from the TE signal line. X = Don't care												
Restriction	This command has no effect when Tearing Effect output is already off.												
Flow Chart													

set_tear_on: 35h

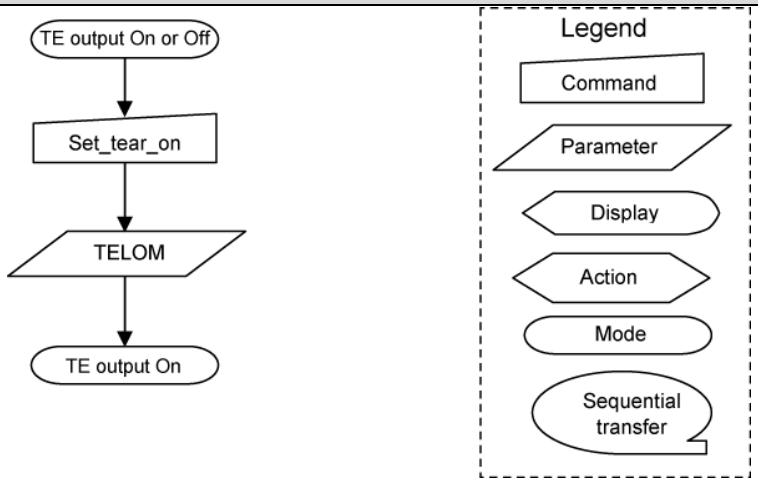
<table>
<tr><td>35h</td><td colspan="13">set_tear_on</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>TEL OM</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on the display module’s Tearing Effect output signal on the TE signal line.
The TE signal is not affected by changing set_address_mode (36h) bit B4 (Line Refresh order).
The Tearing Effect Line On has one parameter, TELOM that describes the Tearing Effect Output Line mode.
See TE Pin Output Signal“ for detail.

TELOM = 0: The Tearing Effect Output line consists of V-Blanking information only.
The Tearing Effect Output line shall be high during vertical blanking period.
 

TELOM = 1: The tearing Effect Output line consists of both V-blanking and H-blanking information.
 

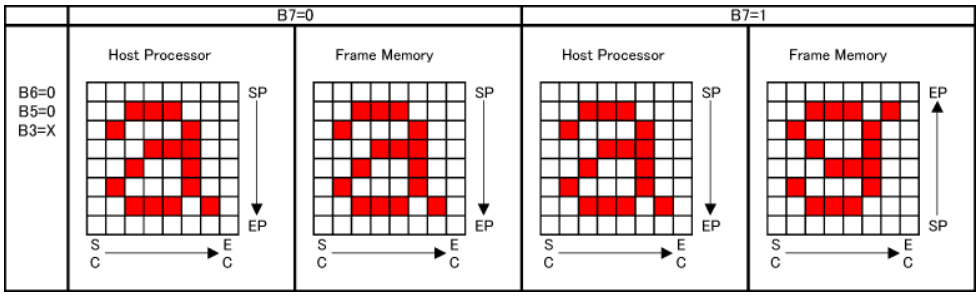
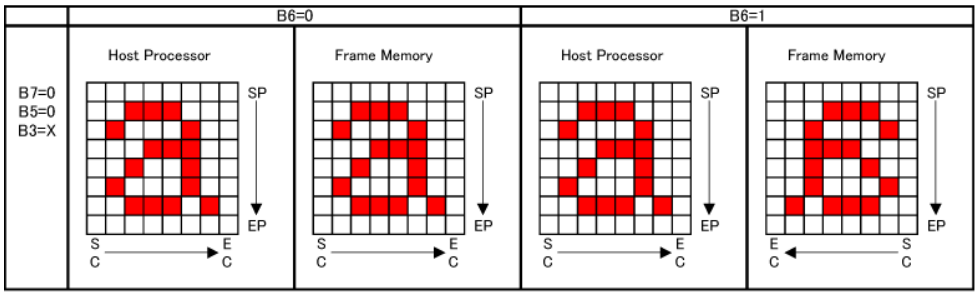
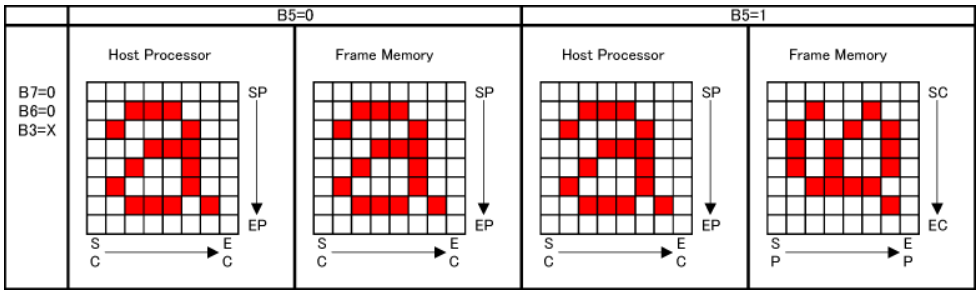
<table>
<tr><td>tvdl</td><td>Number of line defined by NL register</td></tr>
<tr><td>tvdh</td><td>Number of line defined by BP register
+ Number of line defined by FP register</td></tr>
<tr><td>thdl</td><td>3 clocks (Reference for internal operating clock)</td></tr>
<tr><td>thdh</td><td>Number of clock defined by RTN – 3 clocks
(Reference for internal operating clock)</td></tr>
</table>

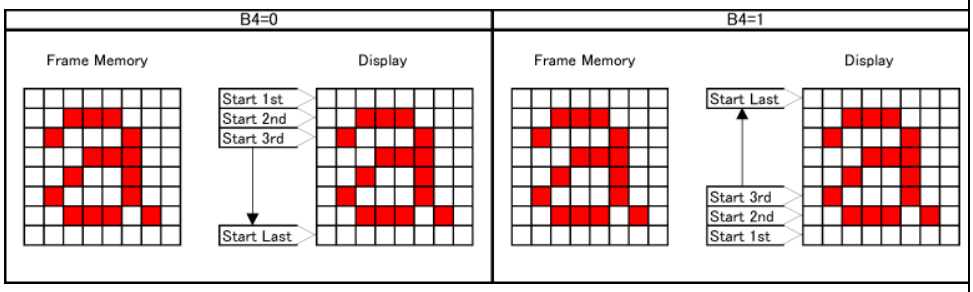
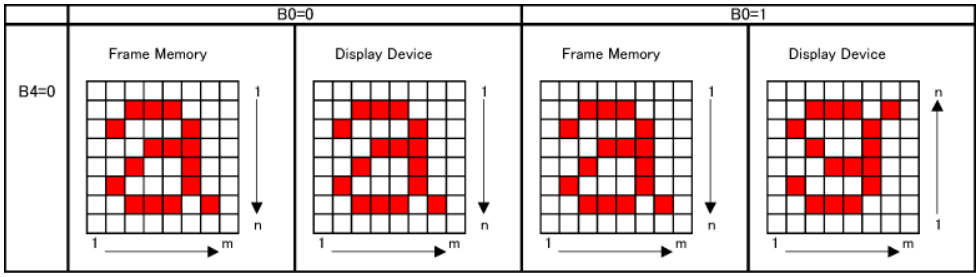
Note: The Tearing Effect Output line shall be active low when the display module is in Sleep mode.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON. Changes in parameter TELOM is enabled from the next frame period.</td></tr>
</table>

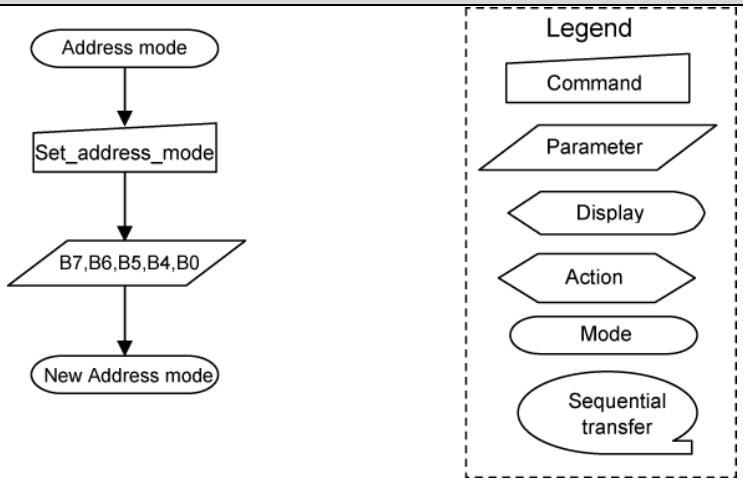
35h	set_tear_on
Flow Chart	

set_address_mode: 36h

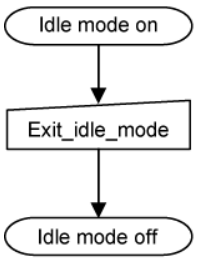
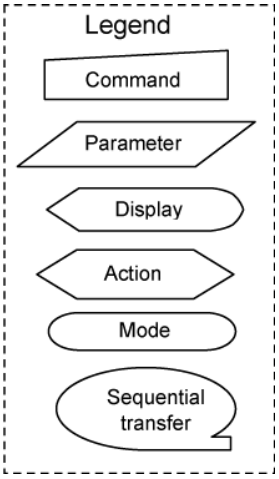
<table>
<tr><td>36h</td><td colspan="13">set_address_mode</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>36h</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>x</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>0</td><td>0</td><td>0</td><td>B0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">This command sets read/write scanning direction of frame memory. No status bits are changed.
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Symbol</th></tr>
<tr><td>D7</td><td>Page Address Order</td><td></td><td>B7</td></tr>
<tr><td>D6</td><td>Column Address Order</td><td></td><td>B6</td></tr>
<tr><td>D5</td><td>Page/Column Addressing Order</td><td></td><td>B5</td></tr>
<tr><td>D4</td><td>Display Device Line Refresh Order</td><td></td><td>B4</td></tr>
<tr><td>D3</td><td>RGB/BGR Order</td><td>Don’t care</td><td>-</td></tr>
<tr><td>D2</td><td>Display Data Latch Data Order</td><td>Don’t care</td><td>-</td></tr>
<tr><td>D1</td><td>Flip Horizontal</td><td>Don’t care</td><td>-</td></tr>
<tr><td>D0</td><td>Flip Vertical</td><td></td><td>B0</td></tr>
</table></td></tr>
</table>

36h	set_address_mode
Description	• Bit B7 - Page Address Order '0' = Top to Bottom '1' = Bottom to Top  • B6 – Column Address Order '0' = Left to Right '1' = Right to Left  • Bit B5 – Page/Column Addressing Order '0' = Normal mode '1' = Reverse Mode  See "Writing image and writing direction from the host to the frame memory" in chapter Frame Memory.

36h	set_address_mode
Description	• Bit B4 – Display Device Line Refresh Order '0' = LCD refresh Top to Bottom '1' = LCD refresh Bottom to Top (Memory reading and gate scanning directions invert simultaneously) It must be set during Seep In mode or Display Off mode.  • Bit B3 – RGB/BGR order This bit is not applicable. Set to "0". (not supported). • Bit B2 – Display Data Latch Data Order This bit is not applicable. Set to "0". (not supported). • Bit B1 – Flip Horizontal This bit is not applicable. Set to "0". (not supported). • Bit B0 – Flip Vertical '0' = Normal '1' = Flipped (gate scan order is inverted)  x = Don't care
Restriction	-

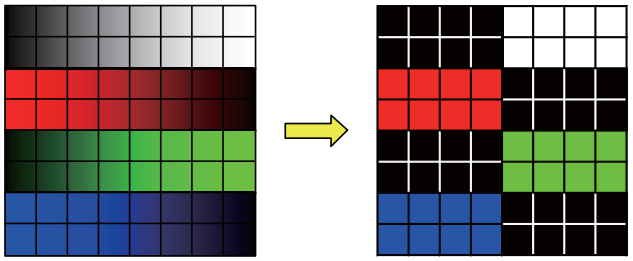
36h	set_address_mode
Flow Chart	

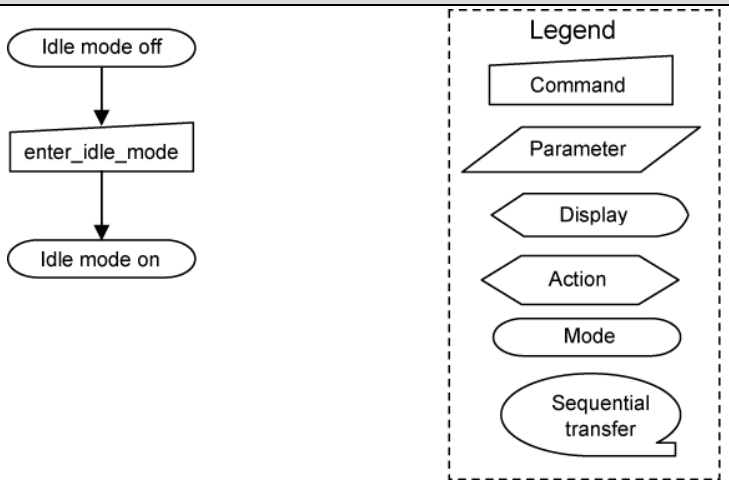
exit_idle_mode: 38h

38h	exit_idle_mode												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	1	0	0	0	38h
Parameter	None												
Description	This command causes the display module to exit Idle mode. LCD can display up to maximum 262,144 colors. If the operation of the R61526 is in synchronization with internal oscillation clock (DM=0), the frame rate and liquid crystal alternating cycle can be adjusted for every display mode (Normal, Partial, Normal+Idle, Partial+Idle modes). See description of the manufacturer commands C1h-C3h's 1st to 3rd parameters for detail. If the operation of the R61526 is in synchronization with internal oscillation clock (DM=0), the current in amplifier and step-up clock cycle can be adjusted for different display modes (Normal, Partial, Normal+Idle, Partial+Idle modes). See description of the manufacturer commands D2-D4h's 1st and 2nd parameters for detail. X = Don't care												
Restriction	This command has no effect when the display module is not in the Idle mode.												
Flow Chart	 												

enter_idle_mode: 39h

<table>
<tr><td>39h</td><td colspan="13">enter_idle_mode</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>39h</td></tr>
<tr><td>Parameter</td><td colspan="13">None</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the display module to enter Idle mode. In Idle mode, color expression is reduced. Eight color depth data is displayed using MSB of each R, G and B color components in the Frame Memory.
Only grayscale levels V0 and V63 are used while other levelsV1 to V62 are halted to reduce power consumption.
If the operation of the R61526 is in synchronization with internal oscillation clock (DM=0), the frame rate and liquid crystal alternating cycle can be adjusted for every display mode (Normal, Partial, Normal+Idle, Partial+Idle modes). See description of the manufacturer commands C1h-C3h's 1st - 3rd parameters for details.

If the operation of the R61526 is in synchronization with internal oscillation clock (DM=0), the current in amplifier and step-up clock cycle can be adjusted for different display modes (Normal, Partial, Normal+Idle, Partial+Idle modes). See description of the manufacturer commands D2-D4h's 1st and 2nd parameters for detail.
Power consumption can be minimized by optimizing Idle mode settings.
Memory Display Panel
 
<table><tr><th colspan="4">Memory contents vs Display Color</th></tr><tr><td></td><td>R5 R4 R3 R2 R1 R0</td><td>G5 G4 G3 G2 G1 G0</td><td>B5 B4 B3 B2 B1 B0</td></tr><tr><td>Black</td><td>0 X X X X X</td><td>0 X X X X X</td><td>0 X X X X X</td></tr><tr><td>Blue</td><td>0 X X X X X</td><td>0 X X X X X</td><td>1 X X X X X</td></tr><tr><td>Red</td><td>1 X X X X X</td><td>0 X X X X X</td><td>0 X X X X X</td></tr><tr><td>Magenta</td><td>1 X X X X X</td><td>0 X X X X X</td><td>1 X X X X X</td></tr><tr><td>Green</td><td>0 X X X X X</td><td>1 X X X X X</td><td>0 X X X X X</td></tr><tr><td>Cyan</td><td>0 X X X X X</td><td>1 X X X X X</td><td>1 X X X X X</td></tr><tr><td>Yellow</td><td>1 X X X X X</td><td>1 X X X X X</td><td>0 X X X X X</td></tr><tr><td>White</td><td>1 X X X X X</td><td>1 X X X X X</td><td>1 X X X X X</td></tr></table>
X = Don't care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in Idle mode.</td></tr>
</table>

39h	enter_idle_mode
Flow Chart	

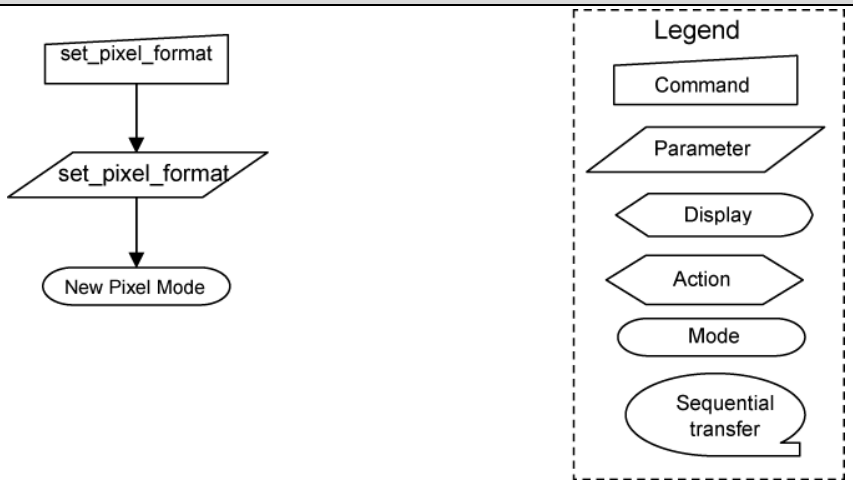
set_pixel_format: 3Ah

<table>
<tr><td>3Ah</td><td colspan="13">set_pixel_format</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3Ah</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>D6</td><td>D5</td><td>D4</td><td>0</td><td>D2</td><td>D1</td><td>D0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define the format of RGB picture data, which is to be transferred via the DBI/DPI. The formats are shown in the following table:
Bit D[6:4] – DPI Pixel Format (RGB Interface Color Format Selection)
Bit D[2:0] – DBI Pixel Format (Control Interface Color Format Selection)
Bit D7 and D3 – These bits are not applicable. Set to “0”.

<table>
<tr><th>Control Interface Color Format</th><th>D6/D2</th><th>D5/D1</th><th>D4/D0</th></tr>
<tr><td>Setting inhibited</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>3 bits/pixel (8 colors)</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Setting inhibited</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Setting inhibited</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Setting inhibited</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>16 bits/pixel (65,536 colors)</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>18 bit/pixel (262,144 colors)</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Setting inhibited</td><td>1</td><td>1</td><td>1</td></tr>
</table>
See “DBI Data Format” and “DPI Data Format”.

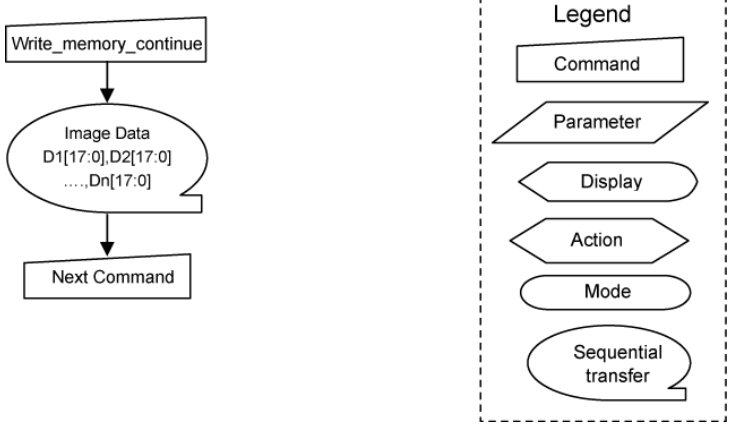
Note 1: When the setting inhibited bits are set, undesirable image will be displayed on the panel.
Note 2: Settings other than D[2:0]=5(16 bits/pixel) or 6(18 bits/pixel) are disabled in DBI Type B operation.
Note 3: Settings other than D[2:0] =1 (3 bits/pixel) and 6 (18 bits/pixel) are disabled in DBI Type C serial interface operation.
Note 4: Settings other than D[6:4]=5(16 bits/pixel) or 6(18 bits/pixel) are disabled in DPI operation.

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">There is no visible effect until the frame memory is written.</td></tr>
</table>

3Ah	set_pixel_format
Flow Chart	

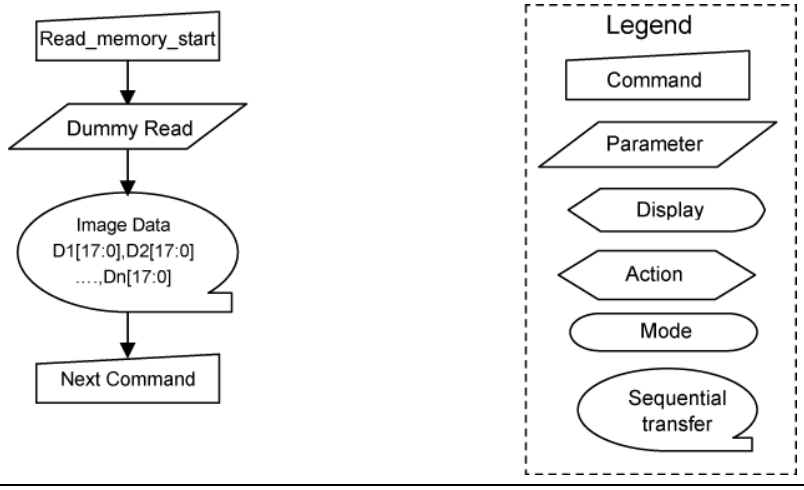
write_memory_continue: 3Ch

3Ch	write_memory_continue												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	1	1	0	0	3Ch
1st parameter	1	1	↑	D1 [17:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h … 3FFh
:	1	1	↑	Dx [17:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h … 3FFh
Nth parameter	1	1	↑	Dn [17:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h … 3FFh
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. Frame Memory Access and Interface setting (B3h): WEMODE = 0 If the number of pixels in the transfer data exceeds (EC-SC+1)x(EP-SP+1), extra pixels are ignored. Frame Memory Access and Interface setting (B3h): WEMODE = 1 When the number of pixels in the transfer data exceeds (EC-SC+1)x(EP-SP+1), the column register and the page register are reset to the Start Column/Start Page positions, and the subsequent data is written to the frame memory. X=Don't care												
Restriction	If write_memory_continue command is executed without setting set_column_address (2Ah), set_page_address (2Bh), and set_address_mode (36h), there is no guarantee that data is correctly written to the frame memory. To execute 2Eh or 3Eh (read_memory) command, wait for 8 write cycles (66ns × 8 cycles) or more after transferring pixel data by 2Ch or 3Ch (write_memory) command. If a write cycle is 180ns or more, wait time is unnecessary. To issue 2Ah command, 2Bh command, 36h command, or B3h command (WEMODE) after executing 2Ch command or 3Ch command, transfer pixel data of 10 words or more by 2Ch or 3Ch command or wait for 10 cycles (66ns × 10 cycles). If a write cycle is 180ns or more, wait time is unnecessary.												

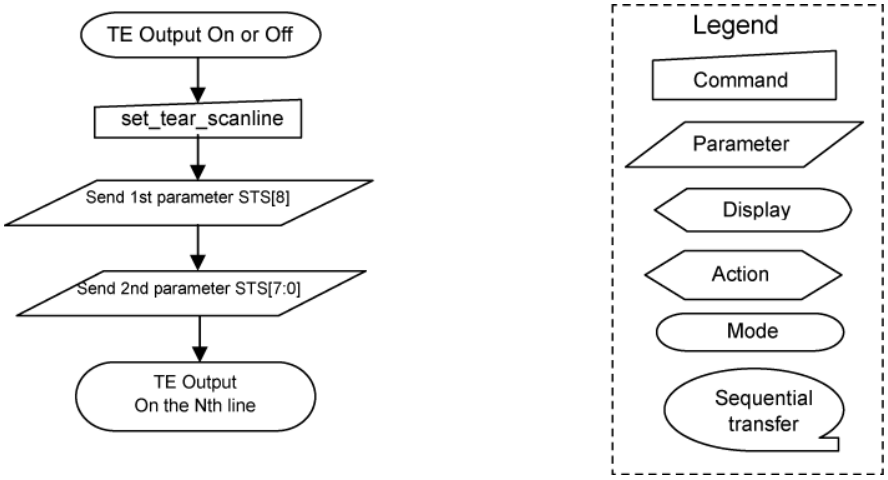
Flow Chart	

Write_memory_continue
Image Data
D1[17:0],D2[17:0]
….,Dn[17:0]
Next Command
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

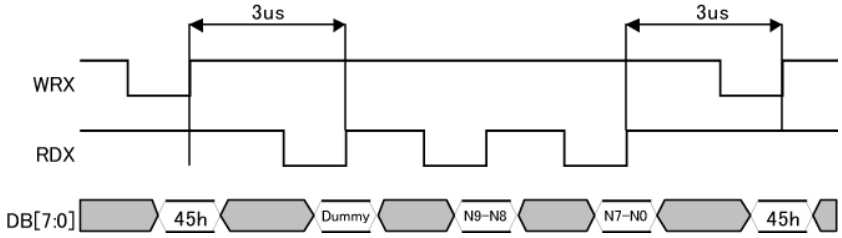
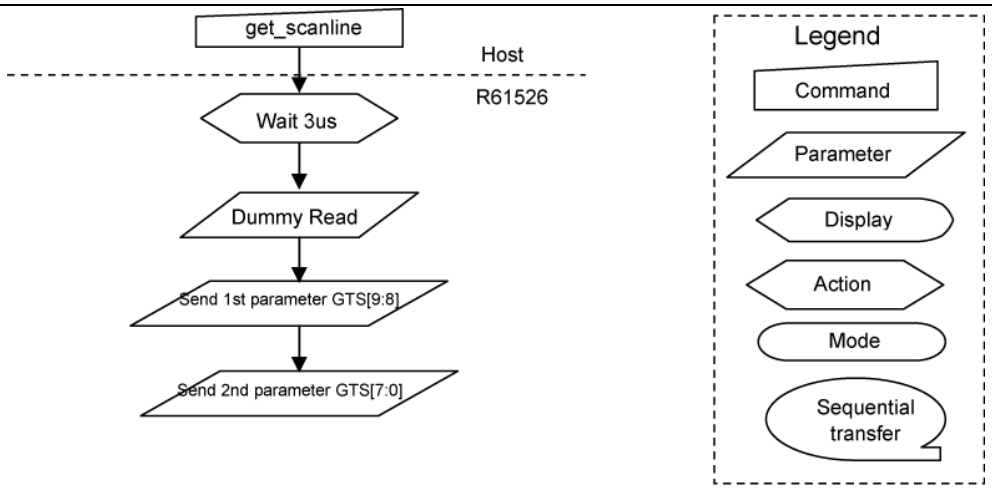
read_memory_continue:3Eh

3Eh	read_memory_continue												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	1	1	1	0	3Eh
1st Pixel data	1	↑	1	D1 [17:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h … 3FFh
:	1	↑	1	Dx [17:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h … 3FFh
Nth Pixel data	1	↑	1	Dn [17:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h … 3FFh
Description	This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command. If read operation is executed after (EP, EC) is read, the last data (EP, EC) continues to output. After pixel data 1 is written frame memory (SC, SP), address counter's direction differs depending on setting of set_address_mode (36h)'s Bits 5, 6, 7. See "Host Processor to Memory Write/Read Direction". X = Don't care												
Restriction	In any color mode, format returned by read_memory_continue is always 18 bits so there is no restriction on the length of parameter. To execute 2Eh or 3Eh (read_memory) command, wait for 8 write cycles (66ns × 8 cycles) or more after transferring pixel data by 2Ch or 3Ch (write_memory) command. If a write cycle is 180ns or more, wait time is unnecessary.												
Flow Chart													

set_tear_scanline:44h

44h	set_tear_scanline												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	0	0	0	1	0	0	44h
1st Parameter	1	1	↑	X	0	0	0	0	0	0	0	STS [8]	0Xh
2nd Parameter	1	1	↑	X	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	XXh
Description	This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N defined by STS [8:0]. TE line is unaffected by change in B4 bit of set_address_mode command. See "TE Pin Output Signal" for the relationship between bit values and waveforms. X=don't care.												
Restriction	The command takes affect on the frame following the current frame. Therefore, if the TE signal is already ON, TE signal is output according to the old set_tear_on and set_tear_scanline commands until the end of currently scanned frame. Setting is disabled when TELOM=1 of set_tear_on (35h). Make sure that STS [8:0] ≤ NL (number of line) + 1.												
Flow Chart													

get_scanline: 45h

45h	get_scanline												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	0	0	0	1	0	1	45h
1st parameter	1	↑	1	X	0	0	0	0	0	0	GTS [9]	GTS [8]	0Xh
2nd parameter	1	↑	1	X	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	XXh
Description	The display module returns the current scan line. The total number of scan lines is defined as (BP + NL + FP). The first scan line of back porch period is defined as line 0. In sleep mode, the value returned by get_scanline is undefined. X = Don't care												
Restriction	After get_line command is input, it takes 3μs or more to read it. After parameters are read, wait 3μs or more to input this command again. 												
Flow Chart													

Write Display Brightness: 51h

51h	WRDISBV (Write Display Brightness)												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	0	1	0	0	0	1	51h
1st parameter	1	1	↑	X	0	0	0	0	0	0	0	0	00h
Description	Setting inhibited. X = don't care												
Restriction	-												
Flow Chart													

Read Display Brightness Value: 52h

52h	RDDISBV (Read Display Brightness)												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	0	1	0	0	1	0	52h
1st parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
2nd parameter	1	↑	1	X	0	0	0	0	0	0	0	0	00h
Description	Setting inhibited. X = Don't care												
Restriction	-												
Flow Chart													

Write CTRL Display: 53h

53h	WRCTRLD (Write Control Display)												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	0	1	0	0	1	1	53h
1st parameter	1	1	↑	X	0	0	0	0	0	0	0	0	00h
Description	Setting inhibited. X = Don't care												
Restriction	-												
Flow Chart													

Read CTRL Value Display: 54h

54h	RDCTRLD (Read CTRL Value Display)												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	0	1	0	1	0	0	54h
1st parameter	1	1	↑	X	X	X	X	X	X	X	X	X	XXh
2nd parameter	1	1	↑	X	0	0	0	0	0	0	0	0	00h
Description	Setting inhibited. X = Don't care												
Restriction	-												
Flow Chart													

Write Content Adaptive Brightness Control: 55h

55h	WRCABC (Write Content Adaptive Brightness Control)												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	0	1	0	1	0	1	55h
1st parameter	1	1	↑	X	0	0	0	0	0	0	0	0	00h
Description	Setting inhibited. X = Don't care												
Restriction	-												
Flow Chart													

Read Content Adaptive Brightness Control: 56h

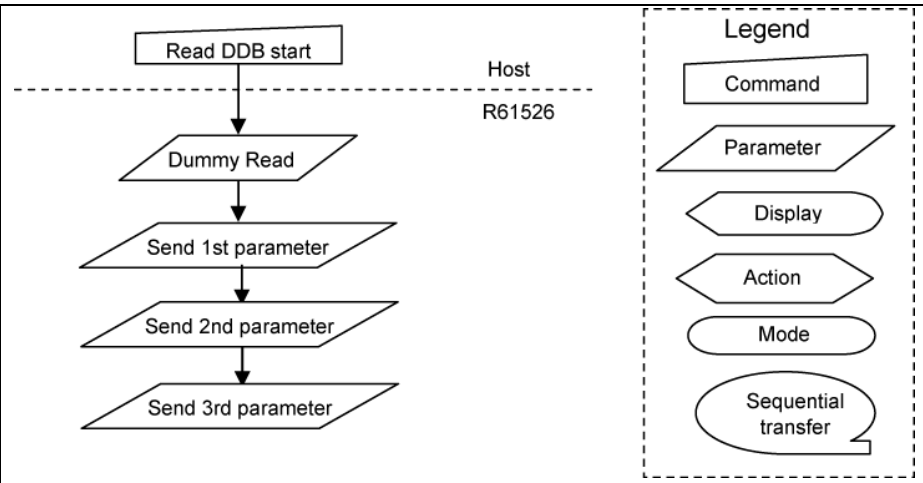
56h	RCABC (Read Content Adaptive Brightness Control)												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	0	1	0	1	1	0	56h
1st parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
2nd parameter	1	↑	1	X	0	0	0	0	0	0	0	0	00h
Description	Setting inhibited. X = Don't care												
Restriction	-												
Flow Chart													

Read Automatic Brightness Control Self-Diagnostic Result: 68h

68h	RABCSDR(Read Automatic Brightness Control Self-Diagnostic Result)												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	1	0	1	0	0	0	68h
1st parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
2nd parameter	1	↑	1	X	0	0	0	0	0	0	0	0	00h
Description	Setting inhibited. X = Don't care												
Restriction	-												
Flow Chart													

read_DDB_start: A1h

A1h	read_DDB_start												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	0	0	0	0	1	A1h
1st parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
2nd parameter	1	↑	1	X	LC MID [7]	LC MID [6]	LC MID [5]	LC MID [4]	LC MID [3]	LC MID [2]	LC MID [1]	LC MID [0]	XXh
3rd parameter	1	↑	1	X	LCD V[7]	LCD V[6]	LCD V[5]	LCD V[4]	LCD V[3]	LCD V[2]	LCD V[1]	LCD V[0]	XXh
4th parameter	1	↑	1	X	Prj ID [7]	Prj ID [6]	Prj ID [5]	Prj ID [4]	Prj ID [3]	Prj ID [2]	Prj ID [1]	Prj ID [0]	XXh
Description	This is a read only command to read the display's identification number. The 1st parameter is dummy read parameter. **LCMID** LCMID is a number to identify module manufacturer of LCM. **LCDV** LCDV is to record versions of the module and the driver. **PRJID** PRJID is to record the project and the product numbers. The above numbers and version are stored in NVM. The numbers and versions can be changed by writing data to NVM. For details, see description of NVM write operation. Values of A1h are the same as those of 04h commands. x = Don't care												
Restriction	-												

Flow Chart	

Read DDB start
Host
R61526
Dummy Read
Send 1st parameter
Send 2nd parameter
Send 3rd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

Manufacturer Command

Additional User Command:

Manufacturer Command Access Protect (B0h)

<table>
<tr><th>B0h</th><th colspan="13">MCAP(Manufacturer Command Access Protect)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB [17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B0h</td></tr>
<tr><td>1st parameter</td><td>1</td><td>#A</td><td>#B</td><td>X</td><td>0</td><td>0</td><td>MCAP B[3]</td><td>MCAP B[2]</td><td>MCAP B[1]</td><td>MCAP B[0]</td><td>MCAP [1]</td><td>MCAP [0]</td><td>XXh</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>#A</td><td>#B</td><td>X</td><td>0</td><td>0</td><td>MCAP C[5]</td><td>MCAP C[4]</td><td>MCAP C[3]</td><td>MCAP C[2]</td><td>MCAP C[1]</td><td>MCAP C[0]</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">Write #A=”1” #B=”↑”
Read #A=”↑” #B=” 1” & Insert dummy read
MCAP[1:0]
The R61526 is required to release Access Packet before inputting a Manufacturer Command. This command releases parameters so that Manufacturer Command inputs are enabled. When the conditions to release Protect, as shown in the table above, are met, Manufacturer Command inputs are enabled.
<table>
<tr><th rowspan="2">MCAP [1]</th><th rowspan="2">MCAP [0]</th><th>User Command</th><th colspan="3">Manufacturer Command</th></tr>
<tr><th>00h-A1h</th><th>B0h</th><th>B1-BFh</th><th>C0h-FFh</th></tr>
<tr><td>0</td><td>0</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
<tr><td>0</td><td>1</td><td colspan="4">Setting inhibited</td></tr>
<tr><td>1</td><td>0</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td></tr>
<tr><td>1</td><td>1</td><td>Yes</td><td>Yes</td><td>Yes</td><td>Yes</td></tr>
</table>
Yes: Access Possible (Protect Off)
No : Access Impossible (Protect On)

MCAPB[3:0]
MCAPB[3:0] has no function. Setting an arbitrary value in MCAPB[3:0] has no effect on the R61526’s operation.

MCAPC[5:0]
MCAPC[5:0] has no function. Setting an arbitrary value in MCAPC[3:0] has no effect on the R61526’s operation.

Once the R61526 enables Manufacturer Command inputs, it keeps the state until MCAP[1:0] is written so that the R61526 enters Protect ON state again.</td></tr>
<tr><td>Restriction</td><td colspan="13">After H/W Reset or exiting Deep Standby Mode, accessing a Manufacturer Command is restricted so that Manufacturer Commands B1h-BFh inputs are identified as nop command.</td></tr>
</table>

Low Power Mode Control (B1h)

B1h	Low Power Mode Control												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	0	0	0	1	B1h
1st parameter	1	#A	#B	X	0	0	0	0	0	STB [1]	STB [0]	0	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **STB[1:0]** If enter_sleep_mode (10h) command is issued after STB[1:0] is set to 2'h2, the R61526 transits to Sleep Mode. Then, the R61526 transits to deep standby mode after stopping internal logic power supply. Frame memory data and instructions are not retained in deep standby mode. Set them again after the R61526 exits deep standby mode. Do not input soft_reset command and other commands. For transition to and from deep standby mode, see "State and Command Sequence."												
Restriction	-												

Frame Memory Access and Interface Setting (B3h)

B3h	Frame Memory Access and Interface Setting												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	1	1	B3h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	WEMODE	0	XXh
2nd parameter	1	#A	#B	X	0	0	0	0	0	TEI [2]	TEI [1]	TEI [0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	0	0	DENC [2]	DENC [1]	DENC [0]	XXh
4th parameter	1	#A	#B	X	0	0	EPF [1]	EPF [0]	0	0	0	DFM	XXh
5th parameter	1	#A	#B	X	0	0	0	0	0	0	0	0	00h
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **WEMODE** After frame memory write operation reaches the end of window address area, the next position to start write is selected. WEMODE = 0: The write start position is not reset to the start of window address, and the subsequent data is disregarded. (Default) WEMODE = 1: The write start position is reset to the start of window address area to overwrite the subsequent data to the previous data.												

Description

TEI [2:0]

The bit is used to define interval between outputs of TE signal. Set in accordance with update cycle and transfer rate of the display data.

TEI[2]	TEI[1]	TEI[0]	Interval
0	0	0	Every frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other setting			Setting inhibited

DENC [2:0]

The bit is used to define Frame Memory write cycle in DPI operation. Set in accordance with update cycle of the display data.

DENC [2]	DENC [1]	DENC [0]	Frame Memory Write Cycle
0	0	0	Every frame
0	0	1	1 frame
0	1	0	2 frames
0	1	1	3 frames
1	0	0	4 frames
1	0	1	5 frames
1	1	0	6 frames
1	1	1	7 frames

EPF[1:0]

This bit is used to set data format when 16bpp (R,G,B) data is converted to 18bpp (r,g,b) and stored in internal frame memory (18bpp).

EPF is enabled when one of

1 DBI TypeB 16 bit interface (set_pixel_format (3Ah) D[2:0]=3'h5)
2 DBI TypeB 8 bit interface (set_pixel_format (3Ah) D[2:0]=3'h5)
3 DPI 16 bit interface (set_pixel_format (3Ah) D[6:4]=3'h5)

is selected. EPF is disabled in other interface operation.

Description

EPF[1:0]	Expand 16bpp(R, G, B) to 18bpp(r, g, b)
2'h0	"0" is written to LSB r[5:0]={ R[4:0], 1'h0 } g[5:0]={ G[5:0] } b[5:0]={ B[4:0], 1'h0 } Note that data is converted as follows: R[4:0], B[4:0]=5'h1F → r, b[5:0]=6'h3F G[5:0]=6'h3F → g[5:0]=6'h3F
2'h1	"1" is written to LSB r[5:0]={ R[4:0], 1'h1 } g[5:0]={ G[5:0] } b[5:0]={ B[4:0], 1'h1 } Note that data is converted as follows: R[4:0], B[4:0]=5'h0 → r, b[5:0]=6'h00 G[5:0]=6'h0 → g[5:0]=6'h00
2'h2	MSB value is written to LSB r[5:0]={ R[4:0], R[4] } g[5:0]={ G[5:0] } b[5:0]={ B[4:0], B[4] }
2'h3	Setting inhibited

DFM

The bit is used to define image data write/read format to the Frame Memory in DBI TypeB (16bit bus interface) and DBI TypeC serial interface operation. See DBI Data Format for details.

Display Mode and Frame Memory Write Mode Setting (B4h)

B4h	Display Mode and Frame Memory Write Mode Setting												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	1	0	0	B4h
1st Parameter	1	#A	#B	X	0	SD OE	0	RM	0	0	DM[1]	DM[0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read **RM** The bit is used to select an interface for the Frame Memory access operation. The Frame Memory is accessed only via the interface defined by RM bit. Because the interface can be selected separately from display operation mode, data can be written to the Frame Memory via system interface when RM = 0, even when in the DPI display operation. Wait 1 frame to transfer data after setting RM. **RM** / **Interface to access Frame Memory** 0 / DBI 1 / DPI See "Display Pixel Interface" for the sequence. **SDOE** The bit is used to regard SDA pin as an I/O pin or an input pin in DBI Type C operation. If this pin is regarded an input pin, signal is output from SDO pin. **SDOE** / **SDA pin function** 0 / I/O 1 / Input												

Description	**DM[1:0]** The bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock, VSYNC, or DPI signal. Note that switching between VSYNC and DPI operation is prohibited.

DM[1]	DM[0]	Display mode
0	0	Display operation in synchronization with internal oscillation clock
0	1	Display operation in synchronization with VSYNC
1	0	Display operation in synchronization with DPI
1	1	Setting inhibited

Device Code Read (BFh)

BFh	Device Code Read												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	1	1	1	1	BFh
1st parameter	1	↑	1	X	0	0	0	0	0	0	0	1	01h
2nd parameter	1	↑	1	X	0	0	1	0	0	0	1	0	22h
3rd parameter	1	↑	1	X	0	0	0	1	0	1	0	1	15h
4th parameter	1	↑	1	X	0	0	1	0	0	1	1	0	26h
Description	The parameters are used to read the information as follows. 1st parameter: Returns the upper byte "01h" of Renesas Technology's Supplier ID decided by MIPI Alliance. 2nd parameter: Returns the lower byte "22h" of Renesas Technology's Supplier ID decided by MIPI Alliance. 3rd parameter: Returns the upper byte "15h" of product code of this LSI. 4th parameter: Returns the lower byte "26h" of product code of this LSI. X = Don't care												
Restriction	-												

Panel Control

Panel Driving Setting (C0h)

C0h	Panel Driving Setting												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	0	0	0	C0h
1st parameter	1	#A	#B	X	0	0	1	REV	SM	GS	BGR	SS	XXh
2nd parameter	1	#A	#B	X	0	NL [6]	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	XXh
3rd parameter	1	#A	#B	X	0	SCN [6]	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]	XXh
4th parameter	1	#A	#B	X	0	0	0	1	0	0	0	0	10h
5th parameter	1	#A	#B	X	1	0	1	0	0	0	BLV	PTV	XXh
6th parameter	1	#A	#B	X	0	0	BLS	NDL	PTDC	PTS	0	0	XXh
7th parameter	1	#A	#B	X	0	0	0	PTG	ISC [3]	ISC [2]	ISC [1]	ISC [0]	XXh
8th parameter	1	#A	#B	X	0	PCD IVH [2]	PCD IVH [1]	PC DIVH [0]	0	PC DIVL [2]	PC DIVL [1]	PC DIVL [0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read												

Description

REV

The grayscale is reversed by setting REV = 1. This enables the R61526 to display the same image from the same set of data on both normally white and black panels. The source output level during the retrace period and non-lit display period is determined by register settings, BLS and NDL, respectively.

REV	Frame Memory data	Source output level in display area	
		Positive polarity	Negative polarity
0	18'h00000	V63	V0
	:	:	:
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	:	:	:
	18'h3FFFF	V63	V0

SM

SM=0: Left/right interchanging scan
SM=1: Left/right one-side scan

GS

GS=0: Forward scan
GS=1: Reverse scan

The R61526 allows changing gate driver assignment and the scan mode by combination of SM and GS bits. Set these bits in accordance with the configuration of the module. For details, see "Scan Mode Setting".

BGR

The bit is used to reverse 18-bit write data in the Frame Memory from RGB to BGR. Set in accordance with arrangement of color filters.

BGR=0: Data is written to the Frame Memory in the order of RGB. (Default)
BGR=1: Data is written to the Frame Memory in the order of BGR.

Description

SS

The bit is used to select the shifting direction of the source driver output. Set in accordance with mounting position of the R61526 to the panel.

SS=0: S1 to S720 (Default)
SS=1 S720 to S1

To change the RGB order, set SS and BGR bit.

SS=0, BGR=0: RGB
SS=1, BGR=1: BGR

NL[6:0]

These bits set the number of lines to drive the LCD at 4 line intervals. The frame memory address mapping is not affected by the number of NL[6:0]. The number of lines should be set according to the panel size.

NL[6:0]	Number of drive line
7'h00-7'h4E	Setting inhibited
7'h4F	320 lines
7'h50-7'h7F	Setting inhibited

Description

SCN[6:0]

The bit is used to set scanning start position.

SCN[6:0]	Scan start position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
7'h00	G1	G(N)	G1	G(2N－320)
Other	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited

N: Number of line(s) defined by NL[6:0].

Make sure to follow the restrictions below:

SM	GS	Restriction
0	0	(Gate scanning start position -1) + (Number of line(s) defined by NL bit) ≤ 320
0	1	Gate scanning start position ≤ 320
1	0	(Gate scanning start position -1)/2 + (Number of line(s) defined by NL bit) ≤ 320
1	1	Gate scanning start position ≤ 320

BLV

The bit selects line or frame inversion during the retrace period.

BLV=0: line inversion is selected for the retrace period when line inversion is selected by BCn=1, C1h~C3h.

BLV=1: Frame inversion is selected for the retrace period.

Check image quality on module before use.

BCn	BLV	Retrace period
0	-	Frame inversion
1	0	Line inversion
	1	Frame inversion

PTV

The bit is used to define inversion in the partial non-lit display area.

PTV=1: frame inversion is selected for the non-lit display area when line inversion is selected (BCn=1).

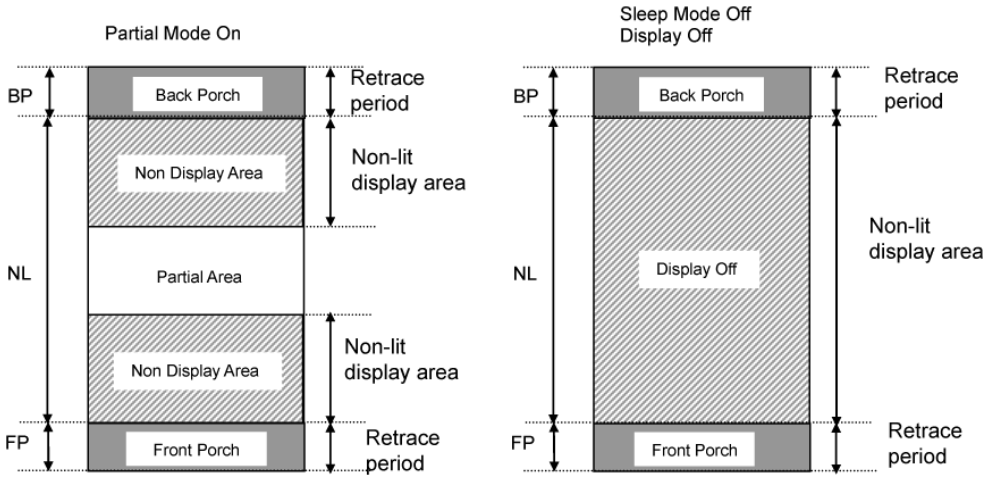
Check image quality on module before use.

BCn	PTV	Inversion in non-lit display area
0	*	Frame inversion
1	0	Line inversion
	1	Frame inversion

“Retrace period” means back and front porches.

"Non-lit display area" means:

Non-display area other than the Partial Area defined by SR[8:0] and ER[8:0].
Display area when Sleep mode is off and the display operation is off.



BLS

The bit is used to source output level in the Retrace Period. The polarity of grayscale voltage in the Retrace period is inverted.

BLS	Retrace Period	
	Positive polarity	**Negative polarity**
0	V63	V0
1	V0	V63

Description

NDL

The bit is used to define source output level in the non-lit display area. The polarity of grayscale voltage is inverted.

NDL	Non-lit display area	
	Positive polarity	Negative polarity
0	V63	V0
1	V0	V63

PTS, PTDC

The bits are used to define low-power consumption operation. PTS[1:0] defines output level in the retrace period and the non-lit display area. PTS[2] defines the operation of the grayscale amplifier and the step-up clock frequency. PTDC is used to define step-up clock frequency.

PTDC	PTS	Source output level in non-lit display area (Note)		Grayscale amplifier in non-lit display area	Step-up clock frequency in non-lit display area
		Positive polarity	Negative polarity		
0	0	V63	V0	V0 to V63	DC0n, DC1n
0	1	V63	V0	V0,V63	DC0n, DC1n
1	1	V63	V0	V0,V63	DC0n x 1/2

Note: The polarity of the source output level in non-lit display period is set by NDL (C0h). The polarity of the source output level during the retrace period is defined by BLS (C0h). If PTDC=1, step-up operation may not be executed properly depending on CD0h and RTNn values.

Description

PTG

The bit is used to select gate scan mode in non-lit display area.

PTG	Gate output in non-lit display area
0	Normal scan
1	Interval scan

Note: Set BCn=0 and select frame inversion in interval scan operation.

ISC[3:0]

The bit is used to set gate interval scan when PTG bit sets interval scan in non-lit display area. The scan interval is always of odd number. The polarity of liquid crystal drive waveform is inverted in the same timing as the interval scan.

ISC[3:0]	Scan interval	ISC[3:0]	Scan interval
4'h0	Setting inhibited	4'h8	17 frames
4'h1	3 frames	4'h9	19 frames
4'h2	5 frames	4'hA	21 frames
4'h3	7 frames	4'hB	23 frames
4'h4	9 frames	4'hC	25 frames
4'h5	11 frames	4'hD	27 frames
4'h6	13 frames	4'hE	29 frames
4'h7	15 frames	4'hF	31 frames

PCDIVH[2:0]/PCDIVL[2:0]

When the R61526's display operation is synchronized with PCLK (DM=1, DPI), internal clock for display operation switches from internal oscillation clock to PCLKD. The bits are used to define the division ratio of PCLKD to PCLK.

PCDIVH defines the number of PCLK in PCLKD=High period in units of 1 clock.
PCDIVL defines the number of PCLK in PCLKD=Low period in units of 1 clock.

Set PCDIVL=PCDIVH or PCDIVH-1.

Also, set PCDIVH and PCDIVL so that PCLKD frequency becomes the closest to internal oscillation clock frequency 800kHz.

See "Display Pixel Interface" for details in setting the bits.

Display Timing Setting for Normal / Partial Mode (C1h), Display Timing Setting for Idle Mode (C3h)

C1h	Display Timing Setting for Normal / Partial Mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	0	0	1	C1h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	BC0	XXh
2nd parameter	1	#A	#B	X	0	0	0	0	0	0	DIV 0[1]	DIV 0[0]	XXh
3rd parameter	1	#A	#B	X	0	0	RTN 0[5]	RTN 0[4]	RTN 0[3]	RTN 0[2]	RTN 0[1]	RTN 0[0]	XXh
4th parameter	1	#A	#B	X	BP0 [7]	BP0 [6]	BP0 [5]	BP0 [4]	BP0 [3]	BP0 [2]	BP0 [1]	BP0 [0]	XXh
5th parameter	1	#A	#B	X	FP0 [7]	FP0 [6]	FP0 [5]	FP0 [4]	FP0 [3]	FP0 [2]	FP0 [1]	FP0 [0]	XXh
C3h	**Display Timing Setting for Idle Mode**												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	0	1	1	C3h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	BC2	XXh
2nd parameter	1	#A	#B	X	0	0	0	0	0	0	DIV 2[1]	DIV 2[0]	XXh
3rd parameter	1	#A	#B	X	0	0	RTN 2[5]	RTN 2[4]	RTN 2[3]	RTN 2[2]	RTN 2[1]	RTN 2[0]	XXh
4th parameter	1	#A	#B	X	BP2 [7]	BP2 [6]	BP2 [5]	BP2 [4]	BP2 [3]	BP2 [2]	BP2 [1]	BP2 [0]	XXh
5th parameter	1	#A	#B	X	FP2 [7]	FP2 [6]	FP2 [5]	FP2 [4]	FP2 [3]	FP2 [2]	FP2 [1]	FP2 [0]	XXh

Description

Write #A="1" #B=" ↑ "

Read #A=" ↑ " #B=" 1" & Insert dummy read

Timings can be defined separately for different modes.
C1h: Enabled when Normal Mode On, Idle Mode Off and Partial Mode On, Idle Mode Off
C3h: Enabled when Normal Mode On, Idle Mode On and Partial Mode On, Idle Mode On

BC0, BC2

These bits define liquid crystal drive waveform inversion.

BC = 0: Frame inversion waveform is selected.
BC = 1: Line inversion waveform is selected.

For details, see "Line Inversion AC Drive".

DIV0[1:0], DIV2[1:0]

These bits set the division ratio of the internal clock frequency (DIVn). The frame frequency can be changed by DIV bit and RTNn.

The R61526's internal operation is synchronized with the clock defined by DIVn bits.

Also, reference clock width in the source delay time, VCOM inversion point gate non-overlap period settings and so on changes in accordance with DIVn setting.

For details, see "Frame Frequency Adjustment Function".

DIVn[1:0]	Division ratio of internal operation clock
2'h0	Setting inhibited
2'h1	Setting inhibited
2'h2	800kHz
2'h3	Setting inhibited

Frame frequency calculation

Frame frequency (f_{FRM}) = {fosc / (Clock per line × division ratio × (NL + FP + BP))} [Hz]

fosc: Internal clock frequency (DIVn bits)
Clocks per line: RTN bit
Line: Number of drive line(s) on the panel: NL bit
Front porch (FP): FP bit
Back porch (BP): BP bit

Description

RTN0[5:0], RTN2[5:0]

These bits set 1 line period.

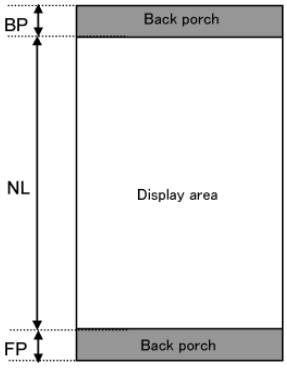
RTNn[5:0]	Clocks per line	RTNn[5:0]	Clocks per line
5'h00-5'h14	Setting inhibited	5'h2A	42 clocks
5'h15	21 clocks	5'h2B	43 clocks
5'h16	22 clocks	5'h2C	44 clocks
5'h17	23 clocks	5'h2D	45 clocks
5'h18	24 clocks	5'h2E	46 clocks
5'h19	25 clocks	5'h2F	47 clocks
5'h1A	26 clocks	5'h30	48 clocks
5'h1B	27 clocks	5'h31	49 clocks
5'h1C	28 clocks	5'h32	50 clocks
5'h1D	29 clocks	5'h33	51 clocks
5'h1E	30 clocks	5'h34	52 clocks
5'h1F	31 clocks	5'h35	53 clocks
5'h20	32 clocks	5'h36	54 clocks
5'h21	33 clocks	5'h37	55 clocks
5'h22	34 clocks	5'h38	56 clocks
5'h23	35 clocks	5'h39	57 clocks
5'h24	36 clocks	5'h3A	58 clocks
5'h25	37 clocks	5'h3B	59 clocks
5'h26	38 clocks	5'h3C	60 clocks
5'h27	39 clocks	5'h3D	61 clocks
5'h28	40 clocks	5'h3E	62 clocks
5'h29	41 clocks	5'h3F	63 clocks

FP0[7:0], FP2[7:0]
BP0[7:0], BP2[7:0]

These parameters define the retrace period (i.e. front and back porches), which appears before and after the display area. DPn bits define number of front porch lines while BPn bits define number of back porch lines.

Description

FPn[7:0], BPn[7:0]	Number of front porch lines	Number of back porch lines
8'h00	Setting inhibited	Setting inhibited
8'h01	Setting inhibited	Setting inhibited
8'h02	Setting inhibited	Setting inhibited
8'h03	Setting inhibited	Setting inhibited
8'h04	4 lines	4 lines
8'h05	5 lines	5 lines
8'h06	6 lines	6 lines
8'h07	7 lines	7 lines
8'h08	8 lines	8 lines
8'h09	9 lines	9 lines
8'h0A	10 lines	10 lines
8'h0B	11 lines	11 lines
8'h0C	12 lines	12 lines
8'h0D	13 lines	13 lines
8'h0E	14 lines	14 lines
8'h0F	15 lines	15 lines
:	:	:
8'h7F	127 lines	127 lines
8'h80	128 lines	128 lines
8'h81	Setting inhibited	Setting inhibited
:	:	:
8'hFF	Setting inhibited	Setting inhibited



Restriction

Set the BP and FP bits as follows.

BP ≥ 4 lines	FP ≥ 4 lines	FP + BP ≤ 192 lines

Display Setting commands (C1h and C3h) can be set according to display mode.

Table 26 Display Modes and Valid Register Setting

Display mode	Operation clock (DIV)	Clocks per line (RTN)	Back Porch (BP)	Front Porch (FP)	VCOM inversion cycle (BC)
(Normal / Partial mode) + Idle mode off	C1h:DIV0	C1h:RTN0	C1h:BP0	C1h:FP0	C1h:BC0
Idle mode on + (Normal / Partial mode)	C3h:DIV2	C3h:RTN2	C3h:BP2	C3h:FP2	C3h:BC2

Source/VCOM/Gate Driving Timing Setting (C4h)

C4h	Source/VCOM/Gate Driving Timing Setting												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	1	0	0	C4h
1st Parameter	1	#A	#B	X	0	SDT [2]	SDT [1]	SDT [0]	0	NOW [2]	NOW [1]	NOW [0]	XXh
2nd Parameter	1	#A	#B	X	0	0	0	0	0	MCP [2]	MCP [1]	MCP [0]	XXh
3rd Parameter	1	#A	#B	X	VEQW [3]	VEQW [2]	VEQW [1]	VEQW [0]	0	0	VEM [1]	VEM [0]	XXh
4th parameter	1	#A	#B	X	0	0	0	0	SPCW [3]	SPCW [2]	SPCW [1]	SPCW [0]	XXh
5th parameter	1	#A	#B	X	0	0	0	0	0	0	0	0	00h

Description

Write #A="1" #B="↑"

Read #A="↑" #B="1" & Insert dummy read

SDT [2:0]

The bit is used to set the source output alternating position in 1 line period.

SDT[2:0]	Source output alternating position	SDT[2:0]	Source output alternating position
3'h0	Setting inhibited	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h and C3h).

NOW[2:0]

These bits set the gate output start position (non-overlap period) in 1 line period.

NOW[2:0]	Gate output start position	NOW[2:0]	Gate output start position
3'h0	Setting inhibited	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: The unit clock here is specified according to the division ratio set by DIVn (C1h and C3h).

Description

MCP [2:0]

The bit is used to set the VCOM output alternating position in 1 line period.

MCP[2:0]	VCOM alternating position	MCP[2:0]	VCOM alternating position
3'h0	Setting inhibited	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h and C3h).

VEQW[3:0]

These bits define VCOM equalize period from VCOM change point defined by MCP[2:0] bit.

VEQW[3:0]	VCOM equalize period	VEQW[3:0]	VCOM equalize period
4'h0	0 clocks	4'h8	8 clocks
4'h1	1 clock	4'h9	9 clocks
4'h2	2 clocks	4'hA	10 clocks
4'h3	3 clocks	4'hB	11 clocks
4'h4	4 clocks	4'hC	12 clocks
4'h5	5 clocks	4'hD	13 clocks
4'h6	6 clocks	4'hE	14 clocks
4'h7	7 clocks	4'hF	15 clocks

Note 1. The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn.

Note 2. When VEM[1:0] is not 2'h0, VEQW[3:0] should not be set to 4'h0.

VEM[1:0]

VEM[0]: VCOMH equalize switch
VEM[0] = 1: When VCOMH level falls from VCOMH to VCOML level, the level first falls to the GND level and then to the VCOML level.

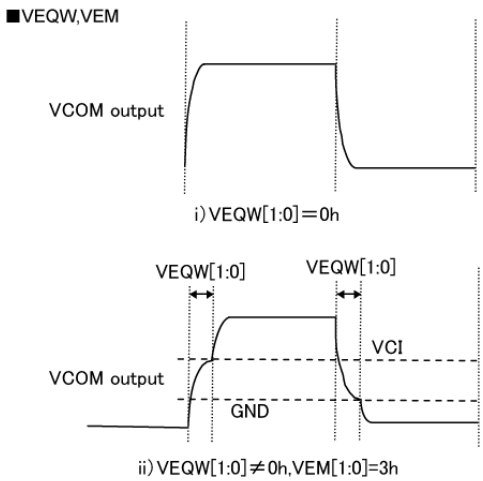
VEM[1]: VCOML equalize switch
VEM[1] = 1: When VCOMH level rises from VCOML level to VCOMH level, the level first goes up to the GND level and then to the VCOMH level.

These bits reduce power consumption during VCOM drive period. In using this function, make sure VCI < VCOMH, GND > VCOML.

VEM[1:0]	Operation
2'h0	Normal VCOM drive (No equalize)
2'h1	VCOMH equalize
2'h2	VCOML equalize
2'h3	VCOMH/VCOML equalize

When enabling VCOM function to reduce power consumption, check the display quality on the panel and effectiveness of power saving.

Description



SPCW[3:0]

The bit is used to set source pre-charge period in 1 line period. Pre-charge period is set by SPCW starting from the source output alternating position defined by SDT. Source output is precharged only on the line where liquid crystal waveform inverts.

This function realizes power consumption reduction depending on image data. Check actual image quality and effect on the panel.

SPCW[3:0]	Source precharge position	SPCW[3:0]	Source precharge position
4'h0	0 clocks (Precharge off)	4'h8	8 clocks
4'h1	1 clock	4'h9	9 clocks
4'h2	2 clocks	4'hA	10 clocks
4'h3	3 clocks	4'hB	11 clocks
4'h4	4 clocks	4'hC	12 clocks
4'h5	5 clocks	4'hD	13 clocks
4'h6	6 clocks	4'hE	14 clocks
4'h7	7 clocks	4'hF	15 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h and C3h).

Gamma Control

Gamma Set A/B/C (C8h-CAh)

C8-CAh	Gamma Set A/B/C												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	1	0	x	x	C8-CAh
1st parameter	1	1	↑	X	0	0	PRGPxP0[5]	PRGPxP0[4]	PRGPxP0[3]	PRGPxP0[2]	PRGPxP0[1]	PRGPxP0[0]	XXh
2nd parameter	1	1	↑	X	0	0	PRGPxP1[5]	PRGPxP1[4]	PRGPxP1[3]	PRGPxP1[2]	PRGPxP1[1]	PRGPxP1[0]	XXh
3rd parameter	1	1	↑	X	0	0	PRGPxP2[5]	PRGPxP2[4]	PRGPxP2[3]	PRGPxP2[2]	PRGPxP2[1]	PRGPxP2[0]	XXh
4th parameter	1	1	↑	X	0	0	PRGPxP3[5]	PRGPxP3[4]	PRGPxP3[3]	PRGPxP3[2]	PRGPxP3[1]	PRGPxP3[0]	XXh
5th parameter	1	1	↑	X	0	0	PRGPxP4[5]	PRGPxP4[4]	PRGPxP4[3]	PRGPxP4[2]	PRGPxP4[1]	PRGPxP4[0]	XXh
6th parameter	1	1	↑	X	0	0	PRGPxP5[5]	PRGPxP5[4]	PRGPxP5[3]	PRGPxP5[2]	PRGPxP5[1]	PRGPxP5[0]	XXh
7th parameter	1	1	↑	X	0	0	PRGPxP6[5]	PRGPxP6[4]	PRGPxP6[3]	PRGPxP6[2]	PRGPxP6[1]	PRGPxP6[0]	XXh
8th parameter	1	1	↑	X	0	0	PRGPxP7[5]	PRGPxP7[4]	PRGPxP7[3]	PRGPxP7[2]	PRGPxP7[1]	PRGPxP7[0]	XXh
9th parameter	1	1	↑	X	0	0	PRGPxP8[5]	PRGPxP8[4]	PRGPxP8[3]	PRGPxP8[2]	PRGPxP8[1]	PRGPxP8[0]	XXh
10th parameter	1	1	↑	X	0	0	PRBOTxP[5]	PRBOTxP[4]	PRBOTxP[3]	PRBOTxP[2]	PRBOTxP[1]	PRBOTxP[0]	XXh
11th parameter	1	1	↑	X	0	0	PIxP1[1]	PIxP1[0]	0	0	PIxP0[1]	PIxP0[0]	XXh
12th parameter	1	1	↑	X	0	0	PRGPxN0[5]	PRGPxN0[4]	PRGPxN0[3]	PRGPxN0[2]	PRGPxN0[1]	PRGPxN0[0]	XXh
13th parameter	1	1	↑	X	0	0	PRGPxN1[5]	PRGPxN1[4]	PRGPxN1[3]	PRGPxN1[2]	PRGPxN1[1]	PRGPxN1[0]	XXh
14th parameter	1	1	↑	X	0	0	PRGPxN2[5]	PRGPxN2[4]	PRGPxN2[3]	PRGPxN2[2]	PRGPxN2[1]	PRGPxN2[0]	XXh
15th parameter	1	1	↑	X	0	0	PRGPxN3[5]	PRGPxN3[4]	PRGPxN3[3]	PRGPxN3[2]	PRGPxN3[1]	PRGPxN3[0]	XXh
16th parameter	1	1	↑	X	0	0	PRGPxN4[5]	PRGPxN4[4]	PRGPxN4[3]	PRGPxN4[2]	PRGPxN4[1]	PRGPxN4[0]	XXh

17th parameter	1	1	↑	X	0	0	PRGP xN5[5]	PRGP xN5[4]	PRGP xN5[3]	PRGP xN5[2]	PRGP xN5[1]	PRGP xN5[0]	XXh
18th parameter	1	1	↑	X	0	0	PRGP xN6[5]	PRGP xN6[4]	PRGP xN6[3]	PRGP xN6[2]	PRGP xN6[1]	PRGP xN6[0]	XXh
19th parameter	1	1	↑	X	0	0	PRGP xN7[5]	PRGP xN7[4]	PRGP xN7[3]	PRGP xN7[2]	PRGP xN7[1]	PRGP xN7[0]	XXh
20th parameter	1	1	↑	X	0	0	PRGP xN8[5]	PRGP xN8[4]	PRGP xN8[3]	PRGP xN8[2]	PRGP xN8[1]	PRGP xN8[0]	XXh
21st parameter	1	1	↑	X	0	0	PRBO TxN[5]	PRBO TxN[4]	PRBO TxN[3]	PRBO TxN[2]	PRBO TxN[1]	PRBO TxN[0]	XXh
22nd parameter	1	1	↑	X	0	0	PIxN1 [1]	PIxN1 [0]	0	0	PIxN0 [1]	PIxN0 [0]	XXh

Description

Substitute a number as below table for x in register names.

Command No.	X	Example
C8h	0	PRGP0P0, PRGP0N3
C9h	1	PRGP1P0, PRGP1N3
CAh	2	PRGP2P0, PRGP2N3

・PRGPxP0—PRGPxP8、PRBOTxP
Parameters to select positive polarity. X is substituted for the numbers in the table.

・PIxP1—PIxP0
Parameters to adjust interpolation level for positive polarity. X is substituted for the numbers in the table.

・PRGPxN0—PRGPxP8、PRBOTxN
Parameters to select negative polarity. X is substituted for the numbers in the table.

・PIxN1—PIxN0
Parameters to adjust interpolation level for negative polarity. X is substituted for the numbers in the table.

See “Gamma Correction” for descriptions of each parameter.

Power Control

Power Setting (Common Setting) (D0h)

D0h	Power Setting (Common Setting)												
	DCX	RDX	WR X	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	0	0	D0h
1st parameter	1	#A	#B	X	0	BT [2]	BT [1]	BT [0]	0	0	1	1	XXh
2nd parameter	1	#A	#B	X	0	1	0	1	0	0	1	1	53h
3rd parameter	1	#A	#B	X	1	0	0	0	0	VC2 [2]	VC2 [1]	VC2 [0]	XXh
4th parameter	1	#A	#B	X	0	0	VRH [5]	VRH [4]	VRH [3]	VRH [2]	VRH [1]	VRH [0]	XXh
5th parameter	1	#A	#B	X	0	0	1	1	0	DCT [2]	DCT [1]	DCT [0]	XXh
6th parameter	1	#A	#B	X	0	0	0	0	0	0	0	0	00h

Description

Write #A="1" #B="↑"

Read #A="↑" #B="1" & Insert dummy read

BT[2:0]

The bit sets the voltage step-up factor according to selected voltage level. Smaller step-up factor leads to less power consumption.

BT[2:0]	DDVDH	VCL	VGH	VGL
3'h0	Setting inhibited			
3'h1	VCI x 2 [x 2]	-VCI [x -1]	VCI2 x 3 [x 6]	-(VCI+VCI2 x 2) [x -5]
3'h2				-(VCI2 x 2) [x -4]
3'h3				-(VCI+VCI2) [x -3]
3'h4	Setting inhibited			
3'h5	VCI x 2 [x 2]	-VCI [x -1]	VCI+VCI2 x 2 [x 5]	-(VCI+VCI2 x 2) [x -5]
3'h6				-(VCI2 x 2) [x -4]
3'h7				-(VCI+VCI2) [x -3]

Note 1: The step-up factors for VCI are shown in the brackets [].

Note 2: DDVDH is clamped so that its maximum voltage is 5.8V.

Description

VC2[2:0]: Reference voltage for internal step-up circuit 2. DDVDH is the maximum.

VC2[2:0]	VCI2
0	4.6V
1	4.8V
2	5V
3	5.2V
4	5.4V
5	5.6V
6	5.8V
7	DDVDH

VRH[5:0] Used to define VREG voltage. Set the VRH bits so that VREG ≤ DDVDH-0.5V.

VRH [5:0]	VREG	VRH [5:0]	VREG	VRH [5:0]	VREG	VRH [5:0]	VREG
5'h00	Hi-Z	5'h10	3.825	5'h20	4.225	5'h30	4.625
5'h01	3.450	5'h11	3.850	5'h21	4.250	5'h31	4.65
5'h02	3.475	5'h12	3.875	5'h22	4.275	5'h32	4.675
5'h03	3.500	5'h13	3.900	5'h23	4.300	5'h33	4.700
5'h04	3.525	5'h14	3.925	5'h24	4.325	5'h34	4.725
5'h05	3.550	5'h15	3.950	5'h25	4.350	5'h35	4.750
5'h06	3.575	5'h16	3.975	5'h26	4.375	5'h36	4.775
5'h07	3.600	5'h17	4.000	5'h27	4.400	5'h37	4.800
5'h08	3.625	5'h18	4.025	5'h28	4.425	5'h38	4.825
5'h09	3.650	5'h19	4.050	5'h29	4.450	5'h39	4.850
5'h0A	3.675	5'h1A	4.075	5'h2A	4.475	5'h3A	4.875
5'h0B	3.700	5'h1B	4.100	5'h2B	4.500	5'h3B	4.900
5'h0C	3.725	5'h1C	4.125	5'h2C	4.525	5'h3C	4.925
5'h0D	3.750	5'h1D	4.150	5'h2D	4.550	5'h3D	4.950
5'h0E	3.775	5'h1E	4.175	5'h2E	4.575	5'h3E	4.975
5'h0F	3.800	5'h1F	4.200	5'h2F	4.600	5'h3F	5.000

<table>
<tr><td>Description</td><td>DCT2[2:0]: DCDC step-up clock operation can be selected from display synchronous mode (synchronized with a start of a line or a frame) or display asynchronous mode (not synchronized with a start of a line or a frame). For details, see description of D2h command or D4h command.
<table>
<tr><th>DCT2[2:0]</th><th>DCDC step-up clock operation</th></tr>
<tr><td>3’h0</td><td>Display synchronous mode</td></tr>
<tr><td>3’h1</td><td>Display synchronous mode (Setting inhibited)</td></tr>
<tr><td>3’h2</td><td>Display synchronous mode (Setting inhibited)</td></tr>
<tr><td>3’h3</td><td>Display synchronous mode (Setting inhibited)</td></tr>
<tr><td>3’h4</td><td>Display synchronous mode (Setting inhibited)</td></tr>
<tr><td>3’h5</td><td>Display synchronous mode (Setting inhibited)</td></tr>
<tr><td>3’h6</td><td>Display synchronous mode (Setting inhibited)</td></tr>
<tr><td>3’h7</td><td>Display asynchronous mode</td></tr>
</table>
</td></tr>
</table>

VCOM Setting (D1h)

D1h	VCOM Setting												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	0	1	D1h
1st parameter	1	#A	#B	X	0	VCM [6]	VCM [5]	VCM [4]	VCM [3]	VCM [2]	VCM [1]	VCM [0]	XXh
2nd parameter	1	#A	#B	X	0	VDV [6]	VDV [5]	VDV [4]	VDV [3]	VDV [2]	VDV [1]	VDV [0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	1	0	0	0	0	10h
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read												

D1h	VCOM Setting
Description	**VCM[6:0]** The bit is used to set VCOMH voltage within the range of VREG x 0.492 ~ 1.000

VCM[6:0]	VCOMH
7'h00	Setting Inhibited
7'h01	Setting Inhibited
7'h02	Setting Inhibited
7'h03	Setting Inhibited
7'h04	Setting Inhibited
7'h05	Setting Inhibited
7'h06	Setting Inhibited
7'h07	Setting Inhibited
7'h08	Setting Inhibited
7'h09	Setting Inhibited
7'h0A	Setting Inhibited
7'h0B	Setting Inhibited
7'h0C	Setting Inhibited
7'h0D	Setting Inhibited
7'h0E	Setting Inhibited
7'h0F	Setting Inhibited
7'h10	Setting Inhibited
7'h11	Setting Inhibited
7'h12	Setting Inhibited
7'h13	Setting Inhibited
7'h14	Setting Inhibited
7'h15	Setting Inhibited
7'h16	Setting Inhibited
7'h17	Setting Inhibited
7'h18	Setting Inhibited
7'h19	Setting Inhibited
7'h1A	Setting Inhibited
7'h1B	VREG x 0.600
7'h1C	VREG x 0.604
7'h1D	VREG x 0.608
7'h1E	VREG x 0.612
7'h1F	VREG x 0.616

VCM[6:0]	VCOMH
7'h20	VREG x 0.620
7'h21	VREG x 0.624
7'h22	VREG x 0.628
7'h23	VREG x 0.632
7'h24	VREG x 0.636
7'h25	VREG x 0.640
7'h26	VREG x 0.644
7'h27	VREG x 0.648
7'h28	VREG x 0.652
7'h29	VREG x 0.656
7'h2A	VREG x 0.660
7'h2B	VREG x 0.664
7'h2C	VREG x 0.668
7'h2D	VREG x 0.672
7'h2E	VREG x 0.676
7'h2F	VREG x 0.680
7'h30	VREG x 0.684
7'h31	VREG x 0.688
7'h32	VREG x 0.692
7'h33	VREG x 0.696
7'h34	VREG x 0.700
7'h35	VREG x 0.704
7'h36	VREG x 0.708
7'h37	VREG x 0.712
7'h38	VREG x 0.716
7'h39	VREG x 0.720
7'h3A	VREG x 0.724
7'h3B	VREG x 0.728
7'h3C	VREG x 0.732
7'h3D	VREG x 0.736
7'h3E	VREG x 0.740
7'h3F	VREG x 0.744

VCM[6:0]	VCOMH
7'h40	VREG x 0.748
7'h41	VREG x 0.752
7'h42	VREG x 0.756
7'h43	VREG x 0.760
7'h44	VREG x 0.764
7'h45	VREG x 0.768
7'h46	VREG x 0.772
7'h47	VREG x 0.776
7'h48	VREG x 0.780
7'h49	VREG x 0.784
7'h4A	VREG x 0.788
7'h4B	VREG x 0.792
7'h4C	VREG x 0.796
7'h4D	VREG x 0.800
7'h4E	VREG x 0.804
7'h4F	VREG x 0.808
7'h50	VREG x 0.812
7'h51	VREG x 0.816
7'h52	VREG x 0.820
7'h53	VREG x 0.824
7'h54	VREG x 0.828
7'h55	VREG x 0.832
7'h56	VREG x 0.836
7'h57	VREG x 0.840
7'h58	VREG x 0.844
7'h59	VREG x 0.848
7'h5A	VREG x 0.852
7'h5B	VREG x 0.856
7'h5C	VREG x 0.860
7'h5D	VREG x 0.864
7'h5E	VREG x 0.868
7'h5F	VREG x 0.872

D1h	VCOM Setting
Description	

VCM[6:0]	VCOMH
7'h60	VREG x 0.876
7'h61	VREG x 0.880
7'h62	VREG x 0.884
7'h63	VREG x 0.888
7'h64	VREG x 0.892
7'h65	VREG x 0.896
7'h66	VREG x 0.900
7'h67	VREG x 0.904
7'h68	VREG x 0.908
7'h69	VREG x 0.912
7'h6A	VREG x 0.916
7'h6B	VREG x 0.920
7'h6C	VREG x 0.924
7'h6D	VREG x 0.928
7'h6E	VREG x 0.932
7'h6F	VREG x 0.936

VCM[6:0]	VCOMH
7'h70	VREG x 0.940
7'h71	VREG x 0.944
7'h72	VREG x 0.948
7'h73	VREG x 0.952
7'h74	VREG x 0.956
7'h75	VREG x 0.960
7'h76	VREG x 0.964
7'h77	VREG x 0.968
7'h78	VREG x 0.972
7'h79	VREG x 0.976
7'h7A	VREG x 0.980
7'h7B	VREG x 0.984
7'h7C	VREG x 0.988
7'h7D	VREG x 0.992
7'h7E	VREG x 0.996
7'h7F	VREG x 1.000

D1h	VCOM Setting
Description	**VDV[6:0]** The bit is used to set VCOMH alternation amplitude within the range of VREG x 0.304 ~ 1.320.

VDV[6:0]	VCOM amplitude
7'h00	Setting Inhibited
7'h01	Setting Inhibited
7'h02	Setting Inhibited
7'h03	Setting Inhibited
7'h04	Setting Inhibited
7'h05	Setting Inhibited
7'h06	Setting Inhibited
7'h07	Setting Inhibited
7'h08	Setting Inhibited
7'h09	Setting Inhibited
7'h0A	Setting Inhibited
7'h0B	Setting Inhibited
7'h0C	Setting Inhibited
7'h0D	Setting Inhibited
7'h0E	Setting Inhibited
7'h0F	Setting Inhibited
7'h10	Setting Inhibited
7'h11	Setting Inhibited
7'h12	Setting Inhibited
7'h13	Setting Inhibited
7'h14	Setting Inhibited
7'h15	Setting Inhibited
7'h16	Setting Inhibited
7'h17	Setting Inhibited
7'h18	Setting Inhibited
7'h19	Setting Inhibited
7'h1A	Setting Inhibited
7'h1B	Setting Inhibited
7'h1C	Setting Inhibited
7'h1D	Setting Inhibited
7'h1E	Setting Inhibited
7'h1F	Setting Inhibited

VDV[6:0]	VCOM amplitude
7'h20	Setting Inhibited
7'h21	Setting Inhibited
7'h22	Setting Inhibited
7'h23	Setting Inhibited
7'h24	Setting Inhibited
7'h25	VREG x 0.600
7'h26	VREG x 0.608
7'h27	VREG x 0.616
7'h28	VREG x 0.624
7'h29	VREG x 0.632
7'h2A	VREG x 0.640
7'h2B	VREG x 0.648
7'h2C	VREG x 0.656
7'h2D	VREG x 0.664
7'h2E	VREG x 0.672
7'h2F	VREG x 0.680
7'h30	VREG x 0.688
7'h31	VREG x 0.696
7'h32	VREG x 0.704
7'h33	VREG x 0.712
7'h34	VREG x 0.720
7'h35	VREG x 0.728
7'h36	VREG x 0.736
7'h37	VREG x 0.744
7'h38	VREG x 0.752
7'h39	VREG x 0.760
7'h3A	VREG x 0.768
7'h3B	VREG x 0.776
7'h3C	VREG x 0.784
7'h3D	VREG x 0.792
7'h3E	VREG x 0.800
7'h3F	VREG x 0.808

VDV[6:0]	VCOM amplitude
7'h40	VREG x 0.816
7'h41	VREG x 0.824
7'h42	VREG x 0.832
7'h43	VREG x 0.840
7'h44	VREG x 0.848
7'h45	VREG x 0.856
7'h46	VREG x 0.864
7'h47	VREG x 0.872
7'h48	VREG x 0.880
7'h49	VREG x 0.888
7'h4A	VREG x 0.896
7'h4B	VREG x 0.904
7'h4C	VREG x 0.912
7'h4D	VREG x 0.920
7'h4E	VREG x 0.928
7'h4F	VREG x 0.936
7'h50	VREG x 0.944
7'h51	VREG x 0.952
7'h52	VREG x 0.960
7'h53	VREG x 0.968
7'h54	VREG x 0.976
7'h55	VREG x 0.984
7'h56	VREG x 0.992
7'h57	VREG x 1.000
7'h58	VREG x 1.008
7'h59	VREG x 1.016
7'h5A	VREG x 1.024
7'h5B	VREG x 1.032
7'h5C	VREG x 1.040
7'h5D	VREG x 1.048
7'h5E	VREG x 1.056
7'h5F	VREG x 1.064

D1h	VCOM Setting
Description	

VDV[6:0]	VCOM amplitude
7'h60	VREG x 1.072
7'h61	VREG x 1.080
7'h62	VREG x 1.088
7'h63	VREG x 1.096
7'h64	VREG x 1.104
7'h65	VREG x 1.112
7'h66	VREG x 1.120
7'h67	VREG x 1.128
7'h68	VREG x 1.136
7'h69	VREG x 1.144
7'h6A	VREG x 1.152
7'h6B	VREG x 1.160
7'h6C	VREG x 1.168
7'h6D	VREG x 1.176
7'h6E	VREG x 1.184
7'h6F	VREG x 1.192

VDV[6:0]	VCOM amplitude
7'h70	VREG x 1.200
7'h71	VREG x 1.208
7'h72	VREG x 1.216
7'h73	VREG x 1.224
7'h74	VREG x 1.232
7'h75	VREG x 1.240
7'h76	VREG x 1.248
7'h77	VREG x 1.256
7'h78	VREG x 1.264
7'h79	VREG x 1.272
7'h7A	VREG x 1.280
7'h7B	VREG x 1.288
7'h7C	VREG x 1.296
7'h7D	VREG x 1.304
7'h7E	VREG x 1.312
7'h7F	VREG x 1.320

Power Setting for Normal/Partial Mode (D2h), Power Setting for Idle Mode (D4h)

D2h	Power Setting for Normal / Partial Mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	1	0	D2h
1st Parameter	1	#A	#B	X	0	0	0	0	0	0	0	1	01h
2nd Parameter	1	#A	#B	X	0	DC 10[2]	DC 10[1]	DC 10[0]	0	DC 00[2]	DC 00[1]	DC 00[0]	XXh
D4h	**Power Setting for Idle Mode**												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	1	0	0	D4h
1st Parameter	1	#A	#B	X	0	0	0	0	0	0	0	1	01h
2nd parameter	1	#A	#B	X	0	DC 12[2]	DC 12[1]	DC 12[0]	0	DC 02[2]	DC 02[1]	DC 02[0]	XXh
Description	Write #A="1" #B=" ↑ " Read #A=" ↑ " #B=" 1" & Insert dummy read Power control is defined for each mode. D2h is enabled when in Normal Mode and Idle Mode is exited, or when in Partial mode and Idle mode is exited. D4h is enabled when in Normal Mode and Idle Mode is exited, or when in Partial and Idle modes.												

Description

DC10[2:0], DC12[2:0]

These bits set the step-up clock frequency of the step-up circuit 2. When DCT (D0h) is set to 0h, display operation is synchronized with a start of a frame by resetting a dividing counter.

DC1n[2:0]	Step-up circuit 2 Step-up clock frequency (f_{DCDC2})	
	DCT=0h	DCT=7h
3'h0	Setting inhibited	Setting inhibited
3'h1	Setting inhibited	Setting inhibited
3'h2	Line frequency / 4	f_{OSC} / 64
3'h3	Line frequency / 8	f_{OSC} / 128
3'h4	Line frequency / 16	f_{OSC} / 256
3'h5	Setting inhibited	Setting inhibited
3'h6	Setting inhibited	Setting inhibited
3'h7	Setting inhibited (Halted)	Setting inhibited (Halted)

DC00[2:0], DC02[2:0]

These bits set the step-up clock frequency of the step-up circuits 1 and 3. When DCT (D0h) is set to 0h, display operation is synchronized with a start of a frame by resetting a dividing counter. Set a division ratio to about the number of clocks per 1H (a value set by RTN) or less.

DC0n[2:0]	Step-up circuits 1, 3 Step-up clock frequency (f_{DCDC1})	
	DCT=0h	DCT=7h
3'h0	Setting inhibited	Setting inhibited
3'h1	Setting inhibited	Setting inhibited
3'h2	f_{OSC} / 8	f_{OSC} / 8
3'h3	f_{OSC} / 16	f_{OSC} / 16
3'h4	f_{OSC} / 32	f_{OSC} / 32
3'h5	f_{OSC} / 64	f_{OSC} / 64
3'h6	f_{OSC} / 128	Setting inhibited (f_{OSC} / 128)
3'h7	Setting inhibited (Halted)	Setting inhibited (Halted)

Note: Make sure $f_{DCDC1} \geq f_{DCDC2}$.

Display Mode and Valid Register Setting

Display Mode	Step-up circuits 1 and 3 Step-up clock frequency	Step-up circuit 2 Step-up clock frequency
(Normal / Partial mode) + Idle mode off	D2h:DC00	D2h:DC10
Idle mode on + (Normal / Partial mode)	D4h:DC02	D4h:DC12

NVM Control

NVM Access Control (E0h)

E0h	NVM Access Control												
	DCX	RDX	WRX	DB [15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	0	0	0	0	E0h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	NVAE	00h
2nd parameter	1	#A	#B	X	0	FTT	0	0	0	0	0	0	00h
3rd parameter	1	#A	#B	X	0	VERIFLGER	0	VERIFLGWR	0	0	0	TEM [0]	00h
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read												

NVAE: NVM access enable register. NVM access is enabled when NVAE=1.

FTT: NVM control bit. FTT=1 triggers NVM erase and write. CALB=0 is returned when NVM Memory Write&Verify is finished.

VERIFLGER: This bit is for read only. Write data to this bit is ignored.

To execute NVM write, an erase and an erase verify is executed in advance. This bit is used to return the result of erase verify.

Erase verify "Pass": VERIFLGER = 1
Erase verify "Fail": VERIFLGER = 0

VERIFLGWR: This bit is for read only. Write data to this bit is ignored.

After NVM data erase, a write and a write verify is executed, This bit is used to return the result of write verify.

Write verify "Pass": VERIFLGWR = 1
Write verify "Fail": VERIFLGWR = 0

State diagram of VERIFLGER, VERIFLGWR bit

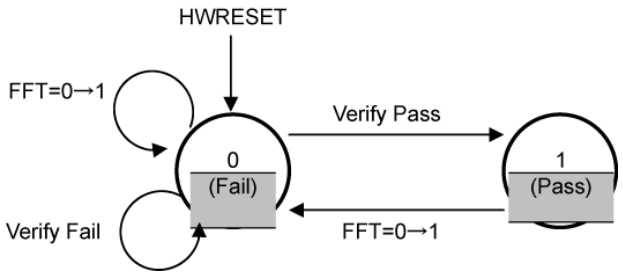


Figure 28

TEM: Used to define output from TE pin.

Table 27

TEM	TE output
1'h0	Tearing Effect
1'h1	NV automatically write data verification result (VERIFLGER&VERIFLGWR) TE = 0 Verification result is unsatisfactory. TE = 1 Verification result is satisfactory.

Note: When in the Sleep mode, and Tearing Effect signal is off (set_tear_off), TE pin output is always "Low".

set_DDB_write_control (E1h)

E1h	set_DDB_write_control												
	DCX	RDX	WRX	DB [15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	0	0	0	1	E1h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	WCDDB	00h
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read												

WCDDB:

WCDDB=1 Data can be written to LCMID[7:0], LCDV[7:0], and PRJID[7:0] (04h and A1h). The bit values can be written to the NVM.

WCDDB=0 Data cannot be written to LCMID[7:0], LCDV[7:0], and PRJID[7:0] (04h and A1h). Set WCDDB=0 when not executing NVM write operation.

NVM Load Control (E2h)

E2h	NVM Load Control												
	DCX	RDX	WRX	DB [15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	0	0	1	0	E2h
1st parameter	1	#A	#B	X	0	0	LD [5]	LD [4]	LD [3]	LD [2]	LD [1]	LD [0]	00h
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read												

LD[5:0]: Selects a command used to execute a data load from NVM.

LD[x] = 0: Data load from NVM is performed. NVM data is updated.

LD[x] = 1: Data load from NVM is not performed. NVM data is not updated but old data is retained.

**h LDx (E2h) controls commands used to load data from NVM.

LD0 : User Command : 04h, A1h
LD1 : Manufacturer Command : B3~B4h (I/F and Frame Memory Control)
LD2 : Manufacturer Command : None.
LD3 : Manufacturer Command : C0~C4h (Panel Drive and Display Timing Setting)
LD4 : Manufacturer Command : D0~D4h (Power Setting)
LD5 : Manufacturer Command : C8~CAh (Gamma Setting)

Interface Control

Read Mode In (F0h)

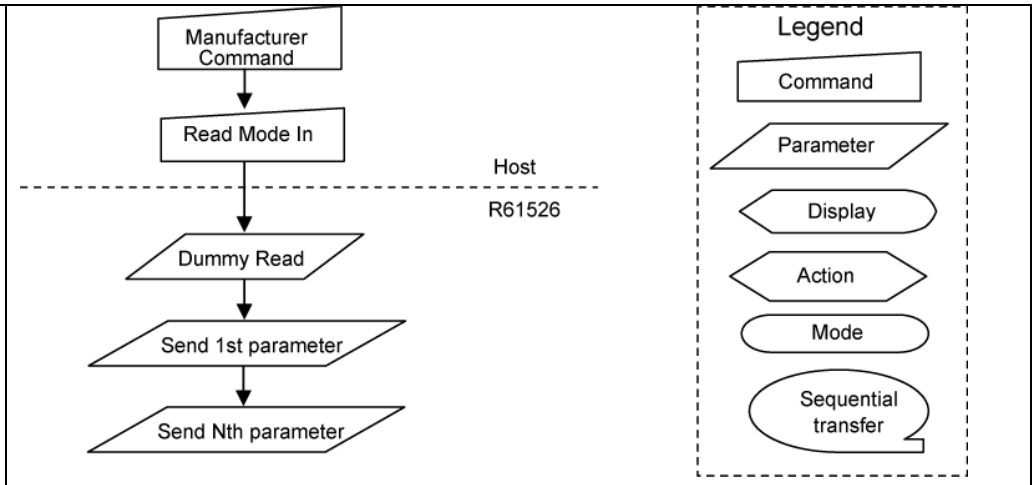
F0h	Read Mode In												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	1	0	0	0	0	F0h

This command is used to read write/read registers categorized as Manufacturer Commands when DBI TypeC-I/F is selected.

A read is performed after writing this command. The read operation is cancelled when CSX=High and a write is performed after the following CSX=Low.

See below table to check if this command is required or not for each command.

Operational Code (Hex)	Commend	Read Mode In Command Required or not
B0h	Manufacturer Command Access Protect	Yes
B3h	Frame Memory Access and Interface Setting	Yes
B4h	Display Mode and Frame Memory Write Mode Setting	Yes
BFh	Device Code Read	No
C0h	Panel Driving Setting	Yes
C1h	Display Timing Setting for Normal/Partial Mode	Yes
C3h	Display Timing Setting for Idle Mode	Yes
C4h	Source/VCOM/Gate Driving Timing Setting	Yes
C8h	Gamma Set A	Yes
C9h	Gamma Set B	Yes
CAh	Gamma Set C	Yes
D0h	Power Setting (Common Setting)	Yes
D1h	VCOM Setting	Yes
D2h	Power Setting for Normal/Partial Mode	Yes
D4h	Power Setting for Idle Mode	Yes
E0h	NVM Access Control	Yes
E1h	NVM Write Data	Yes
E2h	NVM Data Load Register	Yes
F0h	Read Mode In	–

Flow Chart	

Manufacturer Command
Read Mode In
Host
R61526
Dummy Read
Send 1st parameter
Send Nth parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

State Transition Diagram

Definition of Display Operation Mode

The definition of the R61526's state transition (display operation mode) is compliant with MIPI DCS.

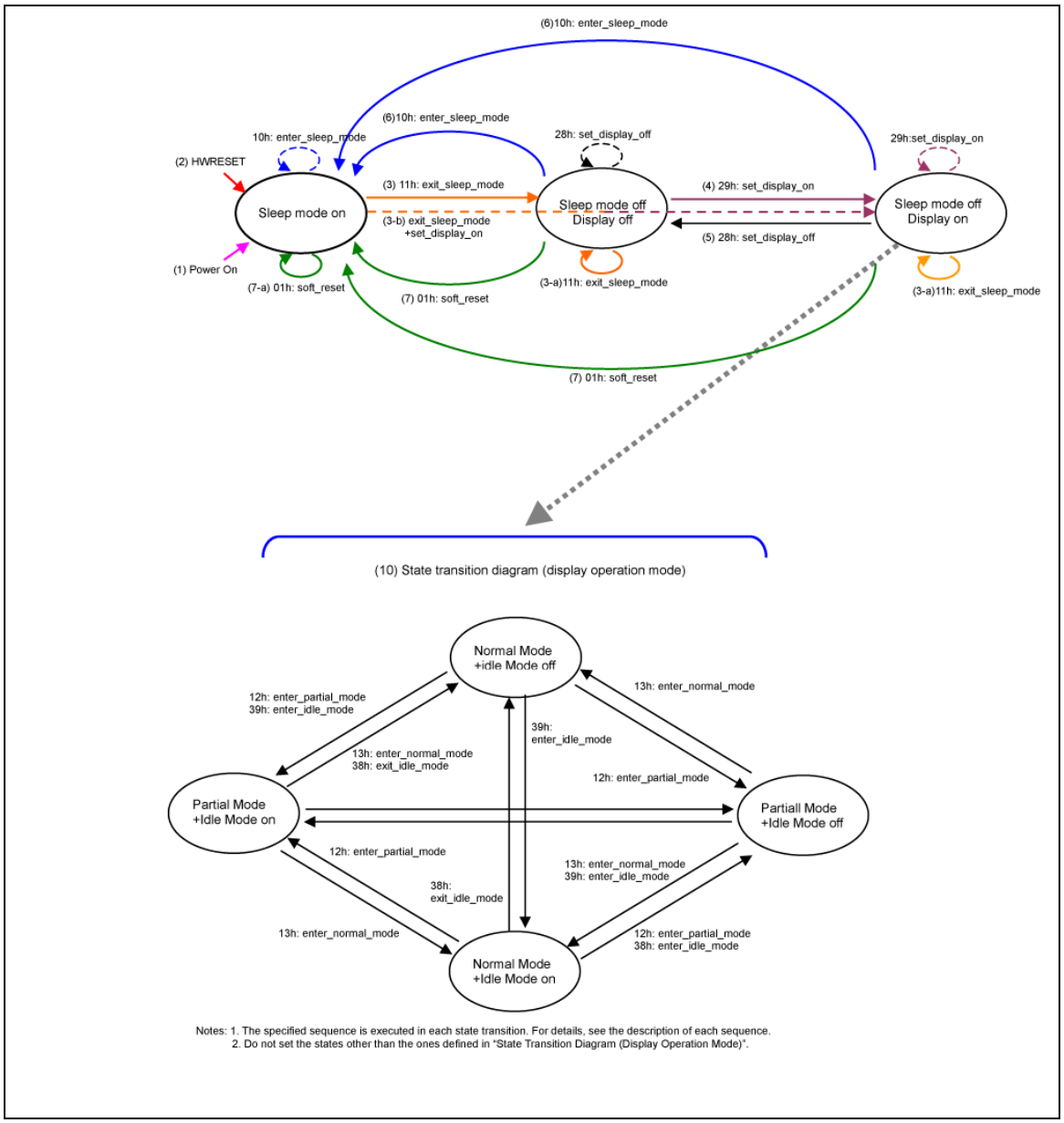


Figure 29

Table 28 Operation Mode Transition Sequence

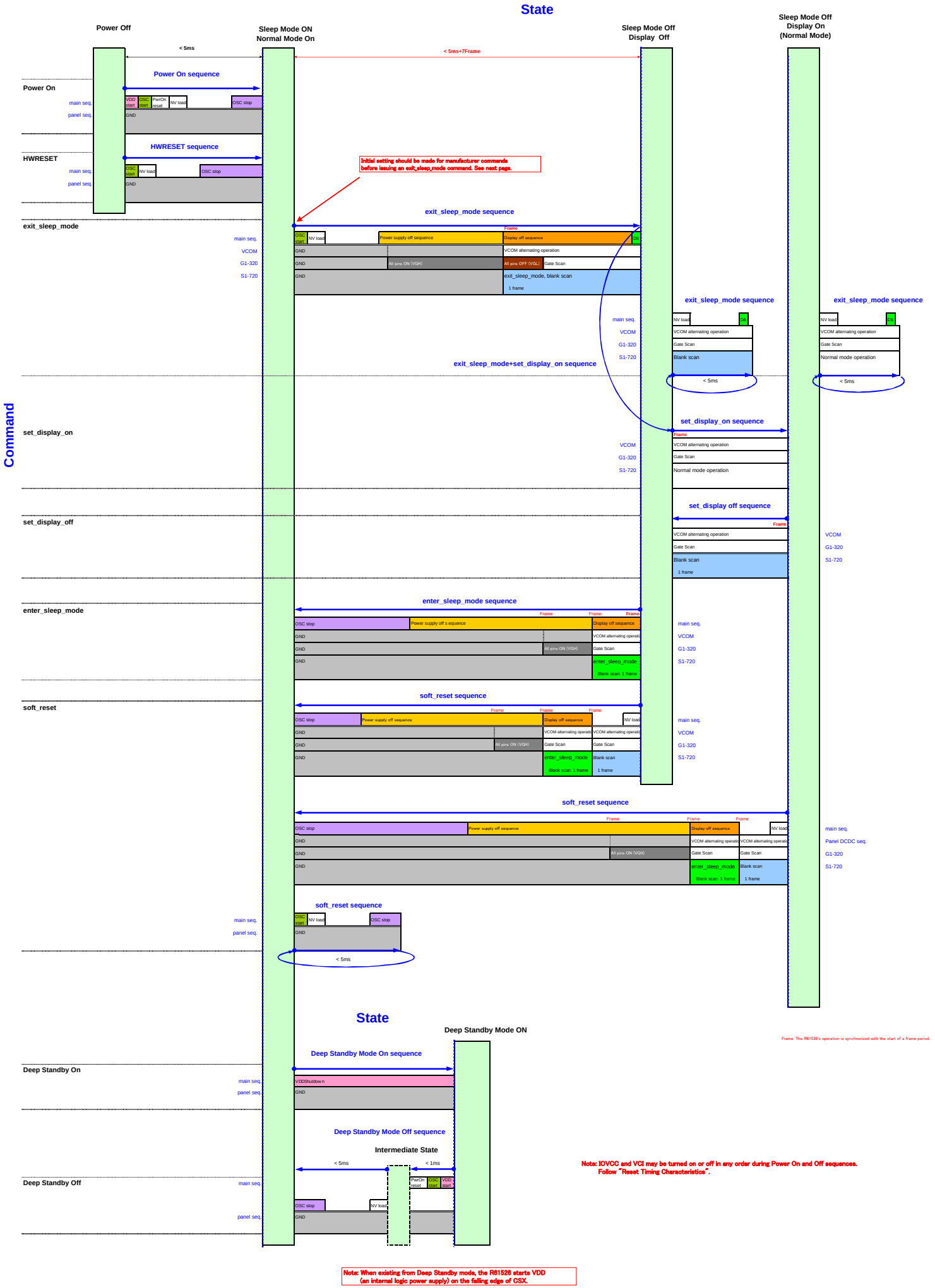
Sequence		Command	State	
			From	To
(1)	Power on sequence	-	-	Sleep mode on
(2)	HWRESET sequence	-	-	Sleep mode on
(3)	exit_sleep_mode sequence	11h: exit_sleep_mode	Sleep mode on	Sleep out Display off
(3-a)			Sleep mode off Display off/on	Sleep mode off Display off/on
(3-b)	exit_sleep_mode sequence + display_on sequence	11h: exit_sleep_mode	Sleep mode on	Sleep mode off Display on
(4)	set_display_on sequence	29h: set_display on	Sleep mode off Display off	Sleep mode off Display on
(5)	set_display_off sequence	28h: set_display_off	Sleep mode off Display on	Sleep mode off Display off
(6)	enter_sleep_mode sequence	10h: enter_sleep_mode	Sleep mode off Display off/on	Sleep mode on
(7)	soft_reset sequence	01h: soft_reset	Sleep out Display off/on	Sleep mode on
(7-a)			Sleep mode on	Sleep mode on

Table 29 Display Mode Transition Sequence

Sequence		Command	State	
			From	To
(10)	Display mode sequence	12h: enter_partial_mode 13h: enter_normal_mode 38h: exit_idle_mode 39h: enter_idle_mode	Previous display mode (Normal/Partial/Idle)	Target display mode (Normal/Partial/Idle)

■ R61526 State & Command sequence

Rev.1 2010.02.01



Example: Power and Display On/Off Sequences

Without NVM

The power and display sequences in which Manufacturer Command is not written to the internal NVM is shown below.

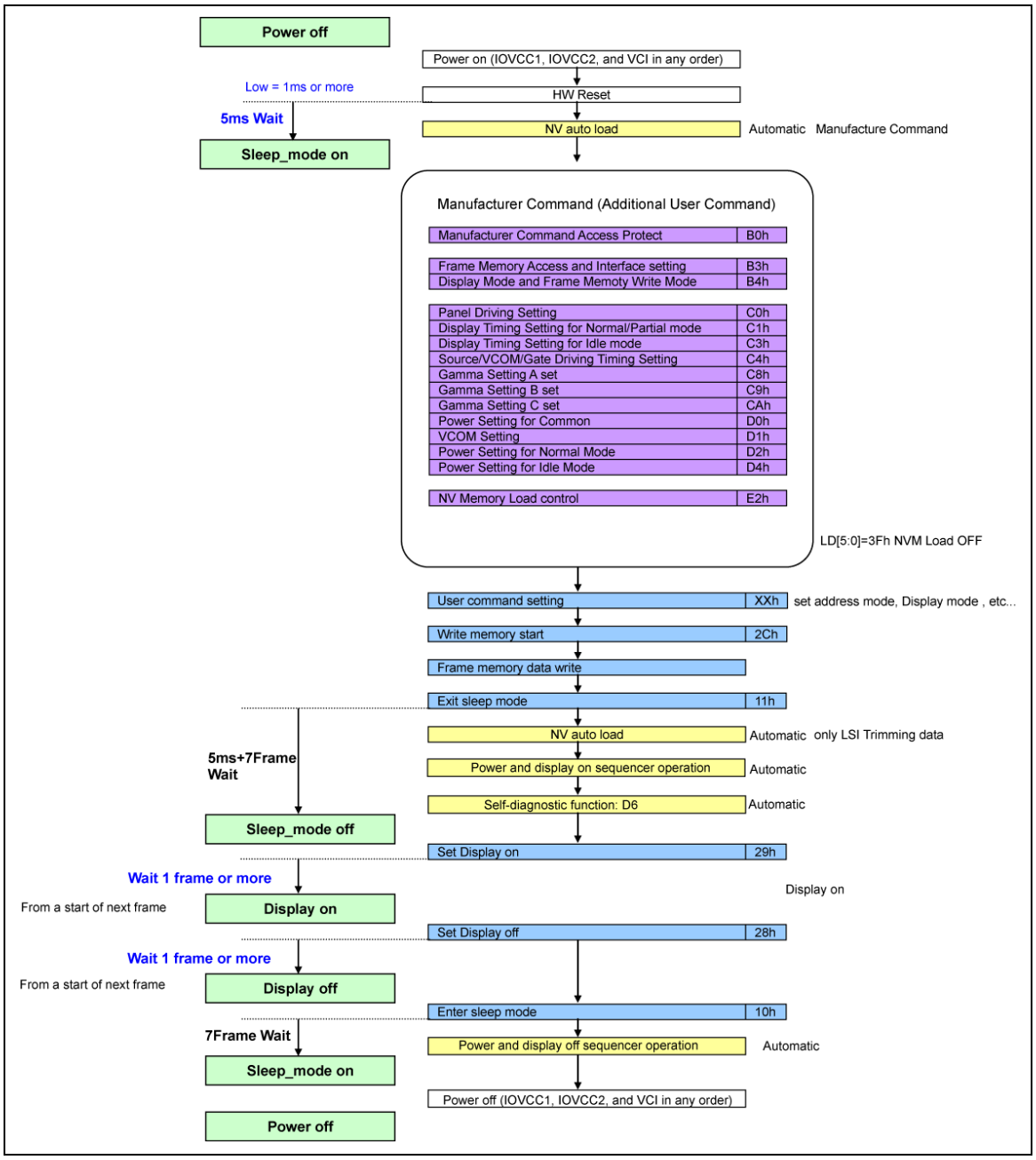


Figure 30

With NVM

The power and display sequences in which Manufacturer Command is not written to the internal NVM is shown below. Using only User Command can turn power and display on.

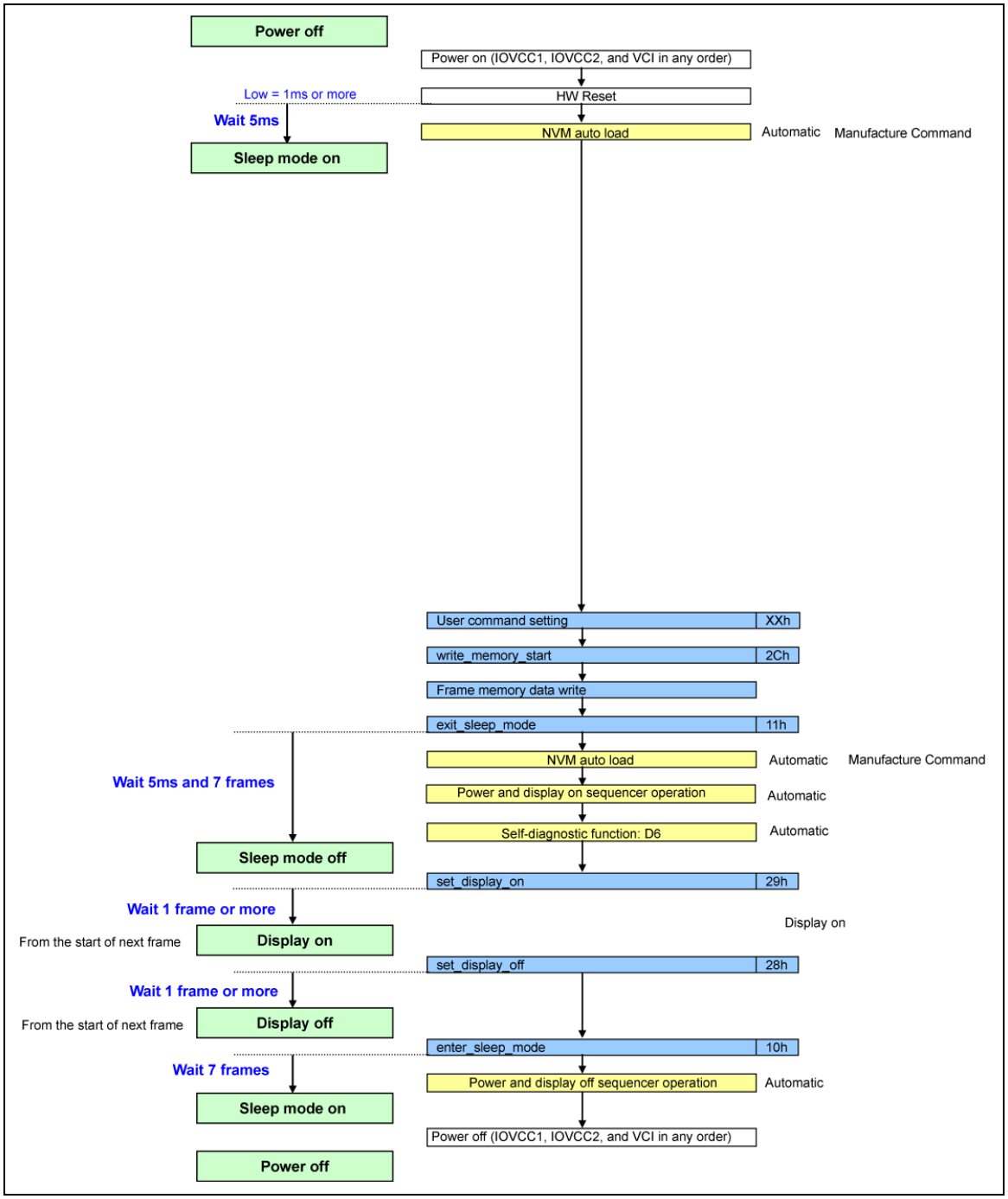


Figure 31

Command	Type	Value(HEX)	Comment
Manufacturer Command Access Protect	**C**	**B0**	
	P1	00	
	P2	00	
Low Power Mode Control	**C**	**B1**	
	P1	00	
Frame Memory Access and Interface setting	**C**	**B3**	**(Note 1)**
	P1	00	
	P2	00	
	P3	00	
	P4	00	
	P5	00	
Display Mode and Frame Memory Write Mode Setting	**C**	**B4**	**(Note 1)**
	P1	00	
Device Code Read	**C**	**BF**	**Read only**
	P1	xx	
	P2	01	
	P3	22	
	P4	15	
	P5	26	
Panel Driving Setting	**C**	**C0**	**(Note 1)**
	P1	00	
	P2	4F	
	P3	00	
	P4	10	
	P5	A2	
	P6	00	
	P7	01	
	P8	00	
Display Timing Setting for Normal/Partial Mode	**C**	**C1**	**(Note 1)**
	P1	01	
	P2	02	
	P3	28	
	P4	08	
	P5	08	
Display Timing Setting for Idle Mode	**C**	**C3**	**(Note 1)**
	P1	01	
	P2	02	
	P3	28	
	P4	08	
	P5	08	
Source/VCOM/Gate Driving Timing Setting	**C**	**C4**	**(Note 1)**
	P1	11	
	P2	01	
	P3	00	
	P4	00	
	P5	00	
Gamma Set A	**C**	**C8**	**(Note 1)**
	P1	00	
	P2	00	
	P3	00	
	P4	00	
	P5	00	
	P6	00	
	P7	00	
	P8	00	
	P9	00	
	P10	00	
	P11	00	
	P12	00	
	P13	00	
	P14	00	
	P15	00	
	P16	00	
	P17	00	
	P18	00	
	P19	00	
	P20	00	
	P21	00	
	P22	00	
Gamma Set B	**C**	**C9**	**(Note 1)**
	P1	00	
	P2	00	
	P3	00	
	P4	00	
	P5	00	
	P6	00	
	P7	00	
	P8	00	
	P9	00	
	P10	00	
	P11	00	
	P12	00	
	P13	00	
	P14	00	
	P15	00	
	P16	00	
	P17	00	
	P18	00	
	P19	00	
	P20	00	
	P21	00	
	P22	00	

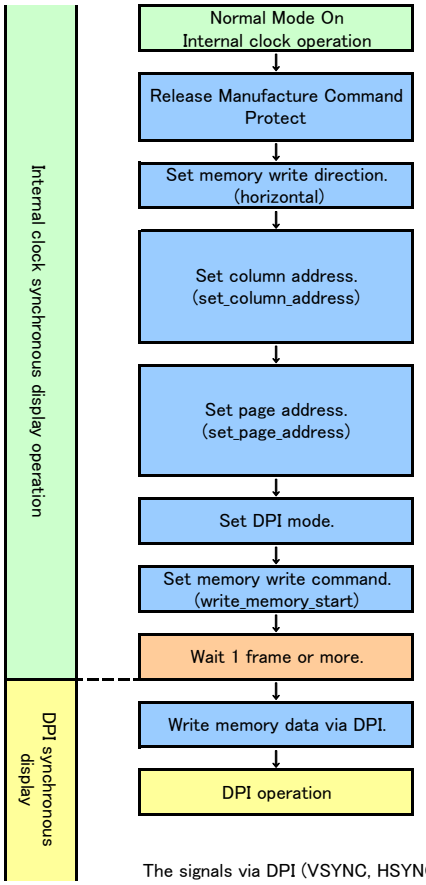
Command	Type	Value(HEX)	Comment
Gamma Set C	**C**	**CA**	**(Note 1)**
	P1	00	
	P2	00	
	P3	00	
	P4	00	
	P5	00	
	P6	00	
	P7	00	
	P8	00	
	P9	00	
	P10	00	
	P11	00	
	P12	00	
	P13	00	
	P14	00	
	P15	00	
	P16	00	
	P17	00	
	P18	00	
	P19	00	
	P20	00	
	P21	00	
	P22	00	
Power Setting (Common Setting)	**C**	**D0**	**(Note 1)**
	P1	63	
	P2	53	
	P3	82	
	P4	3F	
	P5	37	
	P6	00	
VCOM Setting	C	**D1**	**(Note 1)**
	P1	7F	
	P2	00	
	P3	10	
Power Setting for Normal/Partial Mode	**C**	**D2**	**(Note 1)**
	P1	01	
	P2	24	
Power Setting for Idle Mode	**C**	**D4**	**(Note 1)**
	P1	01	
	P2	24	
Test Mode	**C**	**D6**	
	P1	01	
	P2	03	
	P3	62	
Test Mode	**C**	**D7**	
	P1	01	
	P2	02	
	P3	59	
	P4	AC	
	P5	07	
	P6	0C	
	P7	B2	
	P8	0C	
Test Mode	**C**	**D8**	
	P1	44	
	P2	44	
	P3	44	
	P4	40	
	P5	24	
	P6	06	
	P7	02	
	P8	00	
Test Mode	**C**	**D9**	
	P1	FF	
	P2	1F	
NV Memory Access Control	**C**	**E0**	
	P1	00	
	P2	00	
	P3	00	
set DDB Write control	**C**	**E1**	
	P1	00	
NV Memory Load control	**C**	**E2**	
	P1	00	
Test Mode	**C**	**E3**	
	P1	00	
Test Mode	**C**	**E4**	
	P1	00	
	P2	00	
	P3	22	
	P4	AA	
	P5	00	
Test Mode	**C**	**E5**	
	P1	00	
Test Mode	**C**	**F4**	
	P1	00	
Test Mode	**C**	**FA**	
	P1	04	
	P2	00	
	P3	00	
	P4	00	
	P5	30	
Test Mode	**C**	**FC**	
	P1	00	
	P2	80	
	P3	07	
	P4	00	
	P5	00	
	P6	00	
Test Mode	**C**	**FD**	
	P1	00	
	P2	02	
	P3	00	
	P4	00	
	P5	00	
Test Mode	**C**	**FE**	
	P1	00	
	P2	00	
	P3	00	
	P4	01	
	P5	00	
	P6	00	
	P7	00	
	P8	00	
	P9	00	

Notes: 1. When reset is executed, a register value written to NVM is loaded from it. The above values are set in the registers as defaults. If a user change a default, the value is written to NVM, and loaded from NVM when reset is executed.

2. To prevent malfunction caused by external noise, setting the above values in registers including test registers when power on sequence, deep standby off sequence, or refresh sequence is executed.

■Transition Sequence between Internal Clock Operation and DPI Display Operation

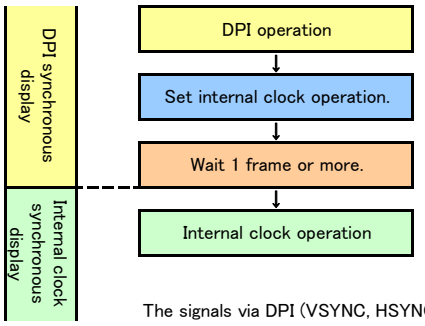
(1) From internal clock operation to DPI operation



Command	B0h
1st Parameter	MCAP1=6'h3F
Command	36h
1st Parameter	B5=1'h0
Command	2Ah
1st Parameter	SC[8]=1'hX
2nd Parameter	SC[7:0]=8'hXX
3rd Parameter	EC[8]=1'hX
4th Parameter	EC[7:0]=8'hXX
Command	2Bh
1st Parameter	SP[8]=1'hX
2nd Parameter	SP[7:0]=8'hXX
3rd Parameter	EP[8]=1'hX
4th Parameter	EP[7:0]=8'hXX
Command	B4h
1st Parameter	12h (RM=1, DM[1:0]=2'h2)
Command	2Ch

The signals via DPI (VSYNC, HSYNC, DOTCLK, ENABLE, and DB[0:17]) should be input before DM and RM are written.

(2) From DPI operation to internal clock operation

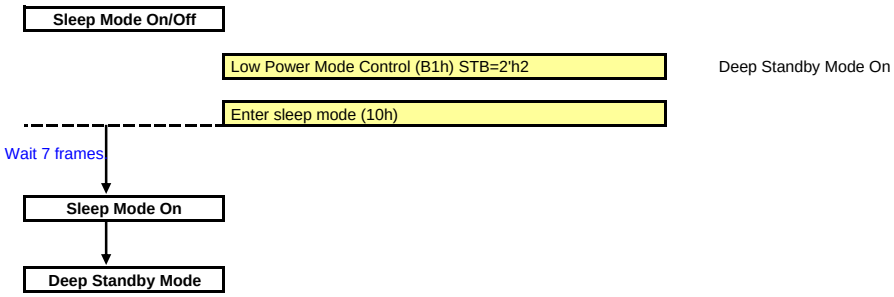


Command	B4h
1st Parameter	00h (RM=0, DM[1:0]=2'h0)

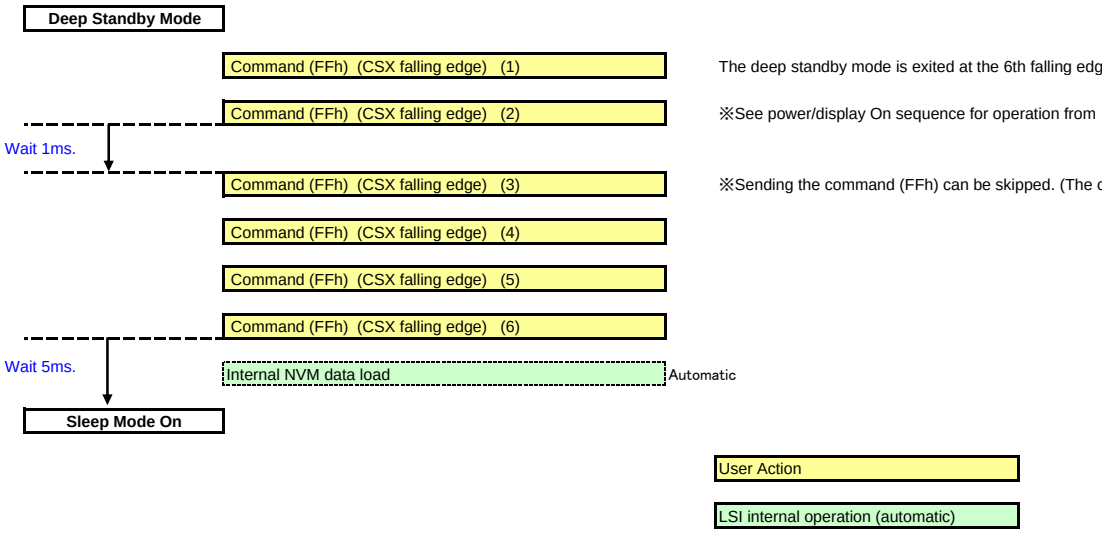
The signals via DPI (VSYNC, HSYNC, DOTCLK, ENABLE, and DB[0:17]) should continue for 2 frames after DM and RM are written.

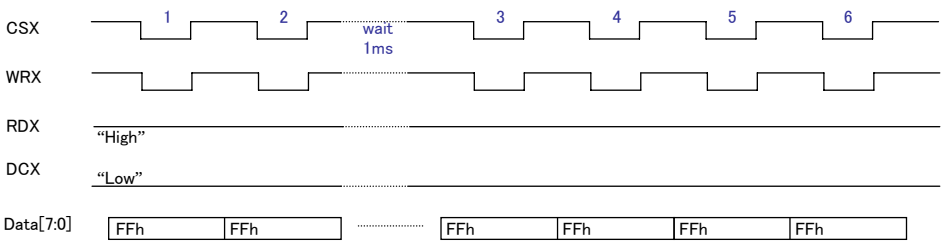
R61526 Deep Standby Mode On/Off Sequence

(1) Transition to Deep Standby Mode



(2) Exit from Deep Standby Mode





Waveforms in exiting deep standby mode

Reset

The R61526's initial internal setting is done with a RESET input. During the RESET period, no access, whether it is command write or frame memory data write operation, is accepted. The source driver unit and the power supply circuit unit are also reset to the respective initial states when RESET signal is inputted to the R61526.

1. Initial state of command

   The initial state of command is shown in Default Modes and Values table in Command List. The command setting is initialized to the default value when executing a Hardware Reset.

2. Frame Memory data initial state

   The Frame Memory data is not automatically initialized by inputting RESET. It needs to be initialized by software during Display Off period.

3. Input/output pin initial state

Table 30 Input/Output Pin Initial State

Pin name	After HW reset
DB[17:0]	Hi-Z
SDA	Hi-Z
SDO	GND
TE	GND
LEDPWM	GND
VDD	1.5V
C11P/C11M	VCI/Hi-Z
C12P/C12M	VCI/Hi-Z
C31P/C31M	VCI/GND
C21P/C21M	GND/GND
C22P/C22M	GND/GND
VCL	GND
VGL	GND
VGH	GND
DDVDH	VCI
VCOM	GND
S[1:720]	GND
G[1:320]	GND

Frame Memory

Arrangement

The frame memory stores display pixels and consists of 1,382,400 bits (320 x 240 x 18 bits).

Address Mapping from Memory to Display

Normal Display or Partial Mode, with Vertical Scroll enabled

In this mode, contents of the frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed.

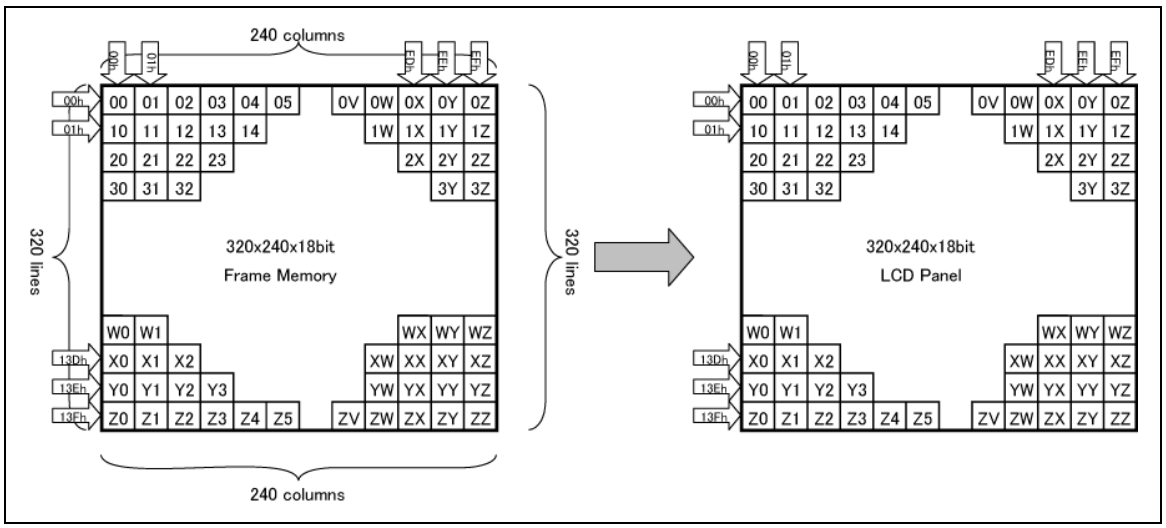


Figure 32

Host Processor to Memory Write/Read Direction

The data stream from host processor is as follows.

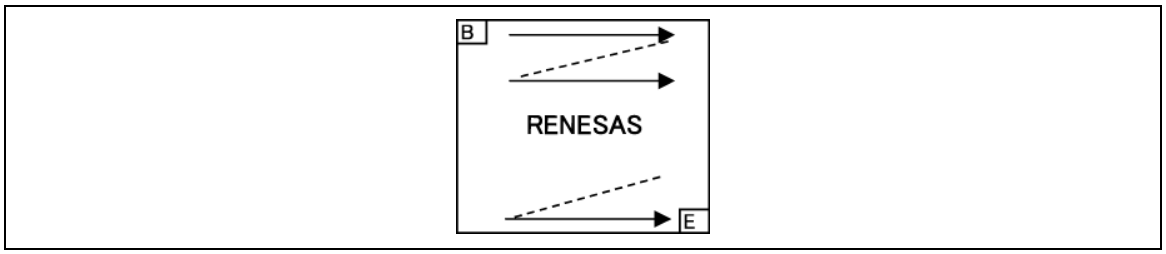


Figure 33

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "set_address_mode (36h)" command Bits B5, B6, B7 as described below.

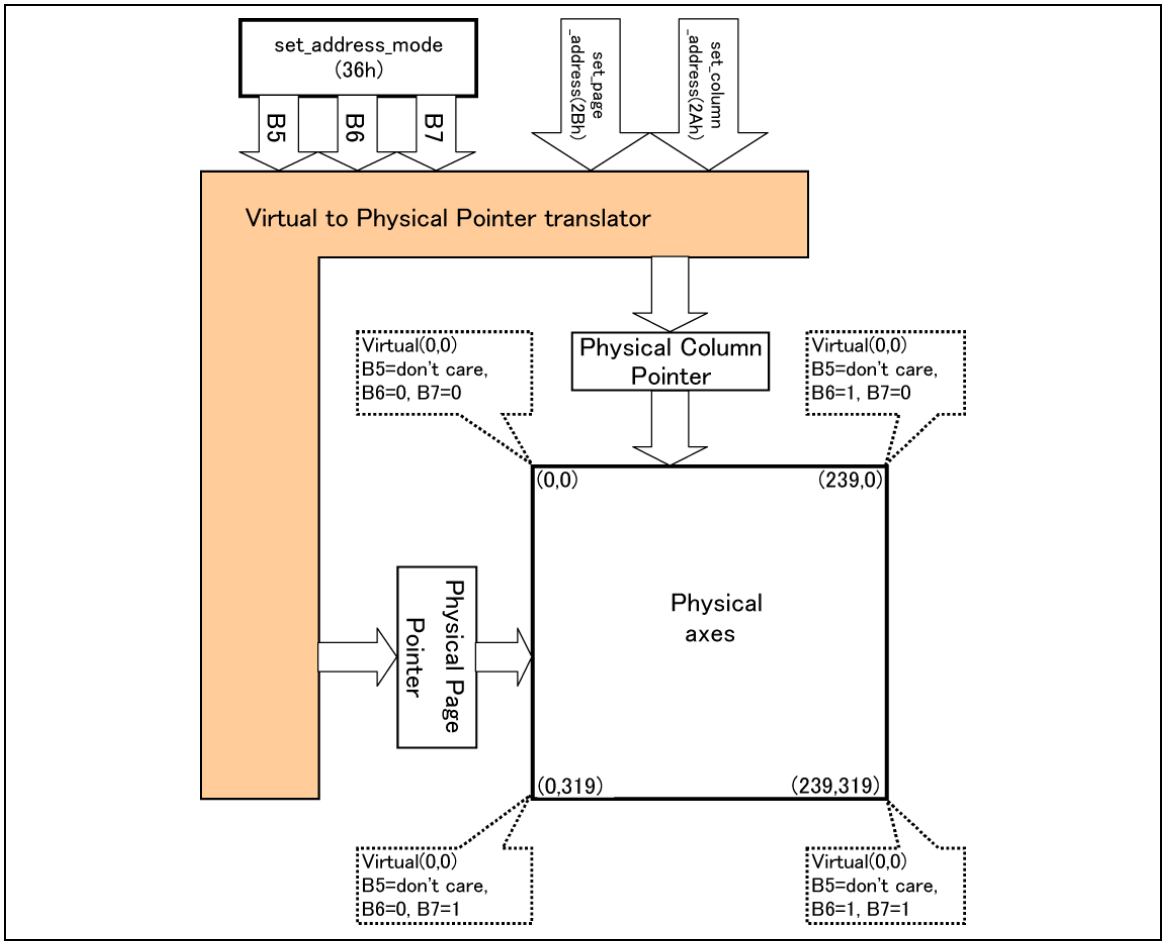


Figure 34

Table 31 set_address_mode Command

B5	B6	B7	Column Address	Page Address
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

For each image orientation, the controls on the column and page counters apply as below.

Note: Data is written to the frame memory not always in the same order. This is not affected by the write direction defined by B7, B6, B5 on set_address_mode (36h). See below for data alignment for subpixels in a pixel.

D 17	D 16	D 15	D 14	D 13	D 12	D 11	D 10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Table 32

Condition	Column Counter	Page Counter	Notes
When write_memory_start (2Ch)/read_memory_start (2Eh) command is accepted.	Return to “Start Column”	Return to “Start Page”	
Complete Pixel Read/Write action	Increment by 1	No change	
The Column counter value is larger than that of “End column.”	Return to Start Column”	Increment by 1	
The Column counter value is larger than that of “End column” and the Page counter value is larger than that of “End page”.	Stop	Stop	Entry Mode (B3h) WEMODE = 0
	Return to “Start Column”	Return to “Start Page”	Entry Mode (B3h) WEMODE = 1

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by set_address_mode (36h) bits B7, B6 and B5. The write order for each pixel unit is as follows.

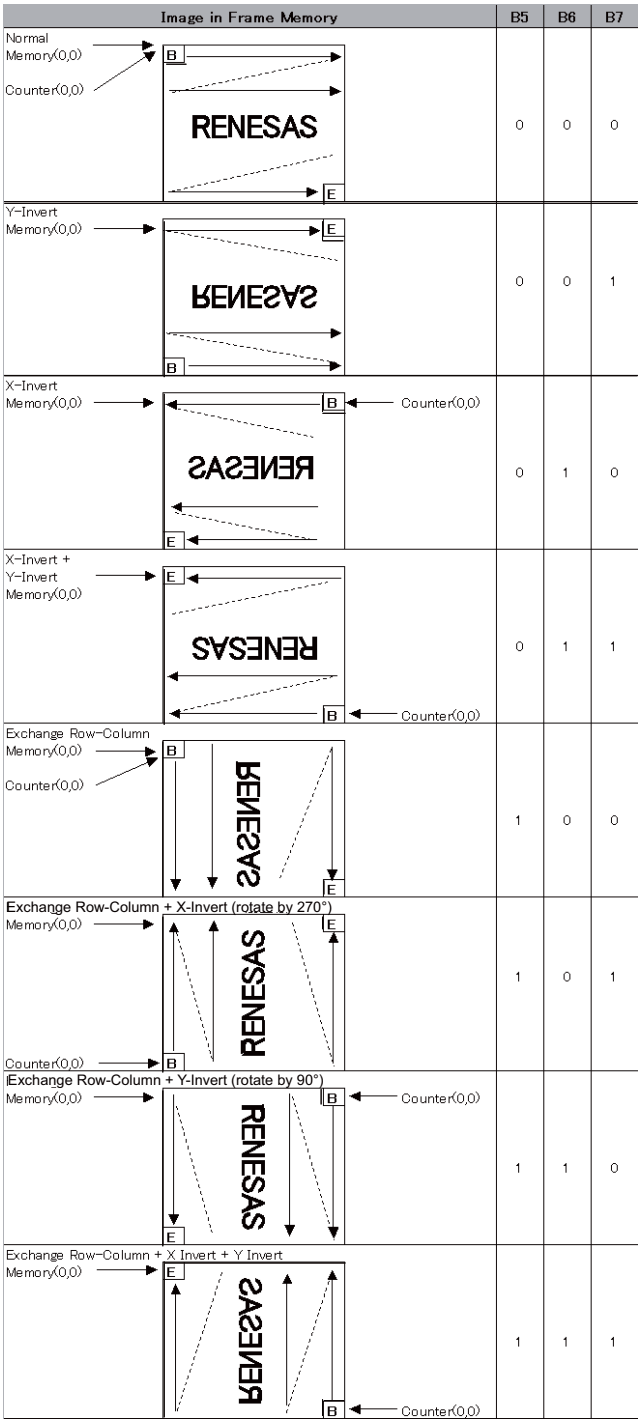


Image in Frame Memory
B5
B6
B7
Normal
Memory(0,0)
Counter(0,0)
RENESAS
0 0 0
Y-Invert
Memory(0,0)
0 0 1
X-Invert
Memory(0,0)
Counter(0,0)
0 1 0
X-Invert +
Y-Invert
Memory(0,0)
0 1 1
Exchange Row-Column
Memory(0,0)
Counter(0,0)
1 0 0
Exchange Row-Column + X-Invert (rotate by 270°)
Memory(0,0)
Counter(0,0)
1 0 1
Exchange Row-Column + Y-Invert (rotate by 90°)
Memory(0,0)
Counter(0,0)
1 1 0
Exchange Row-Column + X Invert + Y Invert
Memory(0,0)
Counter(0,0)
1 1 1

Figure 35

B5=0

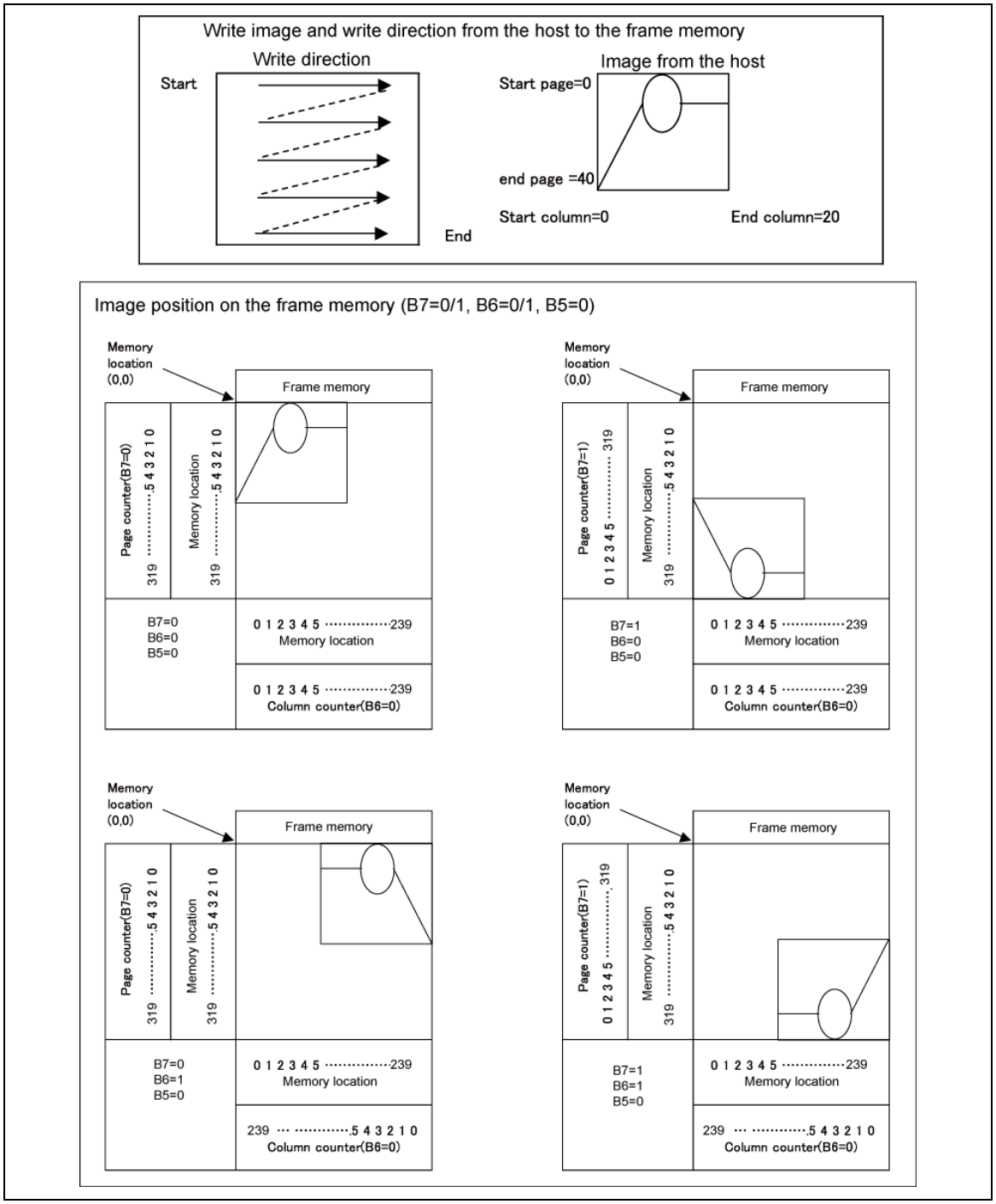


Figure 36

B5 =1

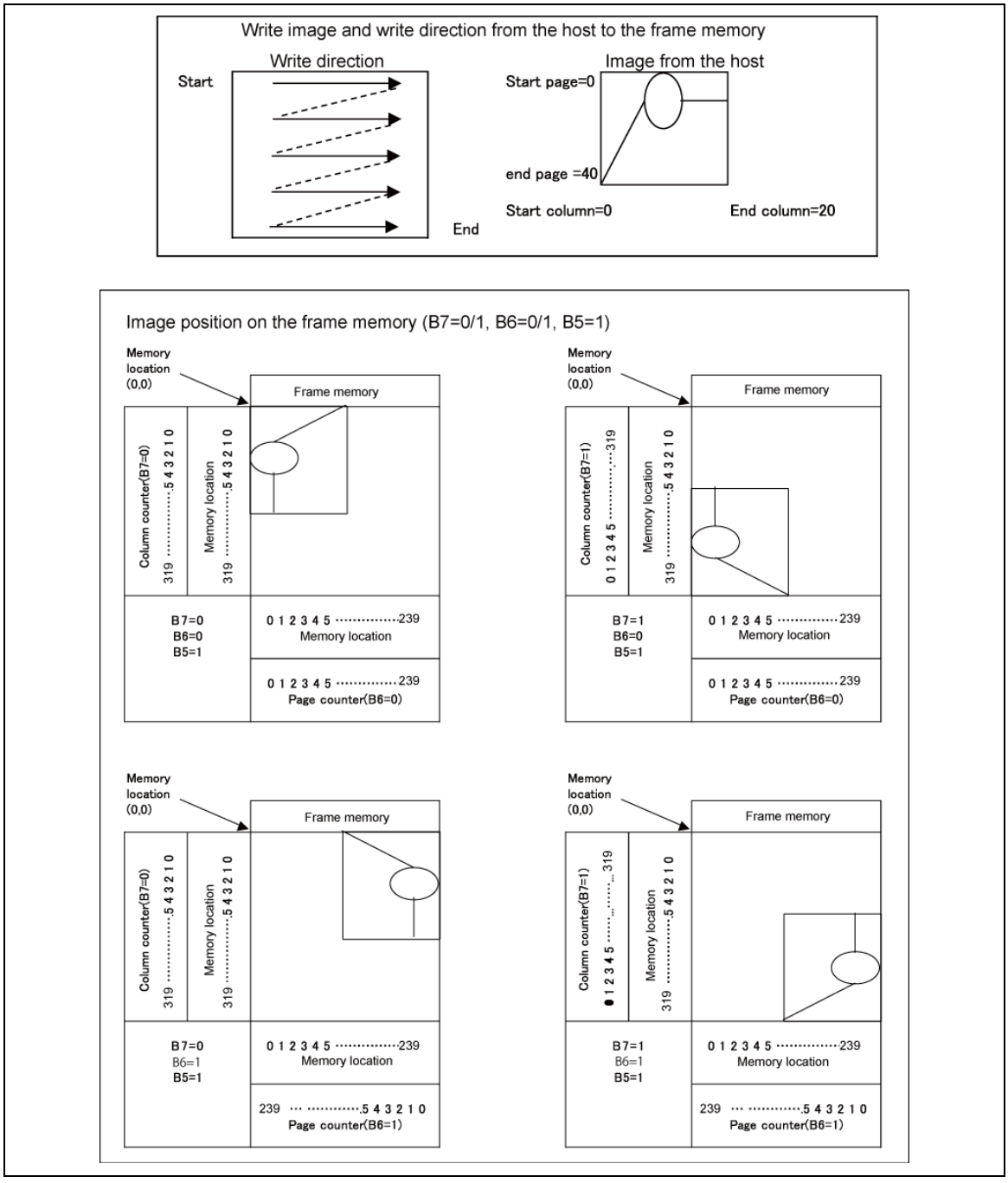


Figure 37

Self-Diagnostic Function

The R61526 supports the self-diagnostic functions. Set get_diagnostic_result (0Fh) 1st parameter's D6 bit as following flow chart.

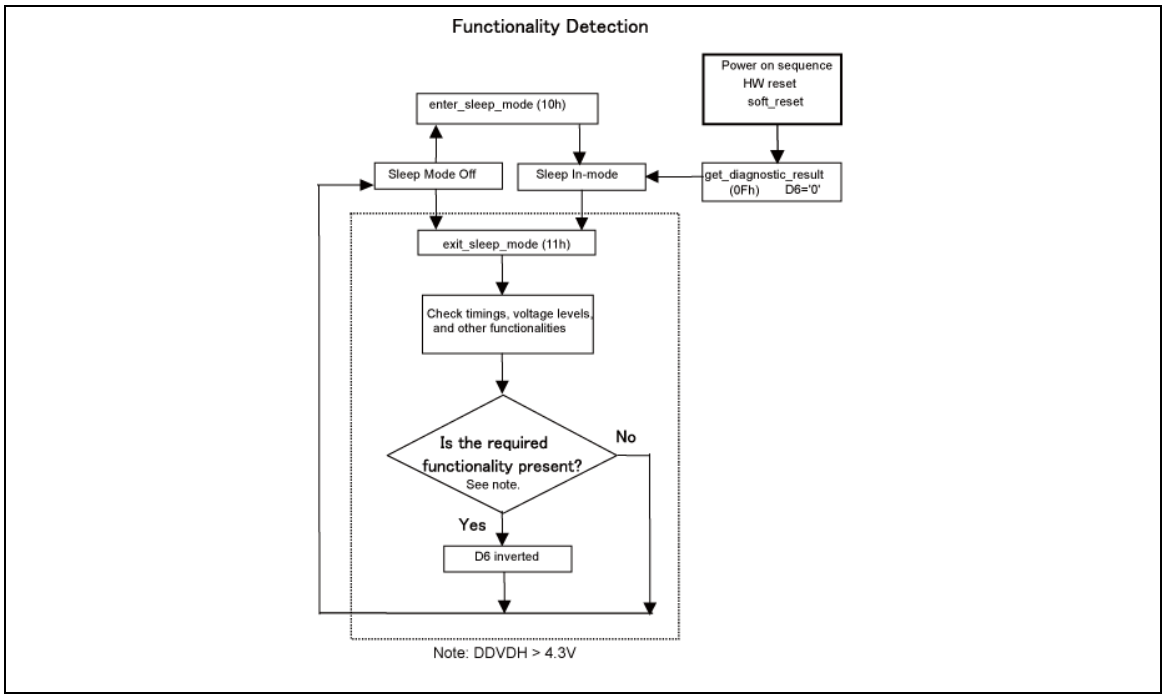


Figure 38

Functionality Detection

The exit_sleep_mode command is a trigger for the Functionality Detection function. If DDVDH is 4.3V or more, the step-up circuit is regarded as operating properly, then bit D6 is inverted.

Scan Mode Setting

The relationship among driver arrangement, GS, SM, SS and BGR register settings and the Frame Memory Address (1) is shown below. In the default status, the top left address is (00,000) and the panel is scanned from top to bottom.

Left/Right Interchanging Scan

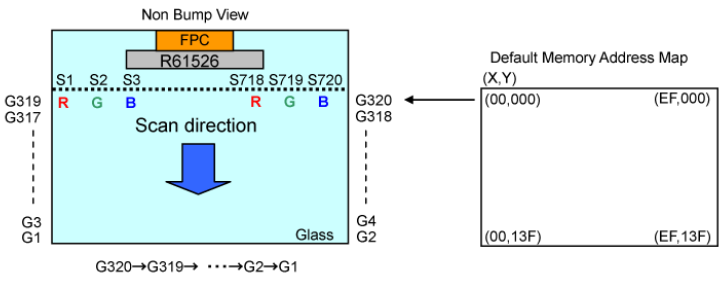
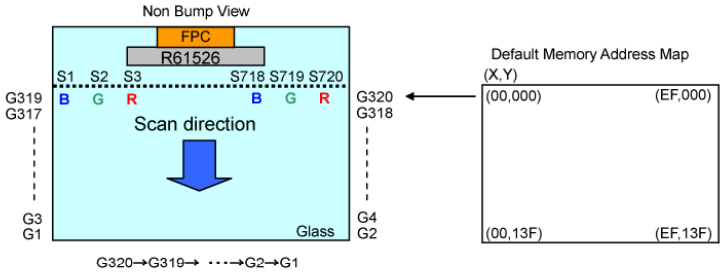
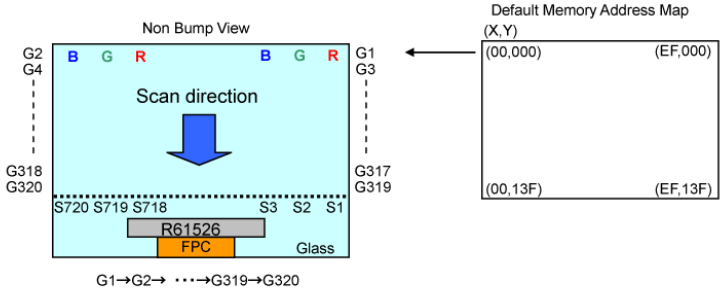
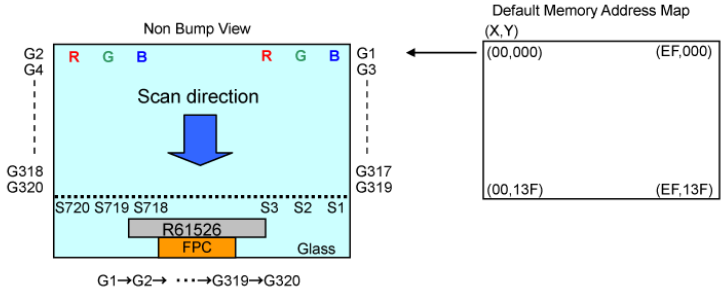
Registers	Position of the LCD Driver and Frame Memory Address
SS=0 BGR=0 GS=1 SM=0	
SS=0 BGR=1 GS=1 SM=0	
SS=1 BGR=0 GS=0 SM=0	
SS=1 BGR=1 GS=0 SM=0	

Figure 39

The relationship among driver arrangement, GS, SM, SS and BGR register settings and the Frame Memory Address (2) is shown below. In the default status, the top left address is (00,000) and the panel is scanned from top to bottom.

Left/Right One-side Scan

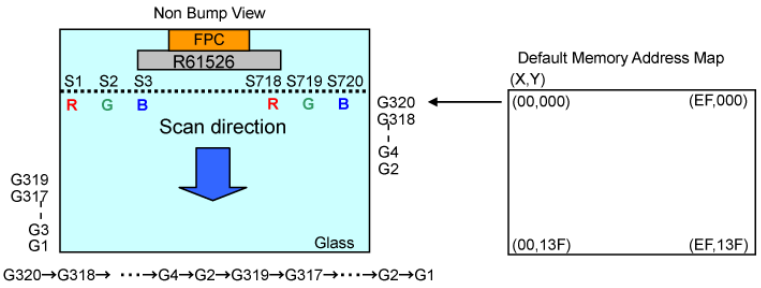
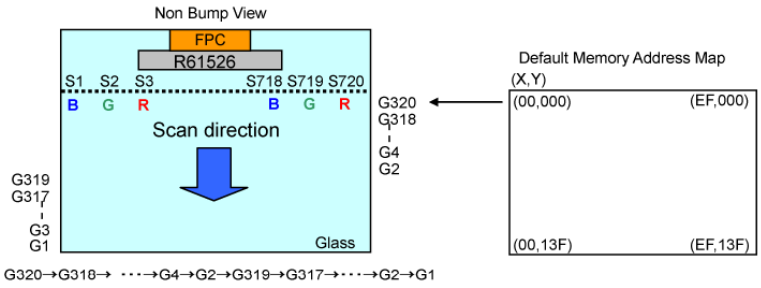
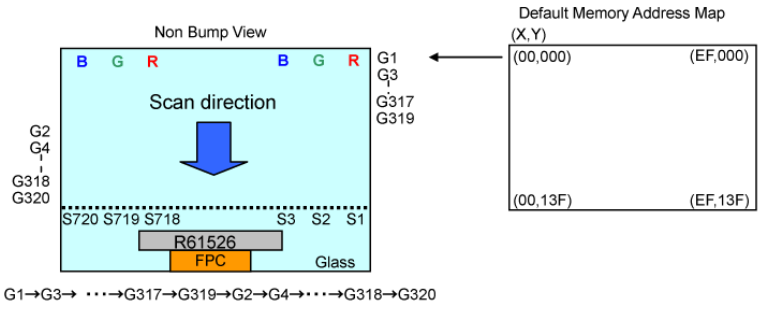
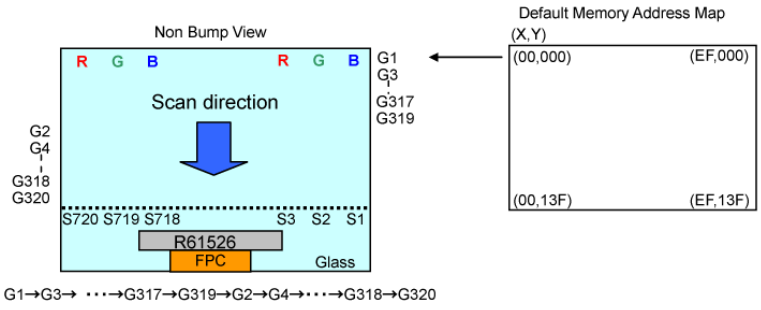
Registers	Position of the LCD Driver and Frame Memory Address
SS=0 BGR=0 GS=1 SM=1	
SS=0 BGR=1 GS=1 SM=1	
SS=1 BGR=0 GS=0 SM=1	
SS=1 BGR=1 GS=0 SM=1	

Figure 40

Frame Frequency Adjustment Function

The R61526 supports a function to adjust frame frequency. The frame frequency for driving the LCD can be adjusted by setting Display Timing Setting (C1h~C3h, DIV and RTN bits) without changing the oscillation frequency.

It is possible to set a low frame frequency for saving power consumption when displaying a still picture and set a high frame frequency when displaying moving image.

Also, the R61526 has frame-frequency adjustment parameters, which can set frame frequency according to display modes (normal and idle modes).

Relationship between the Liquid Crystal Drive Duty and the Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following equation. The frame frequency can be changed by setting 1 line period setting (RTN) bit and operating clock frequency division ratio setting (DIV) bit.

Equation for calculating frame frequency

$$FrameFrequency = \frac{fosc}{NumberofClocks/line \times (NL + FP + BP)}[Hz]$$

fosc: Internal clock frequency (800 kHz)
Clocks per line: RTN bit
Line: Number of drive line(s) on the panel: NL
Front porch (FP): FP bit
Back porch (BP): BP bit

Example of Calculation: when Maximum Frame Frequency = 60 Hz

fosc : 800 kHz
Number of lines: 320 lines
1 line period: 40 clock cycles (RTN[5:0] = 5'h28)
Front porch: 4 lines
Back porch: 4 lines

$$\therefore f_{FLM} = \frac{800kHz}{40clocks \times (320 + 4 + 4)lines} \approx 60Hz$$

In the conditions described here, the frame frequency can be changed as follows by setting RTN and DIV.

Line Inversion AC Drive

The R61526, in addition to frame-inversion liquid crystal alternating current drive, supports line inversion alternating current drive.

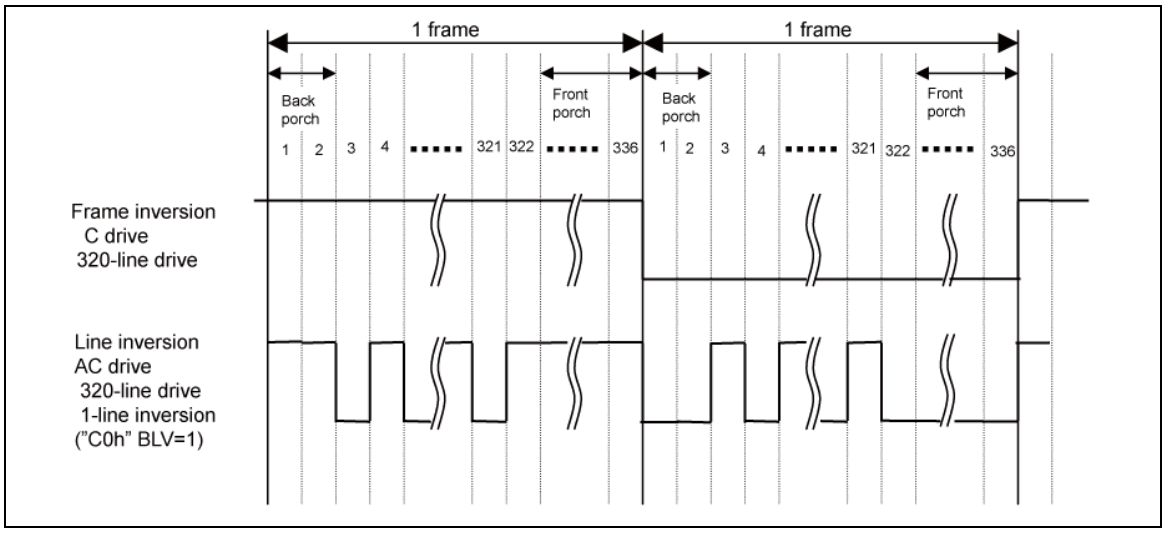


Figure 41 Liquid Crystal Inversion Drive Waveform

Alternating Timing

The following figure illustrates the liquid-crystal polarity inversion timing of different LCD driving methods.

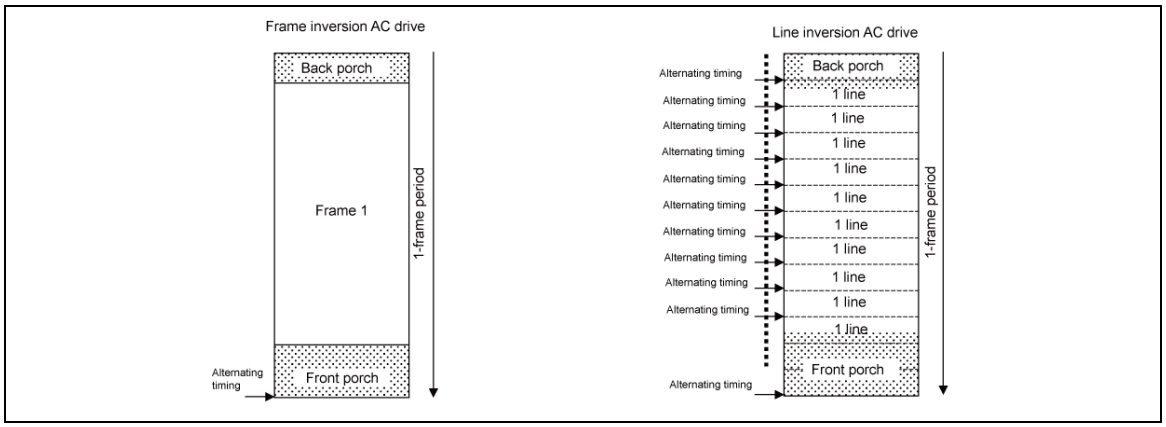


Figure 42 Alternating Timing

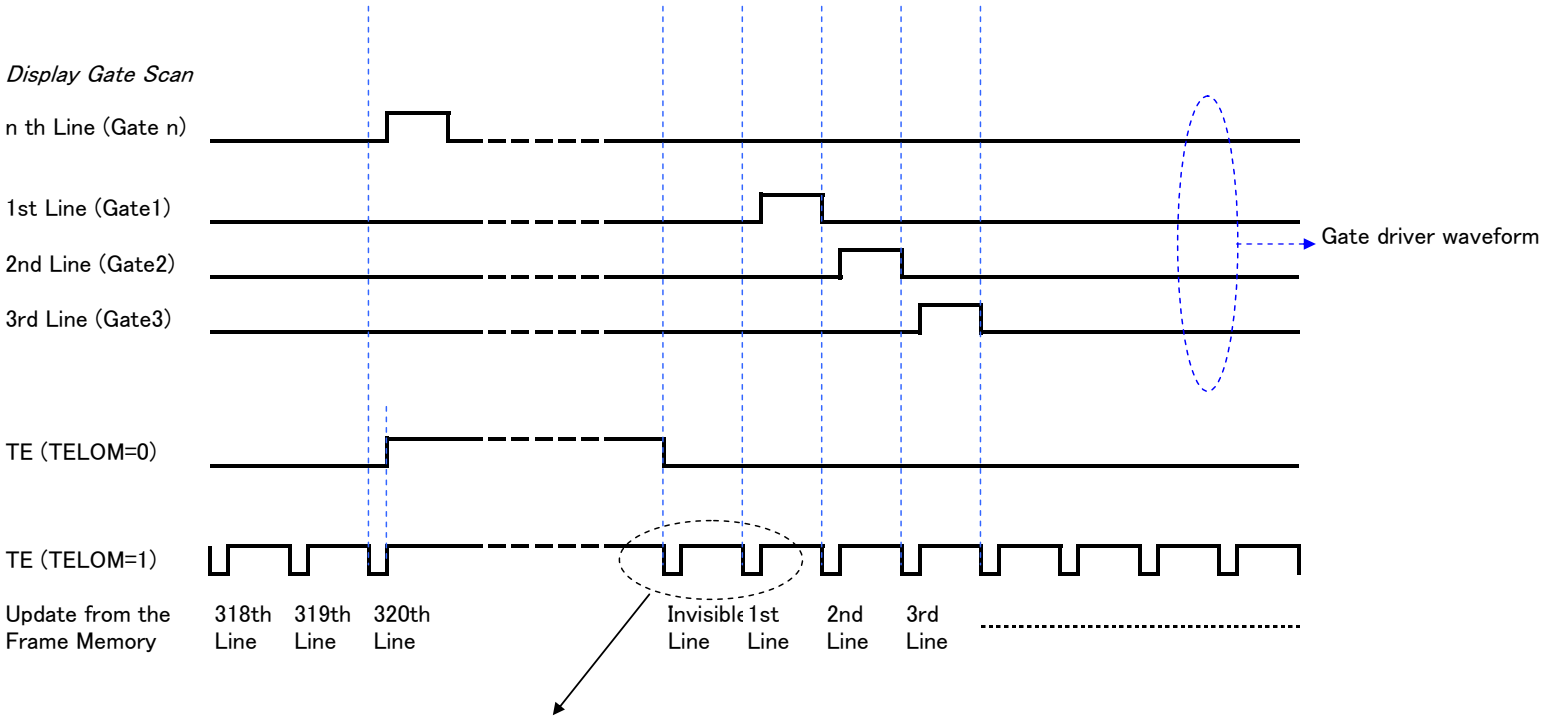
TE Pin Output Signal

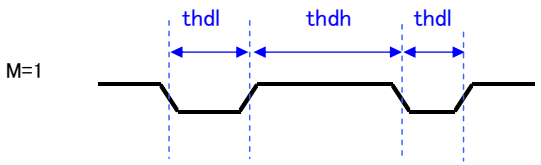
Tearing Effect Line signal can be output from TE pin as frame memory data transfer synchronous signals. TE signal is trigger for frame memory write operation to enable data transfer in synchronization with the scanning operation. Tearing Effect Output signal is turned on/off by set_tear_off (34h) and set_tear_on (35h) commands.

Table 33

TEON(35h)	TELOM (35h's1st parameter)	TE pin output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)

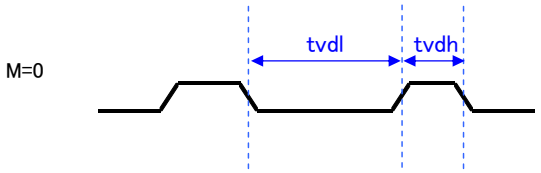
35h set tear on command





Definition

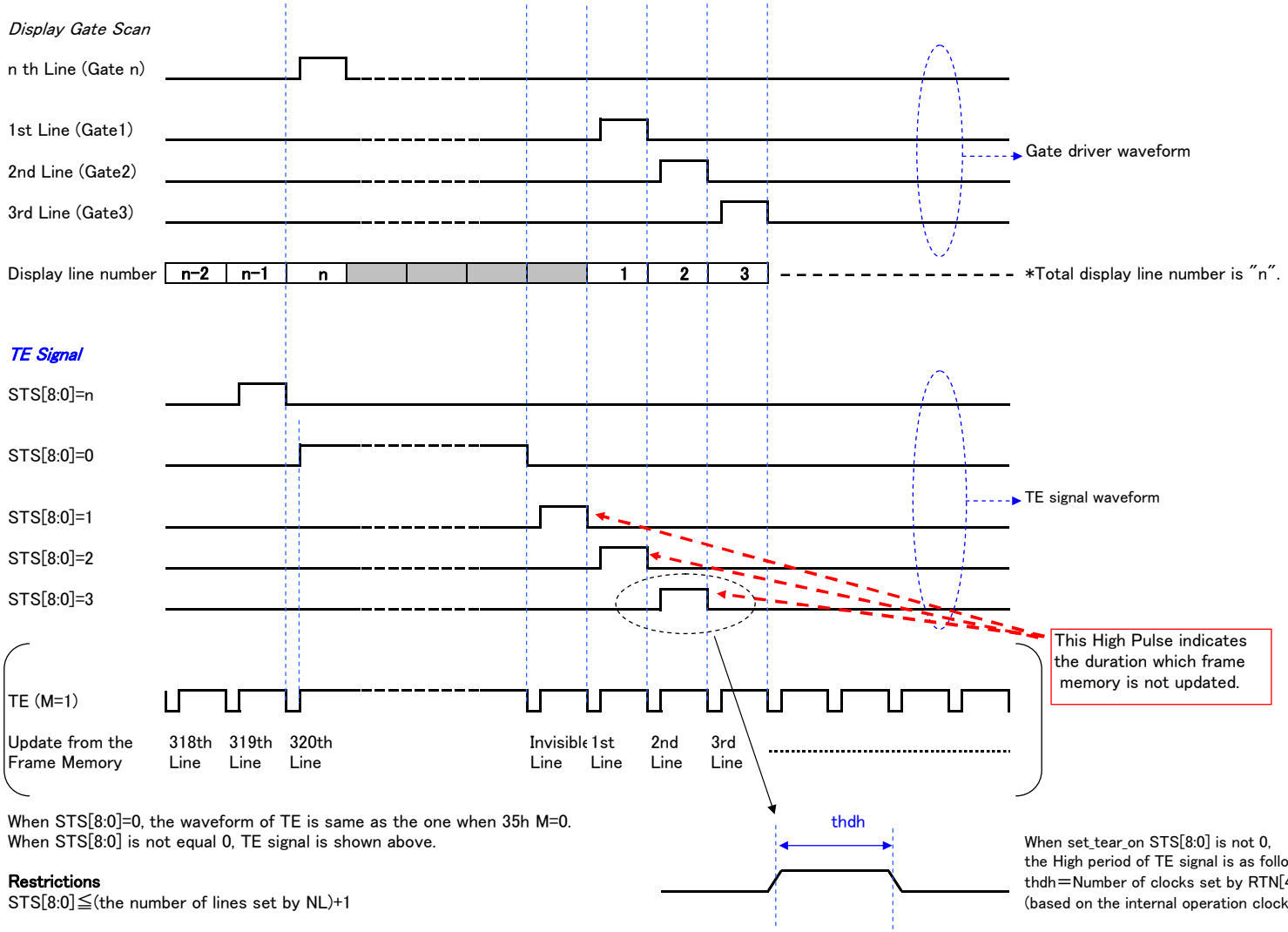
thdh : The LCD Display is not updated from the Frame Memory.
thdl : The LCD Display is updated from the Frame Memory.



tvdh : The LCD Display is not updated from the Frame Memory.
tvdl : The LCD Display is updated from the Frame Memory.

44h set tear scanline command

STS[8:0] Setting (0～n)



When STS[8:0]=0, the waveform of TE is same as the one when 35h M=0.
When STS[8:0] is not equal 0, TE signal is shown above.

Restrictions
STS[8:0]≦(the number of lines set by NL)+1

When set_tear_on STS[8:0] is not 0,
the High period of TE signal is as follows:
thdh＝Number of clocks set by RTN[4:0] − 3 clocks
(based on the internal operation clock)

Display-Synchronous Data Transfer Using TE Signal

The R61526 enables data transfer in synchronization with the display scan by writing data to the internal frame memory using the TE signal as the trigger.

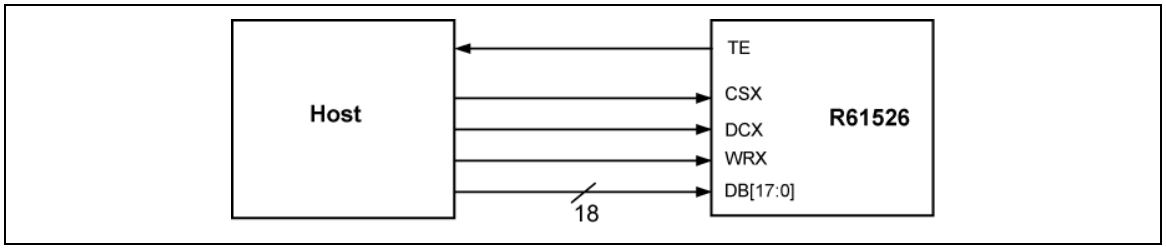


Figure 43 Interface Example for Display-Synchronous Data Transfer

By writing data to the internal Frame Memory at faster than calculated minimum speed, it becomes possible to rewrite the moving image data without flickering the display and display moving image via system interface. The display data is written in the Frame Memory so that the R61526 rewrites the data only within the moving image area and minimize the number of data transfer required to display moving image.

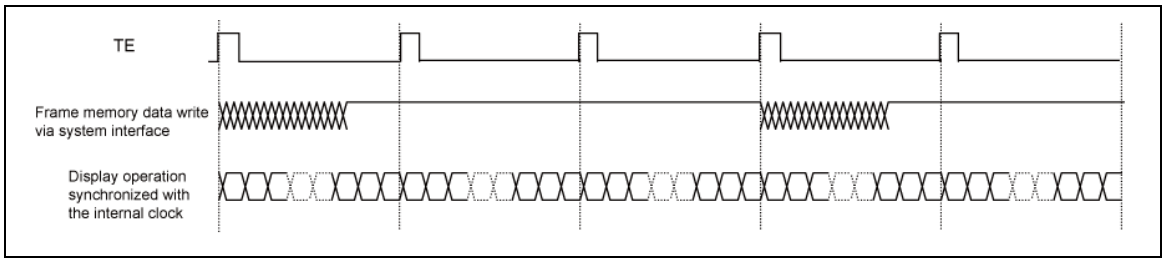


Figure 44 Moving Image Data Write via TE

When transferring data using TE as the trigger, there are restrictions in setting the minimum Frame Memory data write speed and the minimum internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

Internal clock frequency (fosc) [Hz] = Frame frequency × (Display lines (NL) + Front porch (FP) + Back porch (BP)) × Clocks per 1 line (RTN) × Variance

Frame memory write speed (min.) [Hz] >
240 × Display lines (NL) / {(FP + BP + Display lines (NL) – Margins) × Clocks per 1 line (RTN) × 1/ fosc}

Note: When frame memory write operation is not started right after the rising edge of TE, time from the rising edge of TE to the start of frame memory write operation must also be taken into account.

An example of calculating the minimum frame memory writing speed and internal clock frequency for writing data in synchronization with display operation.

[Example]

Display size	240 RGB × 320 lines
Display lines	320 lines
Back/front porch	8/8 lines (BP = 8'h8/ FP = 8'h8)
set_tear_scanline (STS)	The end line of the display: 320th line
Frame frequency	60 Hz
Internal operation clock	800kHz x 1.07 = 856kHz
Clocks in 1 line period	40 clocks

Note: This example includes variances attributed to LSI production process and room temperature. Other possible causes of variances, such as voltage change, are not considered in this example. It is necessary to include a margin for these factors.

Frame memory write speed (min.) [Hz]
> 240 × 320 / {((8+8 + 320 - 2) lines × 40 clocks) × 1/856 kHz} = 5.23 MHz

Notes: 1. In this example, it is assumed that the R61526 starts writing data in the frame memory on the rising edge of TE.
2. There must be at least a margin of 2 lines between the line to which the R61526 has just written data and the line where the display operation on the LCD is performed.
3. TE signal may be set on any line.

In this example, the frame memory write operation at a speed of 5.23MHz or more, which starts on the rising edge of TE, guarantees the completion of data write operation in a certain line address before the R61526 starts the display operation of the data written in that line and can write moving image data without causing flicker on the display.

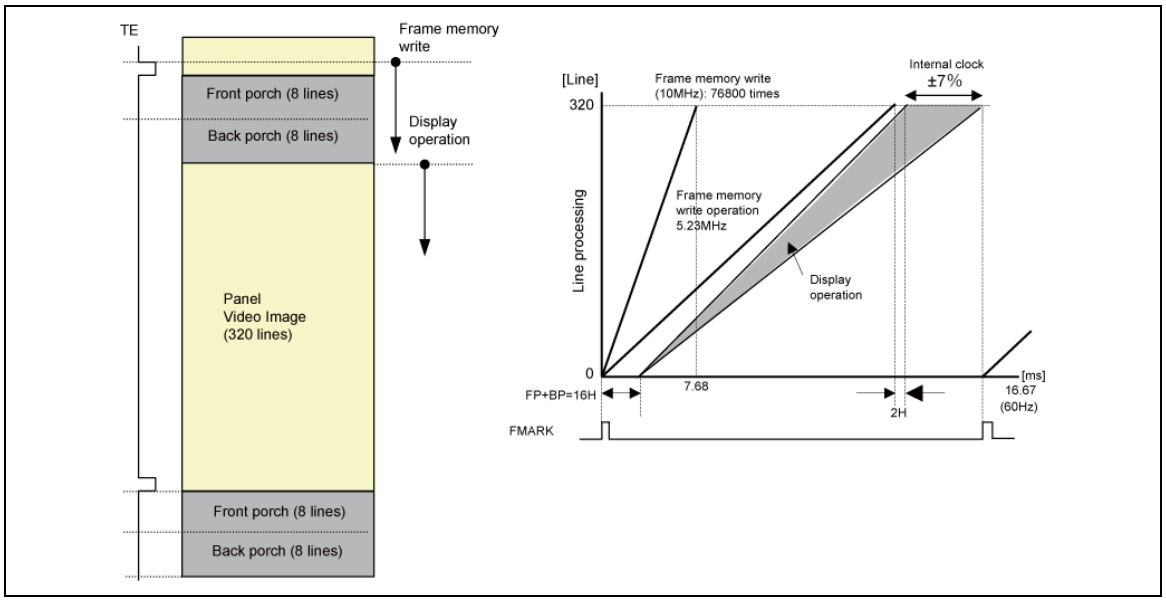


Figure 45

Liquid Crystal Panel Interface Timing

The following figure shows the timing of DPI and liquid crystal panel interface signals in DPI operation.

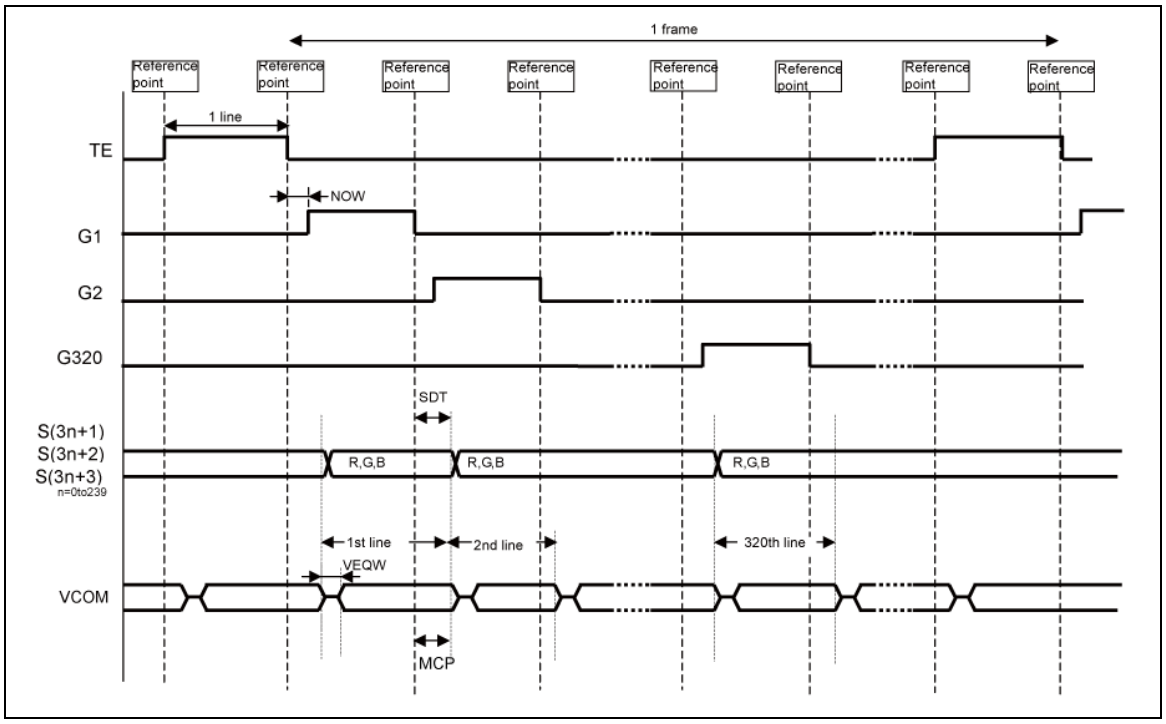


Figure 46 Liquid Crystal Panel Interface Timing in Internal Clock Operation

VCOM and source output alternating positions are defined separately.

Note 1: The shown TE waveform has values M=0, set_tear_scanline STS[8:0]=1.

Note 2: In the figure above, VCOM waveform is example when BCn=1, PTV=1.

Setting range
MCP[2:0]: 1 to 7clks
SDT[2:0]: 1 to 7clks
NOW[2:0]: 1 to 7clks
Units: 1clk

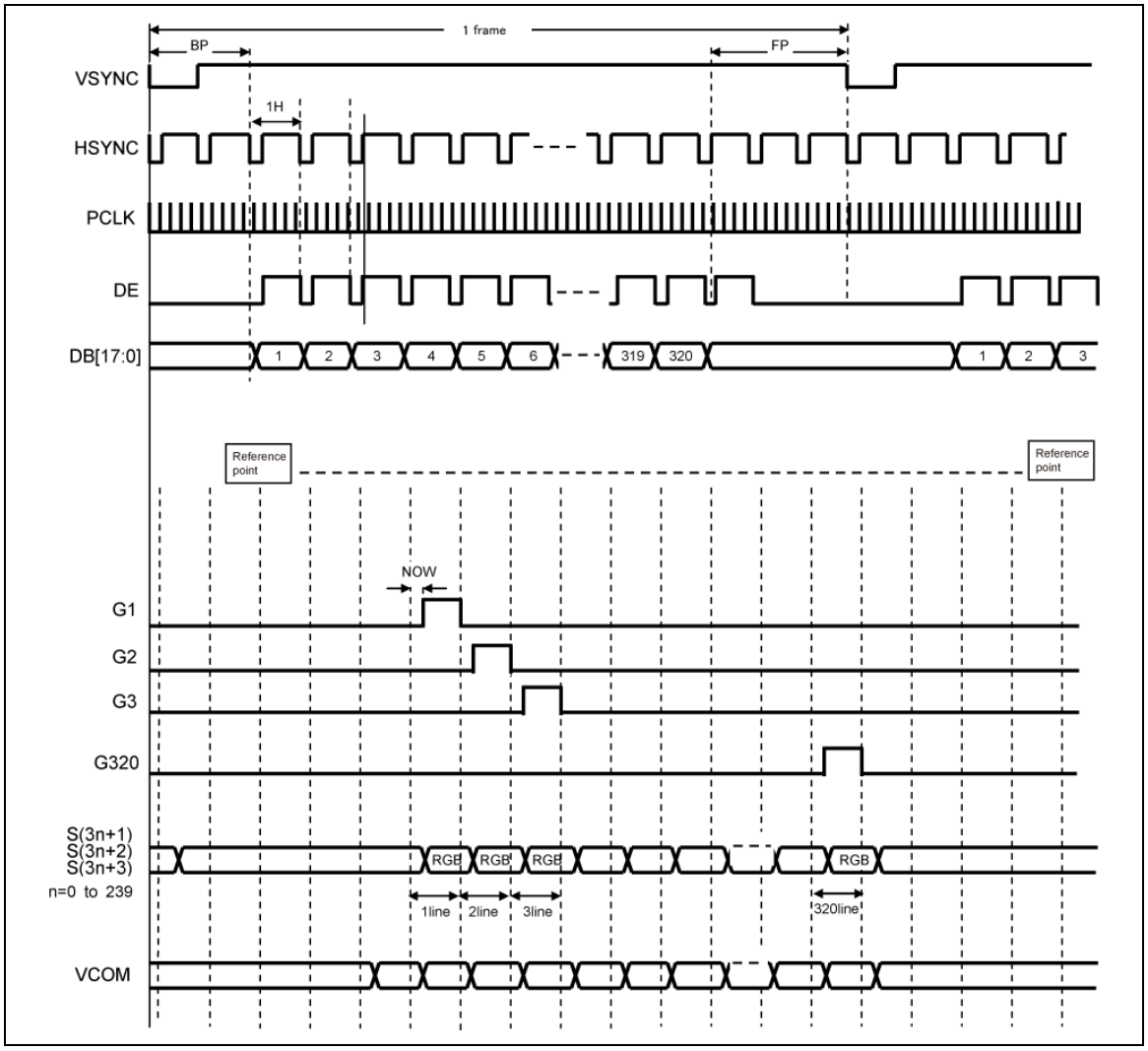


Figure 47 Liquid Crystal Panel Interface Timing in DPI Operation

Note: In the figure above, VCOM waveform is example when BCn=1, BLV=1.

Gamma Correction Function

Gamma Correction Function

The R61526 supports gamma correction function to make the optimal colors according to the characteristics of the panel. Separate gamma settings for R, G and B bits is selected. Write appropriate values to Gamma Sets A, B, and C.

Gamma Correction Circuit

The following figure shows the gamma correction circuit. The resistor ladder is divided by 128 steps that are connected to VREG and VGS. A selector selects the divided voltages and buffer them using amplifiers to generate reference grayscales V0, V1, V4, V8, V20, V43, V55, V59, V62 and V63.

Voltages other than the references are generated by interpolation. See “Grayscale Voltage Calculation Formula”.

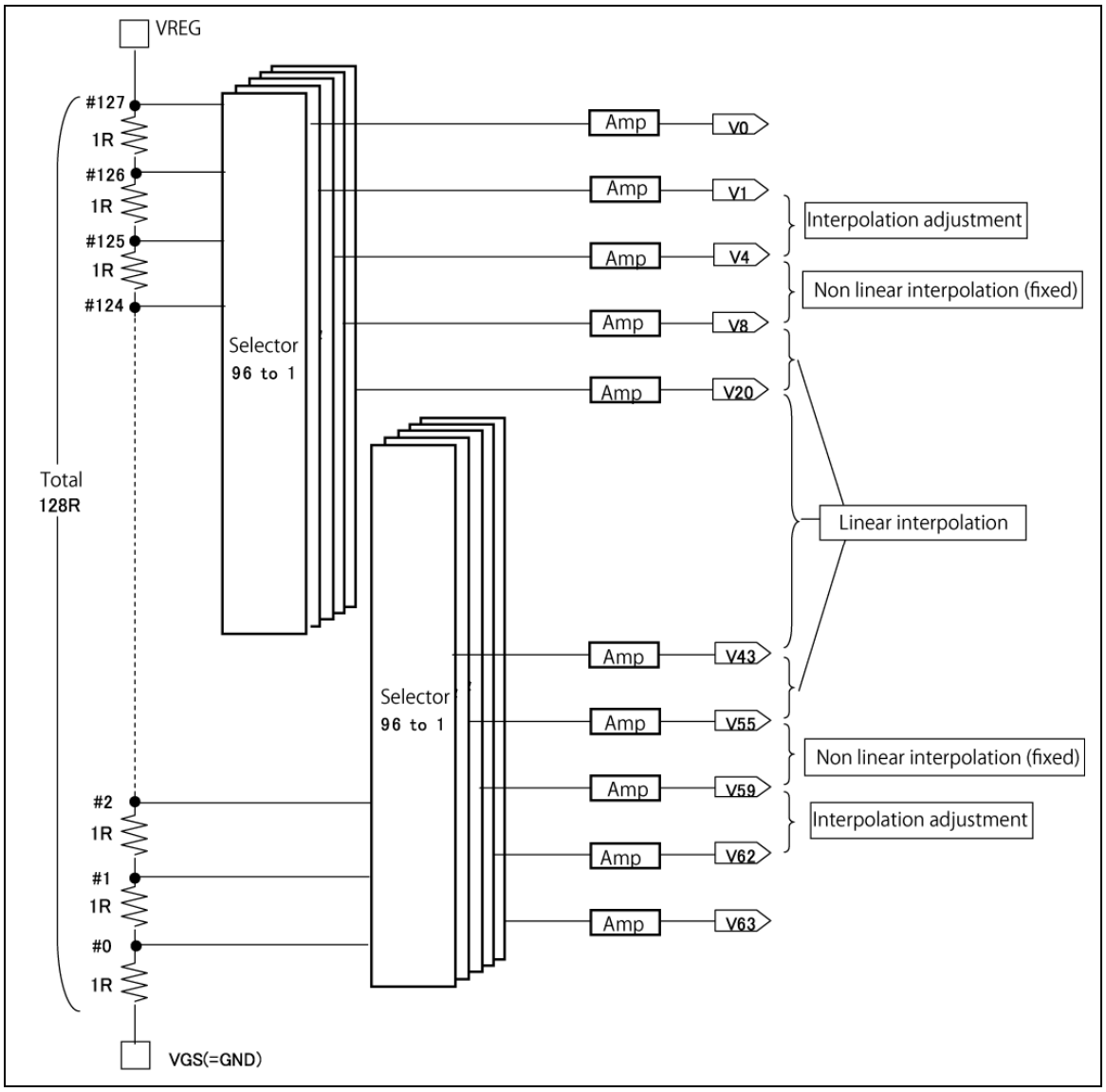

VREG
#127
1R
#126
1R
#125
1R
#124
Selector
96 to 1
Total
128R
Amp
V0
Amp
V1
Amp
V4
Amp
V8
Amp
V20
Interpolation adjustment
Non linear interpolation (fixed)
Linear interpolation
Selector
96 to 1
Amp
V43
Amp
V55
Amp
V59
Amp
V62
Amp
V63
Non linear interpolation (fixed)
Interpolation adjustment
#2
1R
#1
1R
#0
1R
VGS(=GND)

Figure 48

Gamma Correction Registers

The reference level of the gamma correction registers (PRGPxP0~PRGPxP8/PRBOTxP/PRGPxN0~PRGPxN8/PRBOTxN) is defined by GSELxP0~GSELxP9/ GSELxN0~GSELxN9 after below calculations. Adjust GSELxP0~GSELxP9/ GSELxN0~GSELxN9 so that an overflow does not occur. (0~2 is substituted in x.)

・Formulas for Gamma Registers

GSELxP0 = PRGPxP0 + GSELxP1	GSELxN0 = PRGPxN0 + GSELxN1
GSELxP1 = PRGPxP1 + GSELxP2	GSELxN1 = PRGPxN1 + GSELxN2
GSELxP2 = PRGPxP2 + GSELxP3	GSELxN2 = PRGPxN2 + GSELxN3
GSELxP3 = PRGPxP3 + GSELxP4	GSELxN3 = PRGPxN3 + GSELxN4
GSELxP4 = PRGPxP4 + GSELxP5	GSELxN4 = PRGPxN4 + GSELxN5
GSELxP5 = PRGPxP5 + GSELxP6	GSELxN5 = PRGPxN5 + GSELxN6
GSELxP6 = PRGPxP6 + GSELxP7	GSELxN6 = PRGPxN6 + GSELxN7
GSELxP7 = PRGPxP7 + GSELxP8	GSELxN7 = PRGPxN7 + GSELxN8
GSELxP8 = PRGPxP8 + GSELxP9	GSELxN8 = PRGPxN8 + GSELxN9
GSELxP9 = PRBOTxP	GSELxN9 = PRBOTxN

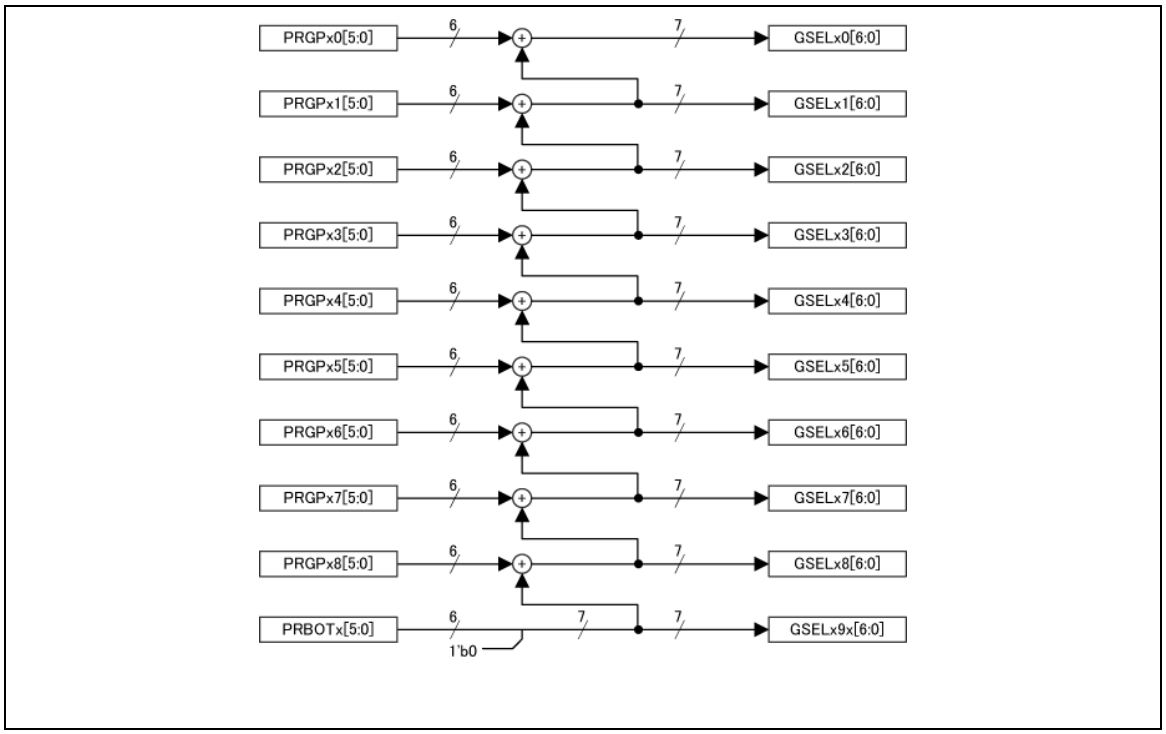


Figure 49

Table 34 Reference Level Adjustment Registers (Data after calculation (GSEL*))

Reference level	Gamma Set A		Gamma Set B		Gamma Set C	
	Positive	Negative	Positive	Negative	Positive	Negative
V0	GSEL0P0[6:0]	GSEL0N0[6:0]	GSEL1P0[6:0]	GSEL1N0[6:0]	GSEL2P0[6:0]	GSEL2N0[6:0]
V1	GSEL0P1[6:0]	GSEL0N1[6:0]	GSEL1P1[6:0]	GSEL1N1[6:0]	GSEL2P1[6:0]	GSEL2N1[6:0]
V4	GSEL0P2[6:0]	GSEL0N2[6:0]	GSEL1P2[6:0]	GSEL1N2[6:0]	GSEL2P2[6:0]	GSEL2N2[6:0]
V8	GSEL0P3[6:0]	GSEL0N3[6:0]	GSEL1P3[6:0]	GSEL1N3[6:0]	GSEL2P3[6:0]	GSEL2N3[6:0]
V20	GSEL0P4[6:0]	GSEL0N4[6:0]	GSEL1P4[6:0]	GSEL1N4[6:0]	GSEL2P4[6:0]	GSEL2N4[6:0]
V43	GSEL0P5[6:0]	GSEL0N5[6:0]	GSEL1P5[6:0]	GSEL1N5[6:0]	GSEL2P5[6:0]	GSEL2N5[6:0]
V55	GSEL0P6[6:0]	GSEL0N6[6:0]	GSEL1P6[6:0]	GSEL1N6[6:0]	GSEL2P6[6:0]	GSEL2N6[6:0]
V59	GSEL0P7[6:0]	GSEL0N7[6:0]	GSEL1P7[6:0]	GSEL1N7[6:0]	GSEL2P7[6:0]	GSEL2N7[6:0]
V62	GSEL0P8[6:0]	GSEL0N8[6:0]	GSEL1P8[6:0]	GSEL1N8[6:0]	GSEL2P8[6:0]	GSEL2N8[6:0]
V63	GSEL0P9[6:0]	GSEL0N9[6:0]	GSEL1P9[6:0]	GSEL1N9[6:0]	GSEL2P9[6:0]	GSEL2N9[6:0]

Table 35 Reference level selection register and selection level

Data after calculation	Register value	Selection point	Selection level	Data after calculation	Register value	Selection point	Selection level
GSEL**0[6:0] GSEL**1[6:0] GSEL**2[6:0] GSEL**3[6:0]	7'h00	Setting inhibited	-	GSEL**4[6:0]	7'h00	Setting inhibited	-
	7'h01	Setting inhibited	-		7'h01	Setting inhibited	-
	7'h02	Setting inhibited	-		7'h02	Setting inhibited	-
	·	·	·		·	·	·
	·	·	·		·	·	·
	7'h1F	Setting inhibited	-		7'h1F	Setting inhibited	-
	7'h20	Setting inhibited	-		7'h20	#32	Δ V x 33/128
	7'h21	Setting inhibited	-		7'h21	#33	Δ V x 34/128
	·	·	·		·	·	·
	·	·	·		·	·	·
	7'h2F	Setting inhibited	-		7'h2F	#47	Δ V x 47/128
	7'h30	#48	Δ V x 48/128		7'h30	#48	Δ V x 48/128
	7'h31	#49	Δ V x 49/128		7'h31	#49	Δ V x 49/128
	·	·	·		·	·	·
	·	·	·		·	·	·
	7'h3F	#63	Δ V x 64/128		7'h3F	#63	Δ V x 64/128
	7'h40	#64	Δ V x 65/128		7'h40	#64	Δ V x 65/128
	7'h41	#65	Δ V x 66/128		7'h41	#65	Δ V x 66/128
	·	·	·		·	·	·
	·	·	·		·	·	·
	7'h5F	#95	Δ V x 96/128		7'h5F	#95	Δ V x 96/128
	7'h60	#96	Δ V x 97/128		7'h60	#96	Δ V x 97/128
	7'h61	#97	Δ V x 98/128		7'h61	#97	Δ V x 98/128
	·	·	·		·	·	·
	·	·	·		·	·	·
	7'h7F	#127	Δ V x128/128		7'h7F	#127	Δ V x128/128

Table 36 Reference level selection register and selection level (continued)

Data after calculation	Register value	Selection point	Selection level	Data after calculation	Register value	Selection point	Selection level
GSEL**5[6:0]	7'h00	#0	ΔV x 1/128	GSEL**6[6:0] GSEL**7[6:0] GSEL**8[6:0] GSEL**9[6:0]	7'h00	#0	ΔV x 1/128
	7'h01	#1	ΔV x 2/128		7'h01	#1	ΔV x 2/128
	7'h02	#2	ΔV x 3/128		7'h02	#2	ΔV x 3/128
	·	·	·		·	·	·
	·	·	·		·	·	·
	7'h1F	#31	ΔV x 32/128		7'h1F	#31	ΔV x 32/128
	7'h20	#32	ΔV x 33/128		7'h20	#32	ΔV x 33/128
	7'h21	#33	ΔV x 34/128		7'h21	#33	ΔV x 34/128
	·	·	·		·	·	·
	·	·	·		·	·	·
	7'h3F	#63	ΔV x 64/128		7'h3F	#63	ΔV x 64/128
	7'h40	#64	ΔV x 65/128		7'h40	#64	ΔV x 65/128
	7'h41	#65	ΔV x 66/128		7'h41	#65	ΔV x 66/128
	·	·	·		·	·	·
	·	·	·		·	·	·
	7'h4F	#79	ΔV x 80/128		7'h4F	#79	ΔV x 80/128
	7'h51	#80	ΔV x 81/128		7'h51	Setting inhibited	-
	7'h52	#81	ΔV x 82/128		7'h52	Setting inhibited	-
	·	·	·		·	·	·
	·	·	·		·	·	·
	7'h5F	#95	ΔV x 96/128		7'h5F	Setting inhibited	-
	7'h60	Setting inhibited	-		7'h60	Setting inhibited	-
	7'h61	Setting inhibited	-		7'h61	Setting inhibited	-
	·	·	·		·	·	·
	·	·	·		·	·	·
	7'h7F	Setting inhibited	-		7'h7F	Setting inhibited	-

Note: ** indicates 0P/0N/1P/1N/2P/2N. ΔV means VREG – VGS.

Make sure that

Reference level is defined so that V0 > V1 > V4 > V8 > V20 > V43 > V55 > V59 > V62 > V63.

V63 ≥ 0.2V.

Interpolation Registers

Table 37 Interpolation Registers

Interpolation adjustment	Gamma Set A		Gamma Set B		Gamma Set C	
	Positive Polarity	Negative Polarity	Positive Polarity	Negative Polarity	Positive Polarity	Negative Polarity
V2, V3	PI0P0 [1:0]	PI0N0 [1:0]	PI1P0 [1:0]	PI1N0 [1:0]	PI2P0 [1:0]	PI2N0 [1:0]
V60, V61	PI0P1 [1:0]	PI0N1 [1:0]	PI1P1 [1:0]	PI1N1 [1:0]	PI2P1 [1:0]	PI2N1 [1:0]

Table 38 Interpolation Factor for V2 and V3

(See "Grayscale Voltage Calculation Formula" for the levels)

PI**0[1:0]	IPV2	IPV3
2'h0	61.9%	28.6%
2'h1	49.6%	22.9%
2'h2	33.9%	15.7%
2'h3	29.9%	13.8%

Table 39 Interpolation Factor for V60 and V61

(See "Grayscale Voltage Calculation Formula" for the levels)

PI**1[1:0]	IPV60	IPV61
2'h0	71.4%	38.1%
2'h1	77.1%	50.4%
2'h2	84.3%	66.1%
2'h3	86.2%	70.1%

Note: ** indicates 0P/0N/1P/1N/2P/2N.

Table 40 How to calculate grayscale voltages

Grayscale voltages	Formulas	Grayscale voltages	Formulas
V0	See reference level selection table	V32	V43 + (V20 - V43) x 11/23
V1	See reference level selection table	V33	V43 + (V20 - V43) x 10/23
V2	V4 + (V1 - V4) x IPV2	V34	V43 + (V20 - V43) x 9/23
V3	V4 + (V1 - V4) x IPV3	V35	V43 + (V20 - V43) x 8/23
V4	See reference level selection table	V36	V43 + (V20 - V43) x 7/23
V5	V8 + (V4 - V8) x 29/40	V37	V43 + (V20 - V43) x 6/23
V6	V8 + (V4 - V8) x 19/40	V38	V43 + (V20 - V43) x 5/23
V7	V8 + (V4 - V8) x 9/40	V39	V43 + (V20 - V43) x 4/23
V8	See reference level selection table	V40	V43 + (V20 - V43) x 3/23
V9	V20 + (V8 - V20) x 11/12	V41	V43 + (V20 - V43) x 2/23
V10	V20 + (V8 - V20) x 10/12	V42	V43 + (V20 - V43) x 1/23
V11	V20 + (V8 - V20) x 9/12	V43	See reference level selection table
V12	V20 + (V8 - V20) x 8/12	V44	V55 + (V43 - V55) x 11/12
V13	V20 + (V8 - V20) x 7/12	V45	V55 + (V43 - V55) x 10/12
V14	V20 + (V8 - V20) x 6/12	V46	V55 + (V43 - V55) x 9/12
V15	V20 + (V8 - V20) x 5/12	V47	V55 + (V43 - V55) x 8/12
V16	V20 + (V8 - V20) x 4/12	V48	V55 + (V43 - V55) x 7/12
V17	V20 + (V8 - V20) x 3/12	V49	V55 + (V43 - V55) x 6/12
V18	V20 + (V8 - V20) x 2/12	V50	V55 + (V43 - V55) x 5/12
V19	V20 + (V8 - V20) x 1/12	V51	V55 + (V43 - V55) x 4/12
V20	See reference level selection table	V52	V55 + (V43 - V55) x 3/12
V21	V43 + (V20 - V43) x 22/23	V53	V55 + (V43 - V55) x 2/12
V22	V43 + (V20 - V43) x 21/23	V54	V55 + (V43 - V55) x 1/12
V23	V43 + (V20 - V43) x 20/23	V55	See reference level selection table
V24	V43 + (V20 - V43) x 19/23	V56	V59 + (V55 - V59) x 31/40
V25	V43 + (V20 - V43) x 18/23	V57	V59 + (V55 - V59) x 21/40
V26	V43 + (V20 - V43) x 17/23	V58	V59 + (V55 - V59) x 11/40
V27	V43 + (V20 - V43) x 16/23	V59	See reference level selection table
V28	V43 + (V20 - V43) x 15/23	V60	V62 + (V59 - V62) x IPV60
V29	V43 + (V20 - V43) x 14/23	V61	V62 + (V59 - V62) x IPV61
V30	V43 + (V20 - V43) x 13/23	V62	See reference level selection table
V31	V43 + (V20 - V43) x 12/23	V63	See reference level selection table

Note: Theoretical values are obtained from the calculation formulas.

Frame Memory Data and Grayscale Voltage

Table 41

Frame memory data	Grayscale voltage				Frame memory data	Grayscale voltage			
	REV = 1		REV = 0			REV = 1		REV = 0	
	Positive	Negative	Positive	Negative		Positive	Negative	Positive	Negative
6'h00	V0	V63	V63	V0	6'h20	V32	V31	V31	V32
6'h01	V1	V62	V62	V1	6'h21	V33	V30	V30	V33
6'h02	V2	V61	V61	V2	6'h22	V34	V29	V29	V34
6'h03	V3	V60	V60	V3	6'h23	V35	V28	V28	V35
6'h04	V4	V59	V59	V4	6'h24	V36	V27	V27	V36
6'h05	V5	V58	V58	V5	6'h25	V37	V26	V26	V37
6'h06	V6	V57	V57	V6	6'h26	V38	V25	V25	V38
6'h07	V7	V56	V56	V7	6'h27	V39	V24	V24	V39
6'h08	V8	V55	V55	V8	6'h28	V40	V23	V23	V40
6'h09	V9	V54	V54	V9	6'h29	V41	V22	V22	V41
6'h0A	V10	V53	V53	V10	6'h2A	V42	V21	V21	V42
6'h0B	V11	V52	V52	V11	6'h2B	V43	V20	V20	V43
6'h0C	V12	V51	V51	V12	6'h2C	V44	V19	V19	V44
6'h0D	V13	V50	V50	V13	6'h2D	V45	V18	V18	V45
6'h0E	V14	V49	V49	V14	6'h2E	V46	V17	V17	V46
6'h0F	V15	V48	V48	V15	6'h2F	V47	V16	V16	V47
6'h10	V16	V47	V47	V16	6'h30	V48	V15	V15	V48
6'h11	V17	V46	V46	V17	6'h31	V49	V14	V14	V49
6'h12	V18	V45	V45	V18	6'h32	V50	V13	V13	V50
6'h13	V19	V44	V44	V19	6'h33	V51	V12	V12	V51
6'h14	V20	V43	V43	V20	6'h34	V52	V11	V11	V52
6'h15	V21	V42	V42	V21	6'h35	V53	V10	V10	V53
6'h16	V22	V41	V41	V22	6'h36	V54	V9	V9	V54
6'h17	V23	V40	V40	V23	6'h37	V55	V8	V8	V55
6'h18	V24	V39	V39	V24	6'h38	V56	V7	V7	V56
6'h19	V25	V38	V38	V25	6'h39	V57	V6	V6	V57
6'h1A	V26	V37	V37	V26	6'h3A	V58	V5	V5	V58
6'h1B	V27	V36	V36	V27	6'h3B	V59	V4	V4	V59
6'h1C	V28	V35	V35	V28	6'h3C	V60	V3	V3	V60
6'h1D	V29	V34	V34	V29	6'h3D	V61	V2	V2	V61
6'h1E	V30	V33	V33	V30	6'h3E	V62	V1	V1	V62
6'h1F	V31	V32	V32	V31	6'h3F	V63	V0	V0	V63

Power Supply Generating Circuit

The following figure shows the configuration of LCD drive voltage generating circuit of the R61526.

Power Supply Circuit Connection Example

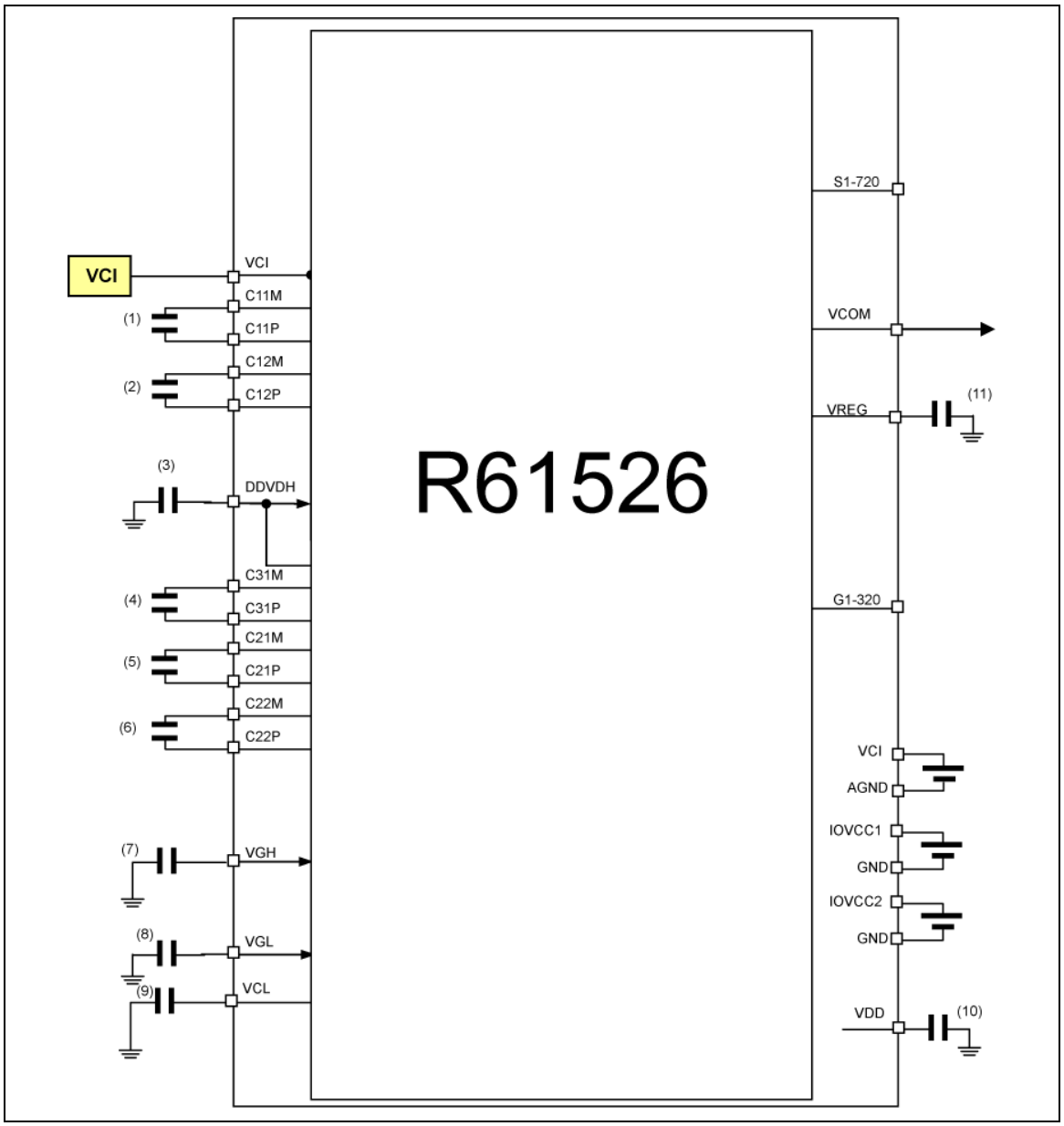


Figure 50

Specifications of External Elements Connected to the Power Supply Circuit

The following table shows specifications of external elements connected to the R61526's power supply circuit. The numbers of the pins to connect correspond to the numbers shown in Power Supply Generating Circuit.

Table 42 Capacitor Connected to LCD Power Supply Circuit

Capacity	Recommended voltage	Pin to connect
1µF (B characteristics)	6V	(1)C11P/M, (2)C12P/M (4)C31P/M, (9)VCL, (10)VDD, (11)VREG
	10V	(3)DDVDH, (5)C21P/M, (6)C22P/M
	25V	(7)VGH, (8)VGL

Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the R61526 and the relationship between TFT display application voltage waveforms and electrical potential.

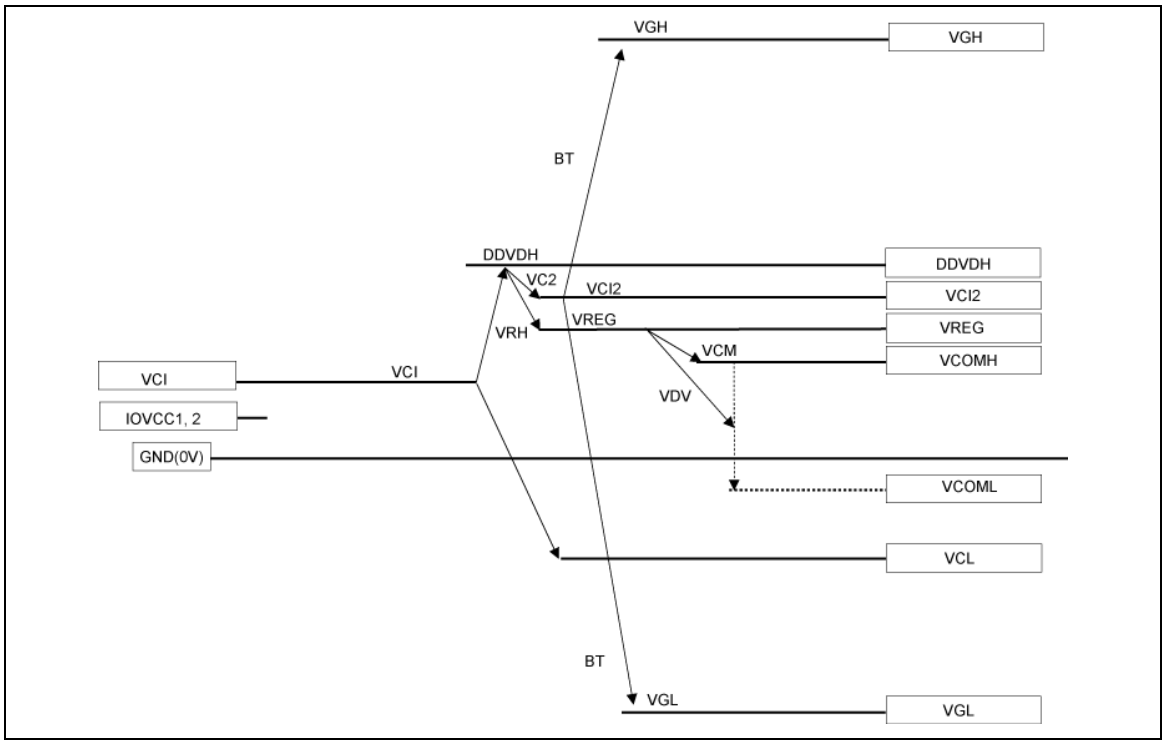


Figure 51 Voltage Setting Pattern Diagram

Note: The DDVDH, VGH, VGL, VCL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at respective outputs. When the alternating cycle of VCOM is high (e.g. polarity inverts every line cycle), current consumption will increase.

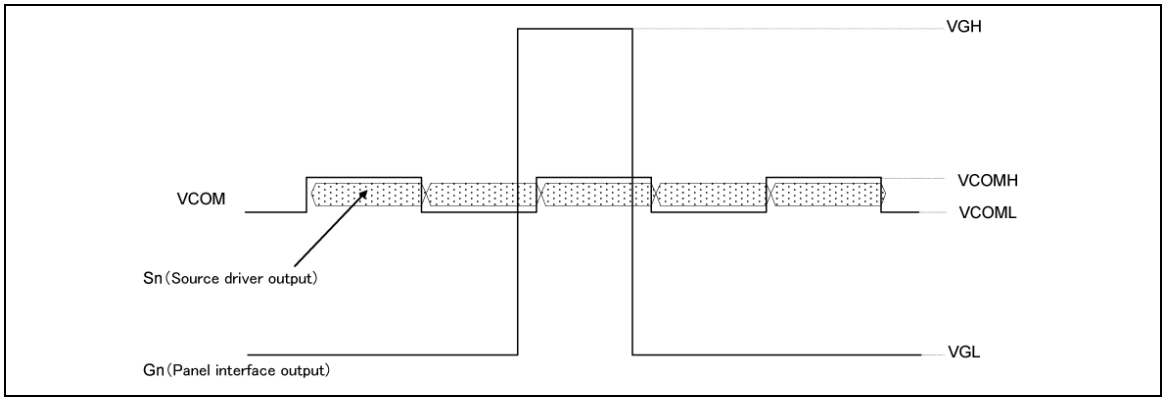


Figure 52 Voltage Application to TFT Display

NVM Control

The R61526 incorporates 896-bit NVM for user's use to store

- 24-bit Supplier ID (read by DDB_start command)
- Manufacturer Command values

To write, read and erase data from/to the NVM, follow below sequences. Data written to the NVM is loaded to the registers automatically when the sequences below are executed. The command used to update data by loading from NVM to registers depends on NVM Load Control command (E2h).

- Power On sequence
- HW RESET sequence
- exit_sleep_mode sequence
- soft_reset sequence

NVM data is retained after power supply is turned off.

The following commands are stored in NVM.

Table 43

List of Command stored in NVM
04h : P1~P3
A1h : P1~P3
B3h : P1~P5
B4h : P1
C0h : P1~P8
C1h : P1~P5
C3h : P1~P5
C4h : P1~P5
C8h : P1~P22
C9h : P1~P22
CAh : P1~P22
D0h : P1~P6
D1h : P1~P3
D2h : P1~P2
D4h : P1~P2

E2h LDx (E2h) controls commands used to load data from NVM.

LD0 : User Command : 04h, A1h
LD1 : Manufacturer Command : B3~B4h (I/F and Frame-Memory Control)
LD2 : Manufacturer Command : None
LD3 : Manufacturer Command : C0~C4h (Panel Drive and Display Timing Setting)
LD4 : Manufacturer Command : D0~D4h (Power Setting)
LD5 : Manufacturer Command : C8~CAh (Gamma Setting)

NVM Write Sequence

Among user/Manufacturer commands, register values that should be stored into the NVM are written. When “1” is written to these bits, the bits are set to “1”. The default value is “0”. Write “0” to bits that will not be written.

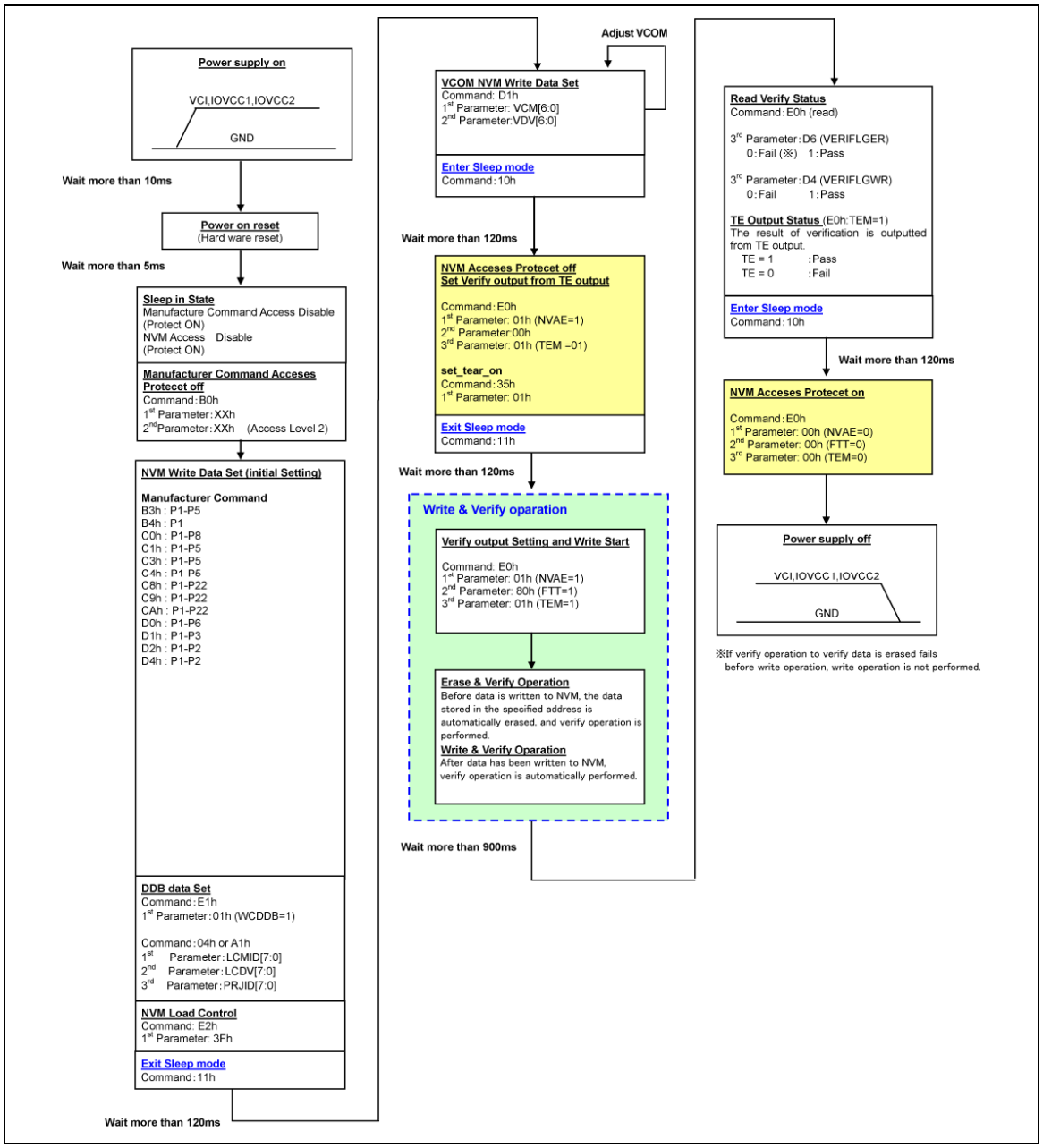


Figure 53

Absolute Maximum Rating

Table 44

Item	Symbol	Unit	Ratings	Note
Power supply voltage 1	IOVCC1, IOVCC2	V	-0.3 ~ +4.6	1, 2
Power supply voltage 2	VCI – AGND	V	-0.3 ~ +4.6	1, 3
Power supply voltage 3	DDVDH – AGND	V	-0.3 ~ +6.5	1, 4
Power supply voltage 4	AGND – VCL	V	-0.3 ~ +4.6	1
Power supply voltage 5	AGND– VGL	V	-0.3 ~ +13.0	1, 6
Power supply voltage 6	VGH– VGL	V	-0.3 ~ +30.0	1
Power supply voltage 7	VCI – VCL	V	-0.3 ~ +6.6	1, 7
Input voltage	Vt	V	-0.3 ~ IOVCC1 + 0.3	1
Operating temperature	Topr	C	-40 ~ +85	1, 8
Storage temperature	Tstg	C	-55 ~ +110	1

Notes: 1. If used beyond the absolute maximum ratings, the LSI may be destroyed. It is strongly recommended to use the LSI within the limits of its electrical characteristics during normal operation. The reliability of LSI is not guaranteed if used in the conditions above the limits and it may lead to malfunction.

2. Make sure (High) IOVCC1 ≥ GND (Low) and (High) IOVCC2 ≥ GND (Low).
3. Make sure (High) VCI ≥ AGND (Low).
4. Make sure (High) DDVDH ≥ AGND (Low).
5. Make sure (High) DDVDH ≥ VCL (Low).
6. Make sure (High) AGND ≥ VGL (Low).
7. Make sure (High) VCI ≥ VCL (Low).

Electrical Characteristics

DC Characteristics

Table 45 IOVCC1=1.65V~3.30V, Ta=-40C ~ +85C

Item		Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input “High” level voltage 1 Interface pin (Except for RESX)		V_{IH1}	V	IOVCC1=1.65V～3.30V	0.80× IOVCC1	–	IOVCC1	1,2
Input “Low” level voltage 1 Interface pin (Except for RESX)		V_{IL1}	V	IOVCC1=1.65V～3.30V	0	–	0.20× IOVCC1	1,2
Input “High” level voltage 2 RESX pin		V_{IH2}	V	IOVCC1=1.65V～3.30V	0.90× IOVCC1	–	IOVCC1	1,2
Input “Low” level voltage 2 RESX pin		V_{IL2}	V	IOVCC1=1.65V～3.30V	0	–	0.10× IOVCC1	1,2
Output “High” level voltage 1 (DB[17:0], TE)		V_{OH1}	V	IOVCC1=1.65V～3.30V, IOH=-0.1mA	0.8× IOVCC1	–	–	1
Output “Low” level voltage 1 (DB[17:0], TE)		V_{OL1}	V	IOVCC1=1.65V～3.30V, IOL=0.1mA	–	–	0.20× IOVCC1	1
Output “High” level voltage 2 (LEDPWM)		V_{OH1}	V	IOVCC2=1.65V～3.30V, IOH=-0.1mA	0.8× IOVCC2	–	–	1
Output “Low” level voltage 2 (LEDPWM)		V_{OL1}	V	IOVCC2=1.65V～3.30V, IOL=0.1mA	–	–	0.20× IOVCC2	1
Bus interface pin input/output leakage current		I_{LI1}	μA	Vin=0～IOVCC1	-1	–	1	4
IM pin input/output leakage current (connected to IOVCC1 via pulled-up resistor)		I_{LI2}	μA	IOVCC1=1.65V(Typ.),3.30V (Max.), Vin=0V	0	0.15	1.2	
		I_{LI3}	μA	IOVCC1=1.65V～3.30V, Vin=IOVCC1	-1	–	1	
Current consumption (IOVCC1-GND)	Normal mode (262,144-color display operation)	I_{OP1}	μA	IOVCC1=1.80V, VCI=2.80V, Ta=25℃, 320-line drive, RTN=28h, FP=BP=8h, frame inversion, frame memory data: 8’h00000 except Pull up current of IM pin.	–	550	750	5,6
	Idle mode (64-line partial display)	I_{op2}	μA	IOVCC1=1.80V, VCI=2.80V, Ta=25℃, 64-line partial display, RTN=28h, FP=BP=8h, frame inversion, frame memory data: 18h’00000, except Pull Up current of IM pin.	–	450	650	5,6
	Sleep mode	I_{ST}	μA	IOVCC1=1.80V, VCI=2.80V, Ta=25℃, except Pull Up current of IM pin.	–	10	50	5,6

	Deep Sleep mode	I_{DST}	μA	IOVCC1=1.80V, VCI=2.80V, Ta=25℃, except Pull Up current of IM pin.	–	0.1	1	5,6
	Frame memory access mode	I_{RAM}	mA	IOVCC1=1.80V, VCI=2.80V, tCYCW=70ns, Ta=25C, consecutive frame memory access during display operation. 8bits x 2 transfer Write data: 18'h00000	–	1.9	2.6	5,6
Liquid crystal power supply current （VCI-AGND）	262,144-color display operation (Normal mode+Idle mode off)	Ici1	mA	IOVCC1=1.8V, VCI=2.8V, Ta=25℃, 320-line drive, RTN=28h, FP=BP=8h, VC2[2:0]=2h , BT1[2:0]=6h, DC0x[2:0]=2h, DC1x[2:0]=2h, frame inversion, frame memory data: 18'h00000, no load on the panel	–	1.8	2.8	5,6
	8-colors (64-line partial) Display operation (Partial mode+Idle mode on)	Ici2	mA	IOVCC1=1.8V, VCI=2.8V, Ta=25℃, 64-line partial display, RTN=3Ch, FP=BP=8h, VC2[2:0]=2h, BT1[2:0]=6h, DC0x[2:0]=2h, DC1x[2:0]=2h, frame inversion, frame memory data: 18'h00000, no load on the panel	–	0.65	0.95	5,6
Output voltage dispersion	V0～V63	ΔVO	mV	–	–	–	40	7
Average Output Variance		ΔVΔ	mV	–	−35	–	+35	8

Step-up Circuit Characteristics

Table 46 Step-up Circuit Characteristics

Item		Unit	Test condition	Min.	Typ.	Max.	Note
Step-up Output Voltage	DDVDH	V	Ta=25℃, IOVCC1=1.8V, VCI=2.8V, VC2[2:0]=2h, BT1[2:0]=6h, DC0x[2:0]=2h, DC1x[2:0]=2h, RTN0[5:0]=28h, NL[6:0]=4Fh, FP0[7:0]=8h, BP0[7:0]=8h, C11=C12=C21=C22=C31=1uF/B characteristics, DDVDH=VGH=VGL=VCL=1uF/B characteristics, Iload1=-3mA, no load on the panel.	5.30	5.45	-	Step-up Output Voltage
	VGH	V	Ta=25℃, IOVCC1=1.8V, VCI=2.8V, VC2[2:0]=2h, BT1[2:0]=6h, DC0x[2:0]=2h, DC1x[2:0]=2h, RTN0[5:0]=28h, NL[6:0]=4Fh, FP0[7:0]=8h, BP0[7:0]=8h, C11=C12=C21=C22=C31=1uF/B characteristics, DDVDH=VGH=VGL=VCL=1uF/B characteristics, Iload2=-100uA, no load on the panel.	12.00	12.40	-	
	VGL	V	Ta=25℃, IOVCC1=1.8V, VCI=2.8V, VC2[2:0]=2h, BT1[2:0]=6h, DC0x[2:0]=2h, DC1x[2:0]=2h, RTN0[5:0]=28h, NL[6:0]=4Fh, FP0[7:0]=8h, BP0[7:0]=8h, C11=C12=C21=C22=C31=1uF/B characteristics, DDVDH=VGH=VGL=VCL=1uF/B characteristics, Iload3=+100uA, no load on the panel.	-	-9.60	-9.20	
	VCL	V	Ta=25℃, IOVCC1=1.8V, VCI=2.8V, VC2[2:0]=2h, BT1[2:0]=6h, DC0x[2:0]=2h, DC1x[2:0]=2h, RTN0[5:0]=28h, NL[6:0]=4Fh, FP0[7:0]=8h, BP0[7:0]=8h, C11=C12=C21=C22=C31=1uF/B characteristics, DDVDH=VGH=VGL=VCL=1uF/B characteristics, Iload4=+200uA, no load on the panel	-	-2.70	-2.65	

Power Supply Voltage Range

Table 47 Power Supply Voltage Range (Ta=-40C ~ +85C, GND=AGND=0V)

Item	Symbol	Unit	Min.	Typ.	Max.	Condition
Power supply voltage	IOVCC1	V	1.65	1.80	3.30	-
Power supply voltage	IOVCC2	V	1.65	1.80	3.30	-
Power supply voltage	VCI	V	2.50	2.80	3.30	-

Output Voltage Range

Table 48 Output Voltage Range (Ta=-40C ~ +85C, GND=AGND=0V)

Item	Symbol	Unit	Min.	Typ.	Max.	Condition
Grayscale, VCOM reference voltage	VREG	V	-	-	DDVDH-0.5	-
Source driver		V	GND+0.2	-	VREG	-
VCOMH Output	VCOMH	V	3.0	-	VREG	-
VCOML Output	VCOML	V	VCL+0.5	-	0.0	-
VCOM amplitude		V	-	-	6.0	-
Step-up Output	DDVDH	V	5.0	-	5.8	-
Step-up Output	VGH	V	10.0	-	18.0	-
Step-up Output	VGL	V	-13.0	-	-4.5	-
Step-up Output	VCL	V	-3.3	-	-1.9	-
Voltage between VCI-VCL		V	-	-	6.6	-
Voltage between VGH-VGL		V	-	-	28.0	-

AC Characteristics

(IOVCC1=1.65V ~ 3.30V, Ta=-40C ~ +85C)

Clock Characteristics

Table 49 Clock Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.
RC oscillation clock	fosc	kHz	IOVCC=1.8V, 25C	744	800	856

DBI Type B (18/16/9/8 Bits) Timing Characteristics

Table 50 1, 3/2, 2, 3 – Transfer, IOVCC1=1.65V ~ 3.30V

Item	Symbol		Unit	Test condition	Min.	Max.
Address Setup Time	DCX	tast	ns		0	-
Address Hold Time (Write/Read)		taht	ns		10	-
Chip Select Setup Time (Write)	CSX	tcs	ns		30	-
Chip Select Setup Time (Read ID)		trcs	ns		270	-
Chip Select Setup Time (Read FM)		trcfm	ns		270	
Chip Select Wait Time (Write/Read)		tcsf	ns		20	-
Write Cycle Time	WRX	twc	ns		66	-
Write Control Pulse ”High” Period		twrh	ns		22	-
Write Control Pulse ”Low” Period		twrl	ns		25	-
ID Read Cycle Time	RDX	trcs	ns		600	-
ID Read Control Pulse ”High” Period		trdhs	ns		270	-
ID Read Control Pulse ”Low” Period		trdls	ns		270	-
FM Read Cycle Time	RDX	trcfm	ns		600	-
FM Read Control Pulse ”High” Period		trdhfm	ns		270	-
FM Read Control Pulse ”Low” Period		trdlfm	ns		270	-
Write Data Setup Time	DB[17:0]	twds	ns	CL Max.30pF Min.8pF	15	-
Write Data Hold Time		twdh	ns		20	-
ID Read Access Time		traccs	ns		10	250
FM Read Access Time		traccfm	ns		10	250
Output Disable Time		trod	ns		10	-
Rise/Fall Time	-	tr/tf	ns		-	15

Notes: 1 transfer: (1)16-bit I/F 16 bits/pixel, (2)18 bits I/F 18 bits/pixel
3/2- transfer: (1)16-bit I/F 18 bits/pixel Option1
2 transfer: (1)8-bit I/F 16 bits/pixel, (2) 9-bit I/F 18 bits/pixel
3 transfer: (1)8-bit I/F 18 bits/pixel, (2)18 bits I/F 18 bits/pixel Option 2

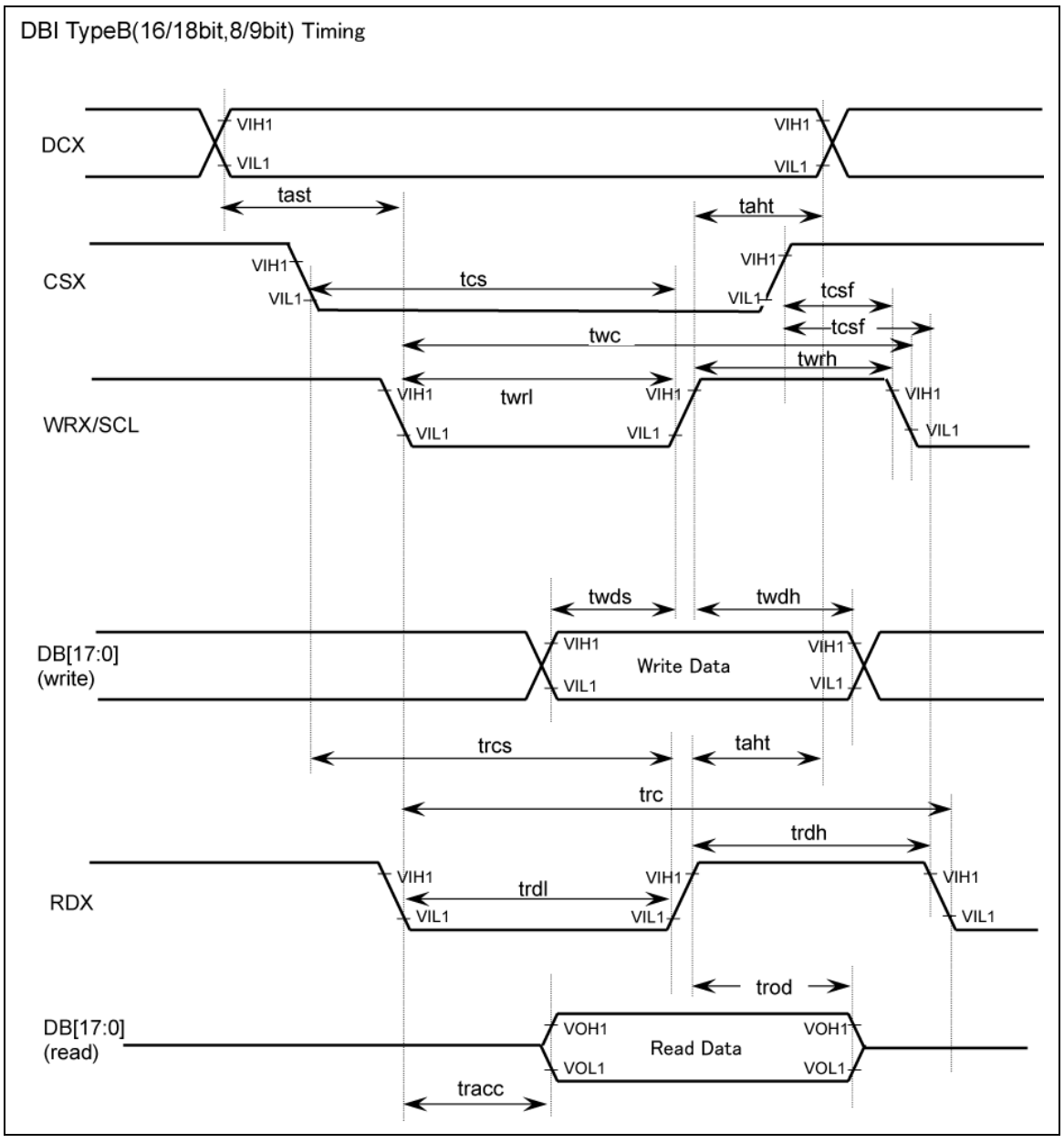


Figure A DBI Type B

DBI Type C Timing Characteristics

Table 51 (IOVCC1=1.65V ~ 3.30V)

Item	Symbol		Unit	Test condition	Min..	Max.
Chip Select Setup Time	CSX	tcss	ns		40	-
Chip Select Hold Time		tcsh	ns		40	-
Chip Select High Pulse Width		tchw	ns		100	
Address Setup Time	DCX	tas	ns		10	-
Address Hold Time (Write/Read)		tah	ns		10	-
Write Cycle Time	WRX/SCL (Write)	twc	ns		100	-
WRX/SCL"High" Period (Write)		twrh	ns		40	-
WRX/SCL"Low" Period (Write)		twrl	ns		40	-
Read Cycle Time	WRX/SCL (Read)	trc	ns		380	-
WRX/SCL"High" Period (Read)		trdh	ns		170	-
WRX/SCL"Low" Period (Read)		trdl	ns		170	-
Data Setup Time	DIN	tds	ns		30	-
Data Hold Time		tdh	ns		30	-
Access Time	DOUT	tacc	ns	CL Max.30pF Min.8pF	-	150
Output Disable Time		tod	ns		10	-
Rise/Fall Time	-	tr/tf	ns		-	15

Note: Address setup and address hold times are defined for Option 3 only.

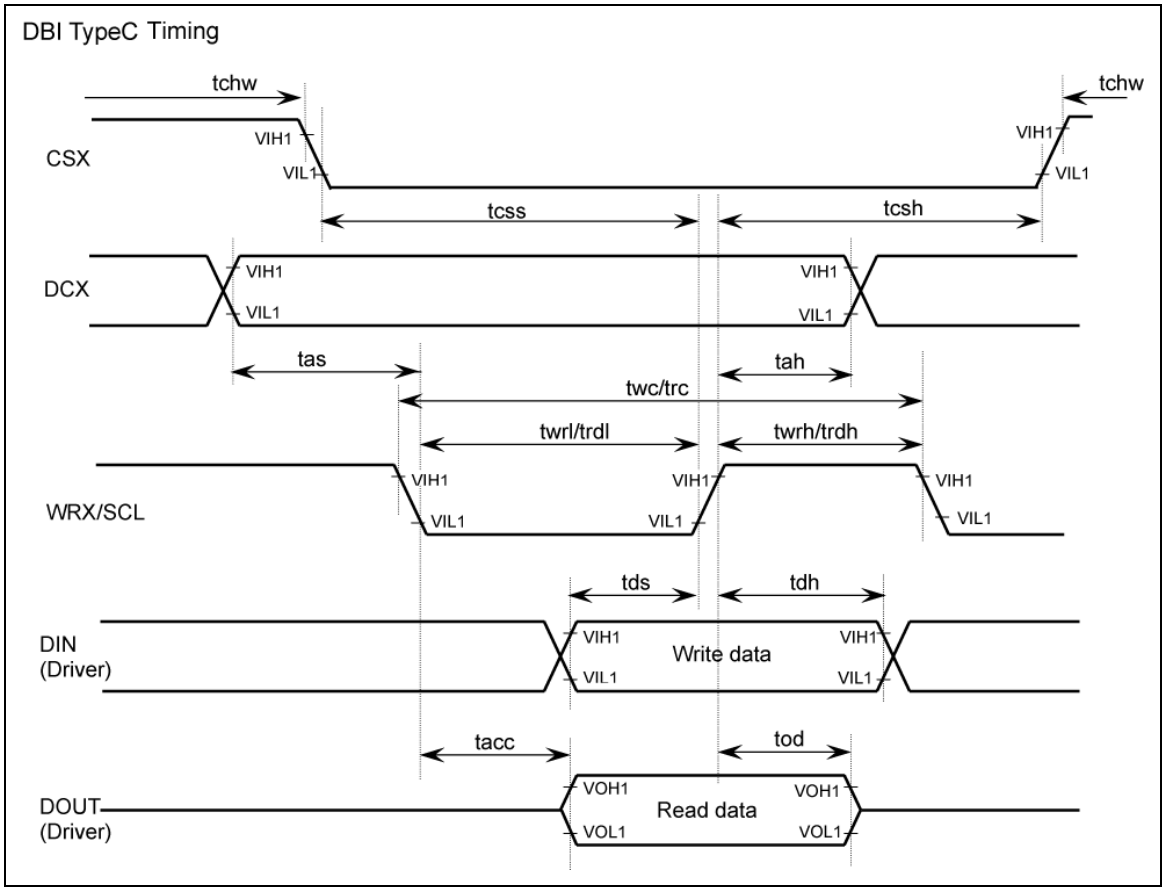


Figure B DBI Type C Timing

DPI Timing Characteristics

Table 52 (IOVCC1 = 1.65V ~ 3.30V) [Target Spec]

Item	Symbol		Unit	Test condition	Min.	Max.
VSYNC Setup Time	VSYNC	tvss	Ns		30	-
VSYNC Hold Time		tvsh	Ns		30	-
HSYNC Setup Time	HSYNC	thss	Ns		30	-
HSYNC Hold Time		thsh	Ns		30	-
Pixel Clock Cycle Time	DOTCLK	tpclkcyc	Ns		100	-
Pixel Clock "Low" Period		tpclkl	Ns		30	-
Pixel Clock "High" Period		tpclkh	Ns		30	-
Data Setup Time	DB[17:0] or DB[15:0] ENABLE	tds	Ns		30	-
Data Hold Time		tdh	Ns		30	-
Rise/ Fall Time	-	tr/tf	Ns		-	15

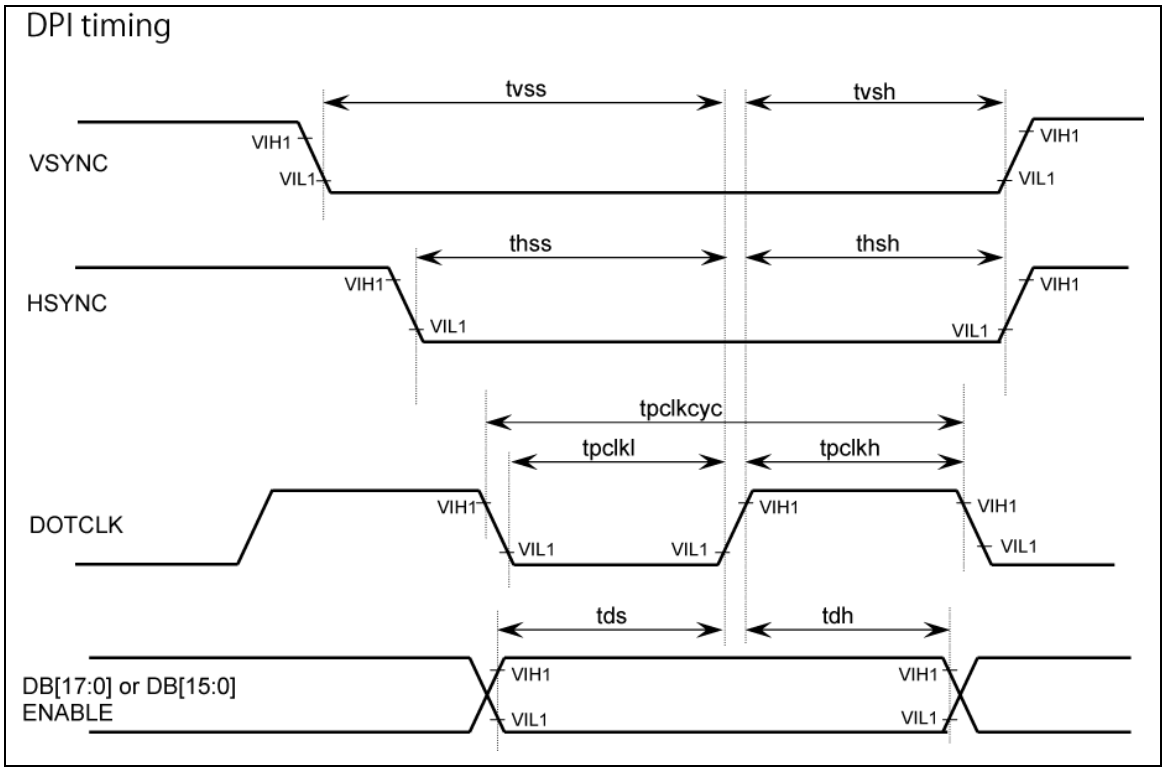


Figure C DPI Timing

Reset Timing Characteristics

Table 53 Reset Timing Characteristics (IOVCC1=1.65V ~ 3.30V, Ta=-40C ~ +85C)

Item	Symbol	Unit	Test Condition	Min.	Max.
Reset ”Low” Level Width 1	tRW1	ms	Power supply input	1	—
Reset ”Low” Level Width 2	tRW2	us	Operation	10	—
Reset Time	tRT	ms		—	5

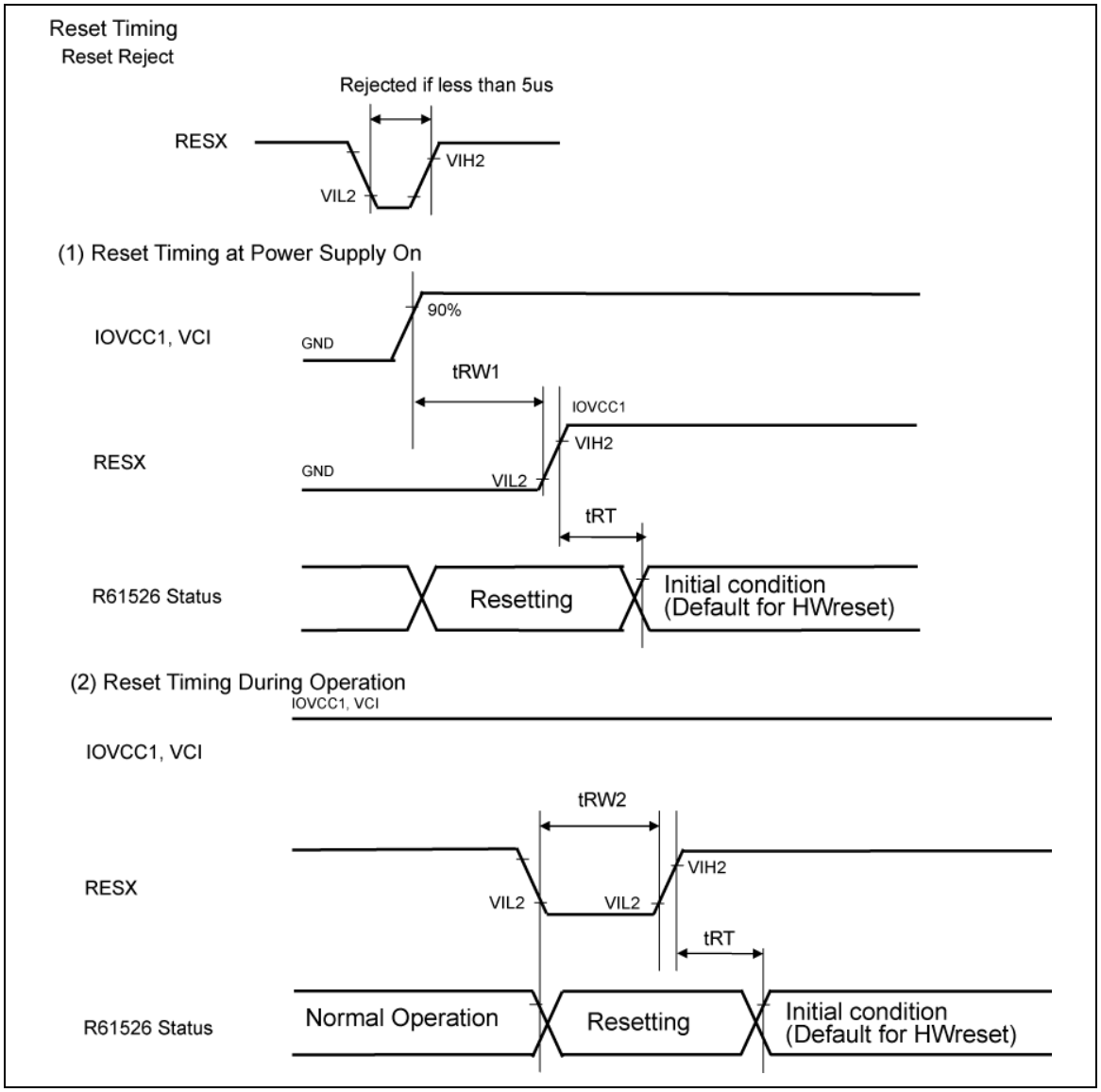


Figure D Reset Timing

Liquid Crystal Driver Output Characteristics

Table 54 Liquid Crystal Driver Output Characteristics

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
VCOM output delay time	tddv	us	Ta=25℃, IOVCC1=1.8V, VCI=2.8V VCM[6:0]=7Fh, VDV[6:0]=63h VEQW[2:0]=0h, VEM[1:0]=0h, MCP[2:0]=1h RTN0[5:0]=28h, NL[6:0]=4Fh, FP0[7:0]=8h, BP0[7:0]=8h DDVDH=5.6V, VCL=-2.8V, VREG=5.0V, VGS=0.0V DDVDH=VCL=VREG=1uF/B characteristics Time to reach ±35m from VCOM alternating point. Load resistance R=100ohm, Load capacitance C=10nF	-	-	25	9
Source driver output delay time	tdds	us	Ta=25℃, IOVCC1=1.8V, VCI=2.8V SDT[2:0]=1h, SPCW[2:0]=0h RTN0[5:0]=28h, NL[6:0]=4Fh, FP0[7:0]=8h, BP0[7:0]=8h DDVDH=5.6V, VCL=-2.8V, VREG=5.0V, VGS=0.0V DDVDH=VCL=VREG=1uF/B characteristics Same change from the same grayscalse on all pins. Time to reach the target voltage ± 35mV when changing V0 ⇔ v63 load resistance R=10kohm, Load capacitance C=20pF	-	-	25	10

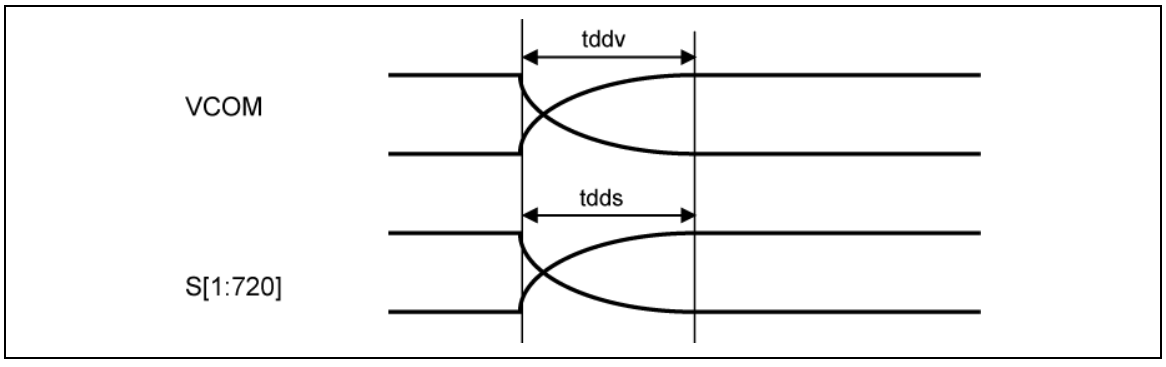


Figure E Liquid Crystal Driver Output Timing

NVM Operating Characteristics [Target Spec]

Table 55

Operation	Power Supply Voltage		Time	Temperature
Write Sequence	VCI	2.60 ~ 3.00V	Write operation period: 900ms	+20C ~ +30C
	IOVCC1	1.650 ~ 3.30V		

Note: Data rewrite is limited up to 5 times.

Notes to Electrical Characteristics

Note 1: DC/AC electrical characteristics of bare die and wafer are guaranteed at +85C.

Note 2: The following figures illustrate the configurations of input, I/O, and output pins.

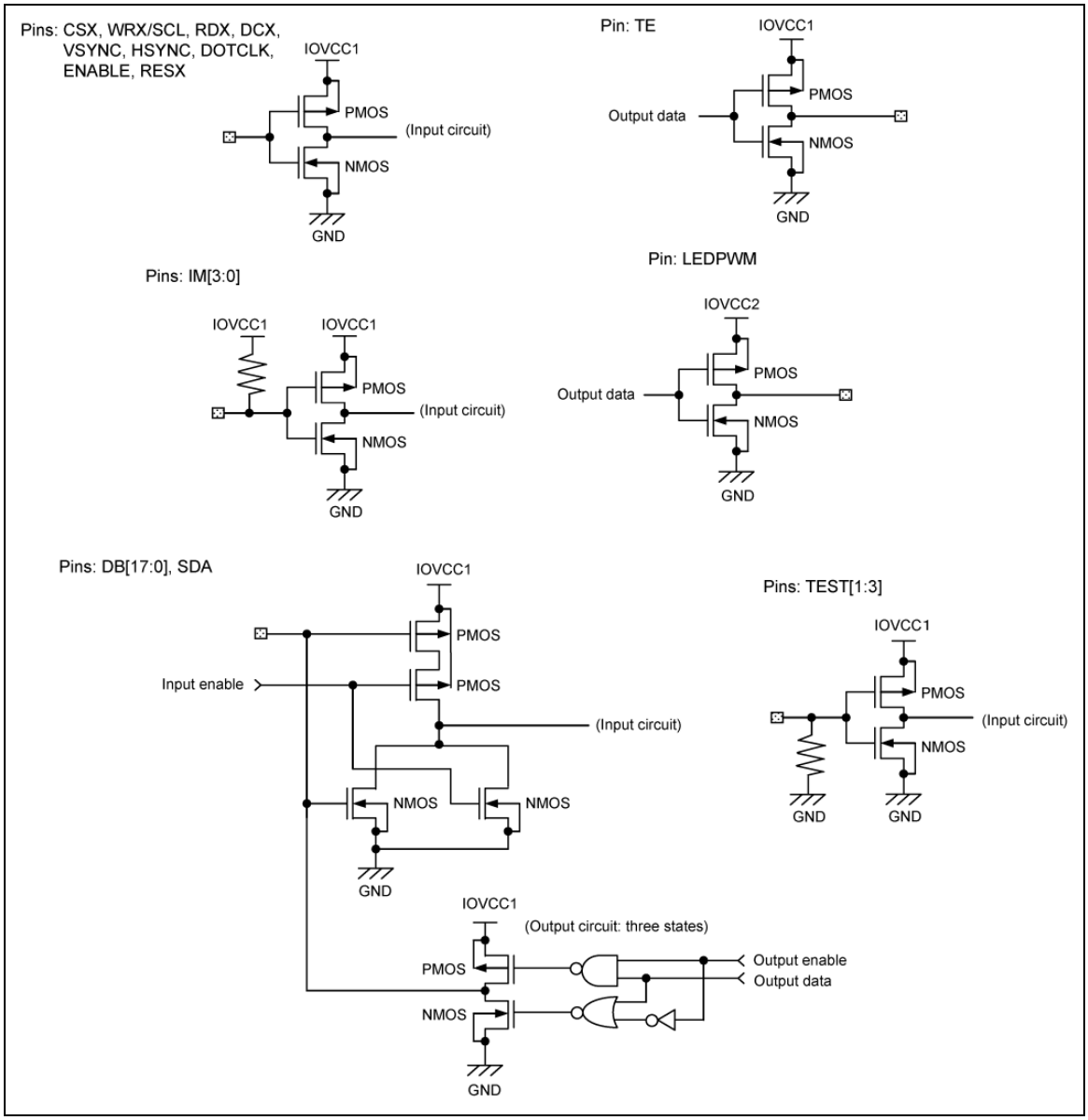


Figure 54

Note 3: Leave TEST[1:3] open.

Note 4: This excludes the current in the output drive MOS.

Note 5: This excludes the current in the input/output units. Make sure that the input level is fixed because through current will increase in the input circuit when the CMOS input level takes a middle range level. The current consumption is unaffected by whether the CSX pin is “high” or “low” while not accessing via interface pins.

Note 6: This is average current value.

Note 7: The output voltage deviation is the difference in the voltages between output pins that are placed side by side in the same display mode. The output voltage deviation is reference value.

Note 8: The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for one chip with same display data.

Note 9: VCOM output delay time depends on load on the liquid crystal panel. Therefore, frame frequency and one line cycle need to be specified checking image quality on the panel to be used.

Note 10: LCD driver output delay time depends on load on the liquid crystal panel. Therefore, frame frequency and one line cycle need to be specified checking image quality on the panel to be used.

Revision Record

Rev.	Date	Page No	Contents of Modification
0.01	2009/08/07		First issue
0.02	2009/10/2	9	Table 1: DDVDH 4.5~6.0V → 5.0~6.0V
		15	Table 6 Bus Interface: Amplitude IOVCC~GND→ IOVCC1~GND RDX when not used IOVCC → IOVCC1 SDA when not used IOVCC → IOVCC1 DB[17:0] when not used IOVCC or GND→ IOVCC1 or GND or OPEN
		16	Table7 Mode Select Pin (Amplitude IOVCC-GND → IOVCC1~GND) Table 8 LED Driver Control Pin (Amplitude: TBD-GND → IOVCC2~GND)
		18	Table 11: VTEST pin deleted. AGNDDUM, VCIDUM, VGSDUM added. DUMMYR1-2 added. GUMMYG1-4 and DUMMYS1-6 → DUMMY.
		19	Pad arrangement, wiring example drawn on the same page.
		20	62□m x 60□m (I/O, No.1-185)→ 40□m x 56□m (I/O side, No.1-232) 14□m x 85□m (LCD output side, No.186-1235) → 14□m x 104□m (Output to LCD, No 233-1278)
		21-33	PAD Coordinates Rev 0.0 (2009.7.17) →Rev 1.0 (2009.9.14)
		34	Bump arrangement: Bump size changed.
		56	Command List: 51h, 52h, 53h, 54h, 55h, 56h, 5Eh, 5Fh and 68h added.
		57	C8h Gamma Set A W/R 20 → C8h~CBh Gamma Set A~D W 22 D8h deleted.
		60-61	Command Accessibility List: 51h, 52h, 53h, 54h, 55h, 56h, 5Eh, 5Fh and 68h added.
		62	B1h deleted. BAh deleted.
		68	51h~68h added. B8h 16th~19th added.
		95	26h (Gamma Set) added.
		121	set_tear_scanline (44h): 1st parameter, DB2~7 X → 0
		124	Write Display Brightness (51h) inserted.
		125	Read Display Brightness (52h) inserted.
		126	Write CTRL Display (53h) inserted.
		128	Read CTRL Value Display (54h) inserted.
		129	Write Content Adoptive Brightness Control (55h) inserted.
		130	Read Content Adaptive Brightness Control (56h) inserted.
		131	Write CABC minimum brightness (5Eh) inserted.
		133	Read CABC minimum brightness (5Fh) inserted.
		132	Read Automatic Brightness Control Self-Diagnostic Result (68h) inserted.

Rev.	Date	Page No	Contents of Modification
		134	Read_DDB_Start (A1h): 3rd and 4th parameters added.
		135	Read ID1 (DAh) 2nd parameter added.
		136	Read ID2 (DBh) 2nd parameter added.
		137	Read ID3 (DCh) 2nd parameter added.
		145-146	Back Light Control 1 (B8h) 16~19th parameters added.
		155	Backlight Control 2 (B9h) 3rd and 4th parameters deleted.
		143 in rev 0.01	Backlight Control 3 (BAh) deleted.
		161	Description of PTDC added.
		171-172	C8h-CBh Gamma Set registers changed.
		174	VRH table: VREG_A → VREG
		178	DC00[2:0], DC02[2:0]: Step-up circuit 3 added.
		169 in rev 0.01	D8h Sequencer Control deleted.
		180	E0h: 4th parameter deleted. Registers in 1st ~ 3rd parameters changed.
		183	E2h LD[6:0]→LD[5:0]
		184	F0h Command table changed.
		212-213	Gamma registers changed. (gamma correction method changed)
		224	Absolute Maximum Rating: Table 38 inserted.
0.03	2009/11/6	6-7, 9, 75-77, 79, 83, 85, 87, 89, 91-92, 94-101, 103, 105, 107-108, 111-112, 114, 118-119, 121, 123-129, 131-141, 143, 146, 148, 156, 158, 159, 166, 171, 174, 176, 178, 183, 186,	Notation of DB corrected. (ex.: "17-0" changed to "[0:17]" ([x:y]: x < y))

Rev.	Date	Page No	Contents of Modification
		188-190	
		7	"IOVCC" changed to "IOVCC1," IOVCC2 added, VCL added as source driver liquid crystal drive/VCOM power supply, the number of bits for user identification code changed to 24, and that for VCOM level adjustment changed to 14.
		9, 11, 16, 48, 253	Notation of IM corrected. (ex.: "0-3" changed to "[3:0]" ([y:x]: x < y))
		9, 10, 13, 34, 199, 234, 252	Notation of S corrected. (ex.: "1-720" changed to "[1:720]" ([x:y]: x < y))
		9, 10, 13, 34, 199, 234	Notation of G corrected. (ex.: "1-320" changed to "[1:320]" ([x:y]: x < y))
		9	Spec for IOVCC1 ("IOVCC" changed to "IOVCC1") changed, and that for IOVCC2 added.
		10	"IOVCC" changed to "IOVCC1," and IOVCC2 added.
		11	"IOVCC" changed to "IOVCC1," method for setting IM3 pin changed, and "Voltage Range" changed to "IOVCC1 Voltage Range."
		12	"DDVDH" changed to "VREG." (error correction)
		14	Spec for IOVCC2 changed. (Description of connecting IOVCC1 added)
		15	"IOVCC" changed to "IOVCC1," "Synchronous clock signal in DBI Type C operation" and "Command/data select signal in DBI Type C (option 3) operation" interchanged, WRX" changed to "WRX/SCL", description related to DPI and "Low active" deleted from a spec for RDX, "DBT Type 1" changed to DBI Type C," and unused states of ENABLE and VSYNC changed to "IOVCC1 or GND."
		16	"IOVCC" changed to "IOVCC1," unused states of HSYNC and DOTCLK changed to "IOVCC1 or GND", note on current deleted from Table 6, and "by IOVCC2 amplitude" added in a spec for LEDPWM.
		18	Unused states of VREFC, VDDTEST, TEST1, TEST2, TEST3, and TSC changed to "IOVCC1 or GND", and functions of VREFC, VDDTEST, DUMMYR[1:2], TEST1, TEST2, TEST3, and TSC changed.
		19	The wiring example changed.
		20	Chip thickness changed to 280µm.
		48	IM[3:0] setting changed.
		52-54	Description of DPI added.
		55	PCLK changed to DOTCLK, DE changed to ENABLE, and the figures changed ("PCLK" changed to "DOTCLK (PCLK)", and "DE" changed to "ENABLE (DE)")
		76, 95	"millisecond" changed to "ms."
		87, 121, 144, 147, 162, 169, 171	"Setting disabled" changed to "Setting inhibited."
		142	Description of an arbitrary password added, and description of writing 3Fh in MCAP1 and MCAP2 changed.

Rev.	Date	Page No	Contents of Modification
		146	Description of SDOE added.
		156	PWMON changed to BCTRL, and description of PWM133 changed.
		157	Table of PWMDIV[7:0] changed.
		158	"1" changed to "0" (DB[7:5] of the 3rd parameter), "F5h" changed to "15h, and "05h" changed to "26h."
		159	"0" changed to "1" (DB4 of the 4th parameter and DB7 and DB5 of the 5th parameter).
		164	Table of PTS[2:0] and PTDC changed.
		165	"678kHz" changed to "800kHz. ."
		166	RTN0[5] and RTN2[5] added.
		168	Table of RTNn changed.
		174	"Gamma Set 0-3" changed to "Gamma Set A/B/C/D."
		177	Table of VRH[5:0] changed.
		179-180	Description and table of VCM[6:0] changed.
		181-182	Description and table of VDV[6:0] changed.
		183	"1" changed to "0" (DB[6:5] of the 1st parameter of D2h and D4h commands).
		184	Table of DC1x[2:0] and step-up clock frequency calculation changed.
		185	Table of DC0x[2:0] and step-up clock frequency calculation changed, and waveforms deleted.
		188	"WCDB" changed to "WCDDB." (error correction)
		189	Description of LDx added. (moved from "NVM Control")
		190	Table of commands changed.
		192	Figure of state transition diagram changed.
		193	Tables of operation mode transition sequence and display mode transition sequence added.
		195-196	Examples of power and display on/off sequences changed.
		197	Default register values deleted. (undefined)
		198	Transition sequence between internal clock operation and DPI operation changed.
		199	SDO added.
		207-214	Description of dynamic backlight control function added.
		217	Example of calculation changed.
		222	Calculation of frame memory write speed changed.
		223	Calculation of frame memory write speed. (See also the figure)
		234	"IOVCC" changed to "IOVCC1," and IOVCC2 and note added.
		235	"(11) VREG" moved from spec of capacity for 10V to that for 6V, and note added.
		236	"IOVCC" changed to "IOVCC1, 2."
		237	The number of bits in NVM corrected, "* bit" changed to "24-bit," "**h" changed to "E2h," description of supplier elective data and deep standby mode off sequence, and a table of restrictions on NVM control deleted.

Rev.	Date	Page No	Contents of Modification
		238	List of command stored in NVM and description below the table changed, and "**h" changed to "E2h."
		239	NVM write sequence added.
		240	"IOVCC" changed to "IOVCC1," and IOVCC2 added.
		241	"IOVCC" changed to "IOVCC1," the range of IOVCC1 changed, "Output ”High” level voltage 2" added, and typ. of IRAM changed (undefined).
		242	"IOVCC" changed to "IOVCC1," and Typ. of Ici1 and Ici2 changed. (undefined)
		243	"IOVCC" changed to "IOVCC1," step-up circuit characteristics changed (almost undefined), the range of IOVCC1 changed, and IOVCC2 added.
		244	"IOVCC" changed to "IOVCC1," VCOMH output (min.), the range of IOVCC1, and clock characteristics (min., typ., and max.) changed.
		246	Table (IOVCC1 = 1.95V-3.30V) added.
		247	Note deleted.
		248, 250	"IOVCC" changed to "IOVCC1," and the range of IOVCC1 changed.
		251	"IOVCC" changed to "IOVCC1," and the range of IOVCC1 changed, and the table of reset timing characteristics changed.
		252	"IOVCC" changed to "IOVCC1," and liquid Crystal Driver Output Characteristics and NVM operating characteristics changed.
		253	"IOVCC" changed to "IOVCC1," pin configurations of LEDPWM and TE changed.
0.04	2009/12/11	7	Description of Messi deleted.
		9	"(IM[2:0] = 100 or 111: 1.65V ~ 1.95V)" deleted.
		11	Table of IM[3:0] changed and description of range of IOVCC1 deleted.
		57-60	09h, DAh-DCh, and CBh deleted and note numbers changed due to deletion of note of Messi.
		62-63, 66, 68	Commands related to Messi (09h and DAh-DCh) deleted.
		77-80	09h command deleted.
		92	26h command deleted.
		131-133	DAh, DBh, and DCh commands deleted.
		150	Description of GIP changed. (GIP = 0: Setting inhibited)
		216, 218-221	CBh command deleted.
		229	Description of Messi deleted from a flow of "DDB data set."
		235	DBI Type B (18/16/9/8 bits) timing characteristics changed.
		239	Specs related to Messi (ID read) deleted.
0.05	2010/03/23	9	DDVDH: 5.0V~6.0V → 5.0V~5.8V VCL: -1.9V~-3.0V → -1.9V~-3.3V (error correction)
		11	IM[2:0] → I[3:0] (error correction) Description of IM[3:0] setting (1111) added.
		12	Description of DPI added in "2. External Display Interface." (error correction)
		16	Description of verify operation added as function of TE.

Rev.	Date	Page No	Contents of Modification
		18	DUMMYR[1:2]: connection resistance → contact resistance Short-circuited → Short-circuited to AGND Condition of contact resistance measurement added.
		21-33	Whole numbers changed to numbers with a decimal point. (no change in coordinates)
		48	"1111" (IM[3:0] setting) added.
		56-57	Description and figure of DPI format added.
		58	04h: 4 → 3 (number of parameters) 0Dh: "Note 1" deleted. 0Fh: (Bit 6 Only) → (Bits 7/6 Only)
		60	5Eh and 5Fh: Deleted. A1h: 4 → 3 (number of parameters)
		61	B1h: Added. B3h: 4 → 5 (number of parameters) BFh: 4 → 5 (number of parameters) C4h: 4 → 5 (number of parameters) D0h: 4 → 6 (number of parameters) D1h: 2 → 3 (number of parameters)
		63	0Eh: "DM=0 (Note)" → "Yes" (Command Accessibility excluding Sleep Mode On) 0Fh: "Yes" → "DM=0 (Note)" (Command Accessibility excluding Sleep Mode On) 26h: Deleted.
		64	5Eh: Deleted.
		65	B1h: No → Yes (Command Accessibility excluding Sleep Mode On) B4h: No → Yes (Sleep Mode On) C8h Gamma Set A → C8h~CAh Gamma Set A ~ C
		66	D8h: Deleted E0h, E1h, and E2h: Yes → No (Command Accessibility excluding Sleep Mode On), No → Yes (Sleep Mode On).
		67	04h: LCM ID → LCMID, LCD Ver → LCDVr, Prj ID → PRJID.
		68	2Bh: "B5=0: 1AFh" → "B5=0: 13Fh"
		69	5Eh and 5Fh: Deleted. 68h: D6=0,D7=0 → 00h A1h: LCM ID → LCMID, LCD Ver → LCDVr, Prj ID → PRJID.
		70	B0h: MCAP1=6'h3F → MCAP=2'h0, MCAPB=4'h0 (1st parameter) MCAP2=6'h3F → MCAPC=6'h00 (2nd parameter) B1h: Added. B3h: 5th parameter added. B4h: "SDOE=0" added.
		72	BFh: 8'hF5 → 8'h15 (3rd parameter) 8'h05 → 8'h26 (4th parameter) C0h: "GIP=0" added. (1st parameter) "NW=0" → 00h (4th parameter) C1h and C3h: "DIVx[1:0]=2'h0" → "DIVx[1:0]=2'h2" (2nd parameter)
		73	C1h and C3h: "RTNx[5:0]=6'h19" → "RTNx[5:0]=6'h28" (3rd parameter) C4h: 5th parameter added.
		74	C8h Gamma Set A → C8h~CAh Gamma Set A ~ C D0h: "BT[2:0]=3'h3" → "BT[2:0]=3'h6" (1st parameter)

Rev.	Date	Page No	Contents of Modification
			2nd, 5th, and 6th parameters added. "VC2[2:0]=3'h7" → "VC2[2:0]=3'h2" (3rd parameter) "8'h3F (VRH[5:0]=6'h3F)" → "VRH[5:0]=6'h3F" (4th parameter) D1h: 3rd parameter added.
		77	DB7 of 2nd parameter: 1 → LCDV[7] Relationship between 04h and A1h commands added. Flow chart corrected.
		84	DSPINVON → 0 DSPINVON deleted from "Command list symbol" and description of D5 changed.
		87	Description of D7 added.
		90	Description of power supply on sequencer and wait time of host processor changed.
		99, 101, 117, 119	Restriction in wait time added.
		128	WRCABC (Write Content Adaptive Brightness Control) → RCABC (Read Content Adaptive Brightness Control). 5Eh and 5Fh commands deleted.
		129	Description of functions changed.
		130	DB7 of 3rd parameter: 1 → LCDV[7] Description changed as a whole.
		132	Name of DB5-DB0 of 1st and 2nd parameters and description changed.
		133	B1h command added.
		134	5th parameter added.
		143-144	Restriction in CGAPW[4:0] and PITCHW[3:0] added.
		151	Table of GIP changed.
		153	Comment of BLV and PTV added and description of PTV changed.
		155	"-" → "0." (PTDC)
		158	"625kHz" → "Setting inhibited" (DIVn[1:0]=2'h3)
		160	Setting and restriction in FPn[7:0] and BPn[7:0] changed..
		162	5th parameter added.
		163	Note 2 added to table of VEQW[3:0].
		164	Table of SPCW[3:0] corrected. (4'h2-4'h7)
		165	"C8h-CBh" → "C8h-CAh" (error correction)
		167	Note 2 added to table of BT[2:0].
		169	Description and table of DCT[2:0] added.
		170	3rd parameter added.
		176	Description and table of DC10[2:0], DC12[2:0], DC00[2:0], and DC02[2:0] changed.
		179	Description of WCDDB changed.
		180	Commands used to data load from NVM changed. (LD[0], LD[4], and LD[5])
		185	Deep standby mode added and sleep mode sequence time changed.
		186	CBh command deleted.

Rev.	Date	Page No	Contents of Modification
			Wait time: 120ms → 5ms and 7 frames 120ms → 7 frames
		187	Wait time: 120ms → 5ms and 7 frames 120ms → 7 frames
		188	Default register values defined.
		189	MCAP setting changed.
		190	Transition sequence of deep standby mode added.
		191	C21P/C21M: VCI/GND → GND/GND C22P/C22M: VCI/GND → GND/GND
		199	BLCON = 1 → BL = 1
		202-203	Restriction in CGAPW[4:0] and PITCHW[3:0] added.
		212-213	Figure corrected.
		224	Note added.
		230	Command stored in NVM and commands used to load data from NVM changed.
		231	Register settings changed. (See "NVM Write Data Set (Initial Setting)" and "DDB data set")
		232	"DDVDH-VCL" deleted power supply voltage No. and note No. changed.
		233	Spec for IM pin input/output leakage current added and BLCON changed to BL.
		234	BLCON changed to BL.
		236	DDVDH: 4.5V → 5.0V (Min.), 6.0V → 5.8V (Max.)
		237	Specs for RDX changed. (Min.)
		238	Length of arrow (tast) changed.
		239	Specs for WRX/SCL (Read) changed. (Min.)
		240	Length of arrow (tas) changed.
		241	Table of DPI timing characteristics defined.
1.00	2010/07/08	9	Power Supply Specifications; Input voltage; IOVCC1; RESX → RESETX LCD voltages; VGL; -4.5V～-13.0V → -7.1V～-14.9V
		15	ENABLE and VSYNC; "Leave open when DPI Is not selected." → "Connect to IOVCC1 or GND when DPI is not selected."
		16	HSYNC and DOTCLK; "Leave open when DPI Is not selected." → "Connect to IOVCC1 or GND when DPI is not selected."
		18	VMONI; "Leave open." → "Leave open or connect to GND." Unused pin; "OPEN" → "OPEN or GND"
		55	16-Bit DPI; Example (Figure); DB[17:15] → DB[17:16]
		56	Notes to Usage of DPI; Note "f" added.
		58	User Command; 26h deleted.
		74	E0h; NVM Access Control; 4th deleted.
		95	2Ah; Restriction revised.
		97	2Ah; Restriction revised.
		110	Bit B4; Description added.
		129	68h; 2nd parameter; DB7; D7 → FUNCL, DB6; D6 → FUNCD

Rev.	Date	Page No	Contents of Modification
		131	A1h; Flow Chart revised.
		134	B3h; 5th parameter; Hex XXh → 00h
		150	C0h; 1st parameter; DB5; GIP → 1, 4th parameter; Hex; XXh → 10h, 6th parameter; DB2; PTS[2] → PTS, DB1; PTS[1] → 0, DB0; PTS[0] → 0
		151	Description; GIP deleted.
		155	PTS[2:0], PTDC → PTS, PTDC Table revised.
		162	C4h; 5th parameter; Hex; XXh → 00h
		167	D0h; 2nd parameter; Hex; XXh → 53h, 6th parameter; Hex; XXh → 00h
		171	Description; VCM[6:0]; 7'h00-7'h1A; VREG x*** → Setting Inhibited
		173	Description; VDV[6:0]; 7'h00-7'h24; VREG x*** → Setting Inhibited
		175	D2h; 1st parameter; DB1; 1 → 0, Hex; XXh → 01h D4h; 1st parameter; DB1; 1 → 0, Hex; XXh → 01h
		177	E0h; 3rd parameter; DB1; TEM[1] → 0
		178	TEM[1:0] → TEM
		198	Self-Diagnostic Function; Note in Figure revised. Functionality Detection; Description revised.
		215	Figure; TBD deleted.
		222-223	Table Reference level selection register and selection level revised.
		227	Figure; VREG; "See note" → "(11)" Note deleted.
		228	"(See note)" and Note deleted.
		232	NVM Write Sequence figure revised.
		234-235	Electrical Characteristics; [Target Spec] deleted. TBD deleted, conditions, values and Deep Sleep mode added.
		236	Step-up Circuit Characteristics; TBD deleted, IOVCC → IOVCC1, conditions and values added.
		237	AC Characteristics; "Note 1" and "TBD" deleted. IOVCC → IOVCC1
		238	DBI TypeB Timing Characteristics; [Target Spec] deleted. CSX; trcs & trcfm; Min.; 170 → 270, DB[17:0]; traccs & traccfm; Max.; 150 → 250
		240	DBI TypeC Timing Characteristics; [Target Spec] deleted. DOUT; Max; 110 → 150
		242	DPI Timing Characteristics; [Target Spec] deleted.
		244	LCD Output Characteristics; [Target Spec] and TBD deleted. Test condition, Typ., Max. revised.
		245	TBD deleted.
		288	Note 8 deleted.
1.00a	2010/07/16	168	VRH[5:0]; 5'h00-5'h1F (doubled) → 5'h20 – 5'h3F

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1.00b	2010/07/21	74	D2h, D4h; 1st para; 8'h3 →8'h1
1.10a	2010/08/19	7	Features; "Dynamic backlight control function" deleted.
		10	Block Diagram revised. "Backlight control circuit" deleted.
		13	"11. Backlight control circuit" deleted.
		14	External power supply; IOVCC2; description revised.
		15	Signal DB[17:0]; Description of unsed pins added.
		16	Table "LED Driver Control Pin (Amplitude: IOVCC2-GND)" deleted.
		18	LEDPWM pin's description added to Table "Other Pins"
		46	(2-2) Read Operation by Read Mode In Command; B8h, B9h deleted.
		61	User Command; B8h, B9h deleted.
		64	User Command; 51h-68h; Command Accessibility → "No"
		65	Manufacturer Command; B8h, B9h deleted.
		69	User Command; 51h/52h; Parameters; "DBV[7:0] deleted. 51h-68h; Default Modes and Values → 00h
		70-71	Manufacturer Command; B8h, B9h deleted.
		121	51h; Changed so as to be "Setting inhibited".
		122	52h; Changed so as to be "Setting inhibited".
		123	53h; Changed so as to be "Setting inhibited".
		124	54h; Changed so as to be "Setting inhibited".
		125	55h; Changed so as to be "Setting inhibited".
		126	56h; Changed so as to be "Setting inhibited".
		127	68h; Changed so as to be "Setting inhibited".
		137-146	Manufacturer Command; B8h, B9h deleted.
		168	E2h; LD[2]; Manufacturer Command; B8-B9h → None.
		169	F0h; Operational Code; B8h, B9h deleted.
		174	Power and Display On/Off Sequences Without NVM; Figure revised.
		176	Default Register Values; B8h, B9h deleted.
		186-194	Section "Dynamic Backlight Control Function" deleted.
		211	List of Command stored in NVM; B8h, B9h deleted. LD[2]; Manufacturer Command; B8-B9h → None.
		212	NVM Write Sequence figure revised. B8h, B9h deleted.
		214-215	Electrical Characteristics; I_{OP3} deleted. "BL=0" deleted from I_{OP1}, I_{OP2}, I_{ci1}, I_{ci2}

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