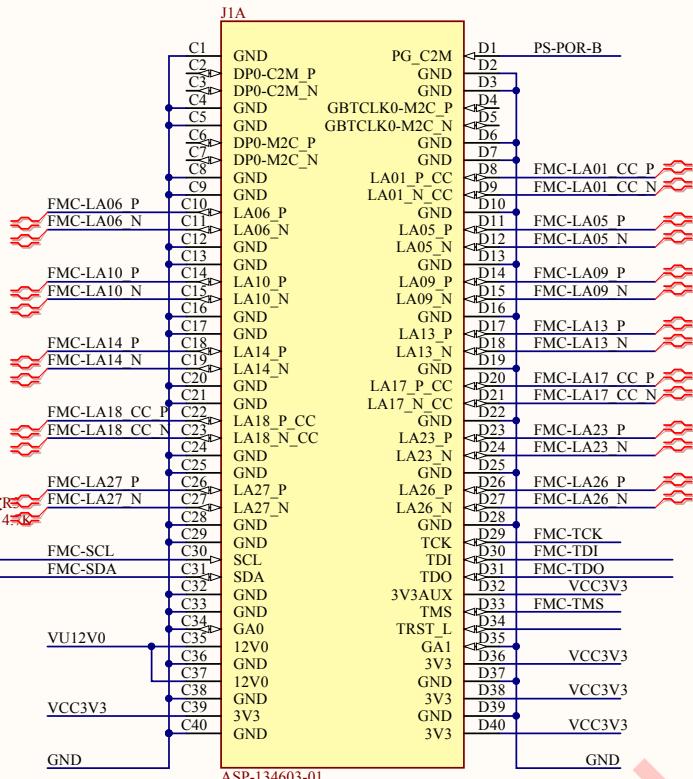
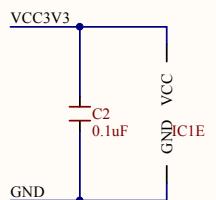
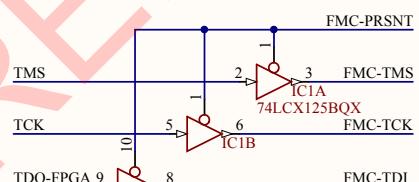
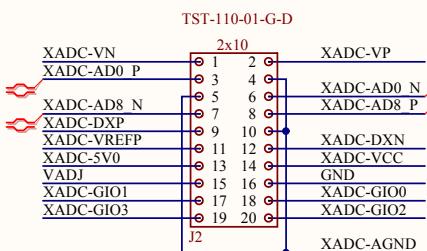
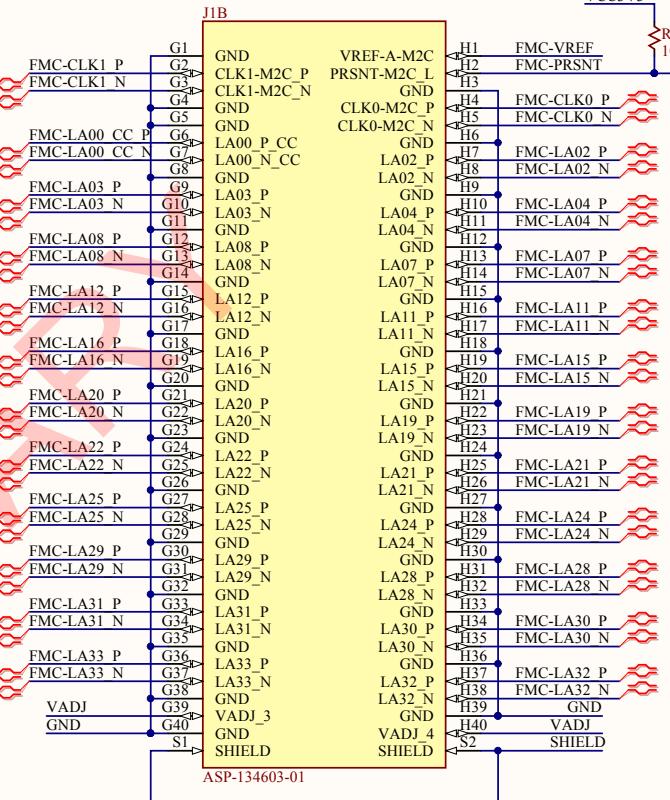


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DIGILENT
BEYOND THEORY

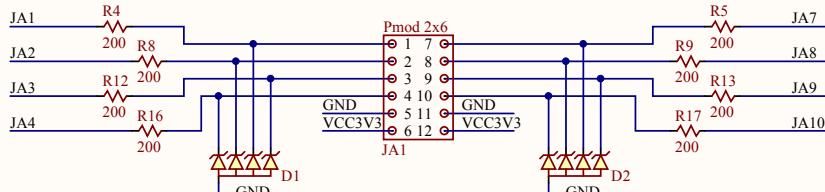
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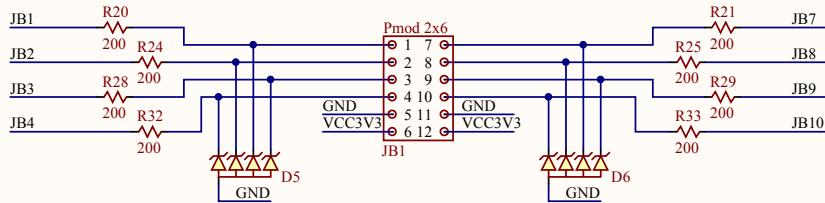
3

4

A



B

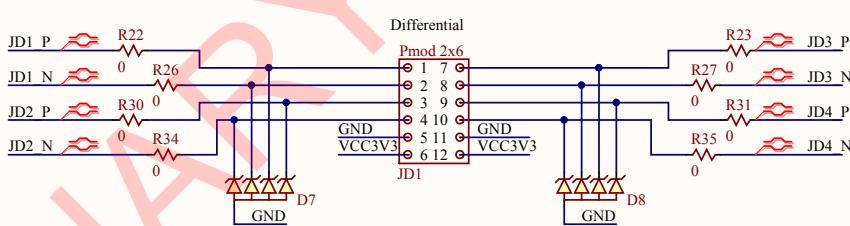
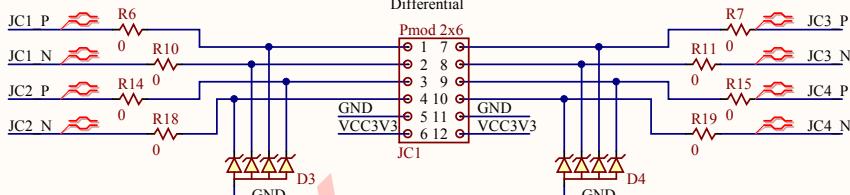
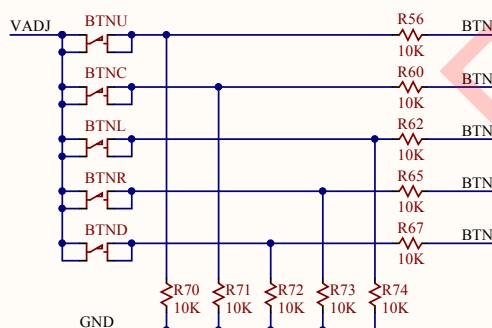


MIO PMOD

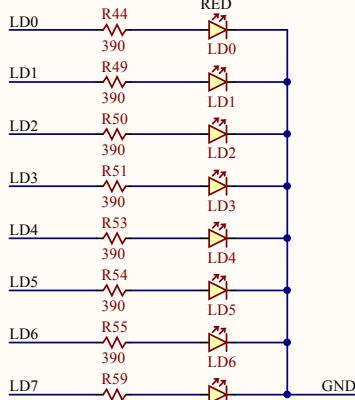
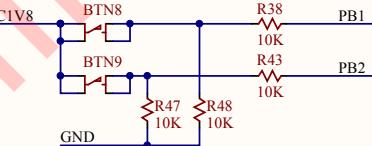
MIO LED



D



MIO BUTTON



Title
ZED

Circuit

PMODs and General I/O

Doc# 500-248

Engineer EG

Author GMA

Date 6/20/2012

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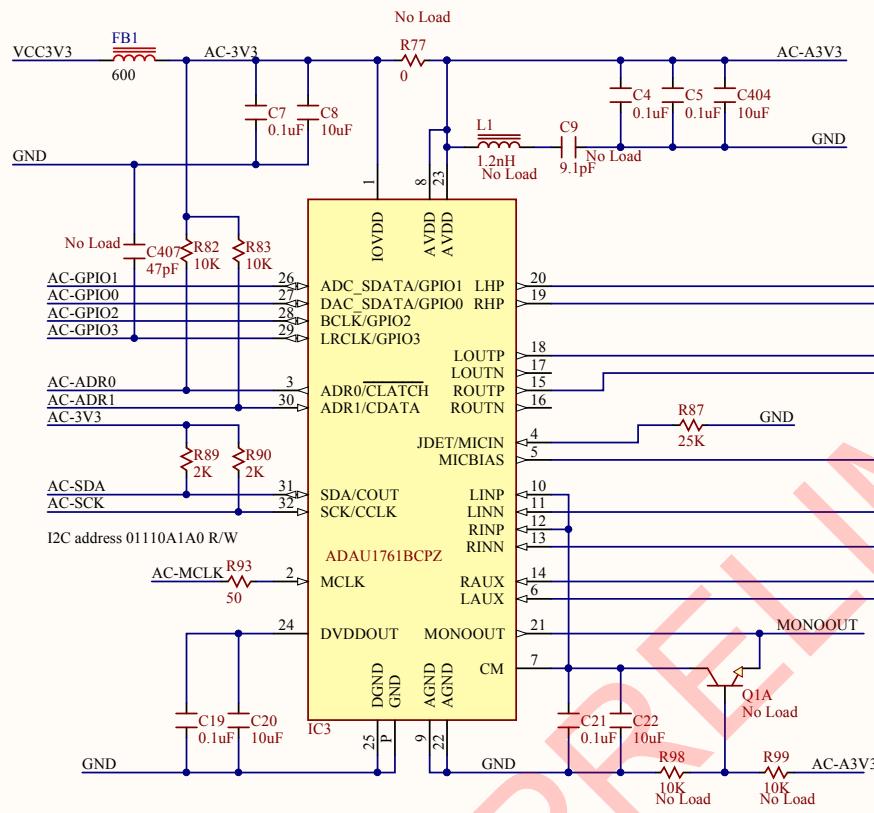
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A



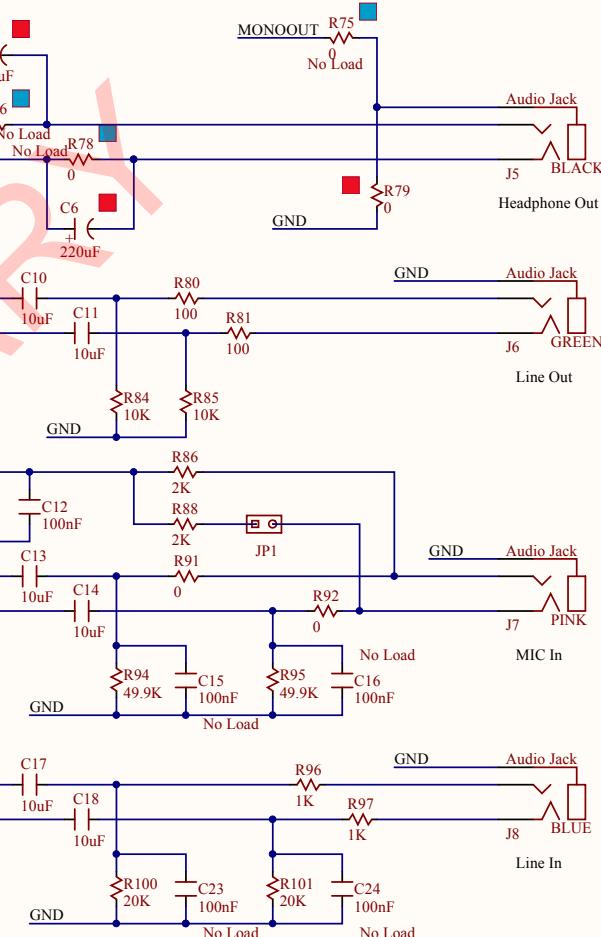
NOTE: AGND and GND pins must connect at single point under ADP150

B

C

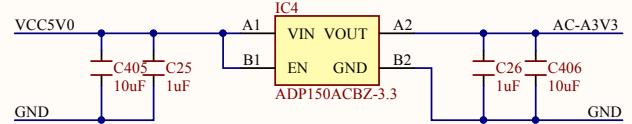
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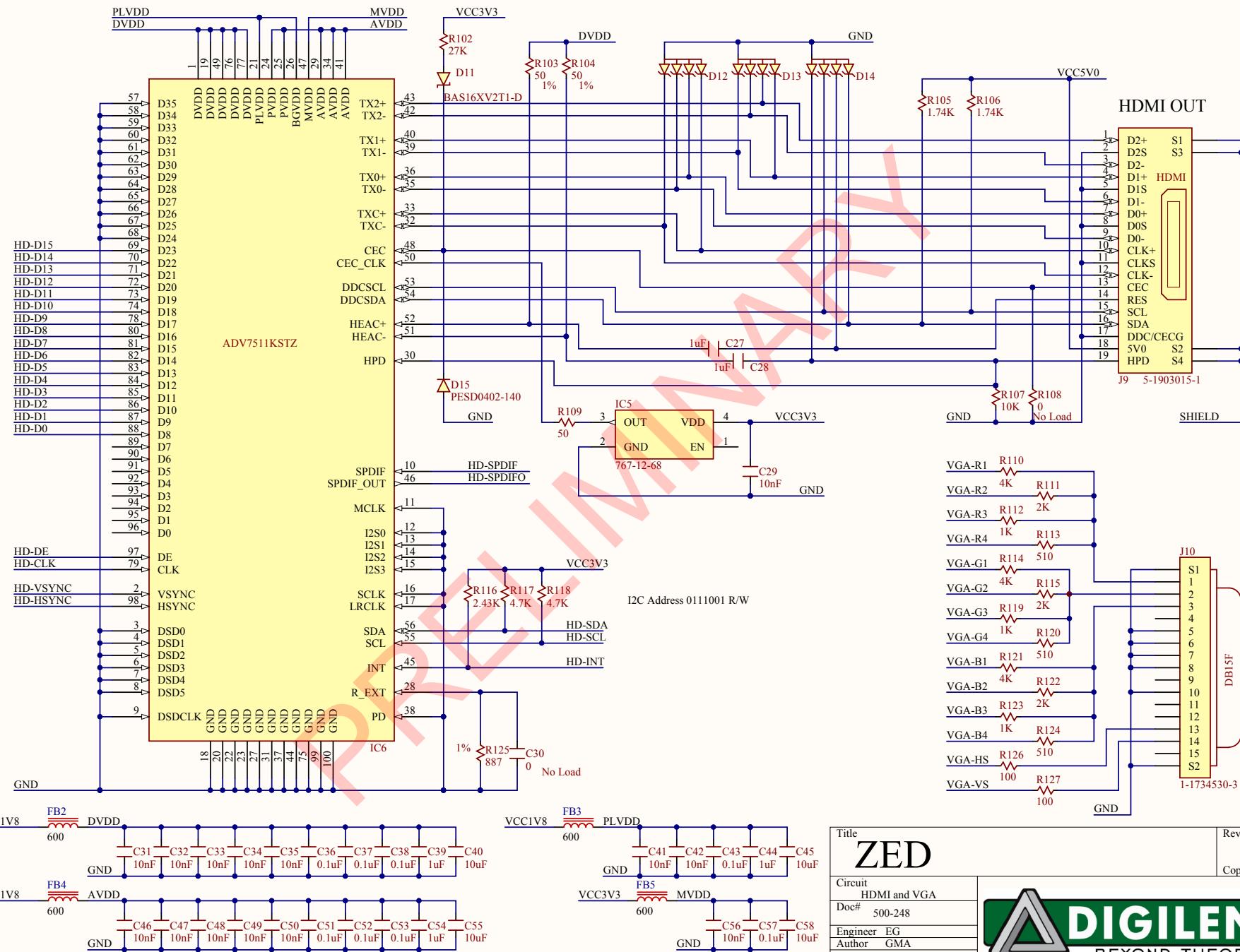
NOTE:
Capless Headphone Load
AC-Coupled Headphone No Load



Title
ZED

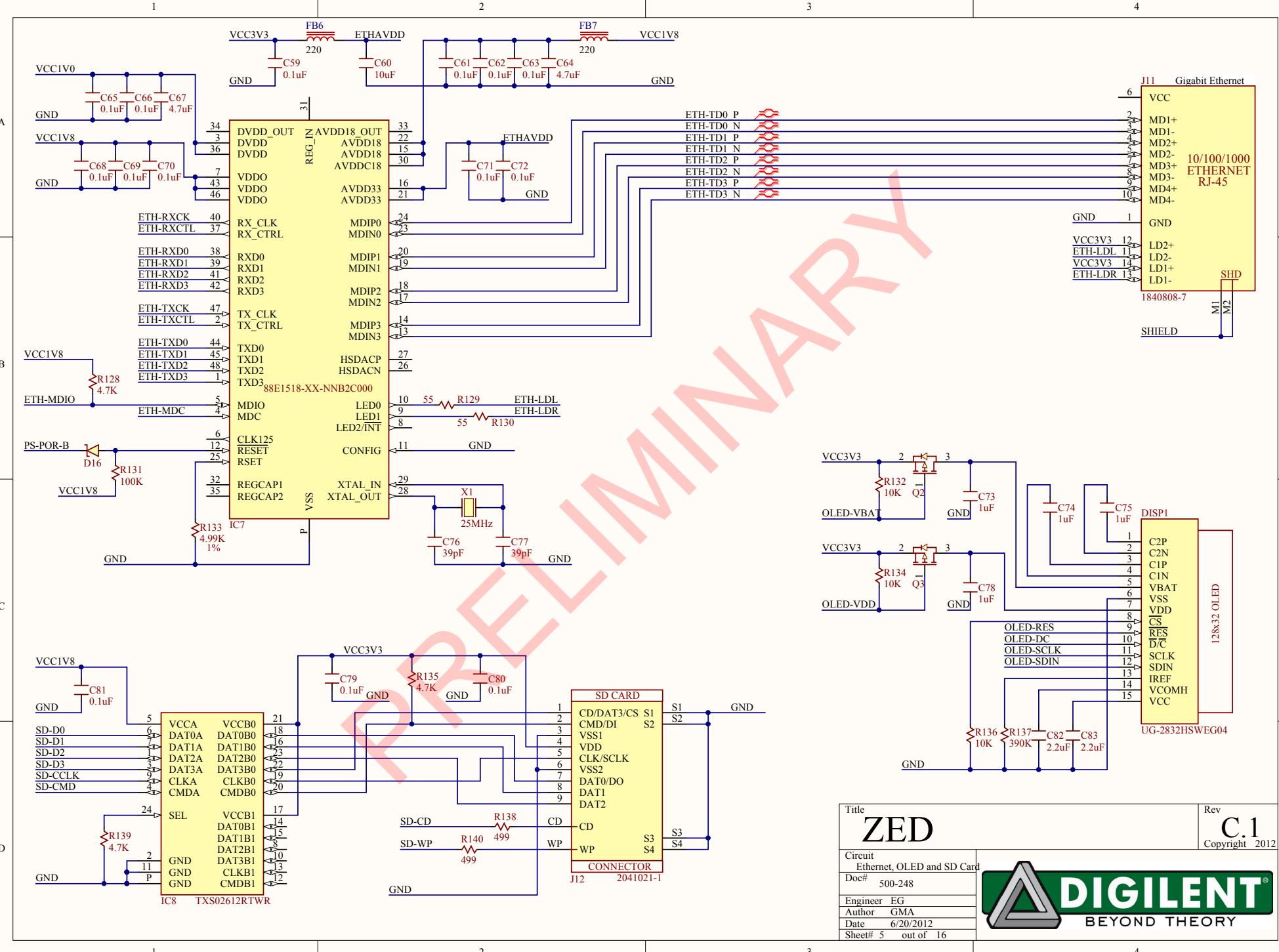
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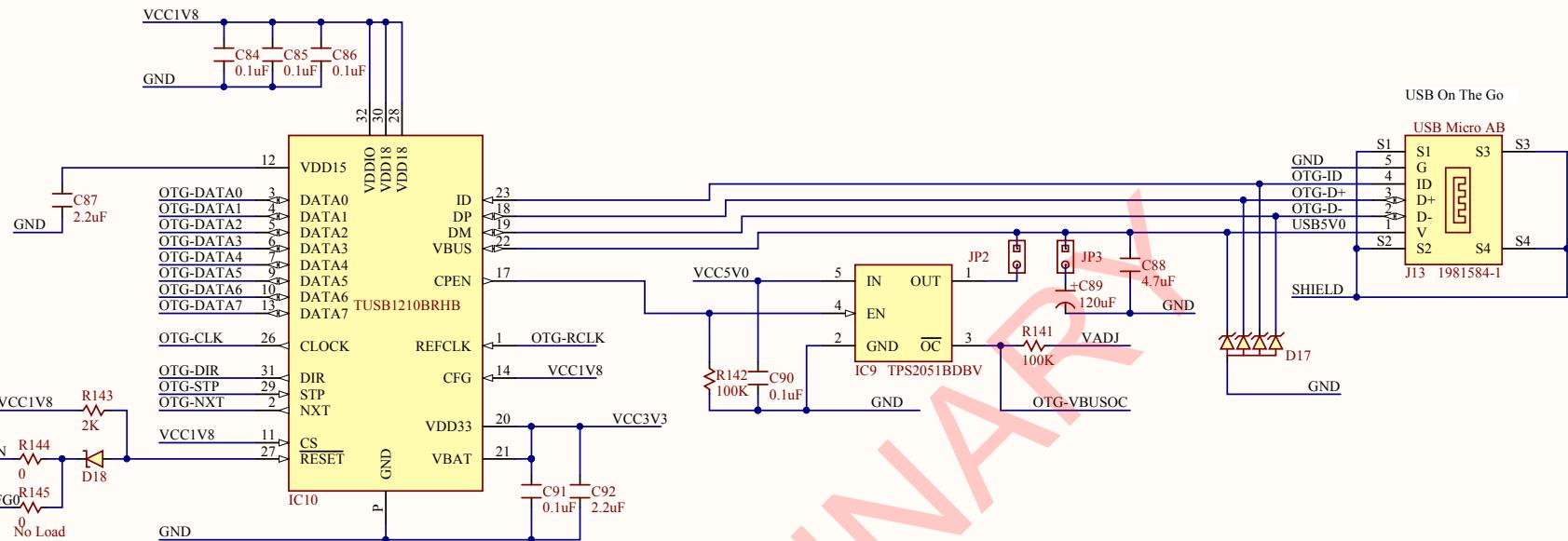




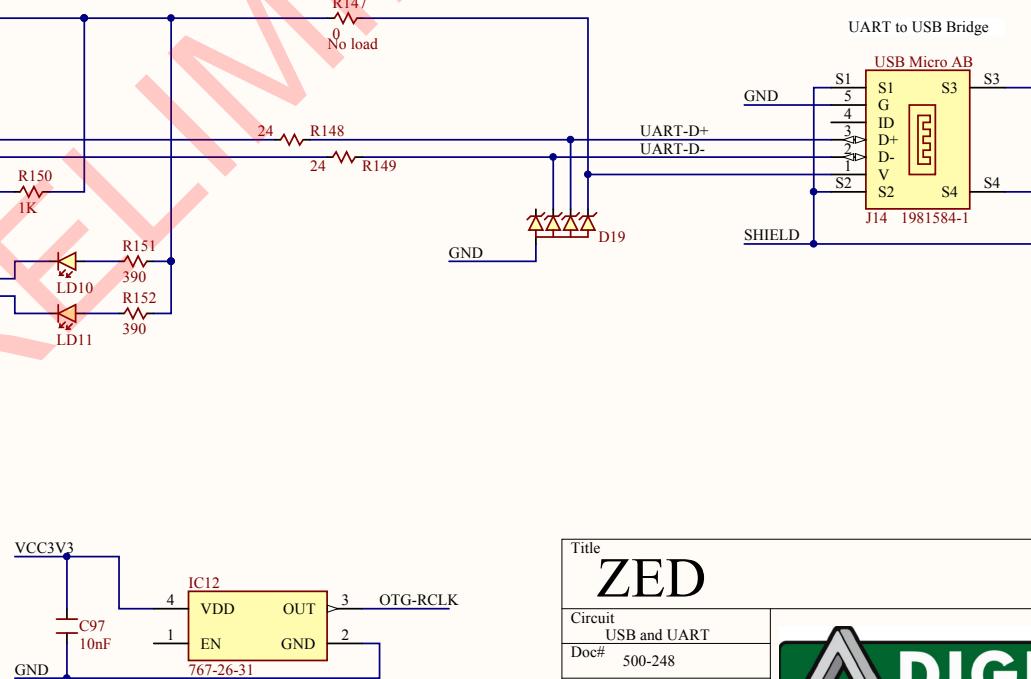
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Circuit HDMI and VGA		Copyright 2012
Doc#	500-248	
Engineer	EG	
Author	GMA	
Date	6/20/2012	
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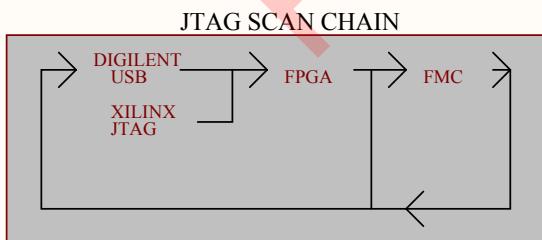
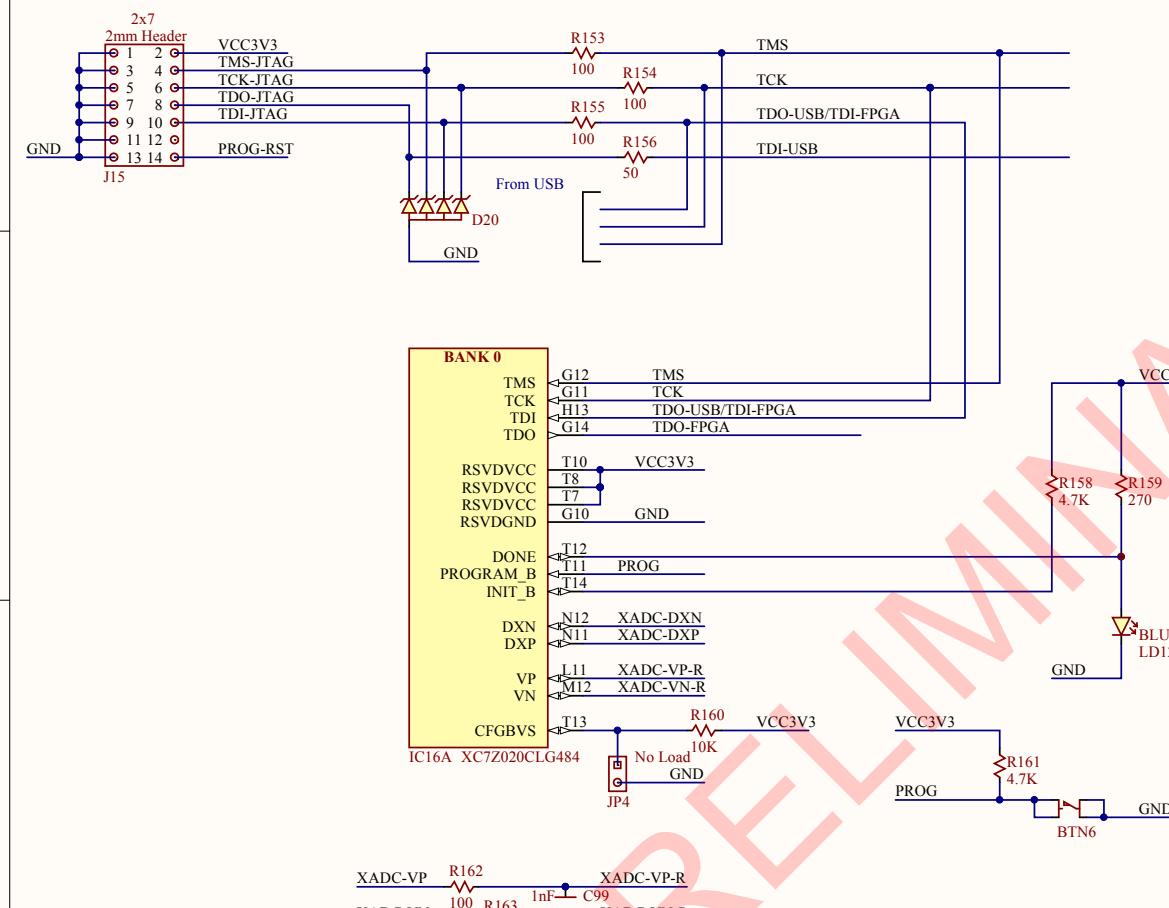
PREVIEW



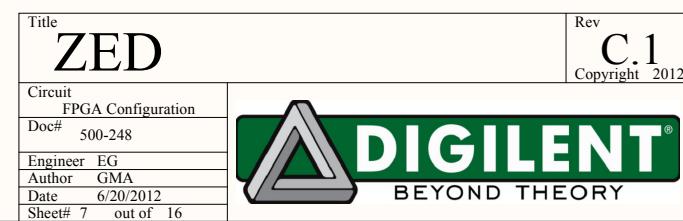
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Circuit		USB and UART	C.1
Doc#	500-248	Date	Copyright 2012
Engineer	EG	Author	GMA
Author	GMA	Date	6/20/2012
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Xilinx JTAG Header



JTAG SCAN CHAIN



title

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VCC3V3

BANK 13	
IO_0	R7 FMC-SCL
IO_25	U7 FMC-SDA
IO_LIN_T0	V9 JB9
IO_LIP_T0	Y10 JB3
IO_L2N_T0	W8 JB4
IO_L2P_T0	V8 JB10
IO_L3N_T0_DQS	W10 JB8
IO_L3P_T0_DQS	W11 JB2
IO_L4N_T0	W12 JB1
IO_L4P_T0	V12 JB7
IO_L5N_T0	T11 OLED-VBAT
IO_L5P_T0	T12 OLED-VDD
IO_L5P_T0	T19 OLED-RES
IO_L6N_T0_VREF	U10 OLED-DC
IO_L6P_T0	AB12 OLED-SCLK
IO_L7N_T1	AA12 OLED-SDIN
IO_L7P_T1	AB11 JA7
IO_L8N_T1	AA11 JA2
IO_L8P_T1	AB9 JA9
IO_L9N_T1_DQS	AB10 JA8
IO_L9P_T1_DQS	AB10 JA3
IO_L10N_T1	AA11 JA1
IO_L10P_T1	AA8 JA10
IO_L11N_T1_SRCC	AA9 JA4
IO_L11P_T1_SRCC	AB8 AC-GPIO0
IO_L12N_T1_MRCC	Y9 GCLK
IO_L12P_T1_MRCC	Y5 AC-ADR1
IO_L13N_T2_MRCC	Y6 AC-GPIO3
IO_L13P_T2_MRCC	AA6 AC-GPIO2
IO_L14N_T2_SRCC	AA7 AC-GPIO1
IO_L14P_T2_SRCC	AB1 AC-ADR0
IO_L15N_T2_DQS	AB2 AC-MCLK
IO_L15P_T2_DQS	AB4 AC-SCK
IO_L16N_T2	AB5 AC-SDA
IO_L16P_T2	AB6 JC1 N
IO_L17N_T2	AB7 JC1 P
IO_L17P_T2	AB8 JC2 N
IO_L18N_T2	AA4 JC2 P
IO_L18P_T2	AB4 JC3 N
IO_L19N_T3_VREF	AB6 JC3 P
IO_L19P_T3	AB4 JC4 N
IO_L20N_T3	AB4 JC4 P
IO_L20P_T3	V4 JD2 N
IO_L21N_T3_DQS	V5 JD2 P
IO_L21P_T3_DQS	V5 JD4 N
IO_L22N_T3	W6 JD4 P
IO_L22P_T3	W7 JD1 N
IO_L23N_T3	V7 JD1 P
IO_L23P_T3	W8 JD3 N
IO_L24N_T3	W5 JD3 N
IO_L24P_T3	W6 JD3 P

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VCC3V3

BANK 33	
IO_0	U19 LD6
IO_25	U14 LD7
IO_LIN_T0	J21 LD3
IO_LIP_T0	J21 LD1
IO_L2N_T0	J22 LD2
IO_L2P_T0	J22 LD0
IO_L3N_T0_DQS	J22 LD5
IO_L3P_T0_DQS	V22 LD4
IO_L4N_T0	W21
IO_L4P_T0	W20
IO_L5N_T0	V20 VGA-R1
IO_L5P_T0	W20 VGA-R2
IO_L6N_T0_VREF	V19 VGA-R3
IO_L6P_T0	V18 VGA-R4
IO_L7N_T1	AB22 VGA-G1
IO_L7P_T1	AA22 VGA-G2
IO_L8N_T1	AB21 VGA-G3
IO_L8P_T1	AA21 VGA-G4
IO_L9N_T1_DQS	V21 VGA-B1
IO_L9P_T1_DQS	Y20 VGA-B2
IO_L10N_T1	AB20 VGA-B3
IO_L10P_T1	AB19 VGA-B4
IO_L11N_T1_SRCC	AA19 VGA-HS
IO_L11P_T1_SRCC	V19 VGA-VS
IO_L12N_T1_MRCC	AA18 HD-SCL
IO_L12P_T1_MRCC	Y18 HD-SPDIFO
IO_L13N_T2_MRCC	W18 HD-CLK
IO_L13P_T2_MRCC	W17 HD-VSYNC
IO_L14N_T2_SRCC	Y16 HD-SDA
IO_L14P_T2_SRCC	W16 HD-INT
IO_L15N_T2_DQS	W16 HD-DE
IO_L15P_T2_DQS	U15 HD-SPDIF
IO_L16N_T2	V17 HD-HSYNC
IO_L16P_T2	U17 HD-D13
IO_L17N_T2	AB17 HD-D7
IO_L17P_T2	AA17 HD-D8
IO_L18N_T2	AB16 HD-D5
IO_L18P_T2	AA16 HD-D6
IO_L19N_T3_VREF	V15 HD-D12
IO_L19P_T3	V14 HD-D14
IO_L20N_T3	W13 HD-D10
IO_L20P_T3	W13 HD-D15
IO_L21N_T3_DQS	Y15 HD-D9
IO_L21P_T3_DQS	W15 HD-D11
IO_L22N_T3	AA14 HD-D2
IO_L22P_T3	Y14 HD-D3
IO_L23N_T3	AA13 HD-D1
IO_L23P_T3	Y13 HD-D0
IO_L24N_T3	AB15 HD-D4
IO_L24P_T3	AB14 FMC-PRSN

IC16C XC7Z020CLG484

VADJ

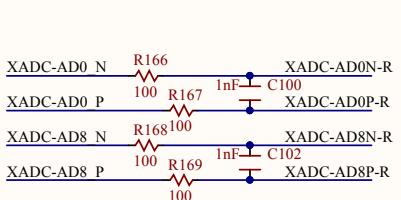
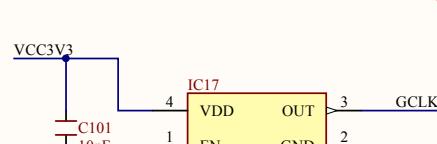
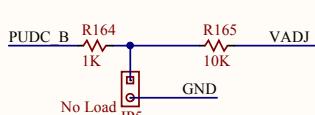
BANK 34	
IO_0	H15 XADC-GIO0
IO_25	U15 XADC-GIO1
IO_LIN_T0	K15 XADC-GIO2
IO_LIP_T0	J15 XADC-GIO3
IO_L2N_T0	H17 FMC-LA15_N
IO_L2P_T0	I16 FMC-LA15_P
IO_L3N_T0_DQS	I16 OTG-VBUSOC
IO_L3P_T0_DQS	K16 PUDC_B
IO_L4N_T0	M17 FMC-LA13_N
IO_L4P_T0	L17 FMC-LA13_P
IO_L5N_T0	N18 FMC-LA11_N
IO_L5P_T0	N17 FMC-LA11_P
IO_L6N_T0_VREF	M16 FMC-VREF
IO_L6P_T0	M15 SW7
IO_L7N_T1	K18 FMC-LA05_N
IO_L7P_T1	I18 FMC-LA05_P
IO_L8N_T1	J22 FMC-LA08_N
IO_L8P_T1	J21 FMC-LA08_P
IO_L9N_T1_DQS	K21 FMC-LA16_N
IO_L9P_T1_DQS	J20 FMC-LA16_P
IO_L10N_T1	J22 FMC-LA06_N
IO_L10P_T1	I19 FMC-LA06_P
IO_L11N_T1_SRCC	K20 FMC-LA14_N
IO_L11P_T1_SRCC	K19 FMC-LA14_P
IO_L12N_T1_MRCC	I19 FMC-CLK0_N
IO_L12P_T1_MRCC	J18 FMC-CLK0_P
IO_L13N_T2_MRCC	M20 FMC-LA00_CC_N
IO_L13P_T2_MRCC	M19 FMC-LA00_CC_P
IO_L14N_T2_SRCC	N20 FMC-LA01_CC_N
IO_L14P_T2_SRCC	N19 FMC-LA01_CC_P
IO_L15N_T2_DQS	M22 FMC-LA04_N
IO_L15P_T2_DQS	M21 FMC-LA04_P
IO_L16N_T2	P22 FMC-LA03_N
IO_L16P_T2	N22 FMC-LA03_P
IO_L17N_T2	I21 FMC-LA09_N
IO_L17P_T2	I20 FMC-LA09_P
IO_L18N_T2	I21 FMC-LA12_N
IO_L18P_T2	P20 FMC-LA12_P
IO_L19N_T3_VREF	P15 FMC-VREF
IO_L19P_T3	N15 BTNL
IO_L20N_T3	P18 FMC-LA02_N
IO_L20P_T3	P17 FMC-LA02_P
IO_L21N_T3_DQS	T17 FMC-LA07_N
IO_L21P_T3_DQS	T16 FMC-LA07_P
IO_L22N_T3	I19 FMC-LA10_N
IO_L22P_T3	R19 FMC-LA10_P
IO_L23N_T3	T18 BTNU
IO_L23P_T3	R18 BTNR
IO_L24N_T3	R16 BTND
IO_L24P_T3	P16 BTNC

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VADJ

BANK 35	
IO_0	H17 SW6
IO_25	H18 SW5
IO_LIN_T0_AD0N	F16 XADC-AD0N-R
IO_LIP_T0_AD0P	F16 XADC-AD0P-R
IO_L2N_T0_AD8N	D17 XADC-AD8N-R
IO_L2P_T0_AD8P	D16 XADC-AD8P-R
IO_L3N_T0_DQS_AD1N	D15 FMC-LA23_N
IO_L3P_T0_DQS_AD3P	E15 FMC-LA23_P
IO_L4N_T0_AD9N	G16 FMC-LA19_N
IO_L5P_T0_AD9P	G15 FMC-LA19_P
IO_L6N_T0_VREF	F18 FMC-LA26_N
IO_L6P_T0	F17 FMC-VREF
IO_L7N_T1_AD2N	G17 OTG-RESETN
IO_L7P_T1_AD2P	B15 FMC-LA30_N
IO_L8N_T1_AD10N	C15 FMC-LA30_P
IO_L8P_T1_AD10P	B17 FMC-LA31_N
IO_L9N_T1_DQS_AD3N	B16 FMC-LA31_P
IO_L9P_T1_DQS_AD3P	A17 FMC-LA28_N
IO_L10N_T1_AD11N	A16 FMC-LA28_P
IO_L10P_T1_AD11P	A19 FMC-LA24_N
IO_L11N_T1_SRCC	A18 FMC-LA24_P
IO_L11P_T1_SRCC	C18 FMC-LA29_N
IO_L12N_T1_MRCC	C17 FMC-LA29_P
IO_L12P_T1_MRCC	C19 FMC-CLK1_N
IO_L13N_T2_MRCC	D18 FMC-CLK1_P
IO_L13P_T2_MRCC	B20 FMC-LA17_CC_N
IO_L14N_T2_SRCC	B19 FMC-LA17_CC_P
IO_L14P_T2_AD4N_SRCC	C20 FMC-LA18_CC_N
IO_L15P_T2_DQDZ_AD12N	D20 FMC-LA18_CC_P
IO_L15P_T2_DQDZ_AD12P	A22 FMC-LA32_N
IO_L16N_T2	A21 FMC-LA32_P
IO_L16P_T2	C22 FMC-LA25_N
IO_L17N_T2_AD5N	D21 FMC-LA27_N
IO_L17P_T2_AD5P	E21 FMC-LA27_P
IO_L18N_T2_AD13N	C22 FMC-LA33_N
IO_L18P_T2_AD13P	B21 FMC-LA33_P
IO_L19N_T3_VREF	H20 FMC-VREF
IO_L19P_T3	H19 SW4
IO_L20N_T3_AD6N	F19 FMC-LA22_N
IO_L20P_T3_AD6P	G19 FMC-LA22_P
IO_L21N_T3_DQS_AD14N	E20 FMC-LA21_N
IO_L21P_T3_DQS_AD14P	F19 FMC-LA21_P
IO_L22N_T3_AD7N	G21 FMC-LA20_N
IO_L22P_T3_AD7P	F20 FMC-LA20_P
IO_L23N_T3	F21 SW0
IO_L23P_T3	F21 SW3
IO_L24N_T3_AD15N	G22 SW1
IO_L24P_T3_AD15P	H22 SW2

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Title **ZED**Rev **C.1**
Copyright 2012Circuit **FPGA Banks**Doc# **500-248**Engineer **EG**Author **GMA**Date **6/20/2012**Sheet# **8**out of **16**

DDR1V5

VCC3V3

VCC1V8

A

B

C

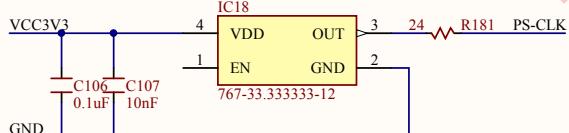
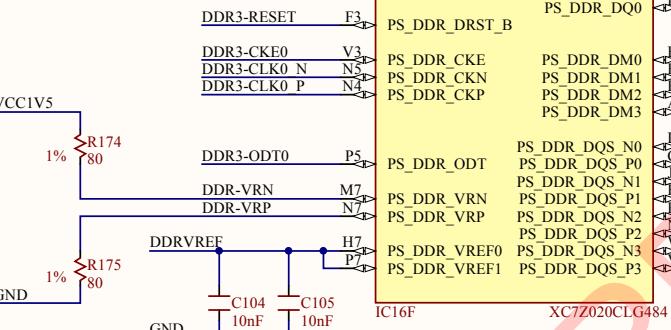
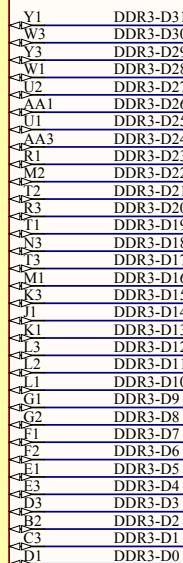
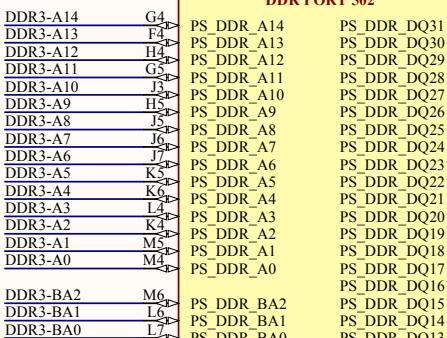
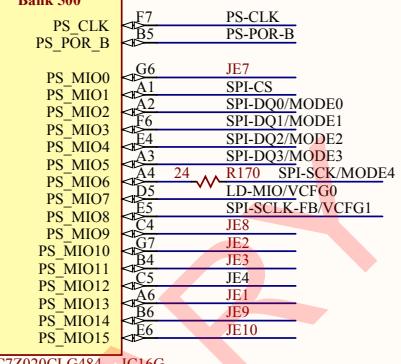
D

A

B

C

D

DDR PORT 502**Bank 500**

XC7Z020CLG484

IC16G

VCC1V8

R171 10K 1%

C103 10nF

R172 10K 1%

GND

VREF0V9

R173 499

JP6

GND

JE7

R174 10K

JP6

GND

R175 499

JP6

GND

R176 10K

JP6

GND

R177 20K

JP7

GND

R178 20K

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Bank 501

PS_MIO_VREF PS_SRST_B

D6 ETH-TXCK

E9 ETH-TXDO

A7 ETH-TXD1

E10 ETH-TXD2

PS_MIO19 A8 ETH-TXCK3

PS_MIO20 F11 ETH-TXCTL

PS_MIO21 A14 ETH-RXCK

PS_MIO22 E11 ETH-RXD0

PS_MIO23 B7 ETH-RXD1

PS_MIO24 F12 ETH-RXD2

PS_MIO25 A13 ETH-RXD3

PS_MIO26 D7 ETH-RXCTL

PS_MIO27 A12 OTG-DATA4

PS_MIO28 E8 OTG-DIR

PS_MIO29 A11 OTG-STP

PS_MIO30 F9 OTG-NXT

PS_MIO31 C7 OTG-DATA0

PS_MIO32 G13 OTG-DATA1

PS_MIO33 B12 OTG-DATA2

PS_MIO34 F14 OTG-DATA3

PS_MIO35 A9 OTG-CLK

PS_MIO36 B14 OTG-DATA5

PS_MIO37 F13 OTG-DATA6

PS_MIO38 C13 OTG-DATA7

PS_MIO39 E14 SD-CCLK

PS_MIO40 D8 SD-CMD

PS_MIO41 B10 SD-CD

PS_MIO42 D11 UART-RXD

PS_MIO43 C14 UART-TXD

PS_MIO44 D13 PB1

PS_MIO45 D12 PB2

PS_MIO46 D10 ETH-MDC

PS_MIO47 D11 ETH-MDO

PS_MIO48 C12 ETH-MDIO

PS_MIO49 D13 PBI

PS_MIO50 C10 PB2

PS_MIO51 D10 ETH-MDC

PS_MIO52 C12 ETH-MDIO

PS_MIO53 C11 PBI

IC16H XC7Z020CLG484

ZED

Rev

C.1
Copyright 2012

Title

Circuit

DDR and MIO Banks

Doc# 500-248

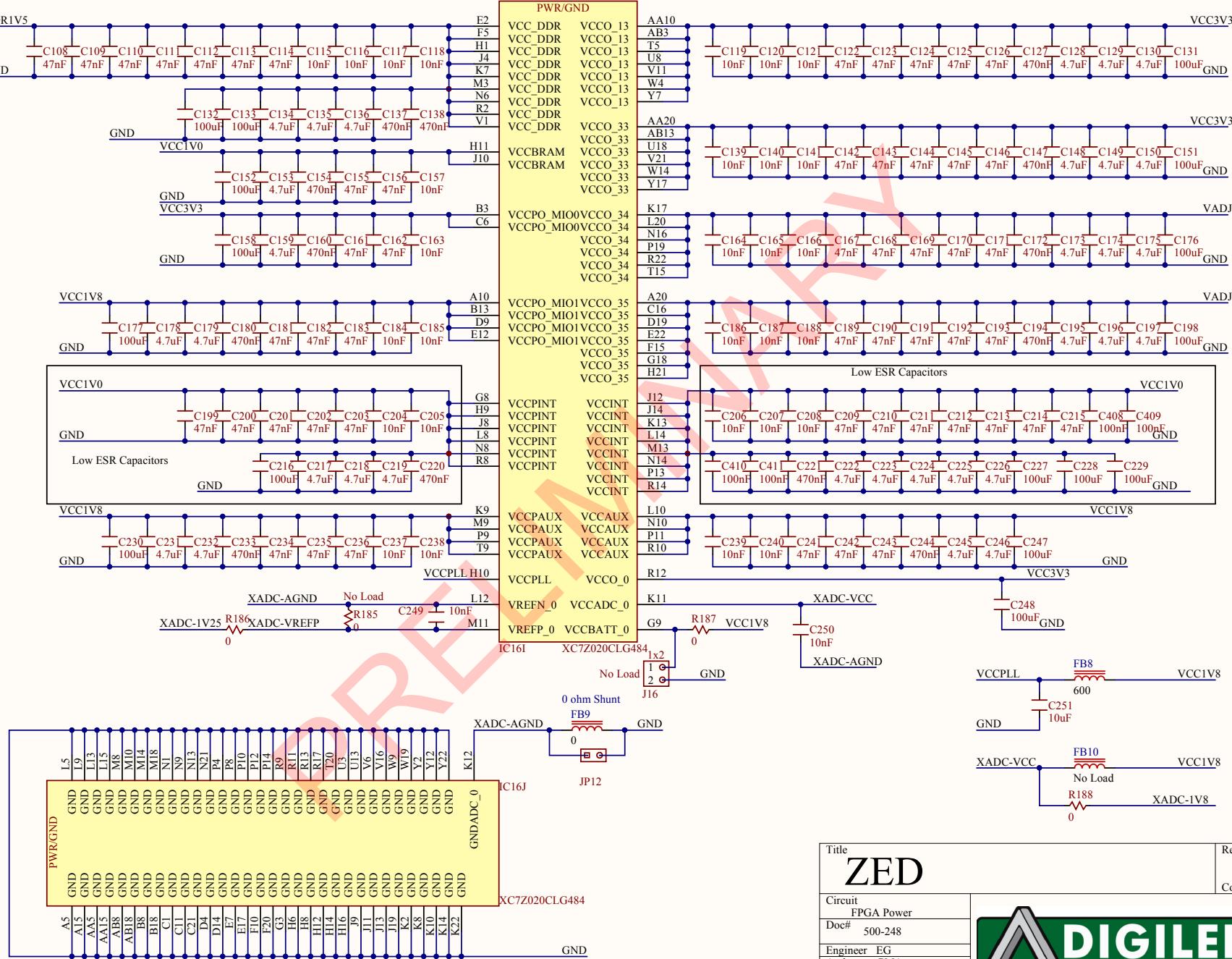
Engineer EG

Author GMA

Date 6/20/2012

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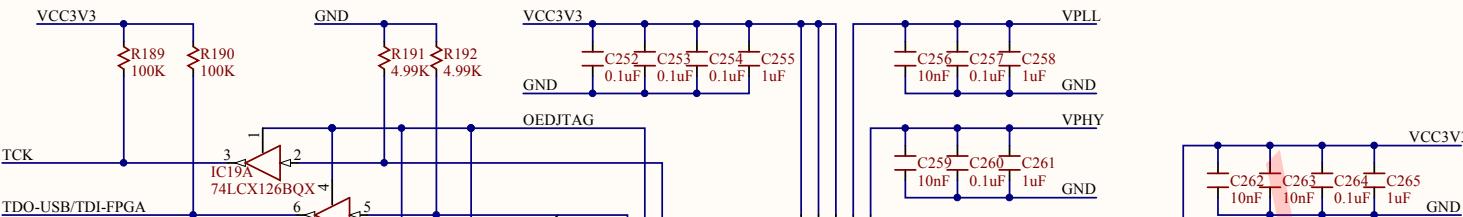
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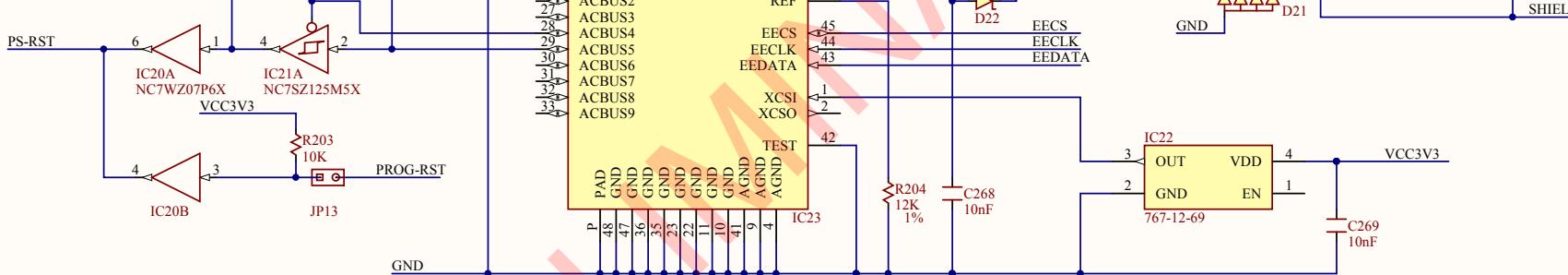
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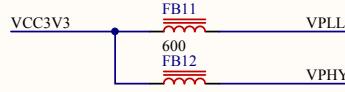
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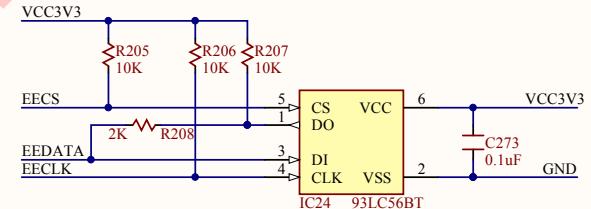
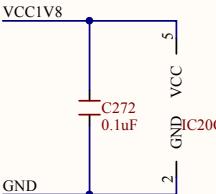
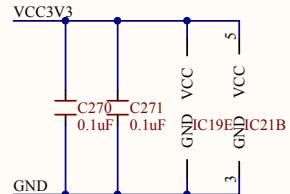
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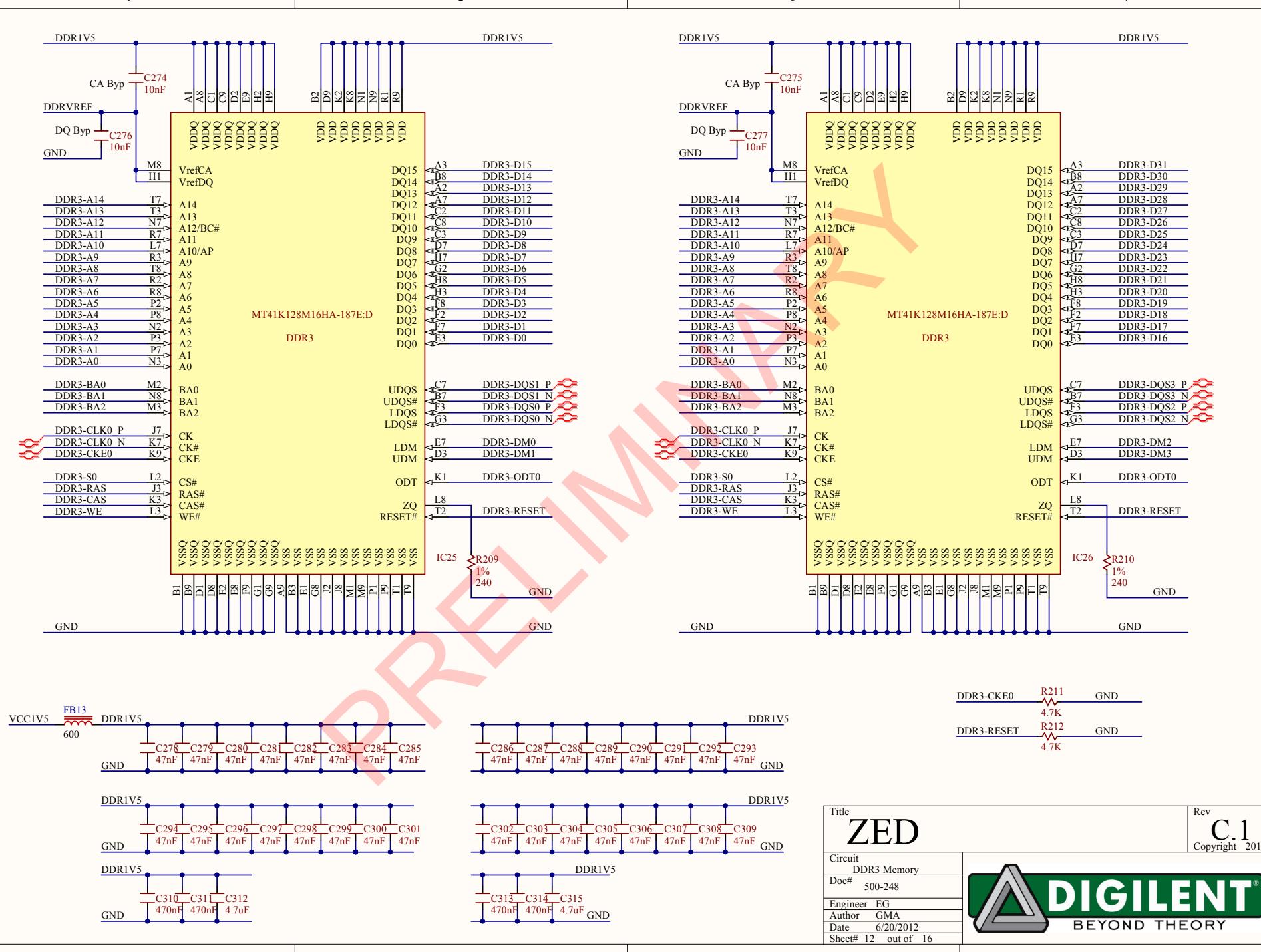
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Author	GMA		
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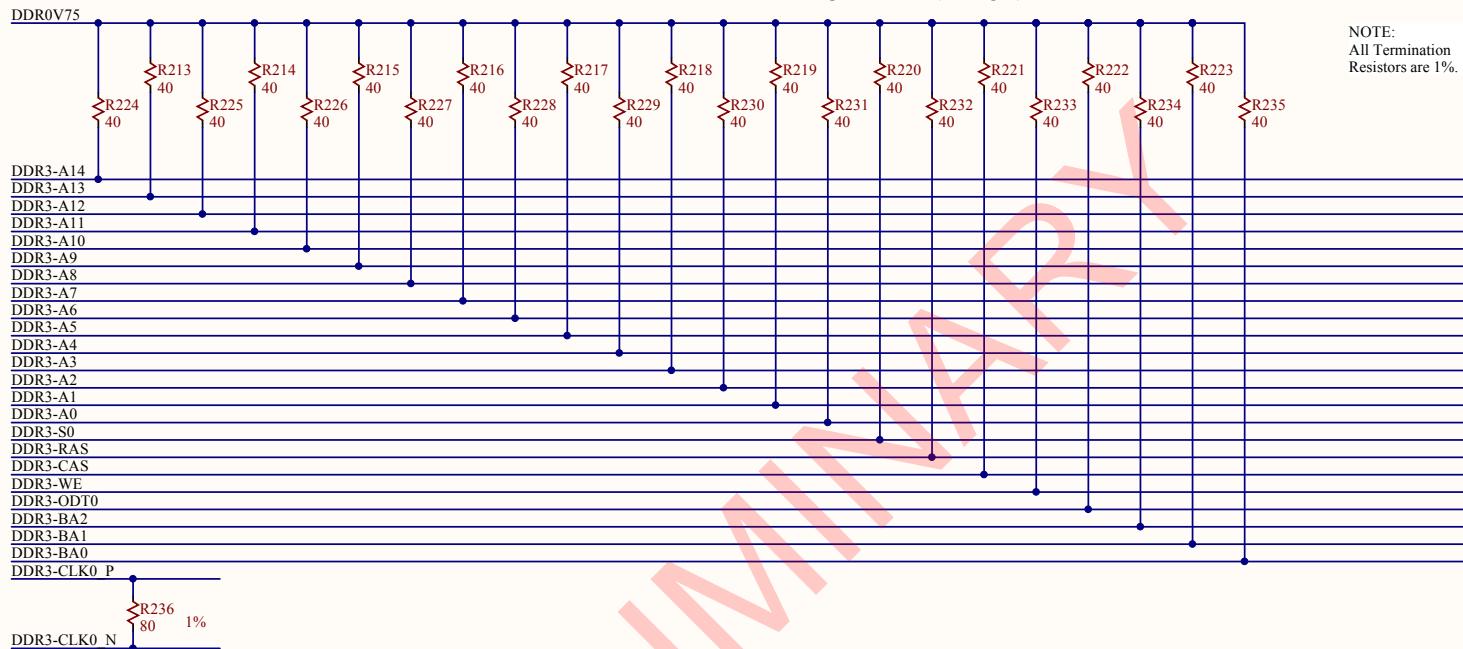




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DDR3 TERMINATION



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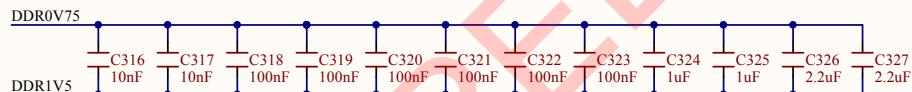
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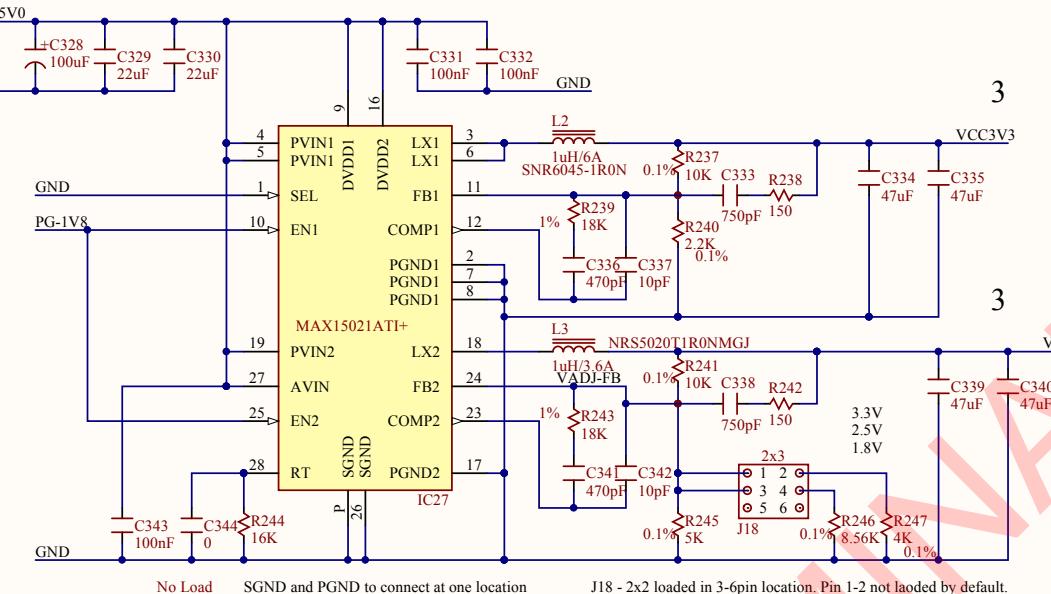
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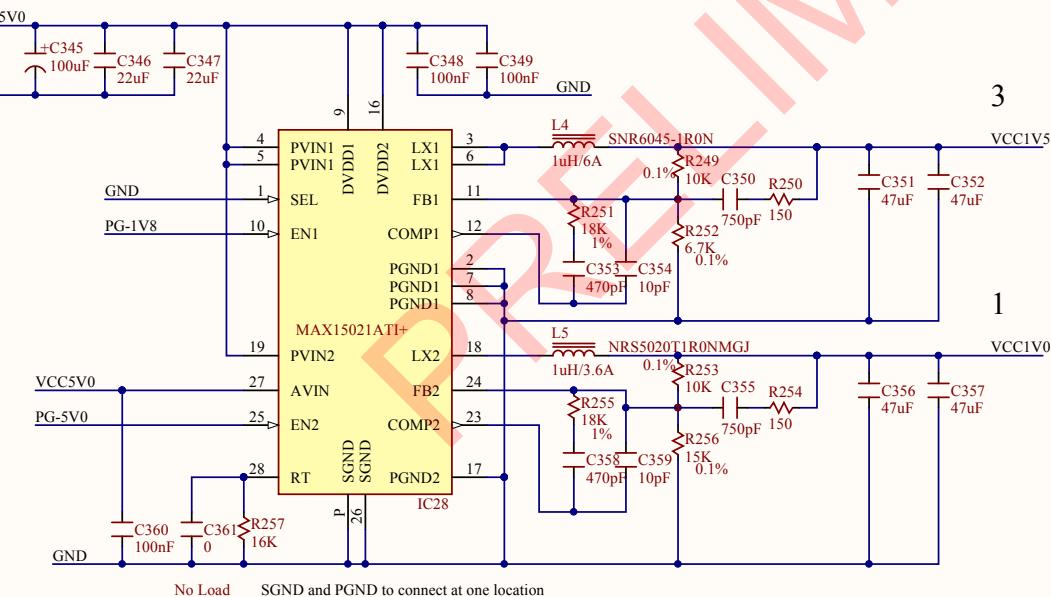


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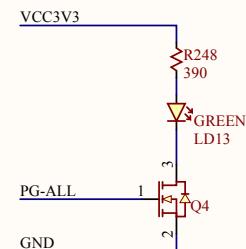


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Title
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Engineer EG

Author GMA

Date 6/20/2012

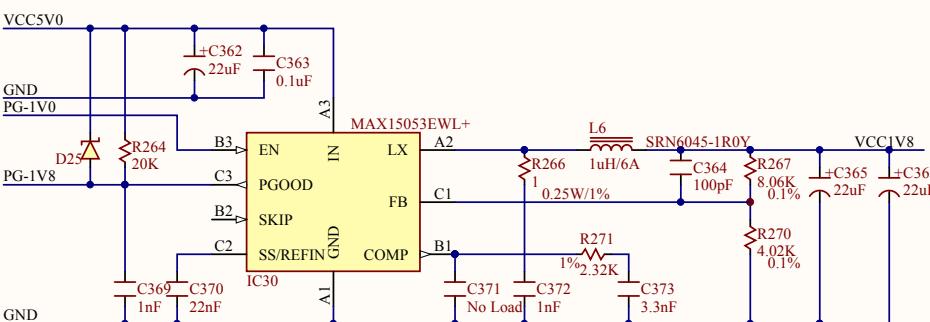
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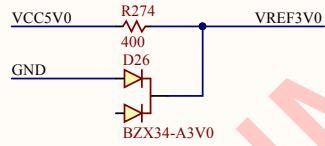


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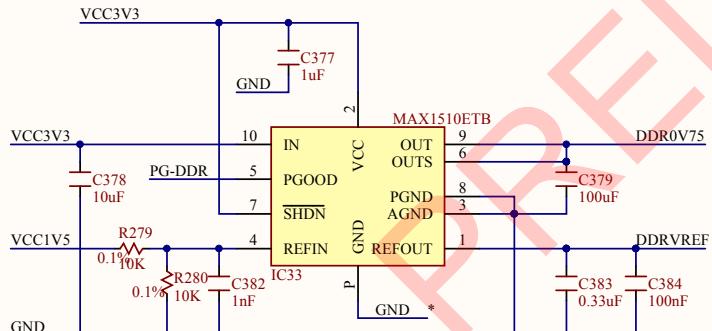
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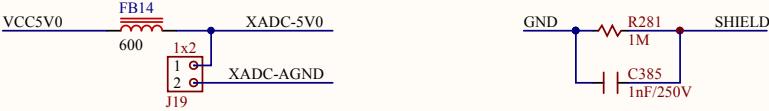
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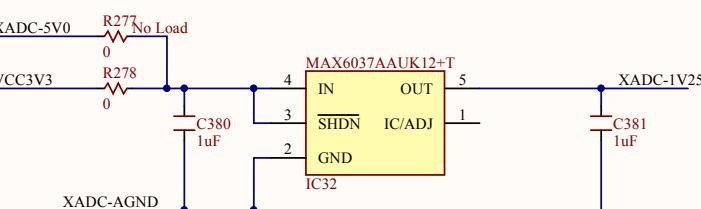
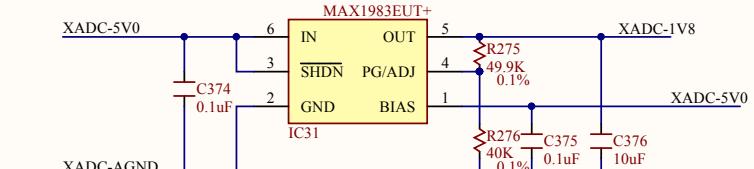
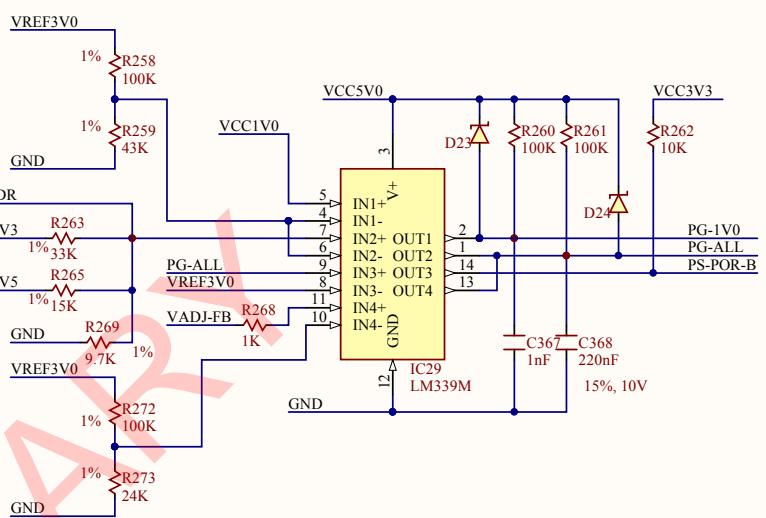
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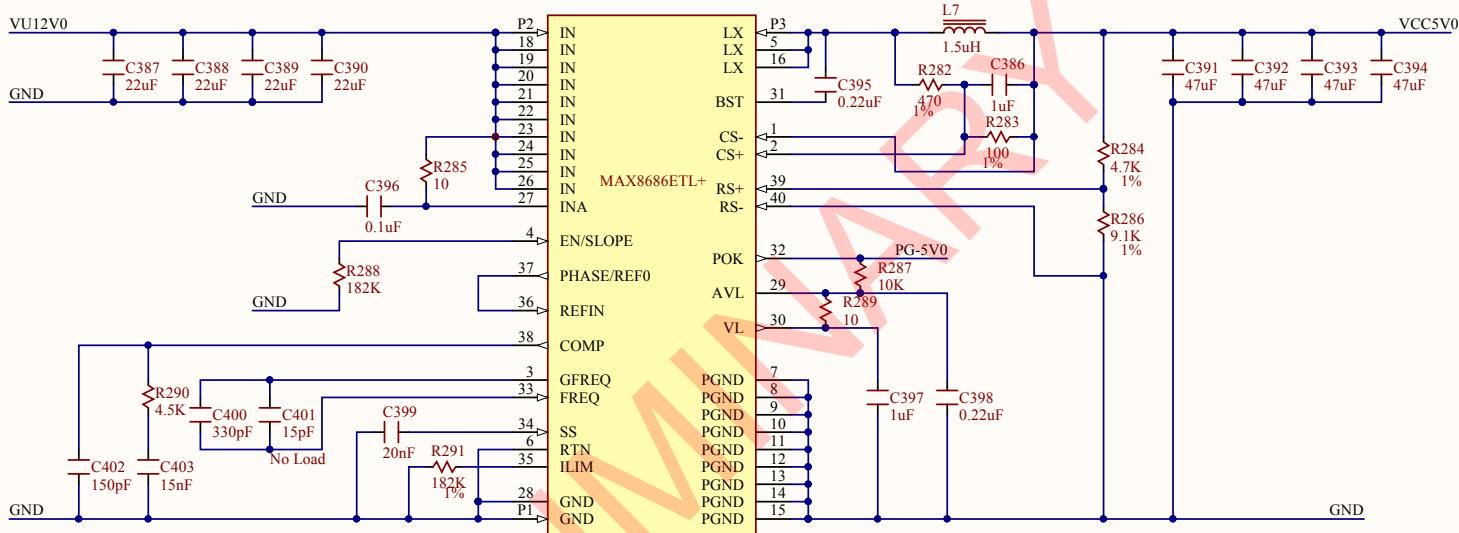
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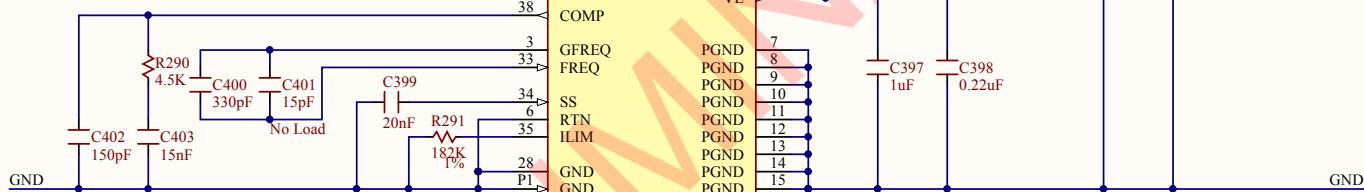
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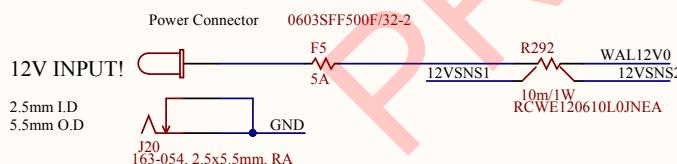
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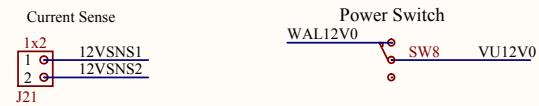
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