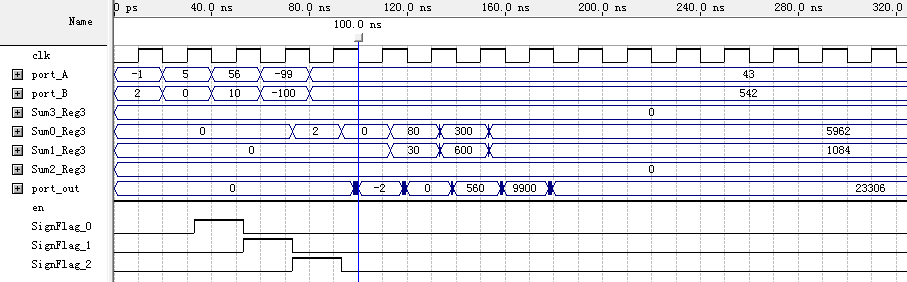
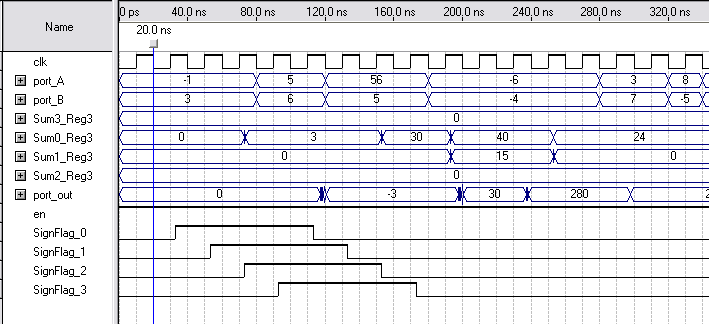
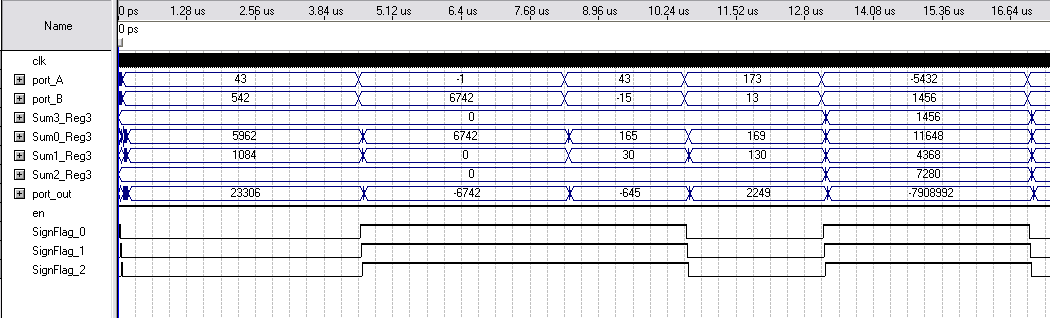
1. Simulation waveform for 4 stage multiplier design



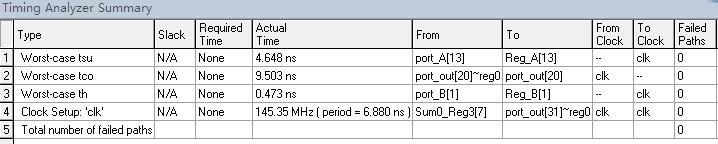
Simulation waveform for 5-stage multiplier design



Simulation waveform for 4-stage multiplier design for larger numbers:

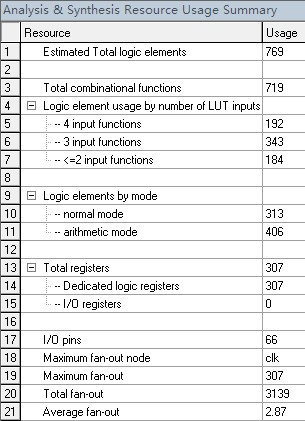


B) The max operating frequency of this design is 145.35 MHz for the 4-stage multiplier and 170.77Mhz for 5-stage multiplier.



1. Total number of LUT, logic elements, registers, I/O pins is summarized in the table below:

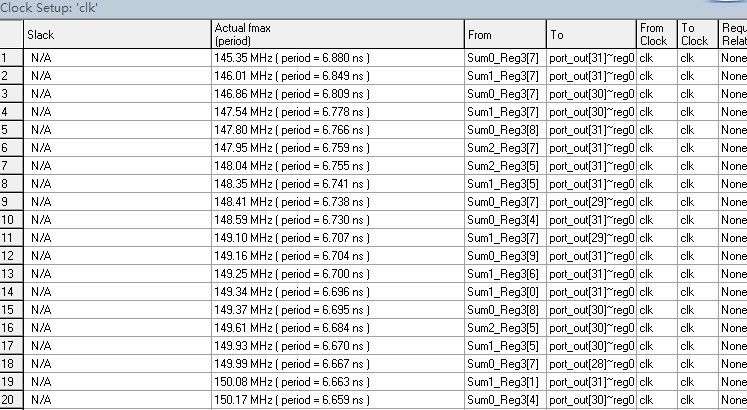
# Number of embedded multipliers is : 0



D) The bottleneck of our design

The list below shows operation from the slowest to the fastest. The bottleneck is the first row of the list.

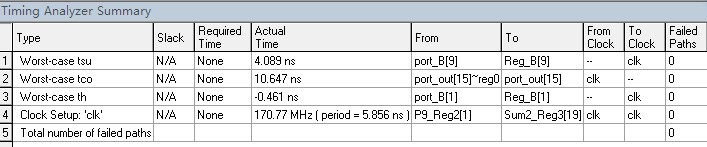
**Throughput** = # of bits/minimum clock period = 32 bits / 6.879 ns = 4.65 Gbits/s



E) The bottleneck is at the last stage where the 2nd sets of partial sum are added, and from which we obtained the output. In this stage, we add the four 20 bits sums together in order to get the final values for our output. This approach resulted in having the last stage to be the slowest.

To increase the processing time, we created an extra stage, divided the last stage into 2 stages. In one stage the added the four 20 bits sums and in the next stage we loaded to the results to the output resister. As a result, the max frequency increased. And the maximum frequency of operation becomes 170.77MHz,an increase of 27.42MHz than the previous 4-stage implementation.

**Throughput** = # of bits/minimum clock period = 32 bits / 5.855 ns = 5.46 Gbits/s



F) Total number of LUT, logic elements, registers. The table below gives a summary of the number of logic elements and registers used in this design

# Number of embedded multipliers is : 0

