VeriBest Analog Model Library Reference Manual

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Analog Circuit Design Library

The Analog Circuit Design Library is a substantial collection of discrete components, and linear integrated circuits. This library is specifically designed for the engineer undertaking standard analog circuit design. It features amplifiers, BJTs, diodes, FETs, MOSFETs and power devices from numerous semiconductor companies from around the world. The following classes of components are contained in the Circuit Design Library:

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Chapter 2
VeriBest Analog Amplifier Model Library

The Amplifier Library consists mainly of operational amplifier macromodels. It also contains macromodels of some special integrated circuits such as precision instrumentation amplifiers, video amplifiers, sample and hold amplifiers, preamplifiers, voltage followers, sense amplifiers, etc. Usually, those parts were designed for very specific purposes, so they are not typical and their macromodels are unique.

The operational amplifier portion of this library is the only large group of similar macromodels and will be described below.

Operational Amplifiers

General Description

The Operational Amplifier macromodel is an improved version of the Boyle et al macromodel. Modeled are some additional features:

- proper common mode input voltage range
- floating output
- short circuit output currents
- temperature dependence of
  - input offset voltage
  - input offset current
  - slew rate
- frequency dependence of CMRR
- frequency dependence of PSRR both for negative and positive power supply independently
- proper supply rail currents
- possibility to use overshoot as a parameter
- input noise

The input stage was modified in order to achieve proper common mode input voltage range. Outside the range the input transistors are either cut off or saturated (BJTs) or work in the nonsaturation (triode) region (unipolar transistors), which dramatically affects the opamp features. The input voltage range depends, of course, on supply voltages, so that to extract the proper internal parameters one should specify the range limits and the supply voltages at which the measurement was performed. Obviously, during simulation, the voltage range depends dynamically on the supply voltages currently applied in the schematic.

The output stage was built in such a manner that when the input offset voltage is compensated then the output voltage is set in the middle between VCC and VEE. This means that the supply voltages may be chosen without any restriction. The output voltage range is also modeled. The limits should be specified together with the supply voltages at which the measurement was done. Usually those supply

voltages are specified in the databooks along with nominal temperature as the conditions of the electrical characteristics measurement. Of course, the output voltage range dynamically depends on the actual supply voltages. The output stage was also modified so that the output current is drawn dynamically from the appropriate supply rail. The sinking output current appears on negative voltage supply rail while the sourcing output current is drawn from positive supply rail. The output current is limited to the range between the sink and the source short-circuit output currents.

The input offset voltage temperature dependence is modeled using a second order polynomial approximation. The polynomial coefficients are extracted from the data for the offset voltages for normal, minimum and maximum temperatures.

There are two types of input bias/offset currents temperature dependence. For BJT input stage opamps the bias current is determined mainly by the hFE temperature dependence of the input transistors, so that only two points are needed to extract the parameters, bias currents for normal and minimum temperatures. The input offset current is calculated using a second order polynomial approximation, so that three points are needed to extract the coefficients.

For unipolar input stage opamps the bias current temperature dependence is exponential, so there are usually bias current values given for normal and maximum temperatures, since for lower than normal temperatures the bias current is negligible. Usually the offset current temperature dependence is similar to the bias current temperature dependence, so that only two measurement points are needed.

The slew rate temperature dependence is modeled using a second order polynomial approximation. Three values of slew rate are needed to extract the coefficients. The positive and negative going slew rates are assumed to vary identically. There are two possible cases:

- the first, when the positive going slew rate is bigger than the negative, as for npn input stage opamps;
- the second, when the positive going slew rate is smaller, as for pnp or unipolar input stage opamps.

In the first case the positive going slew rate should be specified for nominal, minimum and maximum temperatures (SRPN, SRPMIN and SRPMAX). It determines temperature dependence of both positive and negative going slew rates. The negative going slew rate SRNN for nominal temperature determines only the ratio between the negative going and positive going slew rates.

In the second case the situation is opposite, the negative going slew rate is specified for nominal, minimum and maximum temperatures (SRNN, SRNMIN and SRNMAX), and the positive going slew rate (SRPN) is given for nominal temperature only.

There are some modified templates for some specific opamps, where no data about slew rate temperature dependence was available and even the distinction between positive and negative going slew rate was not made, then the only slew rate parameter is SR.

The CMRR and PSRR are modeled using single pole frequency characteristic. In order to keep the macromodel simple the low frequency values of PSRR for positive supply rail (VCC) and for negative supply rail (VEE) are assumed to be the same.

The input noise is modeled using white noise. Low frequency 1/f type noise is not modeled.

Parameter Description

VNOISE is the input noise voltage spectral density in [nV/sqrt(Hz)].The noise model is simple with no frequency dependence, so noise density for medium frequency should be taken as VNOISE value. If no data is available, 20nV/sqrt(Hz) is a good guess for the default value.

GBW is the commonly used gain-bandwidth product

TN, **TMIN** and **TMAX** are respectively: nominal, minimum and maximum temperatures given in degrees Celsius. Usually TN is 25 C and it is the normal temperature for which the data are specified. TMIN and TMAX are needed to extract temperature dependence of any feature, so they should be specified according to available data. If there is no data available, TMIN and TMAX can be given arbitrarily, but they must not be equal to TN, or to each other.

SRPN, **SRPMIN**, **SRPMAX** and **SRN** is the slew rate parameter set for opamps with an npn input stage or other opamps where SRPN>SRN. SRPN, SRPMIN and SRPMAX are positive going slew rates specified respectively for nominal, minimum and maximum temperatures. When there is no data available, SRPMIN and SRPMAX may be equal to SRPN. SRN is the negative going slew rate for nominal temperature. All slew rates should be specified in [V/us]. SRPN must not be smaller than SRN.

SRP, **SRNN**, **SRNMIN** and **SRNMAX** is the slew rate parameter set for opamps with pnp, JFET or MOSFET input stage or other opamps where SRNN>SRP. SRNN, SRNMIN and SRNMAX are negative going slew rates specified respectively for nominal, minimum and maximum temperatures. When there is no data available, SRNMIN and SRNMAX may be equal to SRNN. SRP is the positive going slew rate for nominal temperature. All slew rates should be specified in [V/us]. SRNN must not be smaller than SRP.

VCC and **VEE** are nominal supply voltages which are given in the databook as the measurement conditions for which the data are specified. If the opamp is supplied from one voltage supply then VEE=0. VCC and VEE should be specified as the reference in the process of extracting the internal parameters which describe input and output voltage ranges and the power supply current. Obviously, the actual simulation supply voltages can be whatever the user want to, with no effect to the macromodel performance (the output stage is a floating one).

VIN_CM_MAX and **VIN_CM_MIN** are the limits of the input common mode voltage range for previously specified nominal supply voltages VCC and VEE. If no data is available, then typical input common mode voltage range for opamps with BJT input stage should be about 2V below VCC, and about 2V above VEE. For opamps with JFET or MOSFET input stage VIN_CM_MAX should be about 2V below VCC, and VIN_CM_MIN may be about 0.5V below VEE. Of course, the actual input common mode voltage range depends on the actual values of supply voltages during the simulation.

IBIAS_N and **IBIAS_MIN** are the input bias current specified for nominal and minimum temperatures. This set is used for the opamps with the BJT, either npn or pnp, input stage.

IBIAS_N and **IBIAS_MAX** are the input bias current specified for nominal and maximum temperatures. Usually IBIAS_MAX is bigger than IBIAS_N, especially for opamps with JFET or MOSFET input stage where IBIAS_MAX is 2-3 orders of magnitude larger than IBIAS_N.

ROUT and **ROAC** are the output resistances for DC and alternating current respectively. Usually ROAC is in the range from few to few hundred ohms, ROUT is 2 or more times bigger than ROAC. If no data is available, default values may be ROUT=100 and ROAC=50.

AVD is the commonly used open loop voltage gain given in [V/V]

IOSN and **IOSMAX** are the input offset currents specified for nominal and maximum temperatures respectively.

VOSN, **VOSMIN** and **VOSMAX** are the input offset voltages specified for nominal, minimum and maximum temperatures respectively. If no data is available, VOSMIN and VOSMAX could be equal to VOSN.

CMRR is the low frequency common mode rejection ratio given in [dB]

FCMRR is the 3dB frequency of the common mode rejection ratio. A one pole frequency characteristic is assumed. Usually FCMRR is in the range from few hundred to few thousand Hz. If no data is available, a good default value for FCMRR is 200.

PSRR is the average low frequency power supply rejection ratio in [dB]. Usually PSRR for positive and negative power supply rails are a little bit different, but in order to simplify the macromodel schematic, the average value is assumed. Typical PSRR value is 100dB.

FPSRRP and **FPSRRN** are the 3dB frequencies of respectively positive and negative power supply rejection ratios. Single pole frequency characteristics are assumed. Usually FPSRRP and FPSRRN are in the range from a few Hz to a few tens of thousand Hz and sometimes one of them may be even an order of magnitude different than the other.

ISUP and **ISUP0** are the parameters related to power consumption. Usually the supply current versus supply voltage characteristic is not linear, nevertheless it is close to a straight line for supply voltages greater than few Volts, and abruptly goes down when supply voltage is coming close to zero. Usually the part behavior for very low supply voltage is of no interest, so a linearized supply current versus supply voltage characteristic is assumed. One of the two points of the characteristic is defined by the supply current ISUP for the specified supply voltages VCC and VEE. The other point ISUP0 is determined by the linearized supply current characteristic intersection with the supply current axis. ISUP0 should be smaller than ISUP. If no specific data is available, ISUP0 may be either 0 or something less than ISUP.

OVERSHOOT, **PHIM** and **PHIM_OVRSHT** are the parameters which describe the phase margin phenomenon. Usually phase margin for 0dB frequency is given in databooks, but sometime the overshoot of small signal pulse response is specified. In order to allow the user to use either the phase margin (PHIM) or the overshoot (OVERSHOOT) the switch PHIM_OVRSHT was introduced. When PHIM_OVRSHT is 0, then PHIM is used in the internal calculations, in the other case (PHIM_OVRSHT=1) the OVERSHOOT parameter is used.

ISCP and **ISCN** are the output source (positive) and sink (negative) short-circuit currents. Usually they are in the range from 10 to 100mA.

VOUT_MIN and **VOUT_MAX** are the limits of the output voltage range for the previously specified VCC and VEE voltages. Usually VOUT_MAX is about 2V below VCC and VOUT_MAX is about 2V above VEE. Of course, the actual output voltage range depends on the actual values of the supply voltages during the simulation.

Examples

The following are examples of parsets for three basic templates:

- .PARSET LM307H _OPAMPNPN
  This is a parset for the _OPAMPNPN template for opamps with an npn transistor input stage.

Parameter	Value	Parameter Definition
VNOISE	= 17	# spectral noise density in [nV/sqrt(Hz)]
GBW	= 500K	# gain-bandwidth product
TN	= 25	# nominal temperature in [C]
TMIN	= 0	# minimum temperature of operation (simulation) in [C]
TMAX	= 70	# maximum temperature of operation (simulation) in [C]
SRPN	= 1.87	# positive going slew rate for nominal temperature in [V/us]
SRPMIN	= 1.87	# positive going slew rate for min temperature in [V/us]
SRPMAX	= 1.87	# positive going slew rate for max temperature in [V/us]
SRN	= 0.8	# negative going slew rate in [V/us]
VCC	= 15	# typical positive supply voltage
VIN_CM_MAX	= 14.9	# higher limit of input common mode voltage
VEE	= -15	# typical negative supply voltage
VIN_CM_MIN	= -12.5	# lower limit of input common mode voltage
IBIAS_N	= 90E-9	# input bias current for nominal temperature
IBIAS_MIN	= 11E-8	# input bias current for minimum temperature
ROUT	= 900	# output resistance
ROAC	= 70	# output resistance for alternating current
AVD	= 200K	# open loop voltage gain in [V/V]
IOSN	= 30E-10	# input offset current for nominal temperature
IOSMIN	= 33E-10	# input offset current for minimum temperature
IOSMAX	= 24E-10	# input offset current for maximum temperature
VOSN	= .0015	# input offset voltage for nominal temperature
VOSMIN	= .00165	# input offset voltage for minimum temperature
VOSMAX	= .00123	# input offset voltage for maximum temperature
CMRR	= 100	# common mode rejection ratio in [dB]
FCMRR	= 160	# 3dB frequency of common mode rejection ratio
PSRR	= 115	# average power supply rejection ratio in [dB]
FPSRRP	= 800	# 3dB frequency of positive power supply rejection ratio
FPSRRN	= 800	# 3dB frequency of negative power supply rejection ratio

Parameter	Value	Parameter Definition
ISUP	= .00166	# supply current
ISUP0	= .00146	# extrapolated supply current for VCC=0
OVERSHOOT	= 5	# overshoot of small signal pulse response in [%]
PHIM	= 50	# phase margin for 0dB frequency in [deg]
PHIM_OVRSHT	= 0	# phase margin/overshoot switch [1/0]
ISCP	= 0.025	# output positive short-circuit current
ISCN	= 0.037	# output negative short-circuit current
VOUT_MIN	= -13.5	# minimum output voltage
VOUT_MAX	= 13.8	# maximum output voltage

- .PARSET MC4558 _OPAMPPNP
  This is a parset for the _OPAMPPNP template for opamps with a pnp transistor input stage.

Parameter	Value	Parameter Definition
NOISE	= 45	# spectral noise density in [nV/sqrt(Hz)]
GBW	= 2.8MEG	# gain-bandwidth product
TN	= 25	# nominal temperature in [C]
TMIN	= 0	# minimum temperature of operation (simulation) in [C]
TMAX	= 70	# maximum temperature of operation (simulation) in [C]
SRNN	= 1.6	# negative going slew rate for nominal temperature in [V/us]
SRNMIN	= 1.6	# negative going slew rate for min temperature in [V/us]
SRNMAX	= 1.6	# negative going slew rate for max temperature in [V/us]
SRP	= 1.5	# positive going slew rate in [V/us]
VCC	= 15	# typical positive supply voltage
VIN_CM_MAX	= 14	# higher limit of input common mode voltage
VEE	= -15	# typical negative supply voltage
VIN_CM_MIN	= -14	# lower limit of input common mode voltage
IBIAS_N	= 80E-9	# input bias current for nominal temperature
IBIAS_MIN	= 85E-9	# input bias current for minimum temperature
ROUT	= 200	# output resistance
ROAC	= 50	# output resistance for alternating current
AVD	= 200K	# open loop voltage gain in [V/V]
IOSN	= 20E-9	# input offset current for nominal temperature
IOSMIN	= 25E-9	# input offset current for minimum temperature

Parameter	Value	Parameter Definition
IOSMAX	= 15E-9	# input offset current for maximum temperature
VOSN	= .001	# input offset voltage for nominal temperature
VOSMIN	= .0012	# input offset voltage for minimum temperature
VOSMAX	= .0007	# input offset voltage for maximum temperature
CMRR	= 90	# common mode rejection ratio in [dB]
FCMRR	= 3000	# 3dB frequency of common mode rejection ratio
PSRR	= 90	# average power supply rejection ratio in [dB]
FPSRRP	= 1000	# 3dB frequency of positive power supply rejection ratio
FPSRRN	= 100	# 3dB frequency of negative power supply rejection ratio
ISUP	= .0012	# supply current
ISUP0	= .001	# extrapolated supply current for VCC=0
OVERSHOOT	= 15	# overshoot of small signal pulse response in [%]
PHIM	= 50	# phase margin for 0dB frequency in [deg]
PHIM_OVRSHT	= 0	# phase margin/overshoot switch [1/0]
ISCP	= 0.02	# output positive short-circuit current
ISCN	= 0.02	# output negative short-circuit current
VOUT_MIN	= -14	# minimum output voltage
VOUT_MAX	= 14	# maximum output voltage

- .PARSET TL072CP _OPAMPFET
  The parset for the _OPAMPFET template for opamps with an unipolar transistor input stage.

Parameter	Value	Parameter Definition
VNOISE	= 18	# spectral noise density in [nV/sqrt(Hz)]
GBW	= 4000K	# gain-bandwidth product
TN	= 25	# nominal temperature in [C]
TMIN	= 0	# minimum temperature of operation (simulation) in [C]
TMAX	= 70	# maximum temperature of operation (simulation) in [C]
SRP	= 14.0	# positive going slew rate for nominal temperature in [V/us]
SRNN	= 14.6	# negative going slew rate for nominal temperature in [V/us]
SRNMIN	= 14.9	# negative going slew rate for min temperature in [V/us]
SRNMAX	= 14.1	# negative going slew rate for max temperature in [V/us]
VCC	= 15	# typical positive supply voltage
VIN_CM_MAX	= 15.2	# higher limit of input common mode voltage

Parameter	Value	Parameter Definition
VEE	= -15	# typical negative supply voltage
VIN_CM_MIN	= -12.5	# lower limit of input common mode voltage
IBIAS_N	= 6E-11	# input bias current for nominal temperature
IBIAS_MAX	= 9E-10	# input bias current for maximum temperature
ROUT	= 800	# output resistance
ROAC	= 50	# output resistance for alternating current
AVD	= 150000	# open loop voltage gain in [V/V]
IOSN	= 5E-12	# input offset current for nominal temperature
IOSMAX	= 8E-11	# input offset current for maximum temperature
VOSN	= .002	# input offset voltage for nominal temperature
VOSMIN	= .00225	# input offset voltage for minimum temperature
VOSMAX	= .00155	# input offset voltage for maximum temperature
CMRR	= 100	# common mode rejection ratio in [dB]
FCMRR	= 200	# 3dB frequency of common mode rejection ratio
PSRR	= 105	# average power supply rejection ratio in [dB]
FPSRRP	= 1000	# 3dB frequency of positive power supply rejection ratio
FPSRRN	= 50	# 3dB frequency of negative power supply rejection ratio
ISUP	= .00184	# supply current
ISUP0	= .00125	# extrapolated supply current for VCC=0
OVERSHOOT	= 11	# overshoot of small signal pulse response in [%]
PHIM	= 30	# phase margin for 0dB frequency in [deg]
PHIM_OVRSHT	= 0	# phase margin/overshoot switch [1/0]
ISCP	= .038	# output positive short-circuit current
ISCN	= .035	# output negative short-circuit current
VOUT_MIN	= -13.6	# minimum output voltage
VOUT_MAX	= 13.9	# maximum output voltage

The parameter sets for modified templates for opamps with offset balance circuits and compensation are very similar.

Chapter 3
VeriBest Analog BJT Model Library

On the following pages, BJT model parameters are defined and BJT model equations are shown.

Model Parameters

An asterisk (*) indicates that the model parameters are scaled by the AREA factor.

Name	Parameter	Units	Default
IS *	Transport saturation current	A	1.0E–16
LEVEL	BJT Model Selector (1=normal, 2=user-defined)	—	1
BF	Ideal maximum forward beta	—	100(npn) 50 (pnp)
NF	Forward current emission coefficient	—	1.0
VAF	Forward Early voltage	1/V	—
IKF *	Corner for forward beta high current roll-off	A	—
ISE *	B-E leakage saturation current	A	0.0
C2	B-E leakage saturation current coefficient	—	0.0
NE	B-E leakage emission coefficient	—	1.5
BR	Ideal maximum reverse beta	—	1.0 (npn) 10.0 (pnp)
NR	Reverse current emission coefficient	—	1.0
VAR	Reverse Early voltage	1/V	—
IKR *	Corner for reverse beta high current roll-off	A	—
ISC *	B-C leakage saturation current	A	0.0
C4	B-C leakage saturation current coefficient	—	0.0
NC	B-C leakage emission coefficient	—	2.0
RB *	Zero bias base resistance	Ω	0.0
IRB *	Current where base resistance falls halfway to its minimum value	A	0.0
RBM *	Minimum base resistance at high currents	Ω	RB
RE *	Emitter resistance	Ω	0.0
RC *	Collector resistance	Ω	0.0

Name	Parameter	Units	Default
CJE *	B-E zero bias depletion capacitance	F	0.0
VJE	B-E built-in potential	V	0.75
MJE	B-E junction exponential factor	—	0.33
TF	Ideal forward transit time	sec	0.0
XTF	Coefficient for bias dependence of TF	—	0.0
VTF	Voltage describing VBC dependence of TF	V	—
ITF *	High-current parameter for effect on TF	—	0.0
PTF	Excess phase at 1/(2∗TF)Hz	—	0.0
CC *	B-C zero bias depletion capacitance	F	0.0
VJC	B-C built-in potential	V	0.75
MJC	B-C junction exponential factor	—	0.33
XCJC	Fraction of B-C depletion capacitance connected to internal base node	—	1.0
TR	Ideal reverse transit time	sec	0.0
CJS *	Zero bias substrate junction capacitance	F	0.0
VJS	Substrate junction built-in potential	V	0.75
MJS	Substrate junction exponential factor	—	0.0
XTB	Forward and reverse beta temperature exponent	—	0.0
EG	Energy gap for temperature effect on IS	V	1.11
XTI	Temperature exponent for effect on IS	—	3.0
FC	Coefficient for forward-bias depletion capacitance formula	—	0.5
ISS *	Substrate junction saturation current	A	0.0
NS	Substrate junction emission coefficient	—	1.0
SUBS	Substrate connection selector		
	+1 vertical geometry (NPN)	—	1
	−1 lateral geometry (PNP)	—	1
TRC1	Collector resistor first order temperature coefficient	1/deg	0.0
TRC2	Collector resistor second order temperature coefficient	$1/deg^2$	0.0
TRB1	Base resistor first order temperature coefficient	1/deg	0.0
TRB2	Base resistor second order temperature coefficient	$1/deg^2$	0.0
TRE1	Emitter resistor first order temperature coefficient	1/deg	0.0
TRE2	Emitter resistor second order temperature coefficient	$1/deg^2$	0.0
PMAX	Maximum power dissipation	W	—
KF	Flicker noise coefficient	—	0.0
AF	Flicker noise exponent	—	1.0

BJT Model Equations

$$v_t = \frac{kT}{q}$$

$$ISE = C2IS$$

$$ISC = C4IS$$

DC Current

$$q_1 = \frac{1}{1 - \frac{vbc}{VAF} - \frac{vbe}{VAR}}$$

$$q_2 = \frac{IS}{IKF}\left(e^{\frac{vbe}{v_t}} - 1\right) + \frac{IS}{IKR}\left(e^{\frac{vbc}{v_t}} - 1\right)$$

$$q_b = \frac{1}{2}q_1(1 + \sqrt{1 + 4q_2})$$

$$ic = \frac{IS}{q_b}\left(e^{\frac{vbe}{v_t}} - e^{\frac{vbc}{v_t}}\right) - \frac{IS}{BR}\left(e^{\frac{vbc}{v_t}} - 1\right) - ISC\left(e^{\frac{vbc}{NCv_t}} - 1\right)$$

$$ib = \frac{IS}{BF}\left(e^{\frac{vbe}{v_t}} - 1\right) + ISE\left(e^{\frac{vbe}{NEv_t}} - 1\right) + \frac{IS}{BR}\left(e^{\frac{vbc}{v_t}} - 1\right) + ISC\left(e^{\frac{vbc}{NCv_t}} - 1\right)$$

If IRB = 0.0, then

$$RB = RBM + \frac{RB - RBM}{q_b}$$

If IRB > 0.0, then

$$z = \frac{-1 + \sqrt{1 + 14.59025\left(\frac{ib}{IRB}\right)}}{2.4317\sqrt{\frac{ib}{IRB}}}$$

$$RB = RBM + 3(RB - RBM)\frac{(\tan(z) - z)}{z\tan^2(z)}$$

Charge Storage

$$q_{be} = TF\frac{1 + XTF e^{\frac{vbc}{\sqrt{2}VTF}}\left[\frac{IS\left(e^{\frac{vbe}{v_t}} - 1\right)}{IS\ e^{\frac{vbe}{v_t}} + ITF}\right]^2}{q_b} IS\left(e^{\frac{vbe}{v_t}} - 1\right) + \int_0^{vbe} C_{be}(v)dv$$

$$q_{bc} = TR\ IS\left(e^{\frac{vbc}{v_t}} - 1\right) + XCJC\int_0^{vbc} C_{bc}(v)dv$$

$$q_{bxc} = (1 - XCJC)\int_0^{vbc} C_{bc}(v)dv$$

$$C(v) = \frac{CJO}{\left(1 - \frac{v}{VJ}\right)^M} \qquad if\ v < FC\ VJ$$

$$C(v) = \frac{CJO}{(1 - FC)^{(1+M)}}\left[1 - FC(1 + M) + \frac{v}{VJ}M\right] \quad if\ v \quad FC \geq VJ$$

Temperature Dependence

- TNOM = nominal temperature
- T = analysis temperature
- T_p = previous analysis temperature (TNOM if first temperature analysis)

The model quantities at the current analysis temperature are written without any suffix. The quantities at the previous temperature are denoted by the suffix p. The quantities at the nominal temperature are denoted by the suffix NOM.

$$IS = IS_p \; e^{\frac{q\left(\frac{T}{T_p}-1\right)EG}{kT}} \left(\frac{T}{T_p}\right)^{XTI}$$

$$BF = BF_p\left(\frac{T}{T_p}\right)^{XTB}$$

$$BR = BR_p\left(\frac{T}{T_p}\right)^{XTB}$$

$$ISE = ISE_p e^{\frac{q\left(\frac{T}{T_p}-1\right)EG}{NEkT}} \left(\frac{T}{T_p}\right)^{\frac{XTI}{NE}} \left(\frac{T}{T_p}\right)^{-XTB}$$

$$ISC = ISC_p \; e^{\frac{q\left(\frac{T}{T_p}-1\right)EG}{NCkT}} \left(\frac{T}{T_p}\right)^{\frac{XTI}{NC}} \left(\frac{T}{T_p}\right)^{-XTB}$$

$$VJ = \frac{kT}{q} \; ln\left(\frac{N_A N_D}{n_i^2}\right)$$

$$E_{gT} = 1.16 - \frac{7.02 \times 10^{-4} T^2}{T + 1108}$$

$$VJ = \frac{T}{T_p}\left\{VJ_p - \left\{- 2\frac{kT_p}{q}\left[\frac{3}{2}ln\frac{T_p}{TNOM} + q\left(-\frac{E_{gp}}{2kT_p} + \frac{E_{gNOM}}{2kT_{NOM}}\right)\right]\right\}\right\}$$

$$+ \left\{- 2\frac{kT}{q}\left[\frac{3}{2}ln\frac{T}{TNOM} + q\left(-\frac{E_g}{2kT} + \frac{E_{gNOM}}{2kT_{NOM}}\right)\right]\right\}$$

$$CJ = CJ_{NOM}\left\{1 + M\left[0.0004(T - TNOM) - \frac{VJ - VJ_{NOM}}{VJ_{NOM}}\right]\right\}$$

$$RE = RE_{NOM}[1 + TRE1(T - TNOM) + TRE2(T - TNOM)^2]$$

$$RC = RC_{NOM}[1 + TRC1(T - TNOM) + TRC2(T - TNOM)^2]$$

$$RB = RB_{NOM}[1 + TRB1(T - TNOM) + TRB2(T - TNOM)^2]$$

$$RBM = RBM_{NOM}[1 + TRB1(T - TNOM) + TRB2(T - TNOM)^2]$$

Chapter 4
VeriBest Analog Diode Model Library

On the following pages, diode model parameters are defined and diode model equations are shown.

Model Parameters

An asterisk (*) indicates that the model parameters are scaled by the AREA factor. A number sign (#) indicates that the model parameters are scaled by periphery, PJ.

Name	Parameter	Units	Default
IS*	Saturation current per unit area	A	1.0E–14
ISP#	Sidewall saturation current per unit junction periphery	A/PJ	0.0
N	Emission coefficient	—	1
BV	Reverse breakdown voltage	V	infinite
RS*	Ohmic series resistance	Ω	0.0
CJO*	Zero bias junction capacitance per unit junction bottom wall area	F	0.0
M	Grading coefficient	—	0.5
FC	Coefficient for forward-bias depletion area capacitance formula	—	0.5
VJ	Junction potential for bottom wall	V	1.0
CJP#	Zero bias junction capacitance per unit junction periphery	F/PJ	0.0
MP	Grading coefficient for periphery	—	M
FCP	Coefficient for forward-bias depletion periphery junction capacitance formula	—	FC
VJP	Periphery junction potential	V	VJ
TT	Transit Time	sec	0
EG	Activation Energy	eV	1.11
XTI	Saturation-current temperature exponent (typically 2.0 for Schottky diodes)	—	3.0
TRS	Resistance temperature coefficient	1/deg	0.0
TBV	Temperature coefficient for breakdown voltage	1/deg	0.0
CTA	Temperature coefficient for area junction capacitance	1/deg	0.0
CTP	Temperature coefficient for periphery junction capacitance	1/deg	0.0
PMAX	Maximum power dissipation	W	—

Name	Parameter	Units	Default
KF	Flicker noise coefficient	—	0.0
AF	Flicker noise exponent	—	1.0

Diodes Model Equations

DC Current

$$v_t = \frac{kT}{q}$$

Large Forward Bias (v > 35 N v_t)

$$i = IS\ e^{35}\left[1 + \frac{1}{Nv_t}(v - 35\ N\ v_t)\right] + ISP\ e^{35}\left[1 + \frac{1}{Nv_t}(v - 35\ N\ v_t)\right]$$

Normal Region (v ≥ - BV)

$$i = IS\left(e^{\frac{v}{Nv_t}} - 1\right) + ISP\left(e^{\frac{v}{Nv_t}} - 1\right)$$

Breakdown Region (v ≥ - BV - 35 v_t)

$$i = IS\left(e^{\frac{-BV}{Nv_t}} - e^{\frac{-BV - v}{v_t}}\right) + ISP\left(e^{\frac{-BV}{Nv_t}} - e^{\frac{-BV - v}{v_t}}\right)$$

Large Reverse Bias (v < - BV - 35 v_t)

$$i = IS\left\{e^{\frac{-BV}{Nv_t}} - e^{35}\left[1 - \frac{1}{v_t}(v + BV + 35v_t)\right]\right\}$$

$$+ ISP\left\{e^{\frac{-BV}{Nv_t}} - e^{35}\left[1 - \frac{1}{v_t}(v + BV + 35v_t)\right]\right\}$$

Diode Charge

$$q = TTi + \int_0^v C_{bottom}(v)dv + \int_0^v C_{periphery}(v)dv$$

$$C(v) = \frac{CJO}{\left(1 - \frac{v}{VJ}\right)^M} \qquad if\ v < FC\ VJ$$

$$C(v) = \frac{CJO}{(1 - FC)^{(1+M)}}\left[1 - FC(1 + M) + \frac{v}{VJ}M\right] \qquad if\ v \geq FC\ \ VJ$$

Temperature Dependence

- TNOM = nominal temperature
- T = analysis temperature
- T_p = previous analysis temperature (TNOM if first temperature analysis)

The model quantities at the current temperature are written without any suffix. The quantities at the previous temperature are denoted by the suffix p. The quantities at the nominal temperature are denoted by the suffix NOM.

$$CJ = CJ_{NOM}[1 + CTA(T - TNOM)] \qquad if\ CTA \neq 0.0$$

$$CJP = CJP_{NOM}[1 + CTA(T - TNOM)] \qquad if\ CTP \neq 0.0$$

$$VJ = \frac{kT}{q}\ ln\ \frac{N_A N_D}{(n_i)^2}$$

$$VJ = \frac{T}{T_p}\left\{VJ_p - \left\{-\ 2\frac{kT_p}{q}\left[\frac{3}{2}\ ln\left(\frac{T_p}{TNOM}\right) + q\left(-\frac{E_{gp}}{2kT_p} + \frac{E_{gNOM}}{2kT_{NOM}}\right)\right]\right\}\right\}$$

$$+\left\{-\ 2\frac{kT}{q}\left[\frac{3}{2}\ ln\left(\frac{T}{TNOM}\right) + q\left(-\frac{E_g}{2kT} + \frac{E_{gNOM}}{2kT_{NOM}}\right)\right]\right\}$$

$$CJ = CJ_{NOM}\left\{1 + M\left[0.0004(T - TNOM) - \frac{VJ - VJ_{NOM}}{VJ_{NOM}}\right]\right\}$$

$$VJP = \frac{kT}{q}\ ln\left[\frac{N_A N_D}{(n_i)^2}\right]$$

$$VJP = \frac{T}{T_p}\left\{VJP_p - \left\{-\ 2\frac{kT_p}{q}\left[\frac{3}{2}\ ln\left(\frac{T_p}{TNOM}\right) + q\left(-\frac{E_{gp}}{2kT_p} + \frac{E_{gNOM}}{2kT_{NOM}}\right)\right]\right\}\right\}$$

$$+\left\{-\ 2\frac{kT}{q}\left[\frac{3}{2}\ ln\left(\frac{T}{TNOM}\right) + q\left(-\frac{E_g}{2kT} + \frac{E_{gNOM}}{2kT_{NOM}}\right)\right]\right\}$$

$$CJP = CJP_{NOM}\left\{1 + MP\left[0.0004(T - TNOM) - \frac{VJP - VJP_{NOM}}{VJP_{NOM}}\right]\right\}$$

$$IS = IS_p\left(\frac{T}{T_p}\right)^{\frac{XTI}{N}} e^{\frac{q\left(\frac{T}{T_p}-1\right)^{EG}}{NkT}}$$

$$BV = BV_{NOM}[1 + TBV(T - TNOM)]$$

$$RS = RS_{NOM}[1 + TRS(T - TNOM)]$$

Chapter 5
VeriBest Analog JFET Model Library

On the following pages, JFET model parameters are defined and JFET model equations are shown.

Model Parameters

An asterisk (*) indicates that the model parameters are scaled by the AREA factor.

Name	Parameter	Units	Default
VTO	Threshold voltage (negative for N-type) (positive for P-type)	V	–2.0
BETA *	Transconductance parameter	A/V^2	1E–4
LAMBDA	Channel length modulation parameter	1/V	0.0
RD *	Drain ohmic resistance	Ω	0.0
RS *	Source ohmic resistance	Ω	0.0
CGS *	Zero bias g-s junction capacitance	F	0.0
CGD *	Zero bias g-d junction capacitance	F	0.0
PB	Gate junction potential	V	1.0
IS	Gate junction saturation current	A	1.0E–14
FC	Coefficient for forward-bias depletion capacitance formula	—	0.5
PMAX	Maximum power dissipation	W	—
KF	Flicker noise coefficient	—	0.0
AF	Flicker noise exponent	—	1.0
MJS	Source grading coefficient	—	0.5
MJD	Drain grading coefficient	—	0.5

JFET Model Equations

DC Current

$$ids = 0 \qquad if\ vgs - VTO \le 0$$

$$= BETA\ (vgs - VTO)^2(1 + LAMBDA\ vds) \qquad if\ 0 < vgs - VTO < vds$$

$$= 2BETA(1 + LAMBDA\ vds)\ vds\left(vgs - VTO - \frac{1}{2}\ vds\right) \qquad if\ 0 < vds \le vgs - VTO$$

Temperature Dependence

- TNOM = nominal temperature
- T = analysis temperature
- T_p = previous analysis temperature (TNOM if first temperature analysis)

The model quantities at the current temperature are written without any suffix. The quantities at the previous temperature are denoted by the suffix p. The quantities at the nominal temperature are denoted by the suffix NOM.

$$IS = IS_p\ e^{\frac{q\left(\frac{T}{T_p} - 1\right)\ 1.11}{k\ T}}$$

$$PB = \frac{T}{T_p}\left\{PB_p - \left\{-\ 2\frac{kT_p}{q}\left[\frac{3}{2}\ ln\left(\frac{T_p}{TNOM}\right) + q\left(-\frac{E_{gp}}{2kT_p} + \frac{E_{gNOM}}{2kT_{NOM}}\right)\right]\right\}\right\}$$

$$+\left\{-\ 2\frac{kT}{q}\left[\frac{3}{2}\ ln\left(\frac{T}{TNOM}\right) + q\left(-\frac{E_g}{2kT} + \frac{E_{gNOM}}{2kT_{NOM}}\right)\right]\right\}$$

$$CGS = CGS_{NOM}\left\{1 + 0.5\left[0.0004\ (T - TNOM) - \left(\frac{PB - PB_{NOM}}{PB_{NOM}}\right)\right]\right\}$$

$$CGD = CGD_{NOM}\left\{1 + 0.5\left[0.0004\ (\ T - TNOM\ ) - \left(\frac{PB - PB_{NOM}}{PB_{NOM}}\right)\right]\right\}$$

Chapter 6
VeriBest Analog DIABLOLib Model Library

DIABLOLib models are a unique collection of system level components that allow you to simulate and analyze multi-discipline systems. DIABLOLib components link to the VeriBest Analog Simulation Engine. The models allow you to combine digital logic with analog devices, or mechanical systems and their driving circuitry, to obtain a complete simulation showing the interaction of different disciplines. In other words, only one simulator is now required for a complex system.

Because these components are behavioral models, they provide a means for system design. They can also be used in combination with primitive-level models. Once you have completed your system design, you can create a more in-depth analog design using fully characterized primitive-level models from the VeriBest model libraries.

You can use DIABLOLib models in electrical applications which include designs involving phase-locked loops, motor controls, filters, modems, cellular telephones, audiovisual equipment, switching power supplies, and radio equipment. Applications in the mixed-discipline area include devices such as fluid-level detectors, strain gauges, thermocouples, motors, relays, solenoids, and optical elements. Control systems designed with DIABLOLib components are found in robotics, aircraft ailerons and elevators, supervisory control and alarm networks, and industrial process control.

Parameter passing is a feature of DIABLOLib models and allows you to pass in information to program the components.

DIABLOLib Model

The DIABLOLib model is made up of system level functional blocks. Symbols for functional blocks are installed in the `symlib` directory, in the `diablo.slb` symbol library. The symbols can be placed in your VeriBest Design Capture file.

The parameter files reside in the `/analog` directory in the DIABLO library, and can be edited using the VeriBest Analog Model Library Manager (VBA MLM).

DIABLOLib Symbols

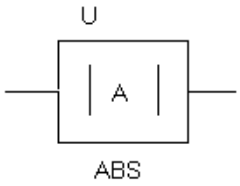
The following pages show the DIABLOLib symbols and their corresponding descriptions. Input and output impedances are provided in most of the models so that it is not necessary for you to add them. Refer to the figure below.

The models which do not have impedances provided are:

- SWITCH1
- SWITCH2
- The input side of CTOS
- The output sides of STOC, STOV, VTOS, and DIFF

ABS

Absolute value of the input.



ADC1

Unipolar straight binary 8-bit analog-to-digital converter. The model converts analog signal ranging from 0 to VREF. The least significant bit is VREF/256. Associated with the model is a parameter file ADC1 with the parameters:

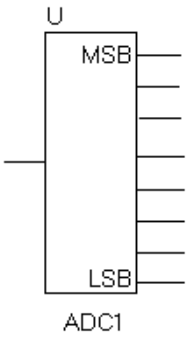
- VREF - reference voltage.
- PERIOD - time interval the input is constant.
- DELAY - delay time from sampling of the input to updating the new digital outputs.
- ST - Sample time

The A/D converter may be used with a sample and hold circuit (SMPLHLD). The following guidelines are useful for selecting parameters of the sample and hold and A/D converter:

- PERIOD = user specified
- ST = .1 ∗ PERIOD
- HT = .9 ∗ PERIOD
- STC = .1 ∗ ST
- HTC = 1000 ∗ HT

For example, the following is a typical parameter set:

PERIOD = .25, ST = .025, HT = .225, STC = .0025, HTC = 225,
DELAY = .025



ADC2

Bipolar straight binary 8-bit analog-to-digital converter. The model converts analog signal ranging from VL to VH. The least significant bit is (VL-VH)/256. Associated with the model is a parameter file ADC2 with the parameters:

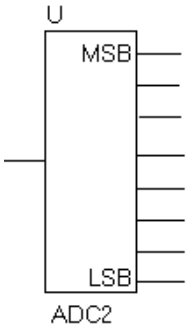
- VH - upper voltage. When all the bits are high (1) the input is greater or equal to 255/256 x (VH-VL)+VL
- VL - lower voltage
- PERIOD - time interval, the input is constant.
- DELAY - delay time from sampling of the input to updating the new digital outputs.
- ST - Sample time

The A/D converter may be used with a sample and hold circuit (SMPLHLD). The following guidelines are useful for parameter selection of the sample and hold and A/D converter:

- PERIOD = user specified
- ST = .1 ∗ PERIOD
- HT = .9 ∗ PERIOD
- STC = .1 ∗ ST
- HTC = 1000 ∗ HT
- Simulation Timestep = 1 to 5 times smaller than STC. HT < DELAY ≤ 5 ∗ timestep.

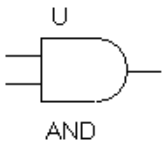
For example, the following is a typical parameter set:

PERIOD = .25, ST = .025, HT = .225, STC = .0025,
HTC = 225, timestep = .001, DELAY = .02



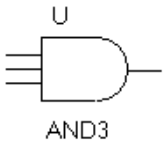
AND

Logical AND, two inputs. Logic one is greater than or equal to 0.5. Logic zero is less than 0.5. The output is either 1 or 0.



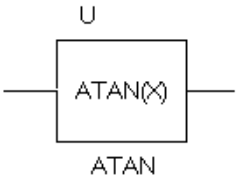
AND3

Logical AND, three inputs. The output is either 1 or 0



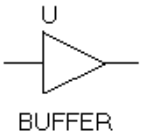
ATAN

Arctangent function whose output is defined from -π/2 to π/2



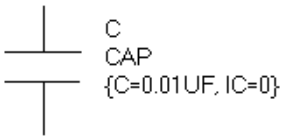
BUFFER

Current buffer with variable input impedance and negligible output impedance. Parameter, R, is the input impedance.



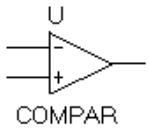
CAP

Capacitor with user-specified initial voltage IC. The user should take caution for any DC balance or topological constraints when selecting the initial condition. The positive reference for the initial voltage is on pin 1



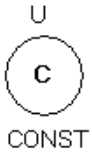
COMPAR

Voltage comparator. The output is 1 if input (+) is greater than input (-). The output is 0 if input (+) is less than or equal to input (-). The block has very high input impedance and negligible output impedance



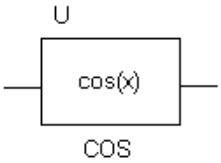
CONST

Constant value signal source.



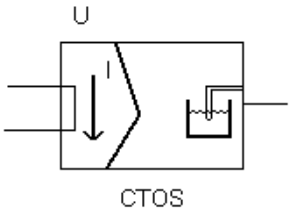
COS

The output is the cosine of the input voltage. The optimal value for inputs is from $-\pi$ to π. This block loses accuracy for very large magnitude inputs



CTOS

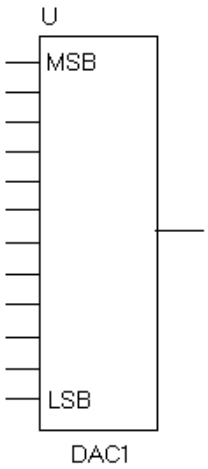
Current to signal transducer. The output signal is proportional to the current flowing through the branch from input 1 to input 2. The path between the input pins is a short



DAC1

Unipolar straight binary 12-bit digital-to-analog converter. The output ranges from zero to VREF∗4095/4096 and the least significant bit is VREF/4096, where VREF is a user defined parameter of the model. The model converts instantaneously. Digital inputs are assumed to take on the values of either 0 for off, or 1 for on.

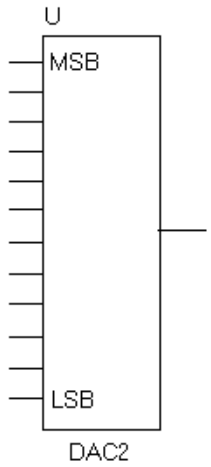
Note: If the input voltages are larger than 0.5, they are treated as on. If the input voltages are less than 0.5, they are treated as off.



DAC2

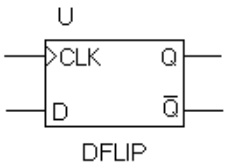
Bipolar straight binary 12-bit digital-to-analog converter. The output ranges from VL to 4095/4096 * (VH-VL)+VL, where VL and VH are user defined parameters. The least significant bit is (VH-VL)/4096. The model converts instantaneously. Digital inputs are assumed to take on the values of either 0 for off, or 1 for on.

Note: If the inputs are larger than 0.5, they are treated as on. If the inputs are less than 0.5, they are treated as off



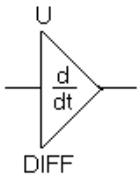
DFLIP

Data flip-flop. The input, D, is a logical value of 1 or 0. The output follows the input when the clock is changing from low (0) to high (1). The initial output state of the flip-flop is low (0). To ensure accuracy, D should be constant while the clock is in transition



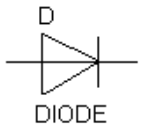
DIFF

Ideal differentiator. In AC analysis, this model is accurate up to 1KHz.



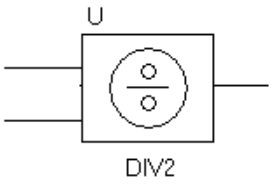
DIODE

Ideal diode.



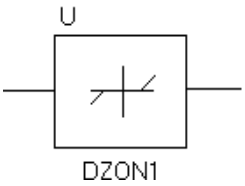
DIV2

The output is upper input divided by lower input. Lower input should not be zero at any time



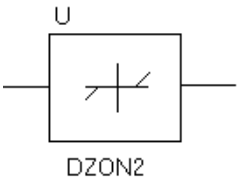
DZON1

Symmetric dead zone with the limit specified as a parameter to the block. The parameter, DEAD, is the symmetric range where the output is zero



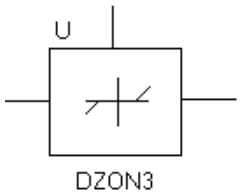
DZON2

Non-symmetric dead zone with the limits specified as parameters. LOW and HIGH are the upper and lower non-symmetric limits inside which the output is zero. LOW must be less than HIGH



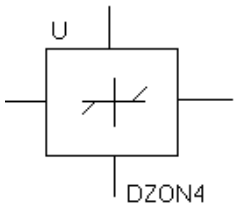
DZON3

Symmetric dead zone with the limit introduced as an external input on the top pin



DZON4

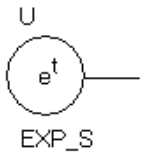
Non-symmetric dead zone with external limits. The voltage on the top pin is the upper limit, and the voltage on the bottom pin is the lower limit.



EXP_S

Exponential pulse source with the parameters entered in a model, EXP_S. The parameters are:

- V1 - initial value
- V2 - peak value
- TDl - rise delay time (sec)
- TAU1 - rise time constant (sec)
- TD2 - fall delay time (sec)
- TAU2 - fall time constant (sec)
- PERIOD - period (sec)

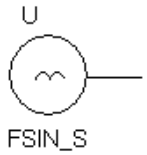


FSIN_S

Full-wave rectified sinusoidal source with the parameters entered in a model FSIN_S. The parameters are:

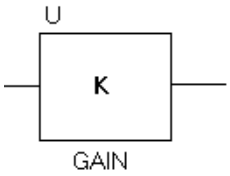
- OFF - offset
- AMP - amplitude
- FREQ - frequency (Hz)
- TD - time delay (sec)
- DAMP - damping factor (1/sec)

- PHASE - phase (radians



GAIN

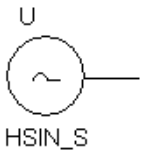
Ideal gain block.



HSIN_S

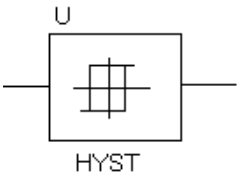
Half-wave rectified sinusoidal source with the parameters entered in a model HSIN_S. The parameters are:

- OFF - offset
- AMP - amplitude
- FREQ - frequency (Hz)
- TD - time delay (sec)
- DAMP - damping factor (1/sec)
- PHASE - phase (radians)



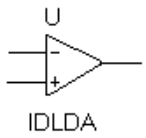
HYST

In the Hysteresis or Schmitt trigger model, the output switches from OUT_LOW to OUT_HIGH when the input crosses IN_HIGH. The output switches back when the input falls below IN_LOW.



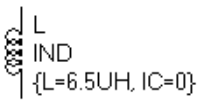
IDLDA

Ideal differential input opamp. The parameter A is the gain of the opamp.



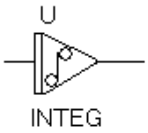
IND

Inductor with user-specified initial condition, IC. The user should take caution for any DC balance or topological constraints when selecting the initial conditions. The initial current is from upper pin to lower pin



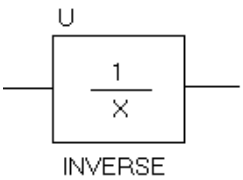
INTEG

Ideal integrating amplifier. The parameter IC allows the user to specify an initial output voltage value. The initial condition is used only if IC is toggled ON in the TIME dialog in the Analysis option in the VeriBest Analog Simulation Engine.



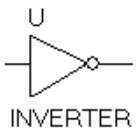
INVERSE

The output is the input to the –1 power. Output is equal to 1/Input. The input should never be zero



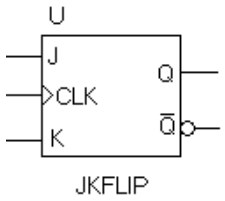
INVERTER

Ideal unit gain inverter. Output is equal to –Input.



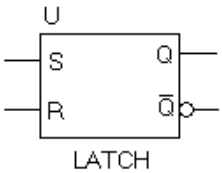
JKFLIP

JK flip-flop. The output can change on a positive-going (from 0 to 1) edge of the clock, its new value depending on J and K. When J and K are zero, there is no change in the output state after clocking. When J is high (1) and K is low (0), the output goes high. When K is high and J is low, the output goes low. When J and K are both high, the flip-flop changes state after clocking. The parameter, DELAY, is a propagation delay time from clocking to steady-state of the flip-flop. The clock pulse may be of any width (but the simulation timestep should accommodate for short pulse widths); however, the time between positive-going edges of the clock pulses should be at least two orders of magnitude greater than DELAY. The initial state of the flip-flop is zero



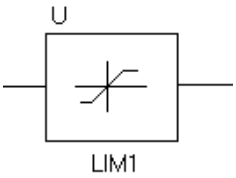
LATCH

Logical SR-Latch with outputs Q and $\overline{Q}$. The output goes high (1) when the set goes high (>0). The output goes low (0) when the reset goes high (>0). The set and reset may not both be high, otherwise, the simulator will not be able to interpret the correct output and will print an error message in the output date file. The initial state of the latch is zero.



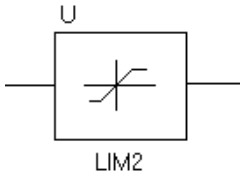
LIM1

Symmetric limiter with the limit value, LIM, as a parameter. LIM is assumed to be a positive value.



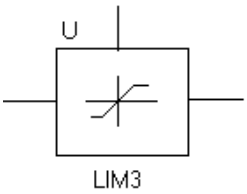
LIM2

Non-symmetric limiter with the limits TOP and BOT as parameters. TOP is the upper limit and BOT is the lower limit



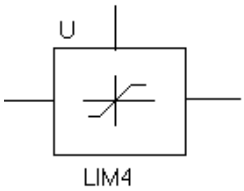
LIM3

Symmetric limiter, where the top pin is the externally supplied limit input. The limit input is assumed to be a positive value.



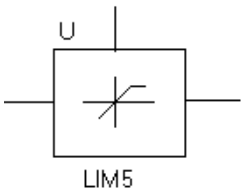
LIM4

Non-symmetric limiter with the limits external. The upper limit source is supplied through the top pin, and the lower limit through the bottom pin



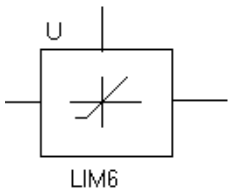
LIM5

Positive limiter with the upper limit TOP as a parameter.



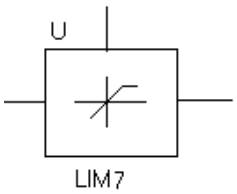
LIM6

Negative limiter with the lower limit BOT as a parameter.



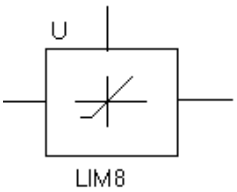
LIM7

Positive limiter with the limit external and applied at the top pin.



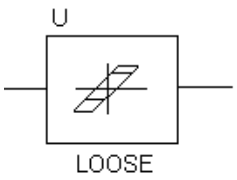
LIM8

Negative limiter with the limit external and applied at the top pin.



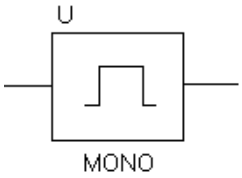
LOOSE

The parameters are LOW, lower limit, and HIGH, upper limit, with HIGH > LOW. LOW and HIGH define a range of values where switching the level of the output is delayed. If the input is increased above HIGH, the output is proportional to the input, but with offset -HIGH. When the input begins to decrease, it's peak value, P, is held at the output until the input goes below (P-(HIGH-LOW)). Below this value the output decreases proportional to the input, but with an offset of LOW, until the input begins to increase, when its minimum value is held at the output.



MONO

Monostable multivibrator or one-shot. A pulse of fixed duration appears at the output when the input is “triggered”. Parameters VCC and T determine, respectively, the trigger level and the pulse width. The output is 0 if the input is greater than VCC/3. When a negative-going pulse less than VCC/3 is applied at the input, a pulse from 0 to 1 lasting T seconds appears at the output. The input should initially be set for the one-shot to be “off”.

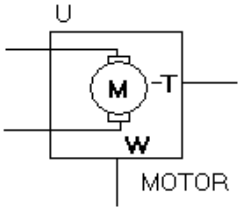


MOTOR

Separately excited DC motor. The model includes electrical effects in a DC motor, namely the conversion from applied voltage to motor torque. The model contains the following parameters:

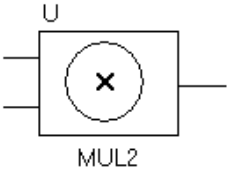
- KI - torque constant (Nm/A)
- KB - back emf constant (V/rad/sec)
- RM - motor resistance (ohms)
- LM - motor inductance [H]
- I0 - idle current [A]
- W0 - idle angular speed [RPM]
- J - rotor movement of inertia [kg m^2]

The mechanical effects of the shaft and load are realized outside of the motor model using the motor torque, available on pin T as a voltage converted within 1V/Nm conversion coefficient, as input. The shaft speed must be fed back to pin W of the motor model for back emf. The mechanical portion may include motor and load moments of inertia, motor and load viscous damping and other effects



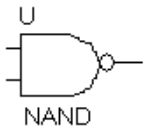
MUL2

Multiplies input 1 and input 2.



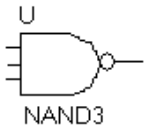
NAND

Logical NAND gate, 2 input. Logic high is > 0.5 Logic low is ≤ 0.5 The output is either 1 or 0



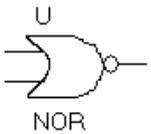
NAND3

Logical NAND gate, 3 input.



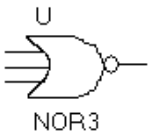
NOR

Logical NOR gate, 2 input. Logic high is > 0.5 Logic low is ≤ 0.5 The output is either 1 or 0



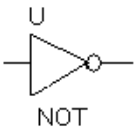
NOR3

Logical NOR gate, 3 input



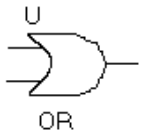
NOT

Logical NOT



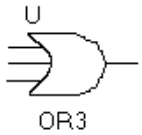
OR

Logical OR gate, 2 input. Logic high is > 0.5 Logic low is ≤ 0.5 The output is either 1 or 0.



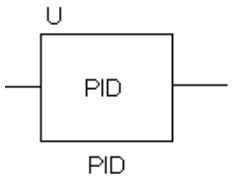
OR3

Logical OR gate, 3 input.



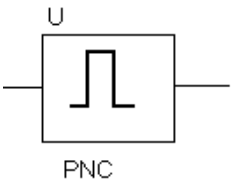
PID

Proportional-Integral-Derivative controller emulates a transfer function of the form: KP+KI/s+KD∗s.



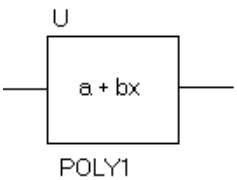
PNC

Pulse narrowing circuit, complement of the component MONO. In response to a positive-going pulse, a pulse of T seconds appears at the output, where T is less than the input pulse width.



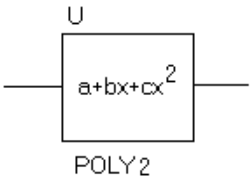
POLY1

Polynomial function block of order 1.



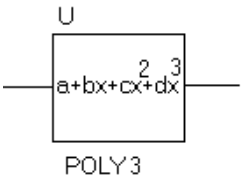
POLY2

Polynomial function block of order 2



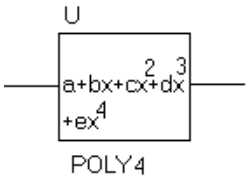
POLY3

Polynomial function block of order 3.



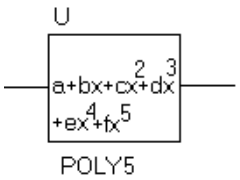
POLY4

Polynomial function block of order 4.



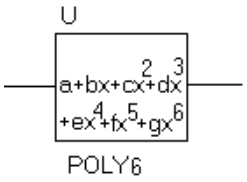
POLY5

Polynomial function block of order 5.



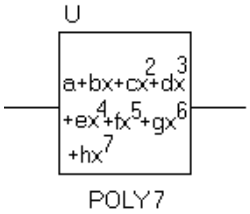
POLY6

Polynomial function block of order 6.



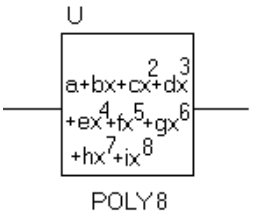
POLY7

Polynomial function block of order 7



POLY8

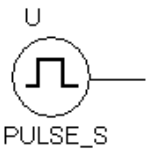
Polynomial function block of order 8.



PULSE_S

Pulse source, where the parameters are entered in the model PULSE_S. The parameters are:

- V1 - initial value
- V2 - peak value
- TD - time delay (sec)
- TR - rise time (sec)
- TF - fall time (sec)
- PW - pulse width (sec)
- PER - period (sec)

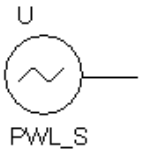


PWL_S

Piecewise linear source where the parameters are entered in the model PWL_S. The parameters are:

- T1, V1 - V1 is the value at time T1
- T2, V2 - V2 is the value at time T2
- T3, V3 - V3 is the value at time T3
- T4, V4 - V4 is the value at time T4
- T5, V5 - V5 is the value at time T5
- T6, V6 - V6 is the value at time T6
- T7, V7 - V7 is the value at time T7
- T8, V8 - V8 is the value at time T8

Linear interpolation is used between the defined points.

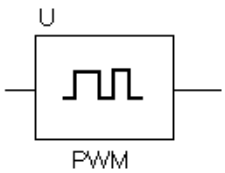


PWM

Pulse width modulator. Produces a square wave varying between -1 and 1 whose duty cycle is given by:

```
D.C. = 1/2-Vin/VMAX
```

Where VMAX is a user-specified parameter and Vin is the input signal. The parameter, period, should be chosen to be greater than the highest frequency of the input and/or to be the fundamental desired frequency at the output.



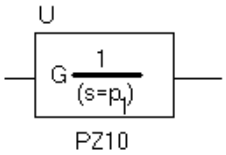
PZ10

Pole/Zero block. Both numerator and denominator polynomials have real coefficients, because the block represents an object described by a differential equation with real coefficients (no real object is described by a differential equations with complex coefficients). This means that poles and zeros are either real or complex conjugate pairs. Complex conjugate pairs require that the imaginary part be entered only once for the pair and the real part (the same value) be entered individually for each pole/zero in the pair. Initial conditions are zero. For example, PZ22 contains the parameters and values:

G = 100
PR1 = 100
PR2 = 100
PI1 = 0
ZR1 = 10

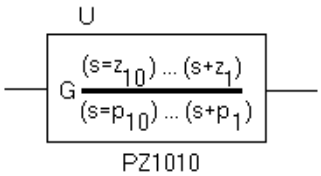
ZR2 = 10
ZI1 = 0

through....



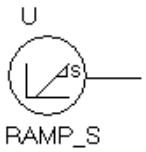
PZ1010

Pole/Zero block. The real and imaginary parts of the poles and zeros are entered in a model PZ1010. Complex conjugate pairs require that the imaginary part be entered only once for the pair and the real part be entered individually for each pole/zero in the pair. Initial conditions are zero



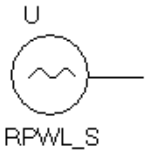
RAMP_S

Ramp input source where the parameters are S, slope, and, DELAY, time delay in seconds.



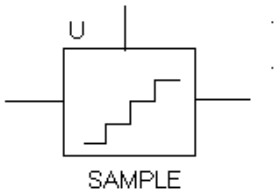
RPWL_S

Repeating piecewise linear source where the parameters are entered in a model, RPWL_S. The parameters are T(1-8), V(1-8) - 8 time points and their values. This pattern of points is repeated periodically. Linear interpolation is used between time points.



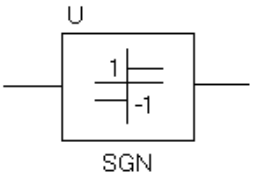
SAMPLE

Sample on condition, for a periodic sampling of a continuous analog signal. The input is sampled (i.e. the output tracks the input) when the control input (pin 2) is 1. The last value of the input is held when the control input is 0. User defined parameters, HTC and STC, are time constants determining, respectively, how long the input value can be held at the output and how quickly the output tracks the input during sampling. HTC should be about 2-3 orders of magnitude greater than the longest anticipated interval between samples. STC is typically much smaller than HTC (for example, 2-3 orders of magnitude) and can be larger for slowly varying inputs.



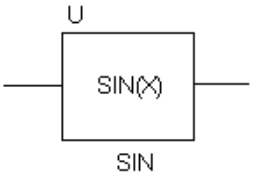
SGN

The sign function. The output is 1 or -1 depending on the sign of the input.



SIN

The output is the sine of the input. The input is optimal in the range: $-\pi/2$ to $\pi/2$. This block loses accuracy for very large magnitude inputs.

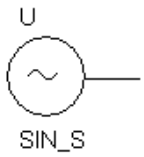


SIN_S

Sinusoidal source with parameters entered in a model SIN_S. The parameters are:

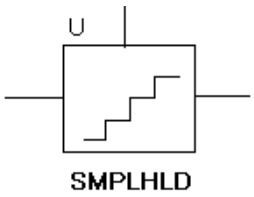
- OFF - offset
- AMP - amplitude
- FREQ - frequency (Hz)
- TD - time delay (sec)
- DAMP - damping factor (1/sec)

- PHASE - phase (radians)



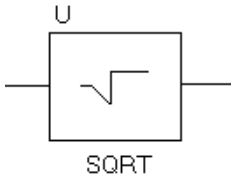
SMPLHLD

Sample and hold circuit for periodic sampling of a continuous analog signal. The output is a staircase-type function having the same value as the input during the sampling interval. The parameters ST and HT determine the sample and hold time, respectively. The parameters HTC and STC are time constants defining respectively, how long a sampled value can be held and how quickly the input can be tracked during sampling. HTC should be about 3 orders of magnitude greater than HT. STC should be about 2 orders of magnitude less than ST. However, if HT is small and the input is slowly varying STC may be larger.



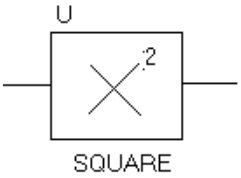
SQRT

Square root of the input. Input must be greater than zero.



SQUARE

The square of the input.

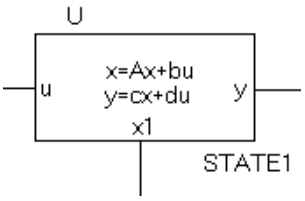


STATE1

First-order state equation of the form:

- $\dot{x} = Ax + bu$
- $y = cx + du$
- $x(0) = x0$

The coefficients a, b, c, and d, and the initial condition x0 are entered in a model, STATE1. Pin 2 is the state variable, x

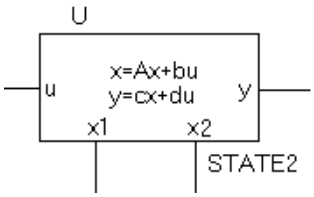


STATE2

Second-order state equation of the form:

- $\dot{x}_1 = a_{11}x_1 + a_{12}x_2 + b_1u$
- $\dot{x}_2 = a_{21}x_1 + a_{22}x_2 + b_2u$
- $y = c_1x_1 + c_2x_2 + du$
- $x_1(0) = x_1$
- $x_2(0) = x_2$

The coefficients of the A matrix, b, c, and d vectors, and the initial conditions x1 and x2 are entered in a model STATE2.

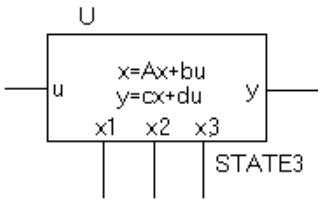


STATE3

Third-order state equation of the form:

- $\dot{x} = Ax + bu$
- $y = cx + du$
- $x(0) = x1, x2, x3$

The coefficients of the A matrix, b, c, and d vectors, and the initial conditions x1, x2, and x3 are entered in a model STATE3



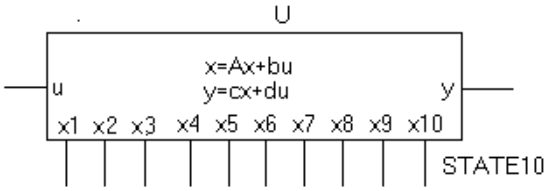
through.....

STATE10

Tenth-order state equation of the form:

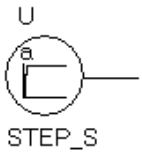
- $\dot{x}$ = Ax + bu
- y = cx + du
- x(0) = x1, x2,.....x10

The coefficients of the A matrix, b, c, and d vectors, and the initial conditions x1, x2, x3, ..., and x10 are entered in a model STATE10.



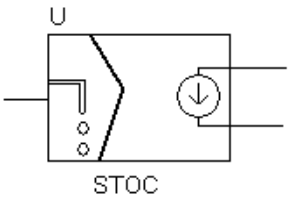
STEP_S

Step input source, where the parameters are time delay, DELAY, in seconds, the magnitude of the step, A, in volts and rise time, TR, in seconds.



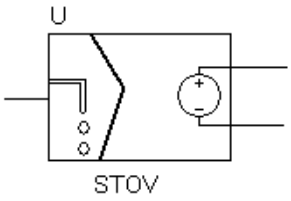
STOC

Signal to current transducer. The input signal is transformed to a current.



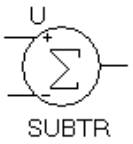
STOV

Signal to voltage transducer. The input signal is transformed to a voltage.



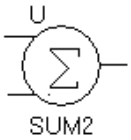
SUBTR

Subtract input 2 from input 1.



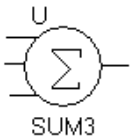
SUM2

Ideal summer with two inputs.



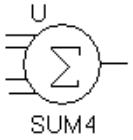
SUM3

Ideal summer with three inputs.



SUM4

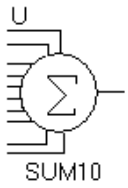
Ideal summer with four inputs.



through.....

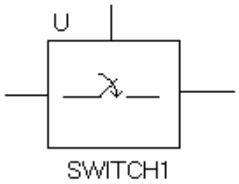
SUM10

Ideal summer with ten inputs



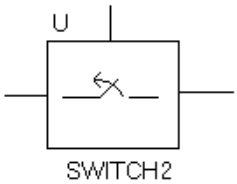
SWITCH1

Half-ideal switch which is either a perfect open or very low impedance short. The switch is open when the control input (top pin) is 0, and it is closed when the control input is 1. To ensure the accuracy of the transition, the control input should be a pulse or a piecewise linear source with minimum rise and fall times.



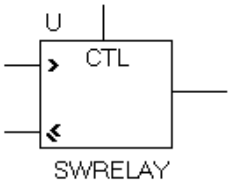
SWITCH2

Half-ideal switch which is either a perfect short or very high impedance open. The switch is open when the control input (top pin) is 1, and it is closed when the control input is 0. To ensure the accuracy of the transition, the control input should be a pulse or a piecewise linear source with minimum rise and fall times



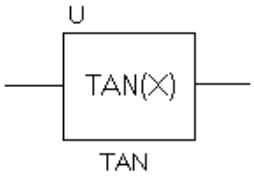
SWRELAY

The output is equal to upper input if the control at top pin is greater than 0. It is equal to lower input if the control is less than or equal to zero.



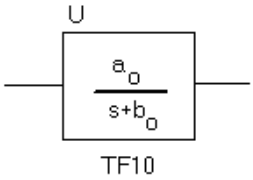
TAN

Tangent function defined between -π/2 and π/2. If at any time the input is equal to n π/2, where n is an integer, the model will fail and the simulator will be unable to converge to a solution at that time point.



TF10

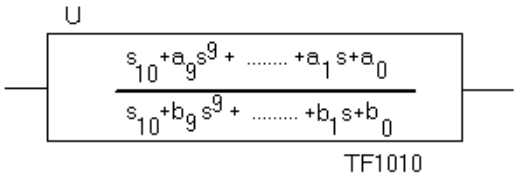
A transfer function with 1 pole and no zeros. The coefficients of the polynomials are entered in a parameter model, TF10.



through.....

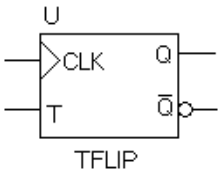
TF1010

A transfer function with 10 poles and 10 zeroes. The coefficients of the polynomials are entered in a parameter model, TF1010. The polynomial a is the numerator and b is the denominator.



TFLIP

Toggle flip-flop. When T is high (1) the output changes state or toggles with each positive-going (from 0 to 1) edge of the clock. When T is low (0), the clock has no effect on the output. The parameter DELAY is a propagation delay time from clocking to steady-state of the flip-flop. The clock pulse may be of any width; however, the time between positive-going edges of the clock pulses should be at least two orders of magnitude greater than DELAY. The initial state of the flip-flop is zero



TIMER

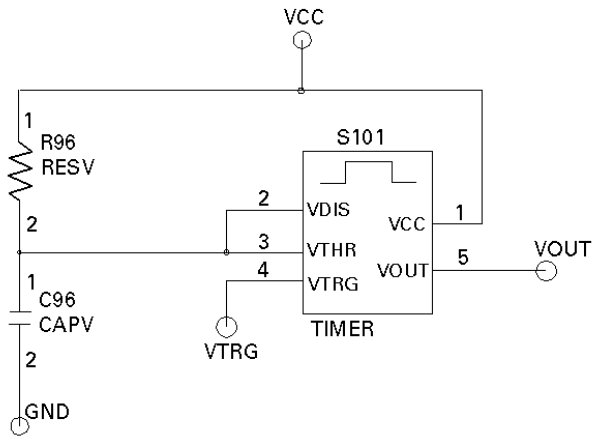
555 timer. The pins are:

- pin 1 - Vcc, supply voltage source (>0)
- pin 2 - Vdis, discharge voltage
- pin 3 - Vthr, threshold voltage
- pin 4 - Vtrg, trigger voltage
- pin 5 - Vout, output

Associated with the timer is a parameter model, TIMER with the following parameters:

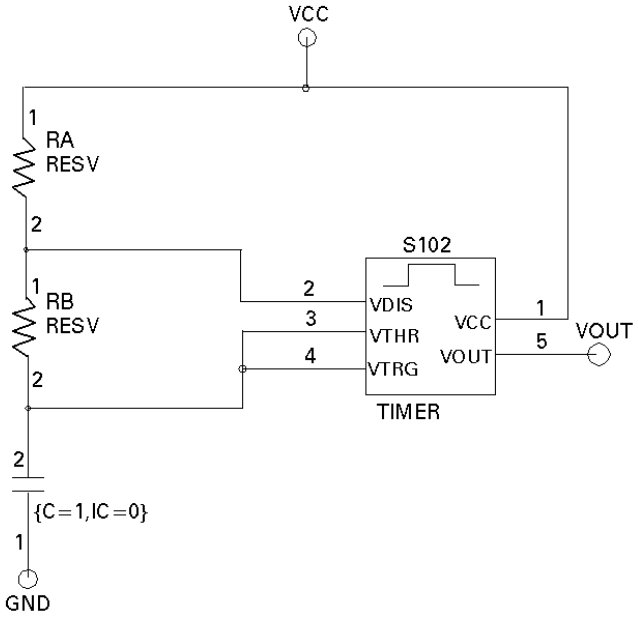
- VCC - initial (or DC) supply voltage
- VOUT - initial output
- VTRG - initial trigger voltage
- VTHR - initial threshold voltage
- DELAY - propagation delay

In order to use the timer as a one-shot, the following circuit can be constructed:

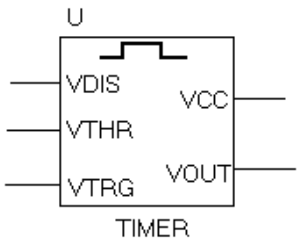


The trigger voltage, Vtrg, should be greater than Vcc/3 when the one-shot is inactive. The initial condition parameters should be set as follows so that the one-shot is “off”: VCC - typically 15V; VOUT = 0; VTRG = DC value of Vtrg (>Vcc/3); VTHR = 0. A negative-going pulse less than Vcc/3 activates the one-shot and a pulse going from 0V to 1V appears at Vout. The output pulse width is given by: T = 1.1RC (sec). The (negative-going) trigger pulse width should be less than T. The parameter, DELAY, may be any small number, less than T/1000.

In order to use the timer as an astable multivibrator, the following circuit can be constructed:

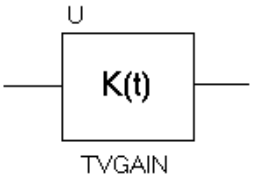


The output is a square wave between 0 and 1 whose frequency is 1.49/(RA+2 RB)C. The duty cycle (≥50%) is determined by the ratio of RA and RB. The astable circuit can be started anywhere in the square wave cycle. The initial state is determined by the capacitor voltage which oscillates between Vcc/3 and 2Vcc/3. Possible starting configurations are: VTHR = VTRG ≤ VCC/3 and VOUT = 1; VCC/3 < VTHR = VTRG < 2VCC/3 and VOUT = 1 or 0; VTHR = VTRG ≥ 2VCC/3 and VOUT = 0. VCC is typically 15V. Finally DELAY should be less than or equal to RB*C/100, and the simulation timestep may be no larger than DELAY.



TVGAIN

Time-varying gain for a piecewise linear variation in time. The parameters T(1-8), V(1-8) are the time points and their values, with linear interpolation in between the points. All are entered in the parameter model TVGAIN.



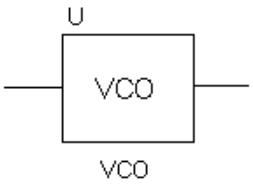
VCO

A voltage controlled oscillator that performs the function:

$$Vout = A \sin\left(\int_0^t 2\pi\ 2(FO+KVin)d\tau+THO\right)$$

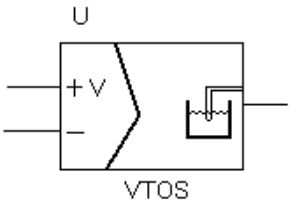
The parameters are:

- A - amplitude [V]
- K - input gain [Hz/V]
- WO - free running frequency [Hz]
- THO - initial phase shift [rad]



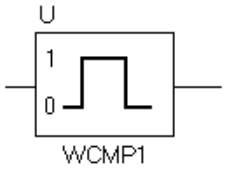
VTOS

Voltage to signal transducer. The output signal is proportional to the input voltage.



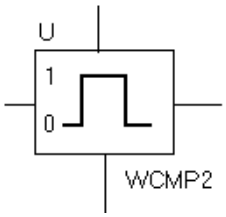
WCMP1

Window comparator. The output is 1 if the input is in the window, else it is 0. The window upper and lower limits, UL and LL, are parameters of the component.



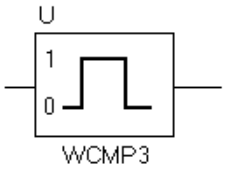
WCMP2

Window comparator. The window is specified by external inputs of upper (top pin) and lower (bottom pin) limits



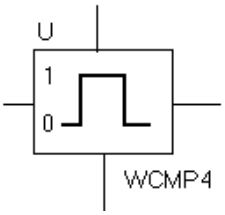
WCMP3

Window comparator. The window is specified by window center and span, CENT and SPAN, which are entered as parameters.



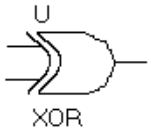
WCMP4

Window comparator. The center and span are specified externally. Center is the top pin and span is the bottom pin.



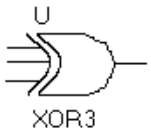
XOR

Logical exclusive OR, 2 inputs. The output is 1 if one of the inputs, but not both, is 1. The output is 0 if both inputs are the same.



XOR3

Logical exclusive OR, 3 input.



Chapter 7
VeriBest Analog High Frequency Model Library

This section describes the RF/Microwave models and their limitations. They are developed as macro-models and can be simulated using the VeriBest Analog Simulation Engine (VBASE).

Transmission lines are the basis of passive RF/Microwave integrated circuits. VBASE simulates only ideal, lossless transmission lines. The characteristic impedance and time delay parameters are needed for this model. These parameters depend on the geometry and material properties of the line.

The discontinuities in the planar transmission line structures contribute to parasitic reactances. These reactances, with the exception of the gap, hole, and notch in the strip conductor (which are introduced purposely for realizing specific circuit functions), are intentionally not introduced. The most common discontinuities are series gap, impedance step discontinuities. The following transmission lines, and their discontinuities at RF/Microwave frequencies, are represented:

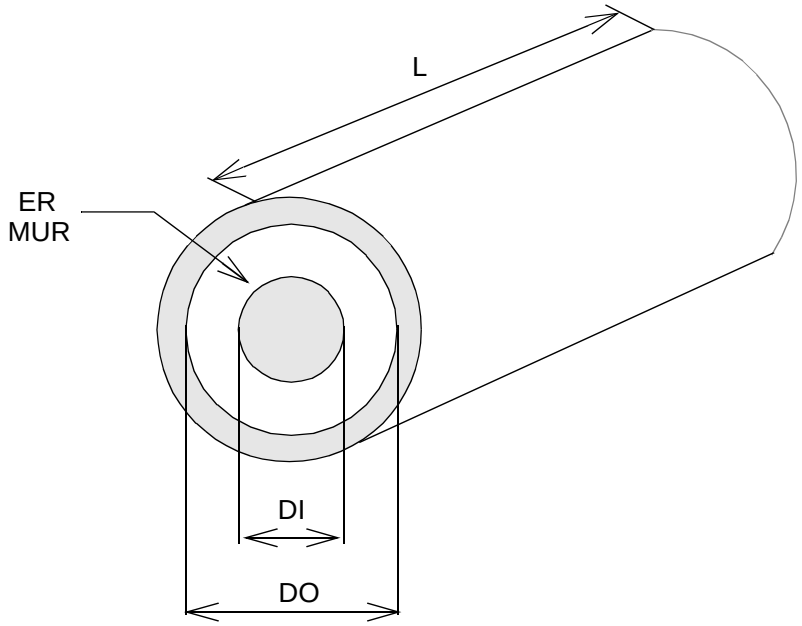
- Coaxial Transmission Lines
- Stripline Elements
- Microstripline Elements
- Lumped Elements at High Frequencies (Microstrip Configuration)
- Suspended Substrate Lines
- Coplanar Guide Transmission Lines
- Rectangular Waveguide Elements
- Antenna Input Impedance Elements
- General Distributed Elements

Coaxial Transmission Lines

The following coaxial transmission lines are represented:

- COAX (Homogeneously Filled Lossless Coaxial Line)
- COAXLOSS (Coaxial Lossy Transmission Line)
- HCOAX (Heterogeneously Filled Lossless Coaxial Line)

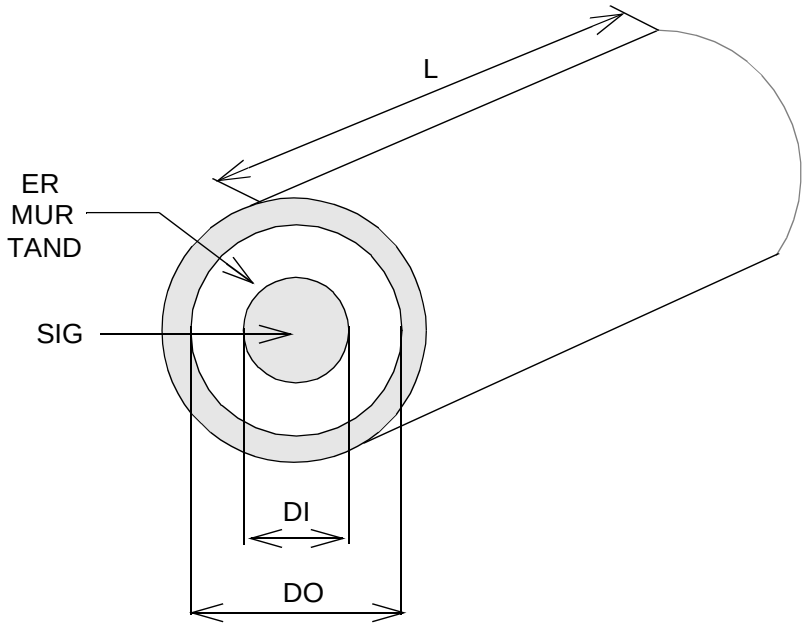
COAX (Homogeneously Filled Lossless Coaxial Line)



The input parameters are:

DO	-	Outer conductor diameter
DI	-	Inner conductor diameter
L	-	Physical length of the line
ER	-	Relative permittivity
MUR	-	Relative permeability

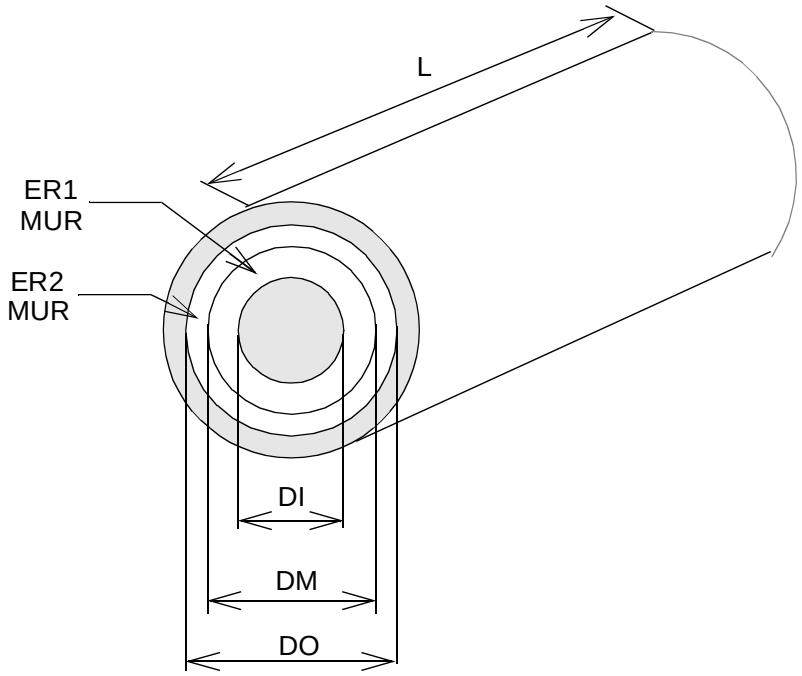
COAXLOSS (Coaxial Lossy Transmission Line)



The input parameters are:

DO	-	Outer conductor diameter
DI	-	Inner conductor diameter
L	-	Physical length of the line
ER	-	Relative permittivity
MUR	-	Relative permeability
SIG	-	Conductivity
TAND	-	Dielectric loss tangent
F	-	Frequency at which the loss is to be accounted

HCOAX (Heterogeneously Filled Lossless Coaxial Line)



The input parameters are:

DO	-	Outer conductor diameter
DI	-	Inner conductor diameter
DM	-	Center conductor diameter
L	-	Physical length of the line
ER1	-	Dielectric constant between inner and center
ER2	-	Dielectric constant between center and outer
MUR	-	Relative permeability

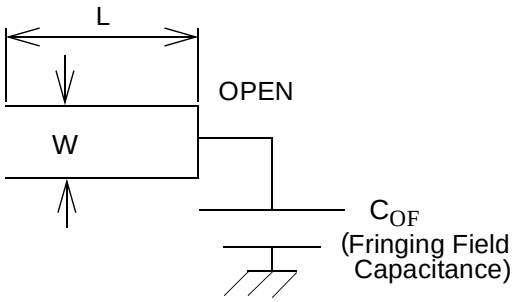
Stripline Elements

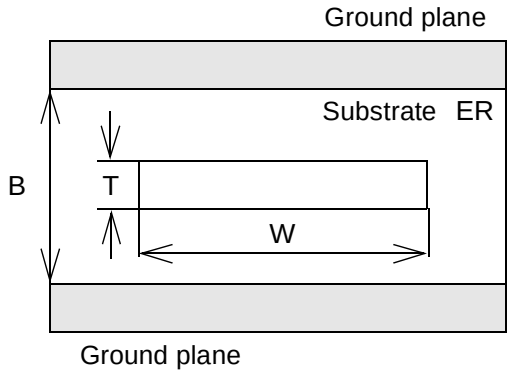
The following stripline elements are represented:

- Transmission Lines
  - SLEF (Stripline With Open End Effect)
  - SLIN (Lossless Strip Transmission Line)
  - SLOC (Ideal Open Circuit Lossless Stripline)
  - SLOSSLIN (Lossy Strip Transmission Line)
  - SLSC (Ideal Short Circuit Lossless Stripline)
  - SOFF (Lossless Stripline With Offset In The Center Conductor)
  - SRLIN (Lossless Strip Transmission Line With Round Conductor)
- Discontinuities
  - SBEND (Stripline With Bend (any angle))
  - SGAP (Stripline With Series Gap Discontinuity)
  - SHOLE (Stripline With Round Hole Discontinuity)
  - SRBEND (Stripline With Right-Angled Bend)
  - SSTEP (Stripline With Step Change in Width)
  - STEE (Stripline With Tee Junction)
- Coupled Lines
  - SBLIN (Symmetrical Broad-Side Coupled Striplines)
  - SCLIN (Symmetrical Edge-Coupled Striplines)
  - SRCLIN (Symmetrical Edge-Coupled Striplines With Round Conductors)

Transmission Lines

SLEF (Stripline With Open End Effect)





The input parameters are:

B - Substrate thickness

W - Width of the conductor

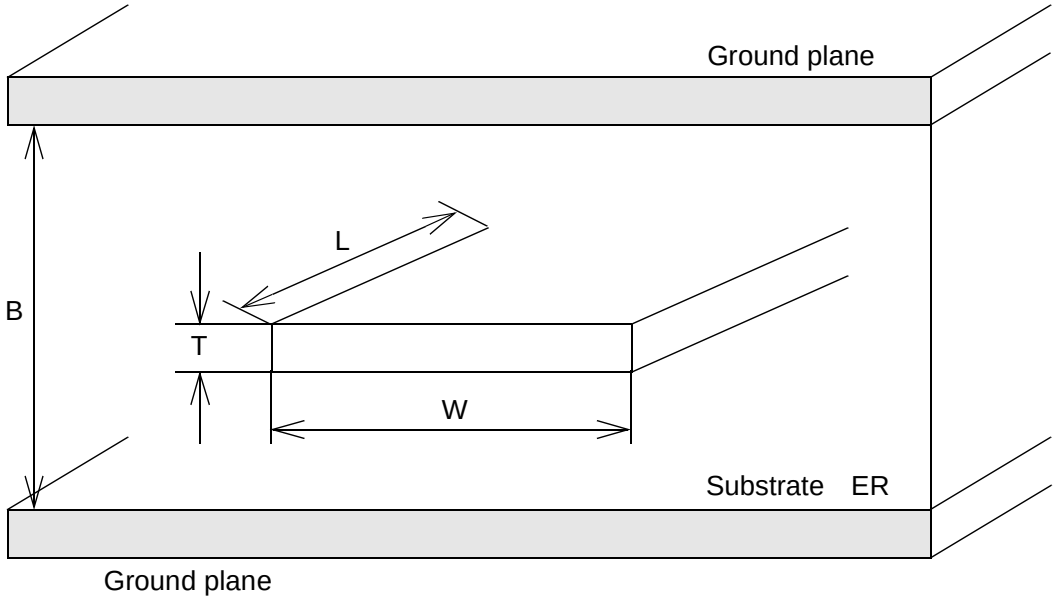
T - Thickness of the conductor

L - Physical length

ER - Substrate dielectric constant

F - Frequency at which the model parameters are to be determined (center frequency of operation)

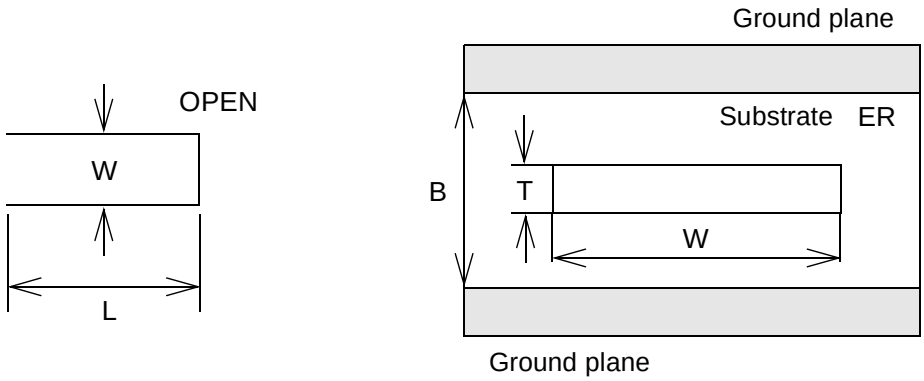
SLIN (Lossless Strip Transmission Line)



The input parameters are:

B	-	Substrate thickness
W	-	Width of the conductor
T	-	Thickness of the conductor
L	-	Physical length of the line
ER	-	Substrate dielectric constant/Relative permittivity

SLOC (Ideal Open Circuit Lossless Stripline)



The input parameters are:

B - Substrate thickness

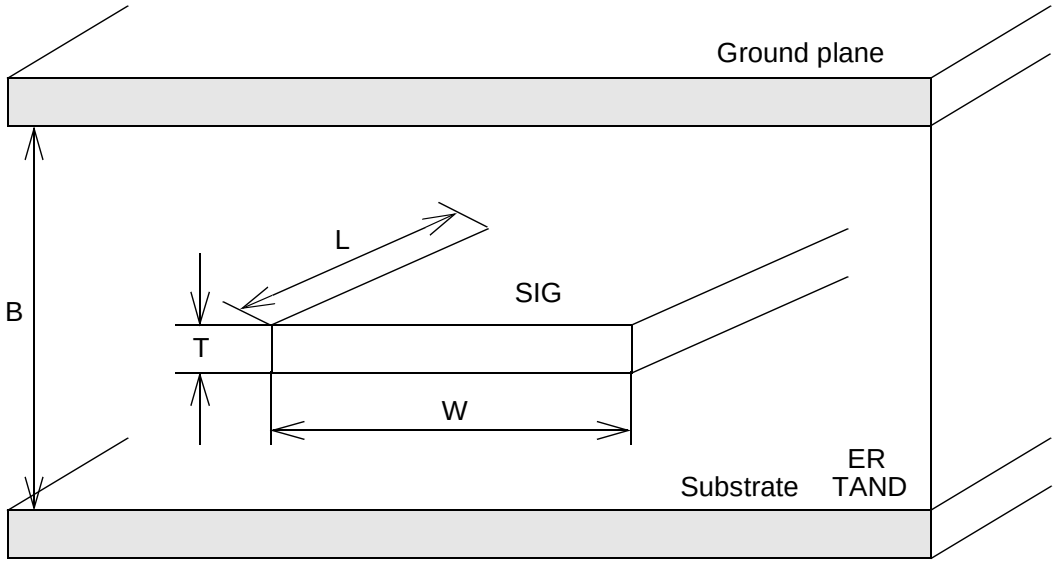
W - Width of the conductor

T - Thickness of the conductor

L - Physical length

ER - Substrate dielectric constant

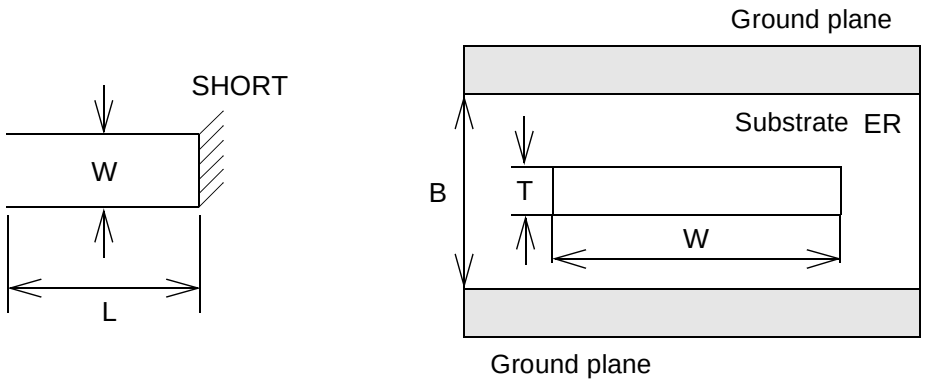
SLOSSLIN (Lossy Strip Transmission Line)



The input parameters are:

B	-	Substrate thickness
W	-	Width of the conductor
T	-	Thickness of the conductor
L	-	Physical length of the line
ER	-	Substrate dielectric constant/Relative permittivity
SIG	-	Conductivity
TAND	-	Dielectric loss tangent
F	-	Frequency at which the dielectric loss is to be calculated

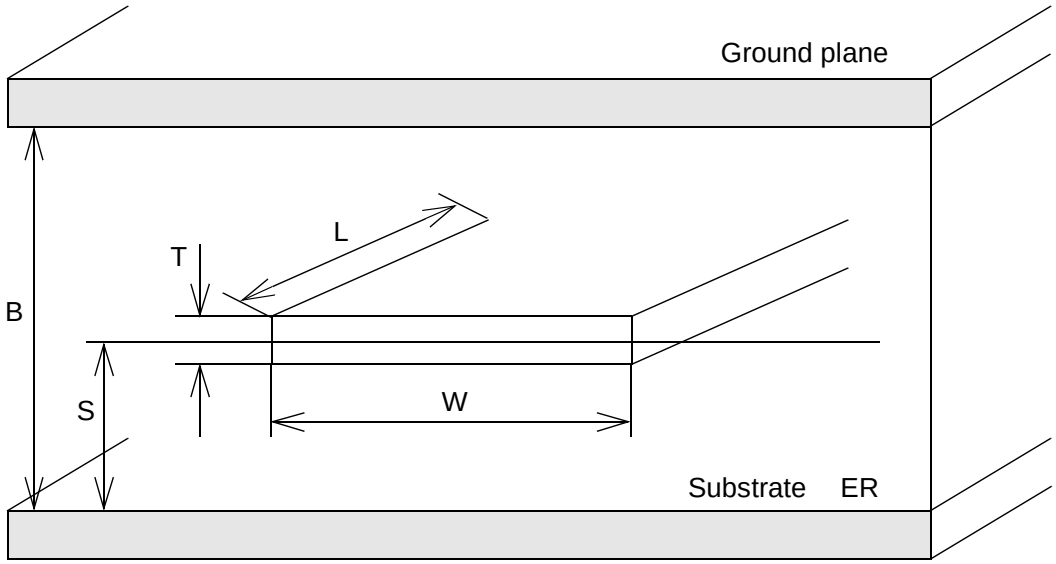
SLSC (Ideal Short Circuit Lossless Stripline)



The input parameters are:

B	-	Substrate thickness
W	-	Width of the conductor
T	-	Thickness of the conductor
L	-	Physical length
ER	-	Substrate dielectric constant

SOFF (Lossless Stripline With Offset In The Center Conductor)



The input parameters are:

B - Substrate thickness

W - Width of the conductor

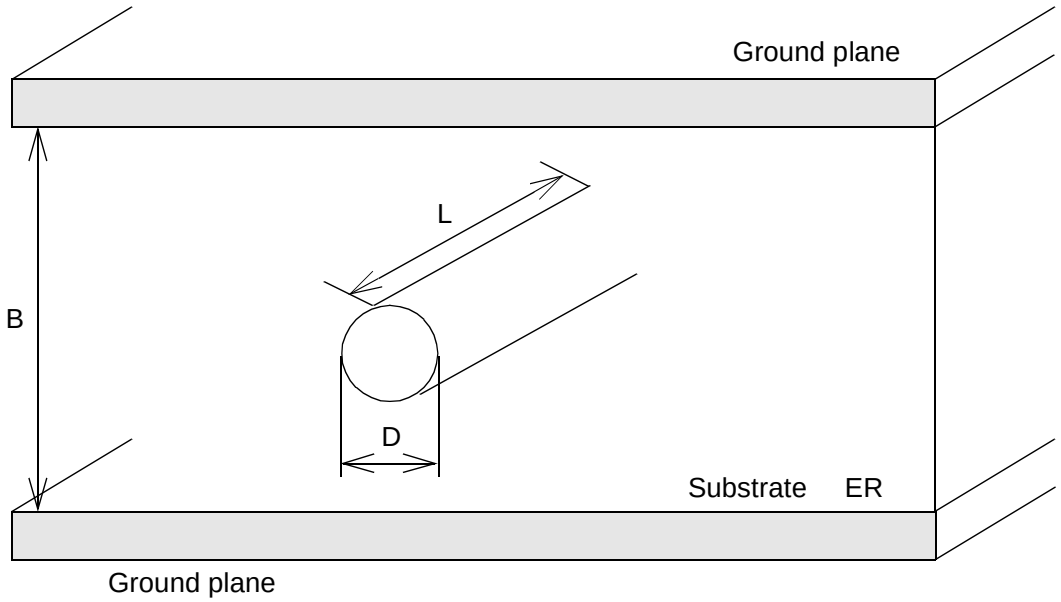
T - Thickness of the conductor

L - Physical length of the line

S - Distance between the bottom ground plane and the center of the conductor

ER - Substrate dielectric constant

SRLIN (Lossless Strip Transmission Line With Round Conductor)



The input parameters are:

B - Substrate thickness

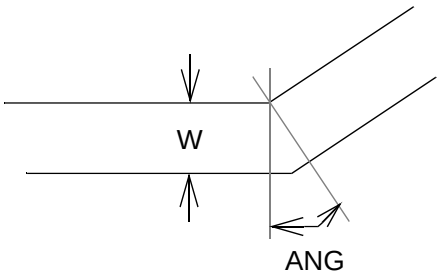
D - Diameter of the conductor

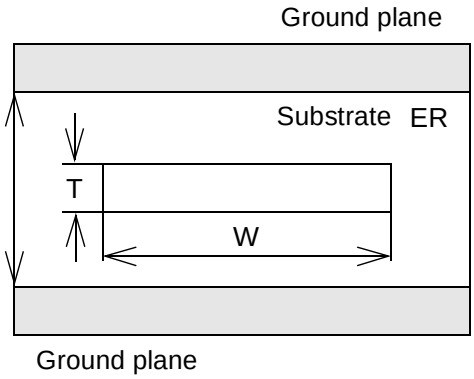
L - Physical length of the line

ER - Dielectric constant of the substrate

Discontinuities

SBEND (Stripline With Bend (any angle))





The input parameters are:

B - Substrate thickness

W - Width of the conductor

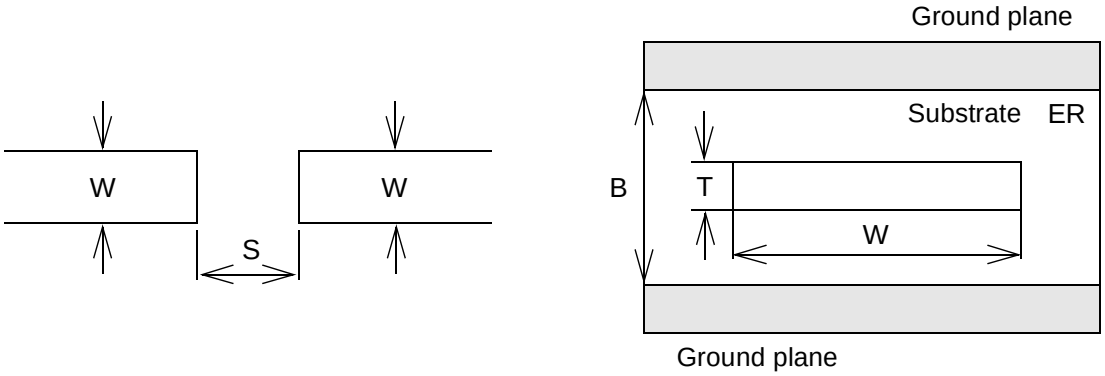
T - Thickness of the conductor

ANG - Angle of the bend

ER - Substrate dielectric constant

F - Frequency at which the model parameters are to be determined

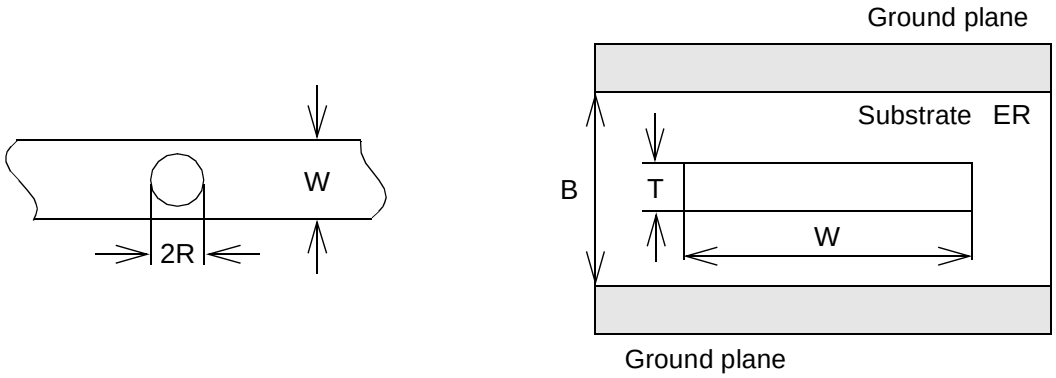
SGAP (Stripline With Series Gap Discontinuity)



The input parameters are:

B - Substrate thickness
W - Width of the conductor
T - Thickness of the conductor
S - Spacing between the edges of the lines
ER - Substrate dielectric constant
F - Frequency at which the model parameters are to be determined

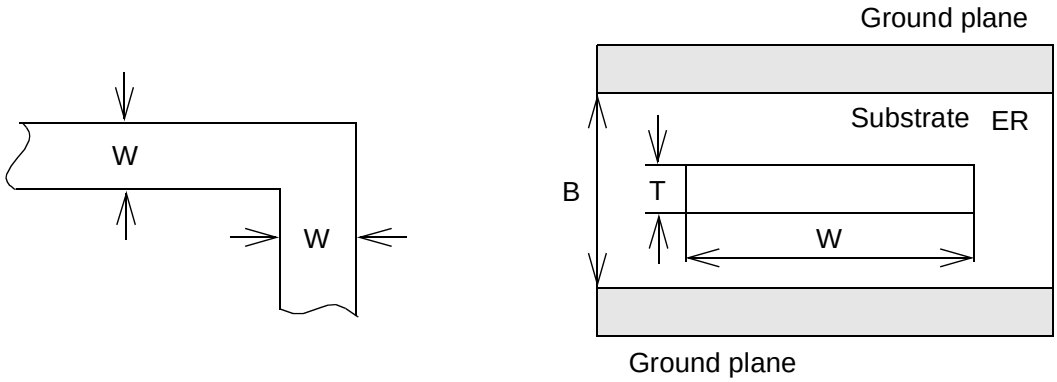
SHOLE (Stripline With Round Hole Discontinuity)



The input parameters are:

B - Substrate thickness
W - Width of the conductor
T - Thickness of the conductor
R - Radius of the shorting hole
ER - Substrate dielectric constant
F - Frequency at which the model parameters are to be determined

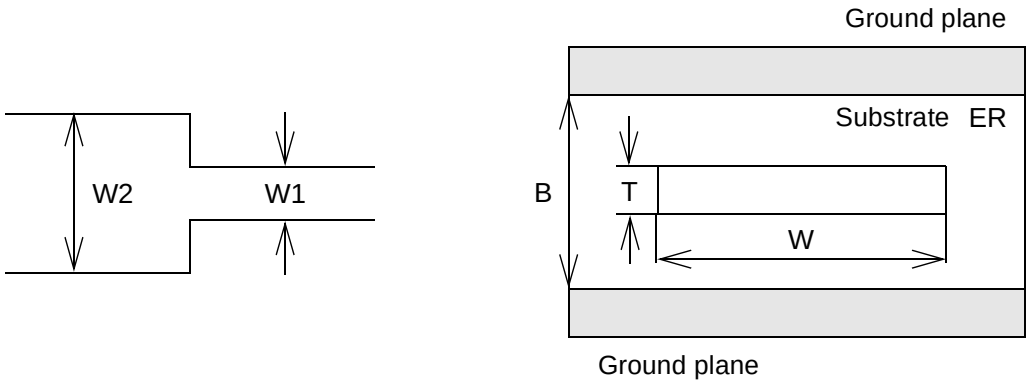
SRBEND (Stripline With Right-Angled Bend)



The input parameters are:

B - Substrate thickness
W - Width of the conductor
T - Thickness of the conductor
ER - Substrate dielectric constant
F - Frequency at which the model parameters are to be determined

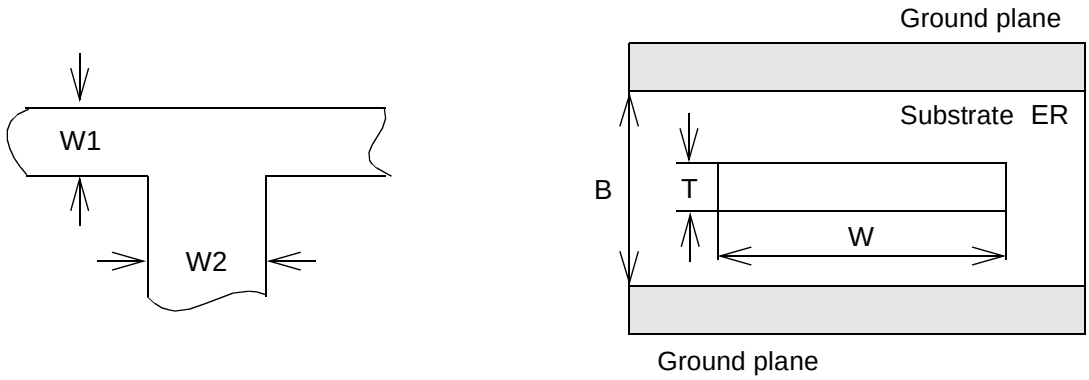
SSTEP (Stripline With Step Change In Width)



The input parameters are:

B - Substrate thickness
W1 - Width of conductor (larger)
W2 - Width of conductor (smaller)
T - Thickness of the conductor
ER - Substrate dielectric constant
F - Frequency at which the model parameters are to be calculated

STEE (Stripline With Tee Junction)

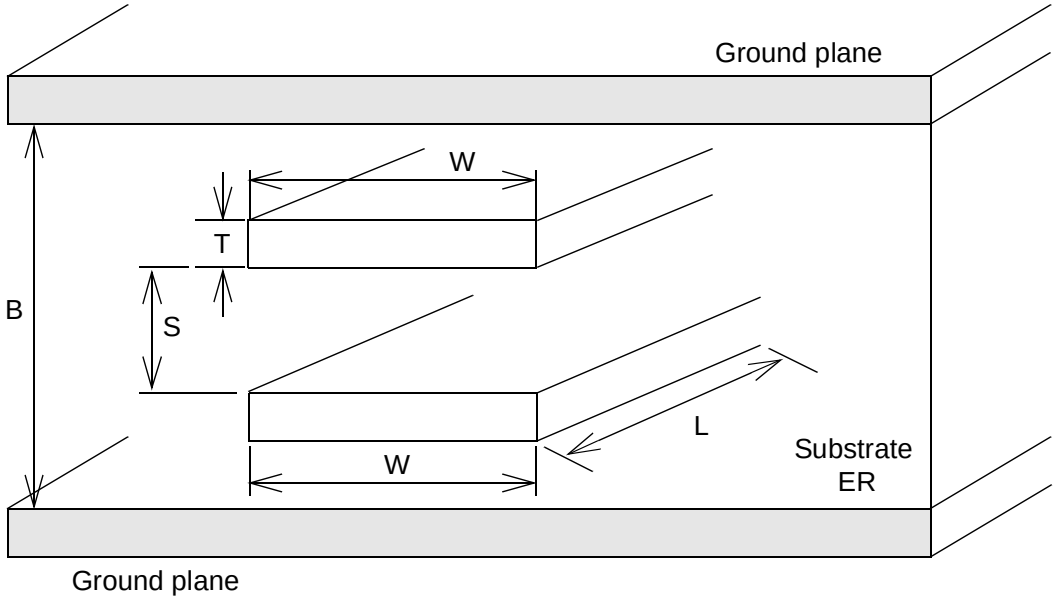


The input parameters are:

B	-	Substrate thickness
W1	-	Width of conductor 1
W2	-	Width of conductor 2
T	-	Thickness of the conductors
ER	-	Substrate dielectric constant
F	-	Frequency at which the model parameters are to be calculated

Coupled Lines

SBCLIN (Symmetrical Broad-Side Coupled Striplines)



The input parameters are:

B - Height of the substrate

W - Width of the lines

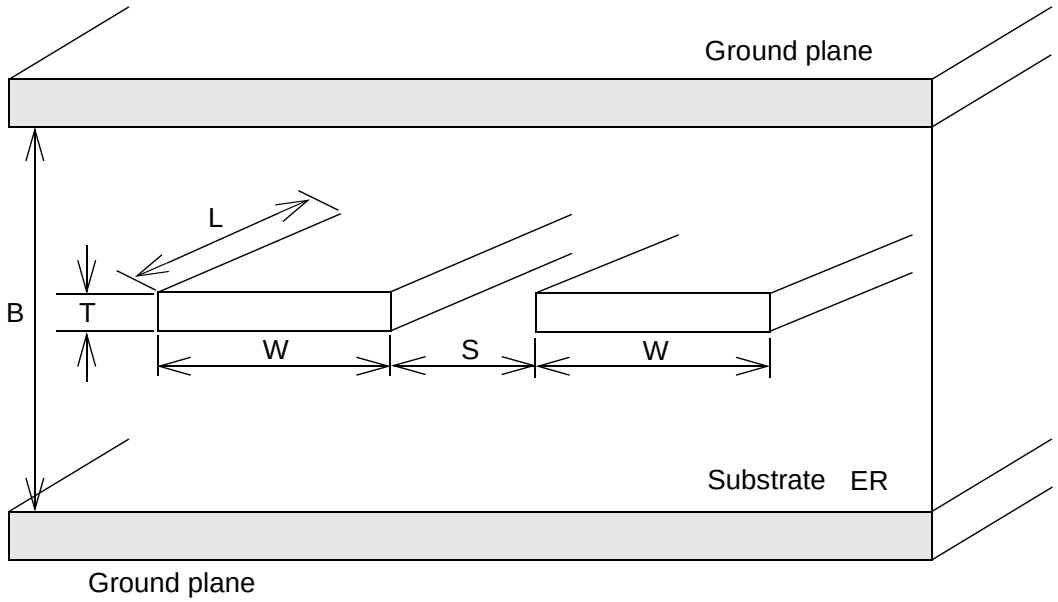
T - Thickness of the conductor

S - Conductor spacing

L - Physical length of the lines

ER - Substrate dielectric constant

SCLIN (Symmetrical Edge-Coupled Striplines)



The input parameters are:

B - Height of the substrate

W - Width of the lines

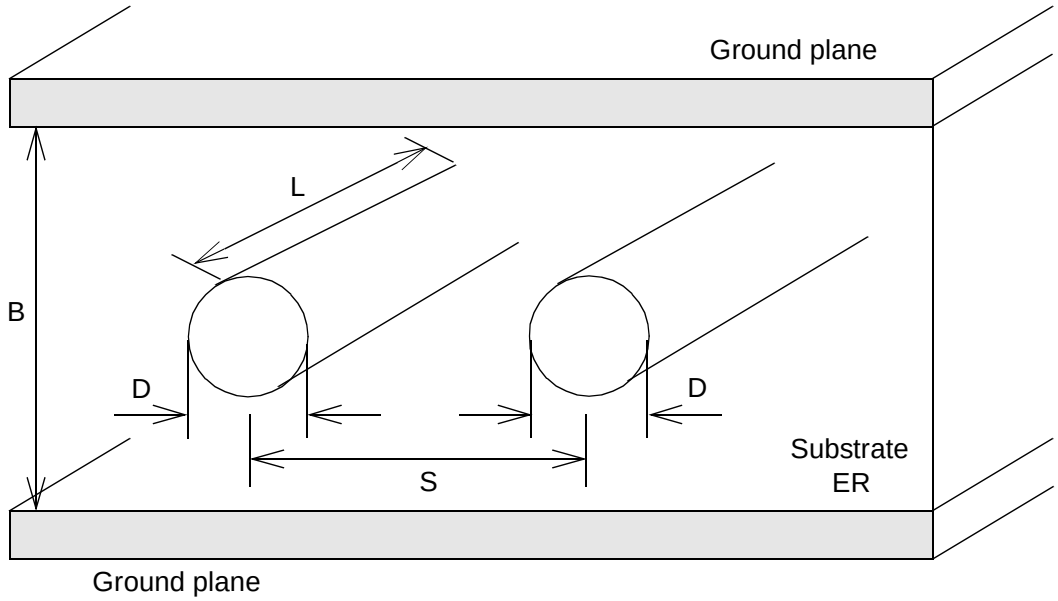
T - Thickness of the conductor

S - Spacing between the lines

L - Physical length of the lines

ER - Substrate dielectric constant

SRCLIN (Symmetrical Edge-Coupled Striplines With Round Conductors)



The input parameters are:

B - Height of the substrate

D - Diameter of the conductors

S - Center-center spacing between the conductors

L - Physical length of the lines

ER - Substrate dielectric constant

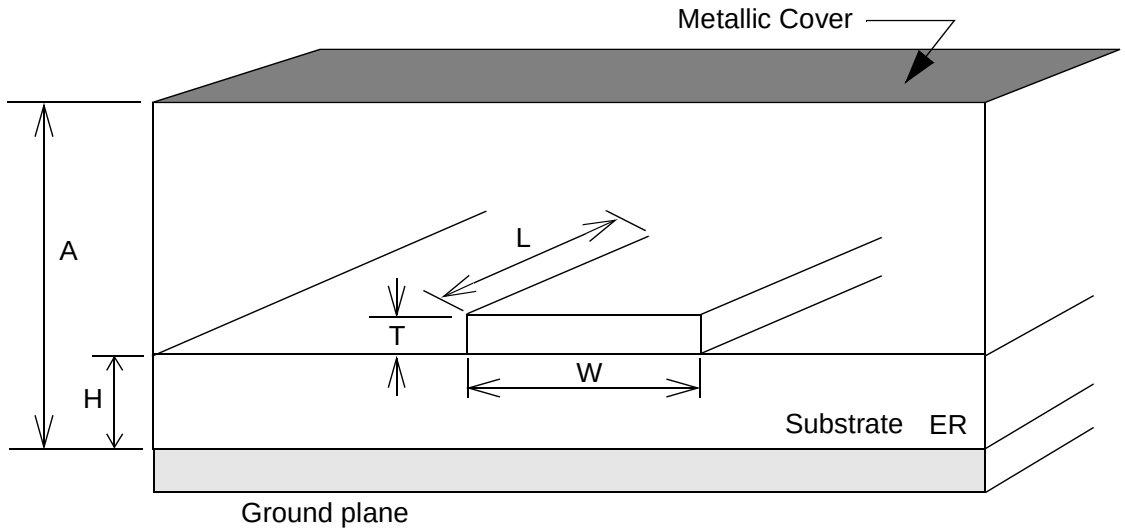
Microstripline Elements

The following stripline elements are represented:

- Transmission Lines
  - MCOVER (Microstripline With Top Metallic Cover)
  - MLEF (Microstripline With Open End Effect)
  - MLIN (Microstrip Lossless Line)
  - MLOC (Ideal Open Circuit Lossless Microstripline)
  - MLOSSLIN (Microstrip Lossy Line)
  - MLSC (Ideal Short Circuit Lossless Microstripline)
  - MRLIN (Lossless Microstrip Line With Round Conductor)
  - SDSLIN (Symmetric Double Strip Lossless Transmission Line)
- Discontinuities
  - MCRBEND (Microstrip With Compensated/Chamfered Right-Angled Bend)
  - MGAP (Microstrip With Series Gap Discontinuity)
  - MRBEND (Microstrip With Right-Angled Bend)
  - MSLIT (Microstrip With Narrow Transverse Slit)
  - MSTEP (Microstrip With Step Change In Width)
  - MVIA (Microstrip With Via Hole Ground)
- Coupled Lines
  - MCLIN (Symmetrical Edge-Coupled Microstriplines)

Transmission Lines

MCOVER (Microstripline With Top Metallic Cover)



The input parameters are:

W - Conductor width

H - Substrate height

T - Conductor thickness

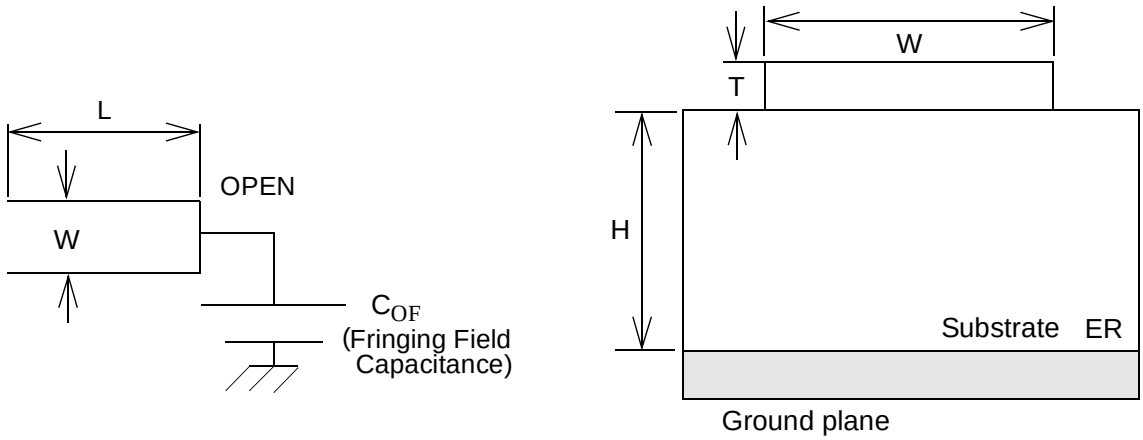
ER - Substrate dielectric constant

A - Distance between the ground plane and the top metallic cover

L - Physical length

F - Frequency at which the dispersion is to be accounted

MLEF (Microstripline With Open End Effect)



The input parameters are:

W - Conductor width

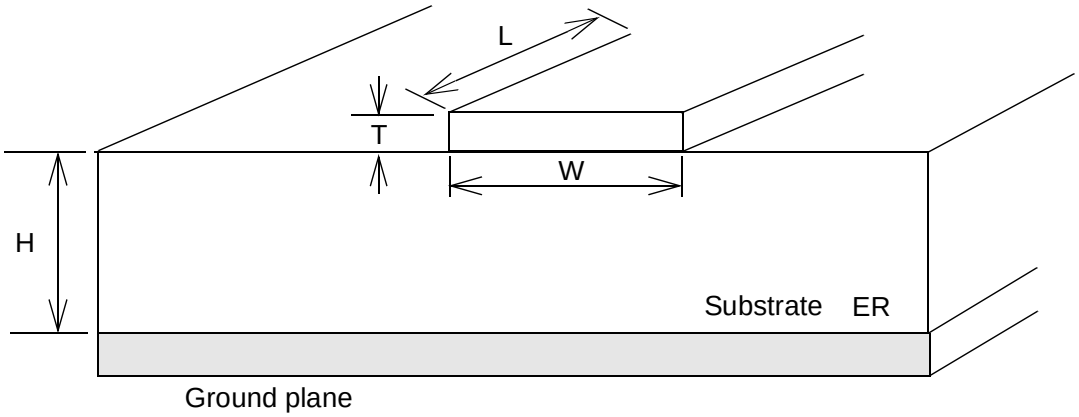
H - Substrate height

ER - Substrate dielectric constant

T - Conductor thickness

L - Physical length

MLIN (Microstrip Lossless Line)



The input parameters are:

W - Conductor width

H - Substrate height

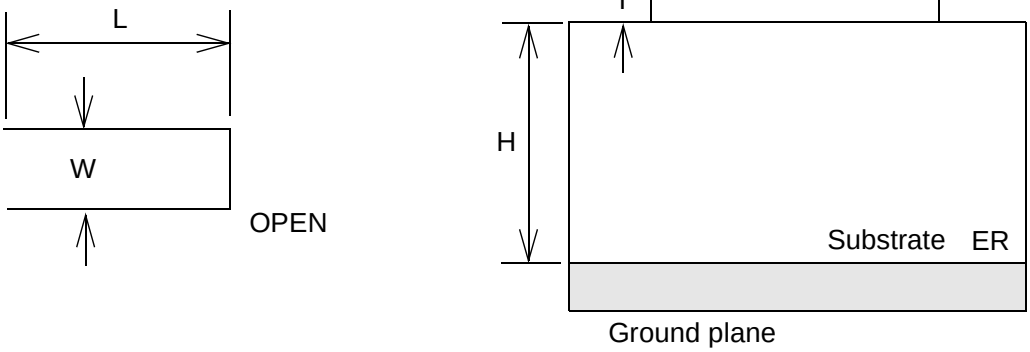
T - Conductor thickness

ER - Substrate dielectric constant

L - Physical length

F - Frequency for which the dispersive effect is to be included

MLOC (Ideal Open Circuit Lossless Microstripline)



The input parameters are:

W - Conductor width

H - Substrate height

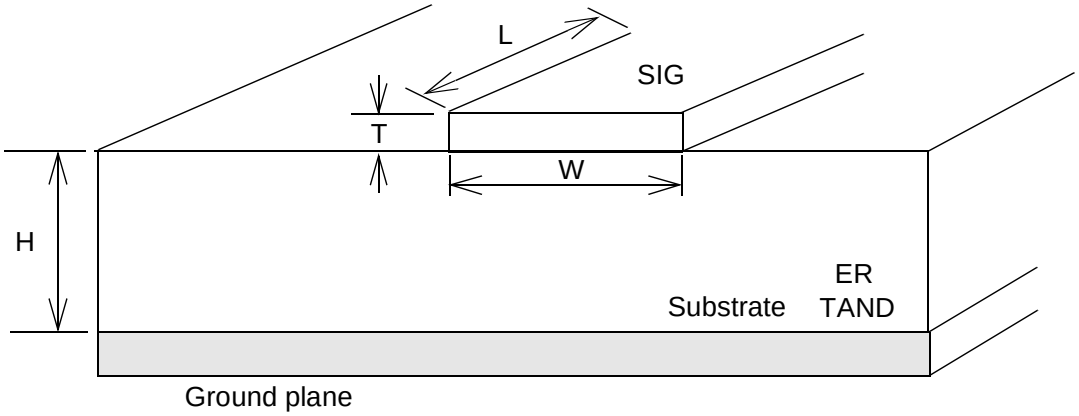
T - Conductor thickness

ER - Substrate dielectric constant

L - Physical length

F - Frequency at which the dispersion is to be accounted

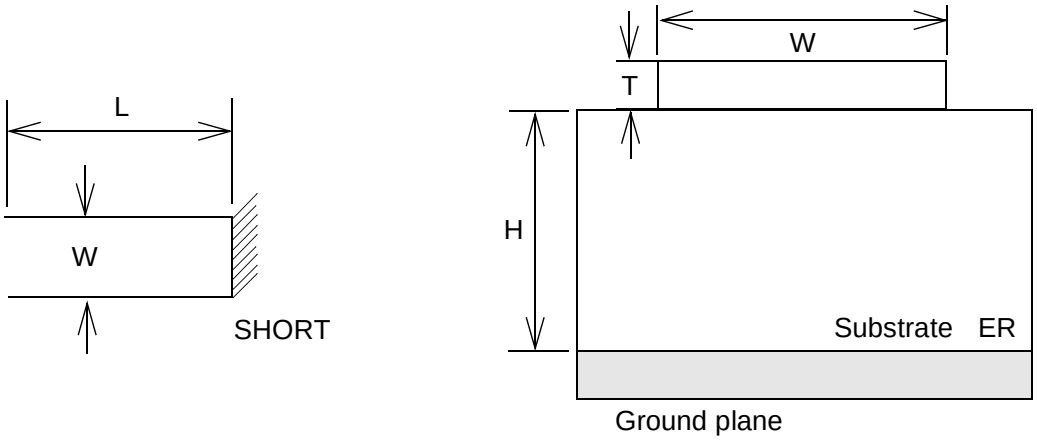
MLOSSLIN (Microstrip Lossy Line)



The input parameters are:

W	-	Conductor width
H	-	Substrate height
T	-	Conductor thickness
ER	-	Substrate dielectric constant
L	-	Physical length of the line
SIG	-	Conductivity
TAND	-	Loss tangent
F	-	Frequency for which the loss and dispersive effects are to be included

MLSC (Ideal Short Circuit Lossless Microstripline)



The input parameters are:

W - Conductor width

H - Substrate height

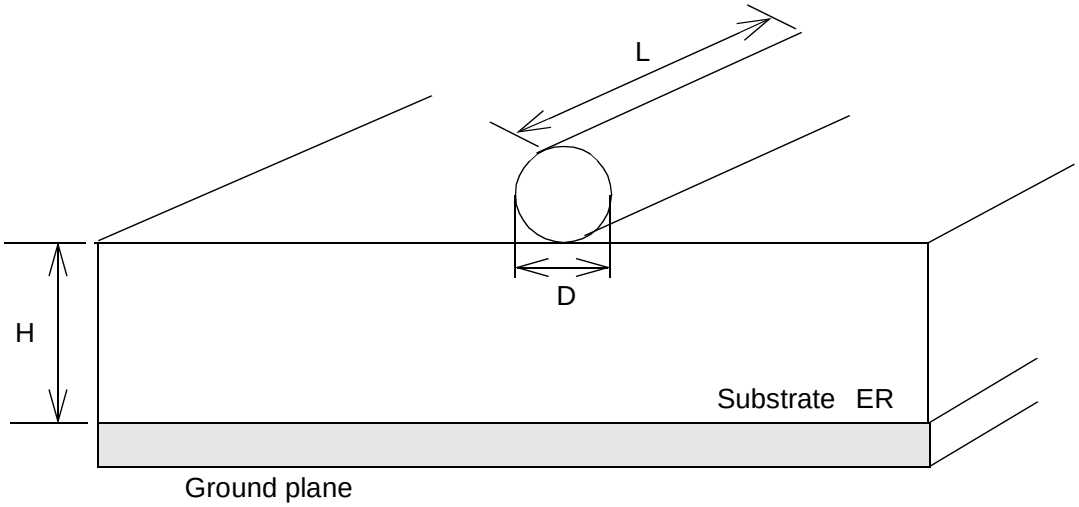
T - Conductor thickness

ER - Substrate dielectric constant

L - Physical length

F - Frequency at which the dispersion is to be accounted

MRLIN (Lossless Microstrip Line With Round Conductor)



The input parameters are:

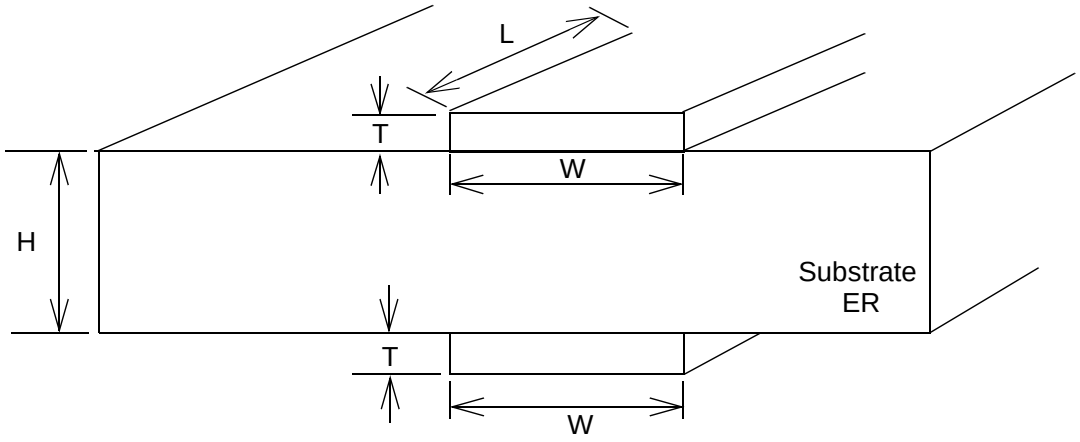
H - Substrate height

ER - Substrate dielectric constant

D - Diameter of the conductor

L - Physical length of the line

SDSLIN (Symmetric Double Strip Lossless Transmission Line)



The input parameters are:

W - Conductor width

H - Substrate height

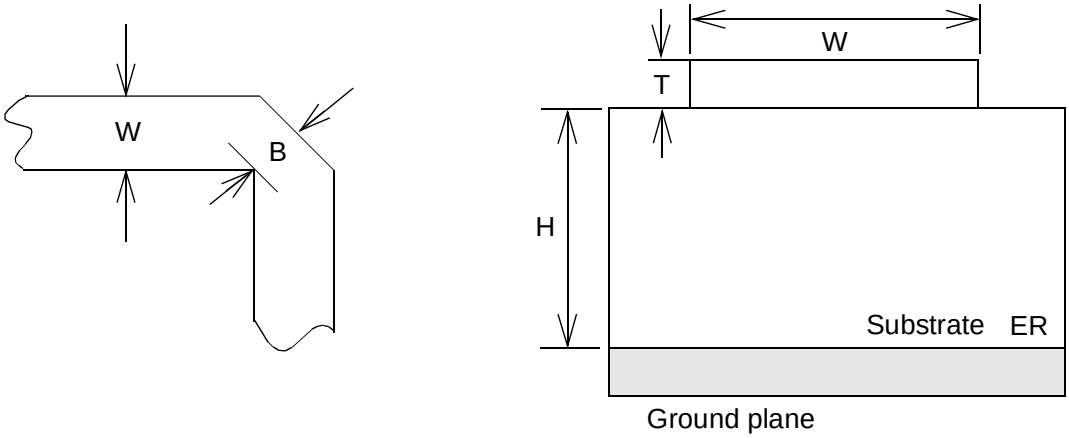
ER - Substrate dielectric constant

T - Conductor thickness

L - Physical length of the line

Discontinuities

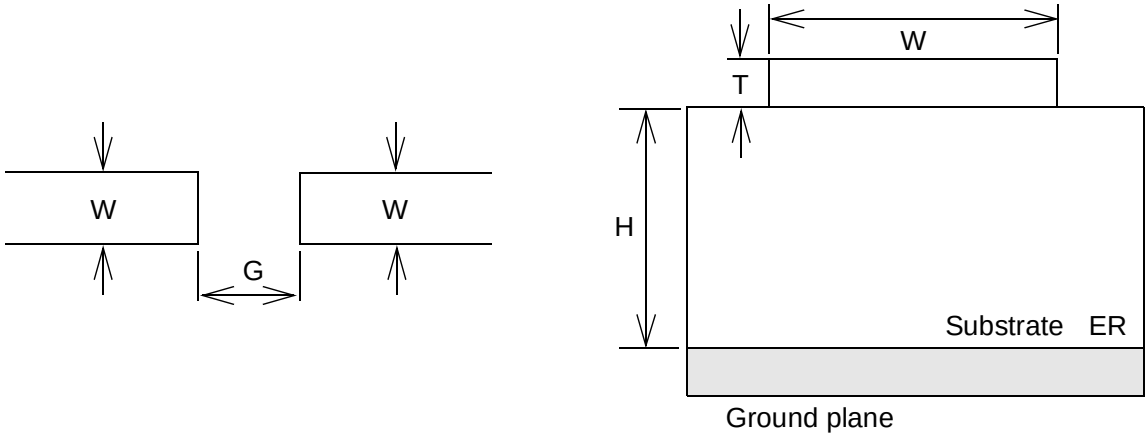
MCRBEND
(Microstrip With Compensated/Chamferred Right-Angled Bend)



The input parameters are:

W	-	Conductor width
T	-	Conductor thickness
H	-	Substrate height
B	-	Width of the strip at the bend
ER	-	Substrate dielectric constant

MGAP (Microstrip With Series Gap Discontinuity)



The input parameters are:

W - Conductor width

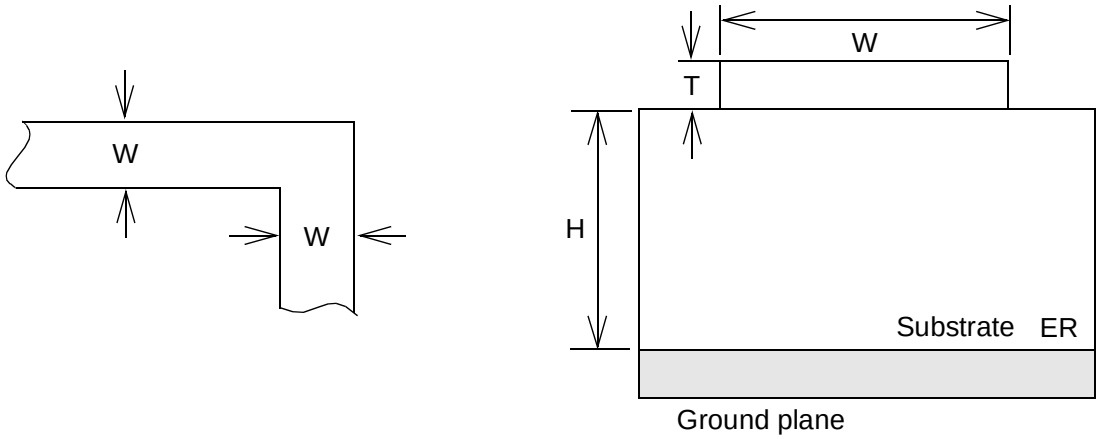
H - Substrate height

ER - Substrate dielectric constant

T - Conductor thickness

G - Distance between the strip edges

MRBEND (Microstrip With Right-Angled Bend)



The input parameters are:

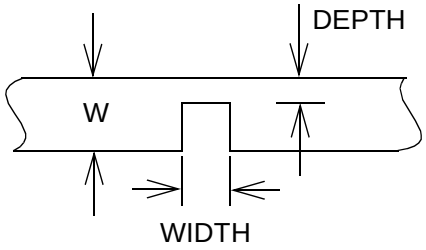
W - Conductor width

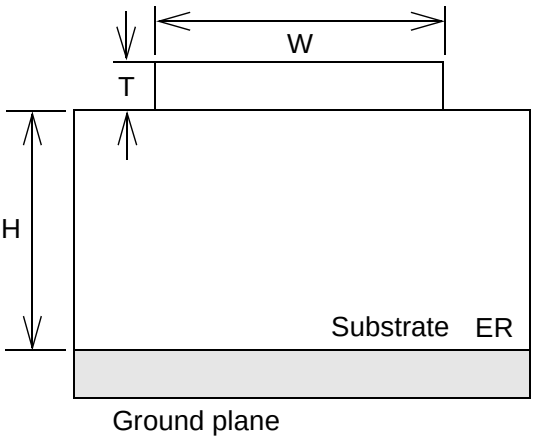
H - Substrate height

ER - Substrate dielectric constant

T - Conductor thickness

MSLIT (Microstrip With Narrow Transverse Slit)

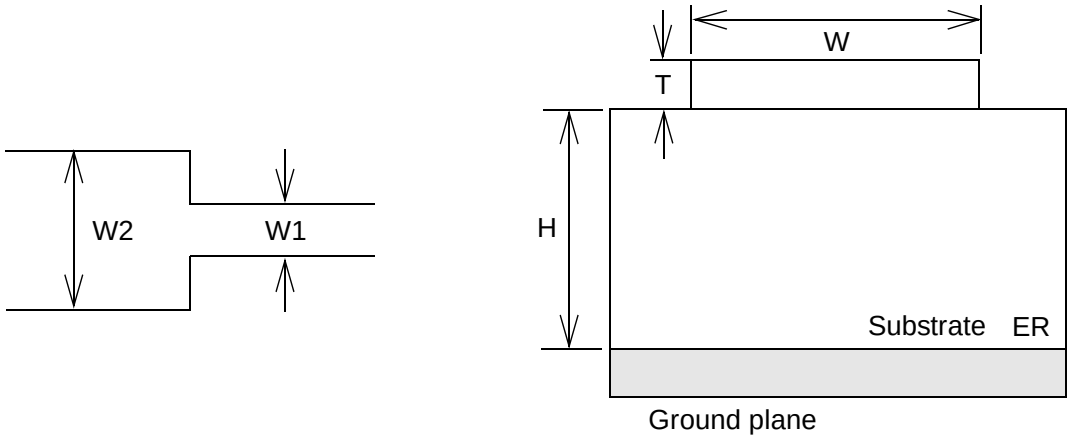




The input parameters are:

W	-	Conductor width
H	-	Substrate height
T	-	Conductor thickness
ER	-	Substrate dielectric constant
WIDTH	-	Width of the slit
DEPTH	-	Depth of the slit

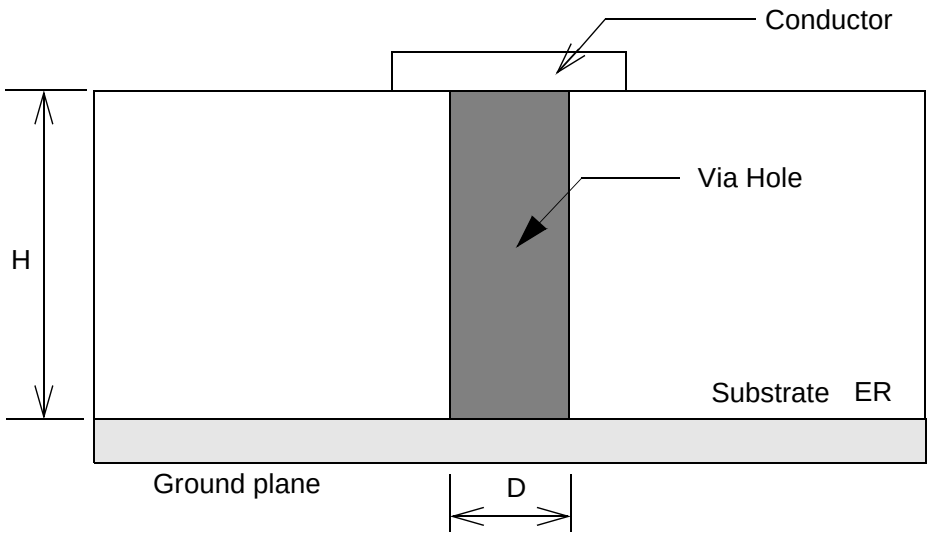
MSTEP (Microstrip With Step Change In Width)



The input parameters are:

W1	-	Width of the conductor (smaller)
W2	-	Width of the conductor (larger)
H	-	Substrate height
ER	-	Substrate dielectric constant
T	-	Conductor thickness

MVIA (Microstrip With Via Hole Ground)



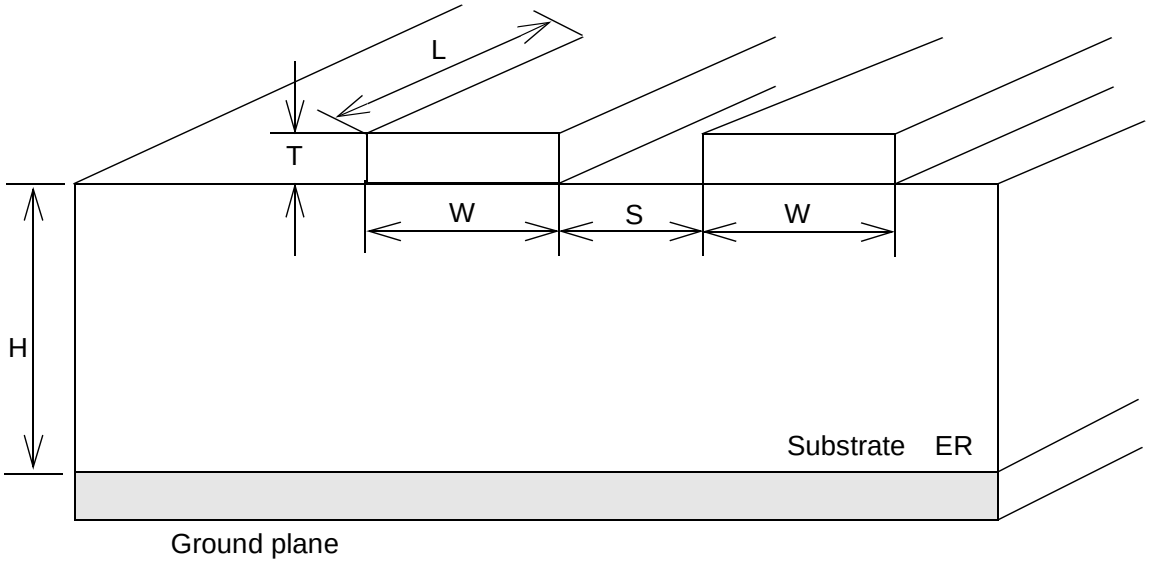
The input parameters are:

H - Substrate height

D - Diameter of the hole

Coupled Lines

MCLIN (Symmetrical Edge-Coupled Microstriplines



The input parameters are:

H - Substrate height

W - Width of the lines

T - Thickness of the line

S - Spacing between the lines

L - Physical length of the line

ER - Substrate dielectric constant

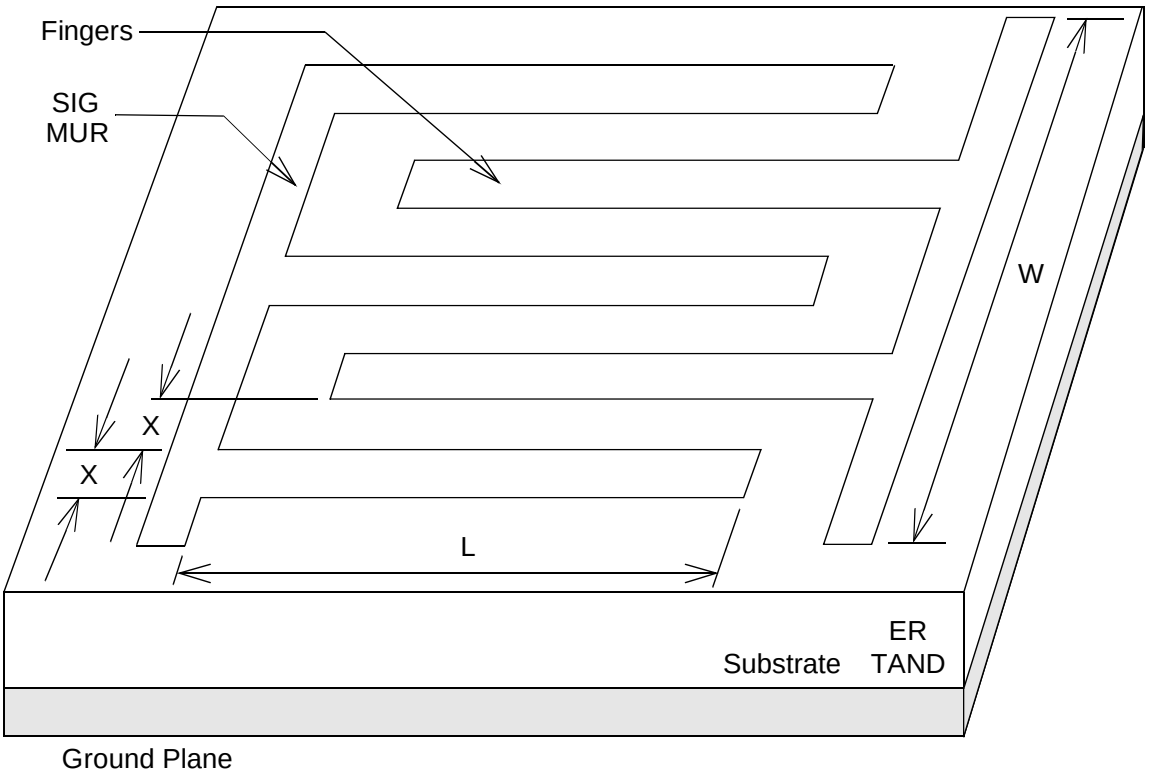
F - Frequency at which the dispersion is to be accounted

Lumped Elements At High Frequencies (Microstrip Configuration)

The following lumped elements are represented:

- MIDCAP (Interdigital Capacitor, Microstrip)
- MLOOP (Single Loop Inductor, Microstrip)
- MRIND (Rectangular/Strip Inductor, Microstrip)
- MRSPIRAL (Spiral (Round Coils) Inductor, Microstrip)
- MSSPIRAL (Spiral (Square Coils) Inductor, Microstrip)
- MWIND (Wire Inductor, Microstrip)
- TFC (Thinfilm/MIM/Overlay Capacitor, Microstrip Configuration)
- TFR (Thinfilm Resistor, Microstrip Configuration)

MIDCAP (Interdigital Capacitor, Microstrip)



The input parameters are:

X	-	Width of the cell
L	-	Length of the cell
N	-	Number of fingers

ER - Substrate dielectric constant

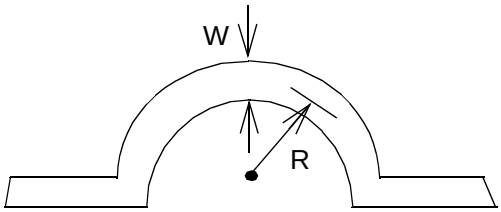
SIG - Conductivity

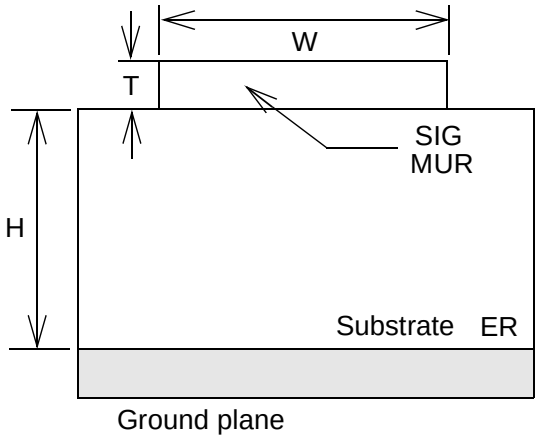
MUR - Relative permeability

TAND - Dielectric loss tangent

F - Frequency at which the model parameters are to be calculated

MLOOP (Single Loop Inductor, Microstrip)





The input parameters are:

W - Conductor width

R - Radius of the loop

T - Conductor thickness

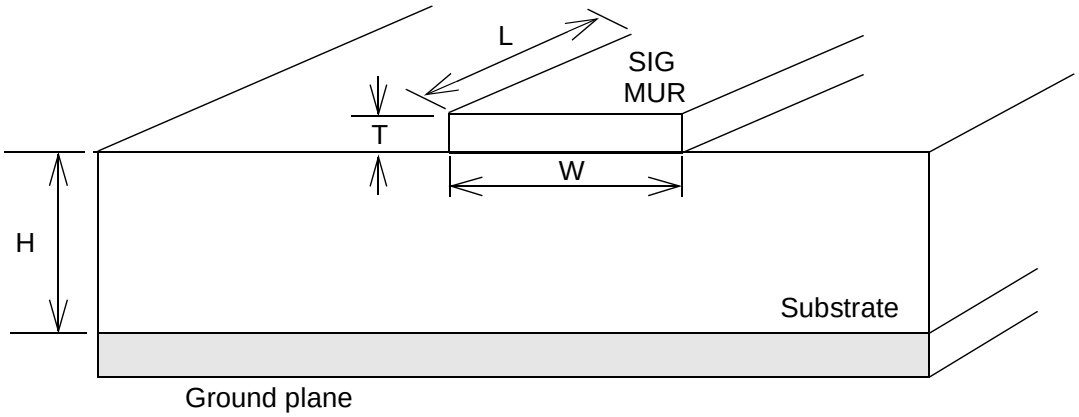
H - Substrate height

SIG - Conductivity

MUR - Relative permeability

F - Frequency at which the model parameters are to be calculated

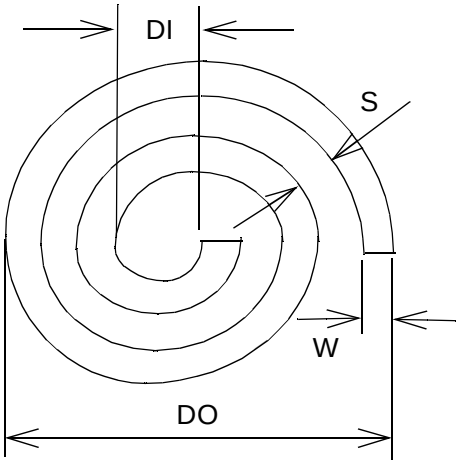
MRIND (Rectangular/Strip Inductor, Microstrip)

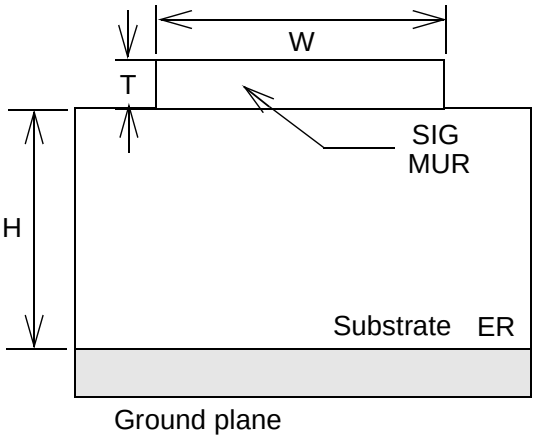


The input parameters are:

W	-	Conductor width
L	-	Physical length
T	-	Conductor thickness
H	-	Substrate height
SIG	-	Conductivity
MUR	-	Relative permeability
F	-	Frequency at which the model parameters are to be calculated

MRSPIRAL(Spiral (Round Coils) Inductor, Microstrip)

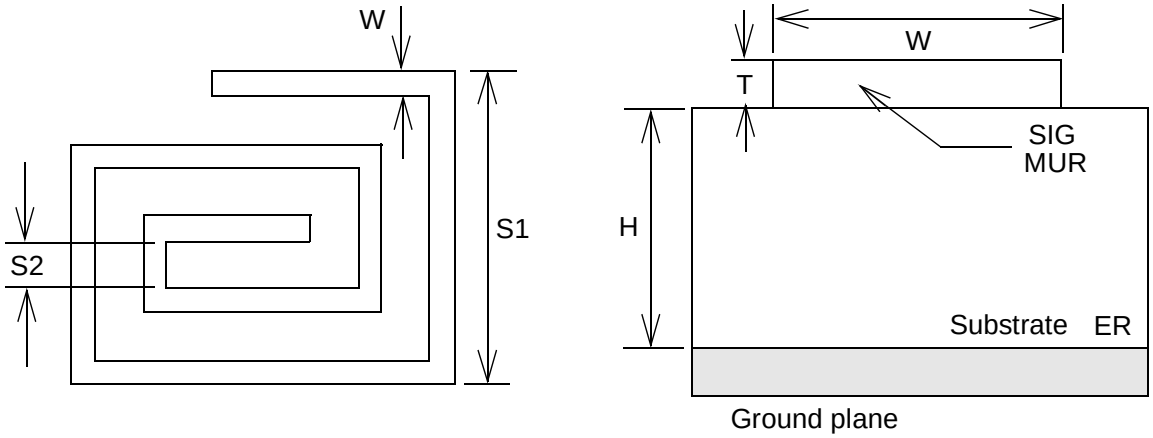




The input parameters are:

W	-	Conductor width
S	-	Spacing between the conductors
T	-	Conductor thickness
DO	-	Outer diameter
DI	-	Inner diameter
H	-	Substrate height
SIG	-	Conductivity
MUR	-	Relative permeability
F	-	Frequency at which the model parameters are to be calculated

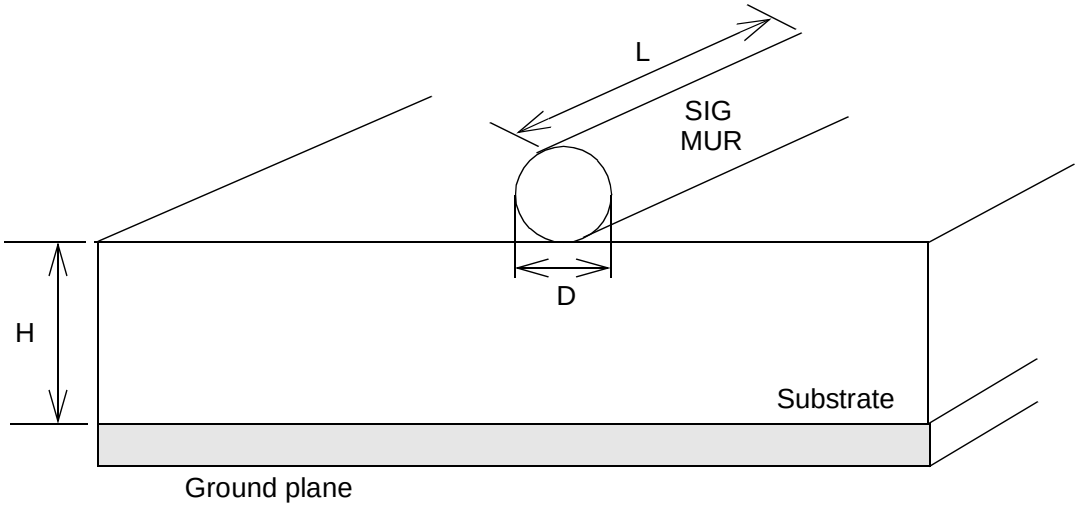
MSSPIRAL (Spiral (Square Coils) Inductor, Microstrip)



The input parameters are:

W	-	Conductor width
T	-	Conductor thickness
S1	-	Maximum outer side length
S2	-	Minimum inner side length
N	-	Number of turns
H	-	Substrate height
SIG	-	Conductivity
MUR	-	Relative permeability
F	-	Frequency at which the model parameters are to be calculated

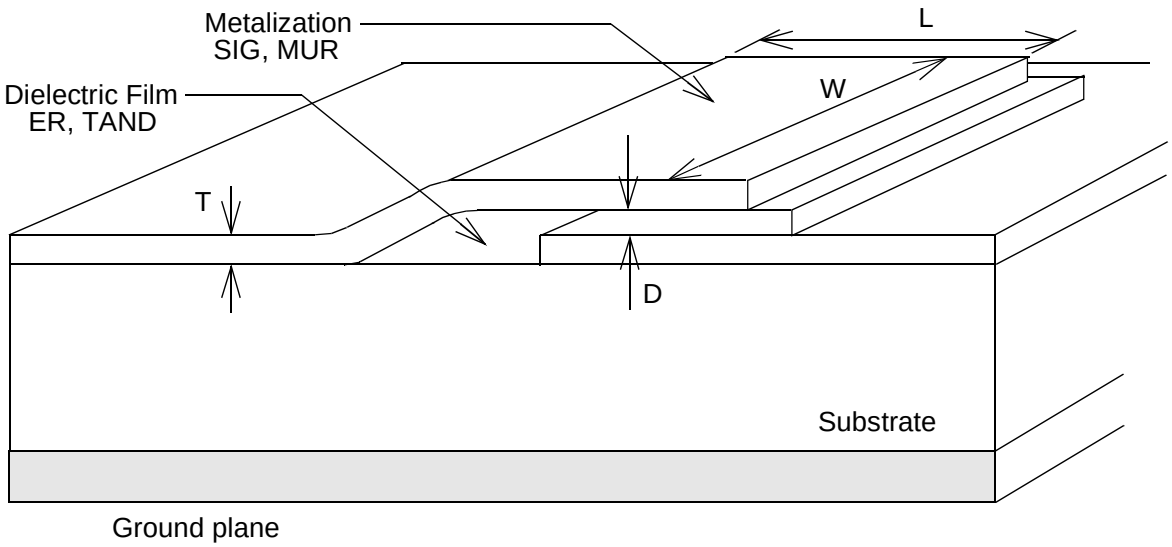
MWIND (Wire Inductor, Microstrip)



The input parameters are:

D	-	Diameter of the conductor
L	-	Length of the conductor
H	-	Substrate height
SIG	-	Conductivity
MUR	-	Relative permeability
F	-	Frequency at which the model parameters are to be calculated

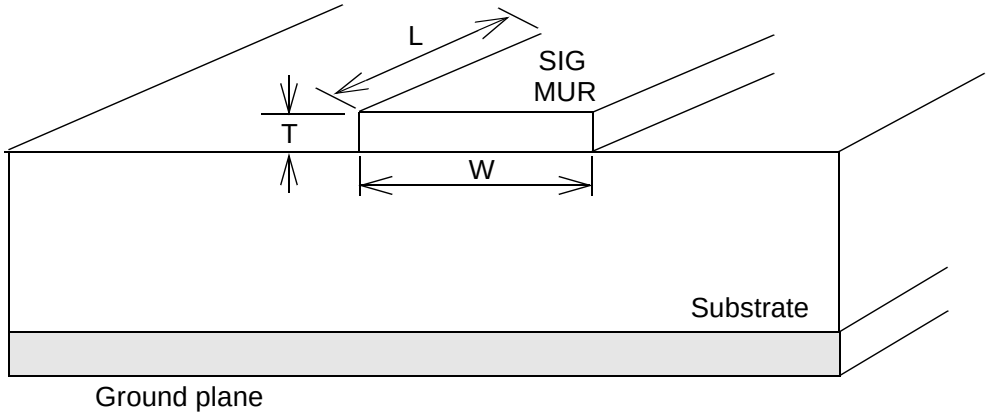
TFC (Thinfilm/MIM/Overlay Capacitor, Microstrip Configuration)



The input parameters are:

W	-	Conductor width
T	-	Conductor thickness
L	-	Length of the conductor
D	-	Height of the substrate layer
ER	-	Substrate dielectric constant
SIG	-	Conductivity
MUR	-	Relative permeability
TAND	-	Dielectric loss tangent
F	-	Frequency at which the model parameters are to be calculated

TFR (Thinfilm Resistor, Microstrip Configuration)



The input parameters are:

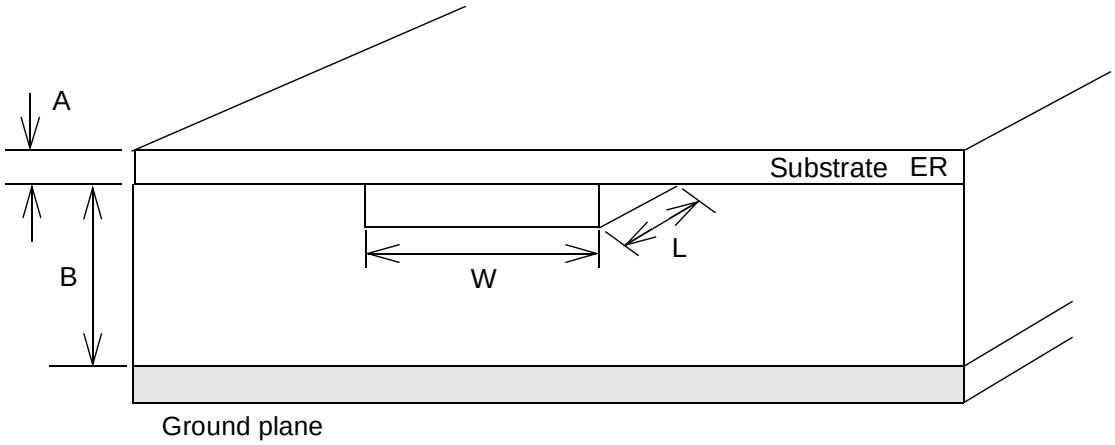
W	-	Width of the conductor film
T	-	Thickness of the film
L	-	Length of the film
SIG	-	Conductivity
MUR	-	Relative permeability
F	-	Frequency at which the surface resistivity is to be calculated

Suspended Substrate Line

The following lumped elements are represented:

- SSIMLIN (Suspended Substrate Lossless Microstripline)
- SSMLIN (Suspended Substrate Inverted Lossless Microstripline)

SSIMLIN (Suspended Substrate Inverted Lossless Microstripline)



The input parameters are:

W - Conductor width

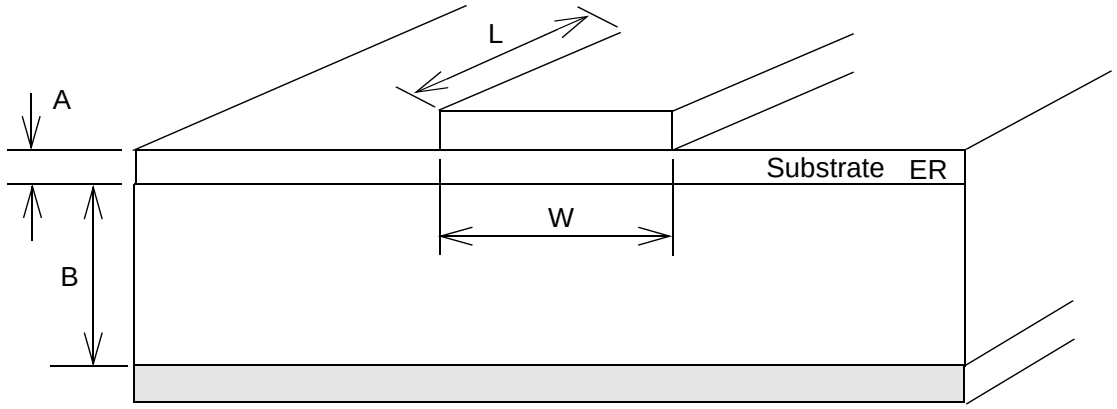
A - Substrate thickness

B - Distance between the ground plane and the lower end of the substrate

L - Physical length of the line

ER - Substrate dielectric constant

SSMLIN (Suspended Substrate Lossless Microstripline)



The input parameters are:

W - Conductor width

A - Substrate thickness

B - Distance between the ground plane and the lower end of the substrate

L - Physical length of the line

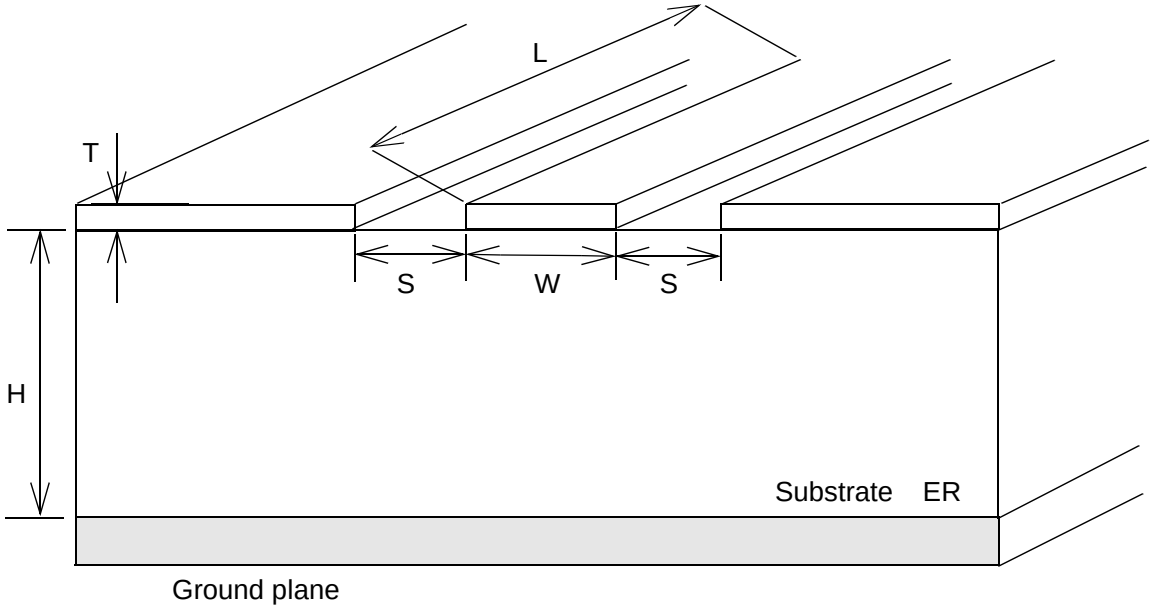
ER - Substrate dielectric constant

Coplanar Guide Transmission Lines

The following coplanar guide transmission lines are represented:

- CPS (Coplanar Strip Lossless Transmission Line)
- CPW (Coplanar Waveguide Lossless Transmission Line)

CPS (Coplanar Strip Lossless Transmission Line)



The input parameters are:

H - Substrate height

W - Conductor width

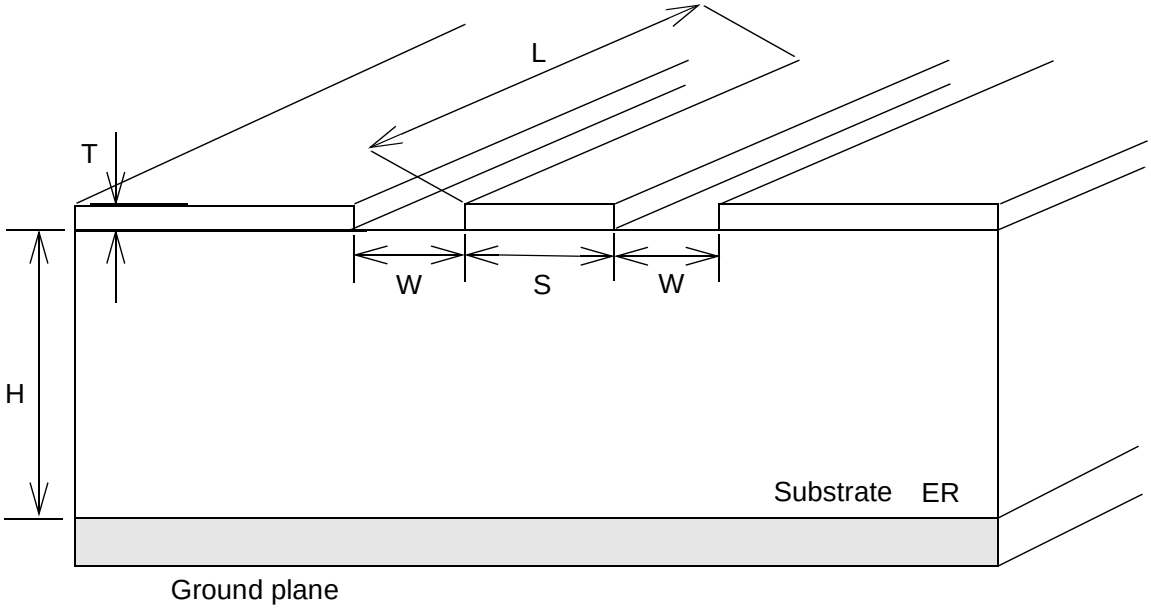
S - Spacing between the conductors

T - Conductor thickness

L - Physical length of the line

ER - Substrate dielectric constant

CPW (Coplanar Waveguide Lossless Transmission Line)



The input parameters are:

H - Substrate height

W - Spacing between the conductors

S - Center conductor width

T - Conductor thickness

L - Physical length of the line

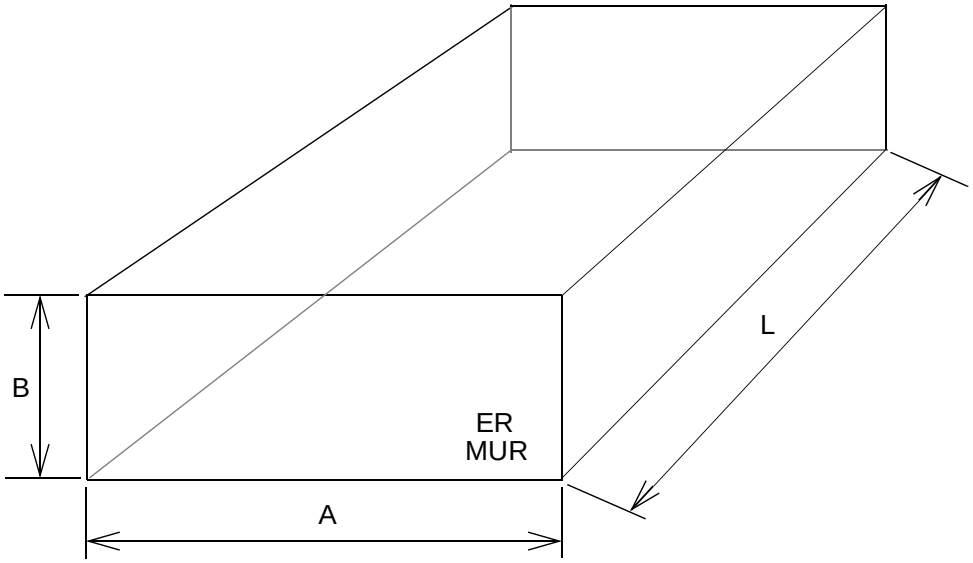
ER - Substrate dielectric constant

Rectangular Waveguide Elements

The following rectangular waveguide elements are represented:

- RWG (Rectangular Waveguide Transmission Line)
- RWGT (Rectangular Waveguide Termination)

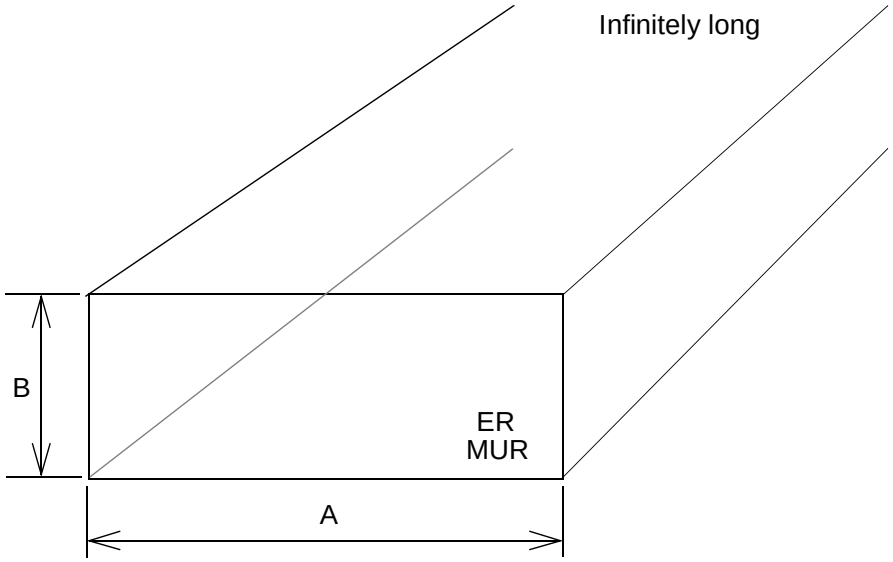
RWG (Rectangular Waveguide Transmission Line)



The input parameters are:

A	-	Waveguide wide dimension
B	-	Waveguide narrow dimension
L	-	Physical length
ER	-	Dielectric constant
MUR	-	Relative permeability
F	-	Frequency of operation

RWGT (Rectangular Waveguide Termination)



The input parameters are:

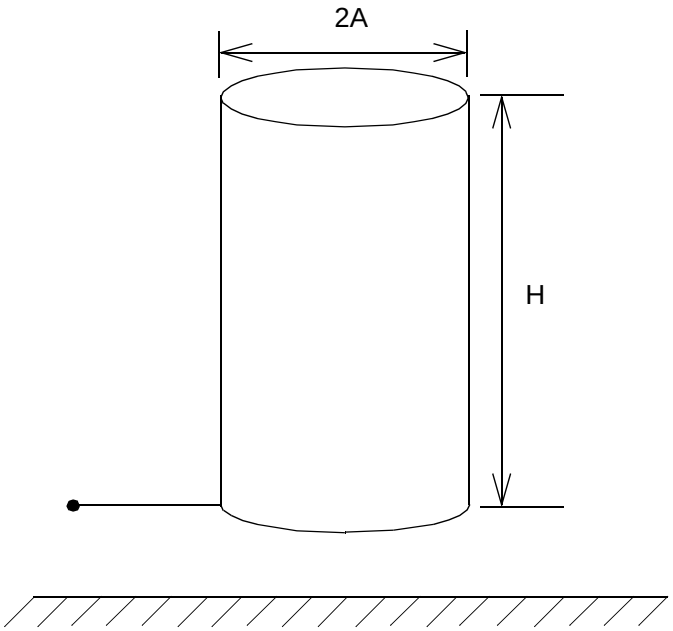
A	-	Waveguide wide dimension
B	-	Waveguide narrow dimension
ER	-	Dielectric constant
MUR	-	Relative permeability
F	-	Frequency of operation

Antenna Input Impedance Elements

The following antenna input impedance elements are represented:

- MONOPOLE (Monopole Input Impedance)
- DIPOLE (Dipole Input Impedance)

MONOPOLE (Monopole Input Impedance)



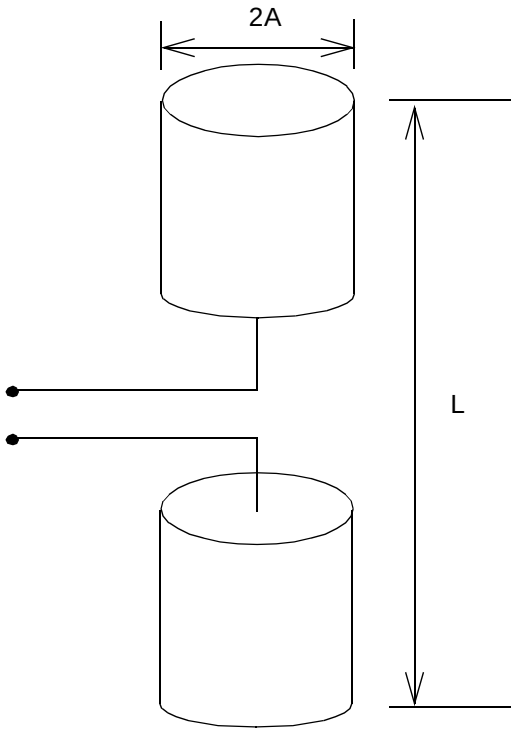
The input parameters are:

H - Height of the monopole

A - Radius of the monopole

F - Frequency of operation

DIPOLE (Dipole Input Impedance)



The input parameters are:

L - Height of the dipole

A - Radius of the dipole

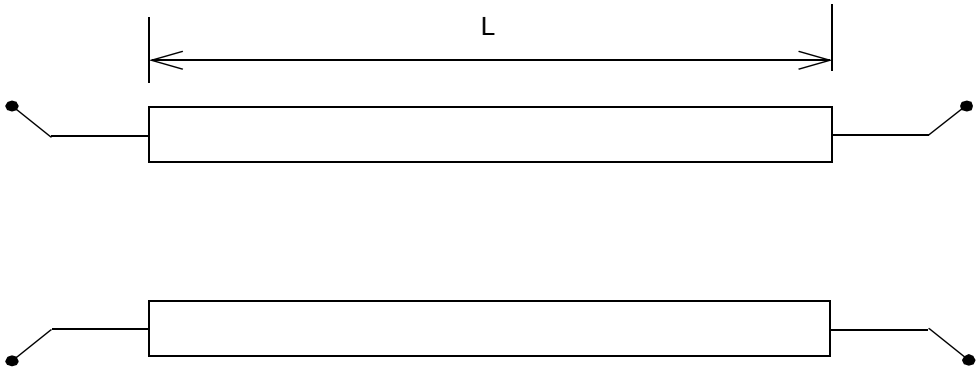
F - Frequency of operation

General Distributed Elements

The following general distributed element is represented:

- CLIN (Coupled TEM/Quasi-TEM Transmission Lines)

CLIN (Coupled TEM/Quasi-TEM Transmission Lines)



ZOE, ZOO, KE, KO

The input parameters are:

ZOE	-	Even-mode impedance
ZOO	-	Odd-mode impedance
KE	-	Even-mode effective dielectric constant
KO	-	Odd-mode effective dielectric constant
L	-	Physical length

Chapter 8
VeriBest Analog Magnetics Model Library

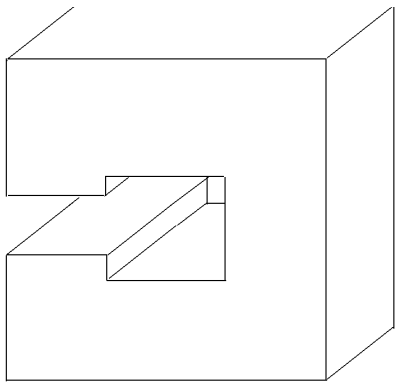
This section describes the transformer models, TRF*n_m*. There are two types of library models in the transformer library: Library core models and simulation models. There are three groups of transformer simulation model parameters: Macromodel, Geometry and Core model. Steps describing how to select a transformer model from the library, assign the geometry parameters, and modify the model's characteristics is included in this section. There are no symbols for core models.

Transformer Models

The transformer model simulates the following physical phenomena:

- Hyperbolic hysteresis (B and H major and minor loop curves)
- Core saturation
- Parasitic capacitance
- Leakage inductance
- Losses due to any of the following factors:
  - Air gaps
  - Fringe field flux
  - Eddy currents
  - Frequency
  - Thermal effects on windings and cores
  - Proximity effects as a fudge factor via the ith winding coefficient of the $K_{i.}$

The transformer model consists of a basic nonlinear magnetic core with losses and inductors whose parameters are expressed in actual physical terms rather than inductance. The transformer simulation model supports only the following transformer configuration:



Supported Core Shape

Graphic Symbol

Graphic symbols for transformers show the number of windings on their respective sides.

Library Reference

A library reference is the name used to call a graphic symbol from the library. Library references for transformer names have the format:

TRF*n_m*

where *n* is the number of windings on the left side of the core, and *m* is the number of windings on the right side.

If you want to switch the number of windings on the left side of the core to the right side of the core and vice versa, mirror the symbol using the Rotate command in VeriBest Design Capture or mirror the symbol when placing it.

For example, to obtain a transformer with two windings on the left side of the core and one winding on the right side, the library reference would be TRF2_1. In VeriBest Design Capture, select the graphic symbol for TRF1_2, and mirror it to create TRF2_1. Terminals with dots have the same voltage sign.

For more information about VeriBest Design Capture commands, see the *VeriBest Design Capture User's Guide*.

Library Part Number (Simulation model property)

The library part number (`Simulation model` property) associates the number of windings with the graphic symbol. The `Simulation model` property is also the name of the subcircuit. Library part numbers for transformers have the format:

TRF*k*

where *k* is the total number of windings. For example, for TR1_2 or TR2_1, the `Simulation model` property is TRF3.

Library Models

There are two types of library models in the transformer library:

- Library core model
- Simulation model

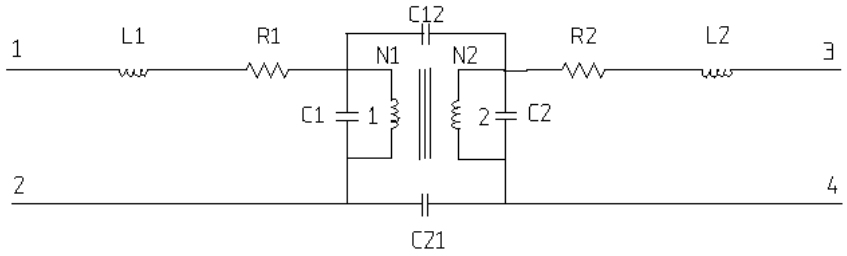
Library Core Model

The library core model associates a magnetic core material model with a transformer. A transformer is associated with a model in the same way that a circuit is associated with a discrete device.

Simulation Model

A transformer simulation model is a subcircuit consisting of the following:

- A nonlinear magnetic core model that simulates the transformer B vs. H hysteresis curve, temperature dependent characteristics, frequency characteristics, and AC loss. The VeriBest Analog Simulation Engine (VBASE) input statement for a core model starts with the letter B.
- A winding model that simulates the winding coupled with the core. The VBASE input statement for the winding model starts with the letter Y.
- R, L, and C components in which R represents wire resistance, L represents leakage inductance, and C represents parasitic capacitance.



The abbreviations used in the illustration above are defined as follows:

- L1 and L2 are leakage inductances
- R1 and R2 are wire resistances
- C1 and C2 are parasitic capacitances
- N1 and N2 are the numbers of turns of windings 1 and 2, respectively
- K1 and K2 are coupling coefficients of windings 1 and 2, respectively
- C12 and C21 are capacitances between windings 1 and 2

Transformer Parameters

There are three groups of transformer simulation model parameters:

- Macromodel parameters
- Geometry parameters
- Core model parameters

Macromodel Parameters

Macromodels have the following parameter definitions and parameter value ranges. These are the parameter definitions for macromodels:

- F is the frequency (same as is specified for the core element.)
- Ni is the number of turns in the ith winding
- Ki is the coupling coefficient of the ith winding
- LIi is the leakage inductance of the ith winding
- RSi is the resistance of the ith winding
- WAi is the wire cross-sectional area of the ith winding
- WDi is the wire diameter (for round wire) of the ith winding
- WPi is the wire perimeter (for rectangular wire) of the ith winding
- CWi is the capacitance of the ith winding
- CXij is the capacitance between the ith and jth windings.
- TC1 and TC2 are the temperature coefficients of winding resistance
- ICi is the initial current of the ith winding

We provide transformer models with up to 12 windings, but only models with up to 6 windings have capacitances between windings CXij built in.

The following table shows default values for macromodel parameters and their ranges. Ni and ICi have the same value for default, minimum, and maximum attributes. This means they can have any value.

Parameter	Default	Minimum	Maximum
F	0 [Hz]	0	
N_i	100		
K_i	1	0.001	1
LI_i	1U [H]	0	1M
RS_i	1M [Ω]	0	10
WAi	0[m^2]	0	
WDi	0[m]	0	
WPi	0[m]	0	
CW_{ij}	1P[F]	0	1N
T_{C1}	0	0	1E–2
TC2	0	0	1E–2
IC_i	0	0	0

These parameters can be modified in VeriBest Analog. Please refer to the *VeriBest Analog User's Guide*.

Skin Effect

An electromagnetic wave is rapidly attenuated in a conducting medium. In a good conductor, such as a copper wire, the attenuation is so rapid at high radio frequencies, the wave penetrates the conductor

only to a small depth. This depth of penetration is called the skin depth. The skin depth varies inversely proportional to the square root of the frequency. This phenomenon is called the skin effect.

The skin depth, δ, is defined as the depth of penetration where the wave decreases to 1/e (approximately 36.8%) of its initial value.

$$\delta = sqrt[2/\omega\mu\sigma]$$

For copper wire,

$$\mu_r \approx 1$$

$$\sigma = 5.8e7\ mho/m$$

Therefore

$$\delta = 6.61e-2/sqrt[F]$$

Skin effect reduces the conducting area to an annular region in the wire. Since wire resistance is inversely proportional to the wire's cross-sectional area, the effective AC resistance is increased by the skin effect. The AC and DC resistances (R_{ac}, R_{dc}) can be related to the AC and DC wire areas (A_{ac}, A_{dc}) as follows:

$R_{ac} / R_{dc} = A_{dc} / A_{ac}$

Where

R_{dc} and A_{dc} are specified in the wire databook

$A_{ac} = \pi\delta(WD - \delta)$ *for cylindrical wire*

WD = wire diameter

$A_{ac} = \delta(WP - 4\delta)$ *for rectangular wire*

WP = wire perimeter

Only WA, WD and WP need to be specified for each winding (*copper wire is assumed*) since the resistance is also specified uniquely. If WD is give, the winding is assumed to be made of cylindrical wire. Therefore,

if (WD > 0) then

$A_{ac} = \pi\delta WD - \delta)$

$elseA_{ac} = (WP - 4\delta)$

endif

if ((F > 0) and (WA > 0) and (WD > 0 or WP > 0) and (WA > A_{ac})) then

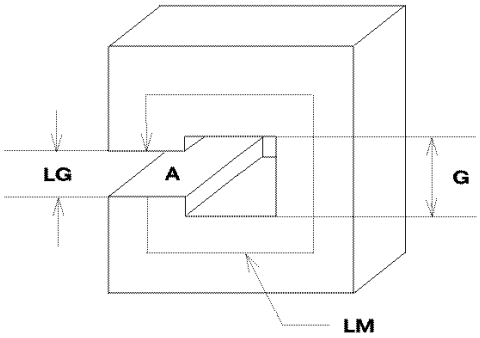
$R_{ac} = R_{dc}$ (WA / A_{ac})

else

$R_{ac} = R_{dc}$

endif

Geometry Parameters



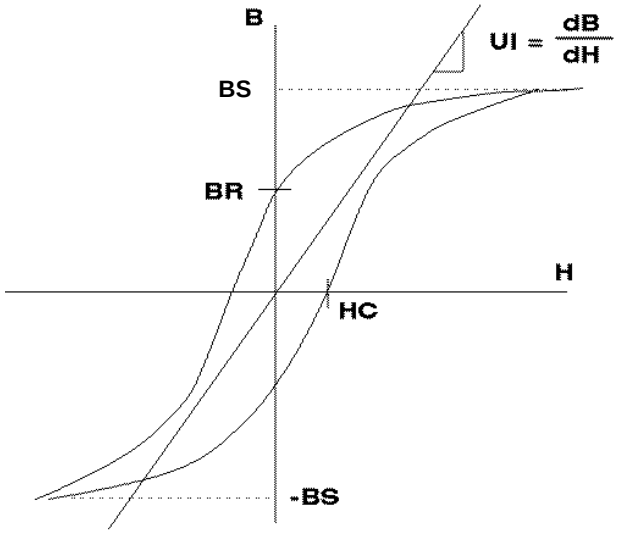
Definitions of the geometry parameters of a typical core are as follows:

LM	Mean length of the core's magnetic path [m]
LG	Air gap length [m]
A	Cross section area of the core [m^2]
G	shoulder width [m]
B	Initial flux density [T]
F	Operating frequency used to calculate core loss [Hz]

These parameters can be added or modified in VeriBest Design Capture through the Property Place or Property Modify command.

Core Model Parameters

This is the data for the B vs. H hysteresis curve:



B vs H hysteresis curves

Parameter definitions for core models are as follows:

BS	Saturation flux density [T]
BR	Residue flux density [T]
HC	Coercive force [A/m]
UI	Initial permeability

The following equations are implemented in VBASE for core model parameters:

$$LM' = \frac{U1 \times LG + LM}{Fac}[m]$$

where

$$Fac = 1 + \frac{LG}{\sqrt{A}} \ln\frac{2G}{LG}$$

$$H = \frac{\Sigma Ni \ Ii}{LM} \qquad [A/m]$$

$$B = f(H)\left[T\right]$$

$$\frac{db}{dh} = f(H, B)$$

The core model temperature coefficients are defined as follows:

TBS	Temperature coefficient of BS
TBR	Temperature coefficient of BR
THC	Temperature coefficient of HC
TUI	Temperature coefficient of UI

The following equations are implemented in VBASE for core model temperature coefficients:

BS(T1) = BS(T0) ∗ [1 + TBS ∗ (T1 - T0)]

BR(T1) = BR(T0) ∗ [1 + TBR ∗ (T1-T0)]

HC(T1) = HC(T0) ∗ [1 + THC ∗ (T1 - T0)]

UI(T1) = UI(T0) ∗ [1 + TUI ∗ (T1 - T0)]

Parameters for frequency dependence core loss are FC1, FC2, and FC3. This equation is implemented in VBASE using the parameters for frequency dependence core loss:

$HC = HC * (FC1 + FC2 * f^{FC3})$

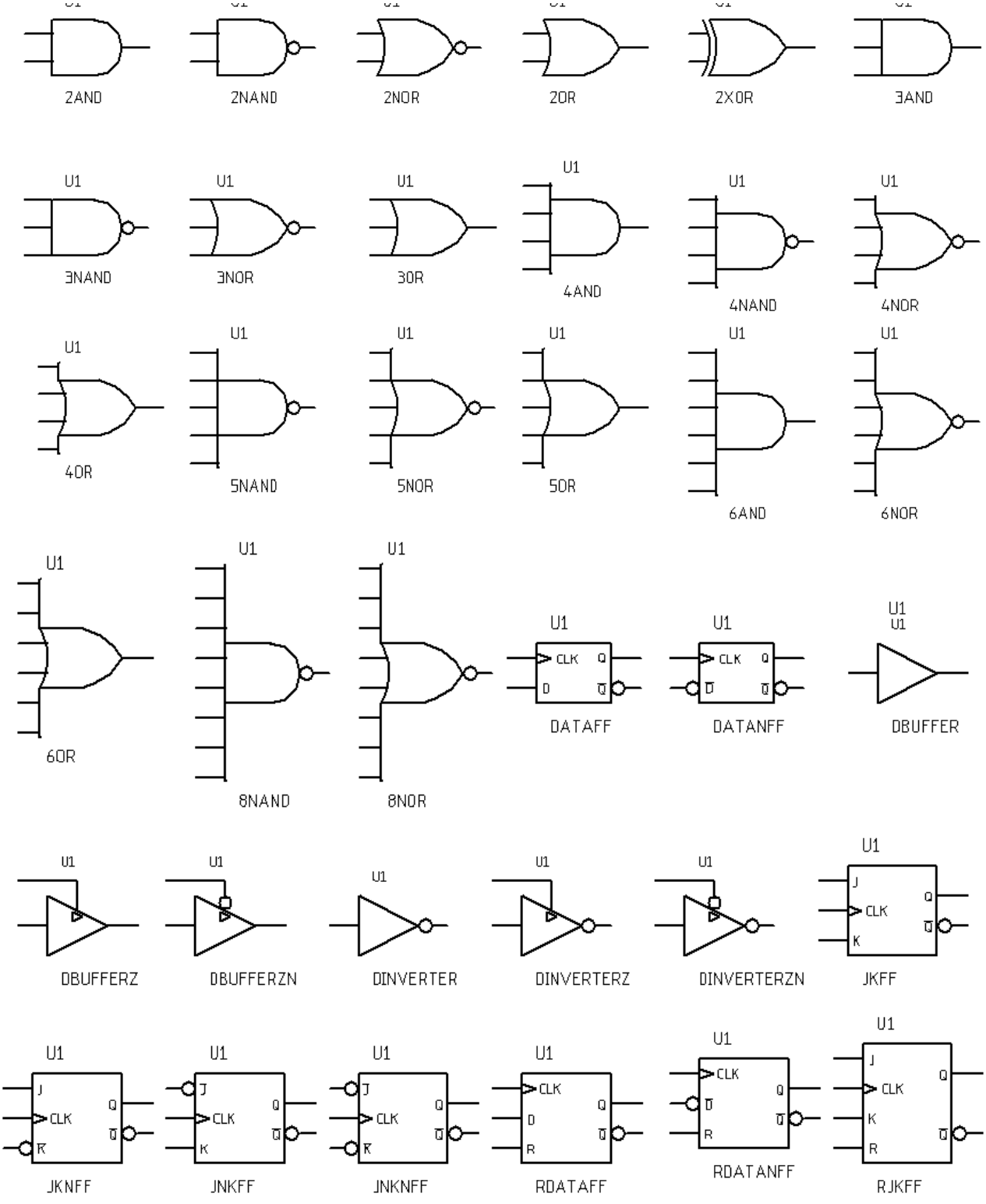
AC relative loss coefficients include DEL1, DEL1P, DEL2, and DEL2P. The following equation uses these AC relative loss coefficients:

$$\frac{\tan(DELTA)}{UI} = DEL1 \times f^{DEL1P} + DEL2 \times f^{DEL2P}$$

The table below shows default values for the core model parameters.

Parameter	Description	Default Value
BS	Saturation flux density	0.2 [T]
BR	Residue flux density	0.1[T]
HC	Coercive force	20 [A/m]
UI	Initial permeability	5E3
TBS	Temperature coefficient of BS	5E-3
TBR	Temperature coefficient of BR	0.00
THC	Temperature coefficient of HC	0.00
TUI	Temperature coefficient of UI	0.00
FC1	Parameter for frequency dependence core loss	1.00
FC2	Parameter for frequency dependence core loss	0.05
FC3	Parameter for frequency dependence core loss	0.20
DEL	AC relative loss coefficient	12E–6
DEL1P	AC relative loss coefficient	0.50
DEL2	AC relative loss coefficient	2E–7
DEL2P	AC relative loss coefficient	0.20

These parameters can be modified in VeriBest Analog. Please refer to the *VeriBest Analog User's Guide*.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2NOR
2OR
2XOR
3AND
U1
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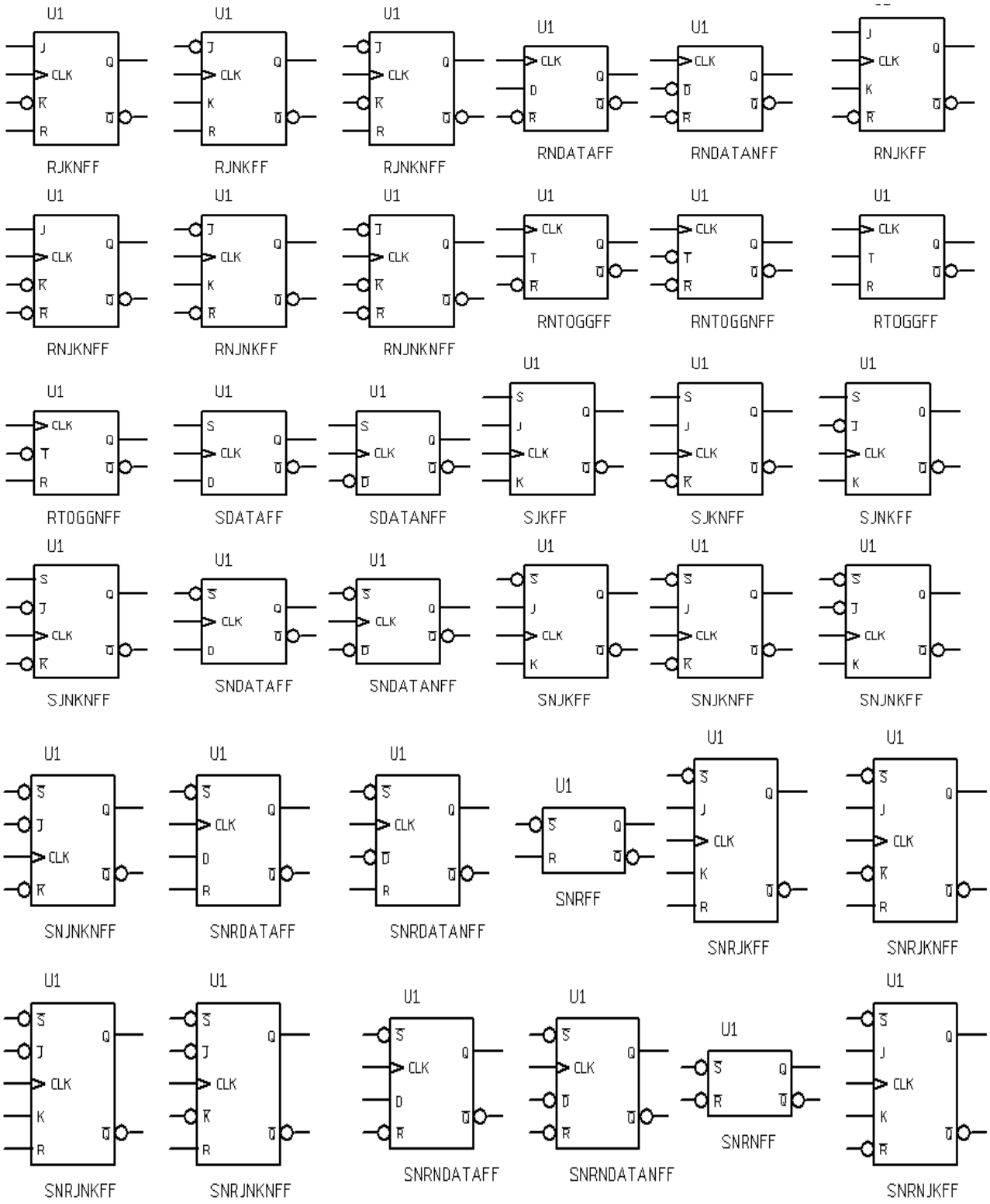
3NOR
3OR
4AND
4NAND
4NOR
4OR
5NAND
5NOR
5OR
6AND
6NOR
6OR
8NAND
8NOR
CLK
D
Q
DATAFF
DATANFF
DBUFFER
DBUFFERZ
DBUFFERZN
DINVERTER
DINVERTERZ
DINVERTERZN
J
K
JKFF
JKNFF
JNKFF
JNKNFF
R
RDATAFF
RDATANFF
RJKFF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RJNKNFF
RNDATAFF
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RNTOGGNFF
RTOGGFF
RTOGGNFF
SDATAFF
SDATANFF
SJKFF
SJKNFF
SJNKFF
SJNKNFF
SNDATAFF
SNDATANFF
SNJKFF
SNJKNFF
SNJNKFF
SNJNKNFF
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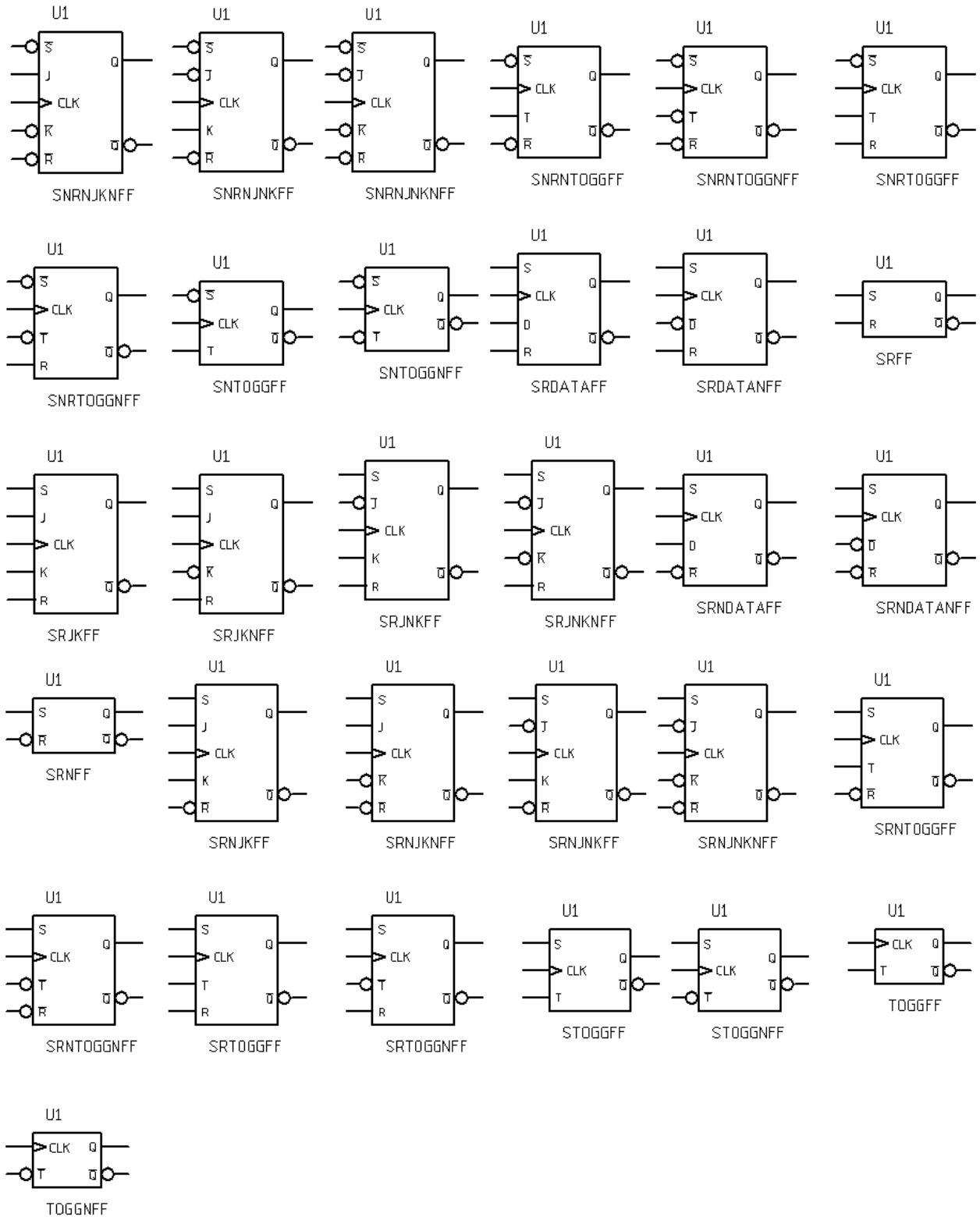
U1
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U1
SNRNJNKFF
U1
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U1
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SNRTOGGFF
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SNRTOGGNFF
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SNTOGGFF
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SRNTOGGNFF
U1
SRTOGGFF
U1
SRTOGGNFF
U1
STOGGFF
U1
STOGGNFF
U1
TOGGFF
U1
TOGGNFF

The Mixed-Signal models, the generic models take into consideration only twelve parameters which meet the functional characteristics for the model. These parameters include the following:

- EVENTFLAG
- ICSTATE
- ICHOLD
- VOH
- VOL
- VIH
- VIL
- tPHL
- tPLH
- tr
- tf
- clkenable

Where:

EVENTFLAG - allows you to turn on recording of events for selected parts if it is set to 1. The events are shown in the data file.

- EVENTFLAG_Q - for Q output of FF models
- EVENTFLAG_QBAR - for QBAR output of FF models

ICSTATE - first guess for the output state

- ICSTATE_Q - for Q output of FF models
- ICSTATE_QBAR - for QBAR output of FF models

ICHOLD - Output state is held at the ICSTATE value during DC operating point calculations if ICHOLD is set to 1.

- ICHOLD_Q - for Q output of FF models.
- ICHOLD_QBAR - for QBAR output of FF models

VOH - voltage level at the output which establishes LOGIC 1

VOL - voltage level at the output which establishes LOGIC 0

VIH - low-to-high bit transition level

VIL - high-to-low bit transition level. Actual transition level is calculated to be the average of VIH and VIL.

tPHL - high-to-low transition propagation delay

tPLH - low-to-high transition propagation delay

tr - rise time. The time from the initial voltage to 63% (RC time constant) of the difference between the initial and final voltages.

tf - fall time. The time from the initial voltage to 37% (RC time constant) of the difference between the initial and final voltages.

clkenable - type of clocking used in flip-flops

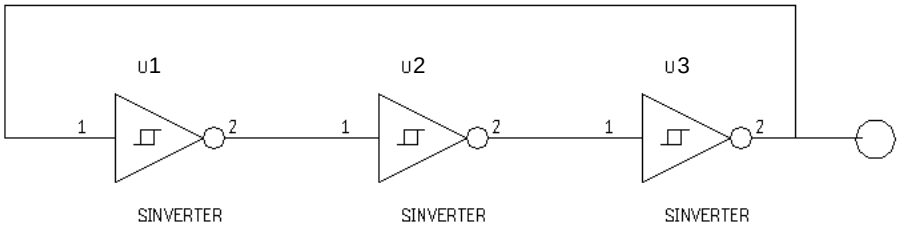
- 0 = no clock
- 1 = positive phase
- 2 = negative phase
- 3 = rising edge
- 4 = falling edge

The parameters ICSTATE and ICHOLD are used for setting initial conditions. They are normally used in starting oscillator circuits and circuits exhibiting tight Feedback. The ten remaining parameters determine the voltage and timing characteristics. The last parameter, *clkenable*, is only applicable to flip-flops. These parameters can be edited inside the VeriBest Analog Simulation Engine (VBASE). For more information see the *VeriBest Analog User's Guide*.

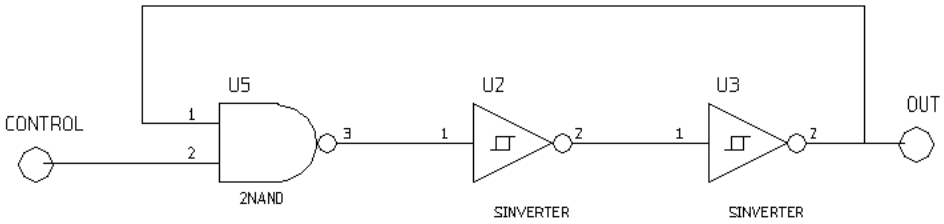
Simulating

Depending on the complexity of the model, simulation times may be longer for some models and shorter for others. The functional models found in the logic function list are the fastest models that can be run on the simulator. Full models may take longer due to their complexity, while Mixed-Signal models are somewhat faster since they are reduced.

When simulating oscillators or mixed-mode Feedback circuits, an initial operating point should be set. The recommended method, if possible, is to disable the oscillation or feedback path so that an initial operating point can be calculated. For example, include a gate in the feedback which uses a control signal to enable or disable the oscillator.



Using the classic ring oscillator, the configuration becomes:



When control is low, the oscillator is disabled. This is because the output of the nand is high, independent of the signal feeding back. After the operating point has been found, the oscillation or feedback can be enabled during transient analysis. Control would most likely be set up as a PWL or PULSE source, whose value would be low at t = 0, and would change to high at some time t > 0. You must also remember to put in some delays in each gate. If an initial operating point is not set, the simulator may take a long time before it converges to a solution.

Another technique would be to use the original three-inverter configuration, but to set the initial operating point using the ICSTATE and ICHOLD parameters. Setting ICSTATE to 0 or 1 serves as a first guess for the output state. Setting ICHOLD to 1 holds the output state (specified in ICSTATE) as its value during DC operating point calculations. Again, some delay times should be given to each stage. For more information on, see the *VeriBest Analog User's Guide*.

Chapter 10
VeriBest Analog MOSFET Model Library

On the following pages, MOSFET model parameters are defined, MOSFET model equations are shown and computation of MOSFET parasitics are described.

Model Parameters

- An asterisk (*) indicates that the model parameters are affected by scalm.
- A number sign (#) tells you to see the Usage Notes at the end of this section.

Setup

Name	Parameter	Units	Default
LEVEL	MOSFET ids equation selector	—	1
BULK	Bulk node assignment	—	—
TLEV	ASPEC style temperature compensation choice	—	0.0
NUMDERIV	Use numerical derivatives instead of analytical derivatives for the MOSFET model (See .OPTION ABS-DELTA and .OPTION RELDELTA)	—	0.0

Geometry

Name	Parameter	Units	Default
LD	Lateral diffusion	m	0.0
LMLT	Length multiplier	—	1.0
DL (or XL)	Correction added to the L on the device card (except for BSIMs where it is subtracted)	m	0.0
WD	Lateral diffusion into channel from bulk along width	m	0.0

Name	Parameter	Units	Default
WMLT	Width multiplier	—	1.0
DEL	Channel length reduction on each side. DEL is not applicable to BSIM (LEVEL=4) $L_{eff} = L_{drawn} * LMLT + DL - 2 * (LD + DEL)$	m	0.0
DW (or XW)	Correction added to the W on the device card (except for BSIMs where it is subtracted)	m	0.0
LDIF	Length of lightly doped diffusion	m	0.0
HDIF	Length of heavily doped diffusion	m	0.0
ACM	ASPEC compatibility Mode	—	1(level 6) 0(othewise)

Stress Analysis

Name	Parameter	Units	Default
PMAX	Maximum power dissipation	W	—

Overlap Capacitances

Name	Parameter	Units	Default
CGBO	Gate-bulk overlap capacitance per meter channel length. It is computed if not specified.	F/m	—
CGDO*	Gate-drain overlap capacitance per meter channel width. It is computed if not specified.	F/m	—
CGSO*	Gate-source overlap capacitance per meter channel width. It is computed if not specified.	F/m	—
FRINGE*	Fringing field factor for G-S and G-D overlap capacitance calculation	m	0.0

Junction Capacitance (bottom)

Name	Parameter	Units	Default
CBS	Zero bias bulk-source junction capacitance	F	0.0
CBD	Zero bias bulk-drain junction capacitance	F	0.0
CJ*	Zero bias bulk junction bottom capacitance. For ACM=1, units are F/m.	F/m^2	0.0
MJ	Bulk junction bottom grading coefficient	—	0.5
	Diode bottom wall junction potential	V	0.8
FC	Forward-bias non-ideal junction capacitance coefficient	—	0.5
CTA	Temperature coefficient	1/deg	0.0
MJSW	Bulk junction sidewall grading coefficient	—	0.33
PBSW	Diode sidewall junction potential	V	PB
CTP	Temperature coefficient	1/deg	0.0

Junction Capacitance (Sidewall)

Name	Parameter	Units	Default
CJSW*	Zero bias junction sidewall capacitance per meter of junction perimeter	F/m	0.0

Leakage Current (Bottom)

Name	Parameter	Units	Default
IS	Bulk junction saturation current	A	1.0E–14
JS*	Bulk junction saturation current per unit area For ACM=1, units are A/m.	A/m^2	0.0

Leakage Current (Sidewall)

Name	Parameter	Units	Default
ISSW	Sidewall junction saturation current	A	0.0
JSSW*	Sidewall junction saturation current per meter of junction perimeter	A/m	0.0

Parasitic Resistances

Name	Parameter	Units	Default
RSH	Drain and source diffusion sheet resistance	Ω/sq	0.0
RS	Source ohmic resistance	Ω	0.0
RD	Drain ohmic resistance	Ω	0.0
TRS	Temperature coefficient for drain and source diffusion resistance	1/deg	0.0
TRSH	Temperature coefficient for resistor	1/deg	0.0
TRD	Temperature coefficient for drain resistor	1/deg	0.0

Channel Capacitance

Name	Parameter	Units	Default
COX	Gate oxide capacitance	F/m^2	0.0
XQC	If .OPTION SPICE is not specified:	—	
	For the Ward-Dutton charge model (QOPT=2)	—	0.5
	For the BSIM charge model (QOPT=3)	—	0.0
	For all other charge models	—	1.0
	When the MOSFET model level is not equal to 4 (for example, when any MOSFET model other than BSIM is used), and when the BSIM charge model (QOPT=3) is used, then:		

Name	Parameter	Units	Default
	–XPC > 0.0 selects a 40/60 partition for drain/source charges in saturation. –XPC = 0.0 selects a 0/100 partition		
	If .OPTION SPICE is specified, XQC is used to determine the charge model. QOPT has no effect –XQC ≤ 0.5 selects the Ward-Dutton charge model –XQC > 0.5 selects the Meyer charge model for drain/source charges in saturation	—	1.0
QOPT	Charge model selection 0 - Yang-Chatterjee 1 - Meyer 2 - Ward-Dutton 3 - BSIM charge model 4 - ASPEC charge model 5 - Zero charge model This parameter is ignored with .OPTION SPICE and with .OPTION QOPT=n	—	0.0

QOPT=4 Parameters

Name	Parameter	Units	Default
CF1	Transition from depletion to weak inversion	V	0.0
CF2	Transition from weak to strong inversion	V	0.1
CF3	Transition from saturation to linear	—	1.0
XCG	Capacitance multiplier	—	0.667

Threshold Voltage

Name	Parameter	Units	Default
VTO	Zero bias threshold voltage	V	0.0
NSS	Surface state density	$1/cm^2$	0.0
TPG	Type of gate material +1 opposite to substrate -1 same as substrate 0 aluminum gate	—	1.0
PHI	Surface potential for strong inversion. (For LEVEL=6, PHI=Fermi potential)	V	0.6
GAMMA	Bulk threshold parameter	$\sqrt{V}$	0.0
NSUB	Substrate doping	$1/cm^3$	0.0
TCV	Temperature coefficient	V/deg	0.0

Mobility

Name	Parameter	Units	Default
KP	Transconductance parameter	A / V^2	2.0E–5
UO	Surface mobility	cm^2/ V-sec	600 (N-chl) 400 (P-chl)
BEX	Temperature exponent for KP	—	–1.5

Level 1

Name	Parameter	Units	Default
LAMBDA	Channel-length modulation	1/ V	0.0
TOX	Gate oxide thickness	m	0.0

Level 2

Name	Parameter	Units	Default
LAMBDA	Channel-length modulation	1/V	0.0
DELTA	Width effect on threshold voltage	—	0.0
VMAX	Maximum drift velocity of carriers	m/sec	0.0
NEFF	Total channel charge coefficient	—	1.0
XJ*	Metallurgical junction depth	m	0.0
UCRIT	Critical field for mobility degradation	V/cm	1.0E4
UEXP	Critical field exponent in mobility degradation	—	0.0
UTRA	Transverse field coefficient	—	0.0
TOX	Gate oxide thickness	m	1.0E–7

Level 3

Name	Parameter	Units	Default
ETA	Static feedback	—	0.0
DELTA	Width effect on threshold voltage	—	0.0
KAPPA	Saturation field factor	—	1.0
THETA	Mobility reduction	1/ V	0.0
TOX	Gate oxide thickness	m	1.0E–7
XJ*	Metallurgical junction depth	m	0.0
VMAX	Maximum drift velocity of carriers	m/sec	0.0
NFS	Fast surface state density	$1/cm^2$	0.0

Level 4

Name	Parameter	Units	Default
VFB#	Flat-band voltage	V	0.0
PHI#	Surface inversion potential	V	0.6
K1#	Body effect coefficient	$\sqrt{V}$	0.0
K2#	Drain/source depletion charge sharing coefficient	—	0.0
ETA#	Zero bias drain-induced barrier lowering coefficient	—	0.0
MUZ	Zero bias mobility	cm^2/ V-sec	600
DL#	Shortening of channel	m	0.0
DW #	Narrowing of channel	m	0.0
U0#	Zero bias transverse field mobility degradation coefficient	1/ V	0.0
U1#	Zero bias velocity saturation coefficient	m / V	0.0
X2MZ#	Sensitivity of mobility to substrate bias at Vds=0	cm^2/ V^2-sec	0.0
X2E#	Sensitivity of drain-induced barrier lowering effect to substrate bias	1/V	0.0
X3E#	Sensitivity of drain-induced barrier lowering effect to drain bias at Vds = Vdd	1/V	0.0
X2U0#	Sensitivity of transverse field	1/ V^2	0.0
X2U1#	Sensitivity of velocity saturation effect to substrate bias	m / V^2	0.0
MUS#	Mobility at zero substrate bias at Vds = Vdd	cm^2/ V-sec	0.0
X2MS#	Sensitivity of mobility to substrate bias at Vds = Vdd	cm^2/ V^2-sec	0.0
X3MS#	Sensitivity of mobility to drain bias at Vds = Vdd	cm^2/ V^2-sec	0.0
X3U1#	Sensitivity of velocity saturation effect on drain bias at Vds=Vdd	m / V^2	0.0

Name	Parameter	Units	Default
TOX	Gate oxide thickness	m	1.0E–7
VDD	Measurement bias range	V	0.0
XPART	Gate-oxide capacitance charge model flag XPART=0 selects a 40/60 drain source charge partition in saturation, while XPART = 1 selects a 0/100 drain/source charge partition. XPART = 1 is recommended.	—	1.0
N0#	Zero bias subthreshold slope coefficient	—	0.0
NB#	Sensitivity of subthreshold slope to substrate bias	—	0.0
ND#	Sensitivity of subthreshold slope to drain bias	—	0.0

Level 6

Name	Parameter	Units	Default
DNS	Doping for LGAMMA computation	$1/cm^3$	0.0
LGAMMA	Multilevel threshold parameter. If LGAMMA is not specified, then LGAMMA is computed from DNS. When VBO is specified, then GAMMA is used if reverse bias on the bulk is less than VBO, and LGAMMA is used for larger reverse bias.	$\sqrt{V}$	0.0
GAMMA*	Junction depth, if VBO is not specified	m	0.0
VBO	Critical voltage for gamma switch	V	0.0
NWM	Narrow width modulation of gamma	—	0.0
SCM	Short channel modulation of gamma	1/ V	0.0
VSH	Threshold voltage shift due to channel length	V	0.0
VFDS	Critical voltage for selection of FDS or UFDS. FDS is used if VDS < VFDS	V	0.0
FDS	Field drain to source controls reduction of threshold due to source-drain electric field	—	0.0

Name	Parameter	Units	Default
UFDS	High field FDS	—	0.0
NWE*	Narrow width effect on threshold voltage	—	0.0
KU	Velocity saturation switch. Alternate saturation model is used if KU > 1.	—	0.0
NU	Switch for mobility reduction due to lateral field. Mobility reduction is modeled if NU = 1.	—	1.0
KA	Short channel VDS scaling factor	—	1.0
MAL	Short channel exponent for VDS scaling factor	—	0.5
MBL	Short channel exponent for mobility reduction	—	1.0
NFS	Fast surface state density	$1/cm^2$	0.0
VMAX	Maximum drift field velocity of carriers. Also determines calculation scheme for saturation voltage. Use zero to indicate an infinite value.	cm/sec	0.0
TOX	Gate oxide thickness	Å	690
ECRIT	Critical lateral electric field	V/cm	0.0
MOB	Mobility equation selector	—	0.0
CLM	Channel length modulation equation	—	0.0
WIC	Weak inversion equation selector	—	0.0
WEX	Weak inversion equation exponent or WIC=2	—	0.0

MOB=1 Parameters

Name	Parameter	Units	Default
F1	Gate field mobility reduction	1/ V	0.1
UTRA	Lateral field mobility reduction factor	1/ V	0.0

MOB=2 Parameters

Name	Parameter	Units	Default
F1	Critical vertical field at which mobility reduction becomes significant	V/cm	0.0
UEXP	Mobility exponent	—	0.0
UTRA	Lateral field mobility reduction factor	1/ V	0.0

MOB=3 Parameters

Name	Parameter	Units	Default
F1	Low-field mobility multiplier	1/ V	0.0
UEXP	Mobility exponent	—	0.0
UTRA	High-field mobility multiplier	1/ V	0.0
F4	Mobility summing constant	—	1.0
VF1	Critical voltage for low to high field multiplier switch	V	0.0

MOB=4 and MOB=5 Parameters

Name	Parameter	Units	Default
F1	Critical field for mobility reduction	V/cm	0.0
F2	Bulk mobility reduction factor	$1/ V^2$	0.0
F3	Critical lateral field for mobility reduction (MOB=5)	V/cm	0.0
ECRIT	Critical lateral field for mobility reduction (MOB=4)	V/cm	0.0

CLM=1 Parameters

Name	Parameter	Units	Default
LAMBDA	Channel length modulation factor. If not specified, it is computed.	$\frac{cm}{\sqrt{V}}$	0.0
KL	Empirical exponent	—	0.0

CLM=2 Parameters

Name	Parameter	Units	Default
A1	First fringing field factor	—	0.2
A2	Second fringing field factor	—	0.6

CLM=3 Parameters

Name	Parameter	Units	Default
LAMBDA	Channel length modulation factor. If not specified, it is computed.	$\frac{cm}{\sqrt{V}}$	0.0
KCL	Exponent for substrate bias scaling factor	—	0.0
MCL	Short channel exponent	—	1.0

CLM=4 Parameters

Name	Parameter	Units	Default
A1*	Junction depth	m	0.0
DND	Drain diffusion concentration	$1/cm^3$	1.0E20
KL	Grading coefficient exponent	—	0.333

Level 8

Name	Parameter	Units	Default
CAV	Thermal voltage multiplier for weak inversion equation	—	0.0
DELTA	Width effect on threshold voltage	—	0.0
ECRIT	Critical electric field for carrier velocity saturation. Typical values are 6000 for electrons and 24000 for holes. Use zero to indicate an infinite value.	V/cm	0.0
LAM1	Channel length modulation correction	1/m	0.0
LAMBDA	Channel length modulation factor	—	0.0
SNVB	Slope of doping concentration versus vbs	$1/\ V\text{-}cm^3$	0.0
UCRIT	Critical voltage for mobility degradation, if UEXP > 0.0	V/cm	0.0
UCRIT	Critical voltage for mobility degradation, if UEXP ≤ 0.0	1/ V	0.0
UEXP	Critical field exponent for mobility degradation	—	0.0
UTRA	Transverse field coefficient for mobility degradation	1/ V	0.0
TOX	Gate oxide thickness	m	1.0E–7

Level 11

Name	Parameter	Units	Default
XJ*	Metallurgical junction depth	m	0.0
VTO#	Zero bias threshold voltage	V	0.0
GAMMA#	Bulk threshold parameter	$\sqrt{V}$	0.0
GAMMA2#	Threshold voltage dependence on bulk bias	—	0.0
ETA#	Threshold voltage dependence on drain bias	1/ V	0.0

Name	Parameter	Units	Default
UO#	Surface mobility	cm^2/ V-sec	600
BETAO#	Zero field conductance coefficient. (computed from UO, if not specified.)	A / V^2	—
THETA1#	Mobility reduction coefficient due to gate bias	1/ V	0.0
THETA2#	Mobility reduction coefficient due to drain bias	1/ V	0.0
THETA3#	Mobility reduction coefficient due to substrate bias	$\frac{1}{\sqrt{V}}$	0.0
GAMMAFF	Substrate doping coefficient for modeling the substrate doping term in the drain current expression	—	1.0
FLGSUBTH	Flag to invoke the subthreshold current model. The five sub parameters that follow are used if FLGSUBTH is set to 1.0	—	0.0
SUBEXP#	Subthreshold exponent multiplier	—	1.0
SUBEXPB#	Effect of substrate bias on the subthreshold exponent multiplier	—	0.0
SUBEXPD#	Effect of drain bias on the subthreshold exponent multiplier	—	0.0
SUBMULT#	Subthreshold current multiplier	—	0.0
SUBLIMT#	Subthreshold current limiting multiplier	—	1.0
LREF*	Length of the reference device	m	infinite
WREF*	Width of the reference device	m	infinite
TOX	Gate oxide thickness	m	1.0E–7

Usage Notes

The overlap capacitances CGSO, CGDO, and CGBO are computed, if you have not specified them. This is different from SPICE.

For the level 11 MOSFET model, parameters marked with the # sign are functions of device dimensions. Each of these parameters has three components. The reference component is represented by the parameter name, for example, VTO or THETA1. Dependence on the reciprocal of channel length

or width is represented by a parameter whose name is formed by appending L or W to the reference parameter name, for example, VTOL, VTOW or THETA1L, THETA1W. The reference components are the parameters for a device having channel length of LREF and width of WREF.

For the level 4 MOSFET model, parameters marked with the # sign also have corresponding parameters for their length and width dependency. For example, for parameter VFB (volts), the corresponding length and width dependency parameters are LVFB and WVFB (volt-meters). The formula to calculate the parameter based on the corresponding length and width dependency is:

$$P = P_o + \frac{P_L}{L_{eff}} + \frac{P_w}{W_{eff}}$$

where

$$L_{eff} = L - DL$$

$$W_{eff} = W - DW$$

The length and width dependency parameters are also affected by scalm.

MOSFET Parasitics

The computation of MOSFET parasitics is described in the following pages.

L_{eff} = L * LMLT + XL – 2.0 * (LD + DEL)

W_{eff} = W * WMLT + XW – 2.0 * WD

Note: DEL is not used in the BSIM model.

If CGSO or CGDO is not specified, then:

CGSO or CGDO = COX * (LD + FRINGE) * W_{eff}

If CGBO is not specified, then:

CGBO = COX * 2.0 * WD * L_{eff}

Sidewall Junction Capacitance (CJ0SW)

Let WR = W * WMLT + XW

If CJSW > 0.0 then

```
if HDIF > 0.0 then
        CJ0SW = CJSW * 2.0 * (WR + 2.0 * HDIF)
else if LDIF > 0.0 then
        CJ0SW = CJSW * 2.0 * (WR + 2.0 * LR)
else
        CJ0SW = CJSW * (PS or PD)
else
CJ0SW = 0.0
```

Bottom Junction Capacitance (CJ0)

Let LR = LD + LDIF

```
If CBS > 0.0 AND CBD > 0.0 then
      CJ0BS = CBS
      CJ0BD = CBD
else if HDIF > 0.0 then
      CJ0BS = CJ0BD = CJ * WR * HDIF
else if LDIF > 0.0 then
      CJ0BS = CJ0BD = CJ * WR * LR
else
      CJ0BS = CJ * AS
      CJ0BD = CJ * AD
```

Bottom Diode Leakage Current (ISDIODE)

```
If JS > 0.0 then
      if HDIF > 0.0 then
            ISDIODE = JS * WR * HDIF
      else if LDIF > 0.0 then
            ISDIODE = JS * WR * LR
      else if (AS or AD) > 0.0
            ISDIODE = JS * (AS or AD)
      else
            ISDIODE = 0.0
 else
      ISDIODE = IS
```

Sidewall Diode Leakage Current (ISSWDIODE)

```
If JSSW > 0.0 then
      if HDIF > 0.0 then
            ISSWDIODE = JSSW * 2.0 * (WR + 2.0 * HDIF)
      else if LDIF > 0.0 then
            ISSWDIODE = JSSW * 2.0 * (WR + 2.0 * LR)
      else if (PS or PD) > 0.0
            ISSWDIODE = JSSW * (PS or PD)
      else
            ISSWDIODE = 0.0
 else
      ISSWDIODE = ISSW
```

Parasitic Resistances (RPAR)

```
Let R = RS or RD and NR = NRS or NRD
If HDIF > 0.0 then
      if NR > 0.0 then
            RPAR = NR * RSH + LR * R / WR
      else
            RPAR = (HDIF * RSH + LR * R) / WR
      else if LDIF > 0.0
            RPAR = NR * RSH + LR * R / WR
      else if (RSH * NR) > 0.0 then
            RPAR = RSH * NR
 else
      RPAR = R
```

MOSFET Model Equations

The MOSFET representation consists of the parasitic diodes between source-bulk and drain-bulk, parasitic resistances, and the intrinsic MOSFET. This section describes all the MOSFET model equations for the intrinsic MOSFET. The equations used for parasitic diodes are the same as the equations described in the section *Diode Model Equations*.

All Levels

This section provides equations that are common to all levels.

Bottom Junction Capacitance

$$CJ = \sqrt{\frac{q \ \varepsilon_{si} \ NSUB}{2PB}}$$

Threshold Voltage

$$PHI = 2\frac{k \ TNOM}{q} \ ln\left(\frac{NSUB}{n_i}\right)$$

$$n_i = 1.45 \times 10^{16}$$

$$COX = \frac{\varepsilon_{ox}}{TOX}$$

$$GAMMA = \frac{\sqrt{2 \ q \ \varepsilon_{si} \ NSUB}}{COX}$$

$$E_g = 1.16 - \frac{7.02 \times 10^4 \times TNOM^2}{TNOM + 1108.0}$$

$$\Phi_{ms} = -0.05 - 0.5E_g - 0.5PHI \qquad if\ TPG = 1$$

$$= 0.5E_g - 0.5PHI \qquad if\ TPG = -1$$

$$vfb = \Phi_{ms} - \frac{qNSS}{COX}$$

$$VTO = vfb + PHI + GAMMA\sqrt{PHI}$$

$$vbi = VTO - GAMMA\sqrt{PHI}$$

$$= vfb + PHI$$

Device Dimensions

$$l' = L \times LMLT + XL - 2 \times LD$$

$$w' = W \times WMLT + XW - 2 \times WD$$

Mobility

$$KP = UO \quad COX \qquad \text{if KP is not specified}$$

$$\beta = KP \ \frac{w'}{l'}$$

$$UO = \frac{KP}{COX}$$

Depletion Layer Width

$$xd = \sqrt{\frac{2\varepsilon_{si}}{qNSUB}}$$

Bias Quantities

$$sarg = \sqrt{PHI - vbs} \qquad if\ vbs \leq 0.0$$

$$= \frac{\sqrt{PHI}}{1 + 0.5\frac{vbs}{PHI} + 0.375\frac{vbs^2}{PHI^2}} \qquad if\ vbs > 0.0$$

$$barg = \sqrt{PHI - (vbs - vds)} \qquad if\ vbs - vds \leq 0.0$$

$$= \frac{\sqrt{PHI}}{1 + 0.5\frac{(vbs - vds)}{PHI} + 0.375\frac{(vbs - vds)^2}{PHI^2}} \qquad if\ vbs - vds > 0.0$$

Level 1

This is a Shichman-Hodges model.

Threshold Voltage

$$vth = vbi + GAMMA \quad sarg$$

Drain Current

If vds ≤ vgs - vth (linear region),

$$ids = \beta(1 + LAMBDA \quad vds)\left(vgs - vth - \frac{1}{2}vds\right)vds$$

If vds > vgs - vth (saturation region),

$$ids = \frac{1}{2}\beta(1 + LAMBDA \quad vds)(vgs - vth)^2$$

Level 2

This is an analytical model.

Threshold Voltage

$$F_N = \frac{1}{8}\frac{2\pi\varepsilon_{si}\ DELTA}{COX\ w'}$$

$$argss = \frac{1}{2}\frac{XJ}{l'}\left[\sqrt{1+2\left(\frac{xd\ \ sarg}{XJ}\right)}-1\right]$$

$$argsd = \frac{1}{2}\frac{XJ}{l'}\left[\sqrt{1+2\left(\frac{xd\ \ barg}{XJ}\right)}-1\right]$$

$$\gamma_{SD} = GAMMA(1-argss-argsd)$$

$$cfs = q\ \ NFS$$

$$Q_{dep} = COX\ \ \gamma_{SD}\ \ sarge$$

$$cd = \frac{\partial Q_{dep}}{\partial vbs}$$

$$xn = 1+\frac{cfs}{COX}+\frac{cd}{COX}+FN$$

$$vth = vbi + F_N(PHI-vbs)+\gamma_{SD}\ \ sarg+\frac{kT}{q}\ \ xn$$

$$vbin = vbi + F_N(PHI-vbs)$$

Mobility Reduction

$$\mu_{fact} = \left[\frac{\varepsilon_{si}\ UCRIT}{COX(vgs - vth - UTRA\ \ vds)}\right]^{UEXP}$$

$$\mu_{eff} = \mu_{fact}\ \ UO$$

Saturation Voltage

$$\eta = 1 + F_N$$

$$\gamma_D = \frac{\gamma_{SD}}{\eta}$$

$$vgsx = vgs \qquad if\ NFS = 0.0$$
$$= vgs \qquad if\ NFS > 0.0\ and\ vgs \geq vth$$
$$= vth \qquad if\ NFS > 0.0\ and\ vgs < vth$$

$$vdsat = \frac{vgsx - vbin}{\eta}$$

$$+ \frac{1}{2}\ \gamma_D^2\left[1 - \sqrt{1 + \left(\frac{4}{\gamma_D^2}\right)\left(\frac{vgsx - vbin}{\eta}\right) + PHI - vbs}\right] \qquad If\ vmax = 0.0$$

If vmax > 0.0 then vdsat is computed by solving the fourth order polynomial obtained as follows:

vmax =

$$\frac{\mu_{eff}\left\{\left(-vbin-\frac{1}{2}\ \eta\ vdsat\right)vdsat-\frac{2}{3}\ \gamma_{sd}[\ \sqrt[3]{(PHI-(vbs-vdsat))}-\ \sqrt[3]{(PHI-vbs)}]\right\}}{l'[vgs-vbin-\eta\ \ vdsat-\gamma_{sd}\sqrt{PHI-(vbs-vdsat)}]}$$

$$xv\ =\ \frac{VMAX\ \ l'}{\mu_{eff}}$$

$$x\ =\ \sqrt{vdsat+PHI-vbs}$$

$$v_1\ =\ \frac{vgs-vbin}{\eta}+PHI-vbs$$

$$v_2\ =\ PHI-vbs$$

$$xv\ =\ \frac{\left(v_1-\frac{v_2}{2}-\frac{x^2}{2}\right)(x^2-v_2)-\frac{2}{3}\ \gamma_D(x^3-\ \sqrt[3]{v_2})}{v_1-\gamma_D\ \ x-x^2}$$

$$A\ =\ \frac{4}{3}\gamma_D \qquad B\ =\ -\ 2(v_1+xv)$$

$$C\ =\ -\ 2\gamma_D\ \ xv \qquad D\ =\ 2v_1(v_2+xv)-v_2^2-\frac{4}{3}\gamma_D\ \ \sqrt[3]{v_2}$$

$$x^4+Ax^3+Bx^2+Cx+D\ =\ 0$$

Channel Length Modulation

If LAMBDA > 0.0, then

$$I_{fact} = 1 - LAMBDA\,vds$$

If LAMBDA ≤ 0.0 and NSUB > 0.0 and VMAX = 0.0, then

$$I_{fact} = 1 - \frac{xd}{l'}\sqrt{\frac{vds - vdsat}{4} + \sqrt{1 + \left(\frac{vds - vdsat}{4}\right)^2}}$$

If LAMBDA ≤ 0.0 and NSUB > 0.0 and VMAX > 0.0, then

$$I_{fact} = 1 - \frac{xd}{\sqrt{NEFF}\ l'} \times \left\{ \sqrt{\left(\frac{VMAX\ \ xd}{2\sqrt{NEFF}\ \ \mu_{eff}}\right)^2 + vds - vdsat} - \frac{VMAX\ \ xd}{2\sqrt{NEFF}\ \ \mu_{eff}} \right\}$$

$$xwb = xd\sqrt{PB}$$

$$I_e = l'\ I_{fact}$$

$$I_{eff} = \frac{xwb}{1 + \frac{xwb\ -\ I_{eff}}{xwb}} \qquad if\ Ieff < xwb$$

$$I_{fact} = \frac{I_{eff}}{l'}$$

Drain Current

$$\beta_{eff} = \beta \frac{\mu_{fact}}{I_{fact}}$$

$$vdsx = vds \qquad if\ vds \leq vdsat$$
$$= vdsat \qquad if\ vds > vdsat$$

$$ids = \beta_{eff}\left\{\left(vgsx - vbin - \frac{1}{2}\eta \ \ vdsx\right)\right.$$

$$\left. - \frac{2}{3} \ \gamma_{SD}[\ \sqrt[3]{PHI - (vbs - vdsx)} - \ \sqrt[3]{PHI - vbs} \ ]\right\}$$

If vgs ≤ vth and NFS > 0.0, then

$$ids = ids \ e^{\frac{q}{kT}\frac{vgs - vth}{xn}}$$

Level 3

This is a semi-empirical model.

Threshold Voltage

$$F_N = \frac{1}{4}\ \frac{2\pi\varepsilon_{si} DELTA}{COXw'}$$

$$\sigma = \frac{\Omega\ \ ETA}{COX(l')^3}$$

$$\Omega = 8.15 \times 10^{-22}$$

$$W_p = xd\ \ sarg$$

$$d_0 = 0.0631353$$

$$d_1 = 0.8013292$$

$$d_2 = 0.01110777$$

$$\frac{W_c}{XJ} = d_0 + d_1\frac{W_p}{XJ} + d_2\frac{W_p^2}{XJ}$$

$$F_s = 1 - \frac{XJ}{l'}\left[\frac{LD + W_c}{XJ}\sqrt{1 - \left(\frac{\frac{W_p}{XJ}}{1 + \frac{W_p}{XJ}}\right)^2} - \frac{LD}{XJ}\right]$$

$$xn = 1 + \frac{qNFS}{COX} + \frac{GAMMA\ \ F_s\ \ sarg + F_N(PHI - vbs)}{2(PHI - vbs)}$$

$$vth = vfb + PHI + \sigma\ \ vds + GAMMA\ \ F_s\ \ sarg + F_N(PHI - vbs) + \frac{kT}{q}xn$$

Mobility Reduction

$$vgsx = max(vgs,vth)$$

$$\mu_{fact} = \frac{1}{1 + THETA(vgsx - vth)}$$

$$\mu_s = \mu_{fact} UO$$

Saturation Voltage

$$F_B = \frac{GAMMA\_S}{4\,sarg} + F_N$$

$$vdsat = \frac{vgsx - vth}{1 + F_B} + \frac{VMAX\_l'}{\mu_s}$$

$$- \sqrt{\left(\frac{vgsx - vth}{1 + F_B}\right)^2 + \left(\frac{VMAX\_l'}{\mu_s}\right)^2}$$

$$vdsx = min(vds,vdsat)$$

Drain Current

$$F_{drain} = \frac{1}{1 + \frac{\mu_s}{VMAX\_l'} vdsx}$$

$$ids = \beta\ \mu_{fact}\ F_{drain}\left(vgsx - vth - \frac{1 + F_B}{2} vdsx\right) vdsx$$

Channel Length Modulation

If vds > vdsat, then the channel length modulation factor is computed.
If VMAX = 0.0, then

$$\Delta l = xd\sqrt{KAPPA(vds - vdsat)}$$

If VMAX > 0.0, then

$$idsat = ids$$

$$gdsat = idsat(1 - F_{drain})\frac{\mu_s}{l' \ VMAX}$$

$$E_p = \frac{idsat}{gdsat \ l'}$$

$$\Delta l = \sqrt{\left(\frac{E_p xd^2}{2}\right)^2 + KAPPA \ xd^2(vds - vdsat)} - \frac{xd^2 E_p}{2}$$

$$If \ \Delta l > \frac{1}{2} \ l', \ then$$

$$\Delta l = l' - \frac{(l')^2}{4\Delta l}$$

$$l_{fact} = \frac{1}{1 - \frac{\Delta l}{l'}}$$

$$ids = ids \ l_{fact}$$

Subthreshold Conduction

$$ids = ids \; e^{\frac{q}{kT}\frac{vgs - vth}{xn}}$$

Level 4

This is the BSIM model, a short channel model.

Threshold Voltage

$$\eta = ETA + X2E \;\; vbs + X3E(vds\text{-}VDD)$$

$$vth = VFB + PHI + K1\sqrt{PHI - vbs} - K2(PHI\text{-}vbs) - \eta \;\; vds$$

Mobility Reduction

$$U_{gs} = U0 + X2U0 \;\; vbs$$

$$U_{ds} = \frac{U1 + X2U1 \;\; vbs + X3U1(vds - VDD)}{l'}$$

Effective Beta

$$\beta_{0_0} = MUZ \ \ cox\frac{w'}{l'}$$

$$\beta_{0_b} = X2MZ \ \ cox\frac{w'}{l'}$$

$$\beta_{vds=0} = \beta_{0_0} + \beta_{0_b} vbs$$

$$\beta_{VDD} = MUS \ \ cox\frac{w'}{l'}$$

$$\beta_{VDD_b} = X2MS \ \ cox\frac{w'}{l'}$$

$$\beta_{vds\,=\,VDD} = \beta_{VDD} + \beta_{VDD_b} vbs$$

$$\beta_{VDD_d} = X3MS \ \ cox\frac{w'}{l'}$$

$$\frac{\partial\beta}{\partial vds} I_{vds=VDD} = \beta_{VDD_d}$$

$$\beta_0 = \beta_{vds=VDD} + \frac{\partial\beta}{\partial vds} I_{vds=VDD}(vds - VDD) \qquad if\ vds > VDD$$

$$= \beta_{vds=0} + vds\{[\frac{2(\beta_{vds=VDD} - \beta_{vds=0})}{VDD} - \frac{\partial\beta}{\partial vds} I_{vds\,=\,VDD}]$$

$$+ \left[\frac{-\beta_{vds\,=\,VDD} + \beta_{vds\,=\,0} + \frac{\partial\beta}{\partial vds} I_{vds\,=\,VDD} \ \ VDD}{VDD^2}\right] vds\,\} \qquad if\ vds \le VDD$$

$$\beta = \frac{\beta_0}{1 + U_{gs}(vgs - vth)}$$

Saturation Voltage

$$g = 1 - \frac{1}{1.744 + 0.8364(PHI - vbs)}$$

$$a = 1 + \frac{gK1}{2\sqrt{PHI - vbs}}$$

$$vc = \frac{U_{ds}(vgs - vth)}{a}$$

$$k = \frac{1 + vc + \sqrt{1 + 2vc}}{2}$$

$$vdsat = \frac{vgs - vth}{a\sqrt{k}}$$

Drain Current

$$vz = vds \qquad if\ vds \leq vdsat$$

$$= vdsat \qquad if\ vds > vdsat$$

$$ids = \frac{\beta}{(1 + U_{ds}vz)}\left[(vgs - vth)vz - \frac{a}{2}vz^2\right]$$

Subthreshold Conduction

$$n = N0 + NB \ \ vbs + ND \ \ vds$$

$$vt = \frac{kT}{q}$$

$$iexp = \beta_{0_0} \ \ vt^2 \ \ e^{1.8} e^{\frac{vgs - vth}{nvt}} \ (1 - e^{-vds/vt})$$

$$ilimit = 4.5 \ \ \beta_{0_0} \ \ vt^2$$

$$isubt = \frac{ilimit \times iexp}{ilimit + iexp}$$

$$ids = ids + isubt$$

Geometry Dependence

Each model parameter has three components: reference value, channel length dependence, and channel width dependence. The reference value is indicated by the parameter name. Length and width dependence component names are formed by prefixing `l` and `w` to the parameter name.

$$l' = L - DL$$

$$w' = W - DW$$

$$param = param + \frac{lpara}{l'} + \frac{wparam}{w'}$$

Level 6

This is the ASPEC model.

Threshold Voltage

If LGAMMA > 0 and VBO = 0, then

$$scf = 1 - \left(\sqrt{1 + \frac{2\ LAMBDA\ \ sarg}{LGAMMA}} - 1\right)\frac{LGAMMA}{l'}$$

Else scf = 1

$$gw = 1 + \frac{NWM}{w'}xd\ \ sarg$$

$$gl = 1 - \frac{XJ}{l'}\left[\sqrt{1 + \frac{2\ LAMBDA\sqrt{PHI - vbs + SCMvds}}{XJ}} - 1\right]$$

If VBO = 0, then $\gamma' = GAMMA$

If VBO > 0 and (-vbs) < VBO, then $\gamma' = GAMMA$

If VBO > 0 and (-vbs) > VBO, then $\gamma' = LGAMMA$

$$\gamma = \gamma'\ gw\ \ gl\ \ scf$$

$$\gamma_1 = GAMMA\ \ gw\ \ gl\ \ scf$$

$$vfb = vfb + (\gamma_1 - \gamma)\sqrt{VBO + PHI} \qquad \text{if } VBO > 0 \text{ and } (-vbs) > VBO$$

$$vfb = vfb + (GAMMA - \gamma)\sqrt{PHI} \qquad \text{if } GAMMA \neq \gamma$$

$$vfb = vfb - \frac{NWE}{w'} - \frac{LD}{l'}VSH -$$

$$\frac{\varepsilon_{si}}{COX \; l'}[FDSmin(vds,VFDS) + UFDS \;\; max(vds - VFDS,0)]$$

$$vte = vfb + PHI + \gamma \;\; sarg$$

$$vg = vgs - vbs - vfb$$

$$vgdrive = vgs - vte$$

Weak Inversion

For WIC = 0:

$$f_{weak} = 1$$

$$von = vg$$

For WIC = 1:

$$V_x = \frac{kT}{q}\left(1 + \frac{qNFS}{COX} + \frac{\gamma}{2sarg}\right)$$

$$von = max(vg,\ PHI - vbs + \gamma\ sarg + V_x)$$

$$f_{weak} = e^{\frac{vg - von}{V_x}}$$

For WIC = 2:

$$V_x = \frac{kT}{q}\left(1 + \frac{qNFS}{COX} + \frac{\gamma}{2sarg}\right)$$

$$von = max(vg,\ PHI - vbs + \gamma\ sarg + V_x)$$

$$voff = max(vg,\ PHI - vbs + \gamma\ sarg - PHI)$$

$$f_{weak} = \left(1 - \frac{von - voff}{V_x + PHI}\right)^{WEX}$$

Saturation Voltage

$$\eta = 1 + \frac{NWE}{w'}$$

$$vsat0 = \left\{ \sqrt{\left(\frac{\eta\gamma}{2}\right)^2 + \frac{von + \frac{NWE(PHI - vbs)}{w'}}{\eta}} - \frac{\gamma}{2\eta} \right\}^2$$

$$vc = ECRIT \quad l' \qquad \text{if } ECRIT > 0$$

$$= \frac{VMAX \quad l'}{\mu_{eff}} \qquad \text{if } VMAX > 0$$

$$vsat = vsat + vc - \sqrt{(vsat + vbs - PHI)^2 + vc^2}$$

Alternate Saturation Voltage

If KU > 1, then

$$\alpha = \frac{ECRIT \quad l'}{vgdrive}$$

$$fu = 1 - \frac{KU}{\sqrt{\alpha^2 + KU^2} + \alpha(KU - 1)}$$

$$fa = KAfu^{2MAL}$$

If KU ≤ 1, then

$$fu = 1$$

$$fa = 1$$

$$vd = vds - vbs + PHI$$

$$vde = min\left(\frac{vd}{fa}, vsat\right)$$

Mobility Reduction

$$vdse = vde + vbs - PHI$$

For MOB = 0:

$$\mu_{fact} = 1$$

For MOB = 1:

$$\mu_{fact} = \frac{1}{1 + F1(vg - vs - UTRA \ \ vdse)}$$

For MOB = 2:

$$\mu_{fact} = \left(\frac{\frac{F1 \ \ \varepsilon_{si}}{COX}}{vg - vs - UTRA \ \ vdse} \right)^{UEXP}$$

For MOB = 3:

$$FF = F1 \qquad \text{if } vgdriveU^{EXP} \leq VF1$$

$$= UTRA \qquad \text{if } vgdriveU^{EXP} > VF1$$

$$F = FFvgdrive^{UEXP}$$

$$= F + (F1 + UTRA)VF1 \qquad \text{if } VF1 > 0 \text{ and } vgdriveU^{EXP} > VF1$$

$$\mu_{fact} = \frac{1}{F4 + F}$$

For MOB = 4 or MOB = 5:

$$vcrit = ECRIT \ \ l' \qquad \text{if } MOB = 4$$

$$= \text{UTRA} \ \ l' \qquad \text{if } MOB = 5$$

$$\mu_{fact} = \frac{1}{1 + \frac{vgdrive\,COX}{F1\ \varepsilon_{si}} + \frac{vdse}{vcrit} + F2\ \ sarg}$$

Effective Mobility:

$$\mu_{eff} = \mu_{fact} UO$$

Channel Length Modulation

For CLM = 0:

$$\Delta l = 0$$

For CLM = 1:

$$LAMBDA = \sqrt{\frac{2\varepsilon_{si}}{qNSUB}} \qquad \text{if not specified}$$

$$\Delta l = LAMBDA\sqrt{vd - vde}\left(\frac{vsat + vbs - PHI}{vsat0 + vbs - PHI}\right)^{KL}$$

For CLM = 2:

$$\Delta l = \frac{\varepsilon_{si}}{COX}\ \frac{vd - vde}{A1(vd - vg) + A2(vg - vde + vbs - PHI)}$$

For CLM = 3:

$$\Delta l = LAMBDA\ \ fu^{2MCL} \times$$

$$(\sqrt{vd - fa\ \ vsat + KCL\ \ vbs + PHI} - \sqrt{KCL\ \ vbs + PHI})$$

For CLM = 4:

$$\Delta l = \left(\frac{2A1\ \ \varepsilon_{si}}{q\ \ NSUB\ \ \ln\left(\frac{DND}{NSUB}\right)}\right)^{KL} [(vd - vde + PHI)^{KL} - PHI^{KL}]$$

Drain Current

$$\beta_{eff} = \mu_{eff}\ \beta\ fa^{2MBL}\ f_{weak}\frac{l'}{l' - \Delta l}$$

$$vs = PHI - vbs$$

$$ids = \beta_{eff}\{von(vde - vs)$$

$$\left(-\frac{1}{2}(vde - vs)\right)\left[vde + vs + \frac{NWE}{w'}(vde - vs)\right]$$

$$-\left(-\frac{2}{3}\gamma[(vde)^{3/2} - (vs)^{3/2}]\right)$$

Level 8

Threshold Voltage

This is an enhanced MOS2 (analytical) model.

$$F_N = \frac{1}{8}\ \frac{2\ \pi\ \varepsilon_{si}\ DELTA}{COX\ \ w'}$$

$$NSUB_{fact} = 1 - \frac{SNVB}{NSUB} vbs$$

$$\gamma = GAMMA\sqrt{NSUB_{fact}}$$

$$\Phi = PHI + 2\frac{kT}{q} ln(NSUB_{fact})$$

$$xd' = \frac{xd}{\sqrt{NSUB_{fact}}}$$

$$argss = \frac{1}{2}\ \frac{XJ}{l'}\left[\sqrt{1 + 2\left(\frac{xd'\ \ sarg}{XJ}\right)} - 1\right]$$

$$argsd = \frac{1}{2}\frac{XJ}{l'}\left(\sqrt{1 + 2\frac{xd'\ \ barg}{XJ}} - 1\right)$$

$$\gamma_{SD} = \gamma(1 - argss - argsd)$$

$$vbin = VTO - GAMMA\sqrt{PHI} + F_N(PHI - vbs)$$

$$xn = 1 + \frac{qNFS}{COX}\ \ \frac{1}{2}\ \ \frac{\gamma_{SD}}{sarg} + \frac{q\ \ \varepsilon_{si}\ \ SNVB\ \ sarg}{COX^2\ \ \gamma_{SD}} + F_N(PHI - vbs)$$

$$vth = vbin + \gamma_{SD} + \frac{kT}{q}\ \ xn\ \ \ CAV$$

Mobility Reduction

If UEXP > 0.0, then

$$\mu_{fact} = \left(\frac{\varepsilon_{si} UCRIT}{COX(vgs - vth)}\right)^{UEXP}$$

If UEXP ≤ 0.0, then

$$\mu_{fact} = \frac{1}{1 + UCRIT(vgs - vth)}$$

Saturation Voltage

$$vgsx = max(vgs, vth)$$

$$\eta = 1 + F_N$$

$$\gamma_D = \frac{\gamma_{SD}}{\eta}$$

$$vdsat' = \frac{vgsx - vbin}{\eta} +$$

$$\frac{1}{2}\ \gamma_D^2\ \left\{1 - \sqrt{1 + \frac{4}{\gamma_D^2}\ \left[\left(\frac{vgsx - vbin}{\eta}\right) + PHI - vbs\right]}\right\}$$

$$vdsat = vdsat' + ECRIT\ \ l' - \sqrt{(vdsat')^2 + (ECRIT\ \ l')^2}$$

Channel Length Modulation

If vds > vdsat, then

$$I_{fact} = 1 - \frac{LAMBDA}{1 + LAM1 \quad l'}(vds - vdsat)$$

If vds ≤ vdsat, then

$$I_{fact} = 1$$

Drain Current

$$vdsx = min(vds, vdsat)$$

$$\beta_{eff} = KP \quad \frac{\mu_{fact}}{I_{fact}} \quad \frac{1}{1 + \frac{UTRA}{l'} \quad vdsx}$$

$$ids = \beta_{eff}\left\{\left(vgsx - vbin - \frac{1}{2}\eta \quad vds\right)\right.$$
$$\left. - \frac{2}{3}\gamma_{SD}[\ \sqrt[3]{PHI - (-vdsx)} - \sqrt[3]{PHI - vbs}\ ]\ \right\}$$

If vgs ≤ vth and NFS > 0.0, then

$$ids = idse^{\frac{q}{kT}\frac{vgs - vth}{xn}}$$

Level 11

This is the CSIM model, a short channel model.

Threshold Voltage

$$vth = VTO + GAMMA(\sqrt{PHI - vbs} - \sqrt{PHI}) + GAMMA2 \quad vbs - ETA \quad vds$$

Mobility Reduction

$$beta = \frac{BETA0}{1 + THETA1(vgs - vth) + THETA3 \times (\sqrt{PHI - vbs} - \sqrt{PHI})}$$

Saturation Voltage

$$g = 1 - \frac{1}{1.744 + 0.8364(PHI - vbs)}$$

$$a = 1 + \frac{g GAMMA GAMMAFF}{2\sqrt{PHI - vbs}}$$

$$vc = \frac{THETA2(vgs - vth)}{a}$$

$$k = \frac{1 + vc + \sqrt{1 + 2vc}}{2}$$

$$vdsat = \frac{vgs - vth}{a\sqrt{k}}$$

Drain Current

$$vz = vds \qquad if\ vds \leq vdsat$$

$$= vdsat \qquad if\ vds > vdsat$$

$$ids = \frac{beta}{1 + THETA2 \cdot vz} \times \left[(vgs - vth)vz - \frac{a}{2}vz^2 \right]$$

Subthreshold Conduction

The subthreshold component is added if the parameter SUBTHFLAG is greater than 0.0.

$$n = SUBEXP + SUBEXPB \cdot vbs + SUBEXPD \cdot vds$$

$$vt = \frac{kT}{q}$$

$$iexp = SUBMULT \cdot BETA0 \cdot vt^2 \cdot e^{1.8} \cdot e^{\frac{vgs - vth}{nvt}} (1 - e^{-vds/vt})$$

$$isl = SUBLIMT \cdot BETA0 \frac{(3vt)^2}{2}$$

$$isubt = \frac{isl \times iexp}{isl + iexp}$$

$$ids = ids + isubt$$

Geometry Dependence

Each model parameter has three components: reference value, channel length dependence and channel width dependence. The reference value is indicated by the parameter name. Length and width dependence component names are formed by appending “l” and “w” to the parameter name.

$$leff = L - 2\ DELTAL$$

$$weff = W - 2\ DELTAW$$

$$lreff = LREF - 2\ DELTAL$$

$$wreff = WREF - 2\ DELTAW$$

$$param = paraml\left(\frac{1}{leff} - \frac{1}{lreff}\right) + paramw\left(\frac{1}{weff} - \frac{1}{wreff}\right)$$

Temperature Dependence

TNOM = nominal temperature

T = analysis temperature

T_p = previous analysis temperature (TNOM if first temperature analysis)

The model quantities at the current analysis temperature are written without any suffix. The quantities at previous temperature are denoted by the suffix p. The quantities at the nominal temperature are denoted by the suffix NOM.

$$UO = UO_p\left(\frac{T}{T_p}\right)^{BEX}$$

$$KP = KP_p\left(\frac{T}{T_p}\right)^{BEX}$$

$$E_g = 1.16 - \frac{7.02\times10^{-4}T^2}{T + 1108.0}$$

$$n_i = 1.45\times10^{16}\left(\frac{T}{TNOM}\right)^{1.5} e^{-\frac{E_g - E_{gNOM}}{2kT}}$$

$$PHI = 2\frac{kT}{q}ln\frac{NSUB}{n_i}$$

$$PHI = \frac{T}{T_p}\left\{PHI_p - \left\{-2\frac{kT_p}{q}\left[\frac{3}{2}ln\frac{T_p}{TNOM} + q\left(-\frac{E_{gp}}{2kT_p} + \frac{E_{gNOM}}{2kT_{NOM}}\right)\right]\right\}\right\}$$

$$+ \left\{-2\frac{kT}{q}\left[\frac{3}{2}ln\frac{T}{TNOM} + q\left(-\frac{E_g}{2kT} + \frac{E_{gNOM}}{2kT_{NOM}}\right)\right]\right\}$$

$$vbi = vbi_p - 0.5(E_g - E_{gp}) + 0.5(PHI - PHI_p)$$

$$vfb = vbi - PHI$$

$$VTO = vbi + GAMMA\sqrt{PHI}$$

$$IS \ \alpha \ e^{-EG/kT}$$

$$IS = IS_p e^{-\left(\frac{E_g}{kT} - \frac{E_{gp}}{kT}\right)}$$

$$JS = JS_p e^{-\left(\frac{E_g}{kT} - \frac{E_{gp}}{kT}\right)}$$

$$ISSW = ISSW_p e^{-\left(\frac{E_g}{kT} - \frac{E_{gp}}{kT}\right)}$$

$$JSSW = JSSW_p e^{-\left(\frac{E_g}{kT} - \frac{E_{gp}}{kT}\right)}$$

$$P = \frac{kT}{q} ln \frac{N_A N_D}{n_i^2}$$

$$PB = \frac{T}{T_p}\left\{PB_p - \left\{-2\frac{kT_p}{q}\left[\frac{3}{2}ln\frac{T_p}{TNOM} + q\left(-\frac{E_{gp}}{2kT_p} + \frac{E_{gNOM}}{2kT_{NOM}}\right)\right]\right\}\right\}$$

$$+\left\{-2\frac{kT}{q}\left[\frac{3}{2}ln\frac{T}{TNOM} + q\left(-\frac{E_g}{2kT} + \frac{E_{gNOM}}{2kT_{NOM}}\right)\right]\right\}$$

$$CJ = CJ_{NOM}\{1 + MJ\left[0.0004(T - TNOM) - \frac{PB - PB_{NOM}}{PB_{NOM}}\right]\}$$

$$CJSW = CJSW_p\{1 + MJ\left[0.0004(T - TNOM) - \frac{PB - PB_{NOM}}{PB_{NOM}}\right]\}$$

$$CBD = CBD_p\{1 + MJ\left[0.0004(T - TNOM) - \frac{PB - PB_{NOM}}{PB_{NOM}}\right]\}$$

$$CBS = CBS_p\{1 + MJ\left[0.0004(T - TNOM) - \frac{PB - PB_{NOM}}{PB_{NOM}}\right]\}$$

$$RS = RS_{NOM}[1 + TRS(T - TNOM)]$$

$$RD = RD_{NOM}[1 + TRD(T - TNOM)]$$

$$RSH = RSH_{NOM}[1 + TRSH(T - TNOM)]$$

Level 4

$$MUZ = MUZ_p\left(\frac{T}{T_p}\right)^{BEX}$$

$$X2MZ = X2MZ_p\left(\frac{T}{T_p}\right)^{BEX}$$

$$MUS = MUS_p\left(\frac{T}{T_p}\right)^{BEX}$$

$$X2MS = X2MS_p\left(\frac{T}{T_p}\right)^{BEX}$$

$$X3MS = X3MS_p\left(\frac{T}{T_p}\right)^{BEX}$$

$$\Delta PHI = PHI_p - PHI$$

$$VFB = VFB_p + \Delta PHI$$

Level 11

$$BETA0 = BETA0_p\left(\frac{T}{T_p}\right)^{BEX}$$

$$BETA0L = BETA0L_p\left(\frac{T}{T_p}\right)^{BEX}$$

$$BETA0W = BETA0W_p\left(\frac{T}{T_p}\right)^{BEX}$$

$$\Delta VTO = VTO - VTO_p$$

$$VTO = VTOL_p + \Delta VTO$$

$$VTOW = VTOLW_p + \Delta VTO$$

TLEV = 1

In this case, the following parameters are not computed using the equations described above. The following equations are used instead.

TCV should be specified with proper sign, similar to VTO specification. The sign for P-channel devices is opposite to that for N-channel devices.

$$VTO = VTO(TNOM) - TCV(T - TNOM)$$

$$CJ = CJ_{TNOM}[1 + CTA(T - TNOM)]$$

Yang-Chatterjee Charge Model

$$\gamma = \frac{vth - vbi}{sarg}$$

$$\alpha_x = \frac{vgs - vth}{vdsat}$$

$$C_o = COX \;\; w' \;\; l'$$

Accumulation Region (vgs ≤ vfb + vbs)

$$Q_g = C_o(vgs - vfb - vbs)$$

$$Q_b = -Q_g$$

$$Q_c = 0$$

$$Q_s = 0$$

$$Q_d = 0$$

Subthreshold Region (vfb + vbs < vgs ≤ vth)

$$Q_g = C_o \frac{\gamma^2}{2} \left\{ -1 + \sqrt{1 + \frac{4(vgs - vfb - vbs)}{\gamma^2}} \right\}$$

$$Q_b = -Q_g$$

$$Q_c = 0$$

$$Q_s = 0$$

$$Q_d = 0$$

Saturation Region (vth < vgs ≤ $\alpha_x$vds + vth)

$$Q_g = C_o\left(vgs - vfb - PHI - \frac{vgs - vth}{3\alpha_x}\right)$$

$$Q_b = C_o\left[vfb + PHI - vth - \frac{(1-\alpha_x)(vgs - vth)}{3\alpha_x}\right]$$

$$Q_c = -\frac{2}{3}C_o(vgs - vth)$$

$$Q_d = 0$$

$$Q_s = -\frac{2}{3}C_o(vgs - vth)$$

Linear Region (vgs > ax vds + vth)

$$Q_g = C_o\left[vgs - vfb - PHI - \frac{vds}{2} + \frac{\alpha_x vds^2}{12\left(vgs - vth - \frac{\alpha_x vds}{2}\right)}\right]$$

$$Q_b = C_o[vfb + PHI - vth + \frac{1-\alpha_x}{2} - \frac{(1-\alpha_x)\alpha_x vds^2}{12\left(vgs - vth - \frac{\alpha_x vds}{2}\right)}]$$

$$Q_c = -C_o\left[vgs - vth - \frac{\alpha_x}{2}vds + \frac{\alpha_x^2 vds^2}{12\left(vgs - vth - \frac{\alpha_x vds}{2}\right)}\right]$$

$$Q_d = -C_o\left[\frac{vgs - vth}{2} - \frac{3}{4}\alpha_x vds + \frac{\alpha_x^2 vds^2}{8\left(vgs - vth - \frac{\alpha_x vds}{2}\right)}\right]$$

$$Q_s = -C_o\left[\frac{vgs - vth}{2} - \frac{1}{4}\alpha_x vds - \frac{\alpha_x^2 vds^2}{24\left(vgs - vth - \frac{\alpha_x vds}{2}\right)}\right]$$

Meyer Charge Model

$$\gamma = \frac{vth - vbi}{sarg}$$

$$\Phi_f = \frac{1}{2} PHI$$

$$C_o = COX \; w' \; l'$$

$$vgb = vgs - vbs$$

Cut-off Region (vgs ≤ vth)

$$C_{GSC} = \frac{2}{3} C_o \frac{vgs - (vth - \Phi_f)}{\Phi_f}$$

$$CGS = 0 \qquad if\ vgs \leq vth - \phi_f$$

$$= C_{GSC} \qquad if\ vth - \phi_f < vgs,\ vds \geq 0.1$$

$$= C_{GSC}\left(\frac{0.1 + vds}{0.2}\right) \qquad if\ vth - \phi_f < vgs,\ vds < 0.1$$

$$CGD = 0 \qquad if\ vgs \leq vth - \phi_f$$

$$= 0 \qquad \text{if } vth - \phi_f < vgs,\ vds \geq 0.1$$

$$= C_{GSC}\left(\frac{0.1 - vds}{0.2}\right) \qquad if\ vth - \phi_f < vgs,\ vds < 0.1$$

$$CGB = \frac{C_o}{\sqrt{1 + \frac{4}{\gamma^2}(vgb - vfb)}} \qquad if\ vgb > vfb$$

$$= C_o \qquad if\ vgb \leq vfb$$

On Region (vgs > vth)

$$C_{GBO} = \frac{C_o}{\sqrt{1 + \frac{4}{\gamma^2}(vgb - vfb)}} \qquad if\ vgb > vfb$$

$$= C_o \qquad if\ vgb \leq vfb$$

$$CGB = C_{GBO}\frac{-vgs + vth + PHI}{PHI} \qquad if\ vgs < vth + PHI$$

$$= 0 \qquad if\ vgs \geq vth + PHI$$

Peak Region (vgs - vth < 0.1)

Where vds < 0.1

$$C_{GS1} = \frac{2}{3} C_o \frac{0.1 + vds}{0.2}$$

$$C_{GD1} = \frac{2}{3} C_o \frac{0.1 - vds}{0.2}$$

$$C_{GS2} = \frac{2}{3} C_o \left[1 - \frac{(0.1 - vds)^2}{(0.2 - vds)^2}\right]$$

$$C_{GD2} = \frac{2}{3} C_o \left[1 - \frac{0.01}{(0.2 - vds)^2}\right]$$

$$CGS = (C_{GS2} - C_{GS1}) \frac{vgs - vth}{0.1} + C_{GS1}$$

$$CGD = (C_{GD2} - C_{GD1}) \frac{vgs - vth}{0.1} + C_{GD1}$$

Where vds ≥ 0.1

$$CGS = \frac{2}{3} C_o$$

$$CGD = 0$$

Transition Region (vgs - vth ≥ 0.1, vds < 0.1)

$$CGS = \frac{2}{3} C_o\left[1 - \frac{(0.1 - vds)^2}{(0.2 - vds)^2}\right]$$

$$CGD = \frac{2}{3} C_o\left[1 - \frac{0.01}{(0.2 - vds)^2}\right]$$

Saturation Region (vgs - vth ≥ 0.1, vds ≥ vdsat)

$$CGS = \frac{2}{3} C_o$$

$$CGD = 0$$

Linear Region (vgs - vth ≥ 0.1, vds < vdsat)

$$CGS = \frac{2}{3} C_o\left[1 - \frac{(vdsat - vds)^2}{(2\ \ vdsat - vds)^2}\right]$$

$$CGD = \frac{2}{3} C_o\left[1 - \frac{vdsat^2}{(2\ \ vdsat - vds)^2}\right]$$

Ward-Dutton Charge Model

$$\gamma = \frac{vth - vbi}{sarg}$$

$$C_o = COX \;\; w' \;\; l'$$

$$v_g = vgs - vbs - vbi + PHI$$

$$v_s = PHI - vbs$$

$$v_z = PHI - vbs + vds \qquad if\ vds < vdsat$$

$$= PHI - vbs + vdsat \qquad if\ vds > vdsat$$

Accumulation Region ($v_g \leq 0$)

$$Q_g = C_o v_g$$

$$Q_b = -Q_g$$

$$Q_c = 0$$

$$Q_d = 0$$

$$Q_s = 0$$

Cut-off Region (vgs ≤ vth)

$$Q_g = C_o\gamma\left[\sqrt{\frac{\gamma^2}{4 + v_g}} - \frac{\gamma}{2}\right]$$

$$Q_b = - Q_g$$

$$Q_c = 0$$

$$Q_d = 0$$

$$Q_s = 0$$

On Region (vgs > vth)

$$i = v_g(\sqrt{v_z} + \sqrt{v_s}) - \frac{2}{3}\gamma(v_z + \sqrt{v_z}\sqrt{v_s} + v_s) - \frac{1}{2}(v_z + v_s)(\sqrt{v_z} + \sqrt{v_s})$$

$$Q_g = C_o v_g - \frac{C_o}{i}\left\{\frac{1}{2}v_g(v_z + v_s)(\sqrt{v_z} + \sqrt{v_s}) - \frac{2}{5}\gamma[v_z^2 + \sqrt{v_z}\sqrt{v_s}(v_z + v_s) + v_s^2] - \frac{1}{3}(\sqrt{v_z} + \sqrt{v_s})(v_z^2 + v_z v_s + v_s^2)\right\}$$

$$Q_b = \frac{-C_o\gamma}{i}\left\{\frac{2}{3}v_g(v_z + \sqrt{v_z}\sqrt{v_s} + v_s) - \frac{1}{2}\gamma(v_z + v_s)(\sqrt{v_z} + \sqrt{v_s}) - \frac{2}{5}[v_z^2 + \sqrt{v_z}\sqrt{v_s}(v_z + v_s) + v_z v_s + v_s^2]\right\}$$

$$Q_c = -(Q_g + Q_b)$$

$$Q_d = \frac{1}{2}\ Q_c \qquad \textit{if } vds \le vdsat$$

$$= XQC\ \ Q_c \qquad \textit{if } vds > vdsat$$

$$Q_s = \frac{1}{2}Q_c \qquad \textit{if } vds \le vdsat$$

$$= (1 - XQC)Q_c \qquad \textit{if } vds > vdsat$$

BSIM Charge Model

$$\gamma = \frac{vth - VFB - PHI}{sarg}$$

$$\alpha_x = \frac{vgs - vth}{vdsat}$$

$$C_o = COX \; w' \; l'$$

Accumulation Region (vgs ≤ VFB + vbs)

$$Q_g = C_o(vgs - VFB - vbs)$$

$$Q_b = -Q_g$$

$$Q_d = 0$$

Subthreshold Region (VFB + vbs < vgs ≤ vth)

$$Q_g = C_o \frac{\gamma^2}{2} \left\{ -1 + \sqrt{1 + \frac{4(vgs - VFB - vbs)}{\gamma^2}} \right\}$$

$$Q_b = -Q_g$$

$$Q_d = 0$$

Saturation Region (vth < vgs ≤ α_x vds + vth)

$$Q_g = C_o\left[vgs - VFB - PHI - \frac{(vgs - vth)}{3\alpha_x}\right]$$

$$Q_b = C_o\left[VFB + PHI - vth - \frac{(1 - \alpha_x)(vgs - vth)}{3\alpha_x}\right]$$

$$Q_d = 0 \qquad \text{if } XPART = 1$$

$$= -\frac{4}{15}C_o(vgs - vth) \qquad \text{if } XPART = 0$$

Linear Region (vgs > α_x vds + vth)

$$Q_g = C_o\left[vgs - VFB - PHI - \frac{vds}{2} + \frac{\alpha_x vds^2}{12\left(vgs - vth - \frac{\alpha_x vds}{2}\right)}\right]$$

$$Q_b = C_o[VFB + PHI - vth$$

$$+ \frac{1-\alpha_x}{2} vds \frac{(1-\alpha_x)\alpha_x vds^2}{12\left(vgs - vth - \frac{\alpha_x vds}{2}\right)}$$

If XPART = 1, then

$$Q_d = -C_o\left[\frac{vgs - vth}{2} - \frac{3}{4}\alpha_x vds + \frac{\alpha_x^2 vds^2}{8\left(vgs - vth - \frac{\alpha_x vds}{2}\right)}\right]$$

If XPART = 0, then

$$Q_d = -C_o\left\{\frac{vgs - vth}{2} - \frac{\alpha_x vds}{2} + \frac{\alpha_x vds}{\left(vgs - vth - \frac{\alpha_x vds}{2}\right)^2}\right.$$

$$\left.\times\left[\frac{(vgs - vth)^2}{6} - \frac{\alpha_x vds(vgs - vth)}{8} + \frac{\alpha_x^2 vds^2}{40}\right]\right\}$$

ASPEC Charge Model

$$C_o = COX \; w' \; l'$$

$$vth = vte$$

$$vth' = vth - CF1$$

$$vds' = CF3 \; vds$$

Gate-to-Bulk Capacitance

$vgs \leq vfb + vbs$ *(accumulation)*

$$CGB = C_o$$

$vfb + vbs < vgs \leq vth$ *(depletion)*

$$CGB = \frac{C_o}{\sqrt{1 + \frac{4}{\gamma^2}(vgs - vfb - vbs)}}$$

$vgs > vth$ *(inversion)*

$$CGB = \frac{C_o G^+}{\sqrt{1 + \frac{4}{\gamma^2}(\gamma\sqrt{PHI - vbs} - PHI - vbs)}}$$

Gate-to-Source Capacitance

$$CGS = x \;\; XCG \;\; C_o$$

vds < 0.1 and vgs ≤ vth′ (accumulation)

$$x = GD$$

vds < 0.1 and vth′ < vgs < vth + CF2 (weak inversion)

$$x = \frac{vgs - vth'}{CF2}\left[1 - \frac{(CF2 - vds)^2}{(2 \;\; CF2 - vds)^2} - D^-\right] + D^-$$

vds < 0.1 and vgs ≥ vth′ + CF2 (inversion)

$$x = 1 - \frac{(vgs - vth' - vds)^2}{(2(vgs - vth') - vds)^2}$$

vds ≥ 0.1, vgs ≤ vth′ and CF1 = 0 (accumulation)

$$x = G^-$$

vds 0.1, vgs ≤ vth′ and CF1 ≠ 0 (accumulation)

$$x = G \;\; D^+$$

vds ≥ 0.1, vth′ < vgs < vth′ + CF2 and CF1 = 0 (weak inversion)

$$x = \frac{vgs - vth'}{CF2}$$

vds ≥ 0.1, vth′ < vgs < vth′ + CF2 and CF1 ≠ 0 (weak inversion)

$$x = max\left[\frac{vgs - vth'}{CF2}, D^+\right]$$

vds ≥ 0.1 and vgs - vth ≤ vds′ (saturation)

$$x = 1$$

vds ≥ 0.1 and vgs - vth > vds′ (linear)

$$x = 1 - \frac{(vgs - vth - vds)^2}{[2(vgs - vth) - vds]^2}$$

Gate-to-Drain Capacitance

$$CGD = x \ XCG \ C_o$$

vds < 0.1 and vgs ≤ vth′ (accumulation)

$$x = G \ D^+$$

vds < 0.1 and vth′ < vgs < vth′ + CF2 (weak inversion)

$$x = D^+ + \frac{vgs - vth'}{CF2} max\left[1 - \frac{CF2^2}{(2 \ CF2 - vds)^2}, D^+\right]$$

vds < 0.1 and vgs ≥ vth′ + CF2 (inversion)

$$x = max\left[D^+, 1 - \frac{(vgs - vth' - vds)^2}{(2(vgs - vth') - vds)^2}\right]$$

vds ≥ 0.1 and vgs < vth′ (accumulation)

$$x = G \ D^+$$

vds ≥ 0.1 and vgs - vth ≤ vds′ (saturation)

$$x = D^+$$

vds ≥ 0.1 and vgs - vth > vds′ (linear)

$$x = max\left[D^+, 1 - \frac{(vgs - vth - vds)^2}{(2(vgs - vth) - vds)^2}\right]$$

Chapter 11
VeriBest Analog Optoelectronic Model Library

The Optoelectronic Library consists of two major groups of models:

- optocouplers
- light emitting diodes (LED) both discrete and 8-segment displays

The optocoupler macromodel contains the input diode, the output transistor and the proper function modeling the signal transfer from input to output. All the parameters of the macromodels were extracted from measurements of the devices.

The light emitting diodes are modeled as diodes with electric parameters extracted from measurements of the parts.

Chapter 12
VeriBest Analog Power Supply Model Library

The Power supply Library consists of macromodels of the following groups of integrated circuits:

- reference voltage devices,
- voltage regulators,
- switch mode power supply (SMPS) controllers.

The reference voltage devices are precision monolithic integrated circuits equivalent to Zener diodes, but with much sharper breakdown characteristics. They are modeled as diodes with parameters extracted from measurements of the devices.

The voltage regulator macromodels are parametrized. The following is a list of parametrized voltage regulator macromodels:

Parameter	Parameter Definition	Unit
VREF	Reference voltage of Vout	[V]
VREF_TC	Temperature coefficient of VREF VREF(T1) = VREF(T0)*[1+VREF_TC*(T1-T0)]	[V/C]
LINE_RG	Line regulation dVo/dVin	[%]
LOAD_RG	Load regulation dVo/dIo	[ohm]
RR_F3	Ripple rejection cutoff frequency	[Hz]
ZO_F3	Output resistance cutoff frequency	[Hz]
IO_MAX	Maximum output current	[A]
IO_MIN	Minimum output current	[A]
IO_SC	Short circuit current	[A]
I_Q	Quiescent current of the common terminal	[A]
I_Q_D	Dynamic range of I_Q as a function of load I_Q_D= dIq/dIo	[%]

Parameter	Parameter Definition	Unit
I_Q_TC	Temperature coefficient of I_Q I_Q(T1) = I_Q(T0)*[1+I_Q_TC*(T1-T0)]	[A/C]
VIN_MAX	Maximum input voltage	[V]
VDRP_MAX	Dropout voltage corresponding to IO_MAX	[V]
VDRP_MIN	Dropout voltage corresponding to IO_MIN	[V]
VDRP_TC	Temperature coefficient of VDRP VDRP(T1) = VDRP(T0)*[1+VDRP_TC*(T1-T0)]	[V/C]
P_SHDN	Power shutdown limit. If it is specified as “internally limited “in the datasheet, the following will suffice: P_SHDN = IO_SC* VIN_MAX	[Watt]
P_SDN_TC	Temperature coefficient of P_SHDN P_SHDN(T1) = P_SHDN(T0)*[1+P_SDN_TC*(T1-T0)]	[V/C]

The macromodels of the switch mode power supply (SMPS) controllers are the most complex. In simulation of SMPS circuits, the accuracy of the output pulse duty coefficient is crucial. Any inaccuracy in determining the duty introduces phase noise, which in turn causes the control loop, containing LC filter, to ring. In order to reduce this effect, the proper mechanism dynamically adjusting the timestep was built into these macromodels. It slows down the simulation speed, but ensures that the simulation results are meaningful.

Appendix A
Modeling

This appendix is meant to aid the engineer in the task of creation of both generic SPICE models and the more complex macromodels.

SPICE models are simply a series of SPICE parameter values for the generic SPICE models built into the VBASE simulation engine. These are for the devices BJT, MOSFET, Diodes, etc. Macromodels are a series of SPICE statements formed together to act as a netlist.

For creation of SPICE models, the normal method is to take an existing template and modify the SPICE parameters to the required values and save the model as a different name. There is no need to create a graphic symbol for these devices as changing the necessary properties under the VBDC symbol editor on an existing graphic symbol is sufficient.

The VBDC schematic editor can be used to create a unique component shape for every created macromodel. Certain necessary properties need to be applied to the graphic symbol to link it to the analog behavioral description or macromodel. These will be explained in more detail later.

The macromodel is a series of SPICE statements, calling standard component definitions like resistors, capacitors, transistors, etc.

Optionally, to be included with the macromodel file, is the parameter set file or PARSET file. This file lists a series of parameters that can be varied by the system. They include the default, minimum, and maximum values for each of the parameters, and they can also be set up as statistical information for performing either Monte Carlo or Worst Case analyses.

Necessary Properties or Parameters for Component Creation

To provide the link between the VBDC schematic symbol and the analog description, a number of properties must be applied to the symbol during the creation stage.

These properties act as pointers for the system to locate the analog model and to instruct the system how the individual wires connected to the pins relate to the description internally. These properties are listed below.

Property Name	Description
Simulation model	refers to the name of the subcircuit or SPICE description.
CLASS	declares that the component is either an analog or a digital component
Value	refers to the part value, such as resistance for a resistor or capacitance for a capacitor
Pin sequence	A pin sequence id number is added to pins to control the order in which the pins appear within the subcircuit description.
Part number	naming information that is required by the VBA and the layout tools to control packaging
DESCRIPTION	field used to identify the type of component if Simulation model is NOMODEL
Instance name	unique name to identify the component when placed in a schematic
Part name	the part's name

There are many other properties that can be added to symbols to control other products. Those listed above are the relevant properties for the analog simulation products. Properties for each of the particular device types are described in detail below.

Model Formats

There are three (3) basic model formats used in the VeriBest CAE tool set.

- SPICE .MODEL cards (generic)
- Unparameterized macromodels (.SUBCKT, no .PARSET)
- Parameterized macromodels (.SUBCKT with .PARSET)

The formats for these devices and the required properties to point to them vary for each of the particular model types.

SPICE Generic Models

These models are the generic models built into VBASE. The format for them is detailed below.

General Form:

`.MOD<EL>` *mname type* (*pname1=pval1 pname2=pval2* . . .)

Where:

mnameis the model name

type is one of the following model types:

DDiode
NPNNPN BJT
PNPPNP BJT
NJFN-Channel JFET
PJFP-Channel JFET
NMESN-Channel MESFET
PMESP-Channel MESFET
NMOSN-Channel MOSFET
PMOSP-Channel MOSFET
RResistor
CCapacitor
LInductor

pnameis the parameter name (for example, BV, IS, RD, ...)

pvalis the parameter value

Example

```
.MODEL  MOD1  NPN  (BF=50  IS=1E-13  VBF=50)
```

or

```
.MODEL  MOD1  NPN
+  BV=50
+  IS=1E-13
+  VBF=50
```

Unparameterized Macromodels

These models are created by combining the element definitions together to form a netlist. They can also contain comments, constant definitions, equations, and model statements. Using the equations and constant section, complex mathematical formula can be added into the description.The format for the unparameterized macromodel is as follows:-

.SUB<CKT> *sname n1 n2* . . .
<*mathematical section*>
netlist information . . .
. . .
model cards
.ENDS *sname*

Where:

sname	is the name of the macromodel
n1, n2 ...	are the external nodes of the macromodel
mathematical section	is an optional section that allows mathematical formula to be added into the macromodel description
netlist information	is the series of element definitions that define the topology and hence the functionality of the macromodel
model cards section	allows definition of generic SPICE models that are utilized within the macromodel

Comments can be added by preceding the line with an asterisk. This enables the engineer to include information like the pin sequencing relationship between the macromodel and the graphic symbol.

The pin sequencing relationship is controlled by the Pin sequence property that is added to the pins on the graphic symbol. It is simply a numerical order.

These models are stored in the Macro directory with the same name as the name embedded within the macromodel definition. This name is also assigned to the Simulation model property, on the graphic symbol to provide the connection between the two.

Unparameterized Macromodel Example

Detailed below is an example of an unparameterized macromodel. The device is an LM105 Voltage Regulator model.

```
.SUBCKT LM105 2 3 4 6 5 7 8 99
*
* Voltage Regulator Model
*
* Pin Seq: I/LIM B/OUT INPUT GND REF F/BCK
* Pin Seq Cont: COMP OUTPUT
*
C0 20 3 10P
D1 99 6 D105A
G2 99 16 6 99 1E-7
G3 99 16 3 20 7.98E-2
I4 19 99 200U
Q5 20 8 19 T105A
Q6 3 4 19 T105A
Q7 3 4 8 T105B
Q8 2 16 5 T105C
Q9 16 5 7 T105D
R10 16 99 400K
R11 6 2 600
R12 2 16 816
R13 5 7 50
R14 6 20 1292.5
R15 6 3 1292.5
R16 8 99 10
R17 6 99 10K
I18 99 8 0.17
...
* MODEL AND SUBCKT STATEMENTS
.MODEL D105A D IS=8.0E-16 BV=50 IBV=10
.MODEL T105A NPN IS=8.0E-16 BF=111.67 CJC=5P
+ CJE=5P CJS=5P
.MODEL T105B NPN IS=8.9E-16 BF=103.7 CJC=5P
+ CJE=5P CJS=5P
+ IKF=0.1 RE=1 RC=10 RB=100
.MODEL T105C NPN IS=8.309E-16 BF=146.  CJC=5P
+ CJE=5P CJS=5P
+ IKF=0.1 RE=1 RC=10 RB=100
.MODEL T105D NPN IS=1.309E-16 BF=100.0 CJC=5P
+ CJE=5P CJS=5P
+ IKF=0.1 RE=1 RC=10 RB=100
.ENDS LM105
```

Parameterized Macromodels

These models consist of two files. The first file (template) is identical in format to that of the unparameterized macromodel, but with one difference, a name syntax change to the model. The second file (Parset) is the parameter set file which contains a list of the parameters being passed to the macromodel and the appropriate statistical spread or tolerance for them.

Template

The format for the parameterized macromodel file is as follows:

```
.SUB<CKT> _sname n1 n2 ...
<parameter section>
<mathematical section>
netlist information ...
...
model cards
.ENDS _sname
```

Where

_sname	is the name of the macromodel. This file is known as the template file, take special note of the underscore preceding the macromodel name, this is explained later.
n1, n2 ...	are the external nodes of the macromodel
parameter section	is a series of parameter names and values used as default for the model in case the template is referenced directly and not via a parset file.
mathematical section	is an optional section that allows mathematical formula to be added into the macromodel description
netlist information	is the series of element definitions that define the topology and hence the functionality of the macromodel
model cards section	allows definition of generic SPICE models that are utilized within the macromodel

Note: Observe the underscore (_) as the first character of the model name which must be included in the filename as well.

Comments can be added by preceding the line with an asterisk. This enables the engineer to include information like the pin sequencing relationship between the macromodel and the graphic symbol.

The pin sequencing relationship is controlled by the Pin sequence property that is added to the pins on the graphic symbol. It is simply a numerical order.

Parset

The format for the parameter set file is as follows:

.PARSET *sname _sname*
+ pname1 = typ <#comment>
+ pname = typ stat min max <:Dist> <#comment> . . .

Where

sname	is the name of the macromodel
_sname	is the name of the template to which this macromodel relates
pname	is the name of the parameter being passed to the macromodel
stat	is the statistical keyword
typ min max	the typical, minimum, and maximum values for this parameter. By assigning a colon and the letter G, a Gaussian distribution can be assigned to this parameter. The same applies to the other distributions available.

An optional comment can be added at the end of the parameter describing the parameter or defining items such as units.

These models are stored in a macro directory with the same name as the name embedded within the parameter set definition. This name is also assigned to the Simulation model property, on the graphic symbol to provide the connection between the two.

Therefore the way the macromodel is found is by the Simulation model property on the graphic symbol pointing to the parameter set file. Then, using the template name, the macromodel is found.

The template or macromodel name does not need to be the same name as the parameter set file preceded by a an underscore in truth. The name can be quite unique. Therefore allowing the engineer to write one template or macromodel definition which can be pointed to by several different graphic symbols and parameter set files.

Parameterized Macromodel Example

Detailed below is an example of a parameterized macromodel. The device is an LM741 Operational Amplifier model.

```
.SUBCKT _LM741 100 101 2 3 4 5 7 PARAM
*
* Pin Seq :B1 B2 NEGI OUT POSI VCC VSS
*
+ IB = 80.0N
+ IOS = 20.0N
+ VOS = 1.0M
+ RIN = 2.0MEG
+ CIN = 0.4P
+ VIC_POS = 13.0
+ VIC_NEG = -13.0
+ VNOISE = 20.0N
+ FNOISE = 100.0
+ VO_POS = 14.0
+ VO_NEG = -14.0
+ RO = 50.0
...
*
"FZ_CMRR=10E5"
"IS_D1=1E-18"
"VT=25.9E-3"
"VT_D1=25.86E-3"
"VT_OUT=25.86E-3"
"PI=3.1416"
"CM=2E-9"
"CC=5E-12"
...
RC1 20 17 "RC"
RC2 20 18 "RC"
C1 17 18 "C1"
CIN 2 4 "CIN"
RE1 24 19 "RE"
RE2 27 19 "RE"
IEE 19 7 "IE"
VCM- 30 7 "VCMN"
VCM+ 5 20 "VCMP"
DCM+ 30 19 D1
Q1 17 2 24 QIN
Q2 18 23 27 QIN
EVOS 23 4 42 0 "VOS"
...
.MODEL D1 D IS="IS_D1"
.MODEL D2 D IS=1E-18
.MODEL QIN NPN BF="BF_IN"
+ KF="KF"
```

```
.MODEL QOUT_PNP PNP IS="IS_OUT" BF=1000
+ RC=300
.MODEL QOUT_NPN NPN IS="IS_OUT" BF=1000
+ RC=300
.ENDS _LM741
```

Parameter Set File

These parameter values override those in the default parameter section of the parameterized macro-model.

```
.PARSET LM741 _LM741
+ IB = 80.0N STAT 20.0N 500.0N :GAUSS
+ IOS = 20.0N STAT -200.0N 200.0N :GAUSS
+ VOS = 1.0M STAT -5.0M 5.0M :GAUSS
+ RIN = 2.0MEG STAT 0.2MEG 12.0MEG :GAUSS # Input Res
+ CIN = 0.4P STAT 0.1P 10P :GAUSS # Input Capacitance
+ VIC_POS = 13.0 STAT 12 20 :GAUSS
+ VIC_NEG = -13.0 STAT -20 -12 :GAUSS
+ VNOISE = 20.0N STAT 10N 60N :GAUSS
+ FNOISE = 100.0 STAT 20 1K :GAUSS
+ VO_POS = 14.0 STAT 10 14 :GAUSS
+ VO_NEG = -14.0 STAT -14 -10 :GAUSS
+ RO = 50.0 STAT 20 500 :GAUSS
...
```

Device Types

Certain properties are mandatory for each device type. These properties and pin names are listed below for each of the specific types. If you want to use the VeriBest delivered symbols for macromodels (Bridges, DIACs, Operational Amplifiers, SCRs, TRIACs, Voltage Comparators, and Voltage Regulators), you must use the pin name and pin numbering convention specified below.

Note: The pin names are in pin sequence order. The pin sequence is fixed for these components and should not be changed.

BJT Model

DESCRIPTION	COMMONLY USED NAMES (shown in appearance frequency)	VeriBest STANDARD PIN NAME
collector	C	C
base	B	B
emitter	E	E

Pin sequence: C B E

Symbol Properties: (required)

- Pin sequence - one per symbol pin
- Pin name - one per symbol pin
- Instance name - one per symbol
- Simulation model - one per symbol
- CLASS - one per symbol

Symbol Properties: (optional)

- DESCRIPTION
- Analog Parameter

SPICE parameters:

- A complete list of the appropriate SPICE parameters can be found in Appendix B.
- Note that SPICE parameters are contained in the device model and not conveyed via symbol properties.

Bridge Model

DESCRIPTION	COMMONLY USED NAMES (shown in appearance frequency)	VeriBest STANDARD PIN NAME
~	~	AC1
~	~	AC2
-	-	NEG
+	+	POS

Pin sequence: AC1 AC2 NEG POS

Symbol Properties: (required)

- Pin sequence - one per symbol pin
- Pin name - one per symbol pin
- Instance name - one per symbol
- Simulation model - one per symbol
- CLASS - one per symbol

Symbol Properties: (optional)

- DESCRIPTION
- Analog Parameter

SPICE parameters:

- A complete list of the appropriate SPICE parameters can be found in Appendix B.
- Note that SPICE parameters are contained in the device model and not conveyed via symbol properties.

DIAC Model

DESCRIPTION	COMMONLY USED NAMES (shown in appearance frequency)	VeriBest STANDARD PIN NAME
MT1	MT1	MT1
MT2	MT2	MT2

Pin sequence: MT1 MT2

Symbol Properties: (required)

- Pin sequence - one per symbol pin
- Pin name - one per symbol pin
- Instance name - one per symbol
- Simulation model - one per symbol
- CLASS - one per symbol

Symbol Properties: (optional)

- DESCRIPTION
- Analog Parameter

SPICE parameters:

- A complete list of the appropriate SPICE parameters can be found in Appendix B.
- Note that SPICE parameters are contained in the device model and not conveyed via symbol properties.

Diode Model

DESCRIPTION	COMMONLY USED NAMES (shown in appearance frequency)	VeriBest STANDARD PIN NAME
anode	A	A
cathode	C	C

Pin sequence: A C

Symbol Properties: (required)

- Pin sequence - one per symbol pin
- Pin name - one per symbol pin
- Instance name - one per symbol
- Simulation model - one per symbol
- CLASS - one per symbol

Symbol Properties: (optional)

- DESCRIPTION
- Analog Parameter

SPICE parameters:

- A complete list of the appropriate SPICE parameters can be found in Appendix B.
- Note that SPICE parameters are contained in the device model and not conveyed via symbol properties.

JFET Model

DESCRIPTION	COMMONLY USED NAMES (shown in appearance frequency)	VeriBest STANDARD PIN NAME
drain	D	D
gate	G	G
source	S	S

Pin sequence: D G S

Symbol Properties: (required)

- Pin sequence - one per symbol pin
- Pin name - one per symbol pin
- Instance name - one per symbol
- Simulation model - one per symbol
- CLASS - one per symbol

Symbol Properties: (optional)

- DESCRIPTION
- Analog Parameter

SPICE parameters:

- A complete list of the appropriate SPICE parameters can be found in Appendix B.
- Note that SPICE parameters are contained in the device model and not conveyed via symbol properties.

MESFET Model

DESCRIPTION	COMMONLY USED NAMES (shown in appearance frequency)	VeriBest STANDARD PIN NAME
drain	D	D
gate	G	G
source	S	S

Pin sequence: D G S

Symbol Properties: (required)

- Pin sequence - one per symbol pin
- Pin name - one per symbol pin
- Instance name - one per symbol
- Simulation model - one per symbol
- CLASS - one per symbol

Symbol Properties: (optional)

- DESCRIPTION
- Analog Parameter

SPICE parameters:

- A complete list of the appropriate SPICE parameters can be found in Appendix B.
- Note that SPICE parameters are contained in the device model and not conveyed via symbol properties.

MOSFET Model

DESCRIPTION	COMMONLY USED NAMES (shown in appearance frequency)	VeriBest STANDARD PIN NAME
(3-Terminal)		
drain	D	D
gate	G	G
source	S	S
(4-Terminal)		
drain	D	D
gate	G	G
source	S	S
body	B	B

Pin sequence: D G S B

Symbol Properties: (required)

- Pin sequence - one per symbol pin
- Pin name - one per symbol pin
- Instance name - one per symbol
- Simulation model - one per symbol
- CLASS - one per symbol

Symbol Properties: (optional)

- DESCRIPTION
- Analog Parameter

SPICE parameters:

- A complete list of the appropriate SPICE parameters can be found in Appendix B.
- Note that SPICE parameters are contained in the device model and not conveyed via symbol properties.

Operational Amplifiers

DESCRIPTION	COMMONLY USED NAMES (shown in appearance frequency)	VeriBest STANDARD PIN NAME
inverting input	-IN INVERTING INPUT -INPUT	IN-
	IN- - IN(-) INV.INPUT INPUT	
noninverting	+IN NON-INVERTING INPUT +INPUT	IN+
output	OUT OUTPUT	OUT
positive supply voltage	V+ +VCC VCC +VS VCC+ VDD	VCC
negative supply voltage	V- -VCC -VS VEE	VEE
offset adjust	BALANCE BAL VOS ADJ. OFFSET NULL	BAL BAL1 BAL2
frequency compensation	COMP COMPENSATION FREQ COMP	COMP COMP1 COMP2
current set	ISET BIAS	ISET
ground	GND	GND

Pin sequence:IN- IN+ OUT V+ V- [BAL1 BAL2] [COMP] [COMP1 COMP2] [ISET] [GND]

Note: Pin names shown in square brackets are optional based on the OpAmp symbol used (that is, 5-pin, 7-pin, etc.).

Symbol Properties: (required)

- Pin sequence - one per symbol pin
- Pin name - one per symbol pin
- Instance name - one per symbol
- Simulation model - one per symbol
- CLASS - one per symbol

Symbol Properties: (optional)

- DESCRIPTION
- Analog Parameter

SCR Model

DESCRIPTION	COMMONLY USED NAMES (shown in appearance frequency)	VeriBest STANDARD PIN NAME
anode	A	A
gate	G	G
cathode	K	K

Pin sequence: A G K

Symbol Properties: (required)

- Pin sequence - one per symbol pin
- Pin name - one per symbol pin
- Instance name - one per symbol
- Simulation model - one per symbol
- CLASS - one per symbol

Symbol Properties: (optional)

- DESCRIPTION
- Analog Parameter

TRIAC Model

DESCRIPTION	COMMONLY USED NAMES (shown in appearance frequency)	VeriBest STANDARD PIN NAME
MT1	MT1 cathode	MT1
MT2	MT2 anode	MT2
gate	G gate	G

Pin sequence: MT1 MT2 G

Symbol Properties: (required)

- Pin sequence - one per symbol pin
- Pin name - one per symbol pin
- Instance name - one per symbol
- Simulation model - one per symbol
- CLASS - one per symbol

Symbol Properties: (optional)

- DESCRIPTION
- Analog Parameter

Voltage Comparators

DESCRIPTION	COMMONLY USED NAMES (shown in appearance frequency)	VeriBest STANDARD PIN NAME
inverting input	-INPUT INVERTING INPUT -IN -	IN-
noninverting input	+INPUT NONVERTING INPUT +IN +	IN+
output	OUT OUTPUT QOUTPUT /QOUTPUT	OUT
positive supply voltage	V+ +VS VCC VCC+ VDD VS+	VCC
negative supply voltage	V- -VS VCC- VS- VEE	VEE
offset adjust	BALANCE BAL	BAL BAL1 BAL2
current set	ISET BIAS	ISET
ground	GND	GND
latch	LATCH	LATCH
strobe	STROBE STB	STB

Pin sequence:IN- IN+ OUT V+ V- [BAL1 BAL2] [ISET] [GND] (LATCH) [STB]

Note: Pin names shown in square brackets are optional based on the voltage comparator symbol used (5-pin, 7-pin, etc.).

Symbol Properties: (required)

- Pin sequence - one per symbol pin
- Pin name - one per symbol pin
- Instance name - one per symbol
- Simulation model - one per symbol
- CLASS - one per symbol

Symbol Properties: (optional)

- DESCRIPTION
- Analog Parameter

Voltage Regulators

DESCRIPTION	COMMONLY USED NAMES (shown in appearance frequency)	VeriBest STANDARD PIN NAME
input voltage	VIN VC	VIN
output voltage	VOUT VO	OUT
adjust	ADJUST ADJ	ADJ
ground	GND	GND
frequency compensation	COMP COMPENSATION FREQ COMP	COMP

Pin Sequence: VIN OUT ADJ (or GND) [COMP]

Note: There are nonstandard voltage regulators with many specific pins. In such cases, the pin names are taken directly from the datasheet (or datasheets, if there are many manufacturers) according to appearance frequency.

Note: Pin names shown in square brackets are optional based on the voltage regulator symbol used (3-pin, 4-pin, 5-pin).

Symbol Properties: (required)

- Pin sequence - one per symbol pin
- Pin name - one per symbol pin
- Instance name - one per symbol
- Simulation model - one per symbol
- CLASS - one per symbol

Symbol Properties: (optional)

- DESCRIPTION
- Analog Parameter

Appendix B
SPICE Parameters

Detailed below are the appropriate SPICE parameters for the following device types:

D	Diode
NPN	NPN BJT
PNP	PNP BJT
NJF	N-Channel JFET
PJF	P-Channel JFET
NMES	N-Channel MESFET
PMES	P-Channel MESFET
NMOS	N-Channel MOSFET
PMOS	P-Channel MOSFET
R	Resistor
C	Capacitor
L	Inductor

Diode Model

SPICE parameters: (DIODE)

AF = 1.00E+00	
BV = Infinite	*VOLTS
CJO = 0.00E+00	*FARADS
EG = 1.11E+00	*ELECTRON VOLTS
FC = 5.00E-01	
IS = 1.00E-14	*AMPS
KF = 0.00E+00	
M = 5.00E-01	
N = 1.00E+00	
RS = 0.00E+00	*OHMS
TT = 0.00E+00	*SECONDS
VJ = 1.00E+00	*VOLTS
XTI = 3.00E+00	

BJT Model

SPICE parameters: (NPN and PNP)

AF=1.00E+00	
BF=1.00E+02	
BR=1.00E+00	
CJC=0.00E+00	*FARAD
CJE=0.00E+00	*FARAD
CJS=0.00E+00	*FARAD
EG=1.11E+00	*ELECTRONVOLTS
FC=5.00E-01	
IKF=Infinite	*AMPS
IKR=Infinite	*AMPS
IRB=Infinite	*AMPS
IS=1.0E-16	*AMPS
ISC=0.00E+00	*AMPS
ISE=0.00E+00	*AMPS
ITF=0.00E+00	*AMPS
KF=0.00E+00	
MJC=3.30E-01	
MJE=3.30E-01	
MJS=0.00E+00	
NC=2.00E+00	
NE=1.50E+00	
NF=1.00E+00	
NR=1.00E+00	
PTF=0.00E+00	*DEGREES
RB=0.00E+00	*OHMS
RBM=0.00E+00	*OHMS
RC=0.00E+00	*OHMS
RE=0.00E+00	*OHMS
TF=0.00E+00	*SEC
TR=0.00E+00	*SEC
VAF=Infinite	*VOLTS
VAR=Infinite	*VOLTS
VJC=7.50E-01	*VOLTS
VJE=7.50E-01	*VOLTS
VJS=7.50E-01	*VOLTS
VTF=Infinite	*VOLTS
XCJC=1.00E+00	
XTB=0.00E+00	
XTF=0.00E+00	
XTI=3.00E+00	

JFET Model

SPICE parameters: (NJF and PJF)

AF = 1.00E+00	
BETA = 1.00E-04	* A/V**2
CGD = 0.00E+00	* FARADS
CGS = 0.00E+00	* FARADS
FC = 5.00E-01	
IS = 1.00E-14	* AMPS
KF = 0.00E+00	
LAMBDA = 0.00E+00	* 1/VOLTS
PB = 1.00E+00	* VOLTS
RD = 0.00E+00	* OHMS
RS = 0.00E+00	* OHMS
VTO = -2.00E+00	* VOLTS
M = 5.00E-01	

MESFET Model

SPICE parameters: (NMES and PMES)

LEVEL = 1	*Mesfet model selector
RD = 0	*ohms,Parasitic drain resistance
RG = 0	*ohms,Parasitic gate resistance
RS = 0	*ohms,Parasitic sourceresistance
RB = 0	*ohms, Parasitic bulk resistance
RSHDS = 0	*ohms/sq,Parasitic sheet resistance for source & drain
RSHG = 0	*ohms/sq,Parasitic sheet resistance for gate
RSHB = 0	*ohms/sq, Parasitic sheet resistance for bulk
TRD1 = 0	*1/deg, 1st order temperature coefficient for RD
TRD2 = 0	*1/deg**2, 2nd order temperature coefficient for RD
TRG1 = 0	*1/deg, 1st order temperature coefficient for RG
TRG2 = 0	*1/deg**2, 2nd order temperature coefficient for RG
TRS1 = 0	*1/deg, 1st order temperature coefficient for RS
TRS2 = 0	*1/deg**2, 2nd order temperature coefficient for RS
TRB1 = 0	*1/deg, 1st order temperature coefficient for RB
TRB2 = 0	*1/deg**2, 2nd order temperature coefficient for RB
TRSHDS1 = 0	*1/deg, 1st order temperature coefficient for RSHDS
TRSHDS2 = 0	*1/deg**2, 2nd order temperature coefficient for RSHDS
TRSHG1 = 0	*1/deg, 1st order temperature coefficient for RSHG
TRSHG2 = 0	*1/deg**2, 2nd order temperature coefficient for RSHG
TRSHB1 = 0	*1/deg, 1st order temperature coefficient for RSHB
TRSHB2 = 0	*1/deg**2, 2nd order temperature coefficient for RSHB
CGDPX = 0	*F, Parasitic capacitance between external g-d nodes
CGSPX = 0	*F, Parasitic capacitance between external g-s nodes
CGPX = 0	*F/width, Parasitic cap/width,

	between external g-s & g-d nodes
CDSPX = 0	*F/width, Parasitic capacitance /width between external d-s node
CGDPI = 0	*F, Parasitic capacitance between internal g-d nodes
CGSPI = 0	*F, Parasitic capacitance between internal g-s nodes
CGPI = 0	*F/width, Parasitic cap/width between internal g-s & g-d nodes
CDSPI = 0	*F/width, Parasitic capacitance /width between internal d-s node
CBD = 0	*F, Parasitic capacitance between internal b-d nodes
CBS = 0	*F, Parasitic capacitance between internal b-s nodes
CB = 0	*F/area, Parasitic cap/area, between internal b-s & b-d nodes
TCB1 = 0	*1/deg, 1st order temperature coefficient for bulk capacitance
TCB2 = 0	*1/deg**2, 2nd order temperature coefficient for bulk capacitance
CGD = 0	*F, Zero bias capacitance for g-d bottom junction diode
CGS = 0	*F, Zero bias capacitance for g-s bottom junction diode
CJ = 0	*F/area, Zero bias cap/area, for g-d and g-s bottom junction diode
MJ = .5	*Grading coefficient
PB = 1	*Volts, Junction potential for g-d & g-s bottom diode capacitances
FCB = .5	*Forward bias junction cap coeff for g-d & g-s bottom junctions
CGDSW = 0	*F, Zero bias capacitance for g-d sidewall junction diode
CGSSW = 0	*F, Zero bias capacitance for g-s sidewall junction diode
CJSW = 0	*F/peri, Zero bias cap /periphery, for g-d & g-s sidewall junction diode
MJSW = .5	*Grading coefficient for g-d & g-s sidewall diode capacitances
PBSW = 1	*Volts, Junction potential for g-d and g-s sidewall diode cap
FCBSW = .5	*Forward bias junction cap coeff for g-d & g-s sidewall junctions
TCJ1 = 0	*1/deg, 1st order temp coeff for g-d & g-s bottom junction cap

TCJ2 = 0	*1/deg**2, 2nd order temp coeff for g-d & g-s bottom junction cap
TCJSW1 = 0	*1/deg, 1st order temp coeff for g-d & g-s sidewall junction cap
TCJSW2 = 0	*1/deg**2, 2nd order temp coeff for g-d & g-s sidewall junction cap
IS = 1E-14	*Amps, Bottom junction leakage current for g-d & g-s diodes
JS = 0	*A/area, Bottom junction leakage current/area for g-d & g-s diodes
ISSW = 0	*Amps, Sidewall junction leakage current for g-d & g-s diodes
JSSW = 0	*A/peri,Sidewall junction leakage current/area for g-d & g-s diode
N = 1	*Emission coefficient
BV = 0	*Volts, Reverse breakdown voltage for g-d & g-s diodes
TTD = 0	*sec, Transit time for g-d diode
TTS = 0	*sec, Transit time for g-s diode
EG = 1.42	*eV, Activation energy for g-d & g-s diodes
XTI = 2	*Temperature exponent for leakage current for g-d & g-s diodes
TBV1 = 0	*1/deg, 1st order tmp coeff for g-d & g-s diode breakdown voltage
TBV2 = 0	*1/deg**2, 2nd order tmp coeff for g-d & g-s diode breakdown volt
RIN = 0	*ohms/width, Input series resistance per unit width
CDGF = 0	*F/width, Feedback capacitance from g-d per unit width
RDSS = 0	*ohms/width, Output series resistance per unit width
CDSS = 0	*F/width, Output series capacitance per unit width
CGD0 = 0	*F, Zero bias g-d capacitance of the intrinsic MESFET
CGS0 = 0	*F, Zero bias g-s capacitance of the intrinsic MESFET
CG0 = 0	*F/area, Zero bias g-s & g-d cap /gate_area of the intrinsic MESFET
M = .5	*Grading coefficient for g-d and

	g-s intrinsic capacitances
VBI = 1	*Volts, Junction potential for g-d & g-s intrinsic capacitances
FC = .5	*Forward bias junction cap coefficient for g-d & g-s intrinsic cap
TCG1 = 0	*1/deg, 1st order tmp coeff for g-d & g-s intrinsic capacitances
TCG2 = 0	*1/deg**2, 2nd order tmp coeff for g-d & g-s intrinsic caps
CGDN = 0	*F, Normal bias g-d capacitance of the intrinsic MESFET
CGSN = 0	*F, Normal bias g-s capacitance of the intrinsic MESFET
CGN = 0	*F/area, Normal bias g-s & g-cap/gate area of the intrinsic MESFET
TCGN1 = 0	*1/deg, 1st order tmp coeff for normal bias g-d & g-s intrinsic cap
TCGN2 = 0	*1/deg**2, 2nd order tmp coeff, normal bias g-d & g-s intrinsic cap
VTO = -2	*Volts, Pinch-off voltage
K1 = 0	*sqrt(Volts), Pinch-off voltage increase
K2 = 0	*Pinch-off voltage increase
TVT1 = 0	1/deg, 1st order temperature coefficient for pinch-off voltage
TVT2 = 0	1/deg**2, 2nd order temperature coefficient for pinch-off voltage
TAU = 0	*sec, Transit time under the gate
ALPHA = 2	*1/V, Saturation voltage parameter
BETA = 1E-4	*A/V**2, Transconductanc parameter
BETATEMP = -1.5	*Temperature exponent for BETA
DELTAEFF = .2	*Volts, Transition voltage range for charge model
DELTA = .5	*Volts, Transition voltage range for charge model
QOPT = 1	*Charge model selection
PMAX = 0	*W, maximum noise dissipation
LAMBDA = 0	*1/V, Channel length modulation parameter
A0 = 836	*V**2, Zero order coefficient in the cubic equation

A1 = 152.8	*V, 1st order coefficient in the cubic equation
A2 = -12.93	*2nd order coefficient in the cubic equation
A3 = -2.33	*1/V, 3rd order coefficient in the cubic equation
A5 = 0	*sec/V, Proportionality constant for transit time
VDSO = 6	*Volts, VDS at which A0 thru A3 are determined.
GAMMA = 0	*1/V, Coefficient of pinch-off change
B = 0	*1/V, Effective doping parameter

MOSFET Model

SPICE parameters: (NMOS and PMOS)

AF = 1.00E+00	
CBD = 0.00E+00	* F/M**2
CBS = 0.00E+00	* F/M**2
CGBO = 0.00E+00	* F/M
CGDO = 0.00E+00	* F/M
CGSO = 0.00E+00	* F/M
CJ = 0.00E+00	* F/M**2
CJSW = 0.00E+00	* F/M
DELTA = 0.00E+00	
ETA = 0.00E+00	
FC = 5.00E-01	
GAMMA = 0.00E+00	* V**(1/2)
IS = 1.00E-14	* A/M**2
JS = 0.00E+00	* A/M**2
KAPPA = 1.00E+00	
KF = 0.00E+00	
KP = 2.00E-05	* A/V**2
LAMBDA = 0.00E+00	* M/V
LD = 0.00E+00	* M
LEVEL = 1	
MJ = 5.00E-01	
MJSW = 3.30E-01	
NEFF = 1.00E+00	
NFS = 0.00E+00	* 1/CM**2
NSS = 0.00E+00	* 1/CM**2
NSUB = 0.00E+00	* 1/CM**3
PB = 8.00E-01	* VOLTS
PHI = 6.00E-01	* VOLTS
RD = 0.00E+00	* OHMS
RS = 0.00E+00	* OHMS
RSH = 0.00E+00	* OHMS/M**2
THETA = 0.00E+00	* 1/V
TOX = 0.00E+00	* M
TPG = 1.00E+00	
UCRIT = 1.00E+04	* V/CM
UEXP = 0.00E+00	
UO = 6.00E+02	* CM**2/V-S
UTRA = 0.00E+00	
VMAX = 0.00E+00	* M/SEC
VTO = 0.00E+00	* VOLTS
XJ = 0.00E+00	* M
XQC = 1.00E+00	

Resistor Model

SPICE parameters:

TC1
TC2
RSH
DEFW
NARROW
PMAX

Capacitor Model

SPICE parameters:

CJ
DEFW
NARROW
VOMAX

Inductor Model

SPICE parameter:

IMAX

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W