An Introduction to In-System Reprogramming (ISR™) with the Ultra37000™

Introduction

This application note provides an introduction to the Ultra37000™ family of In-System Reprogrammable™ (ISR™) CPLDs. The Ultra37000 ISR CPLD family upgrades the FLASH370i™ CPLD family of devices and provides higher density and greater performance. Additionally there are many new features included in the Ultra37000 such as Boundary Scan capability defined in the IEEE 1149.1 JTAG standard, full 3.3V V_{CC} operation, individual output slew rate control, product term clocking capability, logic block low-power mode, and in system programming at the supply voltage with fast programming times. Like the FLASH370i, the Ultra37000 devices can be reprogrammed in the user's system. For the purposes of this application note the name Ultra37000 will be interpreted to mean both the Ultra37000 and Ultra37000V family of devices. The Ultra37000V family is identical to the Ultra37000 but operates at 3.3V. Many of the issues introduced in this application note are explained in detail in the application note "Designing with Cypress In-System Reprogrammable (ISR) CPLDs for PC Cable Programming."

In-System Reprogrammability is the capability of a programmable device to be reprogrammed after being soldered onto a printed circuit board. This allows the configuration and functionality of a device, and therefore the electronic system in which it is contained, to be modified after the system has completed the manufacturing cycle. Reprogramming can happen at any time, such as prior to the shipment of the system or product, in the form of a field upgrade to provide additional capabilities and features, to correct previous problems, or during actual system operation so that a different function or algorithm is implemented.

In many cases, ISR capability is used only to simplify the manufacturing cycle, by eliminating the handling of a traditional programmable logic device (PLD) to facilitate programming. With an ISR device, one handling step can be removed if desired. Additionally, ISR devices can be reprogrammed again and again as required.

Several topics and issues are introduced in this application note. These are: compatibility of the the Ultra37000 devices with FLASH370i devices, the ISR interface of the Ultra37000 devices compared to the FLASH370i devices, the JTAGen pin of the Ultra37000 devices compared to the ISRen pin of FLASH370i devices, the features of ISR, the Ultra37000 pin descriptions and pinouts, the ISR programming options, the ISR programming interface, and the Ultra37000 ISR Kit.

Compatibility of the Ultra37000 Devices With FLASH370i Devices

The Ultra37000 is functionally a superset of the FLASH370i. ranging from 32 macrocells to 512 macrocells. For those members of the family that overlap the FLASH370i, from 32 macrocells to 128 macrocells, the device pinouts are identical and the functionality can be identical if the extra features of the Ultra37000 are unused. The Ultra37000 features the same number and superior allocation of product terms and the same robust interconnect that provides the same excellent routability as the FLASH370i. The programmable interconnect matrix (PIM) architecture is the same as the FLASH370i thereby providing the same simple predictable timing for all members of the family.

The ISR Interface of the Ultra37000 Devices and the FLASH370i Devices

The 4-pin ISR programming interface on the Ultra37000 devices is identical to the FLASH370i devices. The Ultra37000 devices use the JTAG naming convention of TDI, TDO, TMS, and TCK whereas the FLASH370i devices call these same pins SDI, SDO, SMODE, and SCLK respectively. The reason for this different naming convention is that the FLASH370i devices do not include JTAG Boundary Scan capability even though ISR programming conforms to the JTAG standard.

The JTAGen Pin of the Ultra37000 Devices and the ISRen Pin of the FLASH370i Devices

The ISR interface is provided in one of two modes. These two modes are termed "single-function" and "dual-function." The difference between these two modes is that the ISR interface pins are either standalone, single-function, or share their functionality with an I/O pin, dual-function. For the Ultra37000 dual-function devices the JTAGen pin controls the function of the dual-function pins. A TTL HIGH value decodes the JTAG pin function and a TTL LOW value decodes the I/O pin function. The ISRen pin performs the same function for the FLASH370i devices, additionally providing the 12V programming voltage needed to program the device. The difference is that the ISRen pin must be driven to a supervoltage level, 12V, for the JTAG function of the dual-function mode pin to be selected. A TTL HIGH or LOW values selects the I/O function. The JTAGen pin only requires a TTL level. It can tolerate the supervoltage level but sees this level as TTL HIGH. This feature of the JTAGen pin allows replacement of FLASH370i devices with Ultra37000 devices. There are no input current requirements for the JTAGen pin as there are for the ISRen pin for the FLASH370i devices. For the single-function mode Ultra37000 devices, there is no need for the JTAGen pin so this pin does not exist in the single-function mode device pinouts. In the single-function mode devices, the JTAG interface is permanently enabled.

ISR Programming of the Ultra37000 Devices and the FLASH370i Devices

The identical ISR programming interface between the Ultra37000 and the FLASH370i enables both devices to be programmed through the ISR cable connected to the parallel port of a PC. No board changes are required when migrating

from a FLASH370i device to a Ultra37000 device unless the I/O function on the dual-function pins is used and the default state of the JTAGen pin is not in the LOW state.

Converting from FLASH370i to Ultra37000 Devices

If the FLASH370i design uses the I/O function of the dual-function pins then the user must make sure the JTAGen pin is forced to a TTL LOW when the device is replaced by a Ultra37000 device. Without this pin driven LOW the dual-function pin will take the JTAG function instead of the I/O function. To keep the default function on the dual function pins as the I/O function, a weak pull-down device has been employed. This is sufficient to hold the pin LOW in most situations, although there could be situations where a board may contain FLASH370i and Ultra37000 devices in the same chain where the pin may not be held in the LOW state. There are various methods for driving this pin LOW externally. These are further explained in the application note “Designing with Cypress In-System Reprogrammable (ISR) CPLDs for PC Cable Programming.” This pull-down is the reason why the extra parameter I_{JTAG} has been added to the datasheet of dual-function Ultra37000 devices.

Bus-hold on the Ultra37000

The Ultra37000 incorporates the same bus-hold structures as the FLASH370i. The bus-hold latch eliminates the need for connecting unused inputs and I/O pins to a supply by providing an improved version of an internal pull-up resistor. The bus-hold structure provides a weak internal pull-up or pull-down, depending upon the last driven state on the pin. See the application note “Understanding Bus-Hold—A Feature of Cypress CPLDs” on the Cypress website for more information on bus-hold. There are two important difference between bus-hold on the Ultra37000 and on the FLASH370i.

For the first difference, the bus-hold latches are disconnected from the JTAG pins when the JTAGen pin is HIGH and connected when the JTAGen pin is LOW instead of being permanently enabled on the JTAG pins. The reason for removal of the bus-hold latch when the dual-function pins are functioning as JTAG pins is to prevent problems with DC current loading of the JTAG drivers during either ISR programming or JTAG Boundary Scan testing when there are many devices in the ISR chain. For all dual function members of the Ultra37000 family, except Ultra37256P160 early silicon, the bus-hold latch is replaced with a pull-down device. For later Ultra37256P160 silicon the pull-down device is also employed. The pull-down device is used to hold the JTAGen pin LOW when programming completes to that the I/O function is selected on the dual function pins as previously mentioned.

Regarding the second difference, the single function mode devices do not incorporate the bus-hold latches on the JTAG pins since there is no I/O function on these pins. For a summary of bus-hold connections for the Ultra37000 see *Tables 2*, *3*, and *4*.

Global Bus-hold Disable

There is a programming bit on the Ultra37000 that controls whether the bus-hold feature is enabled or disabled. This option is available through the *Warp*™ GUI. In most cases it is good to leave the bus-hold latches enabled but some applications may work better with it disabled. This is especially important for FLASH370 (non-i) designs that are converted to the Ultra37000 devices since the bus-hold can affect signal levels when weak resistor pull-ups or pull-downs are involved. The default state of this bit is HIGH, unprogrammed, which enables all bus-hold latches in the device.

In the FLASH370i devices a HIGH value in a JEDEC map means that the bit is programmed and a LOW value in a JEDEC map means that the bit is unprogrammed. In the Ultra37000 devices just the opposite is true. A LOW value in a JEDEC map means that the bit is programmed and a HIGH value in a JEDEC map means that the bit is unprogrammed.

Pull-ups on the JTAG Pins TDI, TMS

The Ultra37000 incorporates internal pull-ups on the JTAG pins TDI and TMS pins as required from the IEEE 1149.1 specification. This is to ensure that if a solder fault results in an open circuit on a JTAG pin, the internal TAP controller in the device will enter the predictable, safe BYPASS instruction. For the dual-function mode devices, those with a JTAGen pin, the pull-up resistors are present only when the JTAG interface is enabled, JTAGen is HIGH.

Enabling ISR Functions for the Ultra37000

Unlike the FLASH370i, the Ultra37000 does not require any supervoltages (external 12.0V) to enable ISR operations such as programming, erasing, or reading the IDCODE. To guard against accidentally placing the device into an ISR operation, there is a special Enable ISR register within the device that needs to be loaded with an enabling HIGH value before any ISR operation can be performed. This requires a JTAG instruction to be loaded into the instruction register and assures that there is no possibility of accidentally changing the programming of the device during any JTAG operation.

Overview of the Ultra37000 ISR Features

Table 1 shows the packages offered for the Ultra37000 device family.

Table 1. Ultra37000 Family Offering

Device	#Macro-cells	#Pins	Pkg	Function
Ultra37032/V	32	44	TQFP PLCC	dual
Ultra37064/V	64	44	TQFP PLCC	dual
Ultra37064/V	64	84	PLCC	dual
Ultra37064/V	64	100	TQFP	single
Ultra37128/V	128	84	PLCC	dual
Ultra37128/V	128	100	TQFP	single
Ultra37128/V	128	160	TQFP	dual
Ultra37192/V	192	160	TQFP	single
Ultra37256/V	256	160	TQFP	dual
Ultra37256/V	256	208	PQFP	single
Ultra37256/V	256	256	BGA	single
Ultra37384/V	384	208	PQFP	single
Ultra37384/V	384	256	BGA	single
Ultra37512/V	512	208	PQFP	single
Ultra37512/V	512	256	BGA	single
Ultra37512/V	512	352	BGA	single

For those members of the Ultra37000 that are superset pin-compatible replacements for the FLASH370i, the single- and dual-function offerings are identical to the FLASH370i devices.

As with the FLASH370i, cascading of devices in a chain is also allowed in the Ultra37000 ISR family of CPLDs. Ultra37000 CPLDs can be cascaded homogeneously, with other FLASH370i devices, or with other devices that support the JTAG interface. Ultra37000 devices are cascaded by connecting the TDO pin of one device to the TDI pin of the next device, while also connecting the TCK, TMS, and JTAGen (if a dual-function device) pins of all devices in parallel, as provided by the JTAG specification.

As with the FLASH370i, a security bit is included and can be programmed to prevent the reading or verifying of a Ultra37000 device. The IDCODE and the USERCODE are still available from the JTAG port even with the security bit programmed.

Ultra37000 Pin Descriptions

Tables 2, 3, and *4* describe the functionality of all of the ISR pins for the Ultra37000 devices. *Tables 2* and *3* are for the Ultra37000 devices with dual-function ISR pins and *Table 4* is for devices with single-function ISR pins. *Tables 2* and *3* describe the pin functionality when the JTAGen pin is HIGH and LOW, respectively. The dedicated I/O pins enter the high-impedance state (three-state) when either the instruction in the instruction register is the ISR enable instruction upon entering the UpdateIR TAP controller, or the ISR enable register stores a HIGH value.

Table 2. Dual-Function Pin Descriptions (JTAGen = HIGH; ISR Interface Enabled)

Pin	Mode	Description
JTAGen	Input	Set to HIGH chooses the ISR function on the dual-function pins; the bus-hold structure is connected for the Ultra37256P160 early silicon devices. For Ultra37256P160 later silicon and Ultra37128 devices and smaller the bus-hold latch has been replaced with a pull-down device.
TCK (I/O)	Input	I/O three-stated; functions as TCK input for the ISR interface. No bus-hold structure is connected.
TMS (I/O)	Input	I/O three-stated; functions as TMS input for the ISR interface. No bus-hold structure is connected, however an internal pull-up resistor is connected.
TDI (I/O)	Input	I/O three-stated; functions as TDI input for the ISR interface. No bus-hold structure is connected, however an internal pull-up resistor is connected.
TDO (I/O)	Output	Functions as TDO output for the ISR interface; the output is enabled when the JTAG state machine is in the Shift-IR or Shift-DR states and is three-stated in the other states as defined by JTAG. No bus-hold structure is connected.
Other I/Os	High-Z/IO	I/O three-stated if the instruction in the instruction register is the ISR enable instruction or the ISR enable register stores a HIGH value else the I/O functions according to how the device is programmed. The bus-hold structure is connected.
Other Inputs	Input	Unused if the instruction in the instruction register is the ISR enable instruction or the ISR enable register stores a HIGH value else normal input function. The bus-hold structure is always connected.
Other I/CLKs	I/CLK	Unused if the instruction in the instruction register is the ISR enable instruction or the ISR enable register stores a HIGH value else normal input function. The bus-hold structure is always connected.

Table 3. Dual-Function Pin Descriptions (JTAGen = LOW; ISR Interface Disabled)

Pin	Mode	Description
JTAGen	Input	Set to LOW chooses the I/O function on the dual-function pins and disables the ISR interface; the bus-hold structure is connected for the Ultra37256P160 early silicon devices. For Ultra37128 devices and smaller the bus-hold latch has been replaced with a pull-down device.
I/O (TCK) I/O (TMS) I/O (TDI) I/O (TDO)	I/O I/O I/O I/O	Normal I/O function; each of these pins functions according to how the device is programmed; the bus-hold structure is connected; the internal pull-up resistors on the TDI and TMS pins are disconnected; the JTAG state machine returns to the “Test-Logic-Reset” state and does not interfere with the normal operation of the device.
Other I/Os	I/O	Normal I/O function according to how the device is programmed. The bus-hold structure is connected.
Other Inputs	Input	Normal input function; the bus-hold structure is connected.
Other I/CLKs	I/CLK	Normal input/clock function; the bus-hold structure is connected.

Table 4. Single-Function Pin Descriptions

Pin	Mode	Description
TCK	Input	Functions as TCK input for the ISR interface; the bus-hold structure is not connected.
TMS	Input	Functions as TMS input for the ISR interface; the bus-hold structure is not connected, however an internal pull-up resistor is connected.
TDI	Input	Functions as TDI input for the ISR interface; the bus-hold structure is not connected, however an internal pull-up resistor is connected.
TDO	Output	Functions as TDO output for the ISR interface; the output is enabled when the JTAG state machine is in the Shift-IR or Shift-DR states as defined by JTAG; the bus-hold structure is not connected.
All I/Os	High-Z/IO	Output three-stated if the instruction in the instruction register is the ISR enable instruction upon entry into the Update-IR TAP state or the ISR enable register stores a HIGH value else the I/O functions according to how the device is programmed. The bus-hold structure is connected whether ISR is enabled or not.
All Inputs	Input	Unused if the instruction in the instruction register is the ISR enable instruction or the ISR enable register stores a HIGH value else normal input function. The bus-hold structure is connected whether ISR is enabled or not.
All I/CLKs	I/CLK	Unused if the instruction in the instruction register is the ISR enable instruction or the ISR enable register stores a HIGH value else normal input/clock function. The bus-hold structure is connected whether ISR is enabled or not.

Table 5. ISR Pins for All Packages of the Ultra37000

ISR Pin	PLCC 44-Pin	TQFP 44-Pin	PLCC 84-Pin	TQFP 100-Pin	TQFP 160-Pin37(128/256)	TQFP 160-Pin 37192	PQFP 208-Pin	BGA 256-Pin	BGA 352-Pin
JTAGen	11	5	83	N/A	139	N/A	N/A	N/A	N/A
TCK	7	1	14	1	6	6	7	F2	E2
TMS	19	13	35	26	46	46	59	Y4	AF7
TDI	39	33	72	75	116	116	150	D19	AF20
TDO	27	21	51	50	76	76	98	V16	E24

Table 6. The I/O Function on all Dual-Function-Pin Members of the Ultra37000

ISR Pin	PLCC 44-Pin	TQFP 44-Pin	PLCC 84-Pin	TQFP 160-Pin
TCK	I/O 5	I/O 5	I/O 10	I/O 20
TMS	I/O 13	I/O 13	I/O 26	I/O 52
TDI	I/O 27	I/O 27	I/O 54	I/O 108
TDO	I/O 19	I/O 19	I/O 38	I/O 76

Ultra37000 Pinouts

Table 5 shows the location of the ISR pins for all packages of the Ultra37000 family of devices. *Table 6* shows the dual-function I/O pin for those packages that are dual-function.

Ultra37000 ISR Programming Interface

Although detailed knowledge of the ISR internal architecture is not required for users to design with or program Ultra37000 devices, the basics are provided here for those interested. The IEEE 1149.1 specification requires that the finite state machine called the Test Access Port (TAP) shown in *Figure 1* be implemented for controlling the sequence of operations. Transitions are made on the rising edge of TCK, and the TMS input determines the next state.

Figure 2 shows the ISR internal registers that are linked between the test data input (TDI) and the test data output (TDO). The five ISR internal registers are: the Address Register (AR), the Data Register (DR), the Bypass Register (BR), the Instruction Register (IR), and the ISR Enable Register.

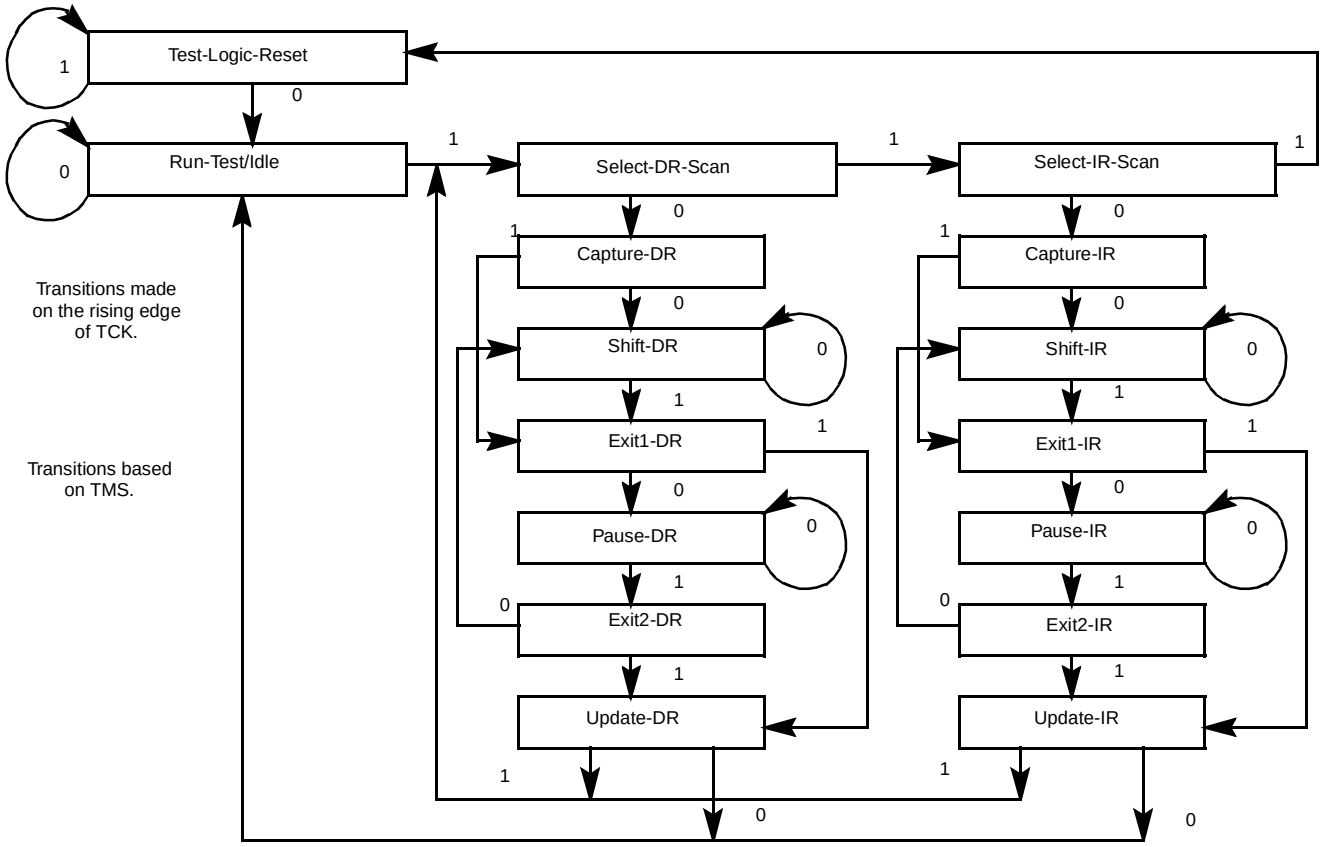

Figure 1. JTAG State Diagram

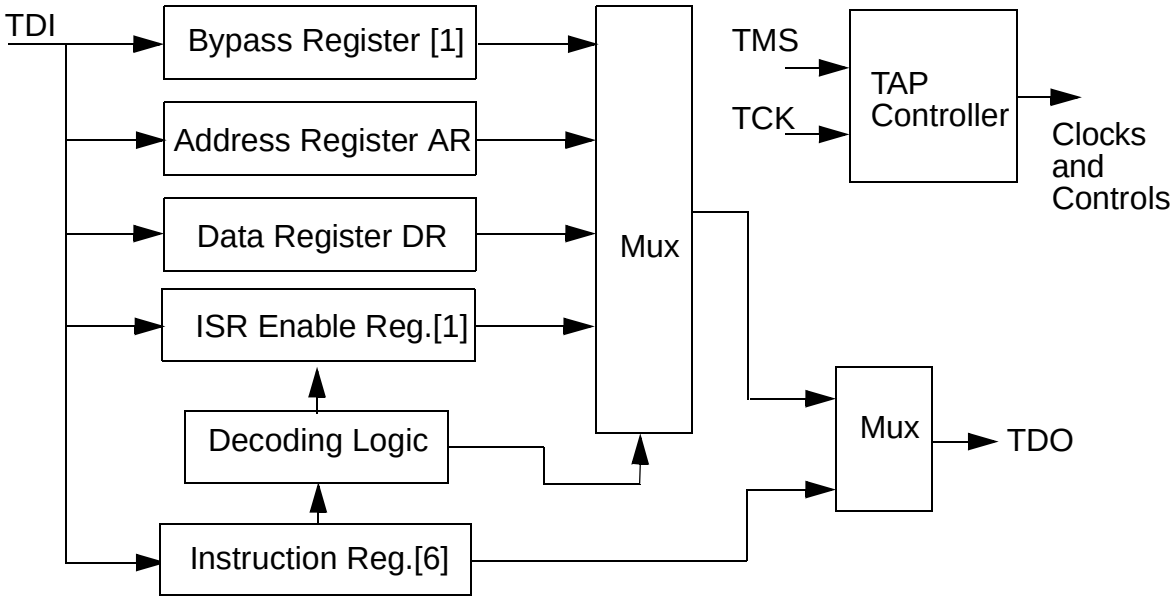

Figure 2. Ultra37000 ISR Interface Registers

The 6-bit instruction register holds the instruction to be executed. The supported instructions and their codes are shown in *Table 7*. The execution of each instruction is beyond the scope of this application note, but the instructions are presented to indicate that the codes are consistent with the IEEE 1149.1 specification, which requires that the EXTEST and BYPASS be assigned the codes with all 0s and 1s, respectively.

Table 7. Ultra37000 ISR Instruction Set

Code	Instruction
000000	EXTEST
001100	ISR enable register
000101	Program / Shift AR
000011	Verify / Shift DR
001000	Bulk Erase Device
111111	Bypass

The AR register defines which row is programmed during a programming pulse. Each row contains hundreds or, on the higher density devices, thousands of bits. The bits to be programmed or left unprogrammed along the row are defined by the pattern shifted into the DR. Programming is achieved by loading the AR register and then the DR register and then programming all desired bits along the chosen row concurrently. After programming, the DR register then receives the programmed or unprogrammed data from the row selected. This data is shifted out and compared to expected data external to the device to determine if the correct data was programmed into the device.

As mentioned previously, the ISR enable register is a single bit that must be loaded with a HIGH value before any ISR operations can be performed. Likewise it must then be loaded with a LOW to discontinue ISR operations.

The single-bit bypass register is used for implementing the bypass mode. This is a requirement of the IEEE 1149.1 standard. Placing a device in Bypass effectively removes the device from the ISR chain by placing a single register between the TDI and TDO pins.

Fast Programming Times

In the Ultra37000, hundreds or thousands of bits in the device are programmed on the same programming pulse. This reduces programming time dramatically. Additionally, programming time is fast because all Ultra37000 devices in a common ISR chain can be concurrently programmed.

Overview of ISR Programming Options

There are four ways of programming Ultra37000 devices. The first is to use a PC with an ISR programming cable and software. The second method is to use existing parallel programmers such as Data I/O. The third method is to program the devices on board via an embedded controller. The fourth method is to program the devices on Automated Test Equipment (ATE). The ISR programming solution for the Ultra37000 is based on the Jam standard.

Jam Programming Support—What is Jam?

Jam is an interpreted language that provides a standard for programming PLDs via the JTAG interface. A full discussion of Jam is beyond the scope of this application note, but a brief discussion of Jam follows. Jam provides a universal platform for programming CPLDs from different silicon vendors. Jam takes advantage of the industry accepted IEEE 1149.1 standard as the programming interface, hence any PLD that incorporates this standard can be supported through Jam.

Jam Implementation

Jam support entails two software programs, which are called the Jam Composer and the Jam Player. The Jam Composer takes a JEDEC file and converts it into a Jam programming file. The Jam programming file is written in the Jam language and contains the algorithm with the proper addresses and data to program the device in the most efficient means possible. The Jam language itself is similar in structure to the Basic language. Statements in a Jam programming file define the transitions in the TAP controller state machine in the PLD and define all aspects of all the ISR operations. The Jam Player program parses the Jam programming file and converts the instructions in this file into actual signals on the JTAG 4-pin serial interface to program the device. It also interprets the output data on the TDO JTAG pin and reports results. The Jam Player for programming through an external cable and PC is written and available on the Cypress web site. The source code can be quickly ported to other embedded processor and test equipment platforms with a simple modification to the I/O portion of the program.

Advantages of Jam

With Jam, any platform (ATE, microprocessor, PC, standalone programmer) incorporating a Jam Player can program devices once a Jam programming file is available for that device. The Jam standard simplifies programming support since support is provided in the Jam programming file only, assuming the Jam player is in place. Because this file is an interpreted language with high level functions and loops, much less space is required to store the Jam file either in a PC or in memory on board if it is desired to program the device via a microcontroller. Updates to programming algorithms is also simplified since only the format of the Jam file needs to be updated. These updates can now be fully controlled by the device vendor.

ISR Programming Using an ISR Cable and PC

For ISR programming via the Ultra37000 ISR cable attached to a PC parallel port, the ISR pins of the Ultra37000 devices are routed to a connector on the printed circuit board. The ISR programming cable is then connected between the parallel port of the PC and this connector. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, erasing, and verifying of the devices.

Parallel Programming Support

The second method for programming Ultra37000 devices is to use the same parallel programmer that is currently being used to program FLASH370i devices. New hardware may not be required for those members of the Ultra37000 that overlap with the FLASH370i devices. Check with third-party programmer vendors regarding hardware requirements.

Embedded Controller Programming Via Jam

The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the user's system. ISR support for any given processor

is available as soon as the Jam Player is available for that particular processor.

ATE Programming Via JAM

The fourth programming option for Ultra37000 devices is to program via ATE. Once the ATE vendor provides Jam support for their equipment, which means providing a working Jam Player, then support for that equipment is available.

The ISR Programming Kit

Separate kits are available for programming the FLASH370i devices and the Ultra37000/V ISR devices. The kits come complete with the following items: the ISR User's Guide, either the ISRPCCABLE or the UltraISRPCCABLE programming cable, the ISR software, and available ISR application notes. *Table 8* shows the devices supported with these ISR cables.

Table 8. ISR Cable Used for Programming

Cable	Devices
ISRPCCABLE(rev 0.03)	FLASH370i, Ultra37000, (Ultra37000V with 5V supply)
UltraISRPCCABLE	Ultra37000, Ultra37000V

The ISRPCCABLE programs FLASH370i devices, Ultra37000 devices, or both FLASH370i and Ultra37000 devices in a common ISR chain. The Ultra37000V can also be programmed with the ISRPCCABLE if a 5V supply is available to power the cable. The UltraISRPCCABLE is designed to program only the Ultra37000 devices including the Ultra37000V devices. This cable does not incorporate a 5V to 12V converter; therefore, it does not program FLASH370i devices.

The ISR User's Guide contains the documentation of how to use the ISR software for programming through an ISR cable connected to the parallel port of a PC. Also included in the ISR User's Guide is a list of error messages that the ISR software generates if problems are encountered.

The ISR programming cable is connected between the parallel port of the PC and the connector on the printed circuit board which contains the Ultra37000 and/or FLASH370i devices.

The ISR software incorporates the Jam composer and Jam Player into a seamless operation with a Windows® GUI.

Other Ultra37000 ISR Application Notes

Please refer to the application notes section on programmable products for more information on the Ultra37000. The Cypress web page URL is http://www.cypress.com.

Conclusion

This application note provides the introductory information to begin designing with the Ultra37000 family of In-System Reprogrammable (ISR) CPLDs. The Ultra37000 ISR CPLD family is a superset replacement for the popular FLASH370i CPLD family while additionally providing improved performance, 3.3-volt power supply operation, extended density to 512 macrocells, and JTAG Boundary Scan. As with the FLASH370i, the Ultra37000 devices offer ISR capability.