Using the Ultra37000™ ISR™ Prototype Board

Introduction

This application note is intended to provide instruction in the use of the Ultra37000™ ISR™ Prototype Board. This board serves two major purposes. First, it provides a board with Cypress Ultra37000 CPLDs already connected to take advantage of In-System Reprogrammability™ (ISR). This allows designers who are unfamiliar with ISR to investigate it as a possible device programming solution. Second, it permits designers who need custom logic to more easily utilize Cypress CPLDs in prototype designs. After programming the Ultra37000 devices on the Ultra37000 ISR Prototype Board, connections can be made between the Ultra37000 ISR Prototype Board and the designer's board using the provided header strips. This gives a designer the ability to verify the functionality of an Ultra37000 CPLD within a system before designing the CPLD into that system.

This application note should familiarize the reader in the use of the Ultra37000 ISR Prototype Board and highlight the board's features. Topics of discussion will include connecting the programming cable, connecting power supplies to the board, using the jumpers on the board, and making connections between the Ultra37000 ISR Prototype Board and other systems.

In-System Reprogrammability allows Complex Programmable Logic Devices (CPLDs) to be reprogrammed after being soldered in place on a printed circuit board. The Ultra37000 ISR Prototype Board is designed to support two Ultra37000 CPLDs. The first device is a 256 macrocell CPLD in a 208-pin PQFP package. The second device, which is already in place on the board, is a 256 macrocell CPLD in a 160-pin TQFP package.

ISR programming of Ultra37000 CPLDs follows the IEEE 1149.1 standard (JTAG). The JTAG interface supports chaining multiple JTAG-compliant devices together and can therefore support programming multiple devices.

Ultra37000 CPLDs support the Jam standard as the solution for ISR programming. Jam is an interpreted language that provides a standard for programming PLDs through the JTAG interface. The Ultra37000 CPLDs on the Ultra37000 ISR Prototype Board are programmed through an ISR cable using the Cypress ISR Programming Software. To learn more about the ISR features of the Ultra37000 family refer to the Cypress application note, "An Introduction to In-System Reprogramming (ISR) with the Ultra37000."

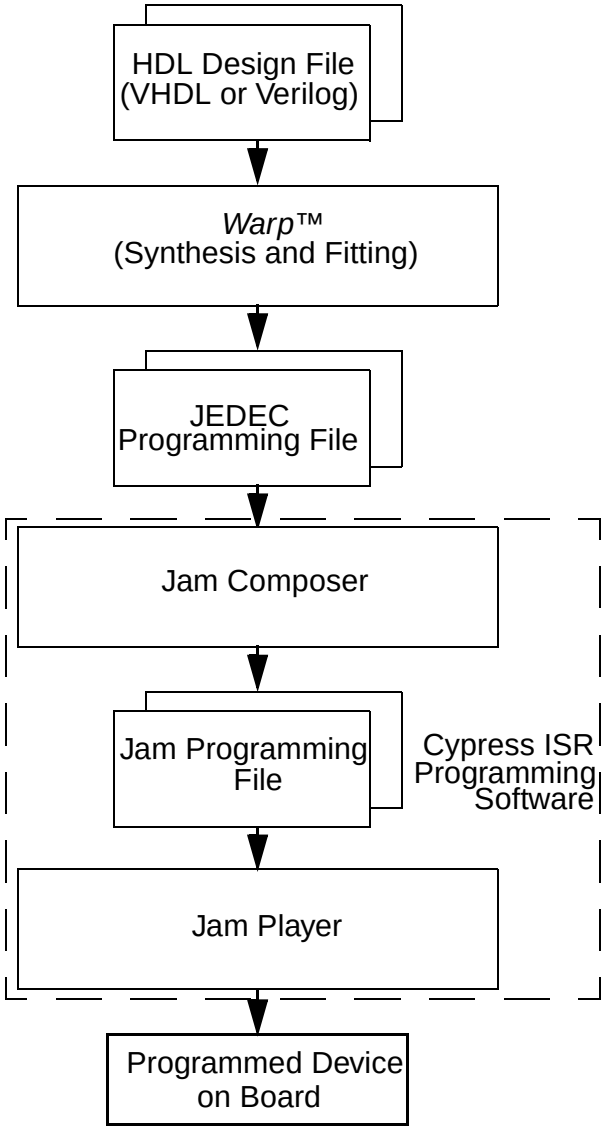

Figure 1. Ultra37000 ISR Design Flow

Ultra37000 ISR Design Flow

In order to use the Ultra37000 ISR Prototype Board, it is important to understand how it fits into the ISR design flow. The basic ISR design flow for Cypress CPLDs is shown in *Figure 1*. Designs are typically specified in VHDL or Verilog code. This code can either be written by the designer or generated from schematics. Once the code for the design is complete, it is synthesized into logic. Fitter software is responsible for mapping the logic into the targeted device. Both synthesis and fitting are accomplished from the *Warp*® environment. The result of the fitting process is a JEDEC file that contains the information about how the logic of the design will be implemented in the device. Jam Composer software uses the JEDEC file from *Warp* to produce a Jam standard programming file. A Jam file contains both the programming data and programming algorithm for the device it targets. Jam Player

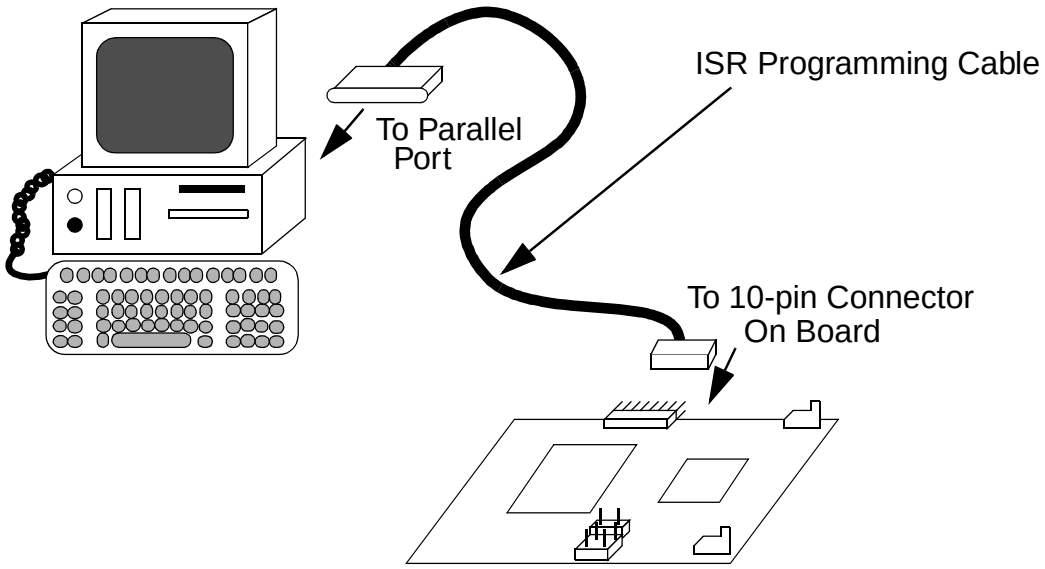

Figure 2. Connecting the ISR Programming Cable

software is then used to program the Ultra37000 device using the Jam file. The Cypress ISR Programming software includes a Jam Composer for Ultra37000 CPLDs and a Jam Player for programming devices on a board through a programming cable attached to a PC parallel port.

The design flow shown in *Figure 1* should be followed to prototype designs with the Ultra37000 ISR Prototype Board. First, design files need to be compiled to produce JEDEC files that target either or both devices on the board. These JEDEC files are then used to create Jam programming files using the Jam Composer provided in the Cypress ISR Programming Software. At this point the Ultra37000 ISR Prototype Board is connected to a PC using an ISR programming cable. Then the Jam Player provided in the Cypress ISR Programming Software programs the Ultra37000 devices on the board using the information in the Jam files.

Using the Ultra37000 ISR Prototype Board

Connecting the Programming Cable

The Ultra37000 devices on the Ultra37000 ISR Prototype Board are programmed using a PC as shown in *Figure 2*. The programming cable connects the parallel port of the PC to the 10-pin connector on the board. Cypress offers two cables for programming ISR devices—the ISRPCCABLE and the UltraISRPCCABLE. The difference between the cables is that the ISRPCCABLE has a 5-volt to 12-volt DC/DC converter while the UltraISRPCCABLE does not. The CPLDs on the Ultra37000 ISR Prototype Board are programmable at 5 volts but are tolerant of 12 volts. Therefore, either programming cable may be used with the Ultra37000 ISR Prototype Board.

Both the ISRPCCABLE and UltraISRPCCABLE have a female end which plugs into the 10-pin, 2 x 5, open header connector provided on the Ultra37000 ISR Prototype Board. The view looking into the end of the programming cable is shown in *Figure 3*. When plugging the cable into the connector on the board, the key on the cable should be at the top away from the board. For further information on ISR programming cables and other design issues related to ISR, consult the Cypress application note, “Design Considerations for In-System Reprogrammable (ISR) Programming of Cypress CPLDs” and “An Introduction to In-System Reprogramming with the Ultra37000.”

Pin 1

GND	$JTAG_{EN}$	ISR*	V_{CC}	TDO
TMS	TCK	TDI	N/C	GND

Figure 3. View Looking into ISR Cable

Providing Board Power

There are two available closed male power jacks for connecting power supplies to the Ultra37000 ISR Prototype Board. These power jacks accept a 2.5-millimeter female plug. A 5-volt AC adaptor can be used to provide power to the Ultra37000 ISR Prototype Board. An AC adaptor with the appropriate female plug or a separate female power plug can be obtained from an electronic components distributor such as Digi-Key. *Table 1* contains sources for obtaining components to be used with the Ultra37000 ISR Prototype Board.

The two power jacks are labeled V_{CC} and V_{CCO}. The power LED labeled DS1 indicates when power is applied to V_{CC}. The Ultra37000 CPLDs on the board always operate with a 5-volt supply which must be supplied by V_{CC}. Ultra37000 CPLDs can support either 3.3-volt or 5-volt I/O levels. If 3.3-volt I/O levels are desired, V_{CCO} must be connected to 3.3 volts. Otherwise, connecting V_{CCO} to 5 volts will provide 5-volt I/O levels.

Table 1. Sources for Ultra37000 Prototype Board Components

Component	Source	Part Number
Male Power Jack, Closed	Digi-Key	CP-002B-ND
2.5mm Female Power Plug	Digi-Key	CP-004B-ND
5 Volt @ 2.4 Amp Wall Transformer	Digi-Key	EPS162-ND
Device 1 Header Strip	Digi-Key	S2011-26-ND
Device 2 Header Strip	Digi-Key	S2011-20-ND

Connecting Power to the Board

When connecting separate power supplies to V_{CC} and V_{CCO}, power must always be applied to V_{CC} first to avoid damaging the devices on the board. If 5-volt I/O levels are desired, power can be provided to V_{CC} and V_{CCO} by the same power supply. This can be accomplished by connecting the power supply to either jack and shorting the JP1 jumper with the provided shunt.

Existing Board Connections

Connections necessary for ISR programming are already provided on the Ultra37000 ISR Prototype Board. These connections are shown in the functional schematic of *Figure 4*. This figure shows both Ultra37000 CPLDs, the ISR connector, the power jacks, and the jumpers. Connections between these locations on the board are either explicitly shown or simply labeled.

Power to the board is supplied through the two jacks at the edge of the board. The zener diodes connected to each power jack protect the devices from high voltage inputs. A 0.1-µF decoupling capacitor is connected to each supply to eliminate noise that may affect device operation. Additionally, selected V_{CC} and V_{CCO} pins of each device are connected to a 0.01-µF decoupling capacitor. Heat dissipation from each device is enhanced through metal heat sinks touching each device package.

The JTAG interface used for ISR programming uses both parallel connections, for TCK, TMS, and $JTAG_{EN}$, and serial connections, for TDI and TDO. The parallel connections between the ISR connector and the Ultra37000 CPLDs are labeled in *Figure 4*. Device 1 does not have a $JTAG_{EN}$ pin since its ISR pins are single-function and therefore does not need $JTAG_{EN}$ to select between pin functions. *Table 2* also shows the parallel ISR connections made to each device site.

The serial JTAG connections are explicitly shown in *Figure 4*. Depending on the needs of the user, either or both of the devices can be included in the ISR chain for programming by configuring the Daisy Chain Jumpers. The three possible configurations are shown in *Table 3*. The Cypress application notes, “Designing with Cypress In-System Reprogrammable (ISR) CPLDs for PC Cable Programming” and “Cascading ISR Devices”, provide more information about chaining together JTAG devices

Table 2. Parallel ISR Connections

JTAG Pin	Device 1 Pin Number	Device 2 Pin Number
TCK	7	6
TMS	59	46
$JTAG_{EN}$	NA	139

Table 3. Daisy Chain Jumper Configurations

Devices in Chain	Jumper Configuration
Device 1 only	A-B C-E
Device 2 only	B-D E-F
Device 1 and Device 2	A-B C-D E-F

Making Board Connections

To facilitate making connections to the devices on the Ultra37000 ISR Prototype Board, each device pin is connected to one of the header strip sites surrounding each CPLD. The sites surrounding the Ultra37256P160 that is in place on the board have been populated with header strips. *Figure 5* shows the dimensions of the header strips used on the Ultra37000 ISR Prototype Board. If an Ultra37256P208 has been added to the board, header strips can be easily added to the header sites around device 1. Ordering information for the suggested header strips can be found in *Table 1*. The header strips allow the Ultra37000 ISR Prototype Board to be easily connected to another circuit board through a ribbon cable. Logic analyzer probes can be attached to the header strips to view device operation. Other possible uses for the header strips include LEDs and seven segment displays for monitoring outputs and banks of DIP switches for providing inputs.

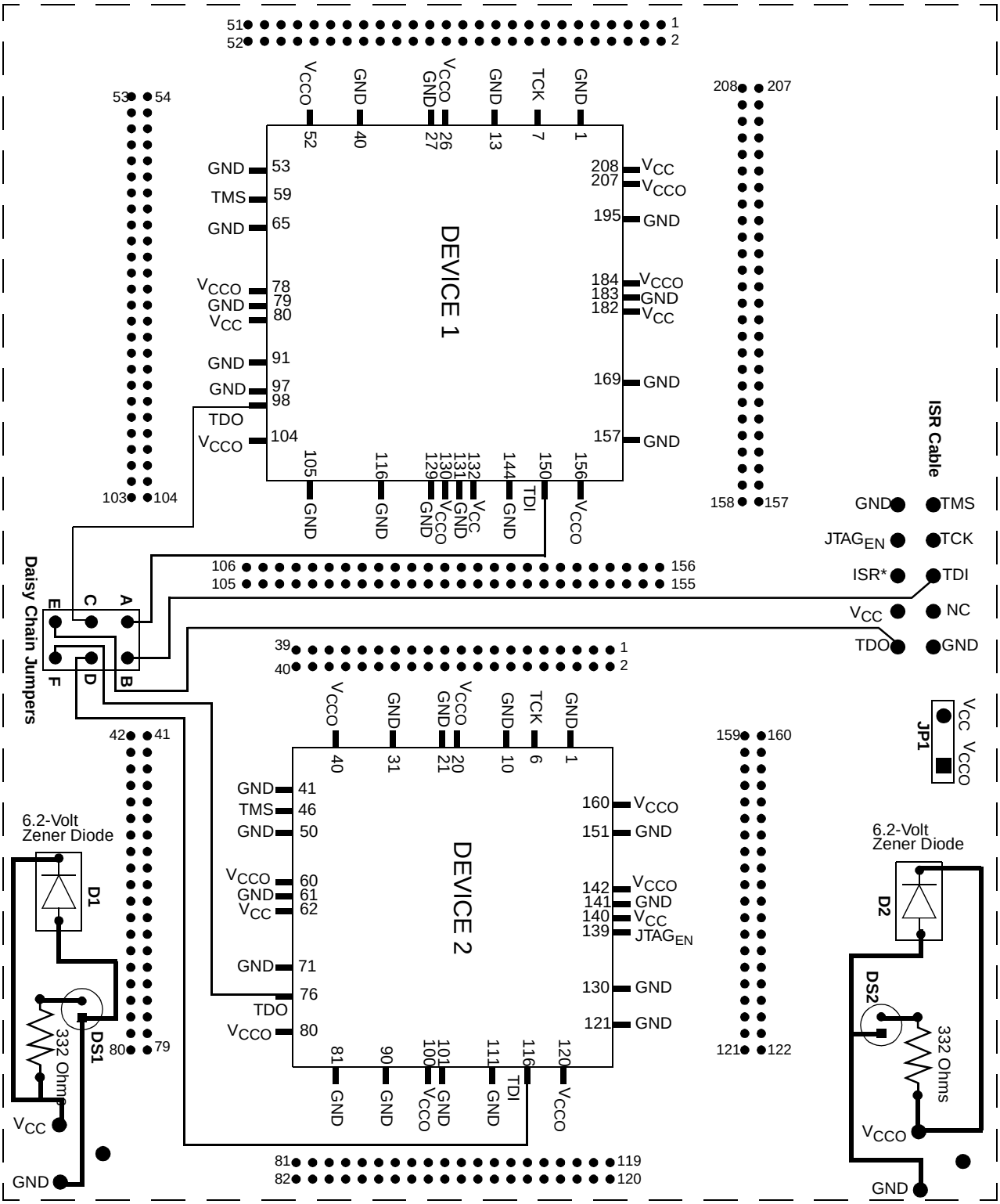

Figure 4. Functional Schematic of the Ultra37000 ISR Prototype Board

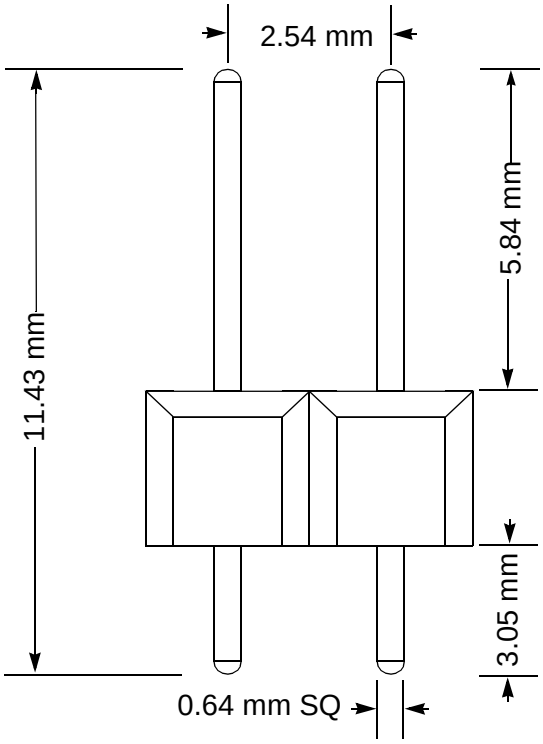

Figure 5. Header Strip Dimensions

Conclusion

This application note highlights the features of the Ultra37000 ISR Prototype Board. The board is designed to support two Ultra37000 CPLDs which may be programmed separately or together by configuring the board's jumpers. Two power supply jacks allow for one power supply to provide 5 volts to the cores of both chips while another can power the devices' I/O levels at either 3.3 or 5 volts. External logic or I/O devices may be connected to the Ultra37000 ISR Prototype Board by using the header strips that surround each device.

The Ultra37000 ISR Prototype Board provides designers with a system already configured to take advantage of the ISR capability of Ultra37000 CPLDs. The board allows designers unfamiliar with In-System Reprogrammability to investigate the Cypress ISR design flow without first designing a board to support the JTAG interface. Designers may also use this board to readily evaluate Cypress programmable logic in their own prototype designs.

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