An Introduction to Active-HDL™ Sim

Introduction

Active-HDL™ Sim is a functional simulator utilizing post-fitting VHDL timing models produced by *Warp™*, the VHDL/Verilog synthesis tool for Cypress Programmable Logic Devices (PLDs). This application note is a brief introduction to Active-HDL Sim, containing four sections:

1. Installing/Uninstalling the Simulator
2. Creating an 1164/VHDL Simulation Model
3. The Simulation Process
4. Applying Stimulus

Please use this document to familiarize yourself with the simulator. Consult the online help as your next resource.

Installing the Simulator

The installation of the Active-HDL Sim application is invoked automatically by running the *setup.exe* program, located in the Aldec folder on the Active-HDL Sim CD-ROM. The *Install Shield Wizard* assists in the installation process, asking for registration information and configuration data including user name, company name, and a destination directory that will store the Active-HDL Sim components.

During the installation process, all Active-HDL Sim components are copied into the destination directory. Most files are copied into the default Active-HDL Sim directory. Several files are also copied into the *WINDOWS\SYSTEM* directory (Windows 95) or *WINDOWS\SYSTEM32* directory (Windows NT). Required parameters for the simulator are written into the operating system's registry. Before running the post-fitting timing simulator the computer must be restarted.

Uninstalling the Simulator

A manual uninstall is not recommended. To uninstall Active-HDL Sim, run the s*etup.exe* program from the CD-ROM drive. The *Install Shield Wizard* will detect a previously installed version of Active-HDL Sim, then will pause for user confirmation on running the uninstall program. The *Uninstall* program performs the following operations:

1. Deletes all files in the Active-HDL Sim directory.
2. Removes the *\HKEY_CURRENT_USER\SOFTWARE\ALDEC\FRAME* branch from the system registry.
3. Removes the files installed in the *WINDOWS\SYSTEM* (or *WINDOWS\SYSTEM32*) directory. The Uninstall program checks the reference counter for each operation to avoid deleting files required for other programs installed on the system.

It is recommended that when the Install Shield Wizard's *Remove Shared Files* window opens, select "No to All," this will leave a few extra "dll" files in your Windows directory but will not harm your system.

Creating the 1164/VHDL Simulation Model

The input file for the Active-HDL Sim is a post-synthesis simulation model. The *Warp* environment can generate the post-synthesis simulation model in many different formats. The Active-HDL Sim needs an IEEE 1164/VHDL simulation model.

Selecting the 1164/VHDL File Format

Warp Release 5 Users

In the Galaxy window, under the *Project* menu, select *Device*. After selecting a device, click the *Compiler Options* button in the *Select Device* window. This will open the *Compiler Options* window as shown in *Figure 1.* The window defaults to the *Synthesis* tab. From the *Timing Model* drop down menu, select the 1164/VHDL output file format. Make sure that the *Enable Testbench Output* checkbox is selected.

The New vhd Directory

When the design is entered and ready to compile, "set top" the VHDL file, and compile the code, the simulation model will be created (see *Warp* User's guide for compiling VHDL code). The 1164/VHDL simulation model has the same file name and extension as the top-level VHDL source file. In order to not over-write the original design file, *Warp* creates a new

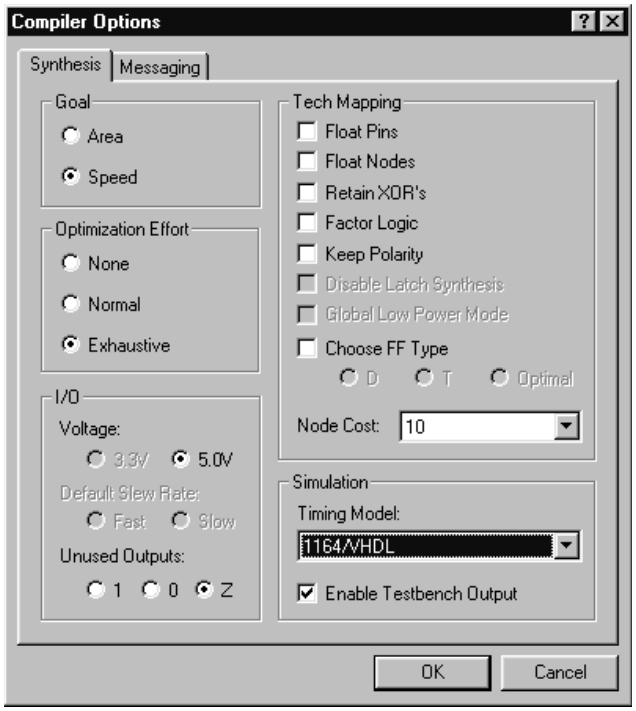

Figure 1. *Warp* Release 5.0 Compiler Options Window

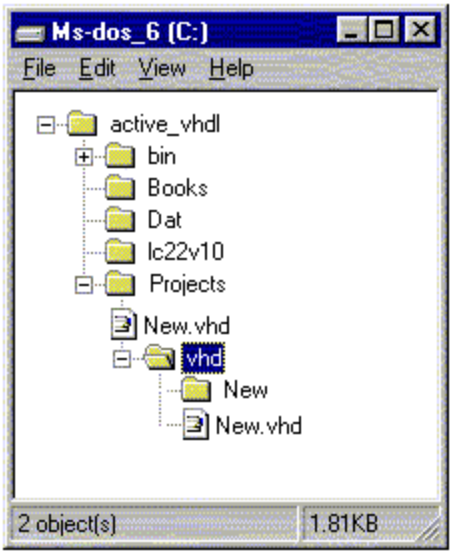

Figure 2. Hierarchical List of the Current Working Directory

subdirectory in your current working directory entitled **vhd**, and places the model in that directory (see *Figure 2*).

The Simulation Process

In order to simulate a design, the following steps are used.

1. Loading an 1164/VHDL Simulation Model File
2. Initializing the Simulation
3. Adding Signals
4. Assigning Stimulus
5. Running the Simulation
6. Viewing the Waveform
7. Saving the Waveform

Loading an 1164/VHDLSimulation Model

The first step is to open Active-HDL Sim by clicking on the desktop shortcut. To load the 1164/VHDL simulation model, select the *Open VHDL* item under the *File* menu. Remember that the 1164/VHDL simulation model is in the *vhd* subdirectory of the current *Warp* working directory. (If you select the standard VHDL file by accident, the Active-HDL Sim compiler will generate several errors in the Console window.) When properly loaded, the 1164/VHDL simulation model will display several messages under the Compiler tab of the Console window. If the Console window is not visible, click on the *View Console* button in the standard toolbar. One of the messages should be a compile successful statement, similar to -- Compile success 0 Errors 0 Warnings Analysis time: 3.0 [s].

Initializing the Simulation

To begin a simulation, initialize the simulator using the *Initialize Simulation* item under the *Simulation* menu. After the simulator has been initialized, open a new Waveform window. To create a new waveform, click the *New Waveform* button in the standard toolbar. A blank waveform is added to the Waveform window of the simulator. This option is also available under the *File* menu.

Adding Signals

The next step is to add signals to the waveform, select *Add Signals…* from the *Waveform* menu. The Add Signals window opens with a list of all inputs, outputs and internal nodes available for the current compiled design. Double-click on the required signals to add them to the waveform.

Assigning Stimulators

Stimulus is applied to the simulation model using input stimulators. To define input stimulators, left-click on an input signal in the left pane of the waveform window. Now click the right

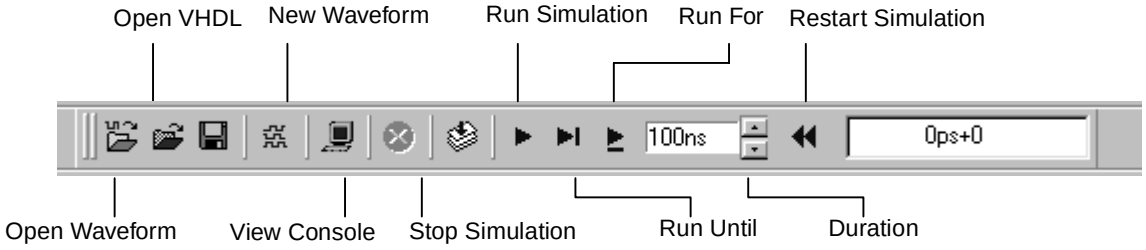

Figure 3. The Standard Toolbar

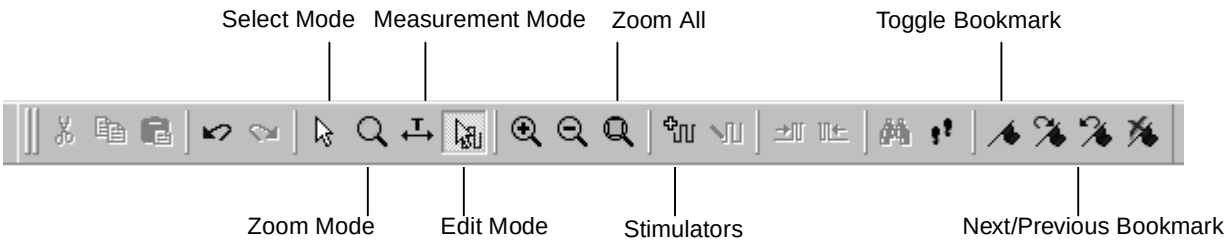

Figure 4. The Waveform Toolbar

mouse button to invoke a pop-up menu, select *Stimulators.* Click on a signal in the *Signals* tab and select a stimulator type in the drop down list. There are several different types of stimulators. A brief description is given in a later section of this application note titled, “Stimulator Types.” Active-HDL Sim has excellent online help on stimulator types and strengths. After defining the stimulator click the apply button.

Running the Simulation

Once the input stimulators are defined and the waveform has been initialized, the simulation can run. Click on the *Run For* button in the standard toolbar. The simulation halts after the specified duration has been simulated. At this point the input stimulators can be altered and will take effect when the simulation continues. Clicking on the *Run For* button again will continue the simulation from the halted point. To end and re-initialize the simulation, click on the *Restart Simulation* button.

Viewing the Waveform

Many waveform properties can be manipulated to enhance the appearance and effectiveness of the simulation. The following is a brief description of some of these properties.

Viewing a Bus

The individual signal lines on a bus can be viewed and edited. Select the “+” box beside the bus name in the waveform window. Stimulators can be assigned to the entire bus or to each individual signal in the bus.

Adding Color to the Waveform

The waveforms can be colored to improve clarity when many signals are displayed. To add color to all the visible waveforms, (not including closed buses) select *Colorize Waveforms* in the *Waveform* menu. However, to alter the color of an individual signal, right-click on a signal and select the *Properties* option in the popup menu.

Zoom

To enter zoom mode, click on the leftmost magnifying glass in the waveform toolbar. Click the new magnifying glass pointer on the waveform to “zoom in.” Clicking the left mouse button, while depressing the control key, “zooms out” the waveform. To quickly “zoom in,” “zoom out,” and “zoom all” (view the entire waveform) click on the three rightmost magnifying glasses  in the waveform toolbar.

Bookmarks

Click on the select mode button  in the waveform toolbar. When in select mode, bookmarks can be placed throughout the waveform for easy referencing. Left-click on any part of the waveform to generate the red time marker. Clicking the *Toggle Bookmark* button in the waveform toolbar creates a new bookmark. The *Next/Previous Bookmark* buttons are used to navigate between all the bookmarks in the current waveform. Bookmarks are displayed as a blue triangle on the timing scale at the top of the waveform window (see *Figure 5*).

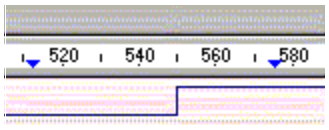

Figure 5. Bookmark Indicators on the Timing Scale of the Waveform

Figure 6. Measurement Mode

Measurement Mode

To enter measurement mode, click on the double-headed arrow  in the waveform toolbar. In measurement mode, exact timing information between two signal transitions can be displayed in the current waveform. To display timing information, move the mouse pointer over a rising or falling edge until the mouse pointer turns green; click and hold the left mouse button (the waveform is highlighted as the mouse moves across the screen). Release the button when the mouse pointer turns green close to another edge of any waveform. An exact measurement with time units is displayed between the two edges (*Figure 6*). To delete a timing measurement, click the edit mode button  in the waveform toolbar, select the measurement, and press the delete key.

Saving the Waveform

There are two different ways of saving in the Active-HDL Sim environment. A *Save* will save the currently selected waveform, whereas a *Save All* saves all the waveforms in the waveform window. The default file extension for a waveform in Active-HDL Sim is “awf.”

Stimulator Types

A stimulator is used to define input waveforms on a signal or bus. Stimulators are defined by their type and strength (see *Figure 7*). The following section gives a brief overview of stimulator types. The online documentation has a more detailed description of both stimulator types and strengths.

There are six different types of stimulators: clock, custom, formula, predefined, value and hotkey.

Clock

A clock stimulator produces a rectangular waveform defined by the following parameters: frequency/period, initial offset time, duty cycle, and initial value.

Custom

A custom stimulator is created using the editing features of the Waveform editor. While in edit mode, the input stimulator can be set high or low by pressing ‘1’ or ‘0’ respectively. Please refer to the online help for further description of how to use the custom waveform editing feature.

Formula

A formula stimulator produces a waveform defined by a simple syntax. The waveform is defined as a sequence of value-time pairs. The time component of a pair indicates the moment the stimulated signal assumes the value component of the pair. The default formula unit of time is picoseconds. To repeat the stimulus at a specified period, add the –r modifier. The formula syntax is as follows:

<value> <time> [, <value> <time> ...] [-r <period>]

The following is a sample formula stimulator. The associating waveform is shown in *Figure 8*.

Formula - 0 0, 1 10000, 0 20000, 1 45000

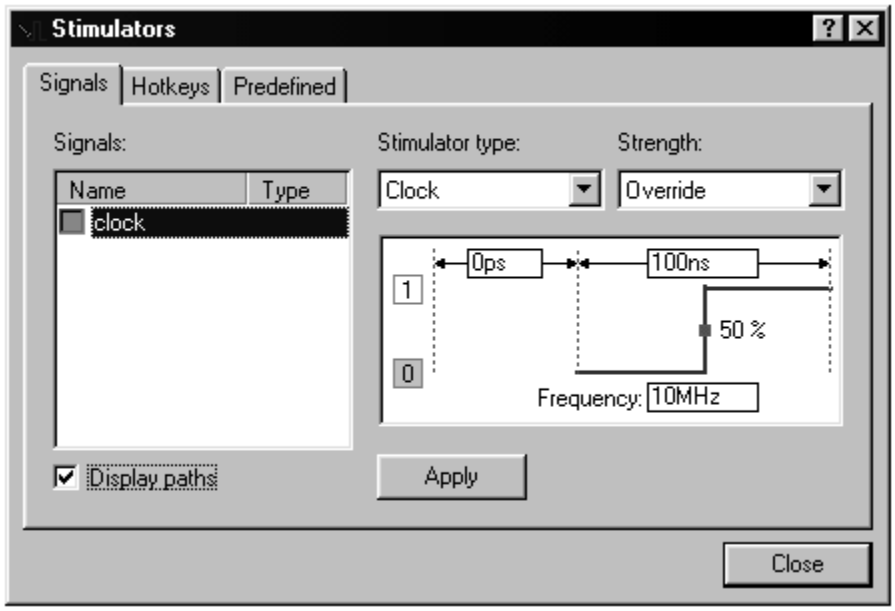

Figure 7. Assigning a Clock Stimulus in the Stimulator Window

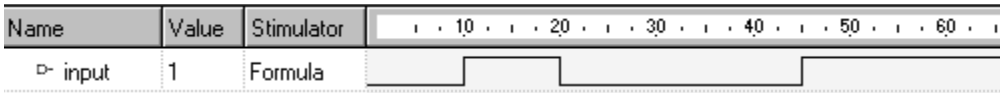

Figure 8. Sample Formula Input Stimulator

Predefined

A predefined stimulator is either a clock or formula stimulator that has been assigned a unique name. A predefined stimulator is referenced by name and can be assigned to several different signals. To create a new predefined stimulator, click on the *Predefined* tab, in the Stimulators window. At the bottom of the *Predefined* list box, create a new stimulator by entering a unique name and clicking the add button. Select the stimulator type clock/formula and define the simulator as in the previous clock and frequency sections.

Value

A value stimulator drives an input signal or bus with a constant value throughout the simulation. For example, '1' active HIGH, '0101' 4 bit input bus.

Hotkey

A hotkey stimulator is similar in concept to a value stimulator except that it provides a convenient mechanism for changing the forced value. Press a specific key to toggle between two signal values. A longer list of values can be defined, which will cyclically be switched by the hotkey.

Summary

This application note provides a brief introduction to the Active-HDL Sim post-fitting timing simulator, and its role in the Warp design process. Further information and details are available in the online help. In the Galaxy environment, A VHDL or Verilog design can be created, synthesized and targeted to any Cypress device. Active-HDL Sim can take a Galaxy-produced 1164/VHDL simulation model and perform full functional and timing post-fitting simulation. The Cypress Programmable Logic Applications group fully supports the *Warp2*® package including Active-HDL Sim. The addition of Active-HDL Sim to the *Warp2* package complements an industry established synthesis tool.

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