Using the Delta39K™ ISR™ Prototype Board

Introduction

This application note is intended to provide instruction in the use of the Delta39K™ ISR™ Prototype Board. This board serves two major purposes. First, it provides a board with Cypress Delta39K and Ultra37000™ CPLDs already connected to take advantage of In-System Reprogrammability™ (ISR). This allows designers who are unfamiliar with ISR to investigate it as a possible device programming solution. Second, it permits designers who need custom logic to more easily utilize Cypress CPLDs in prototype designs. After programming the Delta39K and/or Ultra37000 devices on the ISR Prototype Board, connections can be made between the ISR Prototype Board and the designer's board using the provided header strips. This gives a designer the ability to verify the functionality of the CPLDs within a system before designing them into that system.

This application note should familiarize the reader in the use of the Delta39K ISR Prototype Board and highlight the board's features. Topics of discussion will include connecting the programming cable, connecting power supplies to the board, using the jumpers on the board, and making connections between the Delta39K ISR Prototype Board and other systems.

In-System Reprogrammability allows Complex Programmable Logic Devices (CPLDs) to be reprogrammed after being soldered in place on a printed circuit board. The Delta39K ISR Prototype Board is designed to support one Delta39K and Ultra37000 CPLD. The first device is a 100,000 gate 3.3V Delta39K100 in a 208-pin PQFP package. The second device is a 256-macrocell 3.3V Ultra37000 in a 160-pin TQFP package.

ISR programming of the CPLDs follows the IEEE 1149.1 standard Test Access Port and Boundary Scan architecture, which supports chaining more than one IEEE1149.1/JTAG-compliant devices together. ISR Programming Software supports daisy-chain programming of multiple Cypress CPLDs.

Delta39K and Ultra37000 CPLDs support the STAPL standard as the solution for ISR programming. STAPL is an interpreted language that provides a standard for programming PLDs through the JTAG interface. The CPLDs on the Delta39K ISR Prototype Board are programmed through an ISR cable using the Cypress ISR Programming Software. To learn more about the ISR features of the Delta39K and Ultra37000 family, refer to Cypress application notes at our website (*http://www.cypress.com, Support, Application Notes, Programmable Logic Devices*).

Design Flow

In order to use the Delta39K ISR Prototype Board, it is important to understand how it fits into the ISR design flow. The basic design flow for the Cypress CPLD is shown in *Figure 1*. Designs are typically specified in VHDL or Verilog code. This code can either be written by the designer or generated from schematics. Once the code for the design is complete, it is synthesized into logic. Fitter software is responsible for mapping the logic into the targeted device. Both synthesis and fitting are accomplished from the *Warp*® environment. The result of the fitting process is a compressed Intel Hex file (Delta39K) or a JEDEC file (Ultra37000) that contains the information about how the logic of the design will be implemented in the device. STAPL Composer software uses the output files from *Warp* to produce STAPL standard programming files. A STAPL file contains both the programming data and

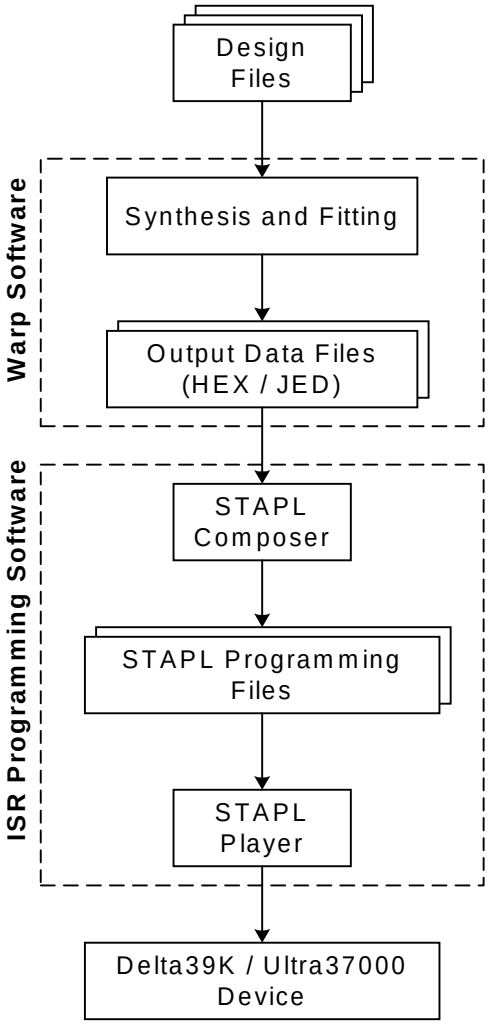

Figure 1. Cypress CPLD Design Flow

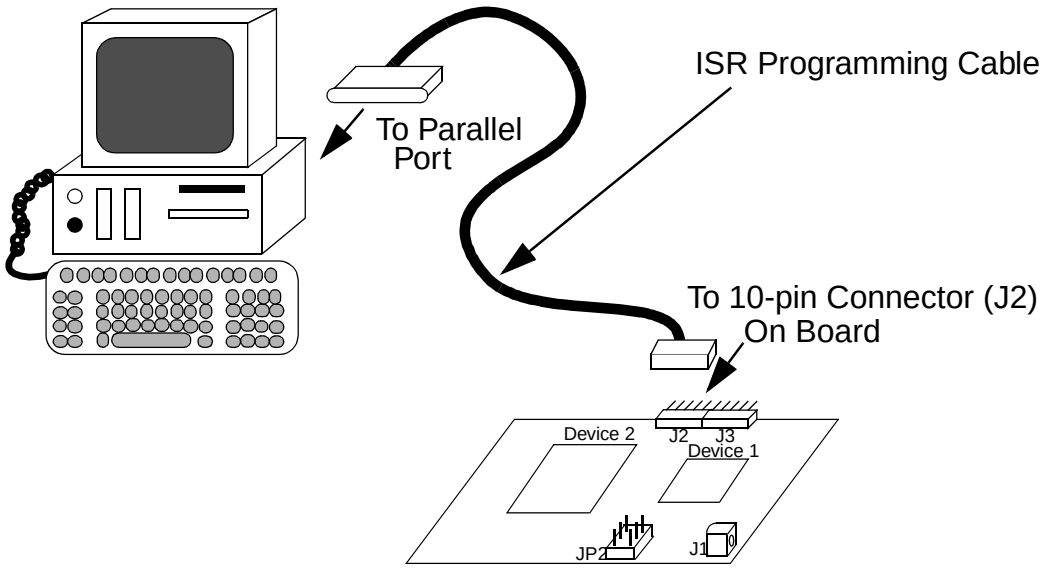

Figure 2. Connecting the ISR Programming Cable

programming algorithm for the device it targets. A STAPL Player is then used to program the CPLDs using the STAPL files. The Cypress ISR Programming software includes a STAPL Composer and a STAPL Player for programming devices on a board through a programming cable attached to a PC parallel port.

The design flow shown in *Figure 1* should be followed to prototype designs with the Delta39K ISR Prototype Board. First, design files need to be compiled to produce output files that target either or both devices on the board. These output files are then used to create STAPL programming files using the STAPL Composer provided in the Cypress ISR Programming Software. At this point the Delta39K ISR Prototype Board is connected to a PC using an ISR programming cable. Then the STAPL Player provided in the Cypress ISR Programming Software programs the CPLDs on the board using the information in the STAPL files.

Using the Delta39K ISR Prototype Board

Connecting the Programming Cable

The CPLDs on the Delta39K ISR Prototype Board are programmed using a PC as shown in *Figure 2*. The programming cable connects the parallel port of the PC to the 10-pin connector (J2) on the board. Cypress offers two cables for programming the CPLDs on this board—the UltraISRPCCABLE and the C3ISRPCCABLE. Either cable will be able to program both devices.

Both of the cables have a female connector which plugs into the 10-pin, 2 x 5, open header connector provided on the Delta39K ISR Prototype Board. The view looking into the end of the programming cable is shown in *Figure 3*. When plugging the cable into the connector on the board, the key on the cable should be at the top away from the board.

The programming cable should be disconnected from the board before connecting the power supply.

Pin 1

GND	$JTAG_{EN}$	ISR*	V_{CC}	TDO
TMS	TCK	TDI	N/C	GND

Figure 3. View Looking into ISR Cable 10-pin Connector

Providing Board Power

The power jack accepts a 2.5-millimeter female plug. A 3.3-volt AC adaptor can be used to provide power to the Delta39K ISR Prototype Board. An AC adaptor with the appropriate female plug or a separate female power plug can be obtained from an electronic components distributor. The power jack is labeled V_{CC}. The power LED labeled DS1 indicates when power is applied to V_{CC}. The Delta39K and Ultra37K CPLDs on the board operate with a 3.3-volt supply which must be supplied by V_{CC}.

Existing Board Connections

Connections necessary for ISR programming are already provided on the Delta39K ISR Prototype Board. Power to the board is supplied through the power jack at the edge of the board. A 0.1-µF decoupling capacitor is connected to the power supply to eliminate noise that may affect device operation. Additionally, selected V_{CC} and V_{CCO} pins of each device are connected to a 0.01-µF decoupling capacitor.

The JTAG interface used for ISR programming uses both parallel connections, for TCK, TMS, and $JTAG_{EN}$, and serial connections, for TDI and TDO. Device 1 does not have a $JTAG_{EN}$ pin since its ISR pins are single-function and therefore does not need $JTAG_{EN}$ to select between pin functions. *Table 1* also shows the parallel ISR connections made to each device site.

The serial ISR connections can be set to include either or both CPLDs by configuring the Daisy Chain Jumpers.

The three possible configurations are shown in *Table 2*. The Cypress application notes “Design Considerations for In-System Reprogrammable (ISR) Programming of Cypress CPLDs” provides more information about chaining together JTAG devices.

Table 1. Parallel ISR Connections

JTAG Pin	Device 1 Pin Number	Device 2 Pin Number
TCK	157	7
TMS	162	46
$JTAG_{EN}$	NA	139

Table 2. Daisy Chain Jumper Configurations

Devices in Chain	Jumper Configuration
Device 1 only	A-B C-E
Device 2 only	B-D E-F
Device 1 and Device 2	A-B C-D E-F

Making Board Connections

To facilitate making connections to the devices on the Delta39K ISR Prototype Board, each device pin is connected to one of the header strip sites surrounding each CPLD. The header strips allow the Delta39K ISR Prototype Board to be easily connected to another circuit board through a ribbon cable. Other possible uses for the header strips include LEDs and seven segment displays for monitoring outputs and banks of DIP switches for providing inputs.

The 10-pin Header (J3) right next to the 10-pin ISR Header will be used for future board’s features expansion.

For a complete list of pins information, please refer to each device’s data sheet/pin list.

Conclusion

This application note highlights the features of the Delta39K ISR Prototype Board. The board is designed to support one Delta39K and one Ultra37000 CPLDs which may be programmed separately or together by configuring the board’s jumpers. External logic or I/O devices may be connected to the Delta39K ISR Prototype Board by using the header strips that surround each device.

The Delta39K ISR Prototype Board provides designers with a system already configured to take advantage of the ISR capability of Delta39K CPLDs. The board allows designers unfamiliar with In-System Reprogrammability to investigate the Cypress ISR design flow without first designing a board to support the JTAG interface. Designers may also use this board to readily evaluate Cypress programmable logic in their own prototype designs.

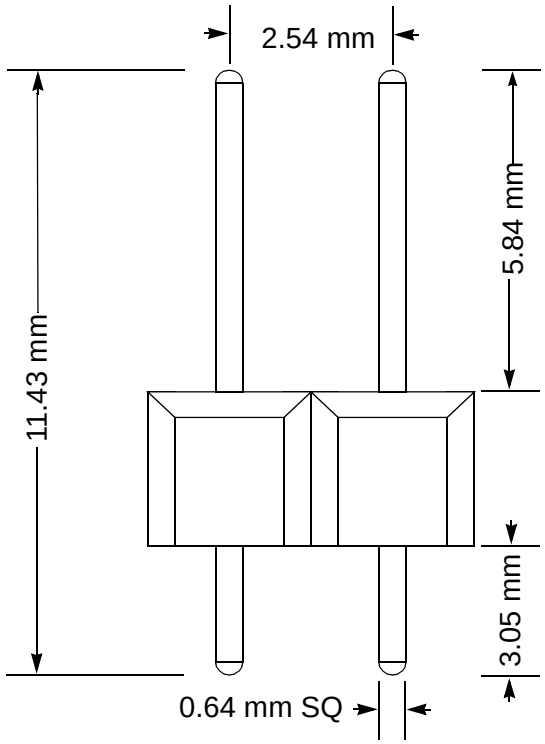

Figure 4. Header Strip Dimensions

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