PRELIMINARY

Interfacing Delta39K™ and Quantum38K™ CPLDs to 5V Devices

Introduction

Operating voltages for digital systems have dropped from 5V to 3V or lower, because of the demand for higher-speed logic families that use ICs with smaller geometries. Contributing to this drop of voltages are the low power-consumption requirements of mobile wireless devices, such as cellular phones, handheld computers, and GPS receivers.

This growing demand for low power consumption/better performance has resulted in system designers moving to use as many low voltage components as possible. However, since not all components are available in 3V operation, designers are forced to use a mix of 3V and 5V components. Somewhere within a mixed voltage design, the designer must interface 3V and 5V devices. The Delta39K™ and the Quantum38K™ CPLD families are not natively 5V tolerant so they require special consideration when interfacing to 5V systems. This application note discusses the various possibilities of interfacing a 5V device to the Delta39K CPLD. All the solutions discussed here for Delta39K are applicable to the Quantum38K also.

There are eight I/O banks in the Delta39K and Quantum38K CPLDs, two I/O banks on each side. Each I/O bank has its own dedicated I/O power supply (V_{CCIO}). The V_{CCIO} between the different I/O banks are not connected together, resulting in eight separate I/O power supplies on the chip. The I/O banks of these two devices allow configuration of multiple I/O standards on the device at the same time.

Both Delta39K and Quantum38K support the following I/O standards: LVCMOS3, LVCMOS, LVCMOS2, LVTTL, 3.3V PCI. *Table 1* shows a summary of the V_{CCIO} values for each I/O standard supported by the Delta39K and Quantum38K CPLDs. Additionally, Delta39K supports GTL+, HSTL Class I through IV, SSTL2 Class I and II, and SSTL3 Class I and II. *Table 2* lists the additional I/O standards supported by Delta39K CPLDs. The I/O pins are 3.3V tolerant and CompactPCI Hot Swap compatible. The I/Os of Delta39K and Quantum38K are not 5V tolerant. However, by introducing simple external circuitry, these devices can be interfaced with a 5V device.

This application note assumes that LVTTL or LVCMOS I/Os will be used to interface to the 5V device. Therefore, at least one I/O bank must be configured to support LVTTL or LVCMOS I/Os. By basing the 5V interface solution on a 3.3V standard, the required voltage translations are simpler to accomplish. The possibility of interfacing 5V devices to other Delta39K supported I/O standards are not considered in this application note.

Interfacing to a 5V External Device

This application note discusses the possible methods of achieving the external circuitry required for this interface. When deriving a solution to interface devices with different voltages, the most important factors to be considered are the voltage and current levels.

Designers trying to interface to a 5V device should make sure that any of the voltage and the current requirements mentioned in the data sheet for the Delta39K family are not violated.

Table 1. Delta39K and Quantum38K Supported I/O Standards

I/O Standards	V_{CCIO}
LVCMOS18	1.8V
LVCMOS2	2.5V
LVCMOS3	3.0V
LVCMOS	3.3V
LVTTL	3.3V
PCI	3.3V

Table 2. Additional I/O Standards Supported by Delta39K CPLD Family

I/O Standards	V_{CCIO}
GTL+	N/A
SSTL2 Class I & II	2.5V
SSTL3 Class I & II	3.3V
HSTL Class I & II	1.5V
HSTL Class III & IV	1.5V

To achieve an interface between low voltage and high voltage devices, the currents I_{OH} and the I_{OL} of the driving device and the voltages V_{IL} and V_{IH} of the receiving device are the most important factors to be considered. Any interface between a low voltage and a high voltage device can be divided into two different conditions. They are

Case(i) When a high voltage device is driving a low voltage device.

Case(ii) When a low voltage device is driving a high voltage device.

Each of these cases can further be divided as when driving high and driving low.

Case(i) When a high voltage device is driving a low voltage device

(a) When driving '0':

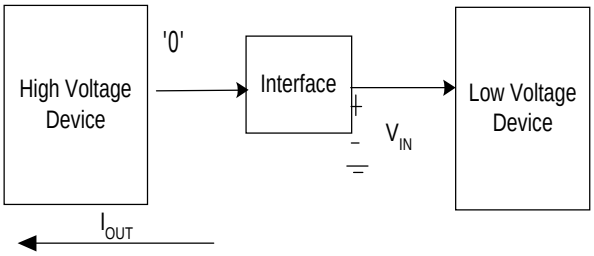

Figure 1. High Voltage Device Driving Low

The requirements for the interface in *Figure 1* are discussed in *Table 3*.

Table 3. High Voltage Device Driving Low

Condition	Requirement
1	$I_{OUT} < \| I_{OL} \|$
2	$V_{IL(MIN)} \le V_{IN} \le V_{IL(MAX)}$

(b) When driving '1':

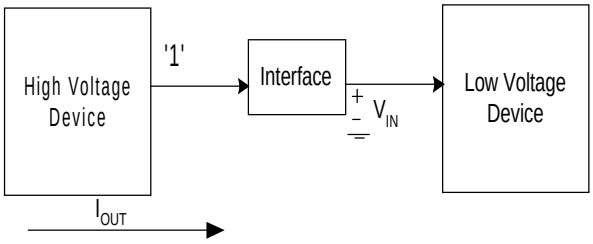

Figure 2. High Voltage Device Driving High

The requirements for the interface in *Figure 2* are discussed in *Table 4*.

Table 4. High Voltage Device Driving High

Condition	Requirement
1	$I_{OUT} < \| I_{OH} \|$
2	$V_{IH(MIN)} \le V_{IN} \le V_{IH(MAX)}$

Case(ii) When a low voltage device is driving a high voltage device

(a) When driving '0':

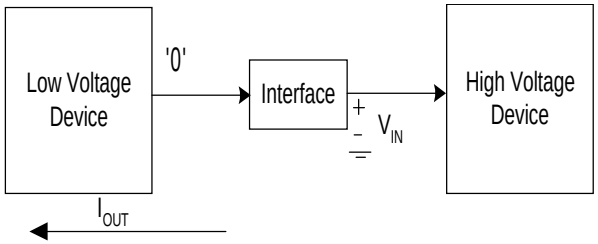

Figure 3. Low Voltage Device Driving Low

The requirements for the interface in *Figure 3* are discussed in *Table 5*.

Table 5. Low Voltage Device Driving Low

Condition	Requirement
1	$I_{OUT} < \| I_{OL} \|$
2	$V_{IL(MIN)} \le V_{IN} \le V_{IL(MAX)}$

(b) When driving '1':

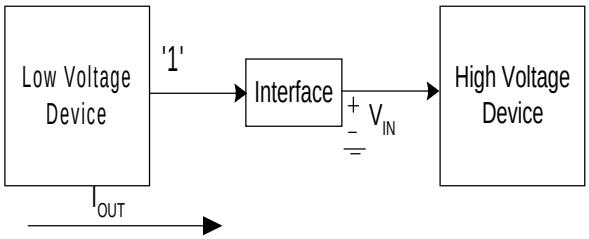

Figure 4. Low Voltage Device Driving High

The requirements for the interface in *Figure 4* are discussed in *Table 6*.

Table 6. Low Voltage Device Driving High

Condition	Requirement
1	$I_{OUT} < \| I_{OH} \|$
2	$V_{IH(MAX)} \le V_{IN} \le V_{IH(MAX)}$

If these conditions are met, then the interface can be achieved.

The voltage translation can be unidirectional or bidirectional. Both these conditions will be discussed in detail.

Unidirectional Voltage Translation

This again involves four possible cases:

A. Using a Delta39K device to drive a TTL device

B. Using a Delta39K device to drive a CMOS device

C. Using a TTL device to drive a Delta39K device

D. Using a CMOS device to drive a Delta39K device

A. Using Delta39K to Drive a TTL External Device

Here the source is Delta39K and the receiver is an external TTL device. No additional circuitry is required for this interface because the electrical characteristics of each device satisfy the required voltage levels. *Table 7* gives the Delta39K output

voltages for both LVTTL and LVCMOS. These voltages are compatible with TTL input voltage requirements.

Table 7. The Voltage Levels of Delta39K and TTL Devices

Voltage (V)	Delta39K LVCMOS	Delta39K LVTTL	TTL (SPEC)
$V_{OH(MIN)}$	3.1	2.4	2.0
$V_{OL(MAX)}$	0.2	0.4	0.8

B. Using the Delta39K to Drive a 5V CMOS External Device.

In this case, the source again is a Delta39K device but the receiver is a 5V CMOS device. The best possible solution for this is using a buffer to implement this interface.

Using a Buffer

One way to translate a 3.3V output to a 5V level is with ACT/HCT logic. These parts accept a TTL level input and output a CMOS standard output.

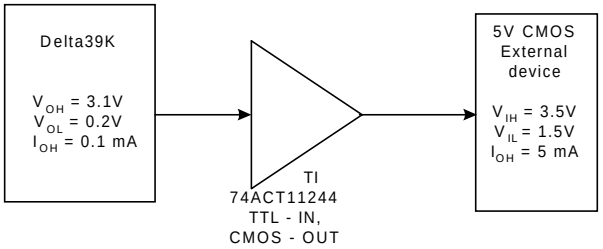

Figure 5. TTL - in CMOS - out Buffer

This is a relatively straightforward approach. Using a buffer satisfies the requirements for a low-voltage device driving a high-voltage device discussed as in Case(ii) (*Figure 3* and *Figure 4*) in the earlier section. A good example for this is using a buffer with ACT logic. TI's 74ACT11244 is an Octal buffer using this logic and the typical $T_{pd(max)}$ of this device is 6.3 ns. Depending on the number of CMOS inputs that need to be driven, wider and narrower buffers are available. The performance of some designs may be improved by using a registered buffer. An example of a registered buffer is 74ACT11374, which is an Octal Edge-triggered D-type FF with three-state outputs. The maximum delay offered by these devices is 5.5 ns. When using a registered buffer, the user must account for the added clock cycle latency and assure setup and hold times can be met. The links to the datasheets for these two devices are given below:

The link for the buffer 74ACT11244 is
http://www-s.ti.com/sc/psheets/scas006c/scas006c.pdf

and the link for the buffer 74ACT11374 is

http://www-s.ti.com/sc/psheets/scas217a/scas217a.pdf

C. Using a TTL device to drive the Delta39K device

In this case, the source is a TTL device and the receiver is Delta39K. This interface can be achieved by four different solutions. They are: using a buffer, using a clamp circuit, using a Zener diode and using a diode clamp.

(i)Using a Buffer

The conditions discussed in Case(i) *Figure 1* and *Figure 2* are met when using a buffer as long as the specifications of the buffer are compatible with CMOS inputs and LVTTL outputs.

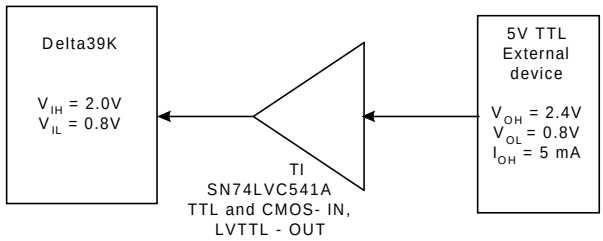

Figure 6. TTL, CMOS - in LVTTL - out Buffer

This device is an 8-bit buffer/driver with three-state outputs and has TTL and CMOS compatible inputs and LVTTL outputs. This is a product of TI and the part number for this device is SN74LVC541A. The $T_{pd(max)}$ for this device is 5.1 ns. If needed, a registered buffer like SN74LVC374A can be used. This buffer can take both 5V and 3.3V inputs. The maximum delay for this device is 8.5 ns and the rest of the specifications are similar for both the devices. The links to the data sheets for these two devices are given below:

The link for the buffer SN74LVC541A is

http://www-s.ti.com/sc/psheets/scas298h/scas298h.pdf

and the link for the buffer SN74LVC374A is

http://www-s.ti.com/sc/psheets/scas296i/scas296i.pdf

(ii)Using a Clamp Circuit

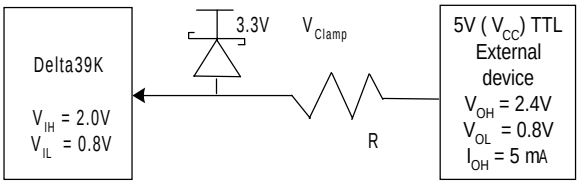

Figure 7. Clamp Circuit

The diode clamps are the best voltage limiters. They prevent the outputs from exceeding certain voltage levels with no effect on voltages less than that (including negative voltages) of the breakdown voltage. The only limitation is that the input must not be driven so negative that the reverse breakdown voltage of the diode is exceeded. Usually, most CMOS inputs have diode clamps. Using a Schottky diode in the clamp circuit is the preferred solution because Forward bias voltage (V_{Diode}) of a Schottky diode is 0.3V compared to 0.7V for a regular diode. In other respects the characteristics of a Schot-

tky diode are similar to a regular diode. *Table 8* gives the high and the low level voltages for both the devices:

Table 8. High and Low Level Voltages for TTL (Driving Device) and Delta39K (Receiving Device)

Receiving device	Driving device
V_{IH} = 2V(min.)–3.6V(max.)	V_{OH} = 2.4V(min.)
V_{IL} = 0.8V (max.)	V_{OL} = 0.8V(max.)
	$I_{OH\ (TTL)}$ = 5 mA V_{CC} = 5V

When designing interface circuitry, care should be taken that the I_{OH} specification of the driving device is not exceeded. In many of the interface circuits described by this application note, the source current is limited by a resistor. To ensure the I_{OH} specification is not exceeded, (0.5) x I_{OH} is used when solving for the required resistor values. This is done to attain resistor values within the specified I_{OH}.

$$R = \frac{V_{CC} - V_{Diode} - V_{Clamp}}{(0.5) \times I_{OH(MAX)}}$$

Here V_{Clamp} is 3.3V, V_{CC} is 5V and V_{Diode} is 0.3V. The R value can be calculated as

$$R = \frac{(5.0 - 3.6)}{(0.5) \times 5 \times 10^{-3}} \cong 60\Omega$$

This is a standard value for 5% and 10% tolerant resistors. Variances in the actual resistor value can be tolerated since a maximum source current of 0.5 X I_{OH} was targeted. Also if we use a 5% tolerant resistor,

Maximum value of the resistance = 560 + 5% of 560

=> 560 + 0.05X560 = 588Ω

The minimum current produced =

$$\frac{5 - 3.6}{588} = 2.3mA$$

The minimum value of the resistance = 560 – 5% of 560

=> 560 - 0.05X560 = 532Ω

The maximum current produced =

$$\frac{5 - 3.6}{532} = 2.6mA$$

The diode clamp ensures the input voltage of the Delta39K device does not exceed 3.6V. A carefully chosen resistor value ensures the source current requirement of the driving device is not exceeded. Therefore a successful interface between the devices has been achieved.

(iii) Using a Zener Diode

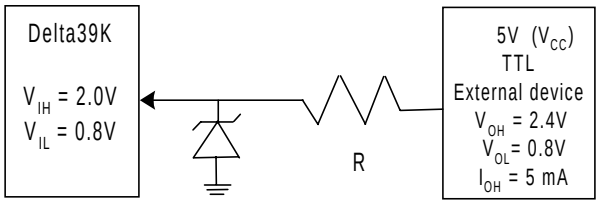

Figure 8. Zener Diode

The simplest form of a constant voltage supply is the Zener diode. It is a diode operating in the reverse-bias region. To use it to output a constant voltage, it is better to provide a roughly constant current. If the current flow from the external device is fairly constant, the Zener diode can be used to limit the voltage at a certain level which is determined by the Zener breakdown voltage. The Zener diode can be selected based on the breakdown voltage. Zeners are available in selected voltages from 2 to 200V to a 5–10% tolerance.

Here the Zener is selected to have a breakdown voltage of 3.3V at 5mA. The required resistance value is determined by the following calculation:

$$R = \frac{V_{CC} - V_{Zener}}{(0.5) \times I_{OH(Max)}}$$

$$= \frac{(5.0 - 3.3)}{(0.5) \times 5 \times 10^{-3}} \cong 680\Omega$$

$=> R \simeq 680\Omega$

This is a standard value for 5% and 10% tolerant resistors.

The output voltage will always be 3.3V as the breakdown voltage for the Zener is selected to be 3.3V. The input voltage never exceeds the $V_{IH(MAX)}$, thus satisfying the voltage requirement discussed in the Case(i) *Figure 1* and *Figure 2*. Since source current is also maintained below I_{OH}, a successful interface will be achieved.

Some regular Zener diodes have poor voltage tolerances. To overcome this, it is recommended to use a Zener with a breakdown voltage (after the voltage tolerance effect) lesser than the maximum input voltage of Delta39K. This is to ensure that the specifications for the Delta39K are not violated and the conditions discussed in Case(i) are met. For example, it is recommended to use a regular Zener with 3.3V breakdown so that even with a 10% voltage tolerance, the voltage doesn't exceed the maximum input voltage of Delta39K.

(iv) Using a Diode

Another solution would be to use a diode to clamp the voltage to the V_{CCIO} of the Delta39K.

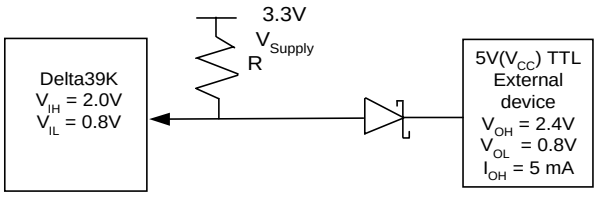

Figure 9. Diode Clamp

The most important concern in designing this circuit is choosing a resistor value that limits the sink current into the driving device.

For example, ***when the device is driving low***, and assuming you want to limit the sinking current to be around 2.5 mA, the resistor should be:

$$R = \frac{V_{Supply} - V_{CC}}{2.5 \times 10^{-3}}$$

$$\Rightarrow \quad \frac{3.3 - 0}{2.5 \times 10^{-3}} = 1.32k\Omega$$

The standard 5% or 10% resistor with a value close to this is 1.2 kΩ.

When the 5V device is driving high, the diode is reverse biased. Hence there is no effect of the voltage and the source current when the device is driving high.

D. Using a CMOS Device to Drive the Delta39K Device

All the solutions discussed for interfacing TTL devices to Delta39K can be used to interface CMOS devices to Delta39K. To convert the solution, V_{CC}, I_{OH} and the I_{OL} values should be replaced with the equivalent CMOS values. V_{CC} for TTL and CMOS devices are the same, so the user should be mainly concerned with staying within the current rating for the CMOS device.

Bidirectional Voltage Translation

The methods described above are sufficient for translating unidirectional signals. There are three solutions for bidirectional voltage translation. They are: using a diode translator, using a Split-Rail transceiver and using a buffer (Ultra37000™).

(i) Using a Diode Translator

To have voltage translation in both the directions, the only way to use any of the previous solutions would be to create a block of logic consisting of two back-to-back unidirectional translators. One such example is discussed here. This solution uses a clamp diode circuit back-to-back.

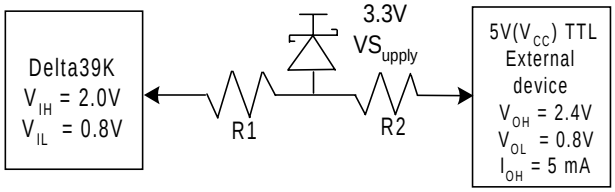

Figure 10. Diode Translator

The most important factor to be considered here is that the voltage supply of 3.3V has to be isolated from the rest of the supplies. This is important because in this circuit a lot of current is sunk into the diode which will add noise. If the same voltage is given to the other devices on the board, this will cause device reliability issues. Hence it is recommended to isolate the voltage supply to the diode from the other supplies. Also in this case, the resistor values have to be carefully selected. As in the earlier solution for unidirectional translation, the resistors should be large enough to limit the source current of the driving device and also should be small enough to allow switching of the outputs. The Delta39K driving TTL device does not cause any problems for this interface as the voltage levels meet the specified conditions as discussed earlier in this application note.

When the TTL device is driving the Delta39K, the resistor values for the above circuit can be calculated as follows:

$$R = \frac{V_{CC} - V_{Diode} - V_{Supply}}{(0.5) \times 5 \times 10^{-3}}$$

$$\frac{5 - 3.6}{2.5 \times 10^{-3}} = 560\Omega$$

The R1 resistor can be of the same value as the R2 as this resistor does not have much effect in either cases. However, it is recommended not to use a resistor of much higher value as this may effect the rise time of the outputs in both the translations.

Hence R1 and R2 can be 560 ohms.

This is a standard value for 5% and 10% resistors.

Fortunately, a number of manufacturers produce buffers which translate bidirectionally between two different voltage levels. These are the most practical solutions for bidirectional translation between 3V to 5V. A good example of this device would be the Split-Rail transceiver from TI.

(ii) Split-Rail Transceiver

These are bus transceivers with adjustable output voltages and three-state outputs. The function of these devices is to transmit data from port A to port B or from port B to A and to perform bus isolation.

The width of the bus depends on the design requirement.

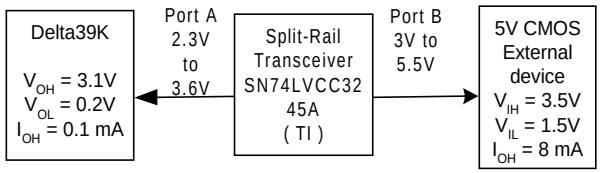

Figure 11. Split-Rail Transceiver

An example of this is SN74LVCC3245A which is an octal Split rail transceiver from TI. The timing for this device is given in *Table 9*.

Table 9. Timing for SN74LVCC3245A

Parameter	From (Input)	To (Output)	V_{CCA} = 2.7 to 3.6V	V_{CCB}=5V± 0.5V
			Min. (ns)	Max. (ns)
T_{PHL}	A	B	1	6
T_{PLH}	A	B	1	5.3
T_{PHL}	B	A	1	5.8
T_{PLH}	B	A	1	7
T_{PZL}	(not) OE	A	1	9.2
T_{PZH}	(not) OE	A	1	9.5
T_{PZL}	(not) OE	B	1	8.1
T_{PZH}	(not) OE	B	1	8.4

For more information on this device, please refer to the data sheet at the link given below:

http://www-s.ti.com/sc/psheets/scas585i/scas585i.pdf

(iii) Using Ultra37000™

Another possible solution would be to use an Ultra37000V™ CPLD for bidirectional buffering. A CY37032V is a 3.3V device with 5V tolerant inputs. The propagation delay of this device is similar to other buffers at 6.2 ns. The user may also be able to take advantage of the device's non-volatile logic for power-up control or other purposes. Like the buffer solutions, no external circuitry is required to use a CY37032V as an interface solution. The data sheet for these devices is available on the Cypress web site. The link to this is given below:

http://www.cypress.com/cypress/prodgate/cpld/37000.html

PCI Compliance

Delta39K supports 3.3V PCI but not 5V PCI. One solution to make the I/Os 5V tolerant could be to use an external clamp. However, clamping directly to 3.3V with a simple diode must never be used in a PCI 5V signaling environment as these high clamp diodes have a negative effect on both signal quality and device reliability. Also, this can lead to violations in PCI timing specifications.

Trade-Offs in Mixed Voltage Systems

Interfacing Delta39K devices to 5V devices has the same disadvantages as any other mixed voltage scenario. One of the major drawbacks of mixed voltage systems is additional current consumption. Devices that use ACT/HCT logic for 3.3V to 5V translation have additional power consumed, per input pin, if an input high is less than V_{CC} – 2.1 V. This number can be up to 1.5 mA per input pin. In a worst case situation, this could be a major source of continuous current consumption. This is the maximum value, though typically the extra current will amount to 100 to 200 µA per input pin. Additionally, this specification only applies to a logic '1' input.

Any of the above mentioned methods used to translate from one voltage to another requires additional current. In addition to current, these extra devices increase the system size, cost and complexity.

Invalid Solutions

Using a Delta39K to Drive a 5V CMOS Device

Using a pull-up resistor with Delta39K to drive 5V TTL device is an invalid solution:

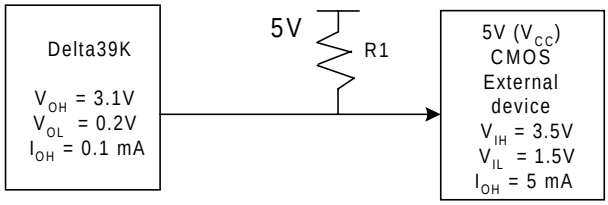

Figure 12. Pull-up Resistor (Invalid)

V_{CCIO} = 3.3V, V_{CC} (5V device) = 5V

$I_{OH(MAX)}$ of Delta39K at LVTTL = 4 mA

When Delta39K three-states the output, approximately 5V will be on the I/O which exceed the data sheet specifications of Delta39K.

Using a 5V TTL Device to Drive the Delta39K

Another solution which is invalid is to use a resistive divider circuit with a TTL device to drive a Delta39K. The given circuit is a simple resistive divider. Assuming the same conditions as in the earlier solutions, the values of the R1 and R2 can be found. Finding the appropriate resistors to satisfy the requirement for the complete voltage ranges is almost impossible.

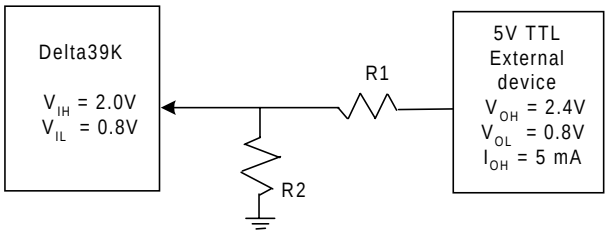

Figure 13. Resistive Divider

The complete voltage range is given below.

V_{IH} =2V(min.)–3.6V(max.) V_{OH} =2.4V(min.)–5.25V (max.)

V_{IL} = 0.8V(max.) V_{OL} = 0.8V(max.)

Let us assume the maximum conditions first. Using the maximum values, the R1 and R2 can be calculated as:

$$\frac{(5.25)}{R1 + R2} = 5x10^{-3}$$

=> R1 + R2 = 1050Ω

Also, V_{IN} (input to Delta39K) = I x R2

=> 3.6 = 5 x 10^{-3} x R2

$$\frac{3.6}{5 \times 10^{-3}} = R2$$

R1 + R2 = 1050 => R2 = 720Ω and

R1 = 330Ω

Using these resistor values, calculating the current for the minimum voltage levels:

$$\frac{2.4}{1050} = (2.3) \times 10^{-3} \text{ A}$$

=> 2.3 x 10^{-3} x 330 = 0.75V

This voltage doesn't meet the data sheet requirements.

Hence we have seen that it is impossible to meet the voltage requirements for the complete range of input and output voltages.

Conclusions

Using the solutions provided in this application note, Delta39K can be a part of a mixed voltage (5V and 3.3V) system. Interfaces between the Delta39K and 5V devices are accomplished with external circuitry.

In situations where Delta39K must be interfaced to 5V devices, this application note provides an excellent guide for reaching a successful solution.