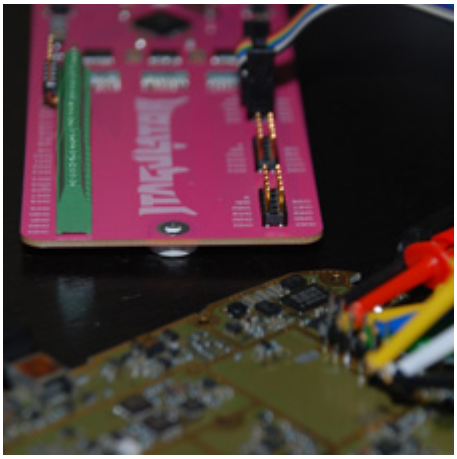
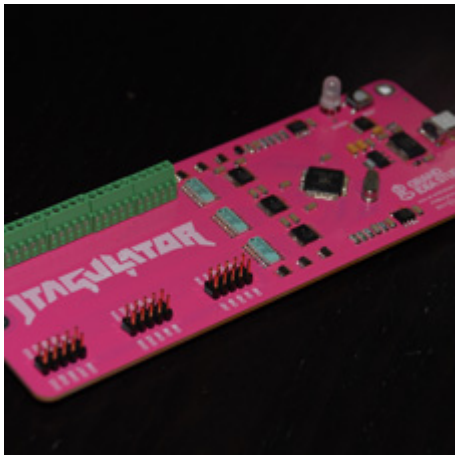
Grand Idea Studio

JTAGulator®

On-chip debug (OCD) interfaces can provide chip-level control of a target device and are a primary vector used by engineers, researchers, and hackers to extract program code or data, modify memory contents, or affect device operation on-the-fly. Depending on the complexity of the target device, manually locating available OCD interfaces can be a difficult and time consuming task, sometimes requiring physical destruction or modification of the device.

JTAGulator is an open source hardware tool that assists in identifying OCD interfaces from test points, vias, component pads, or connectors on a target device.

Assembled JTAGulators are available from Parallax, Inc. For questions and technical support, please contact support@parallax.com. Support is only provided for genuine JTAGulators, which are hot pink in color and contain verifiable serial numbers.

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Features:

- Detection of JTAG/IEEE 1149.1, ARM SWD, and UART/asynchronous serial
- Direct connection to sigrok and OpenOCD
- 24 channels with input protection circuitry
- Adjustable target I/O voltage for level translation: 1.4V to 3.3V
- USB interface for menu-based control from host computer

Documentation:

- Wiki (GitHub)
- Frequently Asked Questions (GitHub)
- Block Diagram
- Schematic
- Bill-of-Materials
- Assembly Drawing
- PCB: Gerber Plots and OSH Park
- Test Procedure and Video (YouTube) (Revised February 26, 2021, v2.1)
- Source Code: Parallax Propeller (GitHub) (Revised April 6, 2023, v1.11.1)
- Development Tool: Parallax Propeller Tool for Windows (v1.3.2)

Additional Resources:

- Video: New Feature Update (YouTube)
- Video: Introduction and Demonstration (Expanded) (YouTube)
- Video: Updating Firmware (YouTube)
- Video: Pin Mapper (EXTEST Scan) (YouTube)
- Video: Black Hat Asia 2014: JTAGulator Part 1 and Part 2 (YouTube)
- Slides: JTAGulator: Assisted discovery of on-chip debug interfaces (Revised September 16, 2018)
- Poem by Zach Houston

Raspberry Pi Zero W:

Environment to demonstrate JTAG, UART, and logic analyzer functionality.

- Notes
- Sample Code (Python 2.7.17)
- OpenOCD Configuration

Acrylic Case:

- Bill-of-Materials
- Bill-of-Materials (w/ Sparkle Add-On Board)
- Design Files
- Assembly Video (YouTube)

Sparkle Add-On Board:

Provides neon pink underglow for maximum aesthetics. Connects to the JTAGulator with pogo pins. LEDs will turn on when the target voltage (VADJ) is set.

- Schematic
- Bill-of-Materials
- Assembly Drawing
- PCB: Gerber Plots and OSH Park
- Pictures (Flickr)

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Episode 161

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I'm a hacker who helps people ...
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