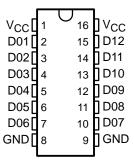
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- Designed to Reduce Reflection Noise
- Repetitive Peak Forward Current to 200 mA
- 12-Bit Array Structure Suited for Bus-Oriented Systems

description/ordering information

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 12-bit high-speed Schottky diode array suitable for clamping to $V_{\rm CC}$ and/or GND.

D, N, NS, OR PW PACKAGE (TOP VIEW)

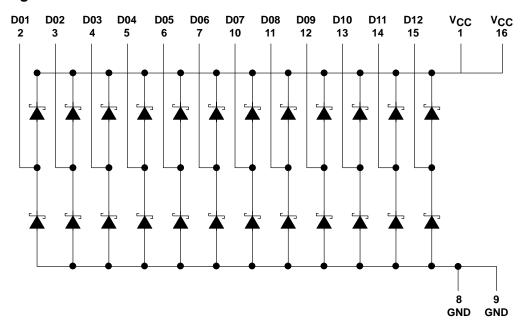


ORDERING INFORMATION

TA	PACK	AGET	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74S1051N	SN74S1051N
	SOIC - D	Tube	SN74S1051D	S1051
0°C to 70°C	3010 - 0	Tape and reel	SN74S1051DR	31031
	SOP - NS		SN74S1051NSR	74S1051
	TSSOP – PW	Tape and reel	SN74S1051PWR	S1051

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

schematic diagrams





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



SN74S1051 12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Steady-state reverse voltage, V _R		
Continuous forward current, IF: Any D termin		
Total through	all GND or V _{CC} terminals	170 mA
Repetitive peak forward current [‡] , IFRM: Any [
Total	through all GND or V _{CC} terminals .	1 A
Package thermal impedance, θ _{JA} (see Note 1): D package	73°C/W
•	N package	67°C/W
	NS package	64°C/W
	PW package	108°C/W
Operating free-air temperature range		0°C to 70°C
Storage temperature range, T _{stg}		–65°C to 150°C
b d th P - t - d d		T

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 2)

	PARAMETER	TEST C	ONDITIONS	MIN TYP§	MAX	UNIT
		To Voc	I _F = 18 mA	0.85	1.05	
\/_	V _F Static forward voltage	To V _{CC}	I _F = 50 mA	1.05	1.3	V
VF		From GND	I _F = 18 mA	0.75	0.95	V
		FIOIII GIND	I _F = 50 mA	0.95	1.2	
V _{FM}	Peak forward voltage		I _F = 200 mA	1.45		V
	Static reverse current	To V _{CC}	V _R = 7 V		5	
^I R	Static reverse current	From GND	vR = 1 v		5	μΑ
C.	Total capacitance	$V_R = 0 V$,	f = 1 MHz	8	16	pF
Ct	rotal capacitance	$V_{R} = 2 V$,	f = 1 MHz	4	8	Pi

[§] All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

	PARAMETER	TEST CO	NDITIONS	MIN	TYP§	MAX	UNIT
	I Internal areastells ourment	Total I _F current = 1 A,	See Note 3		0.8	2	m ^
'X	Internal crosstalk current	Total I _F current = 198 mA,	See Note 3		0.02	0.2	mA

[§] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

NOTE 3: I_X is measured under the following conditions with one diode static, all others switching:

Switching diodes: $t_W = 100 \mu s$, duty cycle = 20%

Static diode: V_R = 5 V

The static diode input current is the internal crosstalk current, $I_{\rm X}$.

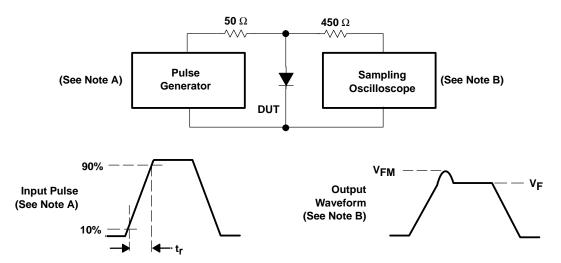
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

	PARAMETER		TEST CON	DITIONS		MIN	TYP	MAX	UNIT
t _{rr}	Reverse recovery time	$I_F = 10 \text{ mA},$	$I_{RM(REC)} = 10 \text{ mA},$	$I_{R(REC)} = 1 \text{ mA},$	$R_L = 100 \Omega$		8	16	ns



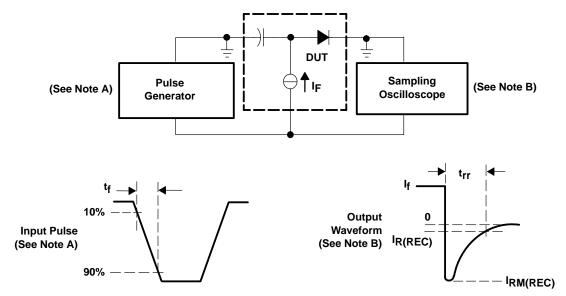
[‡] These values apply for $t_W \le 100 \mu s$, duty cycle $\le 20\%$.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_f = 20$ ns, $Z_O = 50 \Omega$, freq = 500 Hz, duty cycle = 1%.
 - B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_{\Gamma} \le 350$ ps, $R_i = 50 \Omega$, $C_i \le 5$ pF.

Figure 1. Forward Recovery Voltage



- NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_f = 0.5$ ns, $Z_O = 50 \Omega$, $t_W \ge 50$ ns, duty cycle = 1%.
 - B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \le 350$ ps, $R_i = 50 \Omega$, $C_i \le 5$ pF.

Figure 2. Reverse Recovery Time

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APPLICATION INFORMATION

Large negative transients at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1051 diode termination array helps suppress negative transients caused by transmission-line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split-resistor or Thevenin-equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver reduce negative transients, but they also can increase propagation delays down the line because a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current when the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. Typical current-versus-voltage curves for the SN74S1051 are shown in Figures 3 and 4.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 5 was evaluated. The resulting waveforms with and without the diode are shown in Figure 6.

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when the diode arrays are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

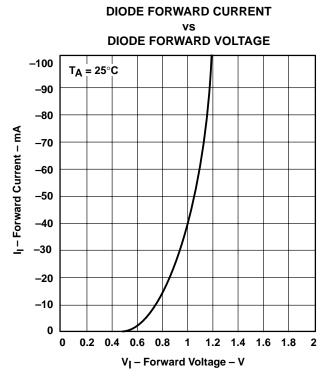


Figure 3. Typical Input Current vs Input Voltage (Lower Diode)



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DIODE FORWARD CURRENT vs DIODE FORWARD VOLTAGE

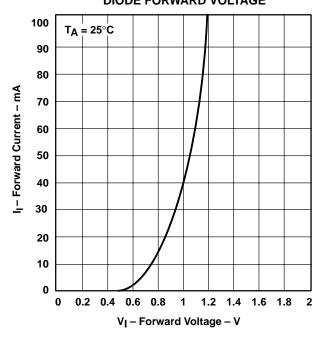


Figure 4. Typical Input Current vs Input Voltage (Upper Diode)

APPLICATION INFORMATION

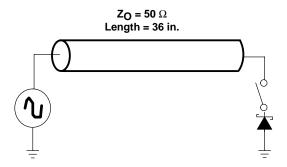


Figure 5. Diode Test Setup

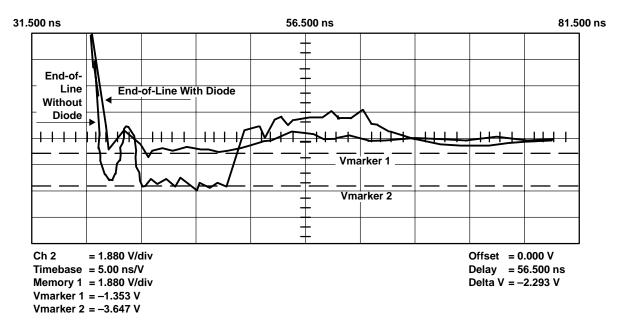


Figure 6. Reduction of Negative Transients at the End of a Transmission Line



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PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
SN74S1051D	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	S1051	
SN74S1051DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	S1051	Samples
SN74S1051N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S1051N	Samples
SN74S1051NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74S1051	Samples
SN74S1051PW	LIFEBUY	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	S1051	
SN74S1051PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	S1051	Samples

(1) The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74S1051DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74S1051NSR	so	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74S1051PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

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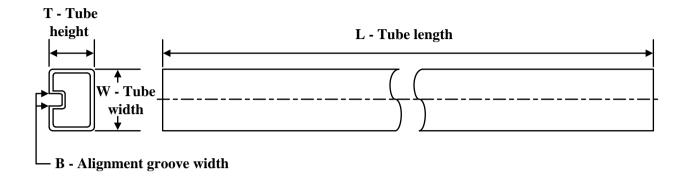
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74S1051DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74S1051NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74S1051PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

PACKAGE MATERIALS INFORMATION

www.ti.com 3-Jun-2022

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74S1051D	D	SOIC	16	40	507	8	3940	4.32
SN74S1051N	N	PDIP	16	25	506	13.97	11230	4.32
SN74S1051N	N	PDIP	16	25	506	13.97	11230	4.32
SN74S1051PW	PW	TSSOP	16	90	530	10.2	3600	3.5

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOP



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOF



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOF



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.





SMALL OUTLINE PACKAGE



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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