Circuit Theory and Electronics Fundamentals

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Laboratory Four Report

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1 Introduction

The main goal of this laboratory assignment is to design a circuit of an audio amplifier and to analyse it theoretically, as well as simulating it using Ngspice.

To successfully create this circuit we had to architecture the gain stage and the output stage

We were also asked to analyse quantitatively the quality of the designed circuit using the Merit expression presented bellow.

$$Merit = \frac{VoltageGain * bandwidth}{Cost * CutoffFreq} \tag{1}$$

2 Simulation Analysis

Before proceeding the theoretycal analysis, we simulated the circuit via the Ngspice software in order to perfect our parameters‘ values.

Parameters	Values
vcc[0]	0.000000e+00,0.000000e+00
in[0]	1.000000e+00,0.000000e+00
in2[0]	9.462362e-01,-4.02794e-02
base[0]	8.821295e-01,4.528835e-02
coll[0]	-6.90782e+01,-4.06314e+01
emit[0]	3.972570e-01,-4.00299e-01
emit2[0]	-6.54598e+01,-2.85270e+01
out[0]	-1.03656e+01,-4.20939e+01

Table 1: Parameters‘ values.

To simulate the transistor behaviour, we utilized the NPN and the PNP models provided by the professor.

We performed transient and frequency analysis of the combined gain and output stages, that represent, respectively, the common emitter and collector amplifiers.

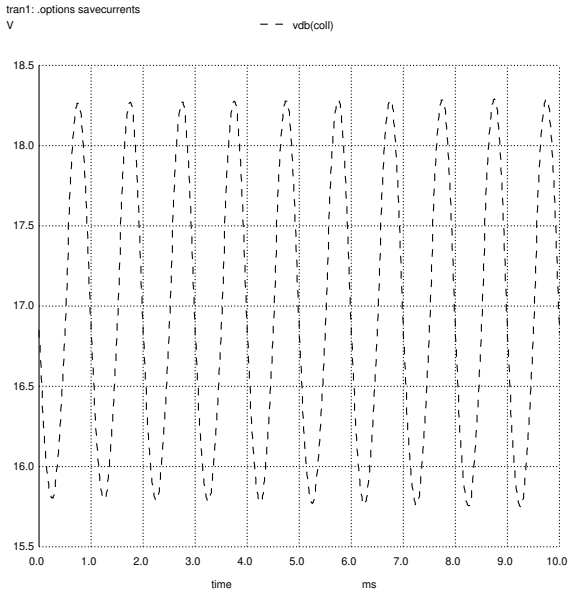

Figure 1: Voltage in the collector, transient analysis.

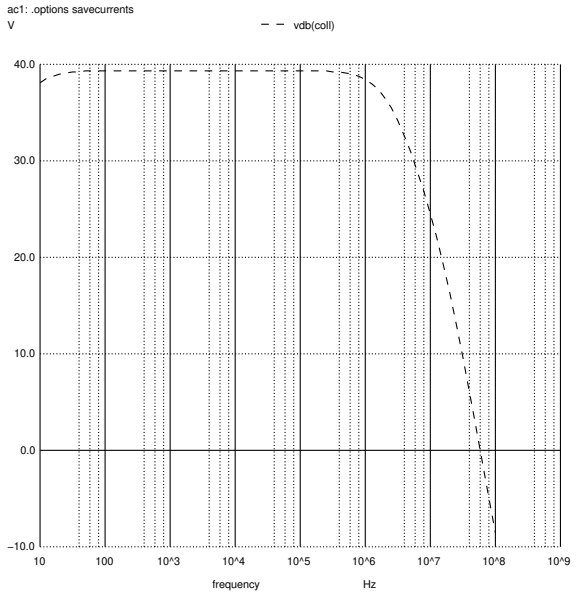

Figure 2: Voltage in the collector[dB], frequency analysis.

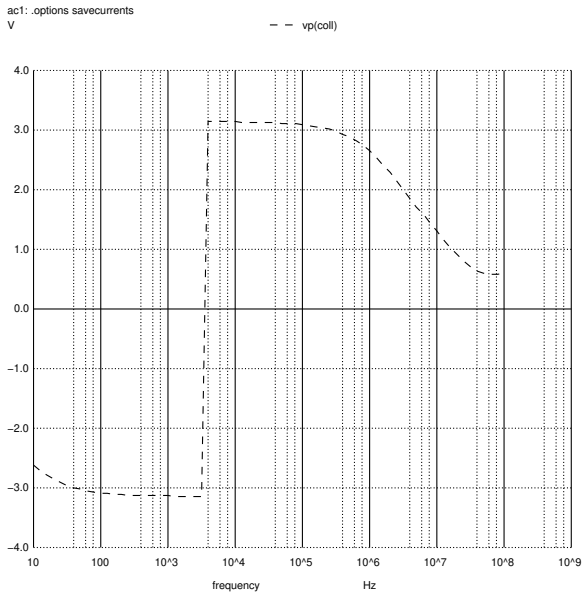

Figure 3: Phase voltage in the collector, frequency analysis.

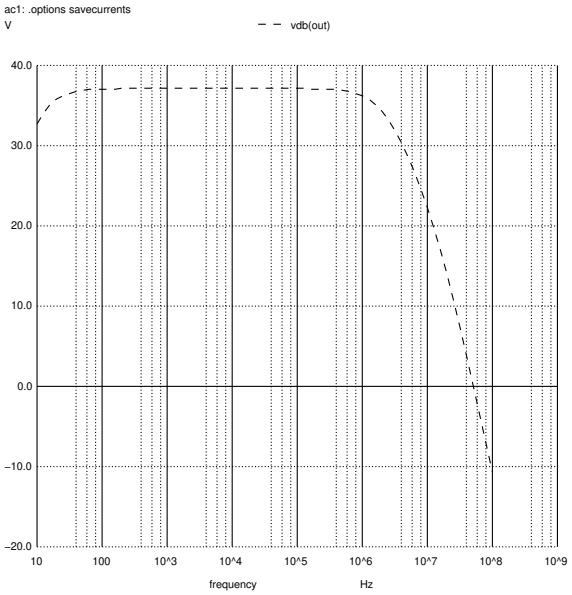

Figure 4: Output voltage[dB].

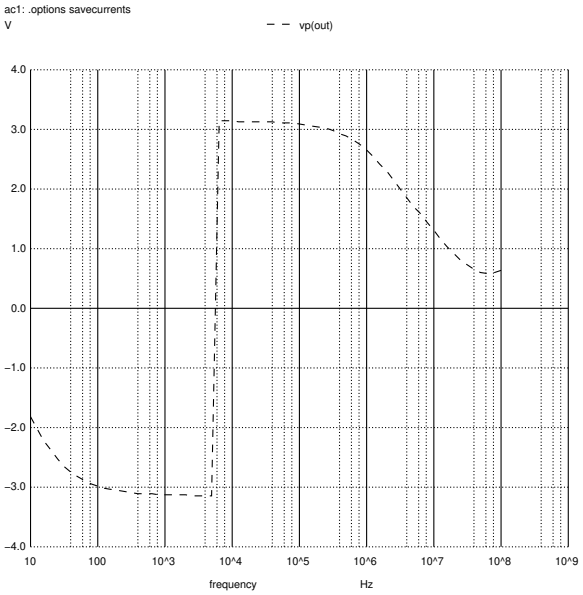

Figure 5: Output voltage phase.

From the simulation we were able to compute the important values of the cut-off frequencies, the gain and the bandwidth, which allowed us to calculate our merit. Furthermore, we found the values for the input and output impedances.

Parameters	**Values**
bandwidth	2.097646e+06
fup	2.097659e+06
flow	1.268798e+01
gain	7.175559e+01
merit	2.644085e+03
cost	4.486628e+03
impedin	9.895030e+01,-9.74274e-01

Table 2: Values computed in the simulation.

Parameters	**Values**
impedout	7.818064e+04

Table 3: Output impedance.

3 Theoretical Analysis

In this section, we used the theorectical model as presented in the lectures. To do so we adopted the equations provided in lecture 16 and 17 and utilised the values of the circuit parameters, that we optimized with the help of Ngspice tool, as showcased previously.

The circuit was divided in two main parts, the gain and output stages. These were combined together because they complemented one another.

The gain stage which consists of a common emitter amplifier has the advantage of generating a high, desirable gain. However, along with this comes the cost of having a very high output impedance which squanders the gain.

Parameters	Values
—VT—	0.025000
—beta—	178.700000
—VA—	69.700000
—VBEON—	0.700000
—Vcc—	12.000000
—Req—	8461.538462
—Veq—	1.846154
—IB1—	0.000026
—IC1—	0.004613
—IE1—	0.004639
—V_{emit}—	0.927733
—V_{coll}—	6.925864
—VCE—	5.998131
—V_{base}—	1.627733

Table 4: Transistor‘s parameters.

Parameters	Values
—gm1—	0.184514
—ro1—	15109.960453
—rpi—	968.489933

Table 5: Parameters of slide 10, lecture 16.

In order to reduce the high impedance value that is associated with the gain stage, we developed an output stage that allows to rectify the problem we had previously. Once again, we followed the instructions given in the lectures.

Parameters	Values
—Input impedance—	869.023345
—Output impedance—	1025.354537
—Gain—	169.668298
—Gain(dB)—	44.592014

Table 6: Gain and impedances.

Parameters	Values
—V_{coll}—	6.925864
—V_{emit}—	7.625864
—Vcc—	12.000000
—IB2—	0.000087
—IC2—	0.019795
—IE2—	0.019882

Table 7: Parameter values for the output stage.

Finally, the gain results of the total circuit.

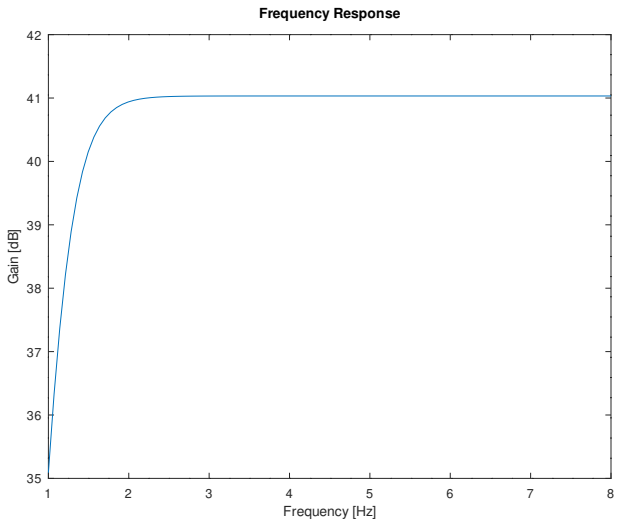

Figure 6: Plot of Gain in order of the Frequency (Hz).

Parameters	Values
—gm2—	0.791814
—go2—	0.000532
—gpi2—	0.003484
—ge2—	0.004545
—Input Impedance—	26837.230759
—Output Impedance—	1.249414
—Gain—	0.989304
—Gain(dB)—	-0.093408

Table 8: Output stage impedance and gain.

4 Conclusion

As one can conclude from observing and comparing the values of the theoretical and the simulation parts of the analysis, there are some glaring differences . This can be due to the fact that the models we are working with are characterized by their non-linearity, which explains the disparity found in our simulation work when compared to the analysis made susing Octave.

The main reason for these differences is the parameters defined by Ngspice for the used transitors (model BC547A for the NPN junction and model BC557A for the PNP junction). However, the complexity of these parameters makes the simulated model a reliable one that is very close to reality.

Nevertheless, we believe that this laboratory work was rather successful when considering the quality (merit) of the architectured circuit.