Bilkent University

Electrical and Electronics Department

EE102-01 Lab 3 Report:

“Combinational Logic Circuit”

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Purpose:

The main purpose of this experiment was to design a combinatorial circuit using logic-gates on a breadboard. Also, the experiment helped us understand how a 4-bit counter IC (74HCT163 counter) works. Different IC’s such as 74HC00N, 74HC02N and 74HC04N was also used in this experiment.

Methodology:

Firstly, before creating a combinatorial circuit the datasheet that was provided to students was examined in order to understand how a 4-bit counter IC (74HCT163) works. This was essential since most of us had no idea about a 4-bit counter and its applications at the start. In order to set the 74HCT163 to "Count" operating mode the following pins **(Figure 1.2)** should have been connected to necessary elements on the breadboard **(Figure 1.1)**. Also, a function generator was used to create a 5V Pk-Pk, 1Hz, square wave signal. Throughout the experiment all components were exposed to a 5V voltage difference. Here is the pin configuration for 74HCT163 that was used in this experiment:

MR (Pin 1): High

CP (Pin 2): Signal Generator (1Hz, 5V Pk-Pk, Square Wave Signal)

D_0, D_1, D_2, D_3 (Pin 3, 4, 5 and 6): Ground (It was later understood that it doesn't make a difference to not connect them to anything)

CEP (Pin 7): High

GND (Pin 8): Ground

PE (Pin 9): High

CET (Pin 10): High

Q_0, Q_1, Q_2, Q_3 (Pin 11, 12, 13 and 14): These pins are the data outputs of 74HCT163, and they will be the inputs of the logic gates that will be used later on in the experiment.

TC (Pin 15): Ground (It was later understood that it doesn't make a difference to not connect this pin to anything)

V_{cc} (Pin 16): High

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h h	↑ ↑	X X	X X	l l	l h	L H	L (1)
count	h	↑	h	h	h	X	count	(1)
hold (do nothing)	h h	X X	l X	X l	h h	X X	q_n q_n	(1) L

Notes

1. The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).
   H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
   q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
   X = don't care
   ↑ = LOW-to-HIGH CP transition

Figure 1.1: The Pin Configuration of "Count" Operation Mode

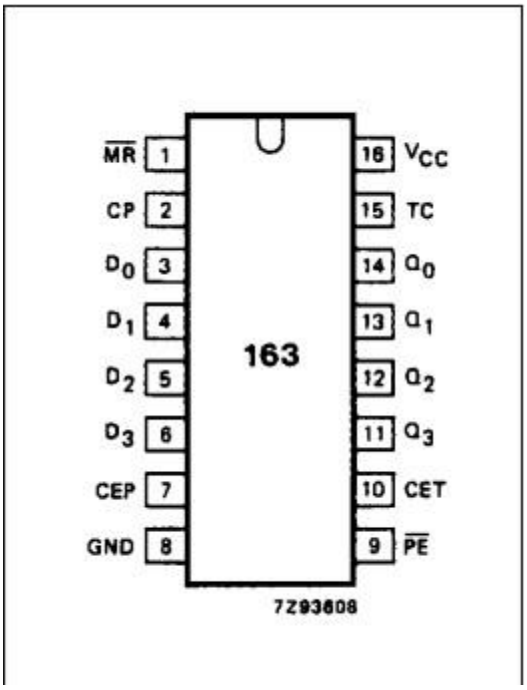

Figure 1.2: The Pin Configuration of 74HCT163

Here is some additional information about every single IC that was used in this specific experiment:

74HCT163 (Synchronous 4-Bit Binary Counter):

By using a certain pin configuration **(Figure 1.1)**, the IC starts to work in counter –also known as clock- mode. This certain pin configuration helps us capture four different synchronized output signals from Q_0, Q_1, Q_2 and Q_3 pins. Basically, 74HCT163 counts from 0 to 16 in binary with Q_0 being the least significant number. In the experiment, 74HCT163 was used as an input generator to other IC's.

74HC32N (Quad 2-Input or Gate):

74HC32N is an integrated circuit consisting of 4 independent or gates, a GND, and a V_{CC} pin with 14 pins in total. In this experiment, 4 signals coming from the 74HCT163 were connected to two different "or" gates in 74HC32N and two different output signals were generated.

74HC00N (Quad 2-Input Nand Gate):

74HC00N is an integrated circuit consisting of 4 independents nand gates, a GND, and a V_{CC} pin. In this experiment, 2 signals coming from the 74HC32N were connected to a single nand gate in 74HC00N and an output was generated.

74HC04N (Hex Inverter):

74HC04N is an integrated circuit consisting of 6 independent not gates, a GND, and a V_{CC} pin with 14 pins in total. In this experiment, the final signal coming from the 74HC00N was inverted via 74HC04N.

Setting up the breadboard, firstly MR (Pin 1), CEP (Pin 7), PE (Pin 9) and CET (Pin 10) pins were connected to high on the breadboard via white jumper cables **(Figure 1.3)**.

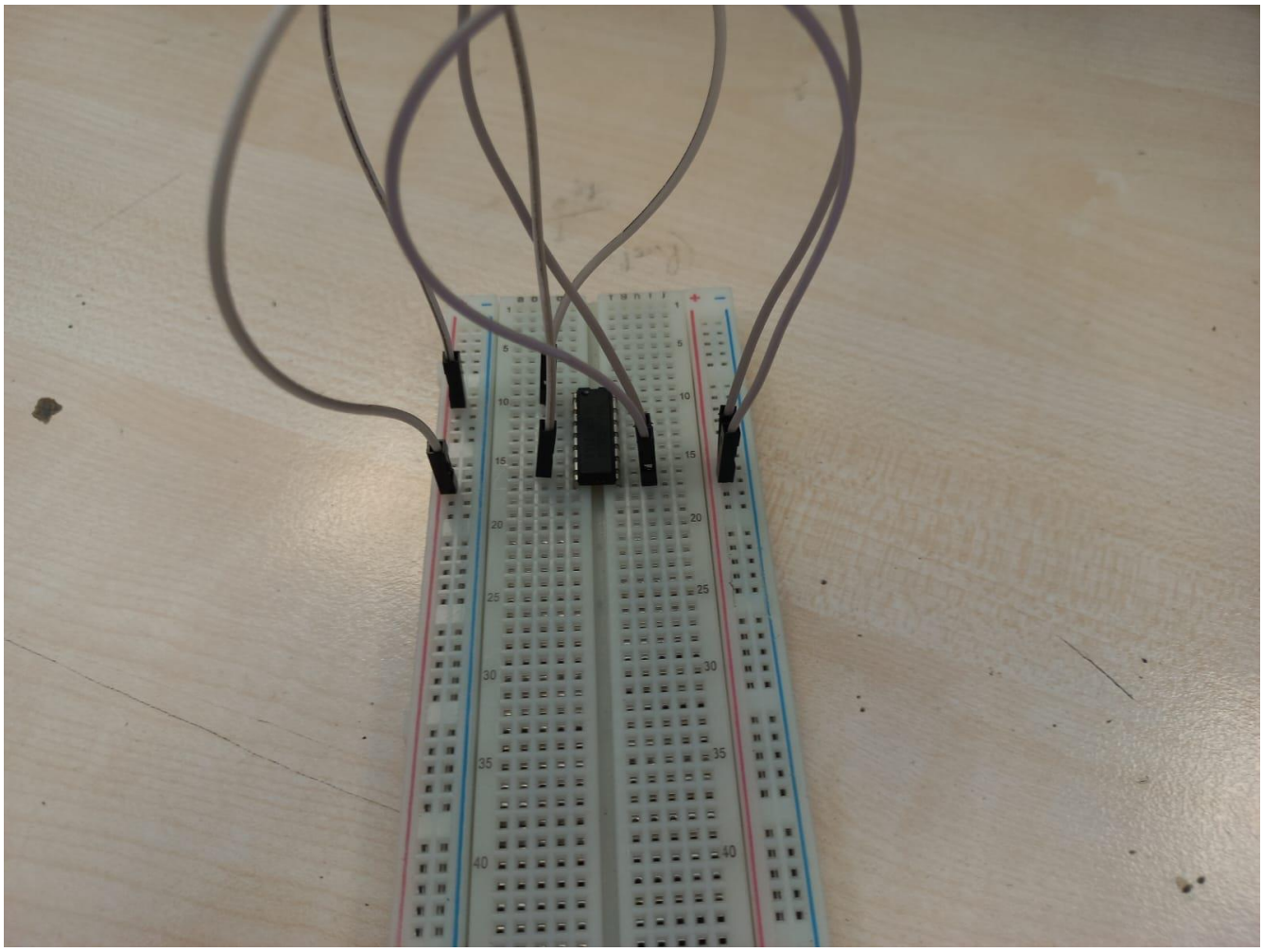

Figure 1.3: MR, CEP, PE and CET Pin Connections

Secondly D_0, D_1, D_2 and D_3 (Pin 3, 4, 5 and 6) pins were connected to ground terminals on the breadboard via green jumper cables **(Figure 1.4)**.

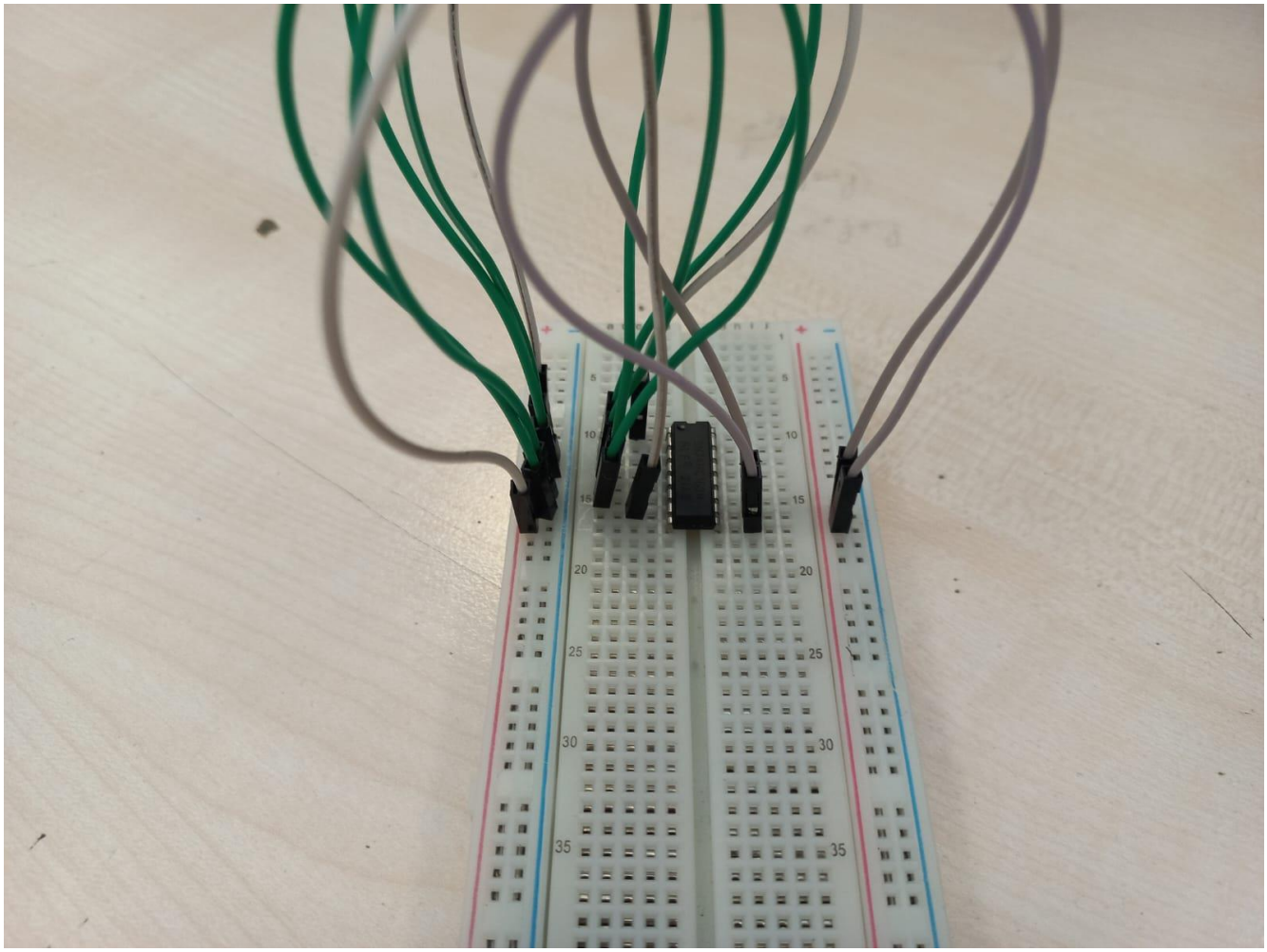

Figure 1.4: D_0, D_1, D_2 and D_3 Connections

Thirdly, V_{cc} (Pin 16), TC (Pin 15) and GND (Pin 8) were connected to high, ground and ground accordingly on the breadboard via black jumper cables **(Figure 1.5)**.

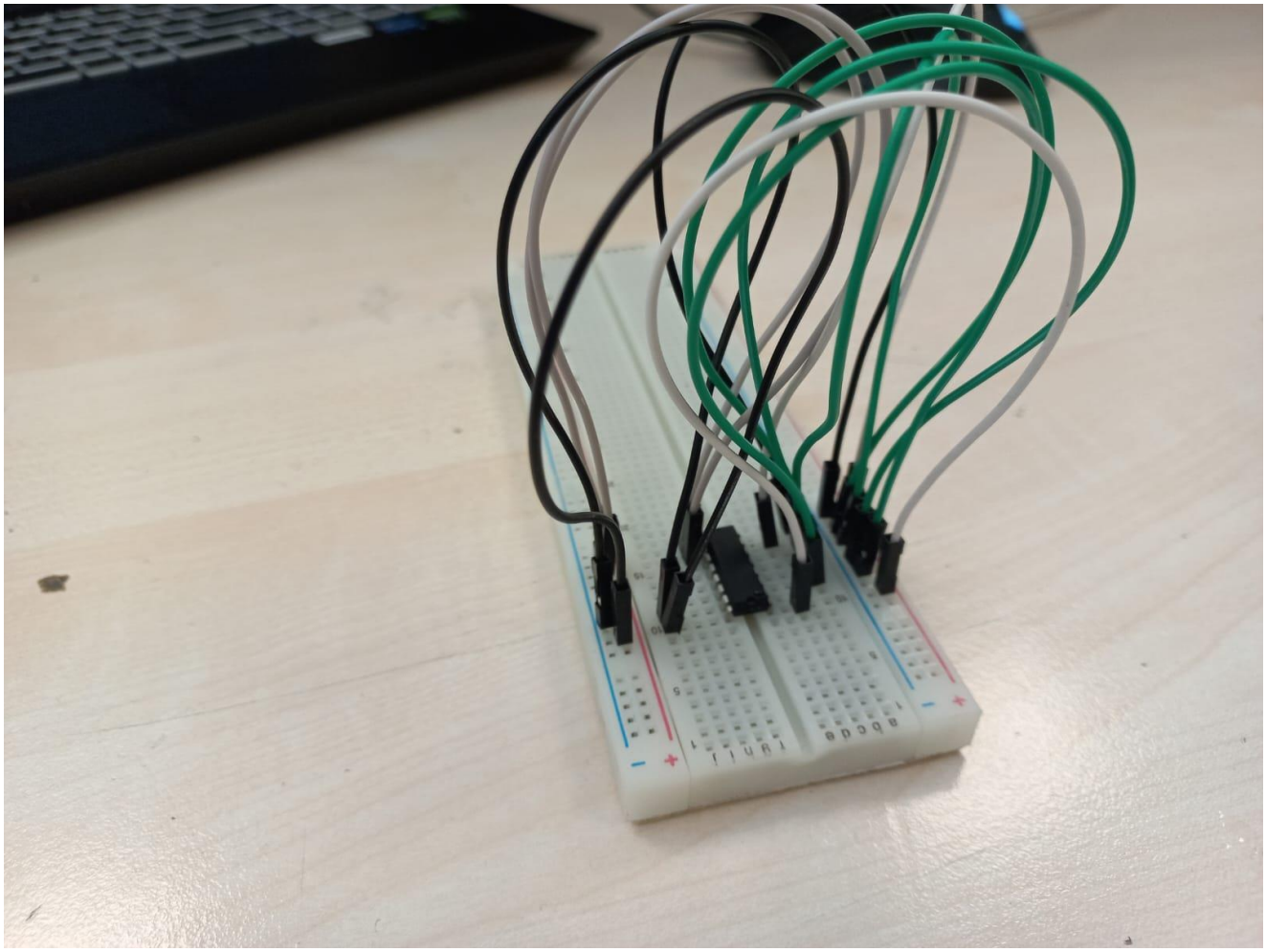

Figure 1.5: V_{cc} , TC and GND Connections

Then, Q_0, Q_1, Q_2 and Q_3 (Pin 11, 12, 13 and 14) pins were extracted from the 4-bit counter **(Figure 1.6)**. Here is the colour configuration of the jumper cables and signals:

Q_0: Yellow

Q_1: Purple

Q_2: Orange

Q_3: Blue

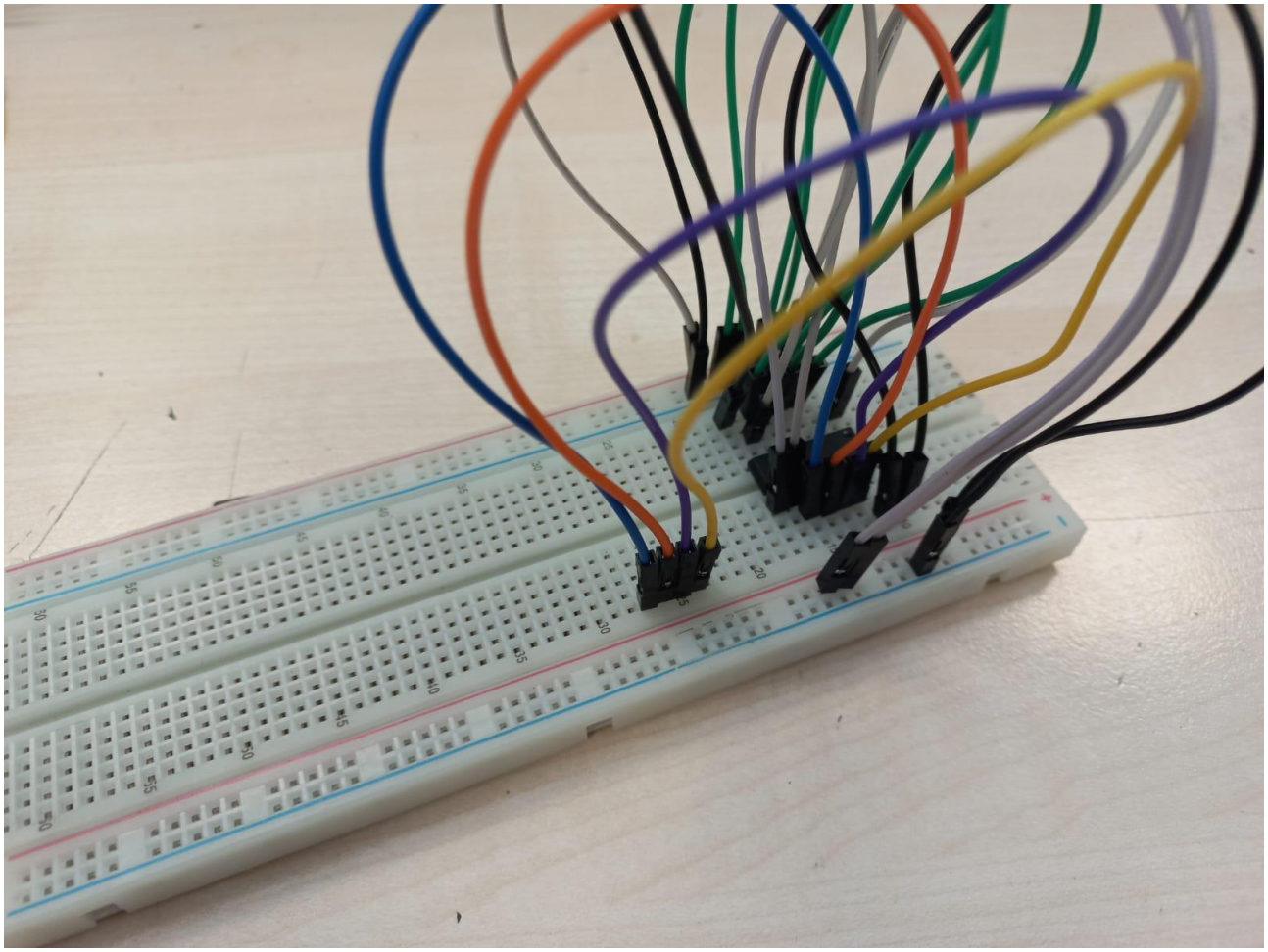

Figure 1.6: Q_0, Q_1, Q_2 and Q_3 Connections

Then, 74HC00N, 74HC02N and 74HC04N were connected to the breadboard **(Figure 1.7)**. The closest one to the counter (74HCT163) is quad 2-input or gate (74HC32N) and the farthest away is the hex-inverter (74HC04N). The one in the middle is quad 2-input nand gate (74HC00N).

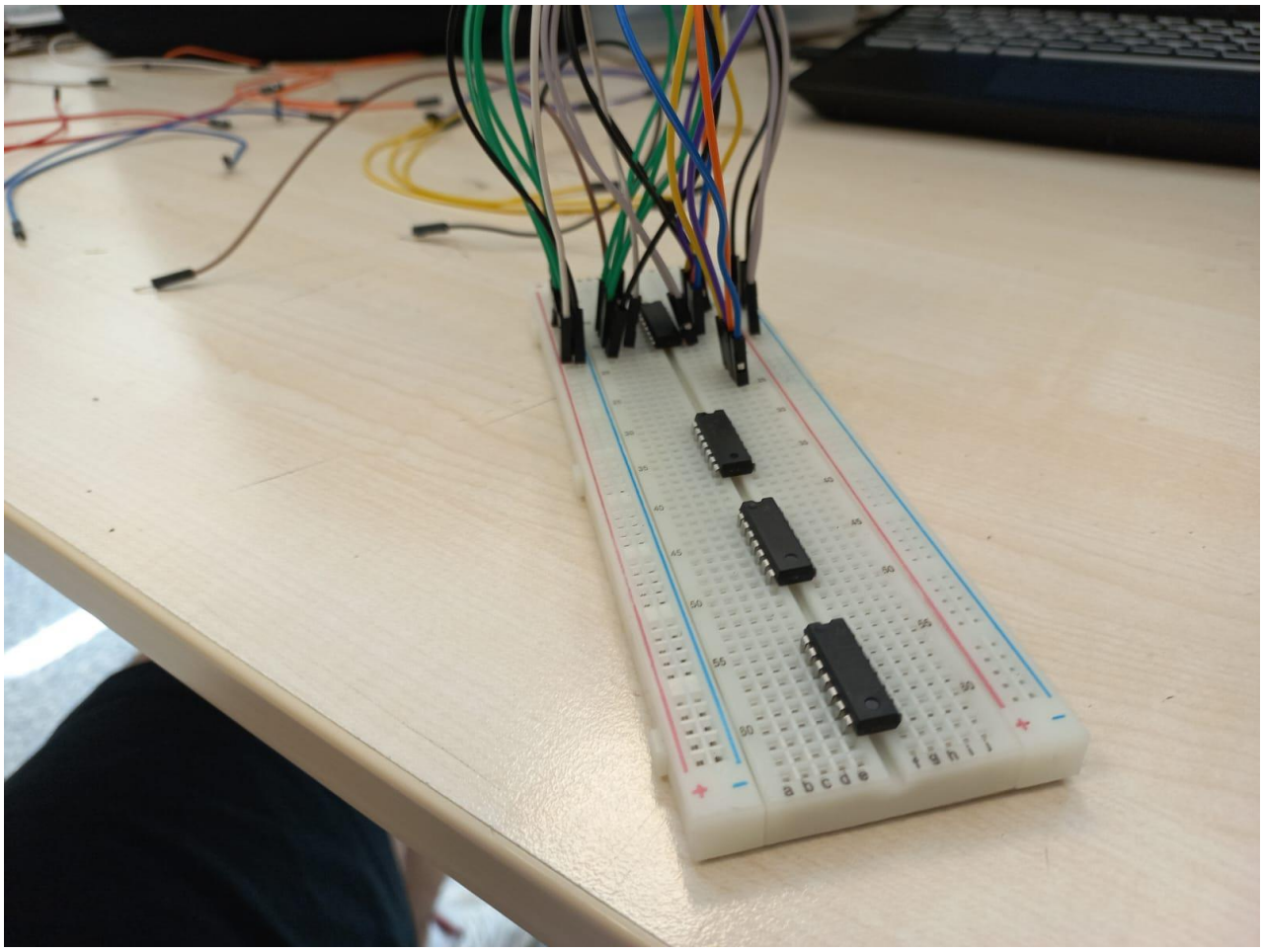

Figure 1.7: Other IC Connections

Then, 4 different signals that were extracted from the binary counter were connected to 2 different “or” gates on 74HC32N **(Figures 1.8 and 1.13)**. The white jumper carries the output signal of the logic equation “Q_0 or Q_1” and the brown jumper carries the output signal of the logic equation “Q_2 or Q_3”.

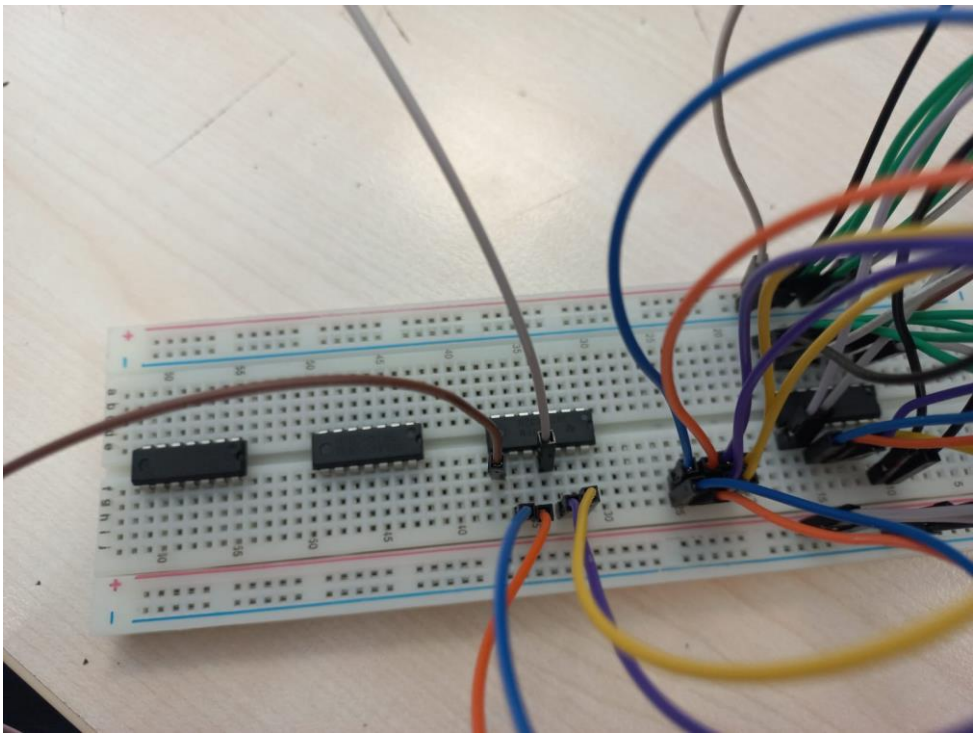

Figure 1.8: Jumper Cable Connections on 74HC32N

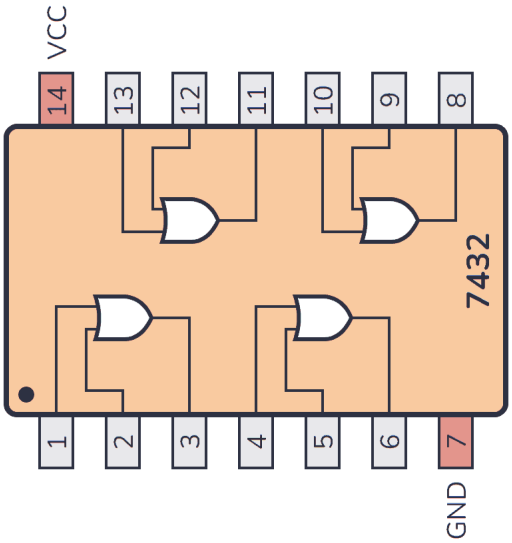

Figure 1.13: Pin configuration of 74HC32N

Then, 2 different signals, which are originated from the 74HC32N, were connected to a single “nand” gate on 74HC00N **(Figures 1.9 and 1.14)**. The blue jumper carries the output signal.

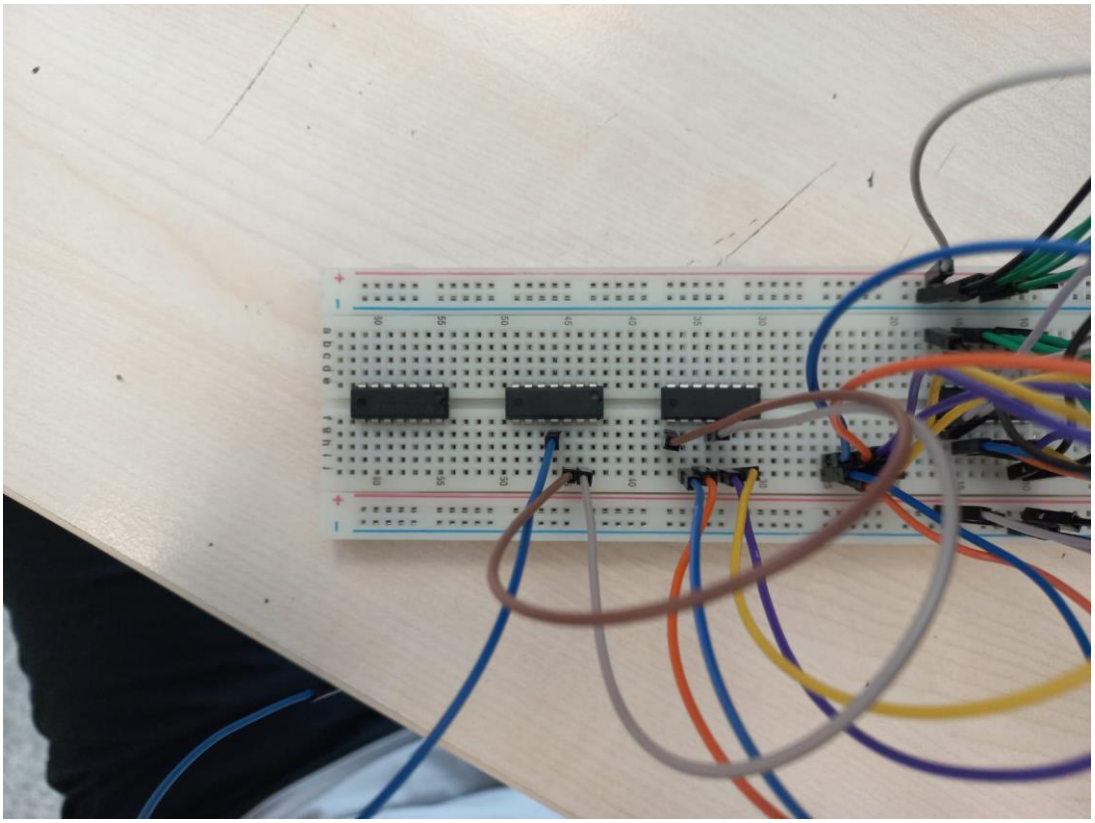

Figure 1.9: Jumper Cable Connections on 74HC00N

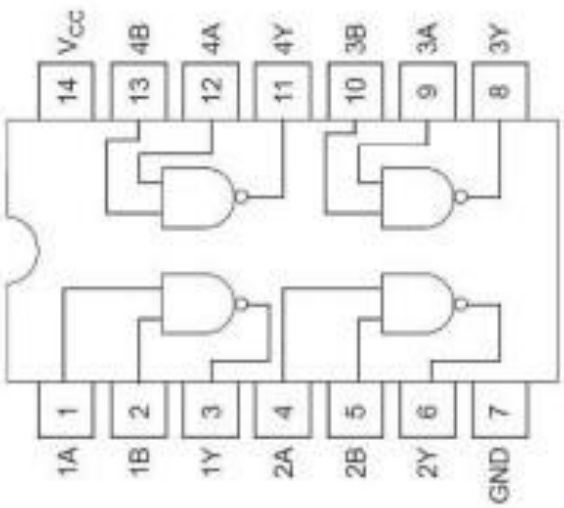

Figure 1.14: Pin Configuration of 74HC00N

Then, the signal coming from the 74HC00N were connected to a single “not” gate on 74HC04N **(Figures 1.10 and 1.15)**. The yellow jumper carries the final output signal.

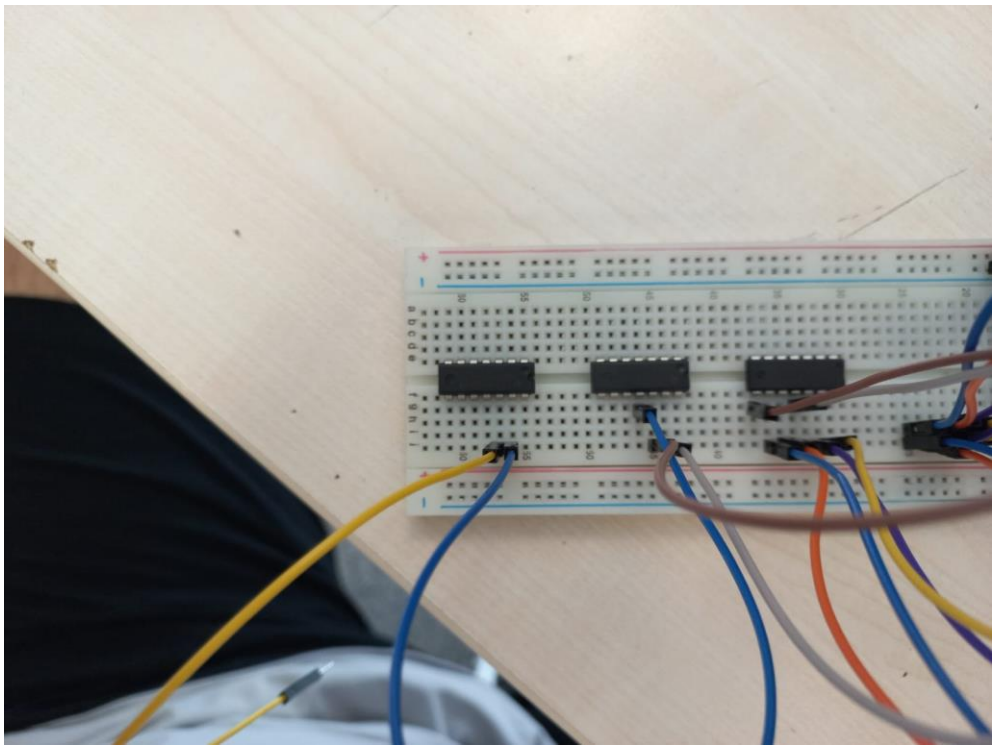

Figure 1.10: Jumper Cable Connections on 74HC04N

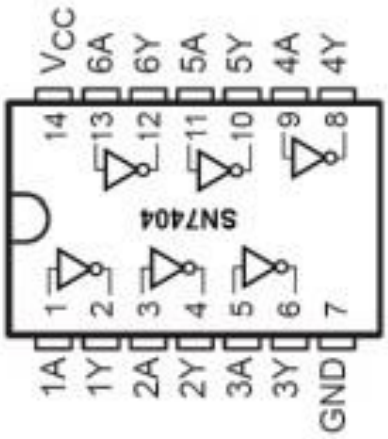

Figure 1.15: Pin Configuration of 74HC04N

Then, the V_{cc} and GND pins of all three IC's (74HC32N, 74HC00N and 74HC32N) were connected to high or ground accordingly **(Figure 1.11)**. This provided the IC's the voltage difference they needed to work properly. 4 red jumpers are used for 74HC32N and 74HC00N, whereas 2 white jumpers are used for 74HC04N.

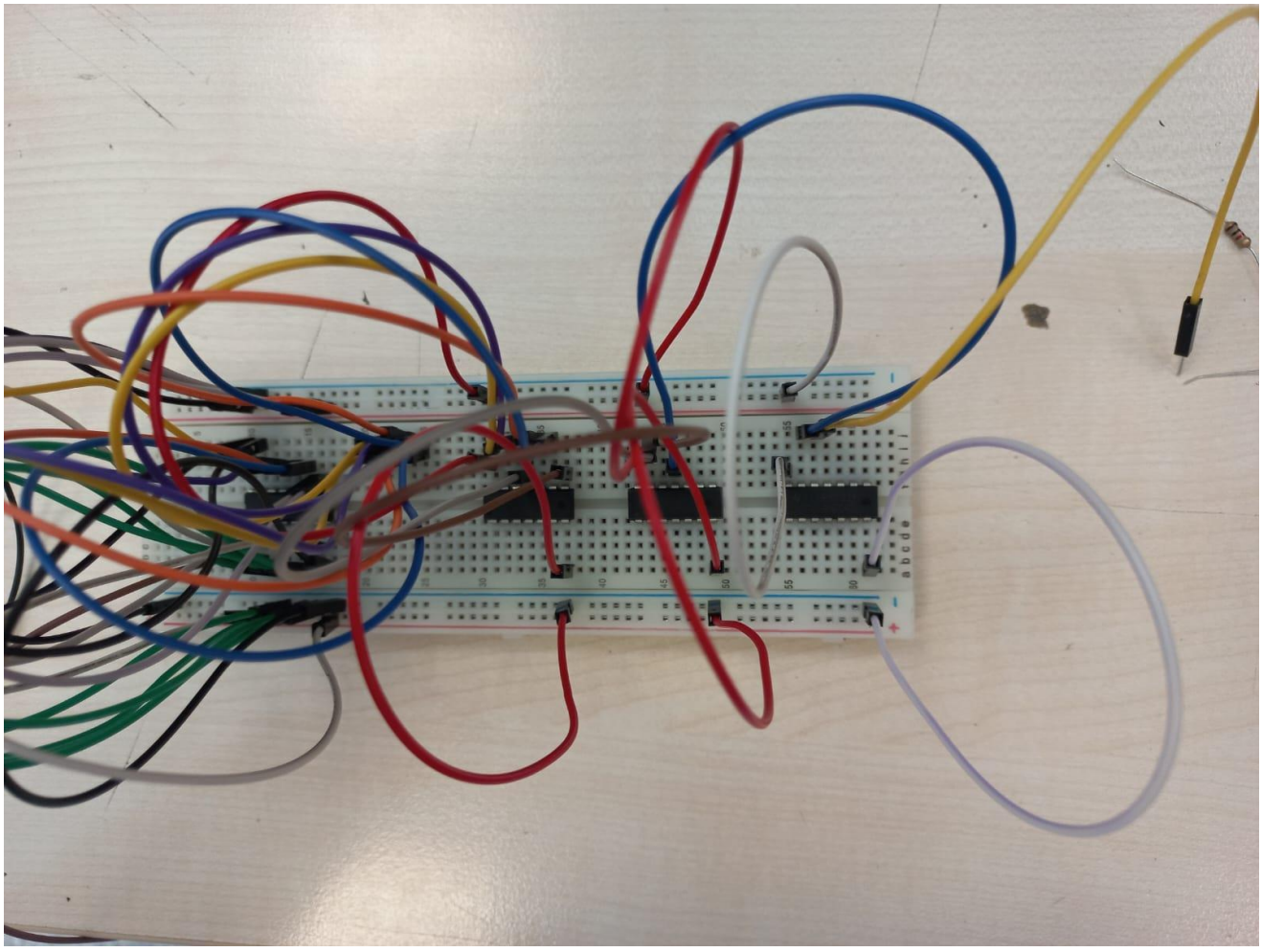

Figure 1.11: Jumper Cable Connections on V_{cc} and GND Pins of 74HC32N, 74HC00N and 74HC04N

Finally, after connecting 4 red LEDs on each output signal of the binary counter and a green LED for the final output of the combinatorial circuit, the circuit was ready to be tested. Function generator, voltage supply and oscilloscope were connected to the circuit on the proper elements. Also, this was the part of the experiment where it was realized that D_0, D_1, D_2, D_3 and TC pins of 74HCT163 were not necessarily had to be connected to the ground. The completed circuit on the breadboard was looking like this **(Figure 1.12)**:

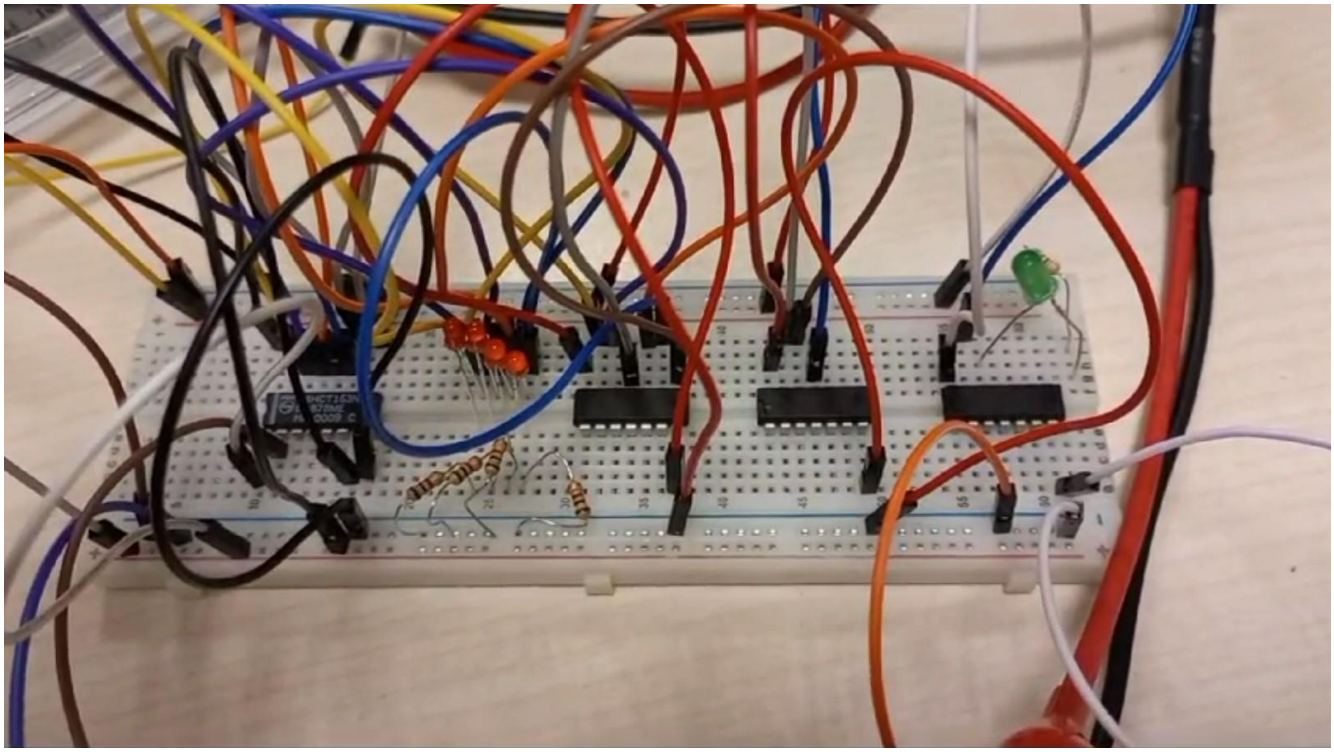

Figure 1.12: The Final Circuit on the Breadboard

Design Specifications:

In the designed logic circuit, there was four inputs (in1, in2, in3 and in4) and a single output (out1). Four inputs were connected to four different red LEDs and the out1 was connected to a green LED in order to be able to observe the input and output signals visually **(Figure1.12)**. Here is the simplest form of the combinatorial circuit using logic gates:

$$out1 = ((in1 \text{ or } in2) \text{ and } (in3 \text{ or } in4)) \quad \textbf{(Eq1)}$$

And here is the truth table for the specific circuit **(Table 1.1)**:

in1	in2	in3	in4	out1
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	0
0	0	1	0	0
1	0	1	0	1
0	1	1	0	1
1	1	1	0	1
0	0	0	1	0
1	0	0	1	1
0	1	0	1	1
1	1	0	1	1
0	0	1	1	0
1	0	1	1	1
0	1	1	1	1
1	1	1	1	1

Table 1.1: Truth Table for Eq1

Since there was not enough and-gate ICs (74HC08N) in the lab, nand-gates (74HC00N) and not-gates (74HC04N) were used to create an and-gate. Here is the RTL schematic of the circuit that was used in the experiment **(Figure 1.16)**:

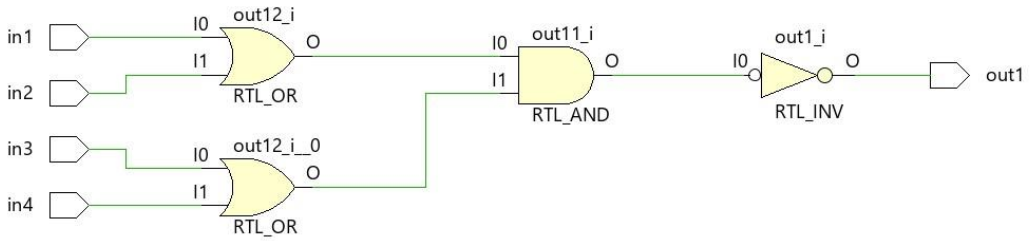

Figure 1.16: RTL Schematic of the combinatorial circuit

Results:

After building the designed combinatorial circuit, the power supply was turned on and the circuit was examined both via an oscilloscope and LEDs. Here is the output wave signal of the circuit **(Figure 1.17)**:

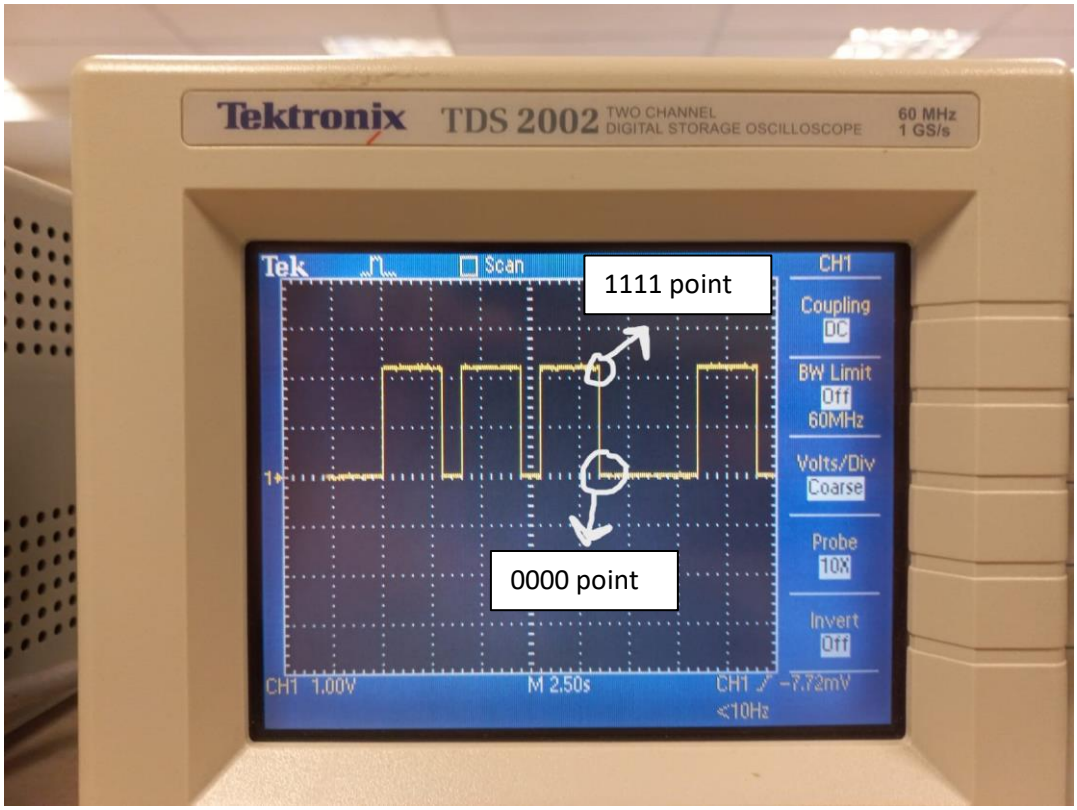

Figure 1.17: The Output Signal of the Combinatorial Circuit on an Oscilloscope

Here are every single possible input and output combinations of the circuit with LEDs:

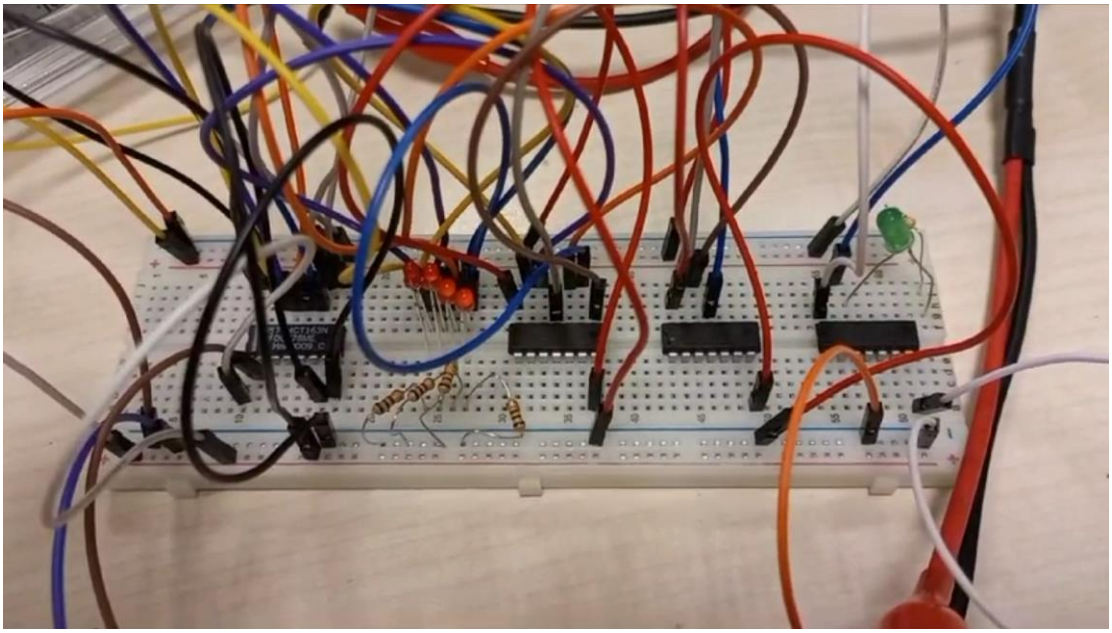

Figure 2.1: out1 = 0 when in1 = 0, in2 = 0, in3 = 0, in4 = 0

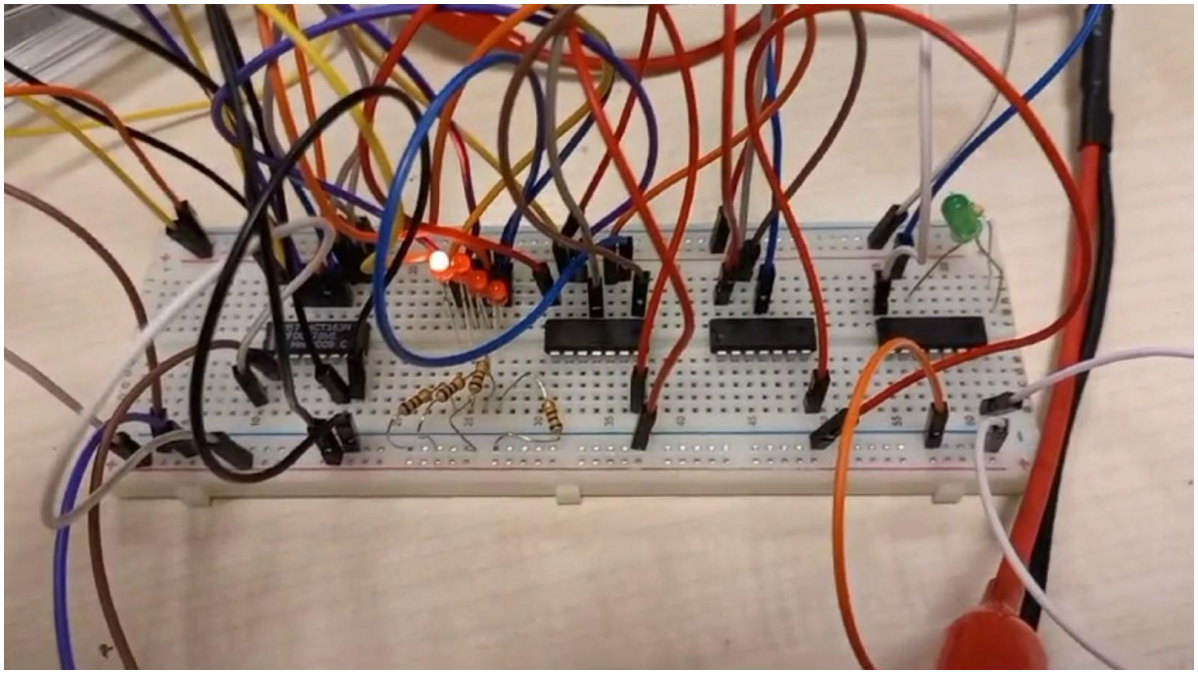

Figure 2.2: out1 = 0 when in1 = 1, in2 = 0, in3 = 0, in4 = 0

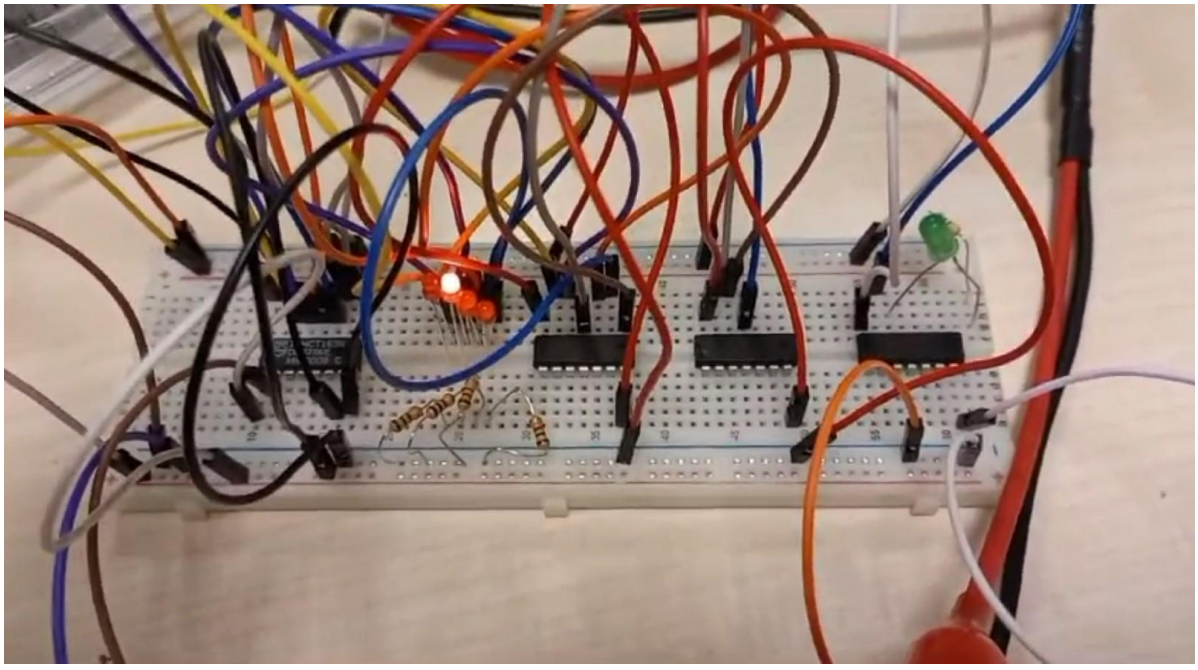

Figure 2.3: out1 = 0 when in1 = 0, in2 = 1, in3 = 0, in4 = 0

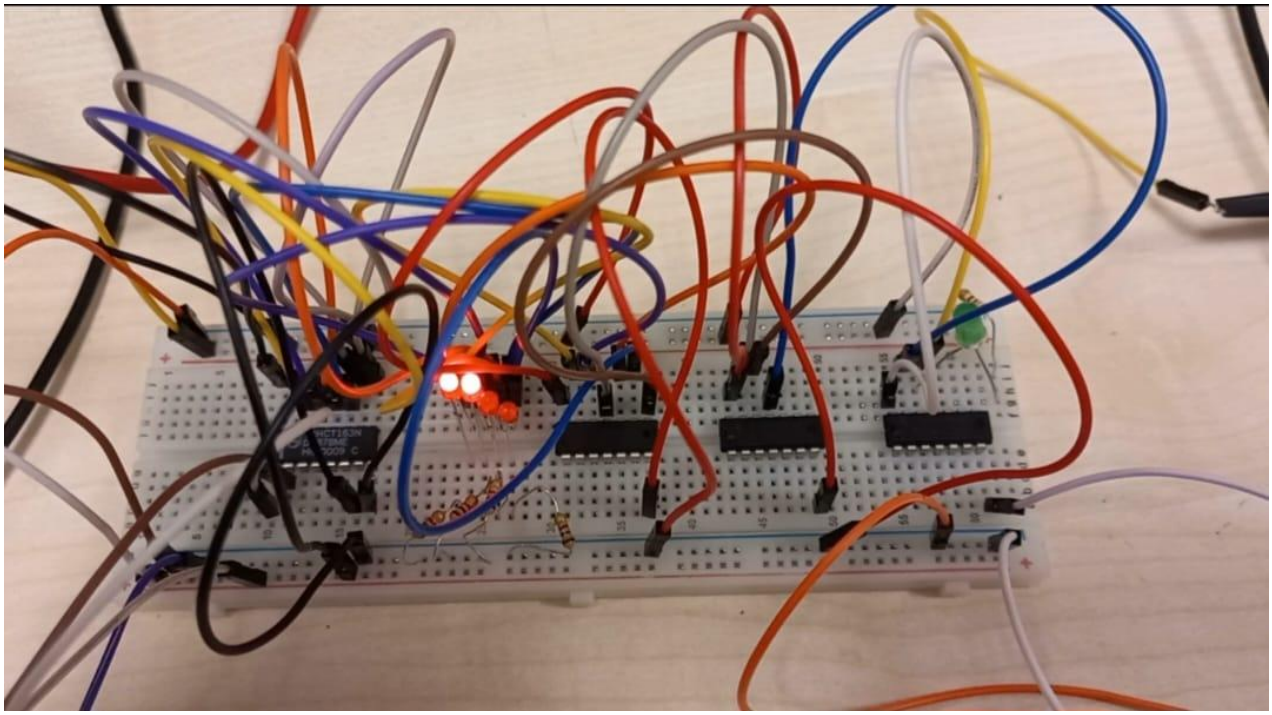

Figure 2.4: out1 = 0 when in1 = 1, in2 = 1, in3 = 0, in4 = 0

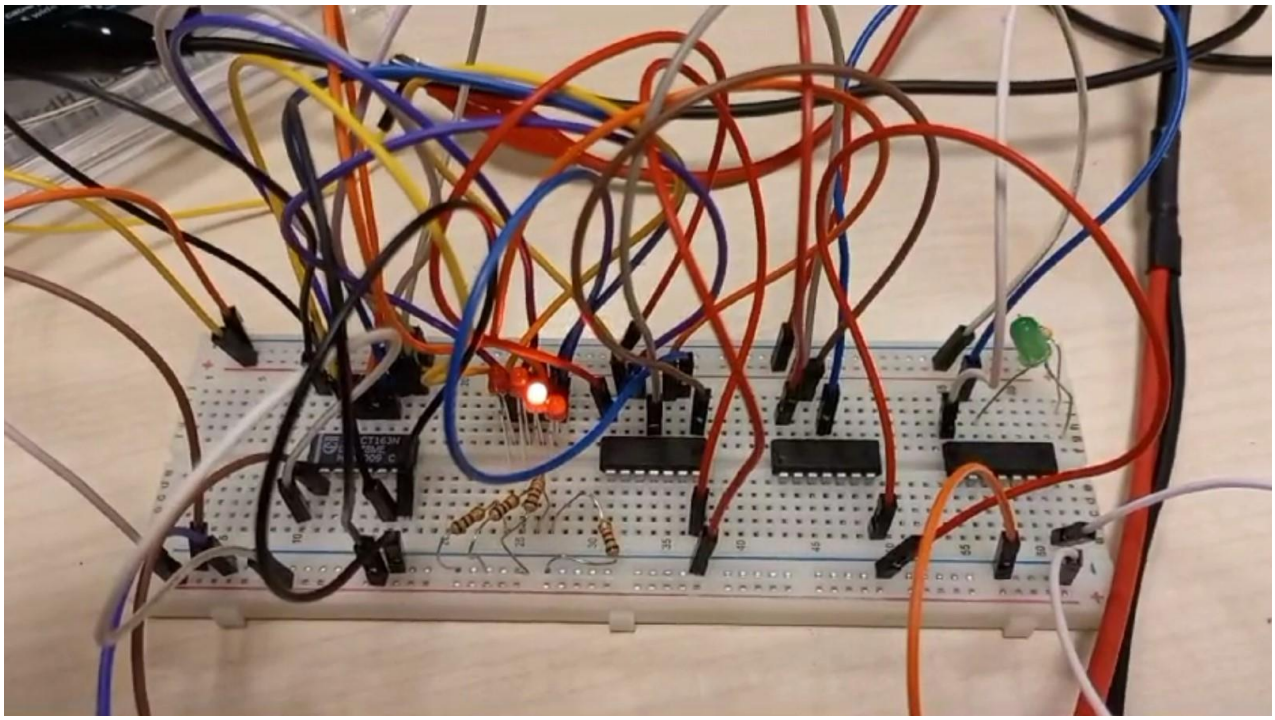

Figure 2.5: out1 = 0 when in1 = 0, in2 = 0, in3 = 1, in4 = 0

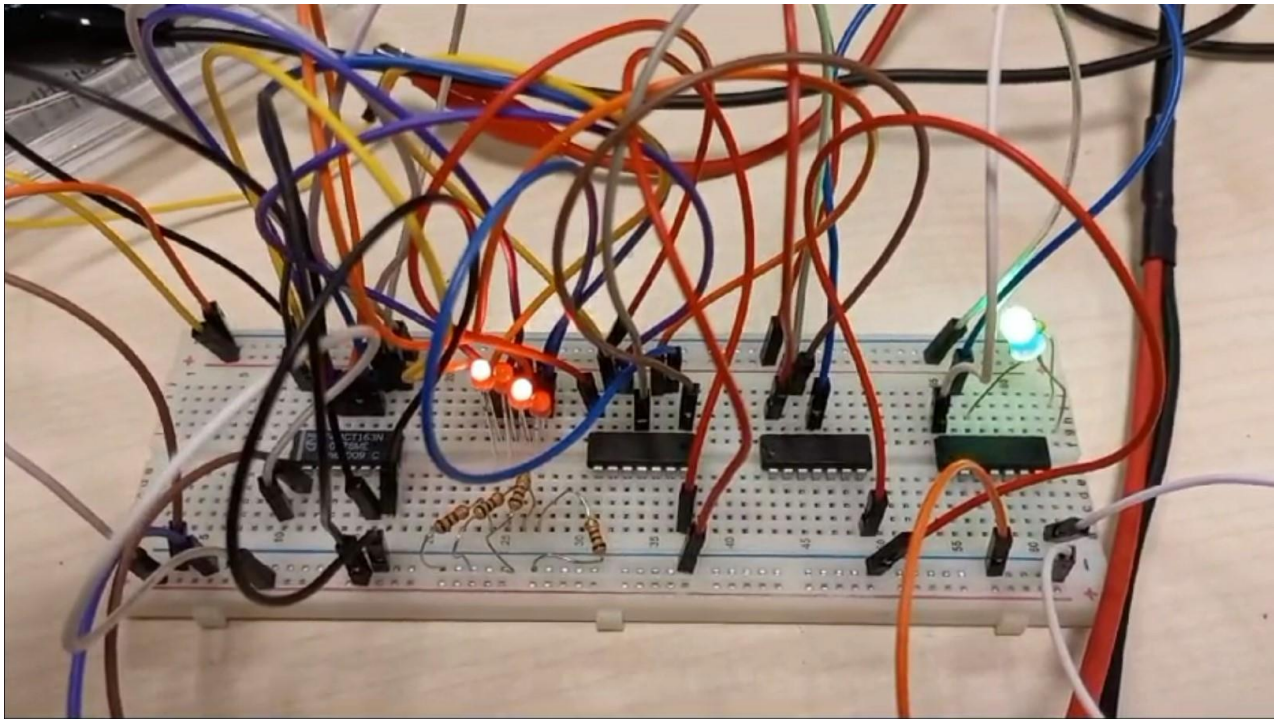

Figure 2.6: out1 = 1 when in1 = 1, in2 = 0, in3 = 1, in4 = 0

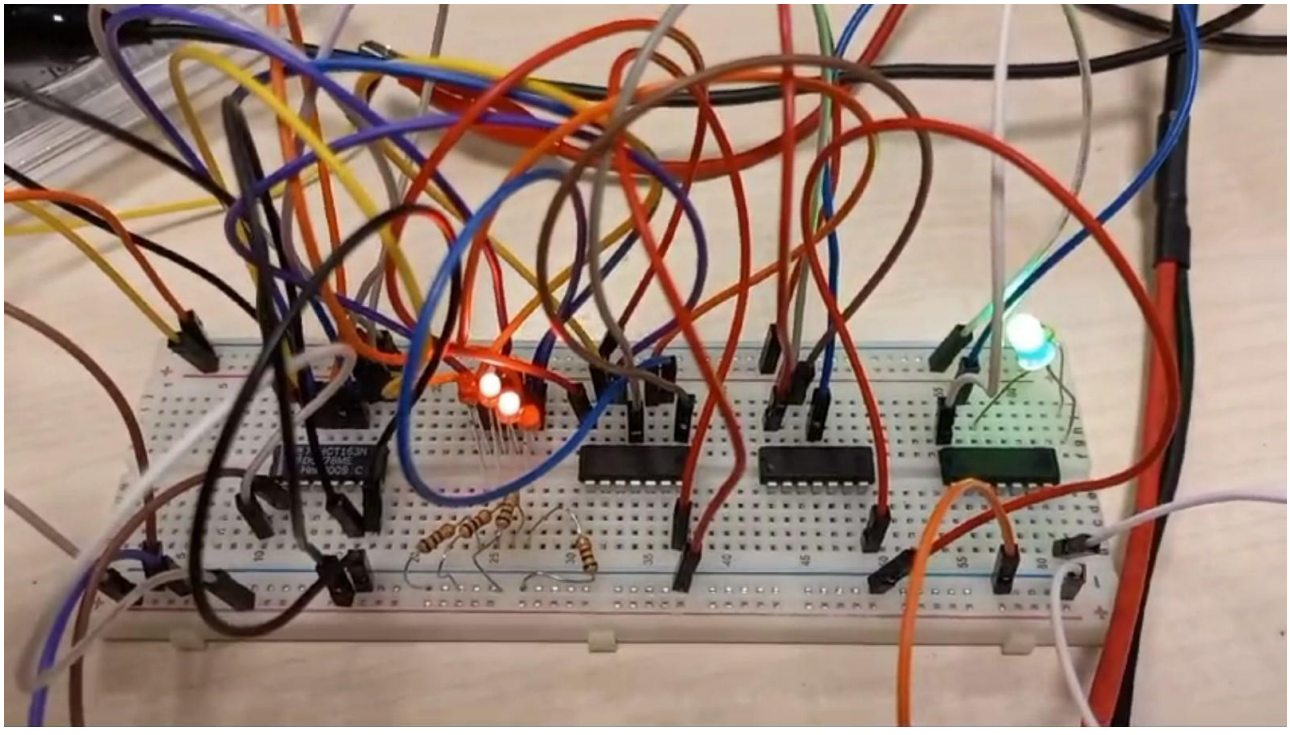

Figure 2.7: out1 = 1 when in1 = 0, in2 = 1, in3 = 1, in4 = 0

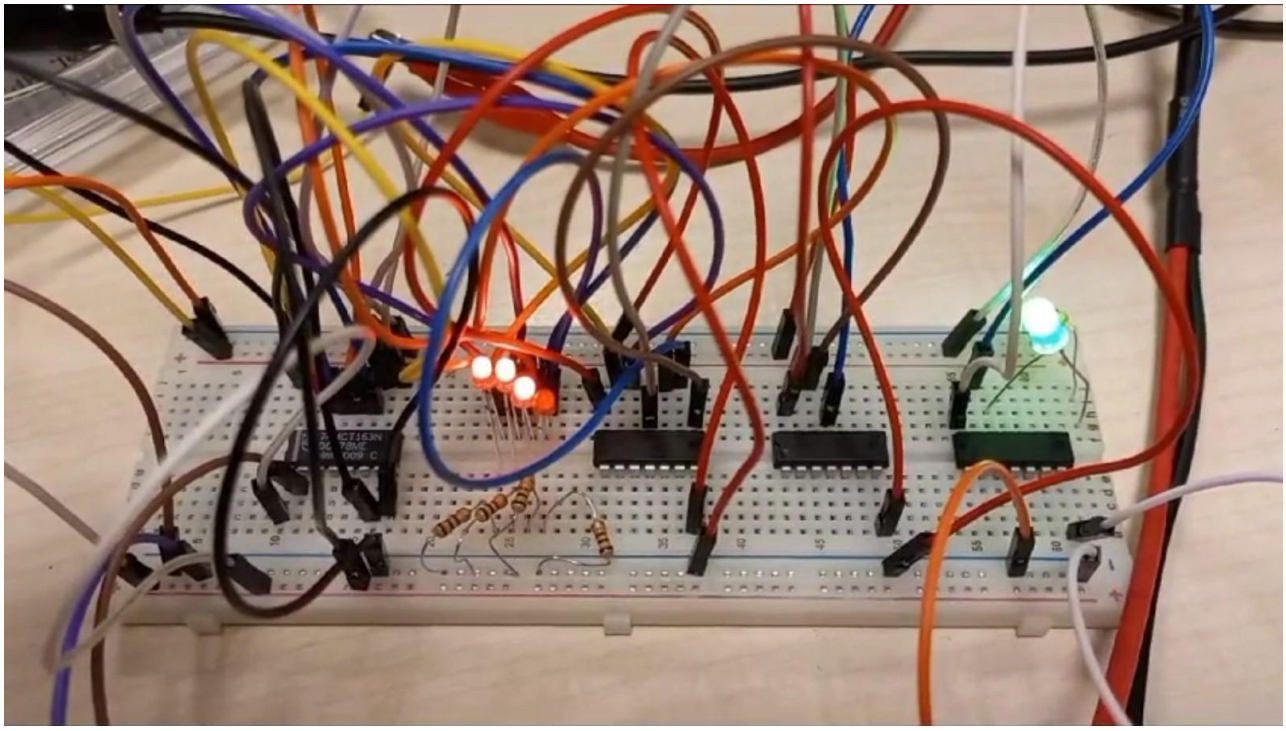

Figure 2.8: out1 = 1 when in1 = 1, in2 = 1, in3 = 1, in4 = 0

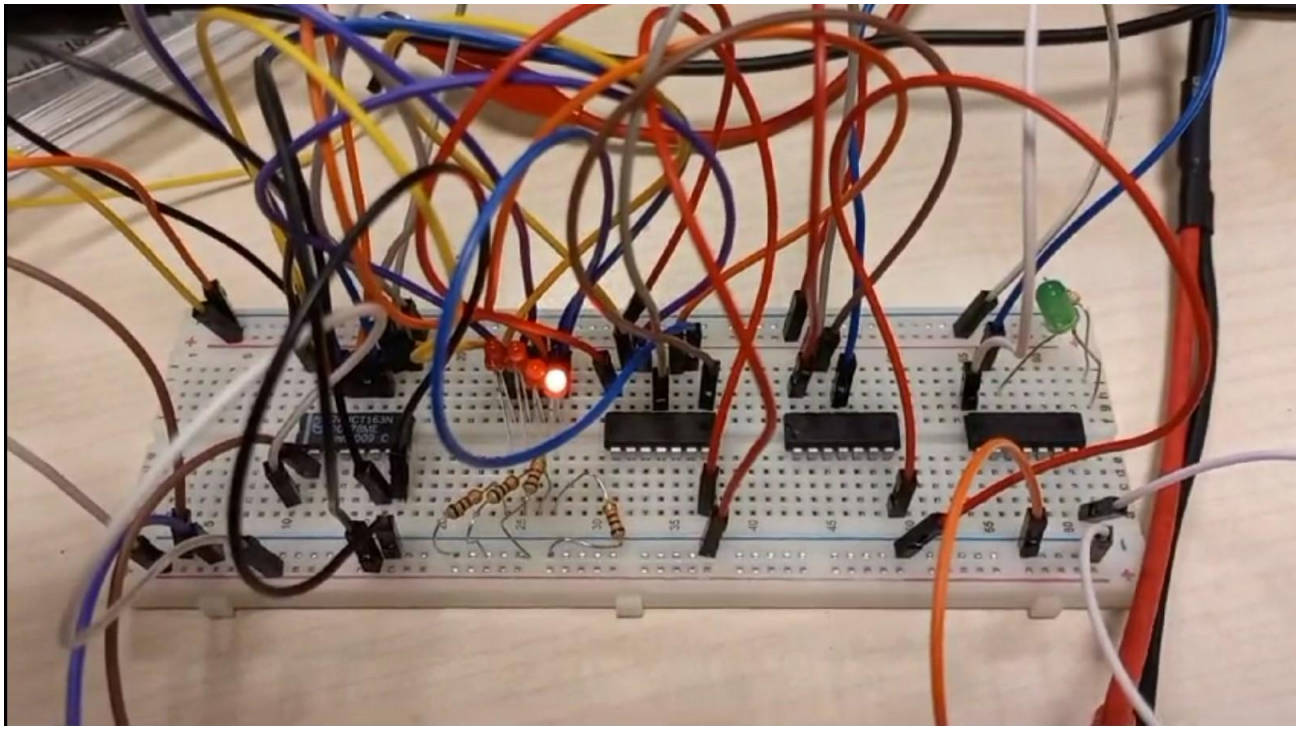

Figure 2.9: out1 = 0 when in1 = 0, in2 = 0, in3 = 0, in4 = 1

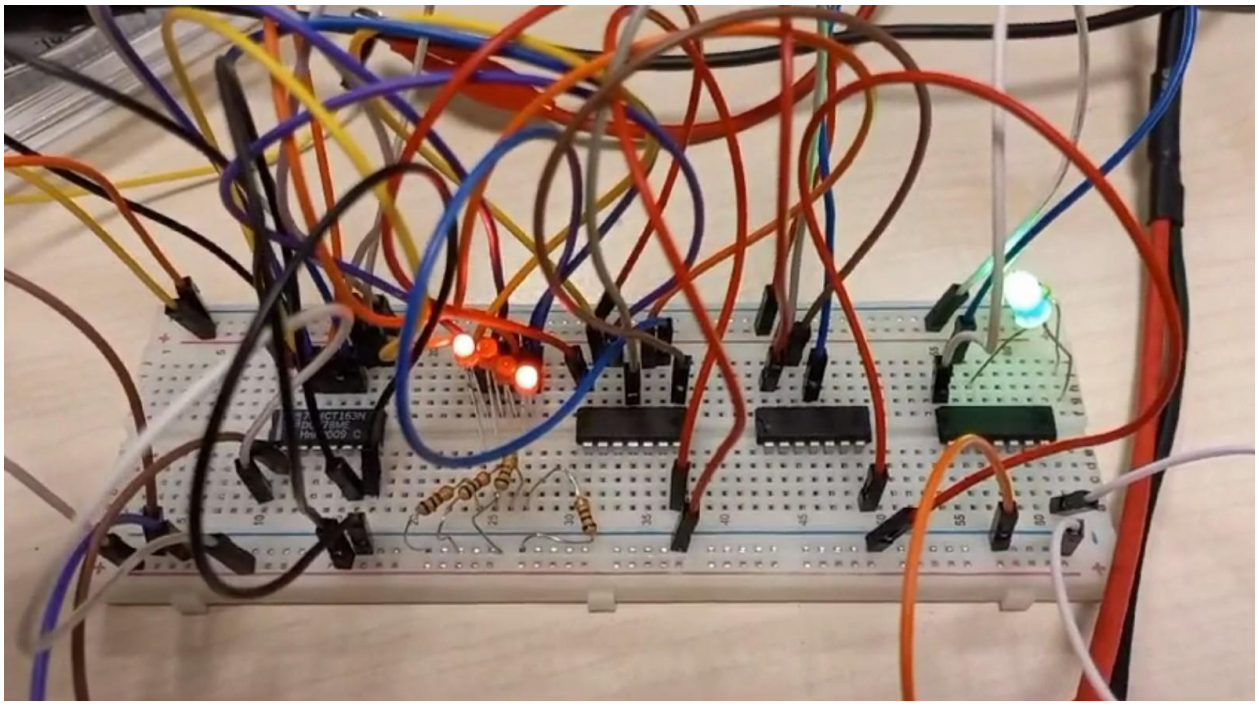

Figure 2.10: out1 = 1 when in1 = 1, in2 = 0, in3 = 0, in4 = 1

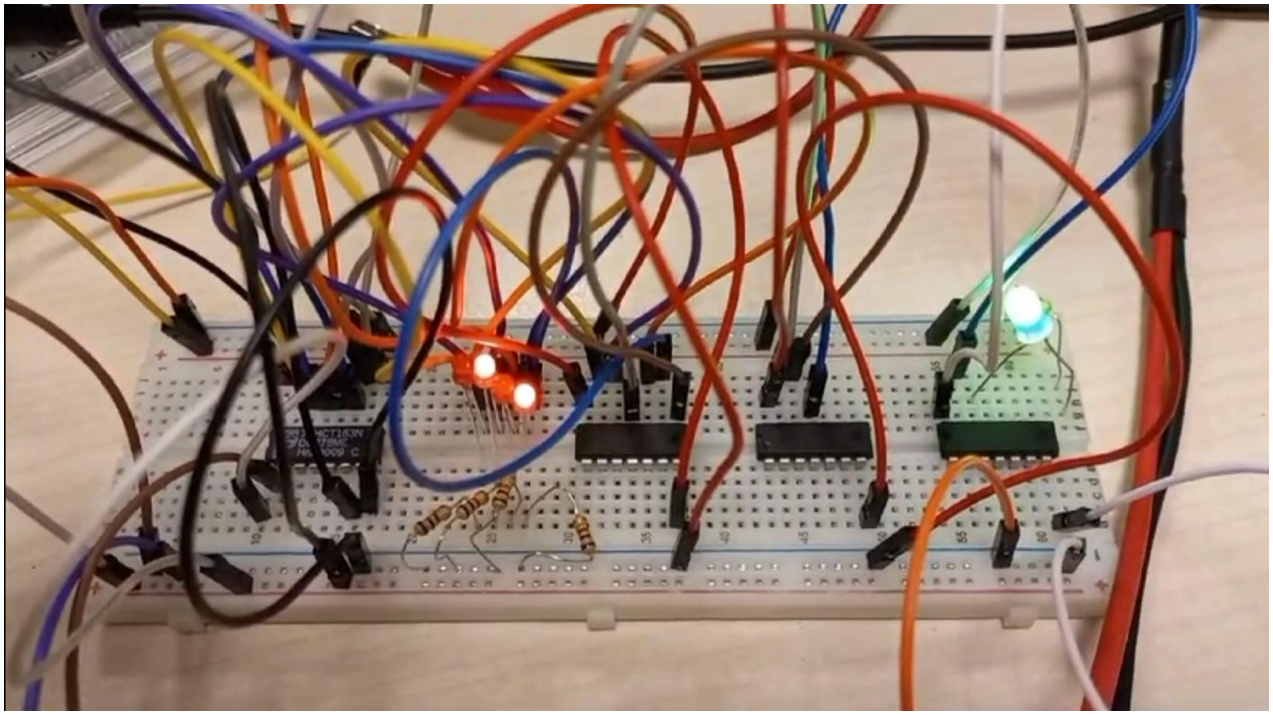

Figure 2.11: out1 = 1 when in1 = 0, in2 = 1, in3 = 0, in4 = 1

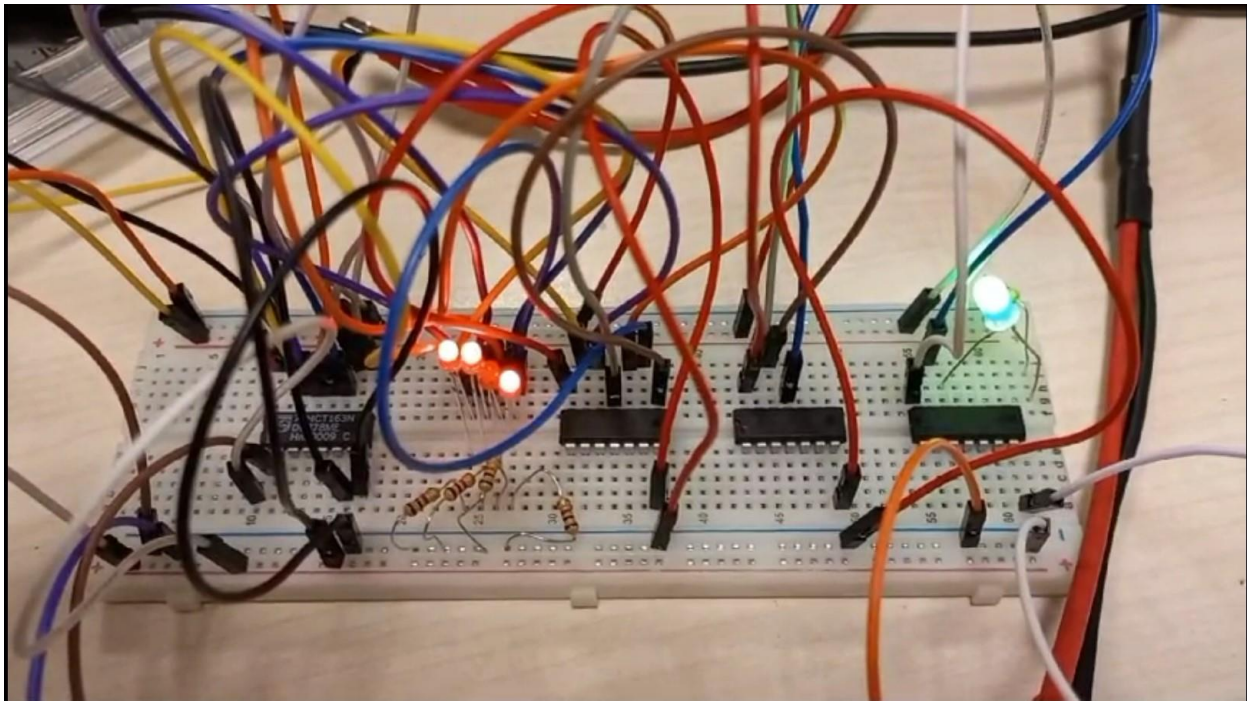

Figure 2.12: out1 = 1 when in1 = 1, in2 = 1, in3 = 0, in4 = 1

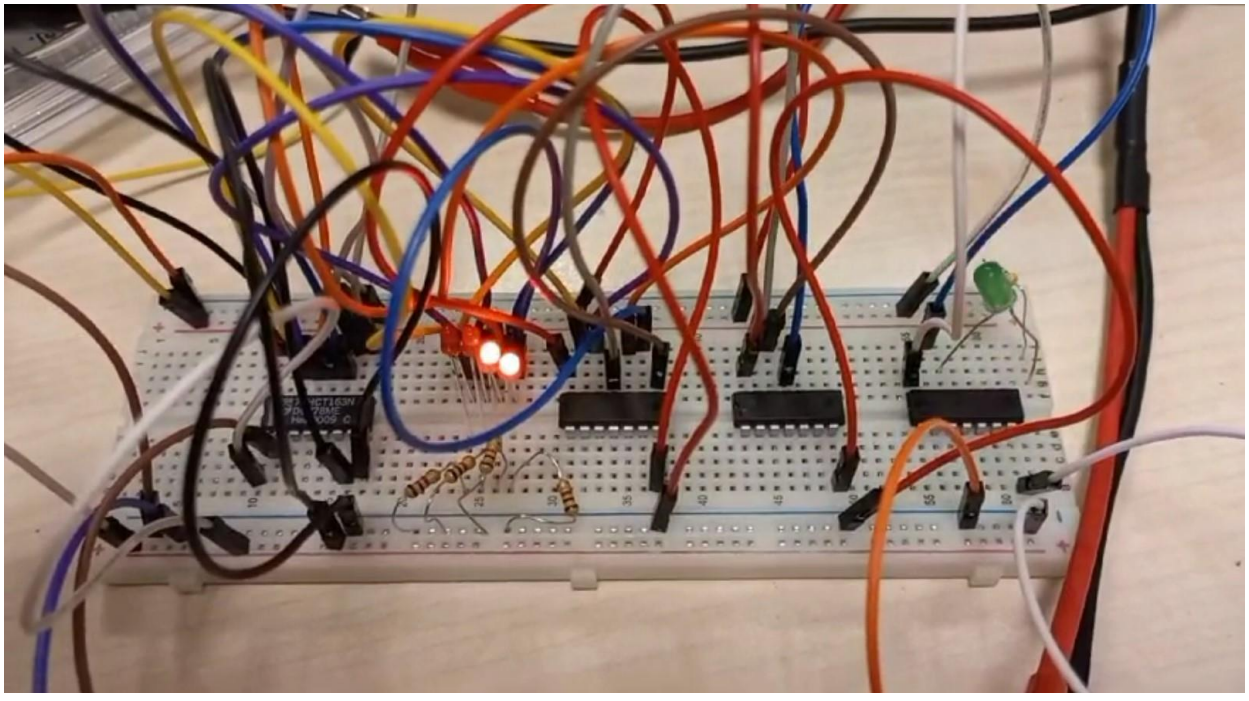

Figure 2.13: out1 = 0 when in1 = 0, in2 = 0, in3 = 1, in4 = 1

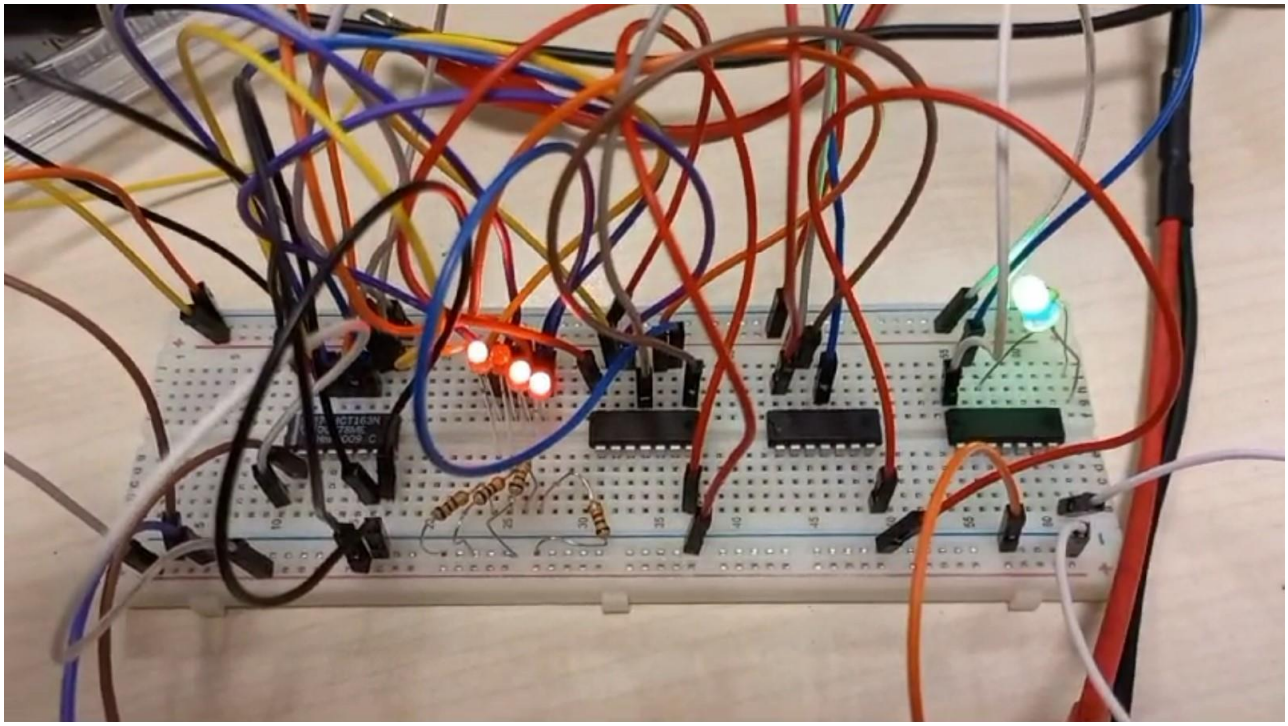

Figure 2.14: out1 = 1 when in1 = 1, in2 = 0, in3 = 1, in4 = 1

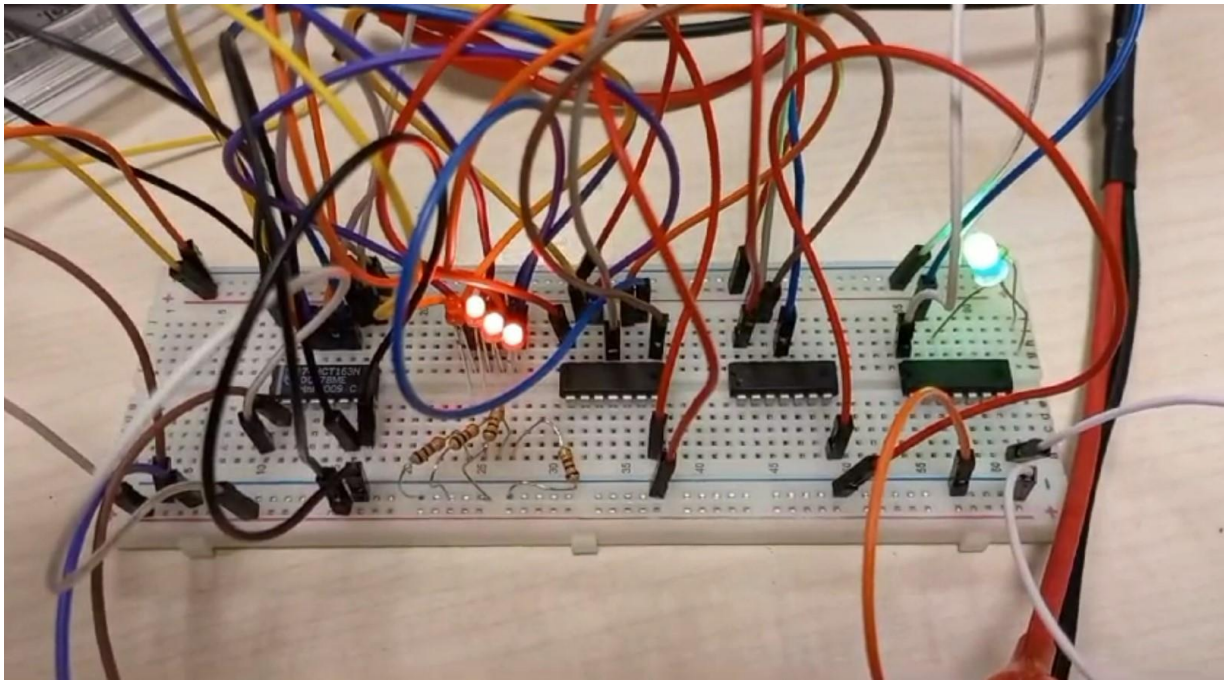

Figure 2.15: out1 = 1 when in1 = 0, in2 = 1, in3 = 1, in4 = 1

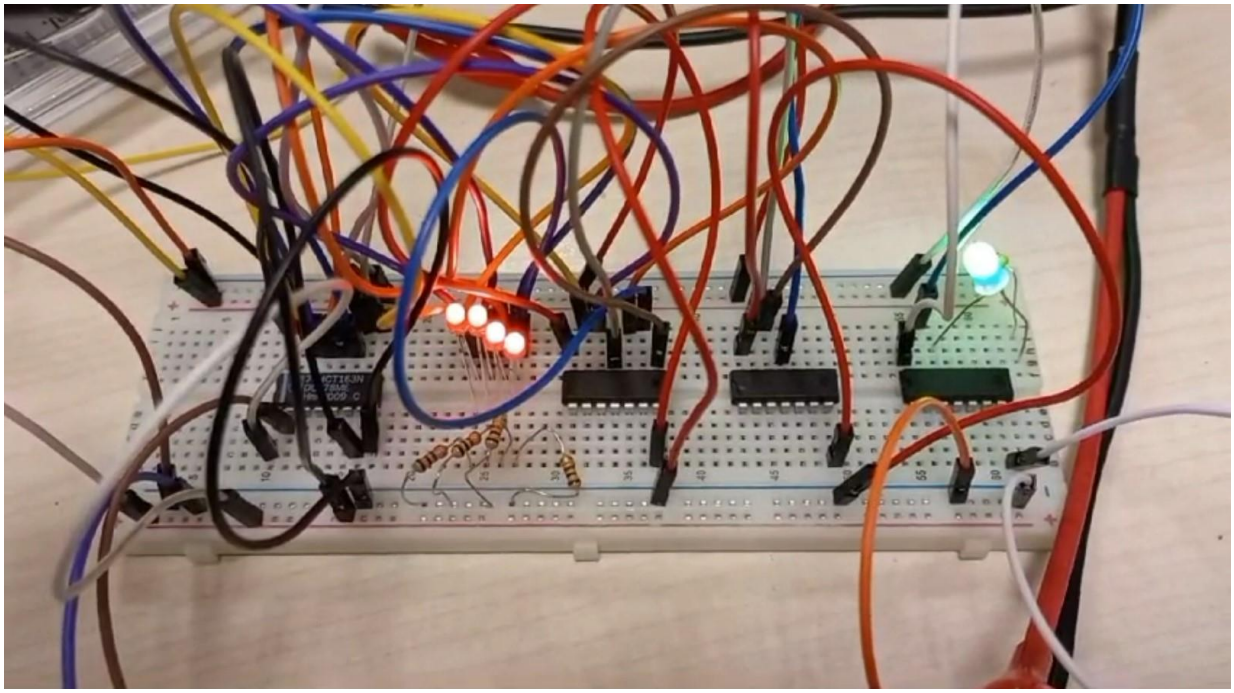

Figure 2.16: out1 = 1 when in1 = 1, in2 = 1, in3 = 1, in4 = 1

The findings from the oscilloscope, LED-backed visual examination and the truth table were all matching. This proved that the circuit was consistent and successful.

Conclusion:

In the lab, building a combinatorial circuit on a breadboard by using IC components were effectively studied. The datasheets of every single IC that was used were examined one by one in order to use the components. Also, the biggest problem that was encountered in this experiment was the damaged IC components in the lab. In this specific experiment the 74HC32N (quad 2-input or gate) that was used initially was replaced with another 74HC32N. The component might be burned from previous experiments or may be exposed to high or low temperatures. Also, the 4-bit binary counter was replaced many times since there was not enough working counter in the lab for everyone. The counter problem took hours to solve. It is recommended that more logistics and infrastructure investments should be made to the labs in order to conduct the experiments faster and safer.