Bilkent University

Electrical and Electronics Department

EE202-03 Lab 5 Report:

“The Design of a Band-Pass Filter”

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1- Software Implementation

1.1- Introduction:

The main purpose of this lab was to create a band-pass filter for a 50Ω load resistance with specific requirements. The central frequency (f_0) was meant to be between 2MHz and 5MHz. The pass-band width (f_{c1} - f_{c0}) should be 0.05 times the central frequency (f_0). The gain variation in the pass-band should be less than 3dB and the gain variation in the stop-band should be greater than 30dB. Here you can see the requirements taken from the original lab manual **(Figure 1.1.1)**.

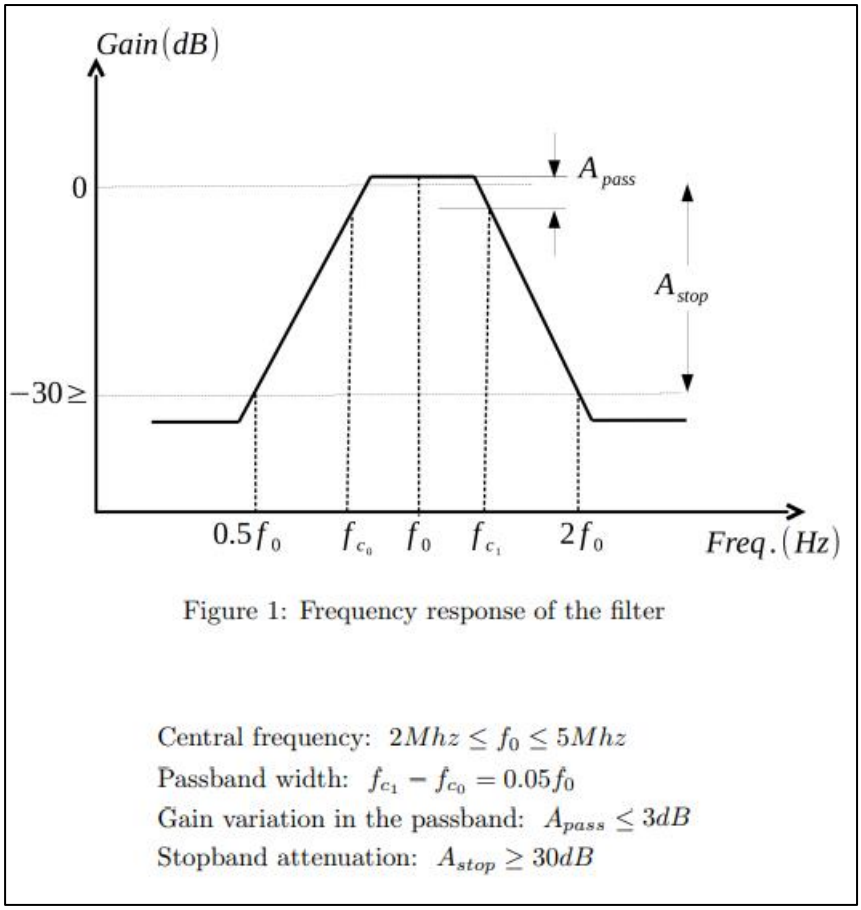

Figure 1: Frequency response of the filter

Central frequency: $2Mhz \leq f_0 \leq 5Mhz$
Passband width: $f_{c_1} - f_{c_0} = 0.05f_0$
Gain variation in the passband: $A_{pass} \leq 3dB$
Stopband attenuation: $A_{stop} \geq 30dB$

Figure 1.1.1: The Requirements for the Band-Pass Filter

The central frequency was chosen as 2MHz. A Butterworth type polynomial filter was decided to be used for this lab assignment. The filter would first be designed theoretically and tested in LTSpice. Then the design would be tested with hardware components.

1.2- Analysis:

The component values will be calculated using the Butterworth filter table **(Table 1)**.

Order	Resistor	C1	L2	C3	L4	C5	L6	C7
1	1.0	2.000	-	-	-	-	-	-
2	1.0	1.4142	1.4142	-	-	-	-	-
3	1.0	1.0000	2.0000	1.0000	-	-	-	-
4	1.0	0.7654	1.8478	1.8478	0.7654	-	-	-
5	1.0	0.6180	1.6180	2.0000	1.6180	0.6180	-	-
6	1.0	0.5176	1.4142	1.9319	1.9319	1.4142	0.5176	-
7	1.0	0.4450	1.2470	1.8019	2.0000	1.8019	1.2470	0.4450

Table 1: The Butterworth Filter Component Value Table up to 7th Order

The next task is to decide the order of the Butterworth filter. Here are the equations **(Equations 1.1 to 1.4)** that will help us determine the order of the Butterworth filter, where n is the order of the filter.

$$\frac{V_L}{V_S} = \sqrt{\frac{1}{1+\left[\frac{f_0}{\Delta f}\left(\frac{f}{f_0}-\frac{f_0}{f}\right)\right]^{2n}}} \qquad \textbf{(Equation 1.1)}$$

With f_0 being 2MHz and pass-band width being 1/20 times f_0:

$$\frac{V_L}{V_S} = \sqrt{\frac{1}{1+\left[20\cdot\left(\frac{f}{2\cdot10^6}-\frac{2\cdot10^6}{f}\right)\right]^{2n}}} \quad \textbf{(Equation 1.2)}$$

For the 1st order case where f is either 4MHz or 1MHz:

$$H(f) = 10\log\left(\sqrt{\frac{1}{1+\left[20\cdot\left(\frac{f}{2\cdot10^6}-\frac{2\cdot10^6}{f}\right)\right]^{2}}}\right) = -29dB \qquad \textbf{(Equation 1.3)}$$

For the 2nd order case where f is either 4MHz or 1MHz:

$$H(f) = 10\log\left(\sqrt{\frac{1}{1+\left[20\cdot\left(\frac{f}{2\cdot10^6}-\frac{2\cdot10^6}{f}\right)\right]^{4}}}\right) = -59dB \qquad \textbf{(Equation 1.4)}$$

The required stop-band attenuation was supposed to be greater than 30dB. 1st order filter does not meet this requirement, but the 2nd order filter does **(Equations 1.3&1.4)**.

For the 2nd order case where f is 1.95MHz:

$$H(f) = 10\log\left(\sqrt{\frac{1}{1+\left[20\cdot\left(\frac{f}{2\cdot10^6}-\frac{2\cdot10^6}{f}\right)\right]^{4}}}\right) = -3.12dB \quad \textbf{(Equation 1.5)}$$

For the 2nd order case where f is 2.05MHz:

$$H(f) = 10\log\left(\sqrt{\frac{1}{1+\left[20\cdot\left(\frac{f}{2\cdot10^6}-\frac{2\cdot10^6}{f}\right)\right]^4}}\right) = -2.90dB \quad \textbf{(Equation 1.6)}$$

Since the pass-band width (f_{c1} - f_{c0}) should be 0.05 times the central frequency (f_0), 2.05MHz and 1.95MHz are the initially projected cut-off frequencies. In equations 1.5 and 1.6 we can see that the gain in these frequencies are close to 3dB each theoretically. This is another justification for using the 2nd order polynomial Butterworth filter.

Now in order to create a 2nd order polynomial Butterworth band-pass filter, we should divide the order of business into two. Firstly, we should create a 2nd order polynomial Butterworth low-pass filter. Secondly, we should tune the respective capacitive and inductive elements for 2MHz central frequency.

Following equations help us determine the values for C_1 and L_2 **(Equations 2.1&2.2)**.

$$C_1 = \frac{1,4142}{2\cdot\pi\cdot R\cdot\Delta f} = \frac{1,4142}{2\cdot\pi\cdot50\cdot2\cdot10^6\cdot 0,05} = 45.02nF \quad \textbf{(Equation 2.1)}$$

$$L_2 = \frac{1,4142\cdot R}{2\cdot\pi\cdot\Delta f} = \frac{1,4142\cdot50}{2\cdot\pi\cdot2\cdot10^6\cdot 0,05} = 112.54\mu H \quad \textbf{(Equation 2.2)}$$

The following figure demonstrates the low-pass filter that is designed in the first part of creating the band-pass filter **(Figure 1.2.1)**:

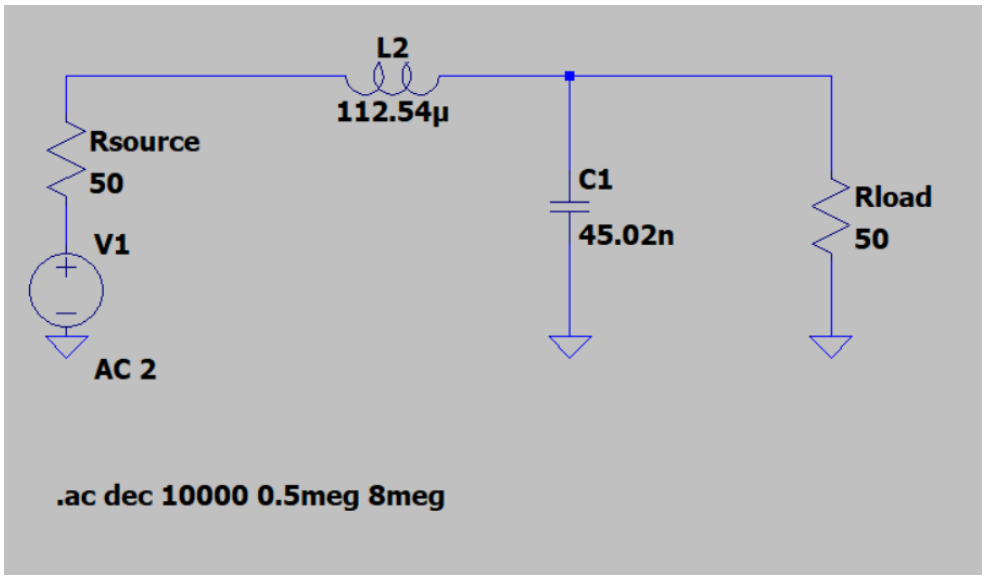

Figure 1.2.1: The Initial Low-Pass Filter Design

Now we should, tune out the capacitive and inductive elements at 2MHz central frequency. Following equations help us determine the values for C_3 and L_4 **(Equations 2.3&2.4)**.

$$C_3 = \frac{1}{\omega^2 \cdot L_2} = \frac{1}{(2 \cdot \pi \cdot 2 \cdot 10^6)^2 \cdot 112{,}54 \cdot 10^{-6}} = 56.3pF \quad \textbf{(Equation 2.3)}$$

$$L_4 = \frac{1}{\omega^2 \cdot C_1} = \frac{1}{(2 \cdot \pi \cdot 2 \cdot 10^6)^2 \cdot 45{,}02 \cdot 10^{-9}} = 140.7nH \quad \textbf{(Equation 2.4)}$$

The final LTSpice schematic of the circuit looks like this **(Figure 1.2.2)**:

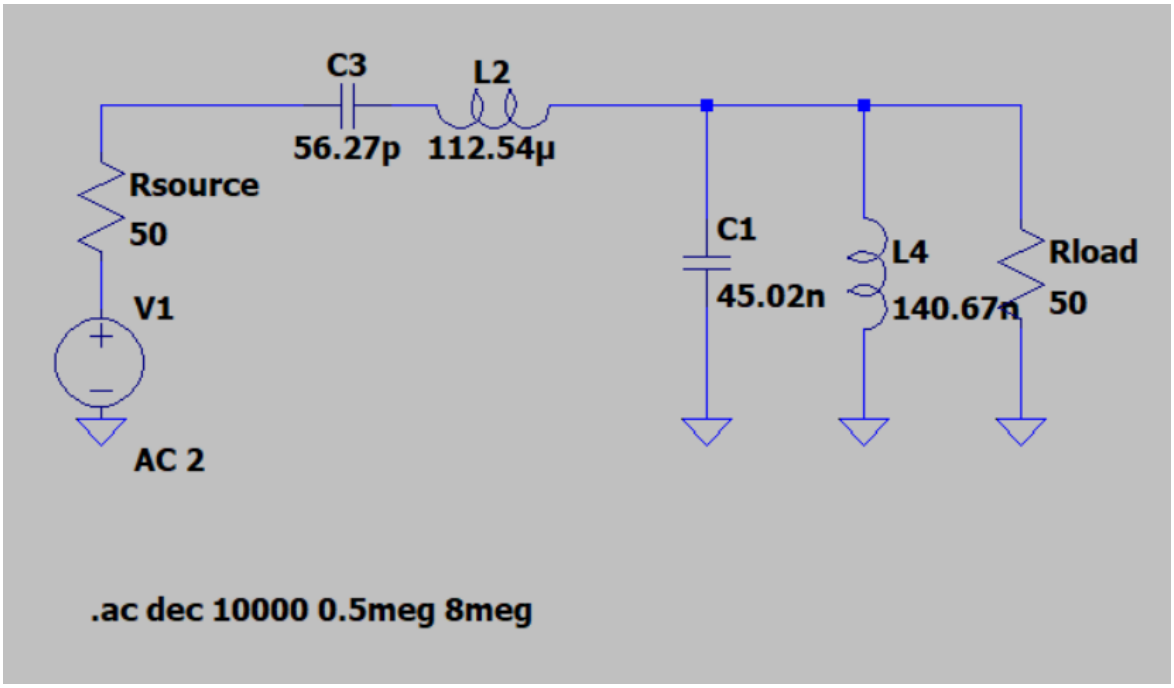

Figure 1.2.1: The Finalised Band-Pass Filter Design

1.3- Simulations:

Here are some necessary plots **(Figures 1.3.1 to 1.3.4)**:

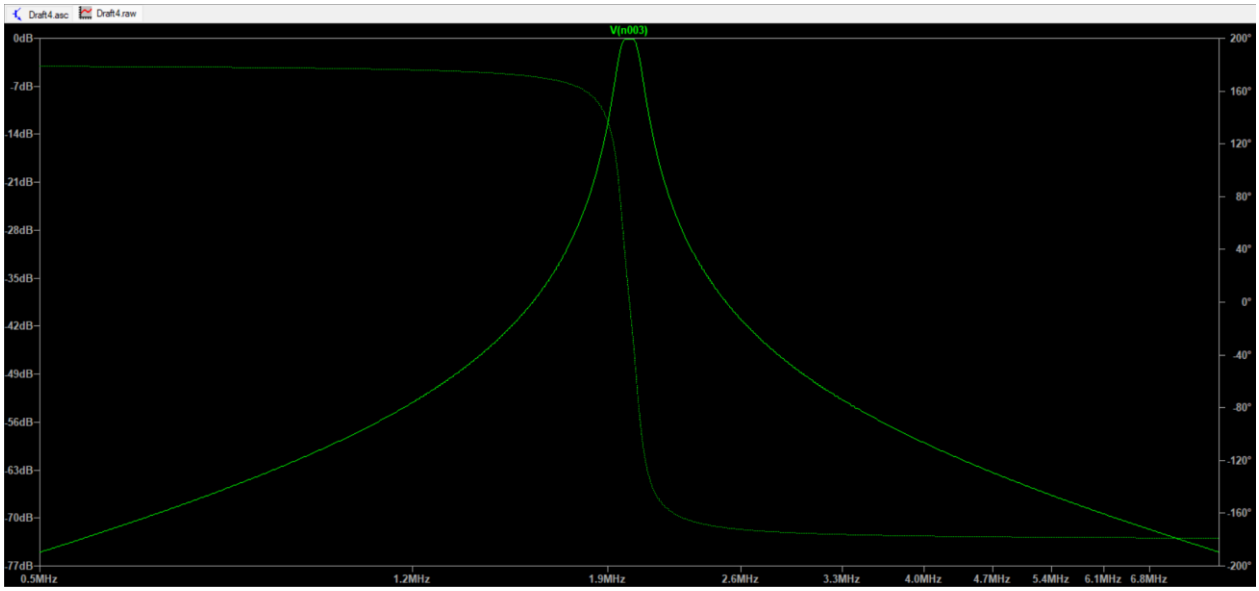

Figure 1.3.1: The Gain-Frequency Plot on the Load Resistor

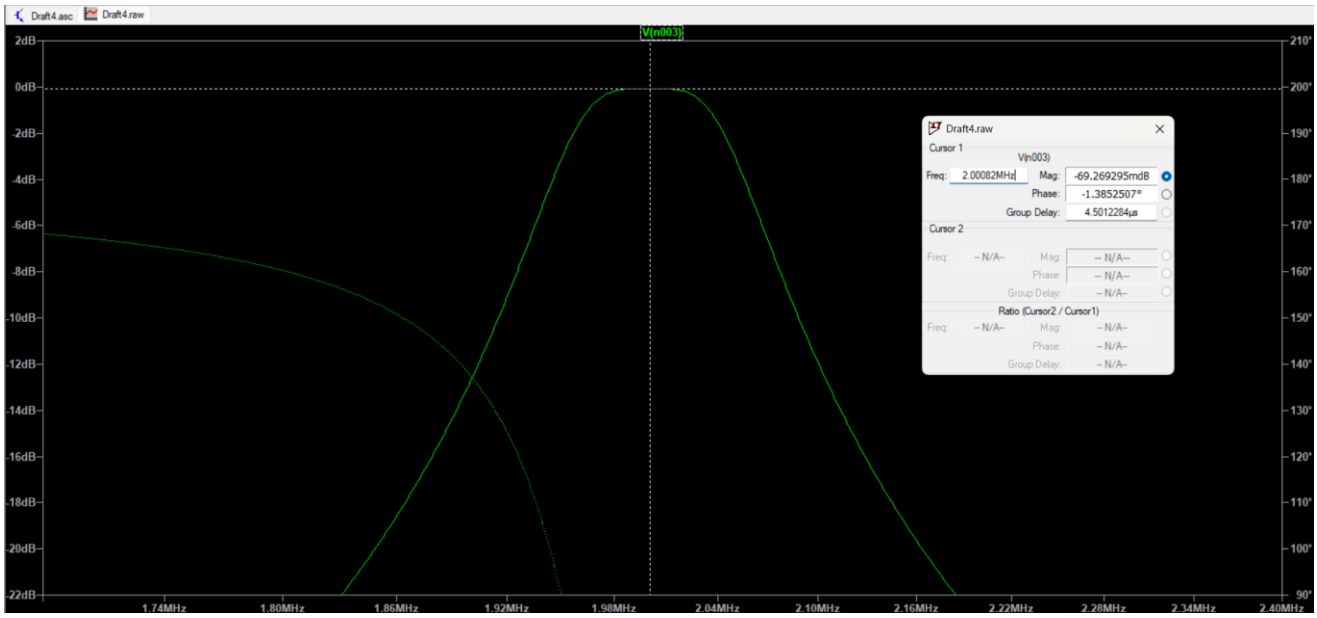

Figure 1.3.2: The Central Frequency of the Filter which is 2.00082MHz.

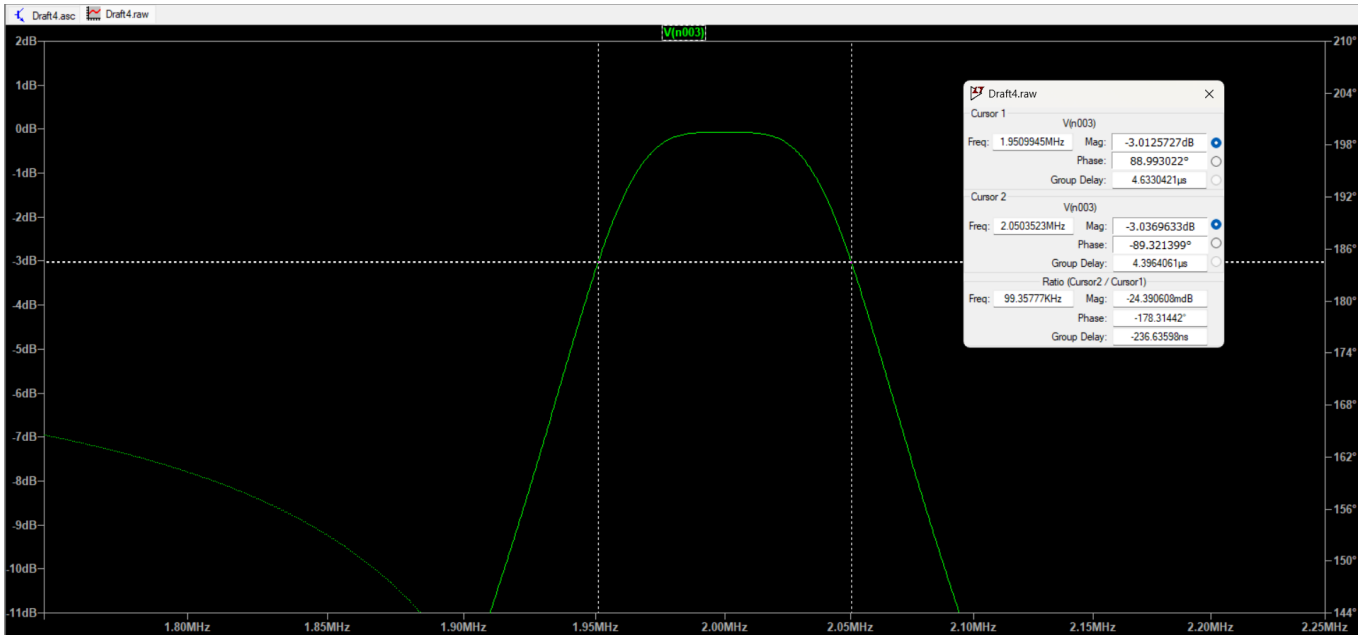

Figure 1.3.3: The 3dB cut-off frequencies; Δf = 99.357kHz

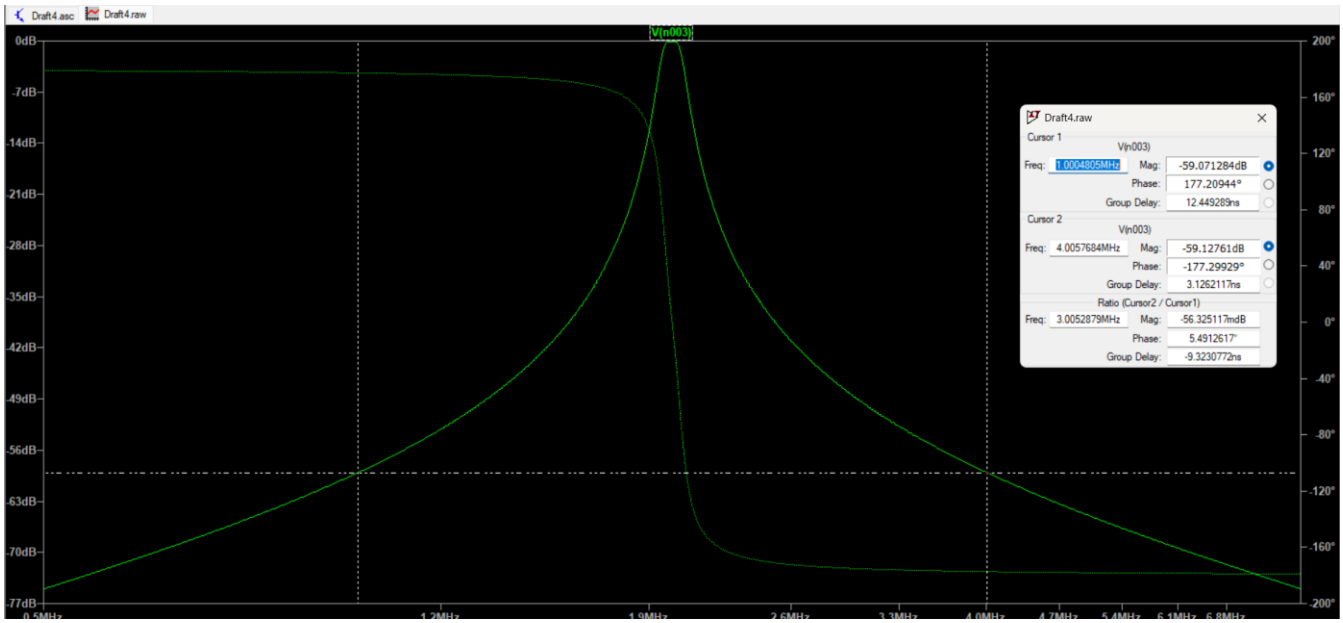

Figure 1.3.4: The stop-band frequencies; gain = -59dB

Here is the table that shows our simulation data error **(Table 2)**:

	Desired	Obtained	Error
Central Frequency	2MHz	2.00082MHz	%0.041
Pass-Band Width	100kHz	99.357kHz	%0.643

2- Hardware Implementation

2.1- Introduction:

I used ceramic capacitors, axial inductors and a winded toroid to complete the design. Here you can see the circuit implemented on the hardware **(Figure 2.1.1)**:

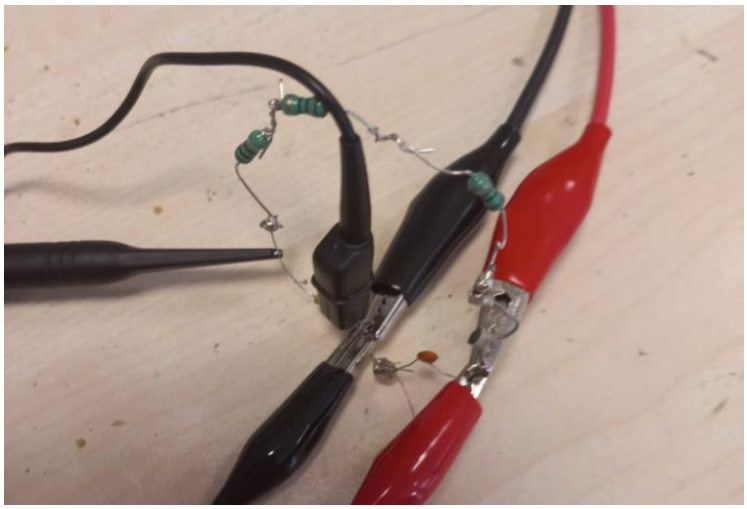

Figure 2.1.1: The Circuit Implemented on the Hardware

2.2- Results

Here are some important results with varying frequencies **(Figures 2.2.1 to 2.2.15)** :

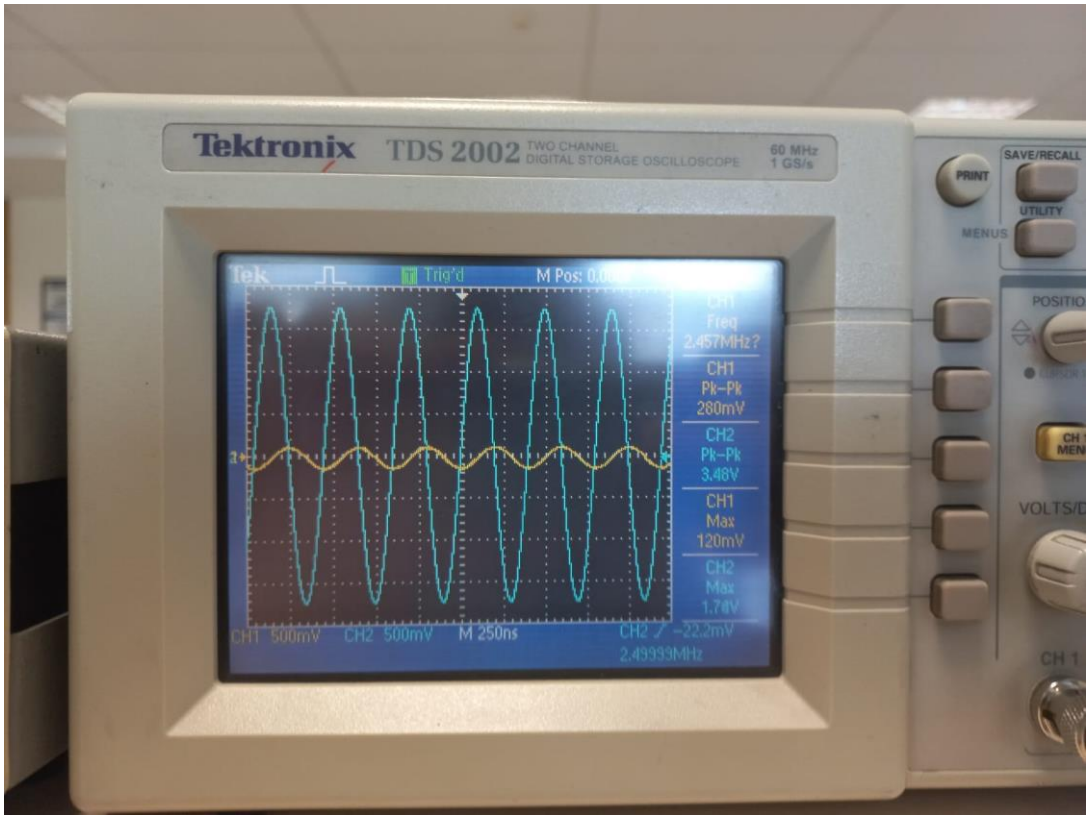

Figure 2.2.1: Output Voltage = 280mV; Gain = -17.07 when Input is 2.50MHz

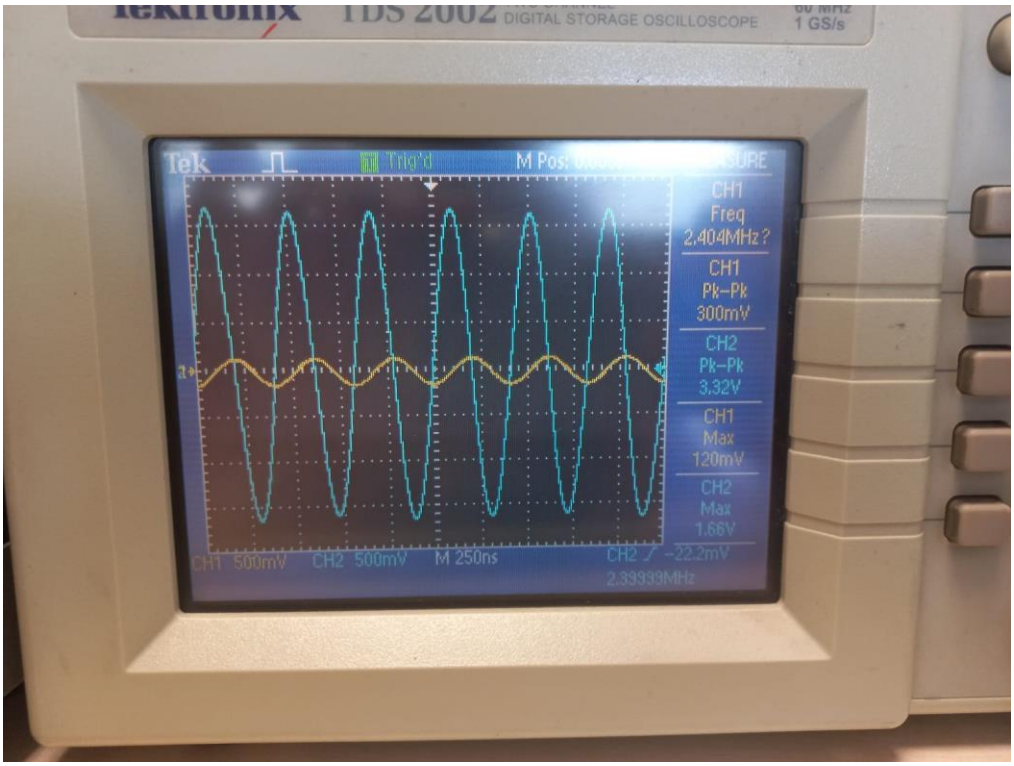

Figure 2.2.2: Output Voltage = 3000mV; Gain = -16.47 when Input is 2.40MHz

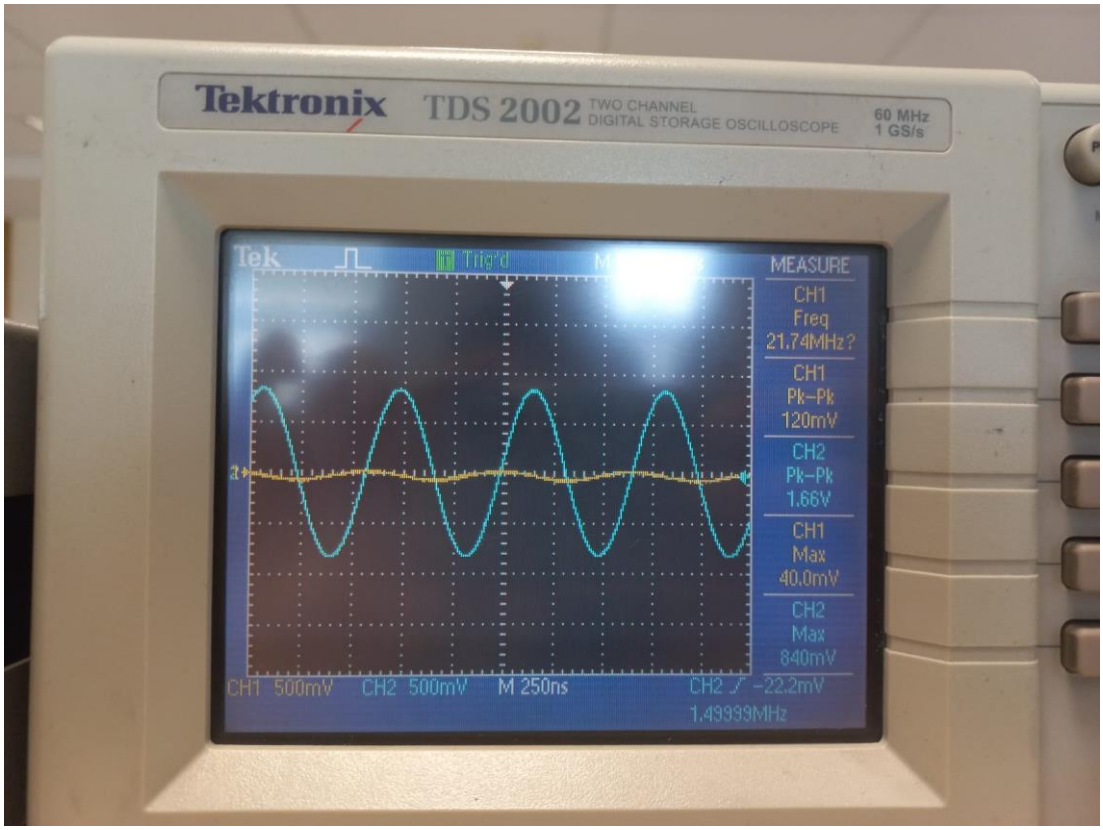

Figure 2.2.3: Output Voltage = 120mV; Gain = -24,43 when Input is 1.50MHz

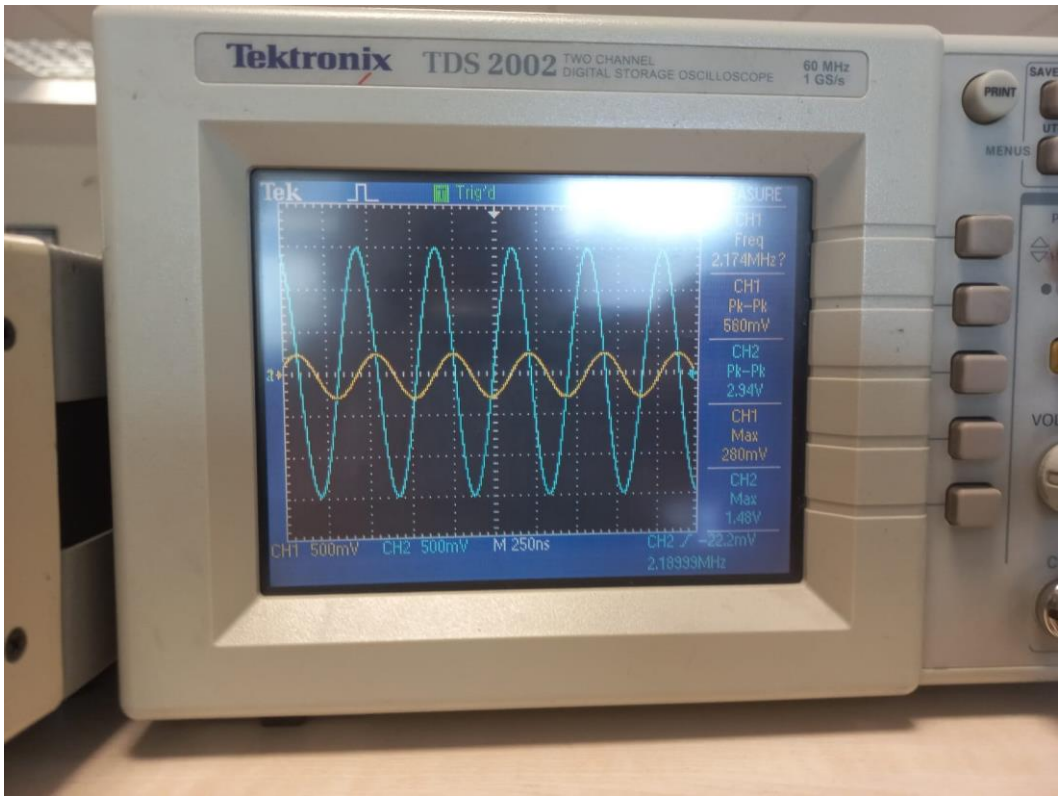

Figure 2.2.4: Output Voltage = 560mV; Gain = -11.05 when Input is 2.20MHz

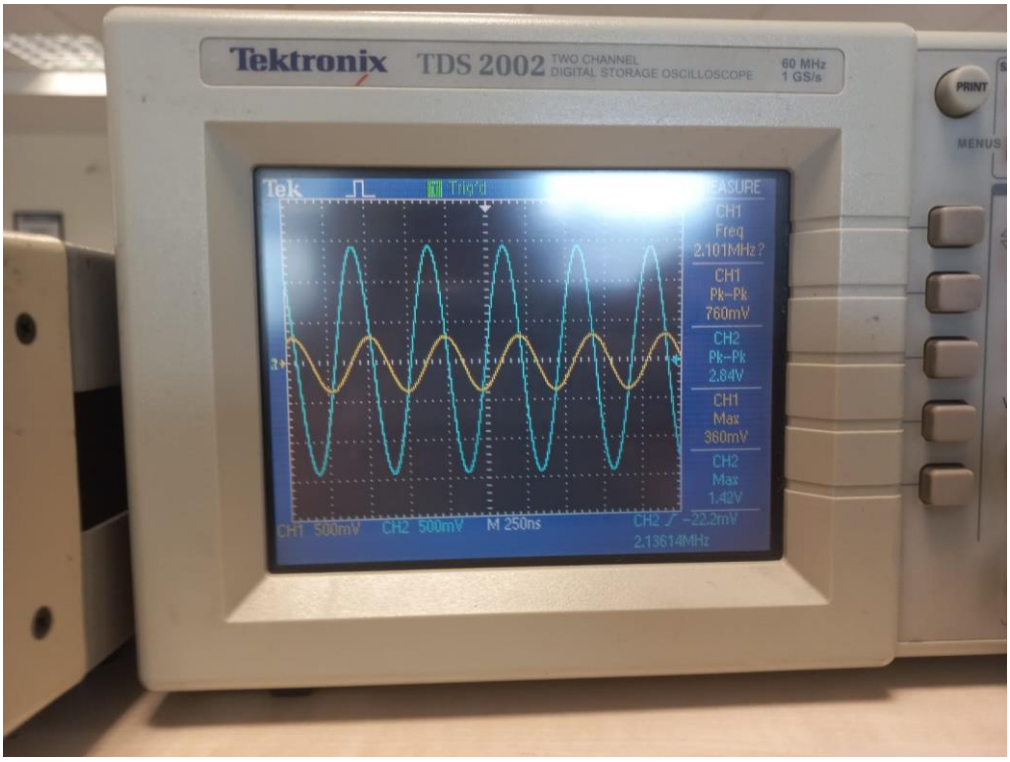

Figure 2.2.5: Output Voltage = 760mV; Gain = -8.40 when Input is 2.10MHz

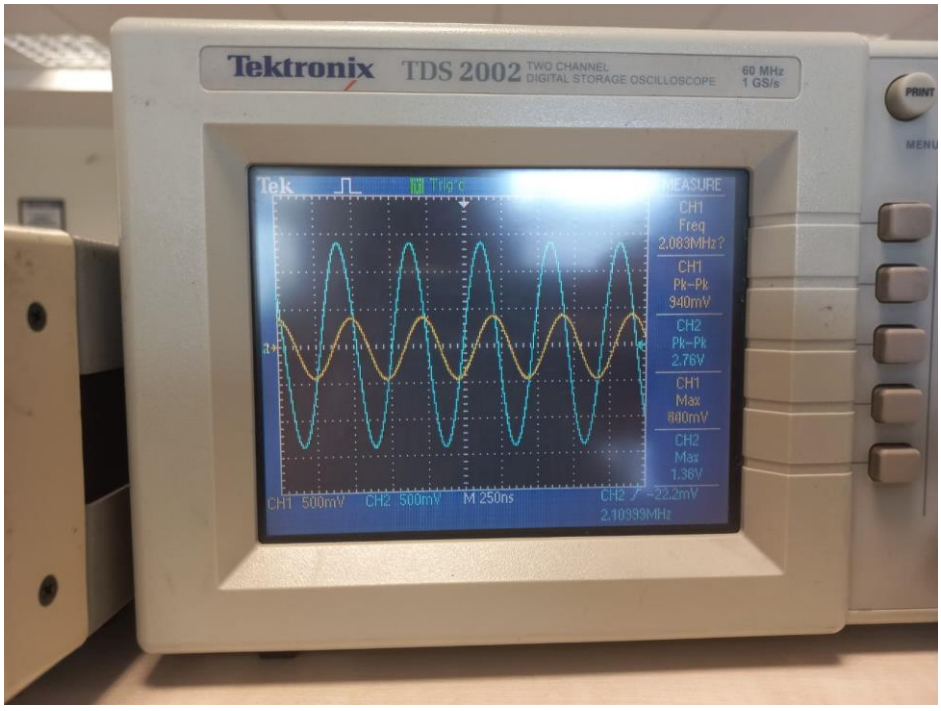

Figure 2.2.6: Output Voltage = 940mV; Gain = -6.55 when Input is 2.05MHz

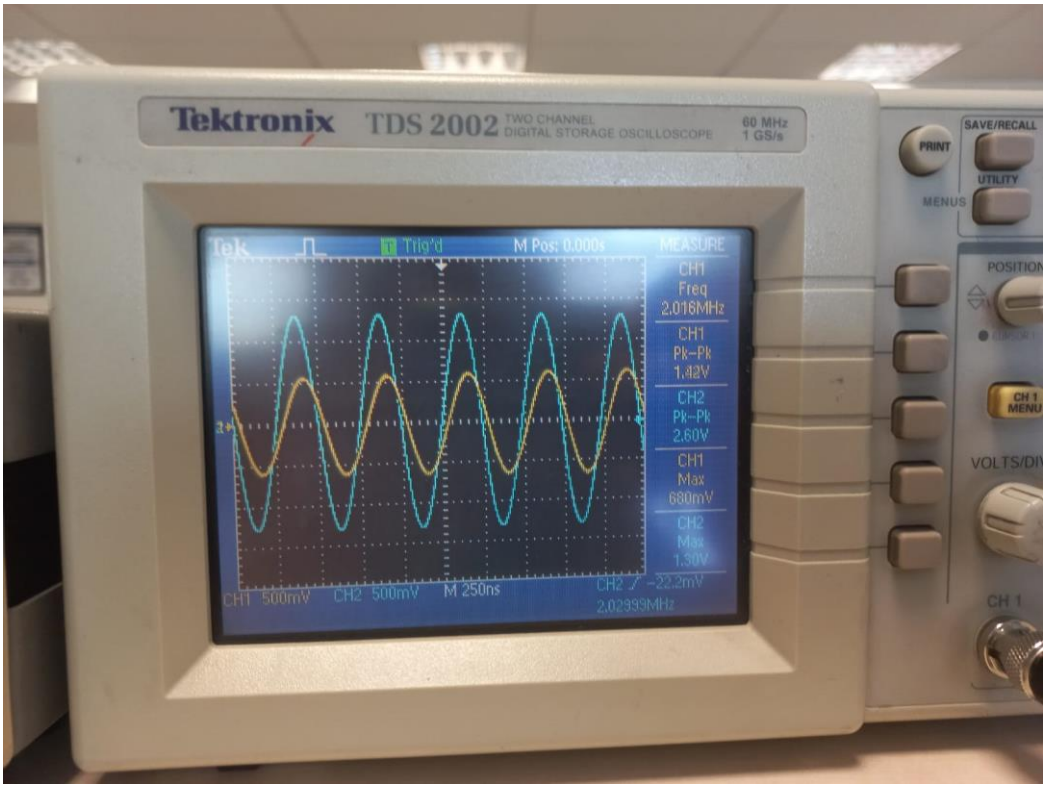

Figure 2.2.7: Output Voltage = 1.42V; Gain = -2.97 when Input is 2.00MHz

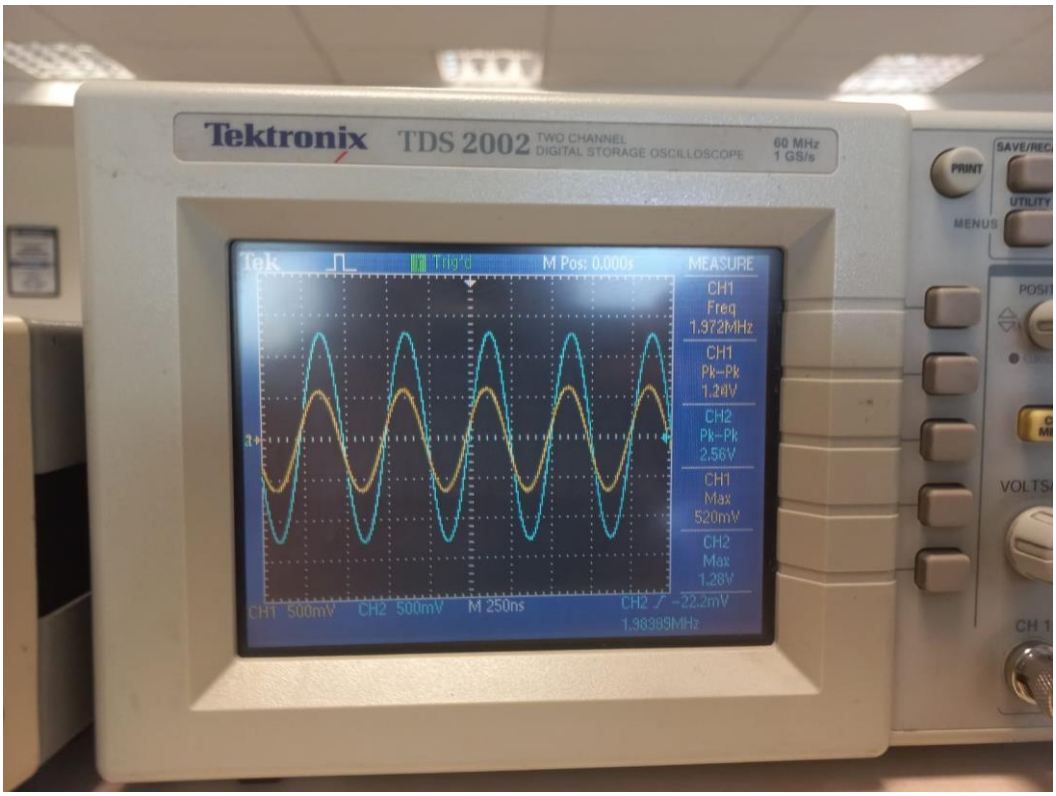

Figure 2.2.8: Output Voltage = 1.24V; Gain = -4.15 when Input is 1.95MHz

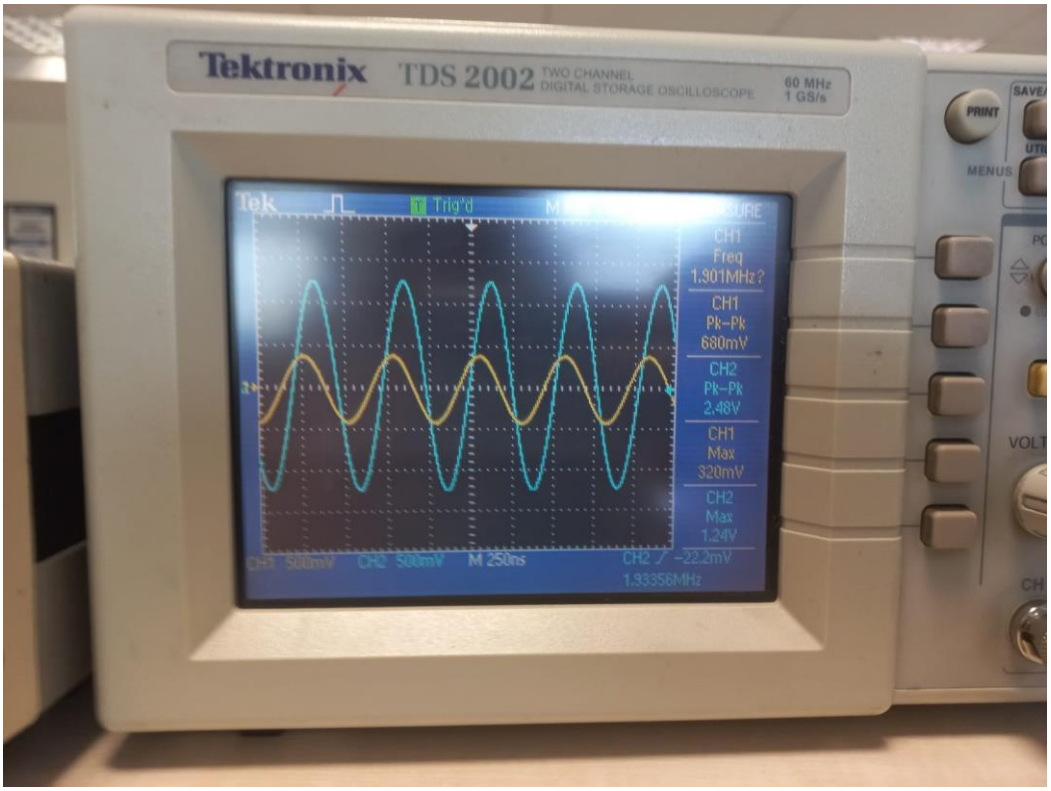

Figure 2.2.9: Output Voltage = 680mV; Gain = -9.37 when Input is 1.90MHz

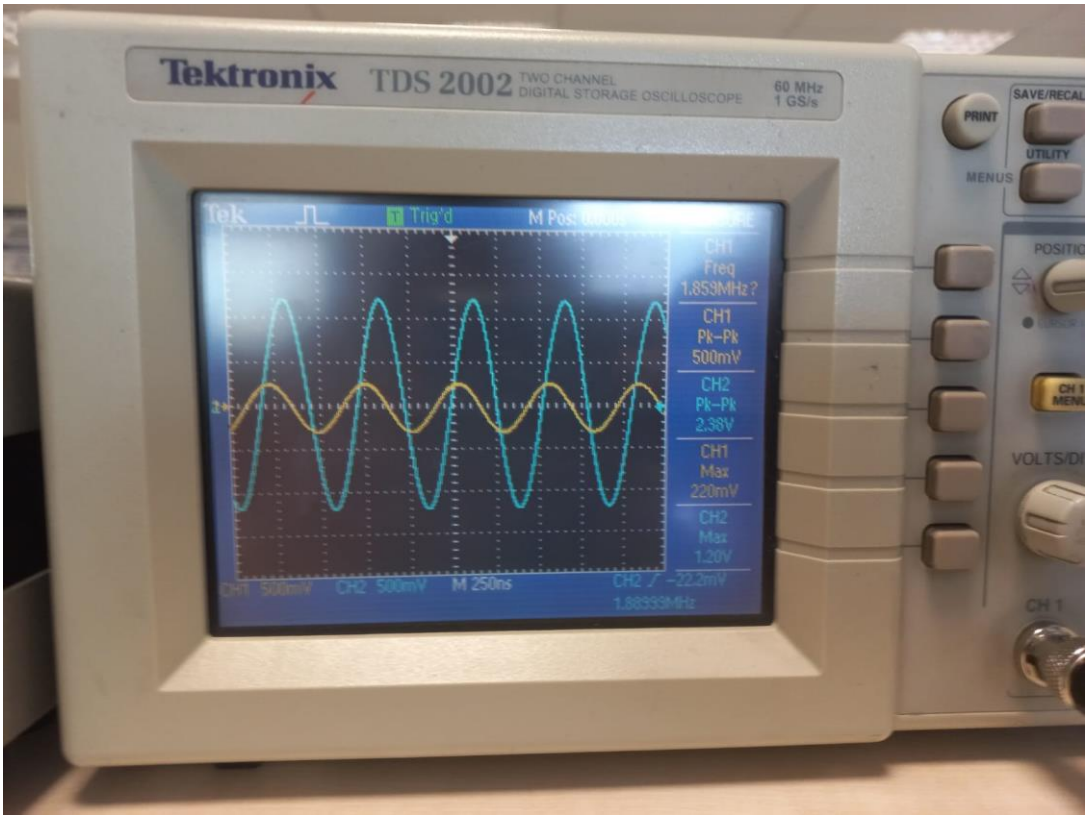

Figure 2.2.10: Output Voltage = 5000mV; Gain = -12.04 when Input is 1.80MHz

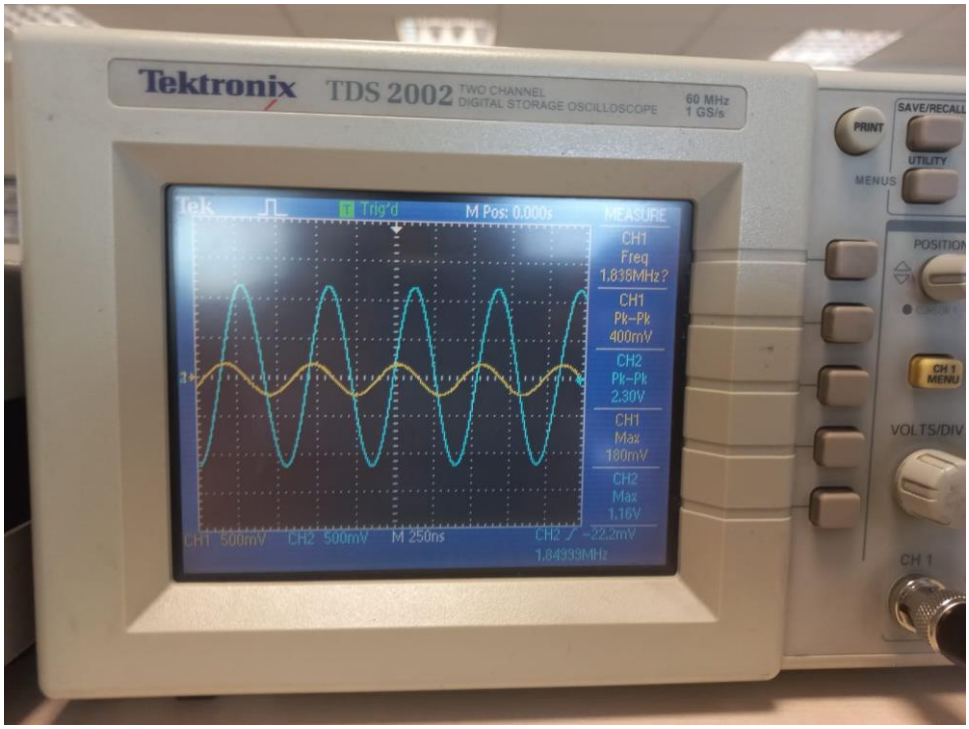

Figure 2.2.11: Output Voltage = 400mV; Gain = -13.97 when Input is 1.70MHz

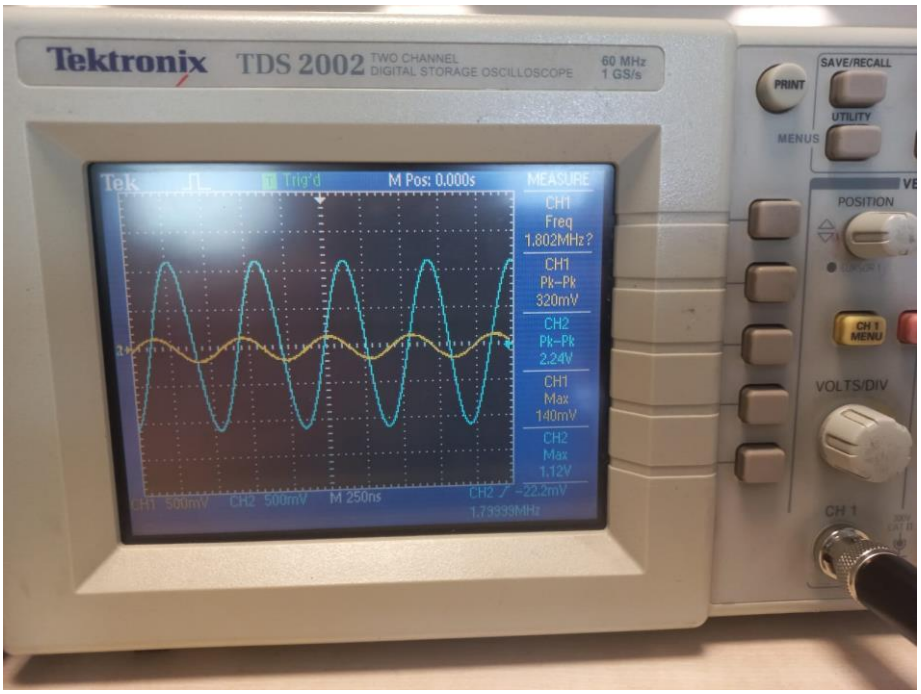

Figure 2.2.12: Output Voltage = 320mV; Gain = -15.91 when Input is 1.60MHz

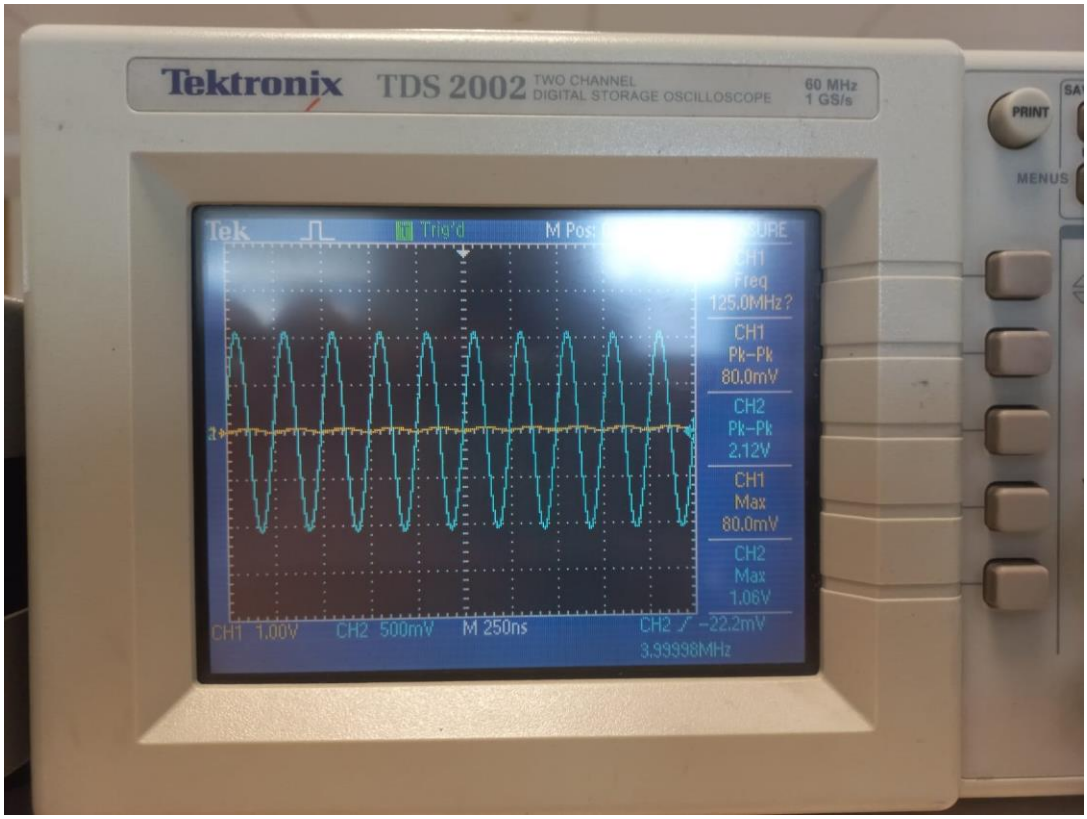

Figure 2.2.13: Output Voltage = 80mV; Gain = -27.95 when Input is 4.00MHz

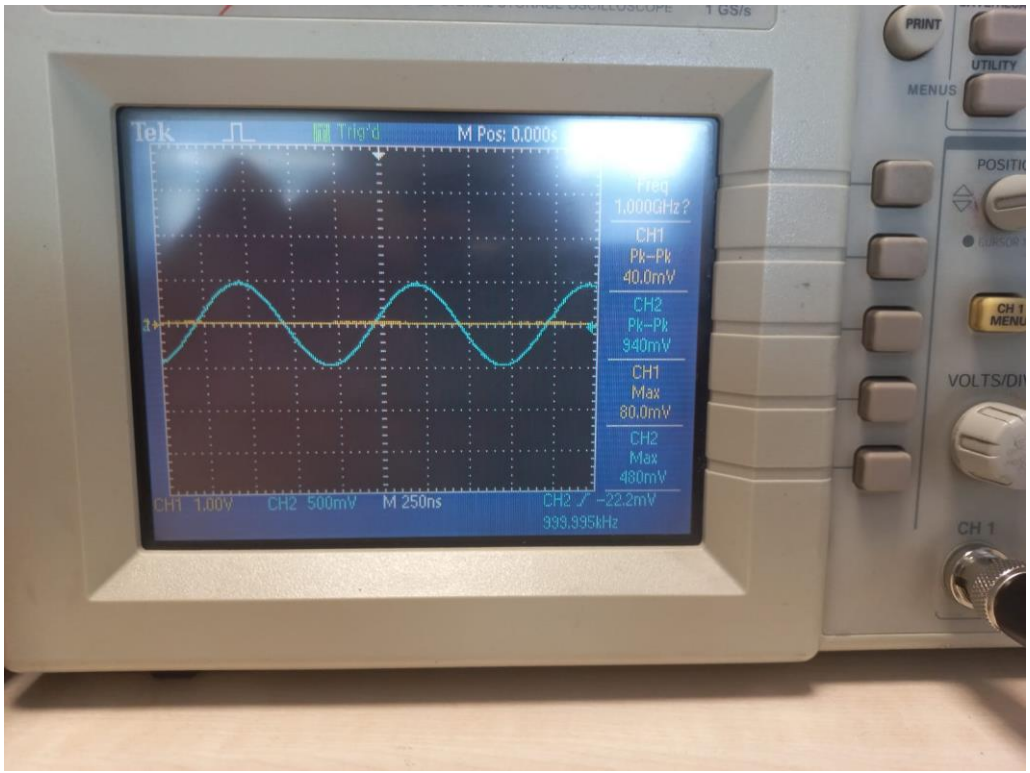

Figure 2.2.14: Output Voltage = 40mV; Gain = -33.97 when Input is 1.00MHz

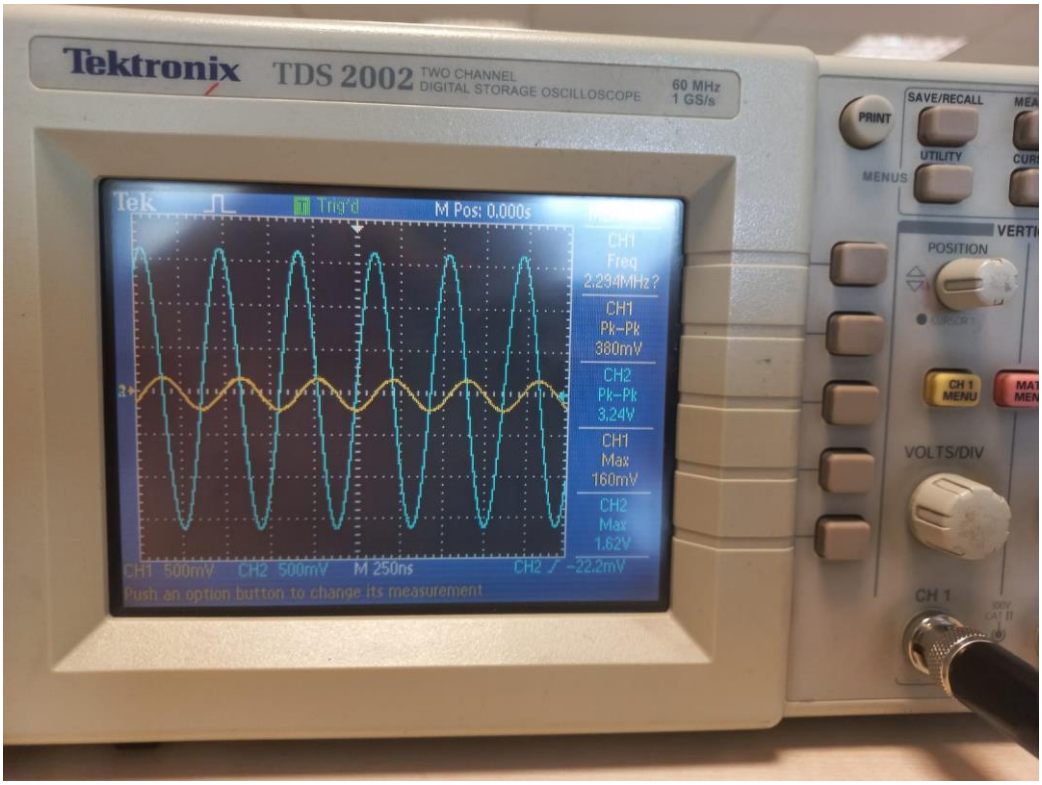

Figure 2.2.15: Output Voltage = 380mV; Gain = -14.42 when Input is 2.30MHz

Here is the MATLAB plot of the hardware results **(Figure 2.2.16)**:

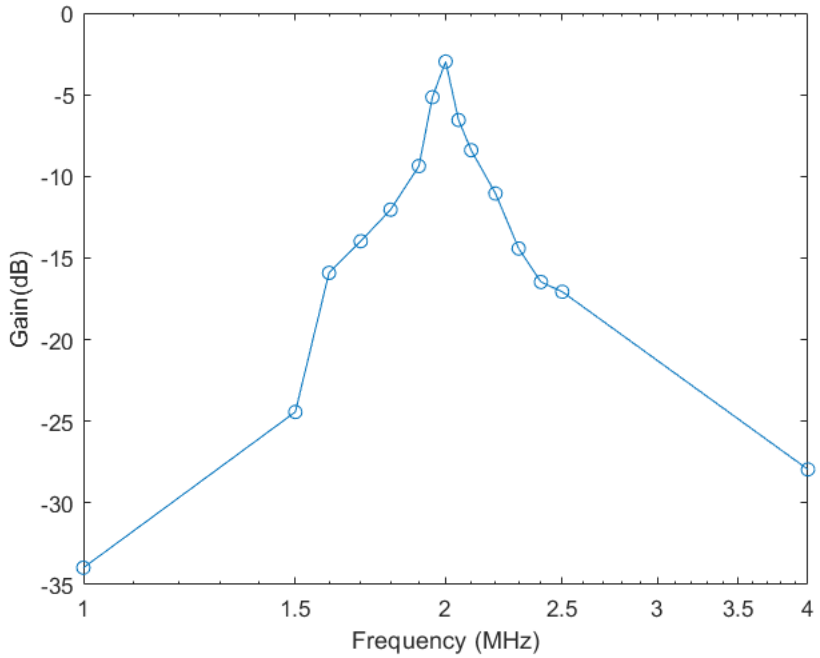

Figure 2.2.16: Frequency vs Gain Plot of the Hardware Results

3- Conclusion

In this lab, we were assigned to design a band-pass filter for a 50Ω load resistance with specific requirements. There were both some errors in the software and hardware parts. In the software part, since LTSpice cannot create real life continous line plots, there were room for rounding some decimals in our findings and this was a reason for the software part errors.

In the hardware part, the error was bigger than the software part as expected. The main reason behind the error was the lack of components with the exact desired values. Also, the lack of calibration of the oscilloscopes and signal generators was another main reason for the error. The frequency given from the signal generator was not matching the frequency on the oscilloscope screen. Also, the self-inductance, and self-capacitance of each component and wires might also contribute to the error.

Considering both software and hardware results, we can say that the lab was a complete success. In both parts, we managed to do what we aimed for with very small error margins. Our hardware plot was pretty similar to the plot we obtained from LTSpice. Figures 1.3.1 & 2.2.16 are very similar in many cases. I believe this lab to be very helpful for understanding how filters work.