1 Work Done

In this report, I will provide detailed information on the work I conducted throughout my internship. This report consists of six subsections: background information, needs, requirements, design process, verification and cost analysis. All these subsections are about the pyrotechnic activation test circuit I designed. I will first introduce some background information regarding the project. Then, I will explain in a detailed manner the industrial need for the project; the technical requirements of the circuit; the entire design process including both the simulation phase which I used LTSpice and the PCB design phase which I used Altium Designer; the verification of the project; and finally, the cost analysis for a single PCB unit.

1.1 Background Information

In missile systems, there are various methods to trigger the detonation/activation mechanism. Mechanical activation is the activation process where the trigger source for the detonation is an impact or a pressure applied to the missile. There are some electronic activation methods that use timers and logic to trigger the detonation. Magnetic activation is the method where a magnetic field change triggers the detonation. Radar-based or IR-based systems use proximity-fuze activation methodology in which optical sensors trigger the detonation of the missile when it gets close to its target and not necessarily on impact [3]. Then there is the pyrotechnic activation mechanism besides these methods.

Pyrotechnic activation circuits are used to trigger time-critical events that require a rapid and irreversible mechanical or explosive response [4]. In other words, a pyrotechnic activation circuit is the circuit which triggers the electro-chemical detonation mechanism of the missile. The activation circuit is present within the missile frame near a pyrotechnic composition.

A pyrotechnic activation circuit works by passing an absurdly high current through a single component -typically a resistor- when the microcontroller sends the detonation command. The high-current on the resistor causes vast amounts of heat to release. This heat then ignites the pyrotechnic composition creating a chain of chemical reactions which leads to the complete detonation of the missile warhead.

A pyrotechnic activation circuit should include carefully designed and multi-layered safety interlocks to prevent accidental triggering. Therefore, the activation circuits generally have proper shielding and multi-trigger signals to prevent EMI caused triggering. [4]

1.2 Needs

Some of the missiles in ROKETSAN use pyrotechnic activation mechanism to detonate/activate the missile. My department is responsible with not only designing, but also testing the electronics of some of the pyrotechnic activation circuits before actually assembling the missile. However, there is a bottleneck in testing the pyrotechnic activation circuits. The testing setup and the procedure of a pyrotechnic activation circuits is as follows.

There are pyrotechnic activation signals coming out from the central control unit's outer-world connectors. During testing, we send the "Firing Signal" from the microcontroller, and then measure whether the desired current passed through the power resistor during a desired time using a current probe. A sample diagram for the testing setup can be seen in the following figure.

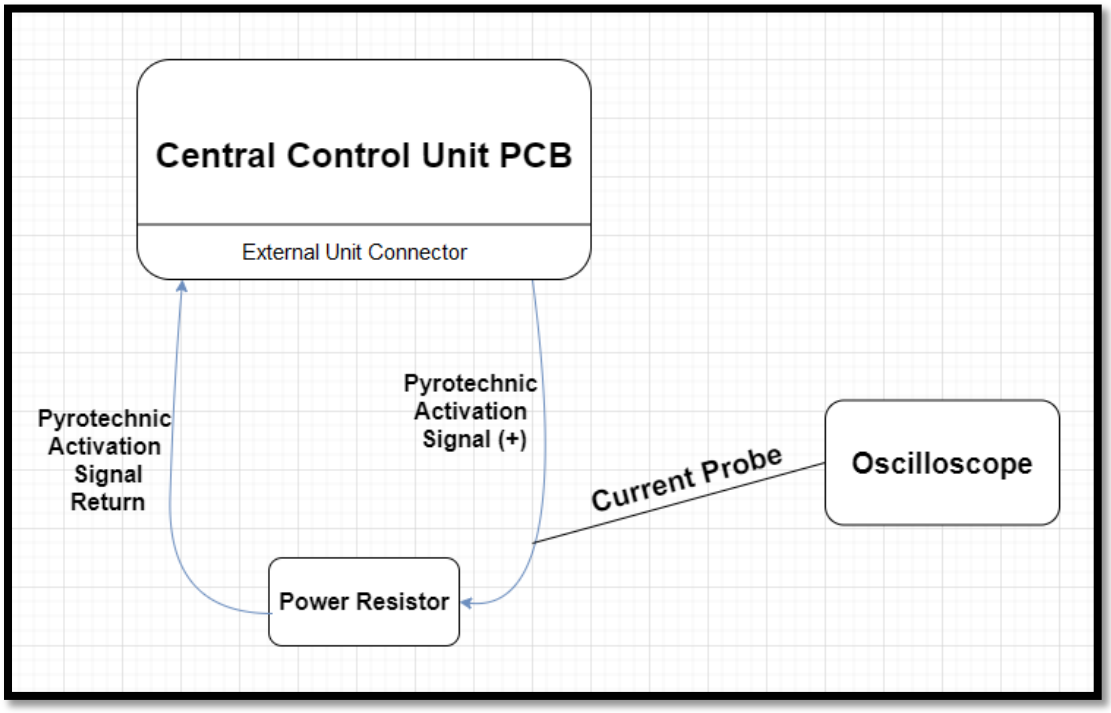


Fig. 2: Sample Diagram for the Pyrotechnic Activation Testing Setup

There can be multiple pyrotechnic activation signals coming out of a single control unit. Therefore, it is time consuming for the engineer running the tests to connect the probe, adjust the oscilloscope, connect the power resistor, measure the current level and the duration of the signal each time when testing the control unit. Considering an engineer is expected to test multiple control unit prototypes at once, there is an industrial need to speed this testing process up and reduce the time it takes to test a single pyrotechnic activation signal.

My goal in this summer internship is to address this industrial need and come up with a PCB design that will reduce the testing time for pyrotechnic activation signals.

1.3 Requirements

My supervisor told me about the technical requirements of the circuit in a detailed manner. The pyrotechnic activation signals are square pulses. Each pulse has a duration of 100ms. However, the current level of the pyrotechnic activation signals might change. The following figure shows an example pyrotechnic activation signal which has the shape of a square pulse.

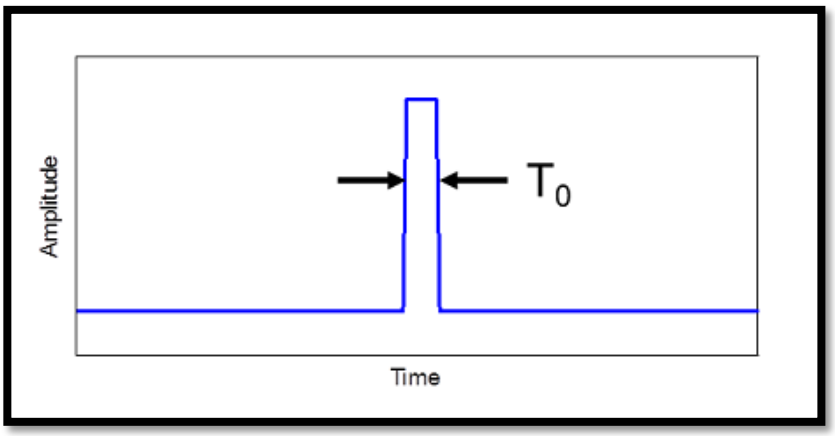


Fig. 3: A Sample Pyrotechnic Activation Signal (T_0 = 100ms)

My supervisor explained me that in my departments' designs, there are 4 different sets of current levels in pyrotechnic activation signals when creating a central control unit for a missile. The value of the power resistor we pass the activation signal on, also changes for different current levels. The following table shows the resistor values, current level limits and the duration of the signal for each preset of pyrotechnic activation signals designed in my department.

Table I: Conditions for each Preset

-	Power Resistor Value	Min Current Value	Max Current Value	Duration of the Signal
Preset 1	0.5 Ω	10.2 A	11 A	100ms
Preset 2	1 Ω	6.8 A	7.5 A	100ms

Preset 3	1 Ω	3.3 A	4 A	100ms
Preset 4	4.7 Ω	400 mA	800 mA	100ms

My supervisor explained me that the circuit I will design should take the pyrotechnic activation pulse as input and then verify whether the current level and the duration of the pulse is in the desired limits. If they are both in the limits, an indicator (possibly an LED) will verify. The user will choose the preset before sending the signal. The following figure is an example diagram for the input output relations of my circuit.

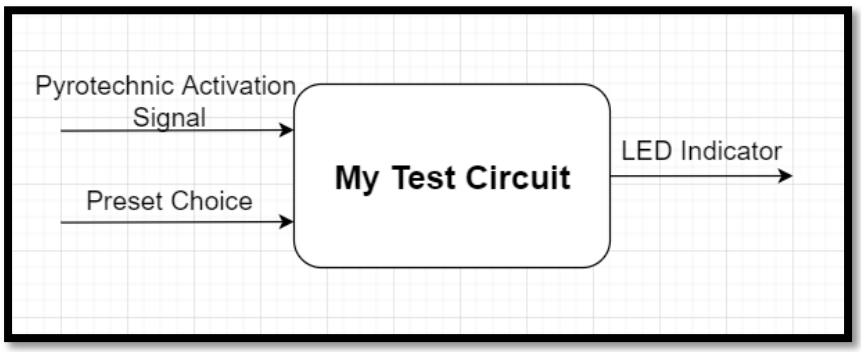


Fig. 4: Input-Output Diagram for the Circuit

My supervisor told me that I have a 10% tolerance margin for the current limits. However, the 100ms duration condition should be strictly complied. He finally mentioned that the circuit should work with DC 28V and/or 5V as power source.

This paragraph marks an end to the technical requirements of the circuit. The following section will focus on the design of the circuit. I will clearly explain my thought procedure while building the circuit step by step.

1.4 Design Process

This section consists of two subsections. Firstly, I will explain how I designed and simulated the circuit using LTSpice. Secondly, I will explain the procedure that led to the final PCB design using Altium Designer.

1.4.1 Circuit Design using LTSpice

After some initial thoughts, I came up with the following basic circuit diagram:

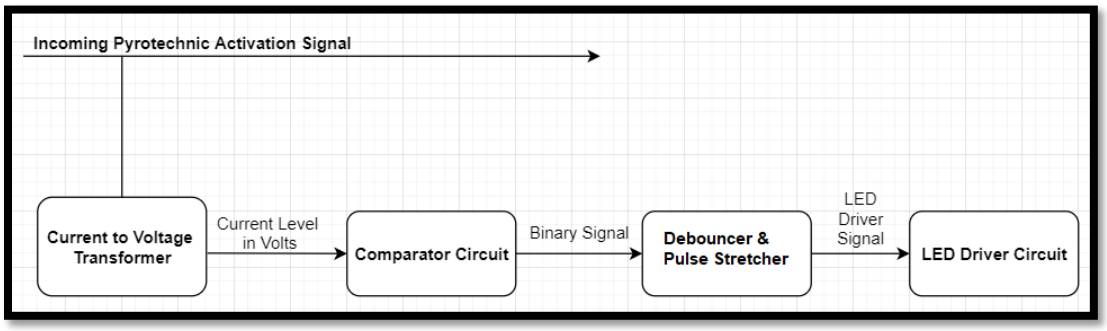


Fig. 5: Initial Circuit Diagram

The idea of mine is as follows. In order to setup a comparison circuit to check the incoming current level and the current limits, I should first create a circuit that transforms the incoming current level into a voltage level. This current to voltage transformer circuit works in parallel with the incoming pyrotechnic activation signal. Therefore, it does not change the incoming current level drastically.

The second sub-part of the diagram is the comparator circuit. The comparator circuit works with 2 comparator OPAMPs, one checking the minimum limit and the other checking the maximum limit. I plan on using switches and voltage dividers at the OPAMPs' input legs to change the minimum and maximum limits. Comparator circuit will give a binary output to indicate whether the incoming activation current level is within the limits.

Then, there is the debouncer & pulse stretcher circuit. It was my supervisor's advice to first check the current limits, and then check the 100ms duration condition for the signal. He advised me to research example debouncer circuits online. The debouncer circuit will check the 100ms duration condition. The pulse stretcher will extend the duration of the 100ms signal into a lengthier and visually distinguishable LED driver signal.

Finally, we have the LED driver circuit. If the incoming pyrotechnic activation signal passed both the current level condition and the 100ms duration condition, a green LED will light up.

It is important to note that the incoming pyrotechnic activation signal can be any arbitrary signal. Therefore, we carefully check each condition one by one to distinguish between the desired square pulses with desired amplitudes and durations, and any arbitrary signal.

The following figure shows my initial design for the current to voltage transformer circuit.

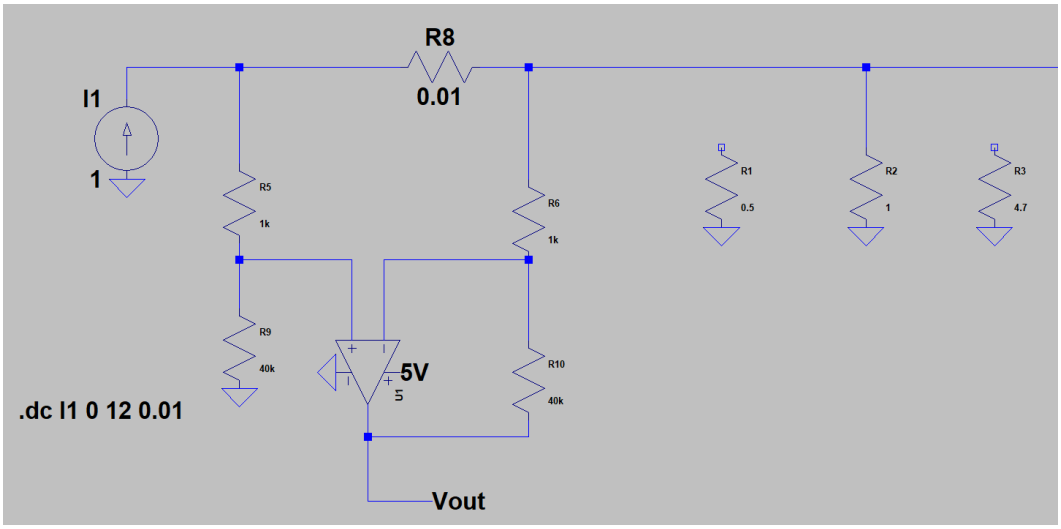


Fig. 6: Initial Current to Voltage Transformer Circuit

The idea behind this transformer circuit is as follows. On the right-hand side we have the three power resistors. There is also a subtractor OPAMP circuit that works in parallel to the incoming pyrotechnic activation signal. I used a small measuring resistor of 0.01Ω to not drop the current level on the power resistors significantly. To compensate this, I also used a high-gain subtractor circuit to get a voltage level variation near to 5V when there is 11A applied. The high-gain subtractor circuit measures the voltage difference between the two nodes of the 0.01Ω resistor and amplifies it.

The following figure shows the simulation output for the incoming current and the transformed voltage level.

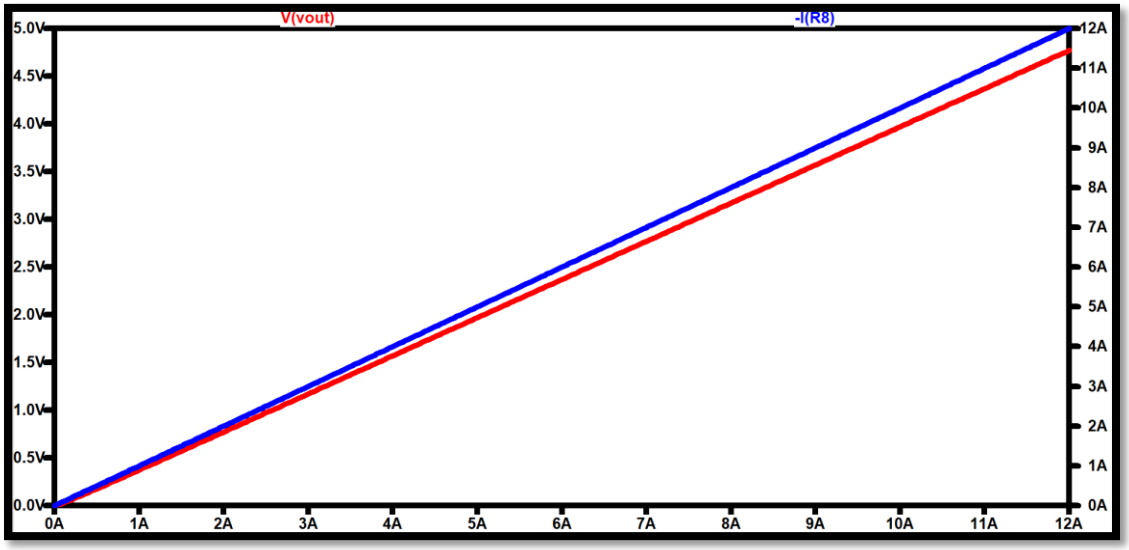


Fig. 7: Incoming Current (A) and Transformed Current (V) Values

As you can see in the simulation output, we have successfully created a circuit which transforms current level into voltage level. We have a gain of 0.4. This means when we apply 11A -which is the maximum current we expect the user to apply- to the power resistor, the circuit will transform it into 4.4V. The reason for this choice of gain was that I wanted to power the circuit with only 5V. I thought that this was possible even though my supervisor told me I could use 28V. If I could design the circuit such that 5V could supply the power, it would be a huge upgrade to the bare minimum requirements my supervisor gave me.

Next, it was time to design the second block in the diagram: Comparator Circuit. The following figure shows my initial design for the comparator circuit.

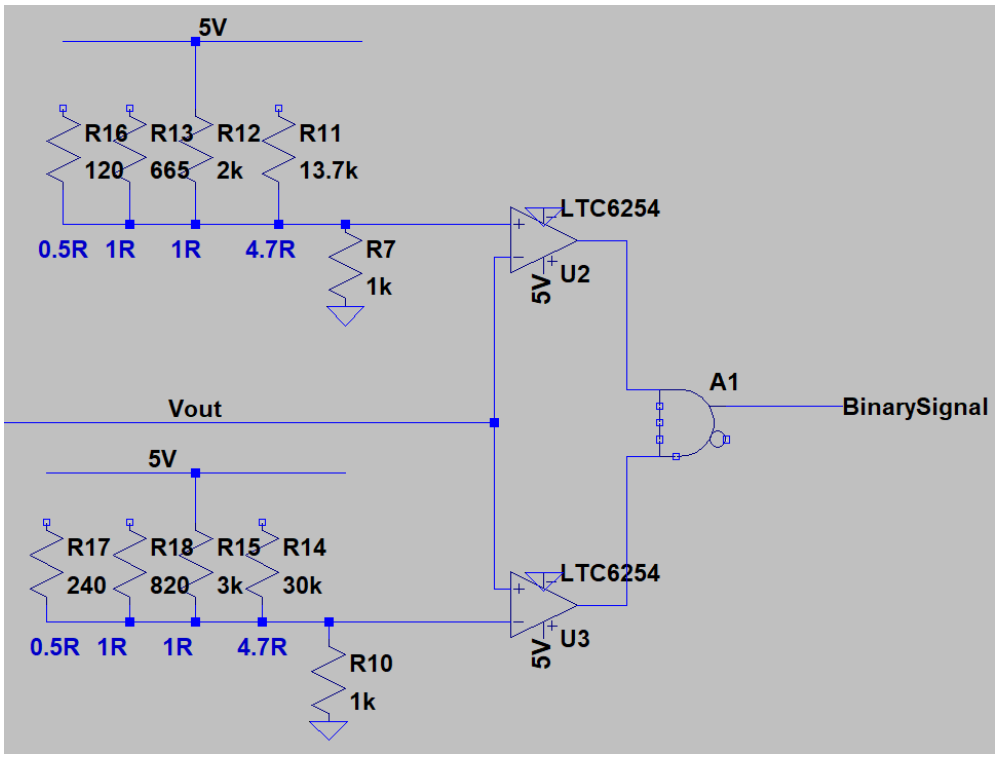


Fig. 8: Initial Comparator Circuit

The idea behind the circuit is as follows. We take the output of the previous transformer circuit as input. We use two comparator OPAMPs to compare the current level with maximum and minimum limits. In the PCB, switches will be used to change the limits as we change the preset. In the figure, the OPAMP at the upper side is the OPAMP that compares the maximum limit to the incoming current value. The OPAMP at the bottom side compares the minimum limit to the incoming current value. If the value we have is below the maximum limit and above the minimum limit, the AND gate at the output of the OPAMPs gives high output.

In the design, the resistor values at the input of the OPAMPs are critical. Since no current will flow to the OPAMPs if they remain in ON mode, a simple voltage divider using two resistors will be enough to determine minimum and maximum limits. I decided to use 1kΩ resistors at the GND side of the voltage dividers for convenience. Switches will be used in the PCB to choose the required resistor at the VCC side of the voltage divider.

The following table shows the resistor values to be used for each preset.

Table II: Initial Resistor Values for OPAMP Inputs

-	Lower Limit OPAMP			Upper Limit OPAMP		
-	GND-side Resistor	VCC-side Resistor	Divider Final Value	GND-side Resistor	VCC-side Resistor	Divider Final Value
Preset 1	1kΩ	225.5 Ω	4.08V	1kΩ	136.3 Ω	4.4V
Preset 2	1kΩ	838.2 Ω	2.72V	1kΩ	666.7 Ω	3V
Preset 3	1kΩ	2.78 kΩ	1.32V	1kΩ	2.13 kΩ	1.6V
Preset 4	1kΩ	30.25 kΩ	160mV	1kΩ	14.62 kΩ	320mV

After consulting to my supervisor, he told me that we use E96 resistor values at my department. I used resistor tables online to find out the closest resistor to the desired value [5]. The following table shows the revised values and the revised calculated voltage divider values.

Table III: Revised Resistor Values for OPAMP Inputs

-	Lower Limit OPAMP	Upper Limit OPAMP

-	GND-side Resistor	VCC-side Resistor	Divider Final Value	GND-side Resistor	VCC-side Resistor	Divider Final Value
Preset 1	1kΩ	240 Ω	4.03V	1kΩ	120 Ω	4.46V
Preset 2	1kΩ	820 Ω	2.74V	1kΩ	665 Ω	3V
Preset 3	1kΩ	3kΩ	1.25V	1kΩ	2kΩ	1.66V
Preset 4	1kΩ	30kΩ	161mV	1kΩ	13.7kΩ	340mV

Then, I simulated varying current levels and checked whether we can get the binary output high.

The following two figures show the Preset 1 circuit connections and the simulation output for the binary signal for varying incoming activation current level.

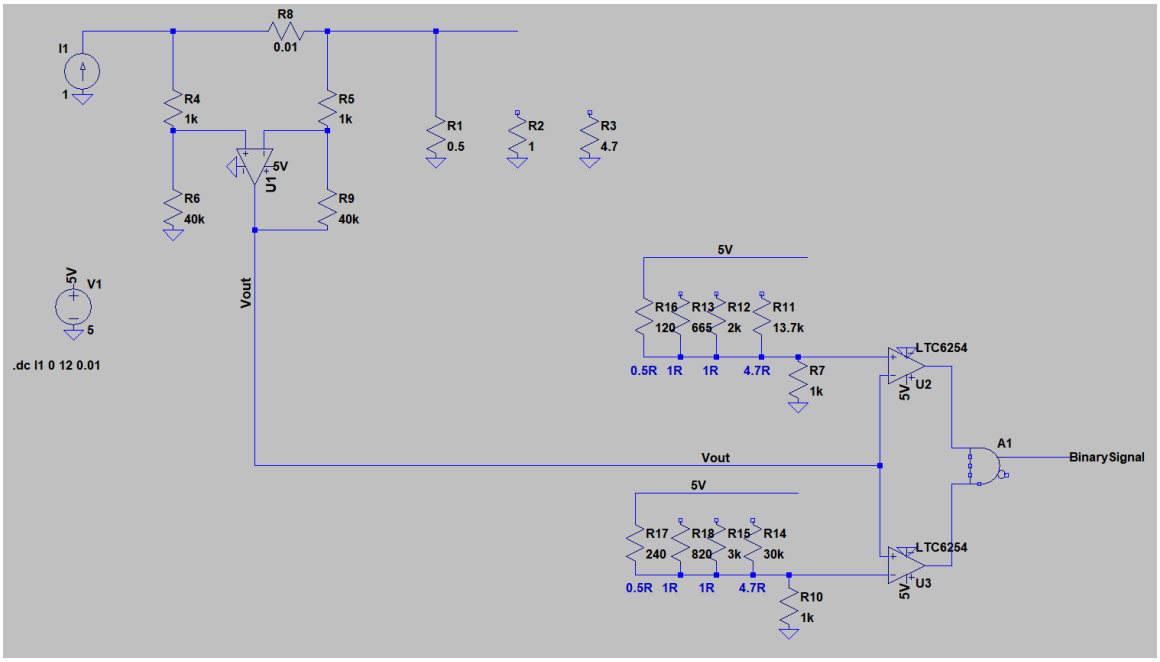


Fig. 9: Preset 1 Connections

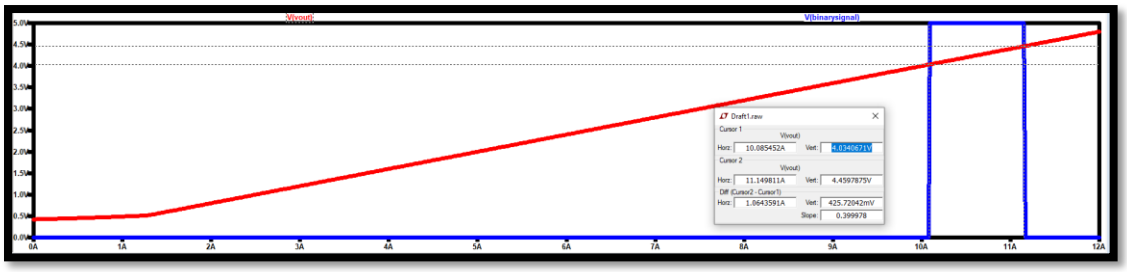


Fig. 10: Simulation Output for Changing Incoming Activation Current

As we can see in the simulation output, the maximum and minimum limits are well below the 10% tolerance threshold from Table I.

The following two figures show the Preset 2 circuit connections and the simulation output for the binary signal for varying incoming activation current level.

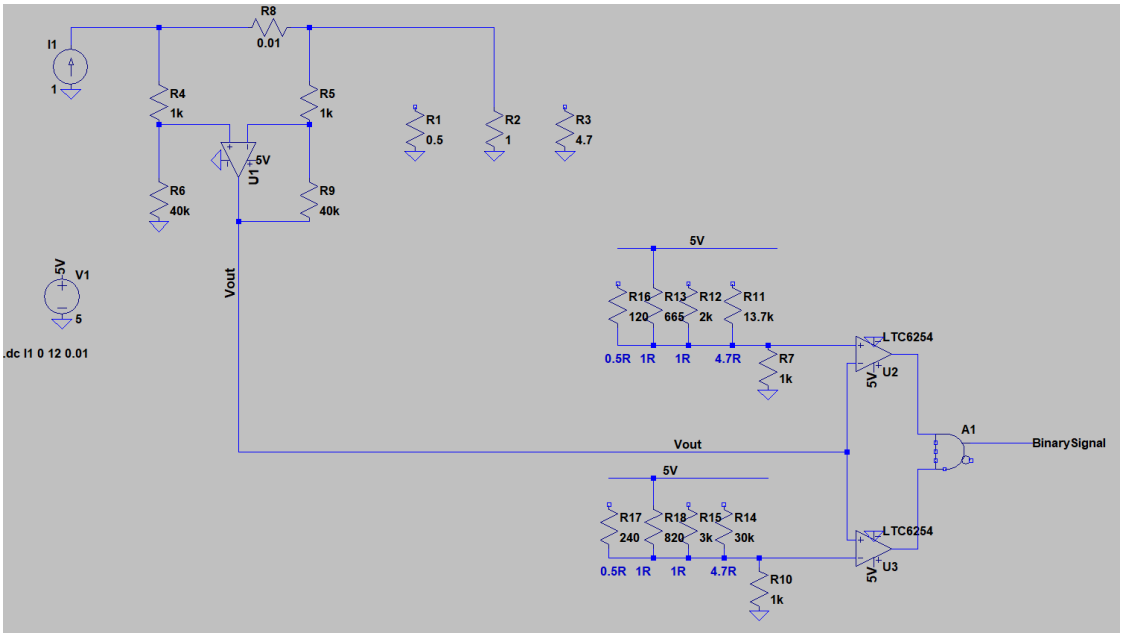


Fig. 11: Preset 2 Connections

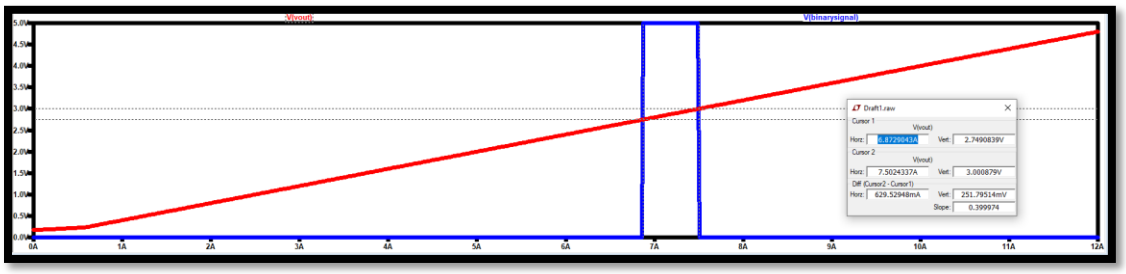


Fig. 12: Simulation Output for Changing Incoming Activation Current

As we can see in the simulation output, the maximum and minimum limits are well below the 10% tolerance threshold from Table I.

The following two figures show the Preset 3 circuit connections and the simulation output for the binary signal for varying incoming activation current level.

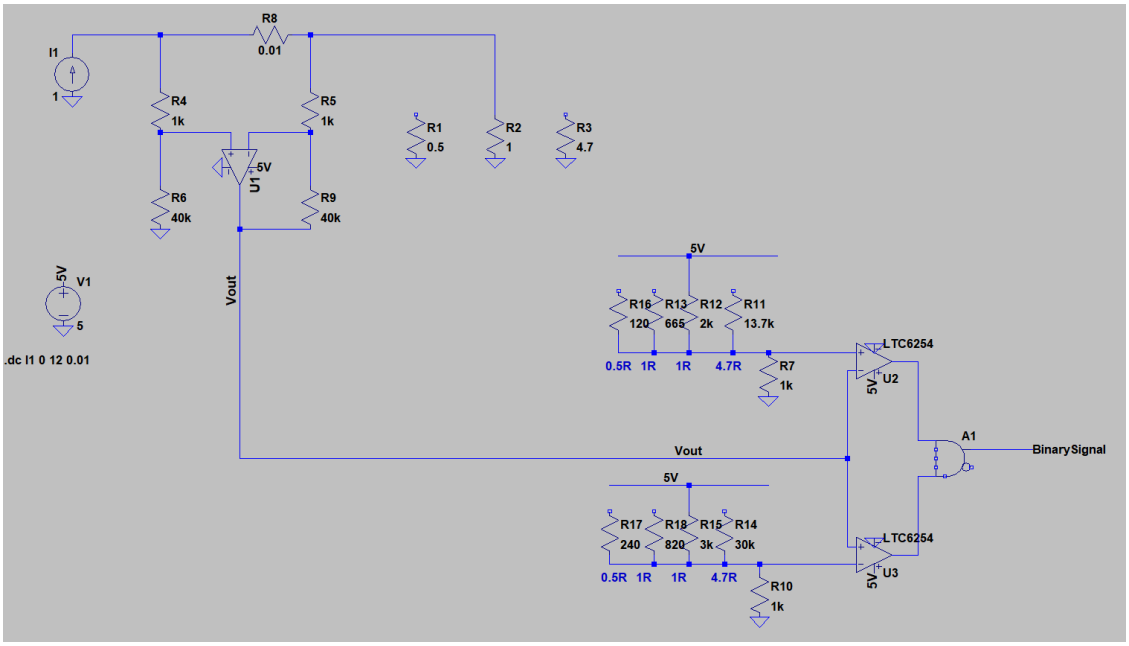


Fig. 13: Preset 3 Connections

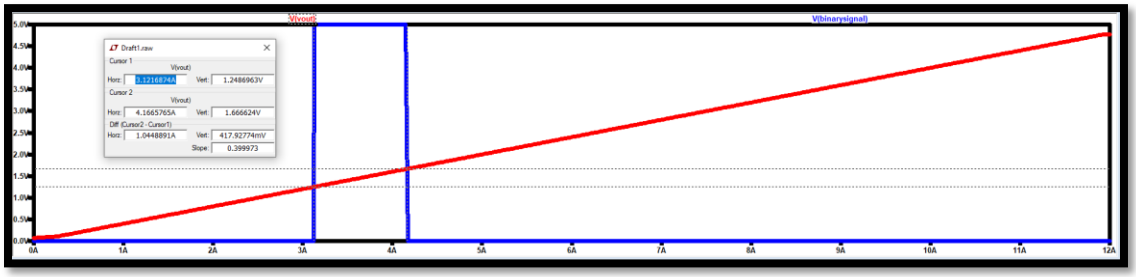


Fig. 14: Simulation Output for Changing Incoming Activation Current

As we can see in the simulation output, the maximum and minimum limits are well below the 10% tolerance threshold from Table I.

The following two figures show the Preset 4 circuit connections and the simulation output for the binary signal for varying incoming activation current level.

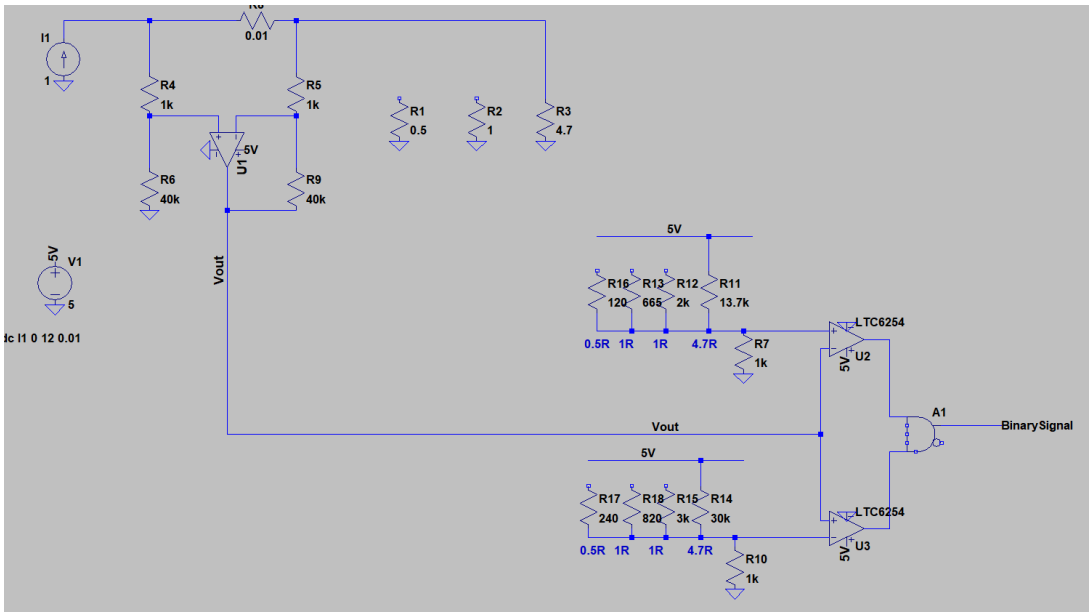


Fig. 15: Preset 4 Connections

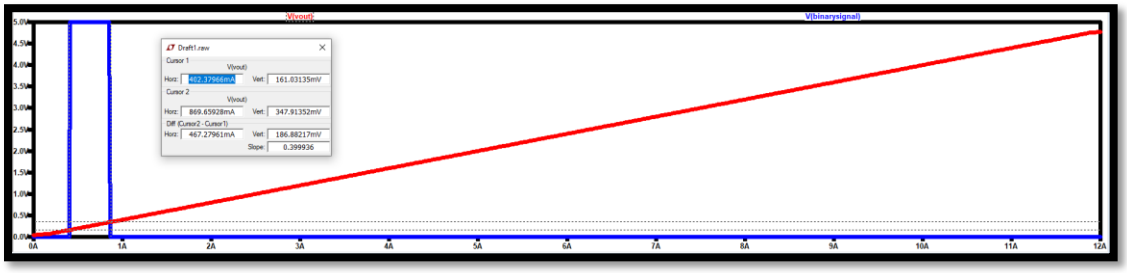


Fig. 16: Simulation Output for Changing Incoming Activation Current

As we can see in the simulation output, the maximum and minimum limits are well below the 10% tolerance threshold from Table I.

The following table shows the maximum and minimum limits for both the incoming current and the transformed voltage value for the binary signal to get high according to the last 4 simulations as well as the initial requirements for the current limits.

Table IV: Simulated Current and Voltage Values for a High Binary Signal

-	Lower Limit for Binary Signal	Upper Limit for Binary Signal

-	Initial Current Value	Simulated Current Value	Transformed Voltage Value	Initial Current Value	Incoming Current Value	Transformed Voltage Value
Preset 1	10.2 A	10.08 A	4.03 V	11 A	11.15 A	4.46 V
Preset 2	6.8 A	6.87 A	2.74 V	7.5 A	7.5 A	3 V
Preset 3	3.3 A	3.12 A	1.24 V	4 A	4.16 A	1.66 V
Preset 4	400mA	402mA	161mV	800mA	869mA	347mV

The simulation results are consistent with our initial estimations and well below the 10% tolerance threshold for the current level. This brings an end to the design of the comparator circuit. Now it is time to design the debouncer circuit.

The logic behind the debouncer circuit is pretty simple. We want to drive an LED if more than 100ms binary signal comes through -i.e. if 100ms of a signal within the current limits flows through the power resistor.

My initial thoughts included using an integrator OPAMP and a comparator OPAMP after. If the integrated output passed a certain voltage value (100ms of integration) the comparator would give a high output. However, before I implemented any of that thoughts, my supervisor suggested that I research two ICs: LTC6993 and LTC6994. He told me that I could design a debouncer circuit using these two ICs.

I used Digikey to find the datasheets of these two components [6, 7]. The LTSpice models for both ICs are embedded into the LTSpice at my computer in the “Special Functions” file in the “Components” tab. Therefore, I did not have any troubles finding the models for these two ICs. LTC6994 is a delay block generator, LTC6993 is a pulse generator. My initial intention was using LTC6994 to check the 100ms duration condition and LTC6993 to stretch out the duration of the incoming binary pulse.

After reading the datasheet of LTC6994, I found out there are 2 types of delay triggers for different LTC6994 models: LTC6994-2 is rising-edge triggered; LTC6994-1 is both-edge triggered. I would need a rising-edge triggered version because the

100ms condition I pursue is for the high-side of the pulse. I don't want to trigger LTC6994 with a falling-edge. Therefore, in my design I decided to use LTC6994-2.

After reading the datasheet of LTC6993, I found out there were 4 types of LTC6993 models. They were categorized by their trigger types -rising or falling edge- and the presence of their retrigger property. I would obviously need a rising-edge triggered version as my previous LTC6994-2 choice. I then decided that I would use the IC with no retrigger option. The reason for this choice is as follows. In the usage of my circuit during testing, there wouldn't be fast and consecutive pyrotechnic activation signals coming through within the lighting duration of the LED (A few seconds). Therefore, in the design it doesn't matter whether LTC6993 retriggers or not simply because there won't be a second signal coming through to retrigger the IC within a few seconds if the engineer running the tests does the job properly. When I checked the stocks of the company, I found out that LTC6993-1 -rising edge triggered with no retrigger property- was in the stocks. However, LTC6993-2 -rising edge triggered with retrigger property- was not in the stocks.

After deciding which specific ICs I would use in my design, I started to design the circuit. The following figure shows my initial design for the debouncer circuit.

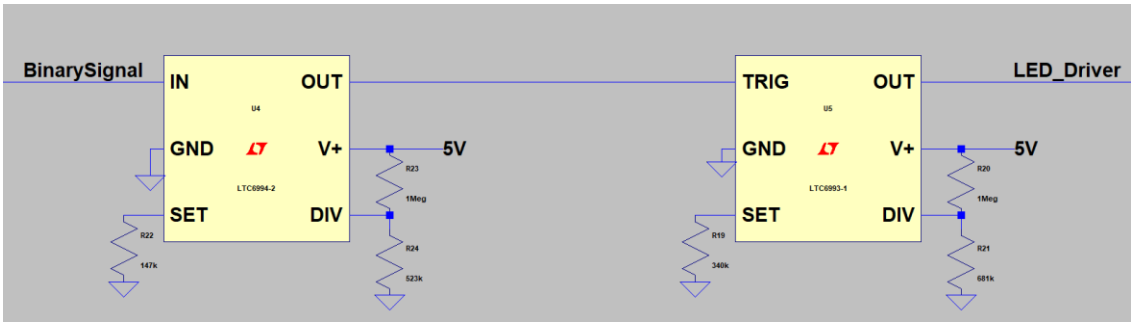


Fig. 17: Initial Debouncer Circuit

The choice of the resistor values within both IC's DIV and SET pins are reasoned from the datasheets. I tuned those resistor values such that a pulse with exactly a 100ms duration would trigger the debouncer mechanism and the LED would be driven for 1-2 seconds.

The following two figures show two different simulation outputs for the debouncer circuit. The first figure is from a circuit with exactly a 100ms of correct pyrotechnic activation signal passing through the power resistors. The second figure shows how the debouncer circuit acts when 95ms of correct pyrotechnic activation signal passed through the power resistors. The green line is the activation signal passing through the power resistors. The Red line is the voltage of the node which is LTC6994's output and LTC6993's input at the same time. The Blue line is the output of the LTC6993, which is also the LED driver signal. The color code is the same in both figures.

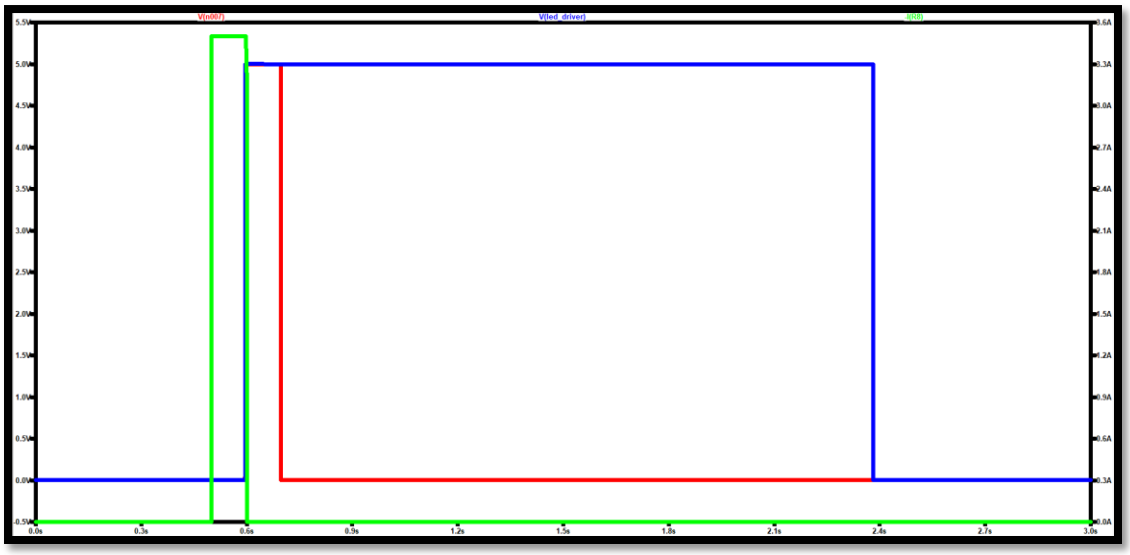


Fig. 18: Outputs of LTC6993&LTC6994 when 100ms of Activation Current with Correct Amplitude Passes Through the Power Resistors

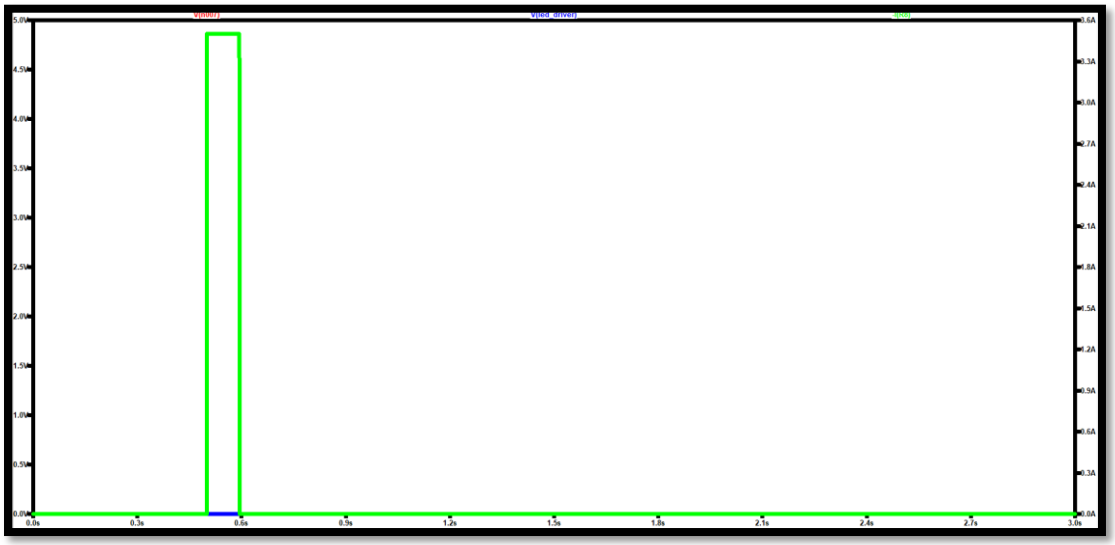


Fig. 19: Outputs of LTC6993&LTC6994 when 95ms of Activation Current with Correct Amplitude Passes Through the Power Resistors

As it can be seen from the figures, the debouncer circuit correctly detects the 100ms duration condition for the activation signal. However, it is important to note that the debouncer circuit drives the LED even if the activation signal is higher than 100ms. Nevertheless, this is not important because an activation signal with more duration than 100ms would still be enough to detonate the pyrotechnic composition within the missile.

Now it was time to move on to the LED driver circuit. I designed a simple LED driver using an NPN-BJT. The following figure shows the LED driver circuit.

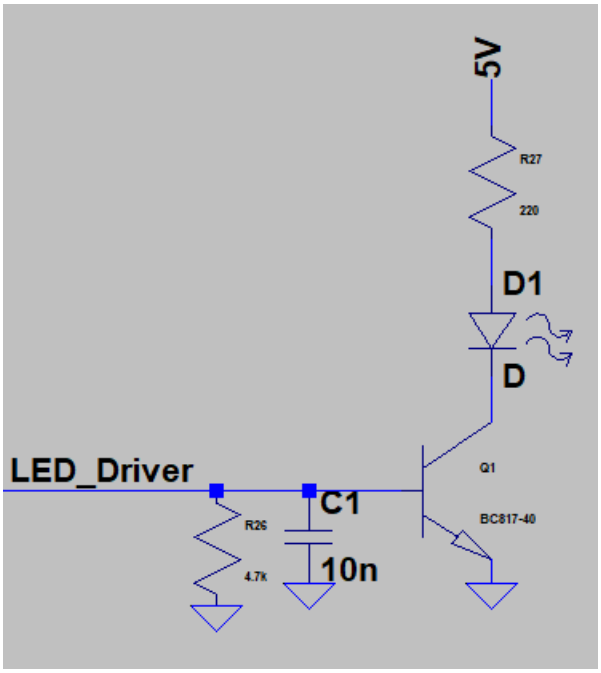


Fig. 20: LED Driver Circuit

The logic behind the circuit is pretty simple. When the debouncer circuit gives a high LED driver signal, the BJT is turned on. This allows a small amount of current to flow through the LED. The LED acts as a final visual indicator of the circuit. The next figure shows the simulation results for the flowing current on the LED and the incoming 100ms pyrotechnic activation signal.

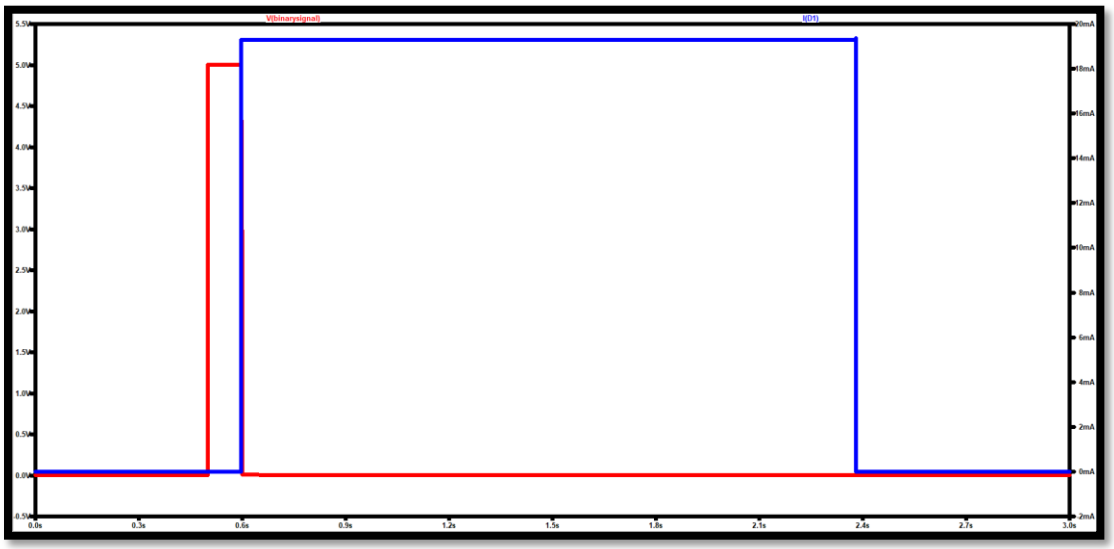


Fig. 21: LED Behavior for a 100ms Incoming Pyrotechnic Activation Pulse

The figure clearly shows that the LED is driven for about 1.8 seconds when a pyrotechnic activation signal with a desired amplitude and duration flows through the

power resistors. The 1.8 second duration for the LED is enough for the engineer running the tests of the central control unit to biologically see the LED.

The entire circuit design up to now can be seen in the following figure.

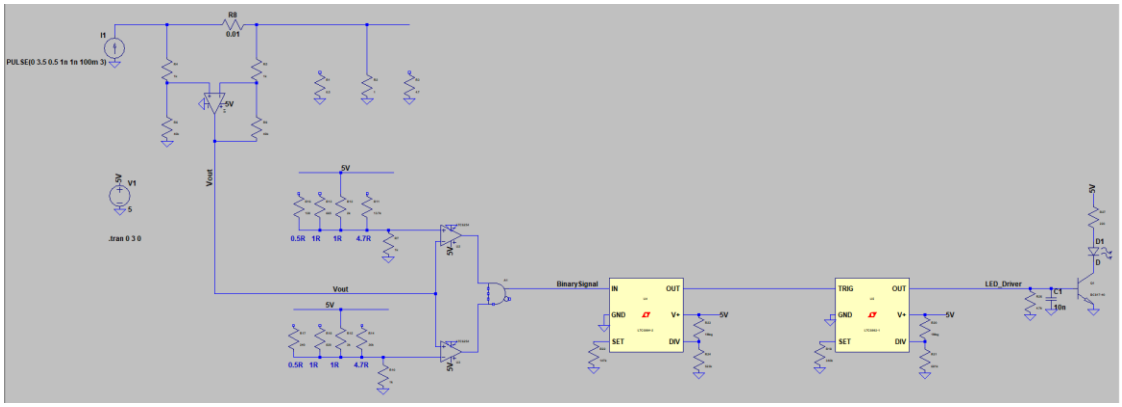


Fig. 22: Entire Circuit Up to This Point

The blocks in the circuit diagram can be seen clearly at the above figure. At this point, I have asked my supervisor to comment on the above circuit I designed. He made some critical comments and asked me to revise the circuit according to the following recommendations.

1. The Current-to-Voltage Transformer Block would be more precise with a current-reading IC instead of a subtractor OPAMP circuit. He recommended I search for the “MAX4080” IC.
2. The VCC pins of all ICs should have a small filtering capacitor attached to them in order to filter out high-frequency components of unwanted voltage spikes.
3. No pin of any IC should be connected to another pin of any another IC without a resistor in between. This is not a necessity since most ICs have high impedance at input pins and low impedance at output pins. However, it was general practice in ROKETSAN when designing circuits.

At this point, I started revising the circuit according to the feedback I got from my supervisor. Firstly, I started to research the MAX4080 IC. I accessed the datasheet of MAX4080 from its’ DigiKey page [8]. The IC was a current-to-voltage transformer. I found out that there were three gain versions available: MAX4080F with a gain of 5, MAX4080T with a gain of 20 and finally MAX4080S with a gain of 60. I would choose one of the MAX4080 models. I should choose the IC which I can map the incoming current range (0A-11A) most effectively to the 0V-5V range which the circuit works in. This wide-range mapping would minimize errors caused by IC offset voltages and several other factors in the circuit.

I had used a 0.01Ω resistor initially. This would mean the resistor would have 0V-110mV voltage difference range between its’ two nodes according to the incoming activation signal (0A-11A). MAX4080F would map this interval to 0V-550mV.

MAX4080T would map this interval to 0V-2.2V. MAX4080S would map this interval to 0V-6.6V.

MAX4080S exceeded the supply voltage threshold: 5V. Using a smaller measuring resistor (which was initially 0.01Ω) would be better for the circuit in order to not drop the incoming activation current much. Therefore, I decided to choose MAX4080T and use a 0.02Ω measuring resistor in order to map the interval onto 0V-4.4V range. I could have done the mapping with MAX4080F as well. However, this would lead to using a higher measuring resistor, which we don't want because of the possible current drop on the power resistor.

Finally, the trade-off between the wideness of the mapping range and the smallness of measuring resistor had been solved and a consensus was reached: 0.02Ω and 0V-4.4V. I found the LTSpice model for MAX4080T online at Analog Devices page and revised the circuit [9]. The following figure shows the revised current-to-voltage transformer circuit.

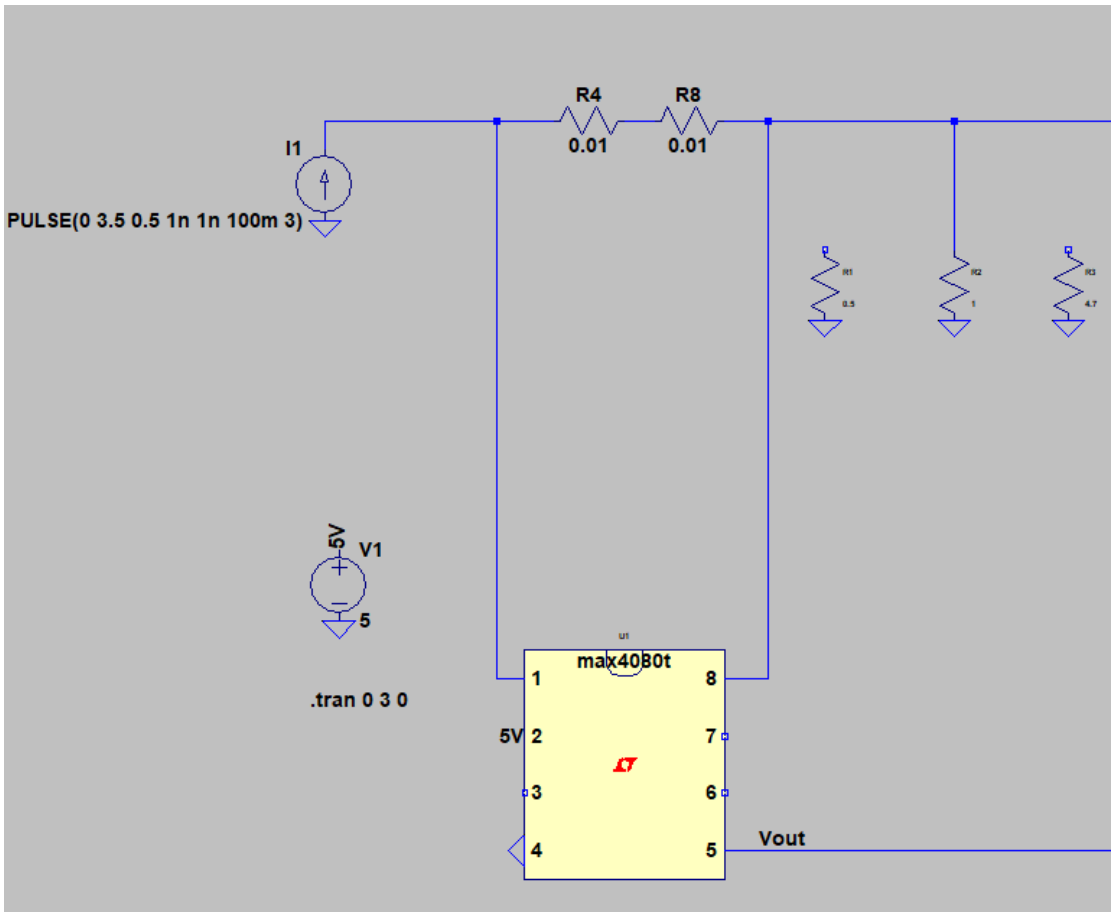


Fig. 23: Revised Current-to-Voltage Transformer Circuit

The following figure shows the varying output signal of MAX4080T according to the changing incoming activation current.

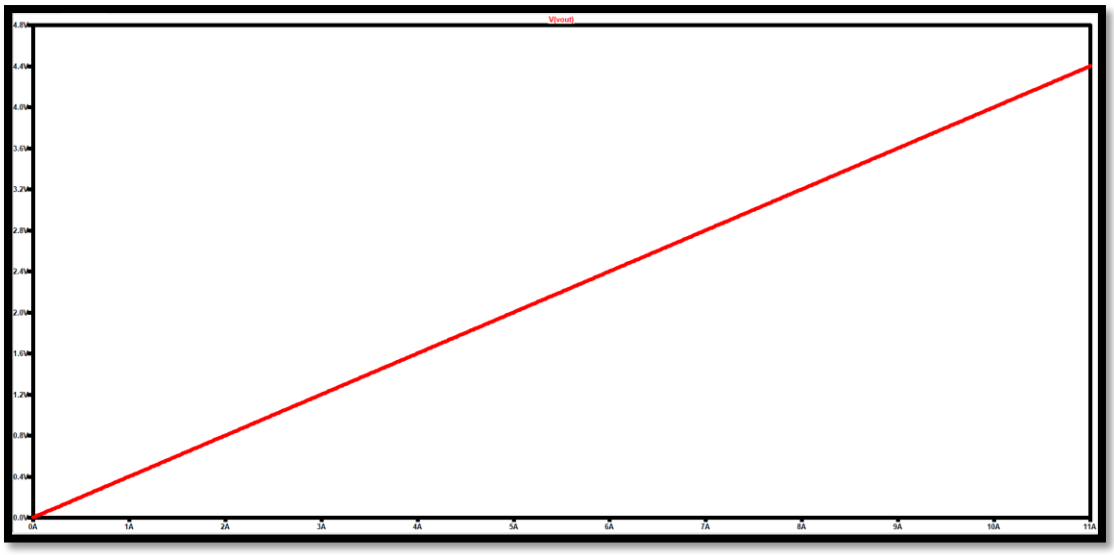


Fig. 24: Output of MAX4080T by Changing Incoming Activation Current

The simulation results show us that the mapping range for 0A-11A incoming current is 0V-4.4V as we anticipated. To our convenience, the total gain of the initial subtractor OPAMP circuit which was 40 did not change. The gain of MAX4080T is 20 and we doubled the value of measuring resistors. This means that we do not need to alter the resistor values in the OPAMP inputs of the comparator circuit.

After addressing the final two recommendations I got from my supervisor and adding resistors and capacitors to necessary nodes of the circuit, the fully revised circuit was complete. The following figure shows the entire revised circuit.

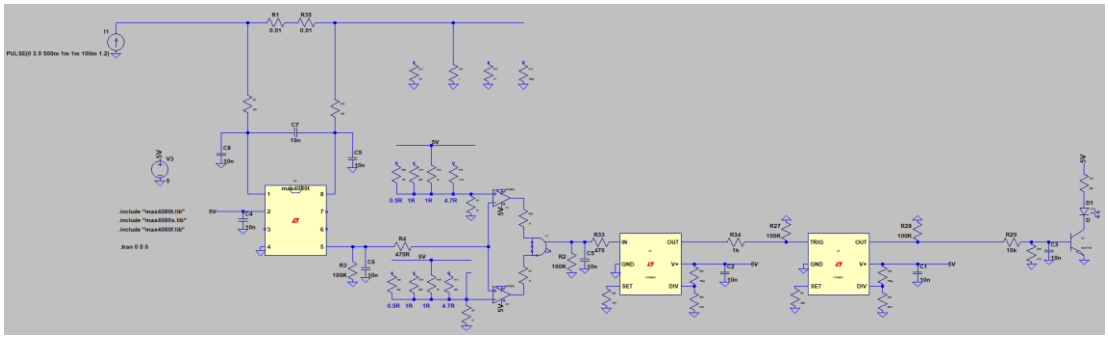


Fig. 25: The Fully Revised Entire Circuit

At this point, I have completed all three recommendations my supervisor gave me. I then once again asked for his feedback for the revised circuit. He said the circuit was looking fine and I could proceed to PCB design using Altium Designer.

1.4.2 PCB Design using Altium Designer

While designing the PCB, I did not use any ROKETSAN library or other online libraries for electronic components. I have created the schematic symbol library and the PCB footprint library all manually and by myself. I have only taken the 3D .stp files of PCB components from several online sources [10, 11, 12]. However, the schematic components and PCB footprints were completely designed by me checking datasheets over and over.

This section will proceed according to the following order. First, I will mention the creation of schematic library and introduce the components. Then, I will explain the circuit schematic. Thirdly, I will mention the creation of the PCB library and how I created the components. Finally, I will explain my PCB design.

The components in the schematic library can be seen in the following figure.

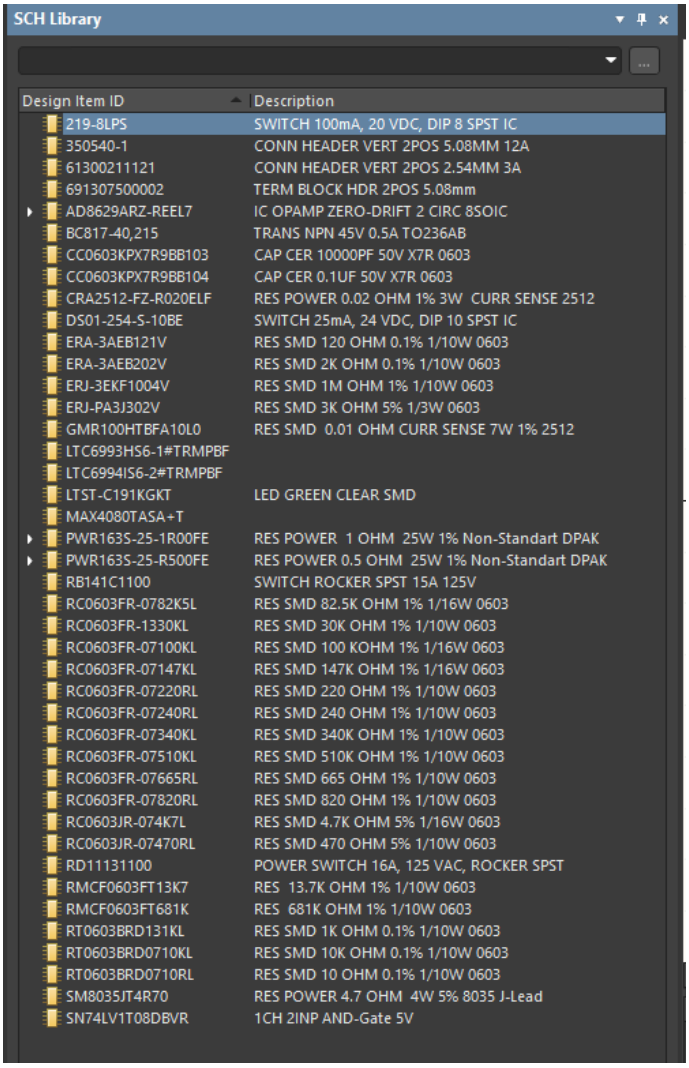


Fig. 26: The Schematic Library Components

I used DigiKey's website to search for datasheets of the components in the above names [10]. I used the datasheets to correctly numerate the pins of the ICs. The following 11 figures show the component symbols I have manually created.

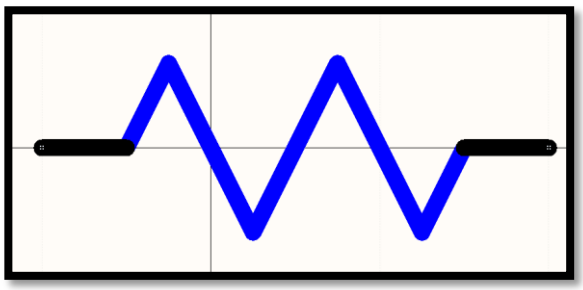


Fig. 27: The Schematic Symbol for All the Resistors in the Library

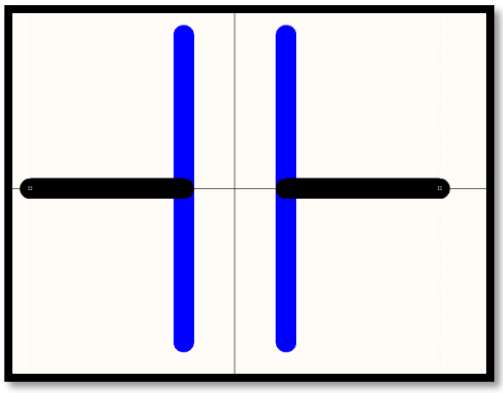


Fig. 28: The Schematic Symbol for All the Capacitors in the Library

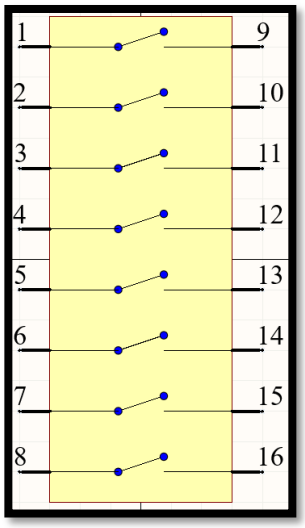


Fig. 29: The Schematic Symbol for the DIP Switch ;219-8LPS

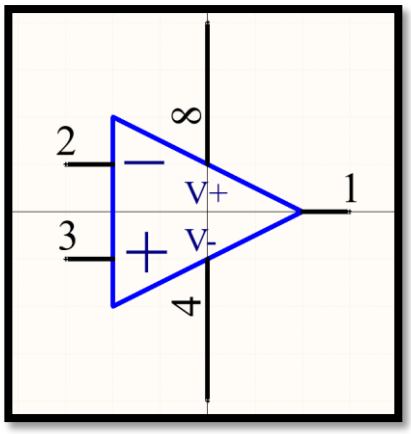


Fig. 30: The Schematic Symbol for the First Part of the Dual OPAMP; AD8629ARZ-REEL7

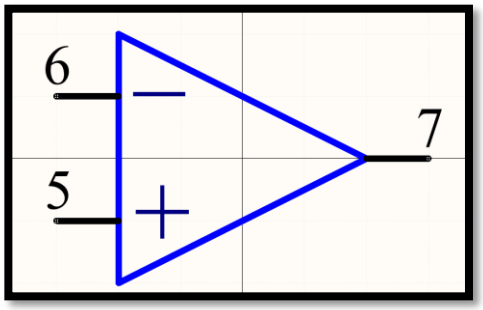


Fig. 31: The Schematic Symbol for the Second Part of the Dual OPAMP; AD8629ARZ-REEL7

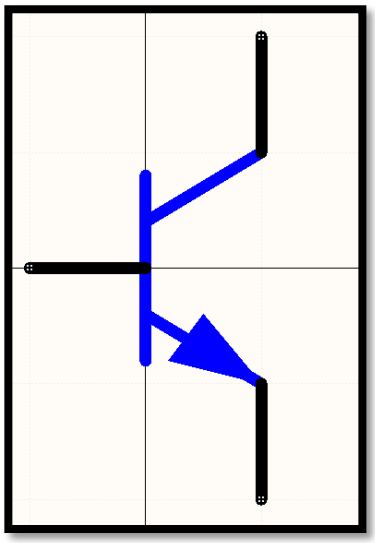


Fig. 32: The Schematic Symbol for the NPN-BJT; BC817-40,215

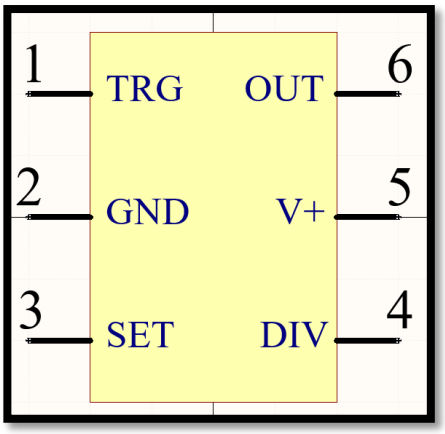


Fig. 33: The Schematic Symbol for the LTC6993HS6-1#TRMPBF

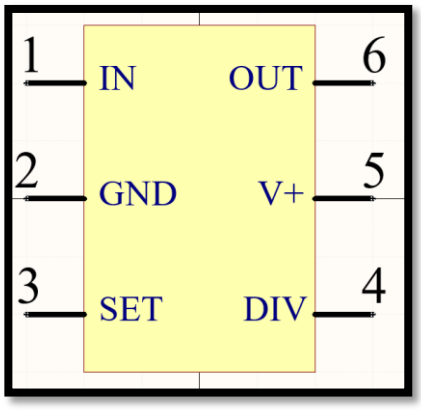


Fig. 34: The Schematic Symbol for the LTC6994IS6-2#TRMPBF_1

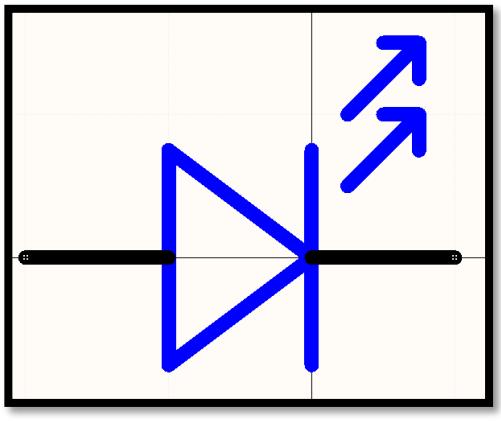


Fig. 35: The Schematic Symbol for the Green LED; LTST-C191KGKT

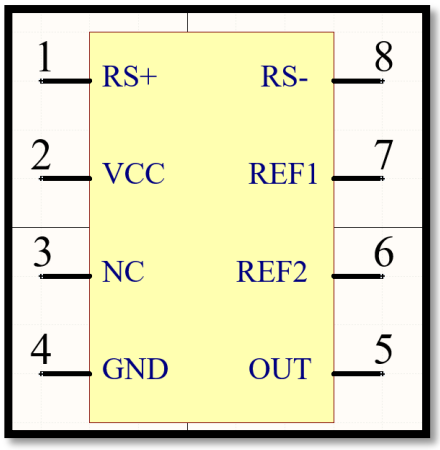


Fig. 36: The Schematic Symbol for the MAX4080TASA+T

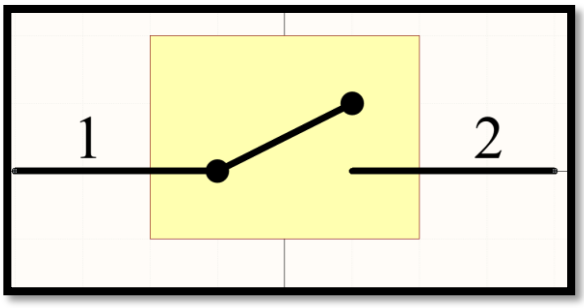


Fig. 37: The Schematic Symbol for the Power Switch; RD11131100

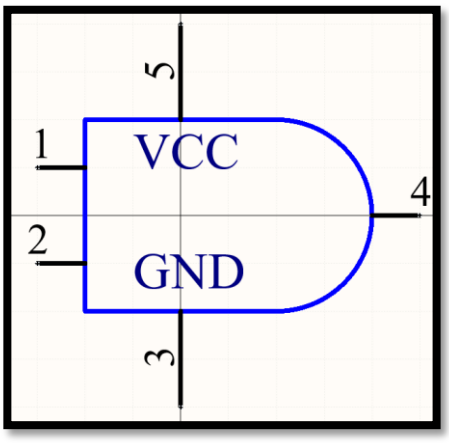


Fig. 38: The Schematic Symbol for the One-Channel AND-Gate; SN74LV1T08DBVR

These were the symbols that I manually created. I have used the same resistor symbol for all the resistors in the circuit. I have initially mainly used two different packages of resistors: 0402 and 0603.

Appendix 1 is the GitHub link to my schematic library.

After creating the library, it was now time to create a schematic document. The following figure shows the initial schematic of the circuit.

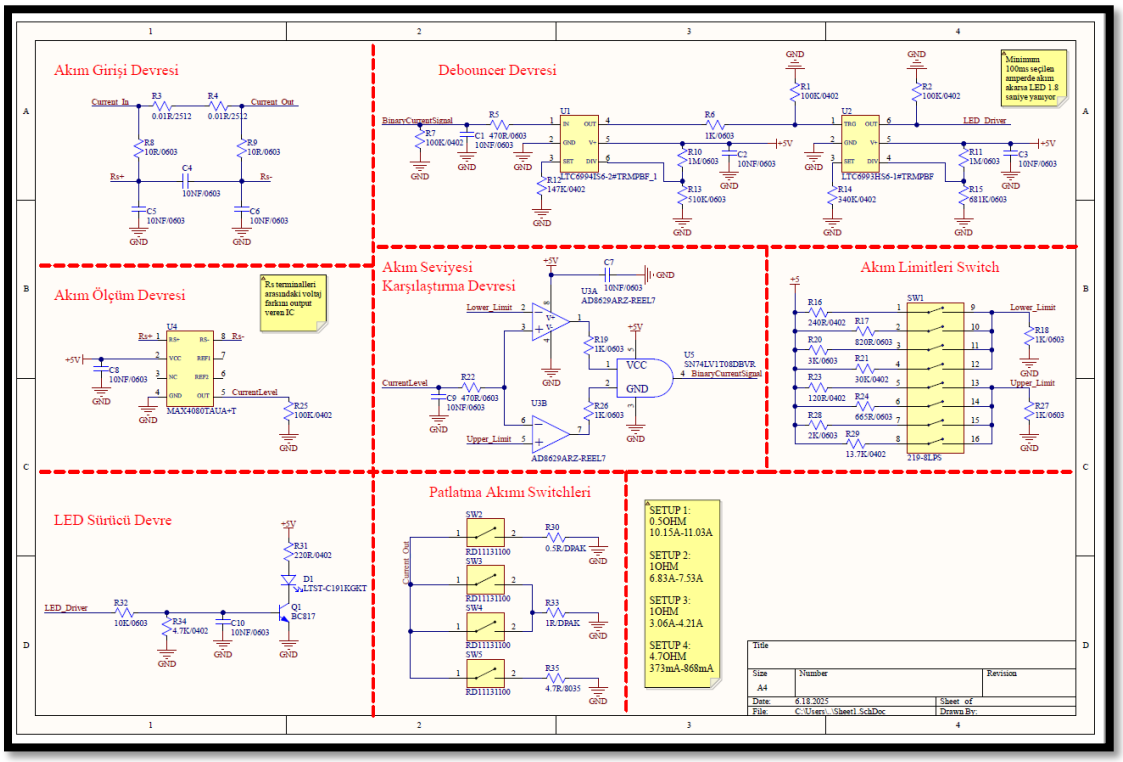


Fig. 39: The Initial Schematic of the Circuit

Appendix 2 is the .pdf file of the initial schematic of the circuit including the exact component IDs and a BOM.

After successfully creating a schematic document, I now turned my attention into creating a PCB footprint library. I used DigiKey, SnapMagic and UltraLibrarian to obtain 3D .stp files of the components in my library [10, 11, 12]. However, I did not use any website to obtain the footprints. I have manually created all the footprints in my library by looking at the component datasheets [10].

The following figure shows the PCB library components.

Footprints

Name	Pads	Primitives
219-8LPS	16	18
350540-1	2	4
61300211121	2	4
691307500002	4	5
AD8629ARZ_REEL7	8	10
BC817-40,215	3	5
CAP 0603	2	3
DS01-254-S-10BE	20	22
GMR100HTBFA10L0	2	3
LTC6993HS6-1#TRMPBF	6	8
LTC6994IS6-2#TRMPBF_1	6	8
LTST-C191KGKT	2	4
MAX4080TASA+T	8	10
PWR163S-25-1R00FE	3	4
PWR163S-25-R500FE	3	4
RB141C1100	2	3
RD11131100	2	5
RES0402	2	3
RES0603	2	3
RES2512	2	3
SM8035JT4R70	2	3
SN74LV1T08DBVR	5	7

Fig. 40: The PCB Library Components

The following 26 figures show the footprints and 3D views of each component in the PCB library.

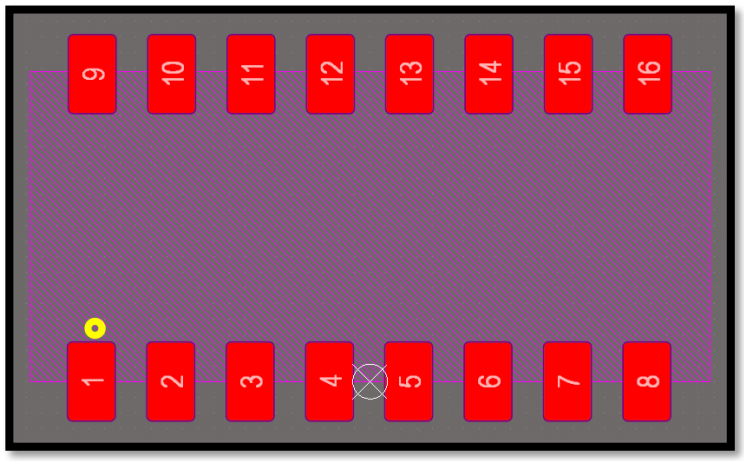


Fig. 41.1: The PCB Footprint for the DIP Switch in the Library; 219-8LPS

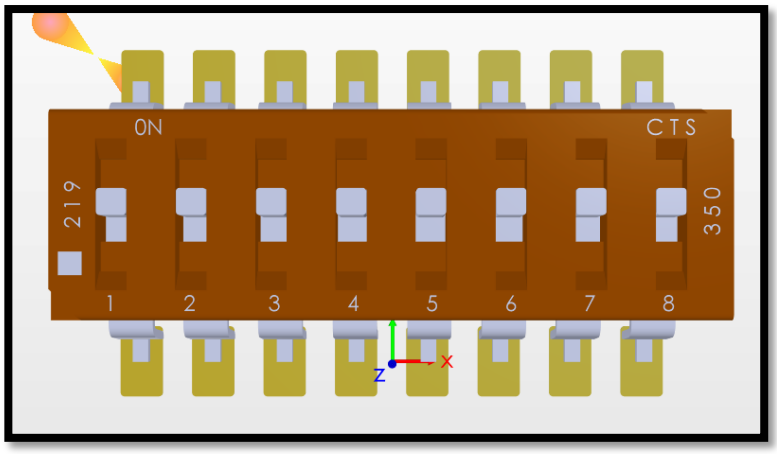


Fig. 41.2: The 3D View of the DIP Switch in the Library; 219-8LPS

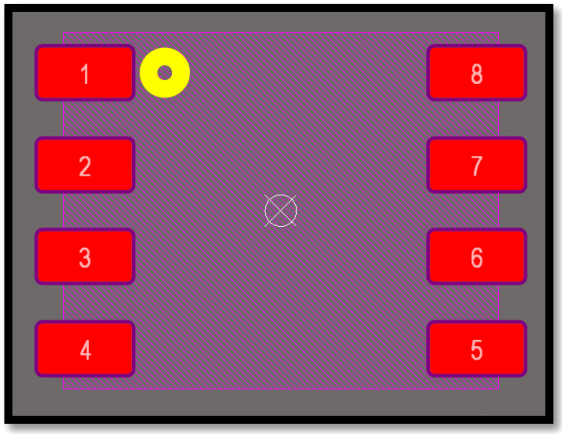


Fig. 42.1: The PCB Footprint for the Dual OPAMP; AD8629ARZ-REEL7

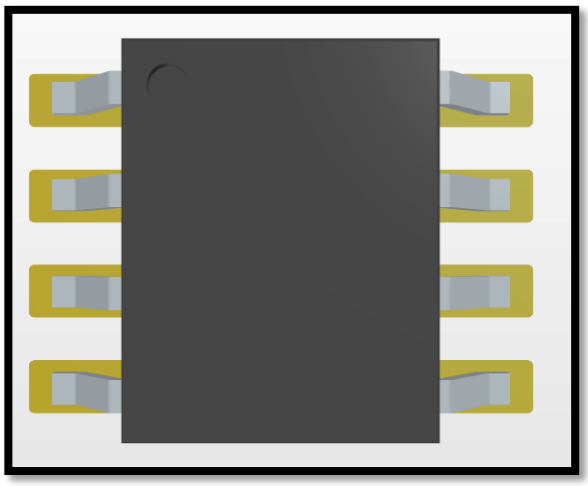


Fig. 42.2: The 3D View of the Dual OPAMP; AD8629ARZ-REEL7

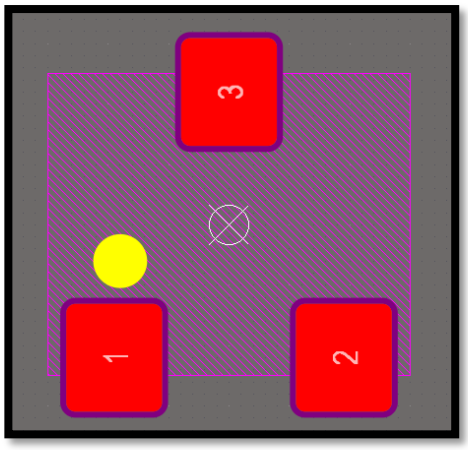


Fig. 43.1: The PCB Footprint for the NPN-BJT; BC817-40,215

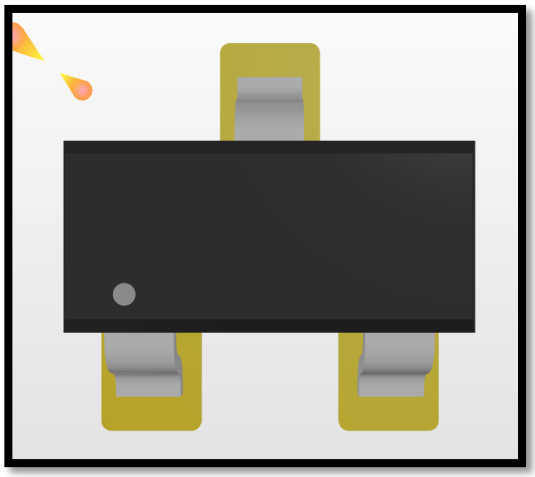


Fig. 43.2: The 3D View of the NPN-BJT; BC817-40,215

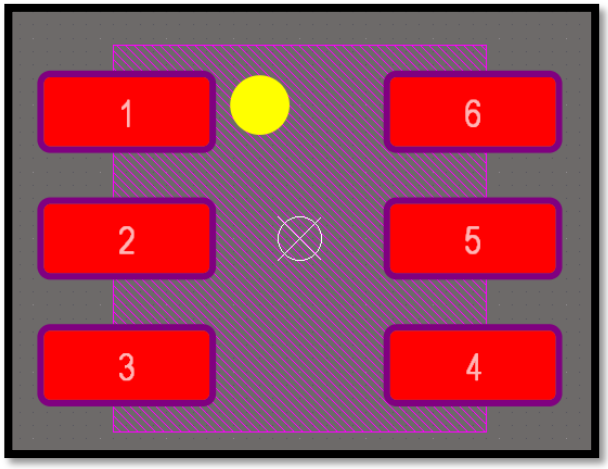


Fig. 44.1: The PCB Footprint for the LTC6993HS6-1#TRMPBF

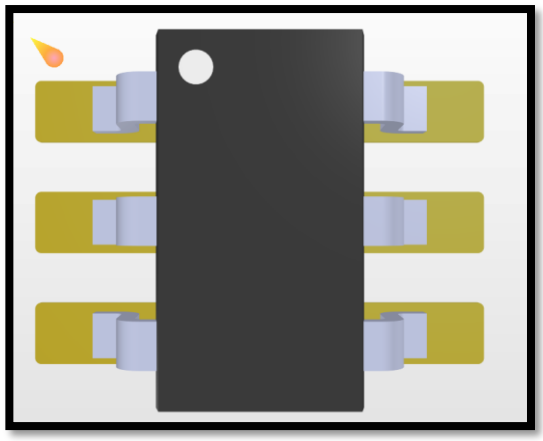


Fig. 44.2: The 3D View of the LTC6993HS6-1#TRMPBF

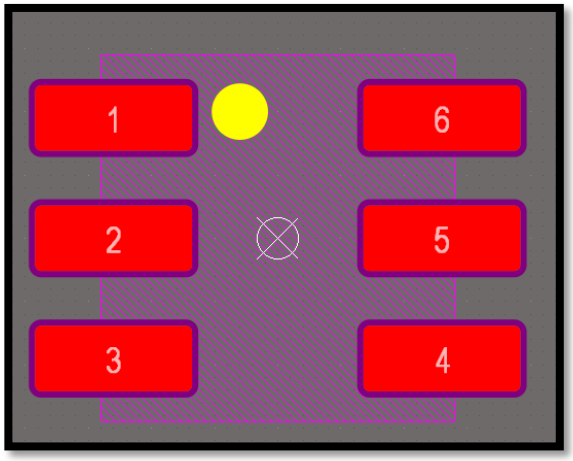


Fig. 45.1: The PCB Footprint for the LTC6994IS6-2#TRMPBF_1

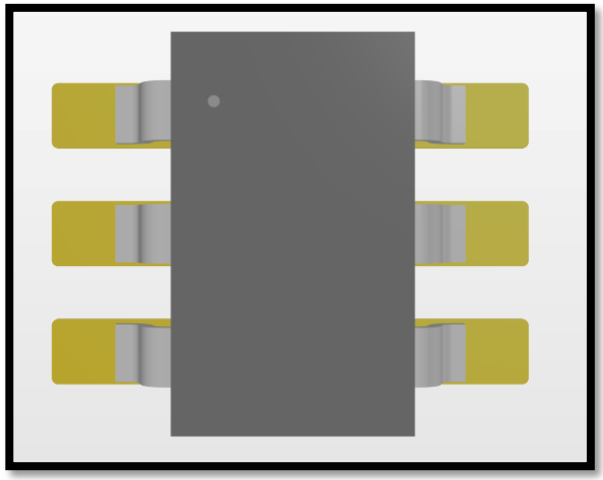


Fig. 45.2: The 3D View of the LTC6994IS6-2#TRMPBF_1

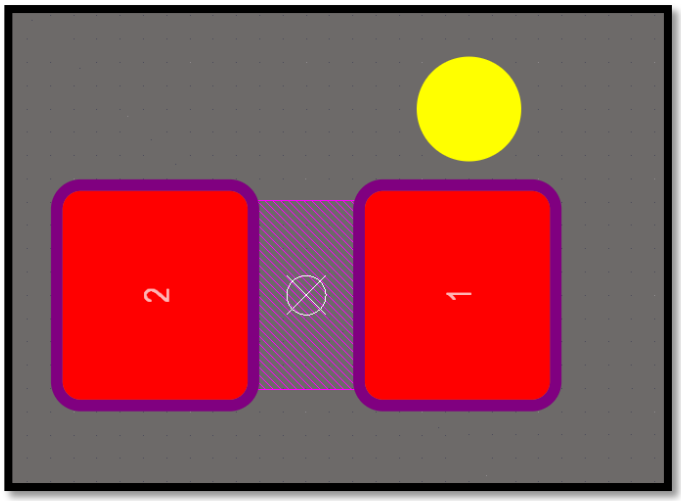


Fig. 46.1: The PCB Footprint for the Green LED; LTST-C191KGKT

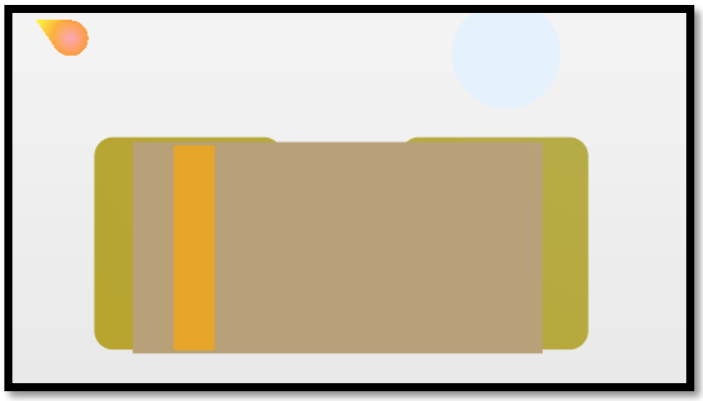


Fig. 46.2: The 3D View of the Green LED; LTST-C191KGKT

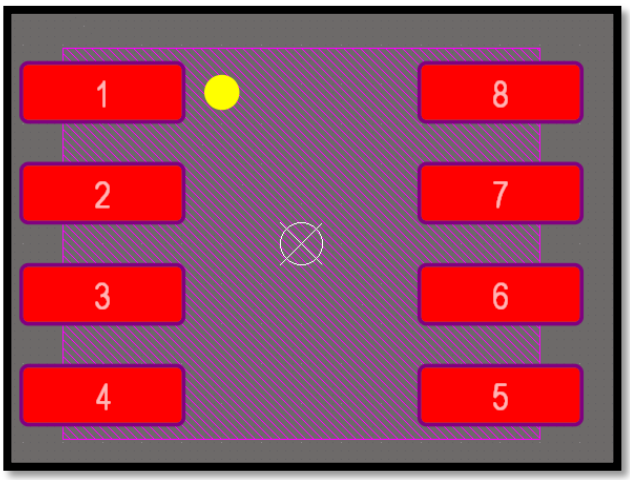


Fig. 47.1: The PCB Footprint for the MAX4080TASA+T

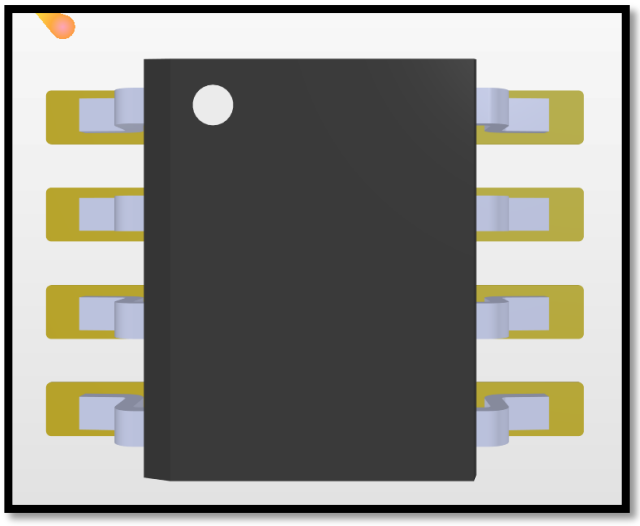


Fig. 47.2: The 3D View of the MAX4080TASA+T

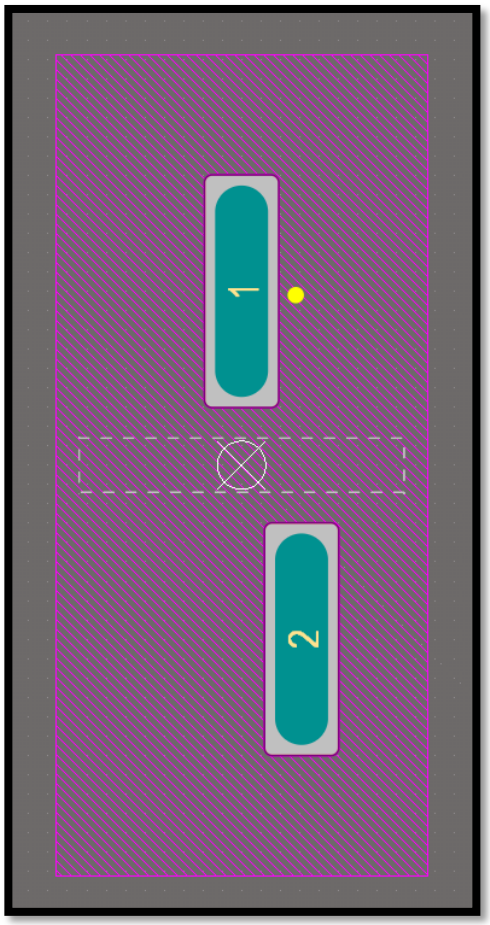


Fig. 48.1: The PCB Footprint for the Power Switch; RD11131100

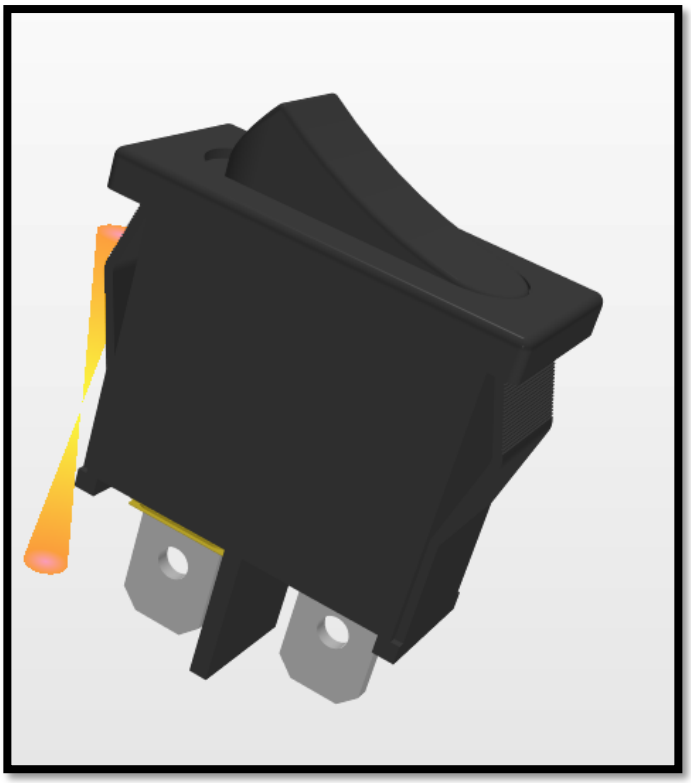


Fig. 48.2: The 3D View of the Power Switch; RD11131100

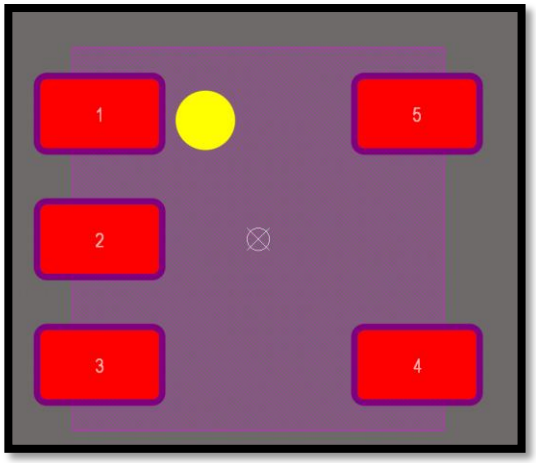


Fig. 49.1: The PCB Footprint for the One-Channel AND-Gate; SN74LV1T08DBVR

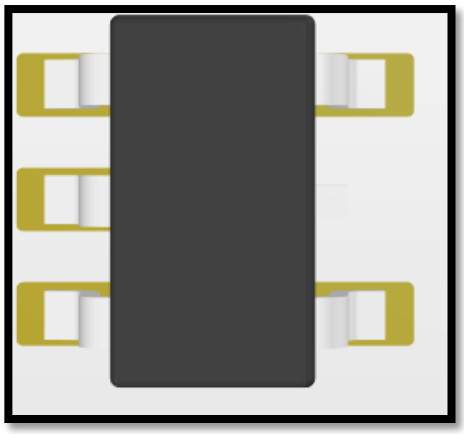


Fig. 49.2: The 3D View of the One-Channel AND-Gate; SN74LV1T08DBVR

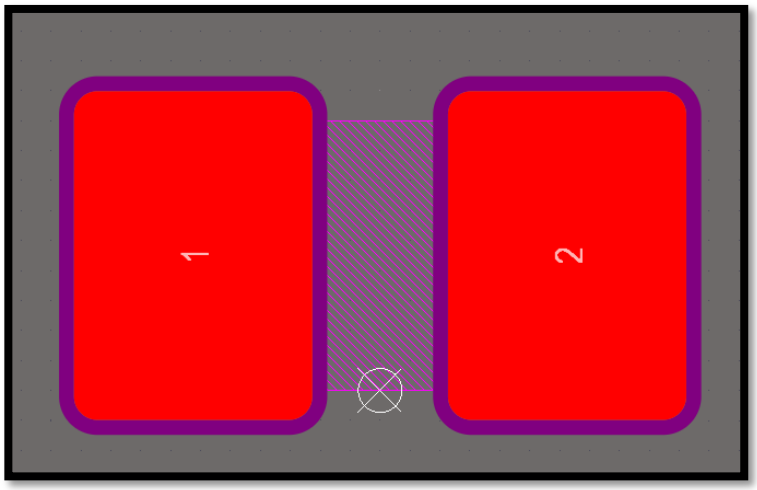


Fig. 50.1: The PCB Footprint for all the Capacitors in the Library (0603 Package)

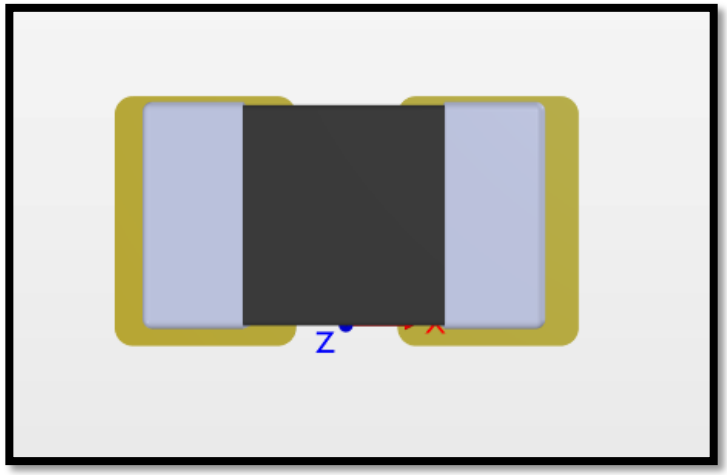


Fig. 50.2: The 3D View of all the Capacitors in the Library (0603 Package)

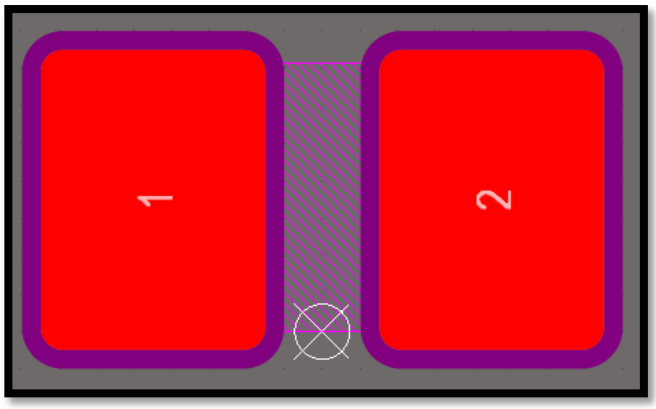


Fig. 51.1: The PCB Footprint for the 0402 Package Resistors in the Library

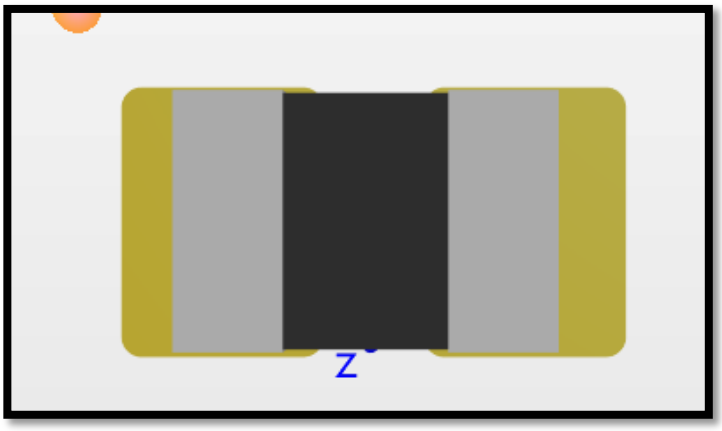


Fig. 51.2: The 3D View of the 0402 Package Resistors in the Library

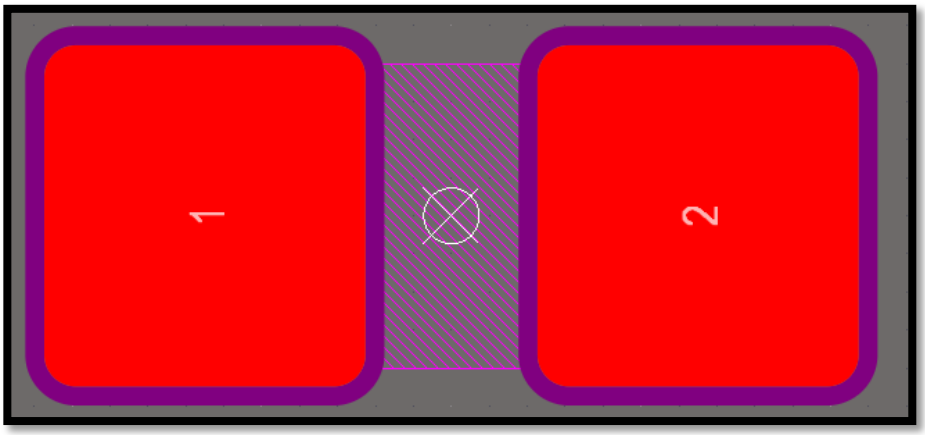


Fig. 52.1: The PCB Footprint for the 0603 Package Resistors in the Library

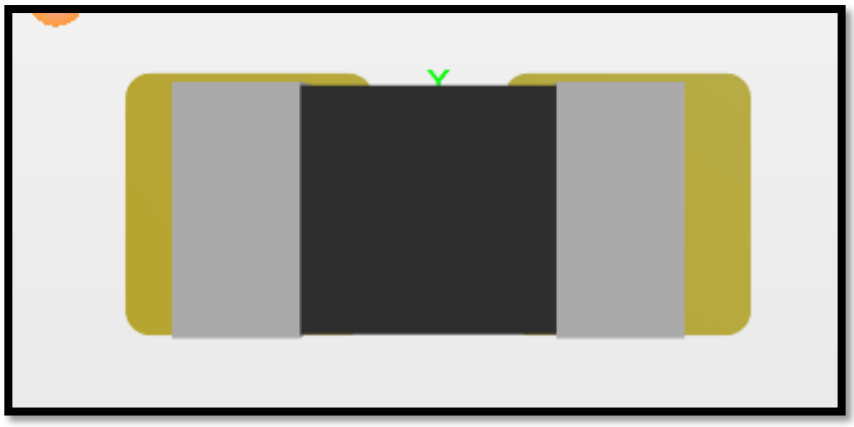


Fig. 52.2: The 3D View of the 0603 Package Resistors in the Library

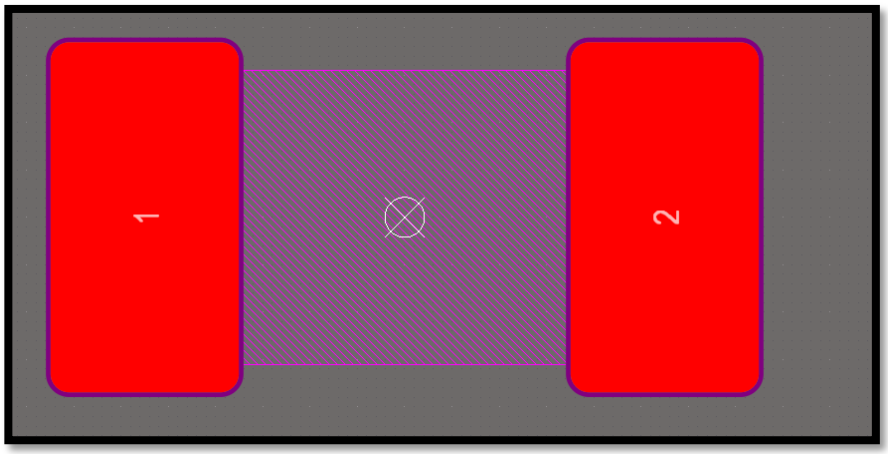


Fig. 53.1: The PCB Footprint for the 2512 Package Resistors in the Library

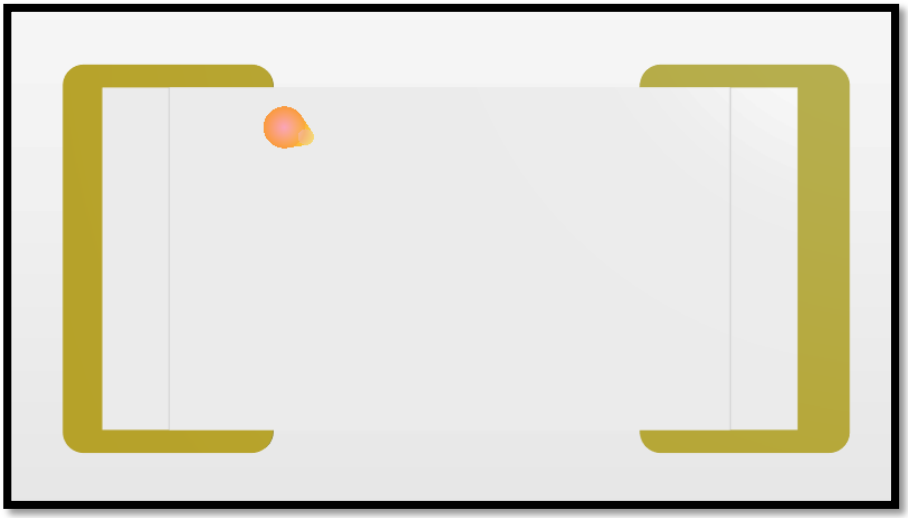


Fig. 53.2: The 3D View of the 2512 Package Resistors in the Library

These were the PCB footprints and 3D views of the components that were present in the library. **Appendix 3** is the GitHub link to my PCB library.

After creating the PCB library, it was now time to start designing the PCB. My supervisor gave me the following recommendations before I started the PCB design:

1. The high-current carrying traces should be wider than normal electronic traces. [12]
2. I should try to minimize EMI and EMC by trying to avoid designing traces with similar length and same direction. A good practice would be to try tracing horizontally on one side of the board and vertically on the other side.
3. Pouring polygons to the power nets (+5V and GND) would be a better approach than tracing each pad on power nets individually.
4. The bypass capacitors of ICs should be very close to the IC physically. It would be better if the power went through the capacitor first before arriving at the IC.
5. Don't hesitate putting via holes to the PCB. They are extremely cheap.

The following 6 figures show my initial PCB design according to the initial recommendations I got from my supervisor.

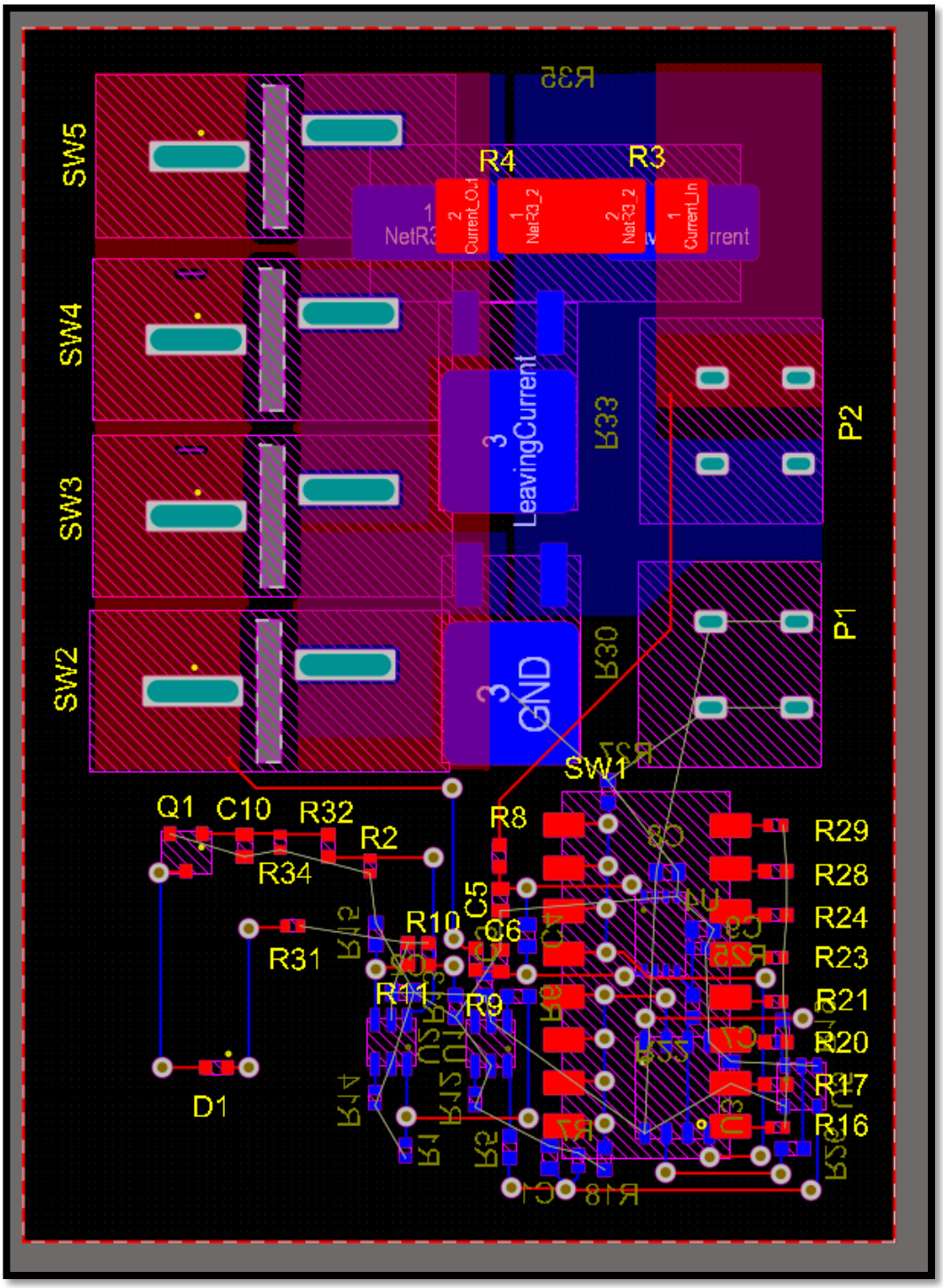


Fig. 54.1: The 2D View of the Initial PCB

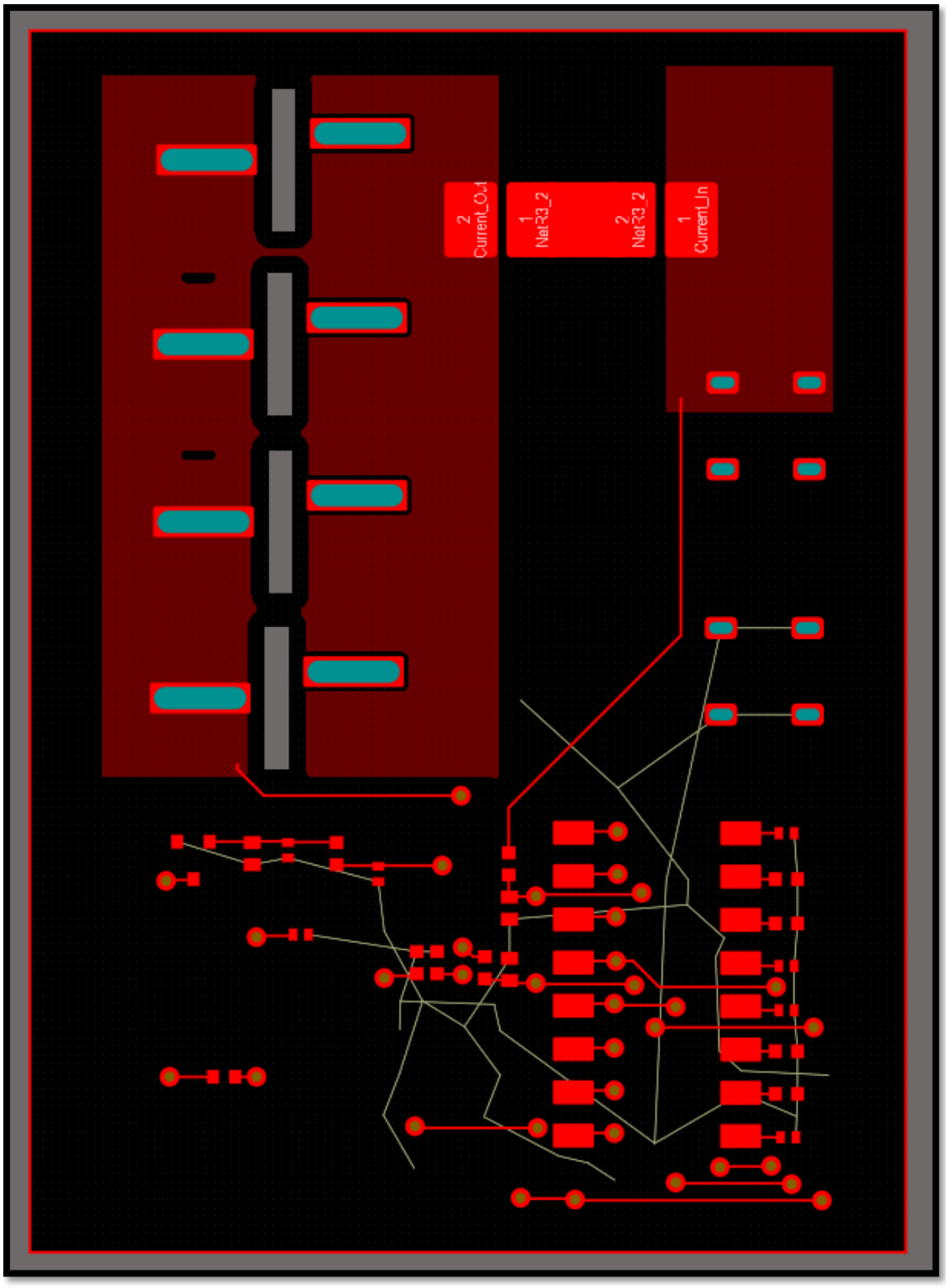


Fig. 54.2: The 2D View of the Top Layer of the Initial PCB

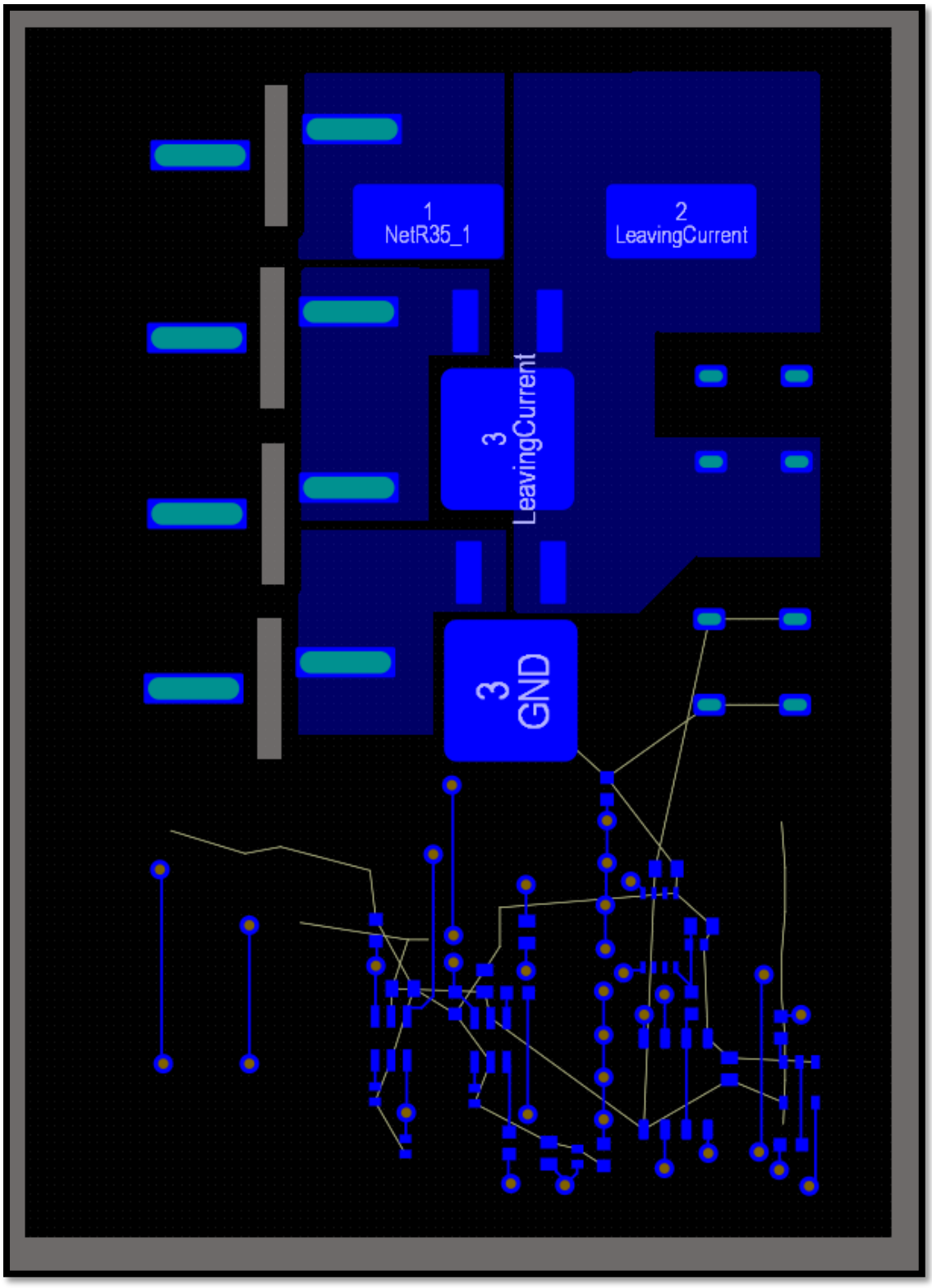


Fig. 54.3: The 2D View of the Bottom Layer of the Initial PCB

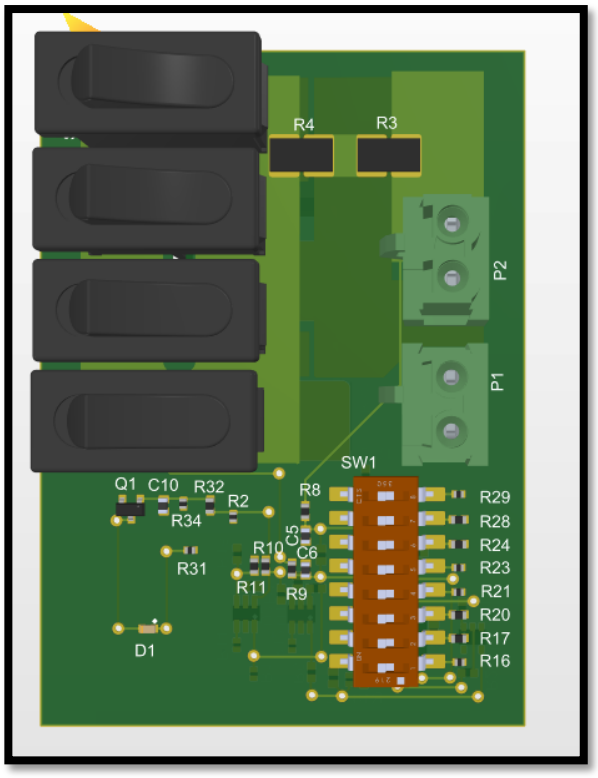


Fig. 54.4: The 3D View from the Top Side of the Initial PCB

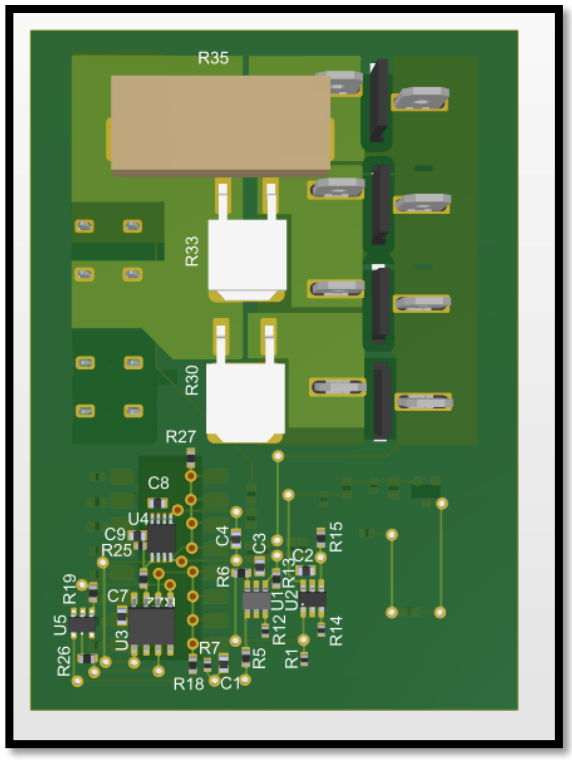


Fig. 54.5: The 3D View from the Bottom Side of the Initial PCB

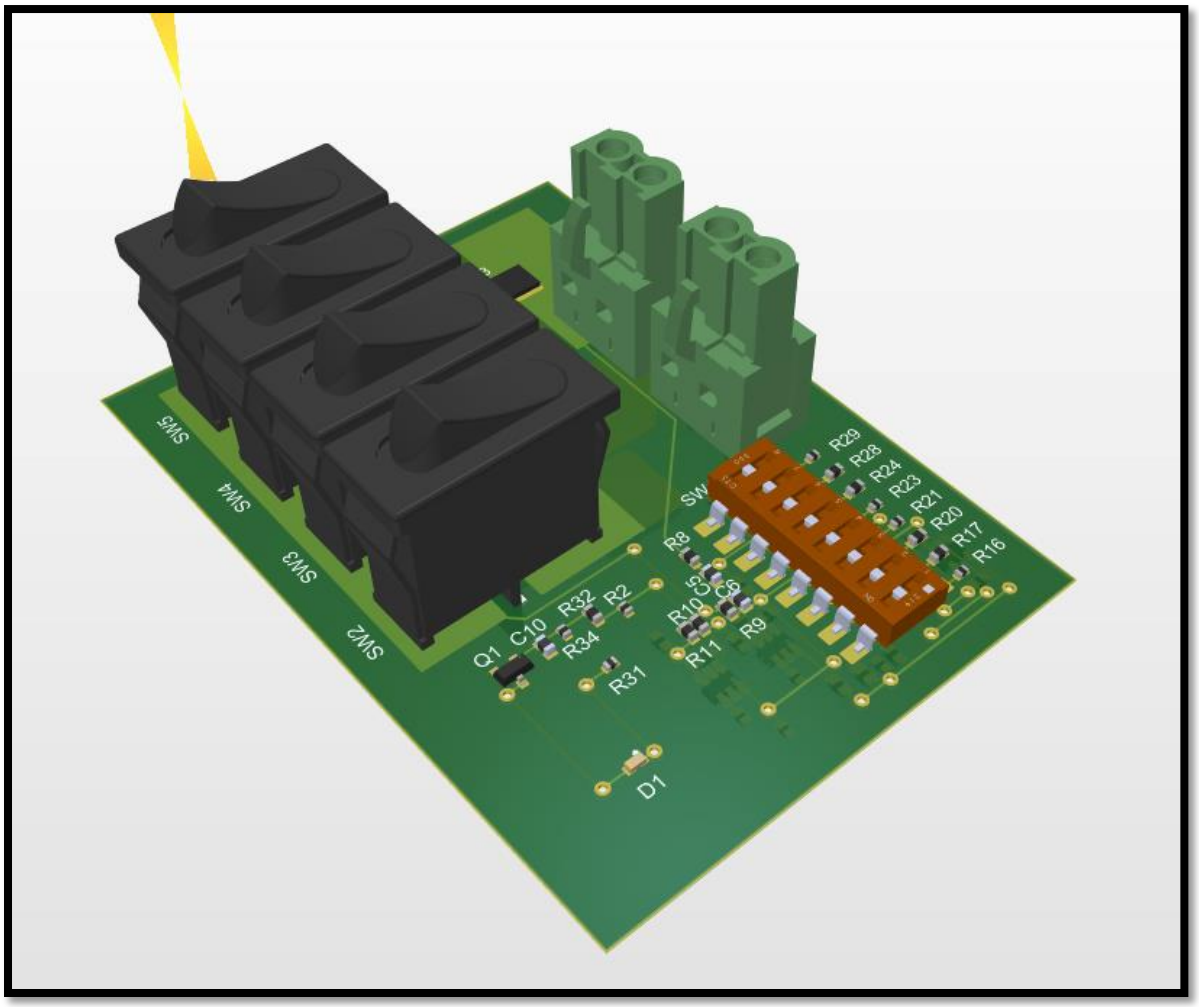


Fig. 54.6: The 3D View of the Initial PCB

Please note that I did not pour the power net polygons yet to the initial design for VCC and GND nets. This is because I showed the circuit to my supervisor to get feedback before pouring the polygons. I thought I did a successful design. However, he has found many errors in my design. He gave me the following feedback:

1. Change the 2 Current Sense 0.01Ω Resistors (R3 & R4) into a single 0.02Ω resistor. Also, the current reading traces are a sensitive differential pair, therefore they have to be same length and symmetric directions.
2. Look at the IC datasheets and change the bypass capacitor value for each IC if necessary.
3. Change all the 0402 package resistors into 0603 package.
4. Drive the LED with no more current than 10mA.
5. Add screw holes to the PCB with hole diameter of 3.5mm.
6. Increase the size of the via holes to 1mm.
7. Increase the width of the traces from 0.254mm to 0.35mm.
8. Increase all the clearance rules to 0.4mm.
9. Don’t put the same external unit connectors to the PCB twice. Choose a different connector for the pyrotechnic activation signals, choose another for the power ports.

10. Check the power rating of the power resistors present in the PCB and increase them up to 50&60W if necessary.
11. Change the MAX4080TAUA+ IC to a bigger MAX4080 package with more space between the ICs' legs.
12. Chamfer the board corners.

I then, revised the PCB by carefully considering all the points my instructor mentioned. I changed the MAX4080TAUA+ IC in the libraries to MAX4080TASA+ which had larger dimensions. I changed both the schematic and the PCB document.

The following figure shows the revised circuit schematic. Also, **Appendix 4** is the .pdf file of the finalized schematic of the circuit including the exact component IDs and a BOM.

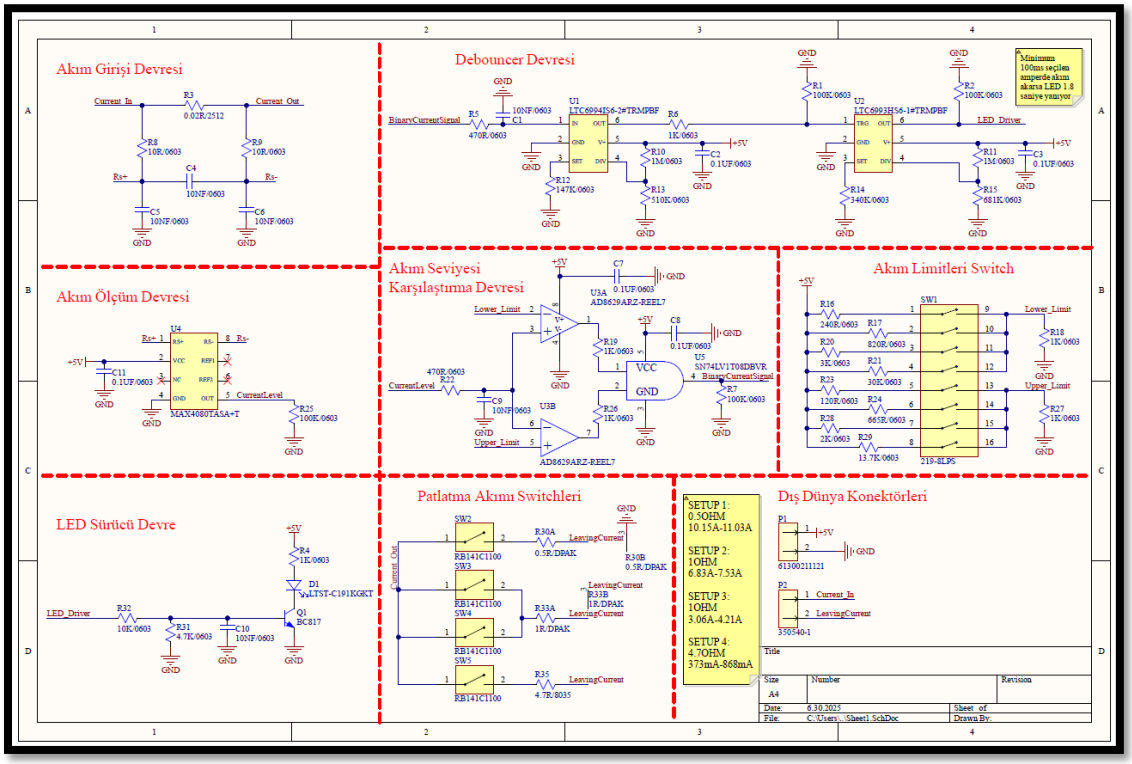


Fig. 55: The Finalized Circuit Schematic

The following 5 figures show the finalized PCB design which has dimensions of 9.2mm X 7.2mm.

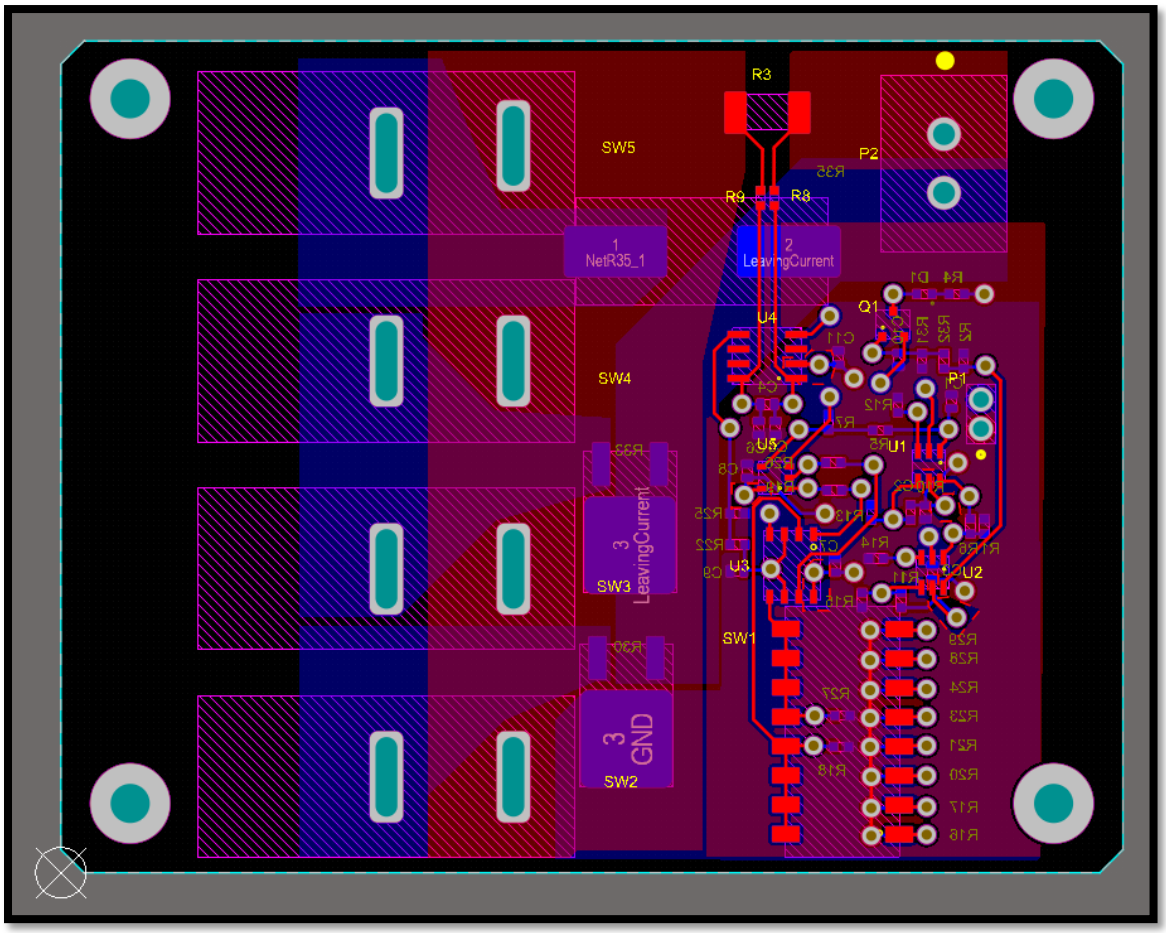


Fig. 56.1: The 2D View of the Finalized PCB

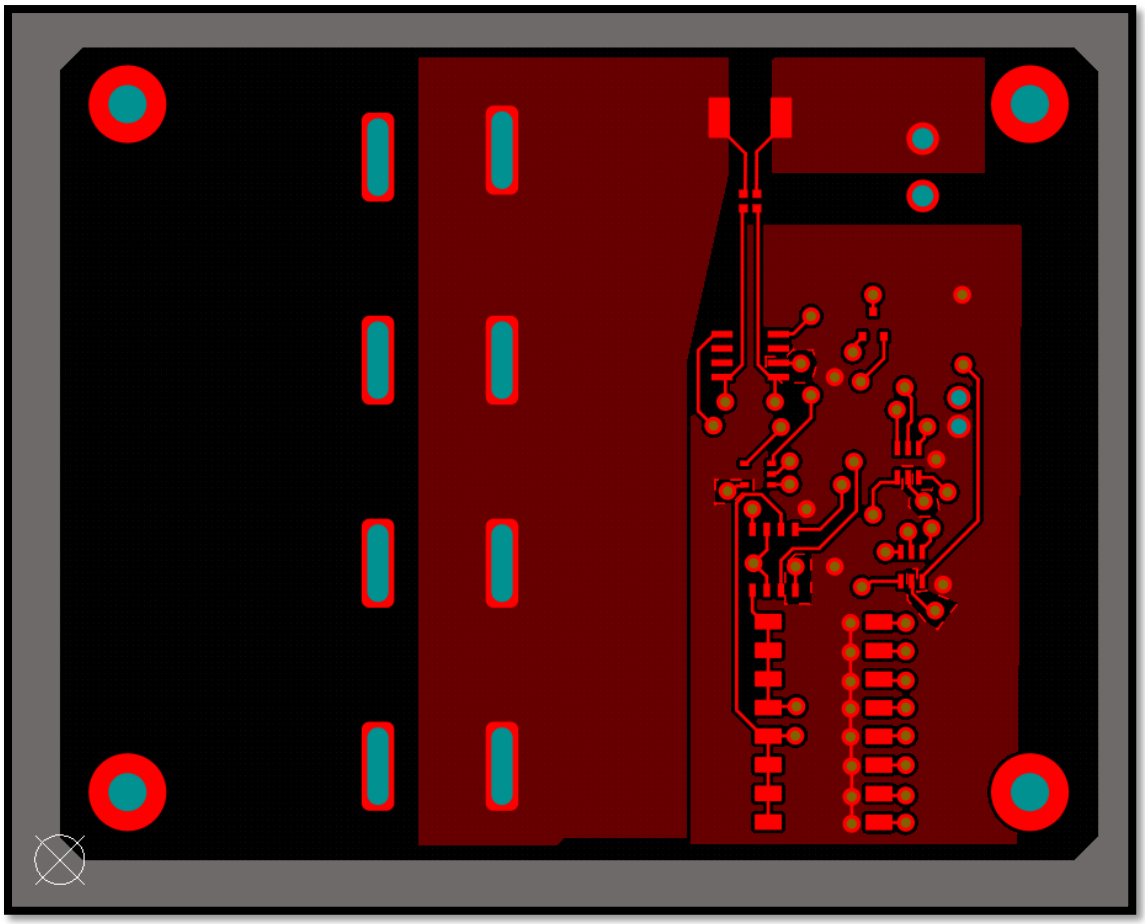


Fig. 56.2: The 2D View of the Top Layer of the Finalized PCB

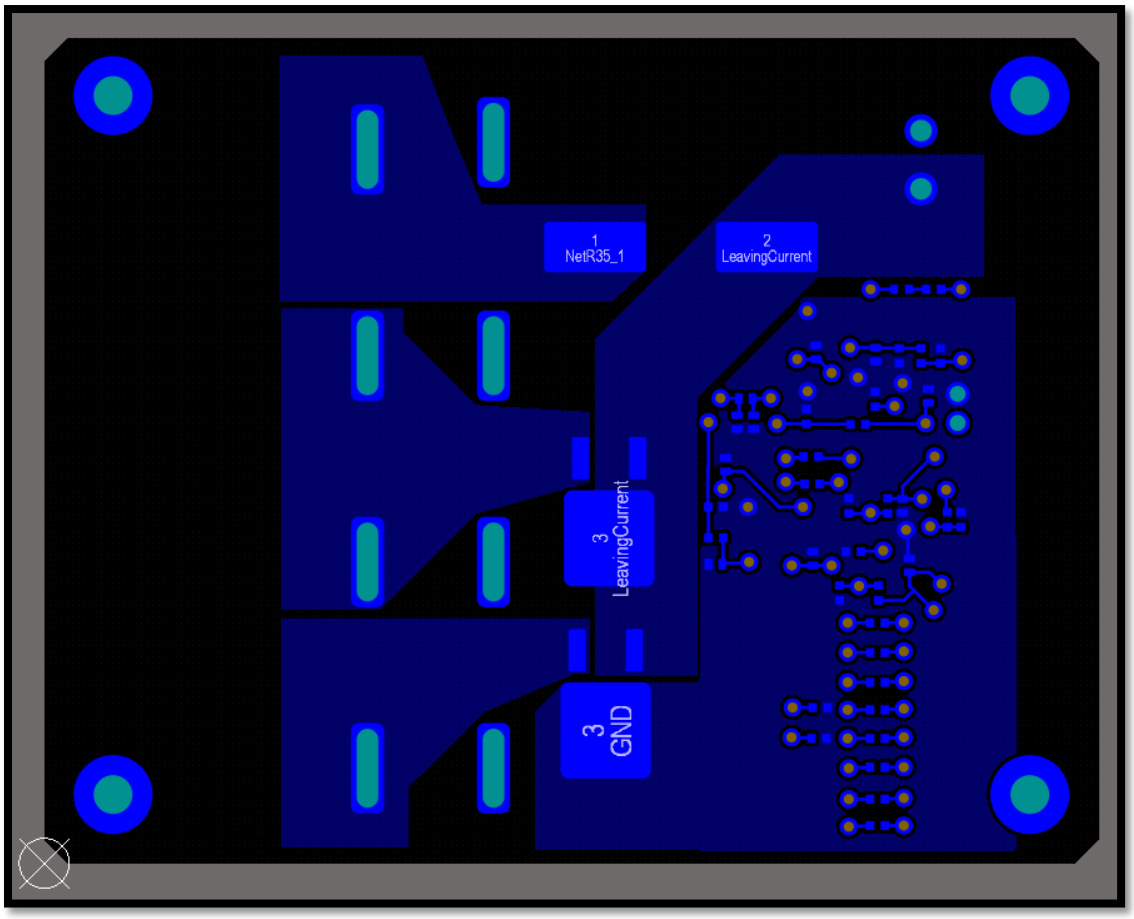


Fig. 56.3: The 2D View of the Bottom Layer of the Finalized PCB

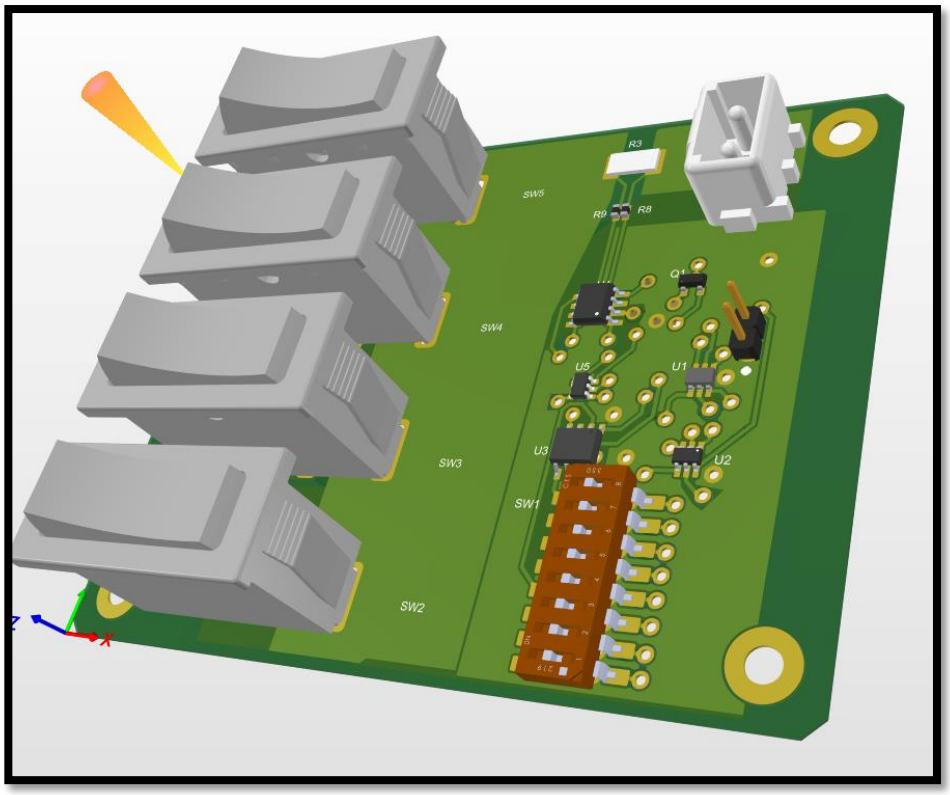


Fig. 56.4: The 3D View of the Top Layer of the Finalized PCB

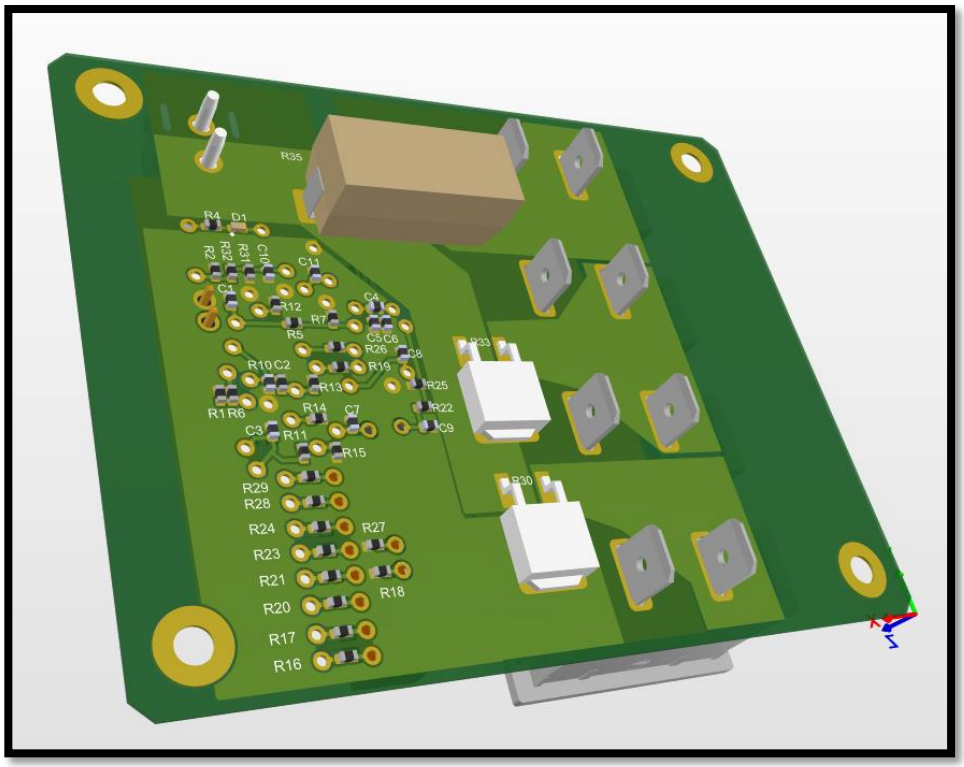


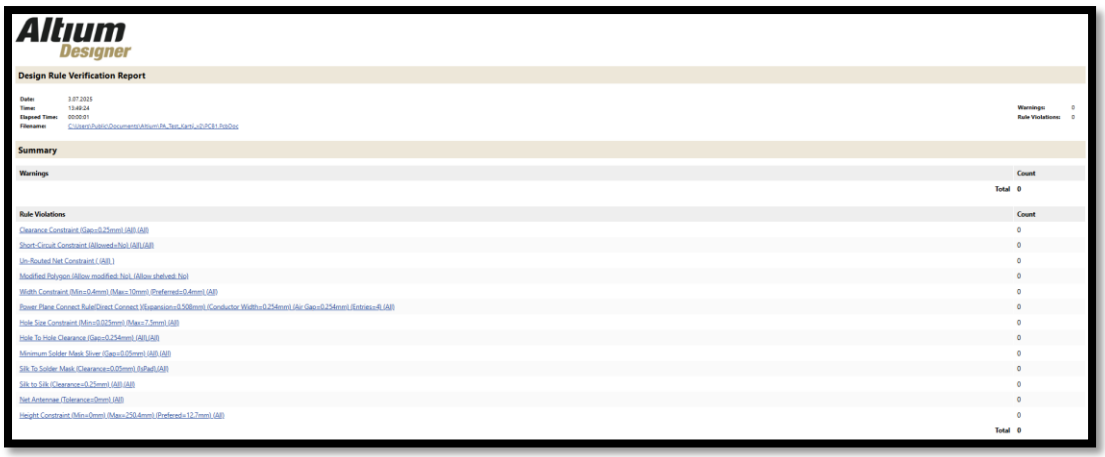
Fig. 56.5: The 3D View of the Bottom Layer of the Finalized PCB

This paragraph marks an end to the entire design process I went through. I first designed the circuit using LTSpice. Then I moved onto using Altium Designer. I created both the schematic symbols and the PCB footprint libraries manually. Then, I designed a schematic and a PCB using the components from my own library.

1.5 Verification

The previous section contains software tools and simulation results that verify whether the circuit meets the requirements or not. However, since a 20-day internship is not enough to manufacture an entire PCB from scratch, the physical verification of the project will not be included in this report.

Nevertheless, after designing the final PCB, I have run a design rule check in Altium Designer. There were no rule errors present in the final design. The following figure shows the Altium Designer log of the design rule check. I have encountered zero rule breaks.


Altium Designer

Design Rule Verification Report

Date: 3.07.2025
Time: 13:49:24
Elapsed Time: 00:00:01
Filename: C:\Users\Public\Documents\Altium\PA_Test_Kartı_v2\PCB1.PcbDoc

Warnings: 0
Rule Violations: 0

Summary

Warnings	Count
Total	0

Rule Violations	Count
Clearance Constraint (Gap=0.25mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.4mm) (Max=10mm) (Preferred=0.4mm) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm) (Entries=4) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=7.5mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.05mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.05mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.25mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=250.4mm) (Prefered=12.7mm) (All)	0
Total	0

Fig. 57: The Altium Designer Design Rule Verification Report

1.6 Cost Analysis

The engineer that creates the most technically accurate design is not the best engineer. The best engineer is the one that takes all the constraints, which can be both technical or non-technical, into account. In the industry, it is crucial to do cost analysis on our designs. Cost should be a significant driving factor when choosing components.

I have also taken cost into account when designing my project. Cost affected my component choices significantly. The following table shows the components I used as well as their quantity and market prices in DigiKey as of July 2025 [10].

Table V: Cost Analysis of the Components

Component ID	Unit Cost (USD)	Quantity	Total Cost (USD)
CC0603KPX7R9BB103	0.01016	6	0.06096
CC0603KPX7R9BB104	0.01522	5	0.07610
LTST-C191KGKT	0.04972	1	0.04972
61300211121	0.06390	1	0.06390
350540-1	0.78728	1	0.78728
BC817-40,215	0.03741	1	0.03741
RC0603FR-07100KL	0.00510	4	0.02040
CRA2512-FZ-R020ELF	0.17077	1	0.17077
RT0603BRD131KL	0.05202	6	0.31212
RC0603JR-07470RL	0.00510	2	0.01020
RT0603BRD0710RL	0.06566	2	0.13132

ERJ-3EKF1004V	0.00995	2	0.01990
RC0603FR-07147KL	0.00200	1	0.00200
RC0603FR-07510KL	0.00200	1	0.00200
RC0603FR-07340KL	0.00569	1	0.00569
RMCF0603FT681K	0.00480	1	0.00480
RC0603FR-07240RL	0.00510	1	0.00510
RC0603FR-07820RL	0.00612	1	0.00612
ERJ-PA3J302V	0.02950	1	0.02950
RC0603FR-1330KL	0.00765	1	0.00765
ERA-3AEB121V	0.04438	1	0.04438
RC0603FR-07665RL	0.00510	1	0.00510
ERA-3AEB202V	0.04226	1	0.04226
RMCF0603FT13K7	0.00480	1	0.00480
PWR163S-25-R500FE	1.83904	1	1.83904

RC0603JR-074K7L	0.00510	1	0.00510
RT0603BRD0710KL	0.04896	1	0.04896
PWR163S-25-1R00FE	1.83934	1	1.83934
SM8035JT4R70	0.64534	1	0.64534
219-8LPS	0.71094	1	0.71094
RB141C1100	0.55377	4	2.21508
LTC6994IS6-2#TRMPBF	2.67508	1	2.67508
LTC6993HS6-1#TRMPBF	2.98750	1	2.98750
AD8629ARZ-REEL7	2.80000	1	2.80000
MAX4080TASA+T	2.14029	1	2.14029
SN74LV1T08DBVR	0.07958	1	0.07958

The total component cost is 19.88573$ (USD) for the PCB.

However, there are also the PCB manufacturing and shipping costs as well. I used a Chinese PCB manufacturing website to calculate the manufacturing cost of my PCB [13]. I calculated the cost of my PCB with the specific parameters as hole size, track width, number of layers, PCB width & length etc. 10 units of my PCB costed 65.6$

(USD) including the shipping to Turkey. This meant a single unit of my PCB costs 6.56$ to manufacture and cargo. 4.36$ is for the manufacturing, 2.20$ is for the shipping of the PCB.

The typesetting of the components of simple PCB projects as mine are done at ROKETSAN. Therefore, there aren't any additional costs for the typesetting of the PCB. The following table shows the cost analysis for a single PCB unit.

Table VI: Cost Analysis of a Single PCB Unit (USD)

Component Cost	Manufacturing Cost	Shipping Cost	**Total Cost**
19.89$	4.36$	2.20$	**26.45$**

This paragraph marks an end to the work I did in my internship. I believe this project really contributed to my LTSpice and Altium Designer skills as well as my theoretical information on power and electronic circuit design. I also spent many hours reading datasheets. I got used to using Digikey's website to search for components and categorizing the components in the market according to the circuit's needs [10].

References

[3] Siouris, G.M. “Missile Guidance and Control Systems”. https://ftp.idu.ac.id/wp-content/uploads/ebook/tdg/MILITARY%20PLATFORM%20DESIGN/Missile%20Guidance%20And%20Control%20Systems.pdf . [Accessed: Jul 12, 2025].

[4] “Applications Catalog of Pyrotechnically Actuated Devices&Systems”. https://web.archive.org/web/20220822092153/https://ntrs.nasa.gov/api/citations/19950011972/downloads/19950011972.pdf . [Accessed: Jul 12, 2025].

[5] “Standard Series Values in a Decade for Resistances and Capacitances”. https://www.vishay.com/docs/28372/e-series.pdf . [Accessed: Jul 12, 2025].

[6] “LTC6993HS6-1#TRMPBF”, DigiKey. https://www.digikey.com/en/products/detail/analog-devices-inc/LTC6993HS6-1-TRMPBF/2399198 . [Accessed: Jul 12, 2025].

[7] “LTC6994IS6-2#TRMPBF”, DigiKey. https://www.digikey.com/en/products/detail/analog-devices-inc/ltc6994is6-2-trmpbf/2399244 . [Accessed: Jul 12, 2025].

[8] “MAX4080TAUA+T”, DigiKey. https://www.digikey.com/en/products/detail/analog-devices-inc-maxim-integrated/max4080taua-t/1703901 . [Accessed: Jul 12, 2025].

[9] “MAX4080”, Analog Devices. https://www.analog.com/en/products/max4080.html . [Accessed: Jul 12, 2025].

[10] “DigiKey”. https://www.digikey.com/ . [Accessed: Jul 12, 2025].

[11] “SnapMagic”. https://www.snapeda.com/ . [Accessed: Jul 12, 2025].

[12] “UltraLibrarian”. https://www.ultralibrarian.com/ . [Accessed: Jul 12, 2025].

[13] “PCB Prototype the Easy Way”. https://www.pcbway.com/orderonline.aspx . [Accessed: Jul 12, 2025].

[14] Peterson, Z. “PCB Trace Width vs. Current Table for High Power Designs”. https://resources.altium.com/p/pcb-trace-width-vs-current-table-high-voltage-design . [Accessed: Jul 12, 2025].

Appendices

1. https://github.com/fmcetin7/Roketsan-Internship/blob/main/PA_Test_Kart%C4%B1_v2.SchLib
2. https://github.com/fmcetin7/Roketsan-Internship/blob/main/Schematic_v1.pdf
3. https://github.com/fmcetin7/Roketsan-Internship/blob/main/PA_Test_Kart%C4%B1_v2.PcbLib
4. https://github.com/fmcetin7/Roketsan-Internship/blob/main/Schematic_v2.pdf