AHSANULLAH UNIVERSITY OF SCIENCE & TECHNOLOGY

ASSIGNMENT SUBMISSION

Course No: EEE 4293

Course Name: Computer Architecture

Topic: 8 bit modified SAP design.

Submitted By:

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Department: EEE

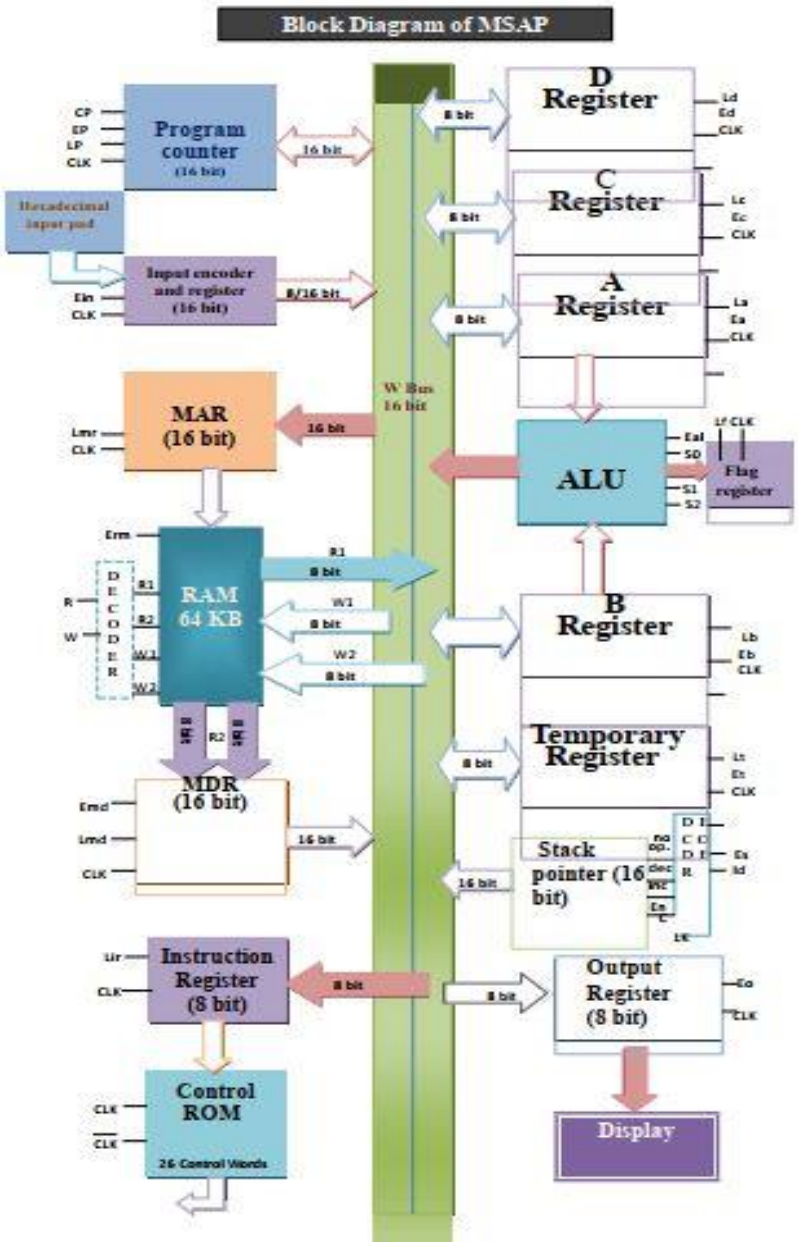
4TH Year 2nd Semester

Section : A

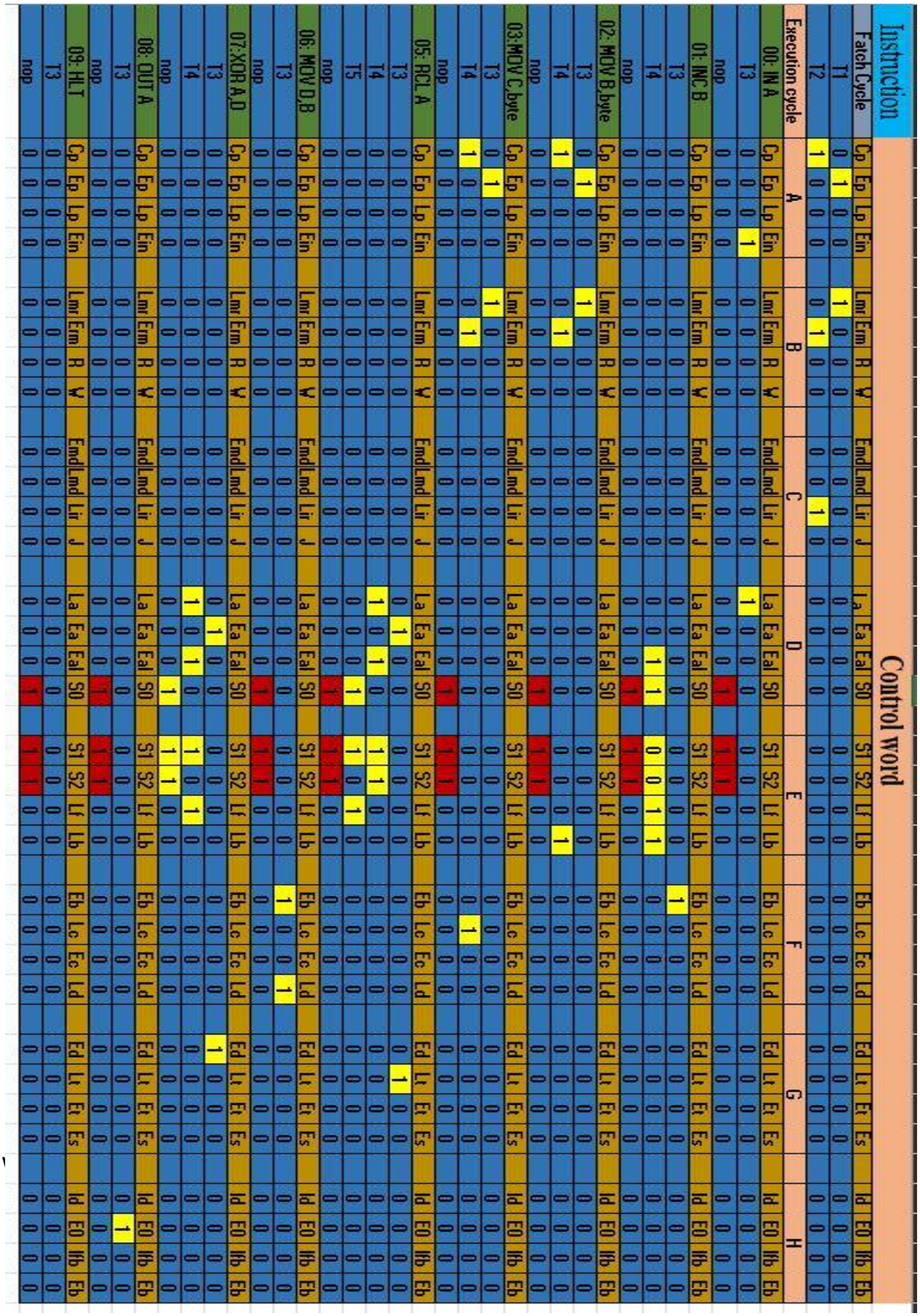
Introduction:

The objective of this assignment is to design an 8-bit Microinstruction Sequencer and to generate a control word for executing specific instructions. We executed the generated control word for the given instructions in ISIS software.

Block Diagram of MSAP:



CONTROL WORD DESIGN IN BINARY FORMAT:



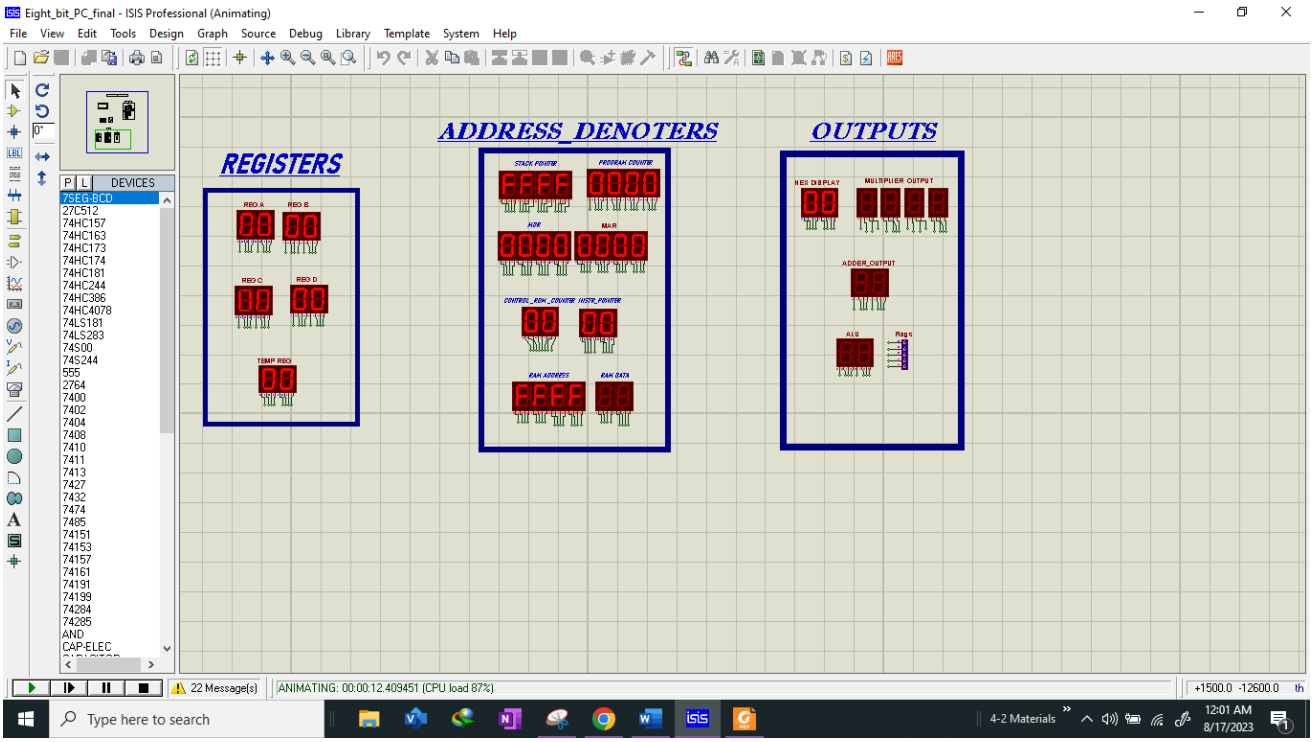
We design our control word according to our instructions set by enabling the associated pins of different block of MSAP.Then we convert it to hexadecimal file as its ROM can store only 8bit data .so we covert 32bit data to 8 bit hexadecimal file to load the RoM.Here Four ROM is connected serially .We convert the hexadecimal file to BIN file or MACHINE file to input to the ROM block by MATLAB.

A	B	C	D	E	F	G	H	I	J	K	L	M
4	8	0	0	0	0	0	0	Fatch	0	2		
8	4	2	0	0	0	0	0		0	4		
1	0	0	0	1	0	0	0	IN A	0	7		
0	0		0	1	12	0	0		0	10		
0	0	0	0	0	8	0	0	INC B	0	13		
0	0	0	5	0	0	0	0		1	1		
0	0	0	1	12	0	0	0		1	5		
4	8	0	0	0	0	0	0	MOV B,b	1	8		
8	4	0	0	0	1	0	0		1	10		
0	0	0	1	12	0	0	0					
4	8	0	0	0	0	0	0	MOV C,byte				
8	4	0	0	0	4	0	0					
0	0	0	1	12	0	0	0					
0	0	0	4	0	0	4	0	RCL A				
0	0	0	8	12	0	0	0					
0	0	0	1	10	0	0	0					
0	0	0	1	12	0	0	0					
0	0	0	0	0	8	4	0	MOV D,B				
0	0	0	0	0	1	2	0					
0	8	0	0	0	0	8	0					
0	0	0	1	12	0	0	0					
0	0	0	4	0	8	0	0	XOR A,B				
0	0	0	2	8	0	0	0					
0	0	0	1	12	0	0	0					
0	0	0	0	0	0	0	4	OUT A				
0	0	0	1	12	0	0	0					
0	0	0	0	0	0	0	0	HLT				
0	0	0	1	12	0	0	0					

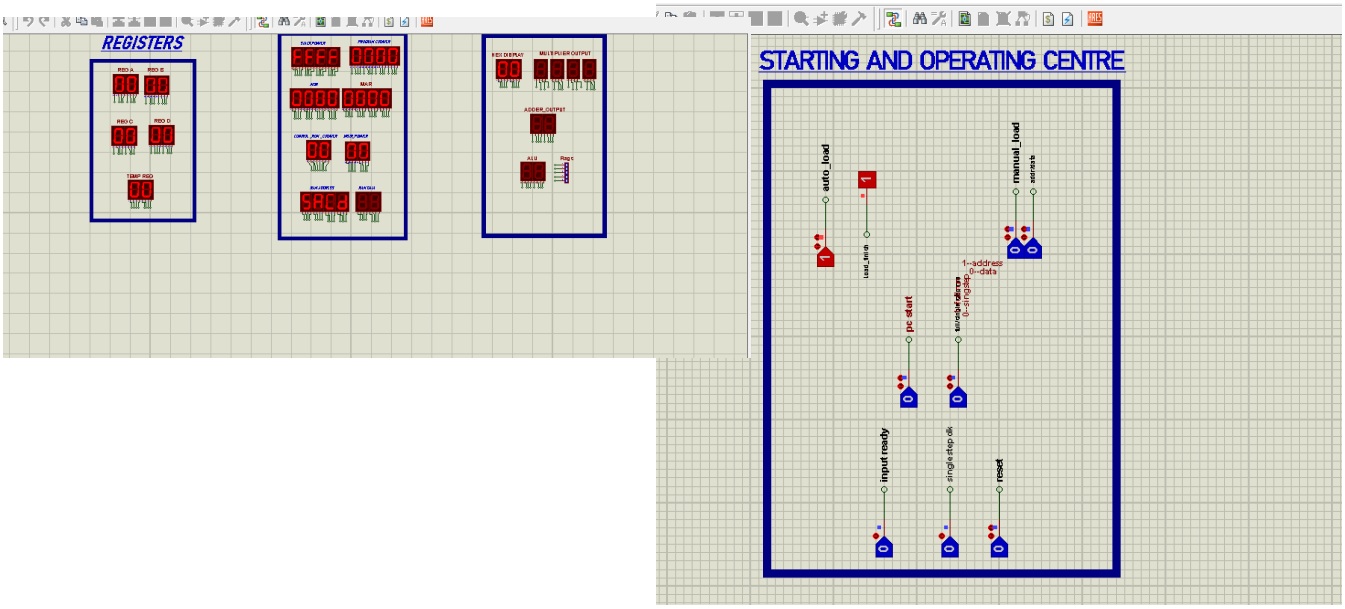
FIGURE: 8bit Hexadecimal control word.

WORKING PROCEDURE:

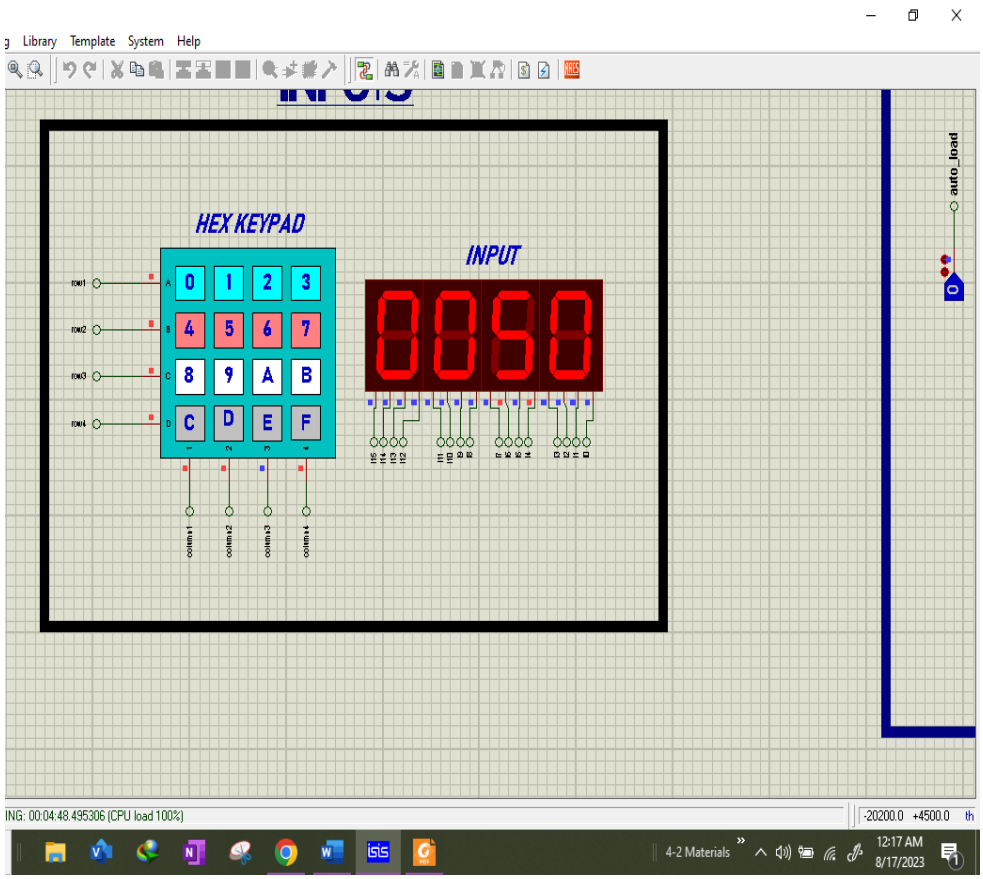
1.Resetting the memory block.



2. Ram data load.

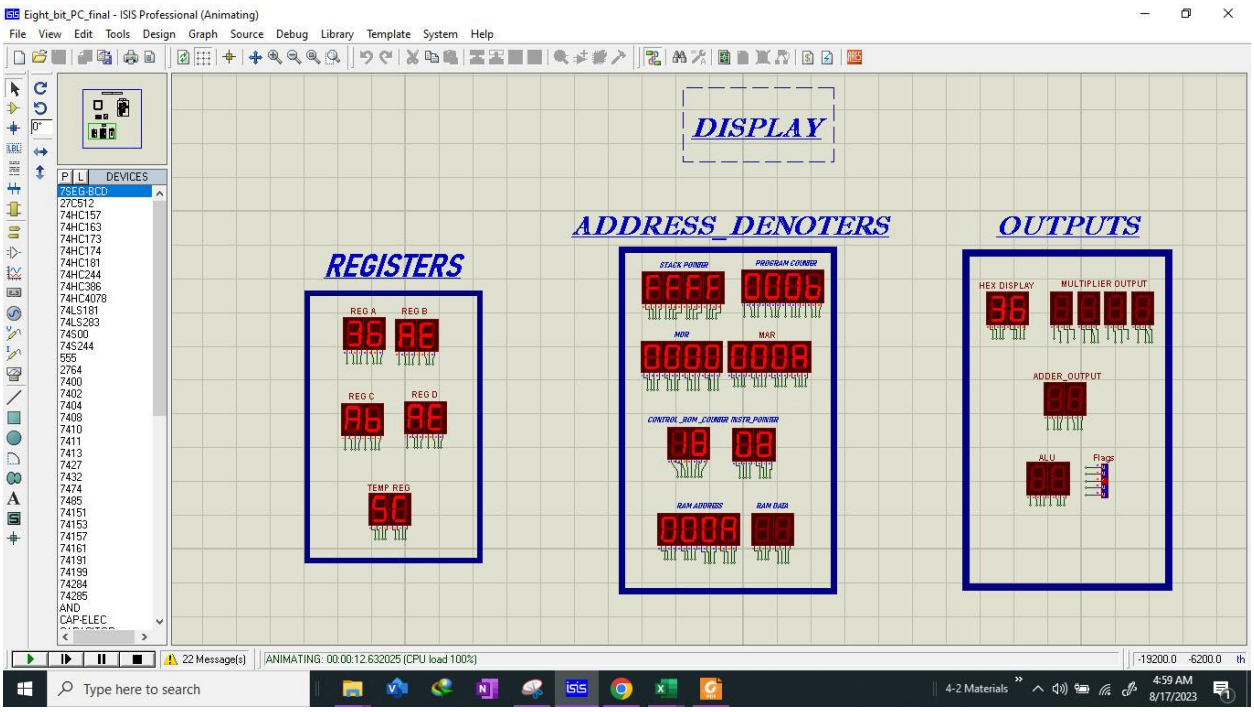


3.loading input from Keyboard.

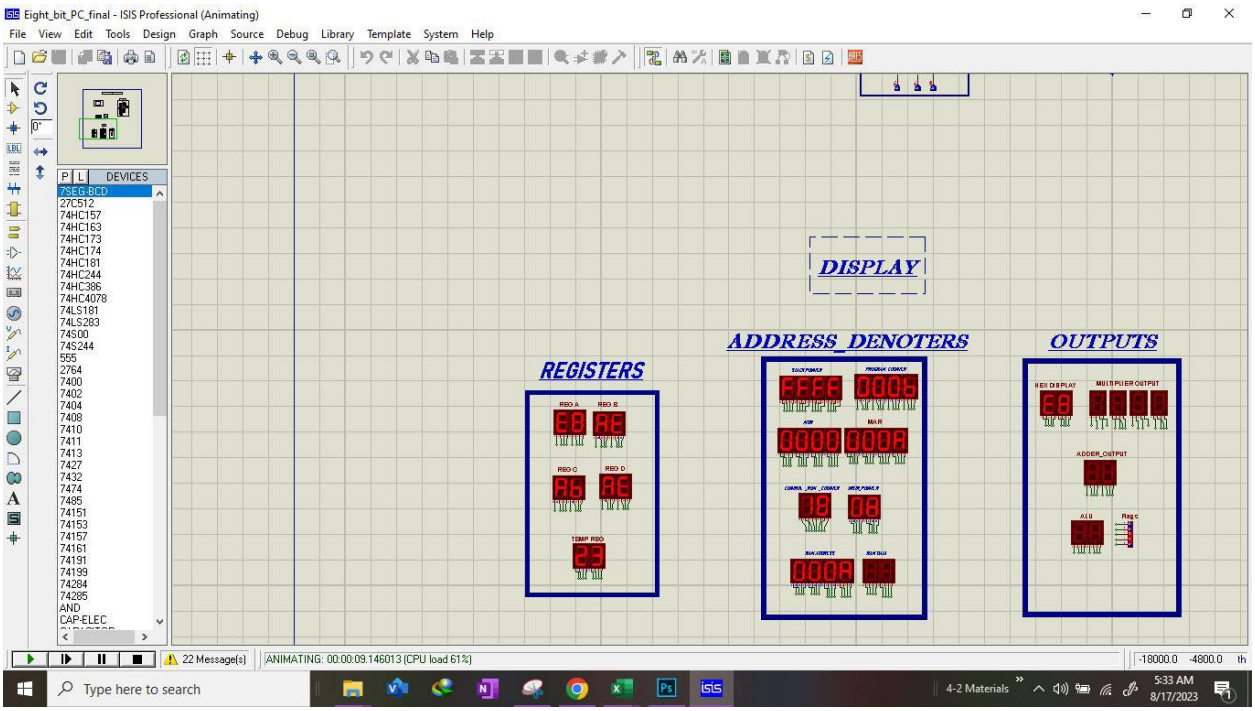


6. Then pushing the ready pin ,the input taking is done.

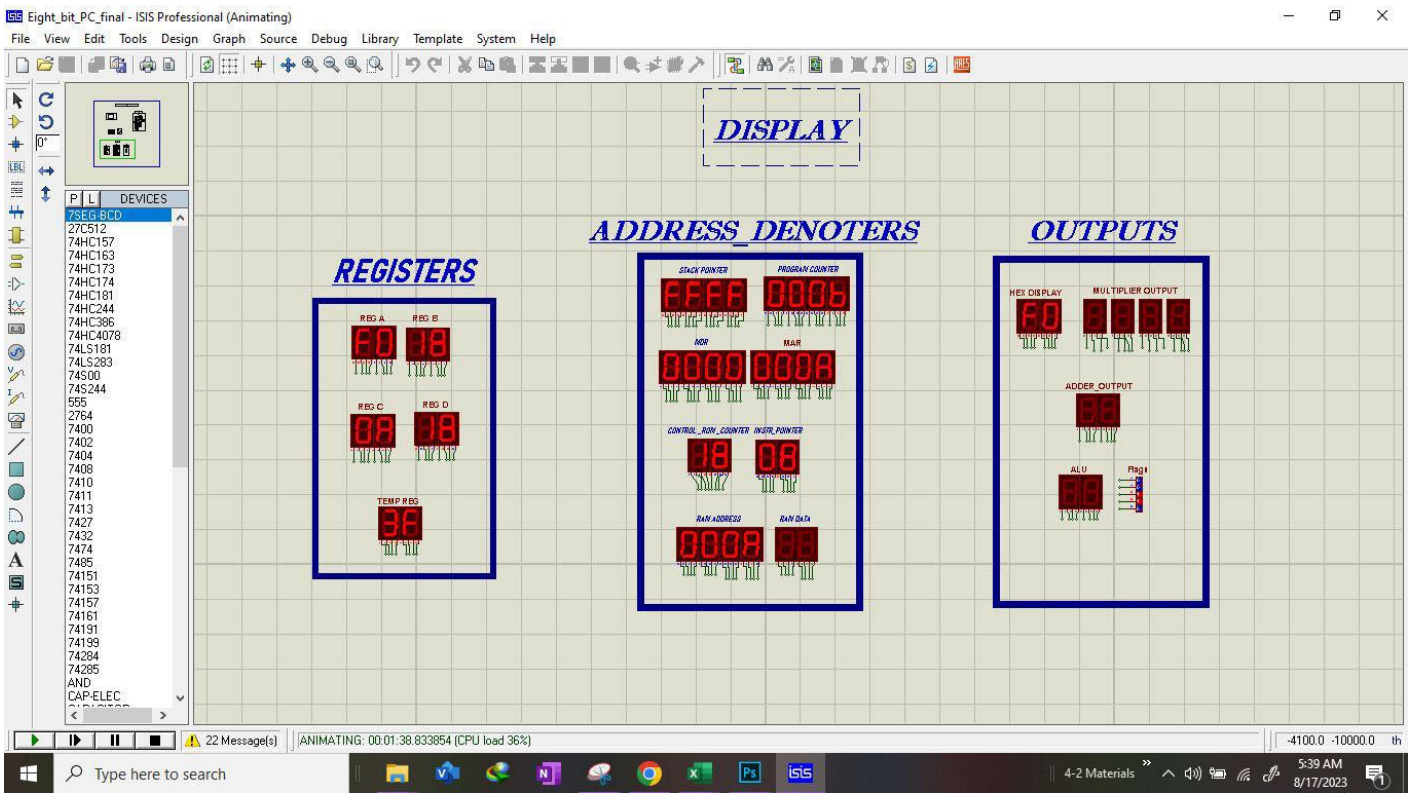
OUTPUT :



OPCODE	INSTRUCTION	A	B	C	D
00	IN A	13	00	00	00
01	INC B	00	01	00	00
02	MOV B,byte	00	AE	00	00
03	MOV C,byte	00	AE	A6	00
04	RCL A	14	AE	A6	00
05	MOV D,B	14	AE	A6	AE
06	XOR A,B	36	AE	A6	AE
07	OUT A	36	AE	A6	AE



OPCODE	INSTRUCTION	A	B	C	D
00	IN A	23	00	00	00
01	INC B	00	01	00	00
02	MOV B,byte	00	AE	00	00
03	MOV C,byte	00	AE	A6	00
04	RCL A	2E	AE	A6	00
05	MOV D,B	2E	AE	A6	AE
06	XOR A,B	E8	AE	A6	AE
07	OUT A	E8	AE	A6	AE



OPCODE	INSTRUCTION	A	B	C	D
00	IN A	3F	00	00	00
01	INC B	3F	01	00	00
02	MOV B,byte	3F	18	00	00
03	MOV C,byte	3F	18	0A	00
04	RCL A	7E	18	0A	00
05	MOV D,B	7E	18	0A	18
06	XOR A,B	F0	18	0A	18
07	OUT A	F0	18	0A	18