

Project Name: Analysis of 8T, 10T and 14T 1-bit full adders in comparison.

Course No: **EEE 4134**

Course Title: **VLSI I LAB**

Year/Semester: Fourth Year first Semester

Section: **A1**

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INTRODUCTION

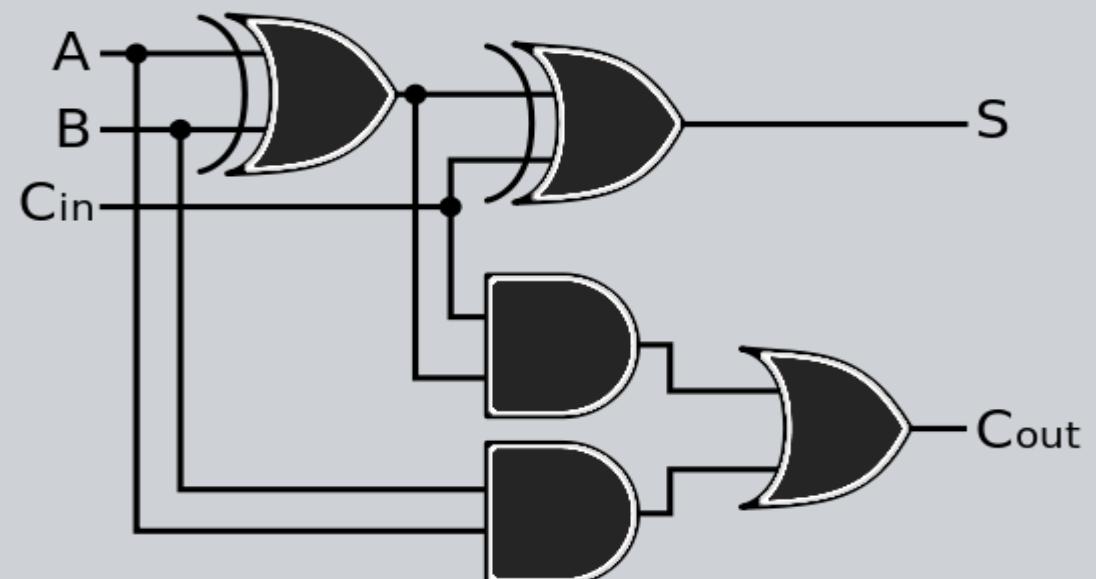
- A full adder is an important component in digital circuits used to perform addition operations.
- In recent years, various low-power full adder designs have been proposed for VLSI applications.
- The 8T, 10T and 14T full adders are some of the popular low-power full adder designs.
- These full adders differ in terms of their transistor count and layout area, and each has its own advantages and limitations.
- The analysis of these full adders will help in determining which design is most suitable for specific VLSI applications.
- The aim of this presentation is to compare the performance of these four full adders and identify which design offers the best trade-off between power consumption, delay, and layout area.

Full-Adder | Truth Table & Logic Diagram

Truth Table

Inputs			Outputs	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

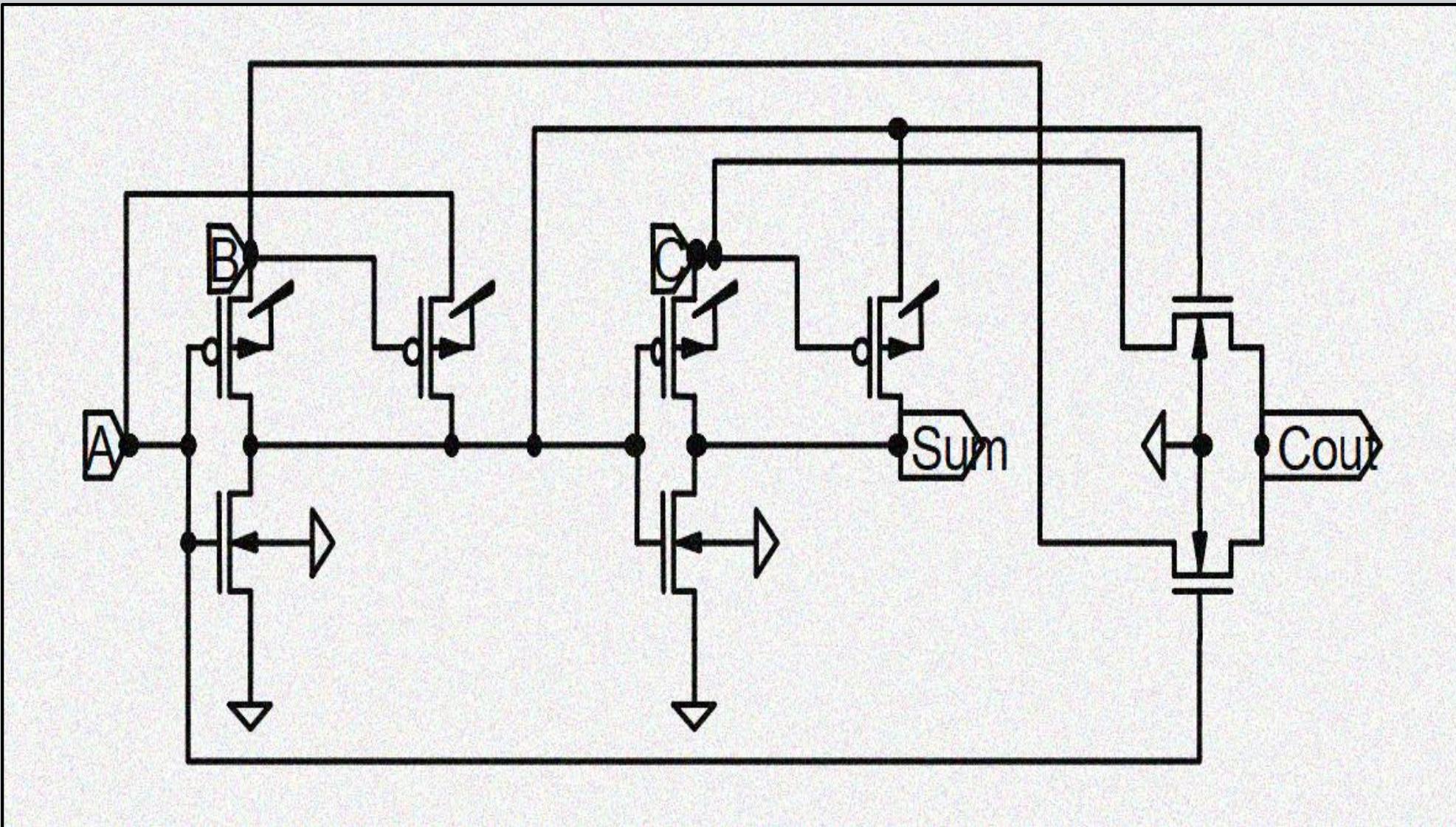
Logic Diagram



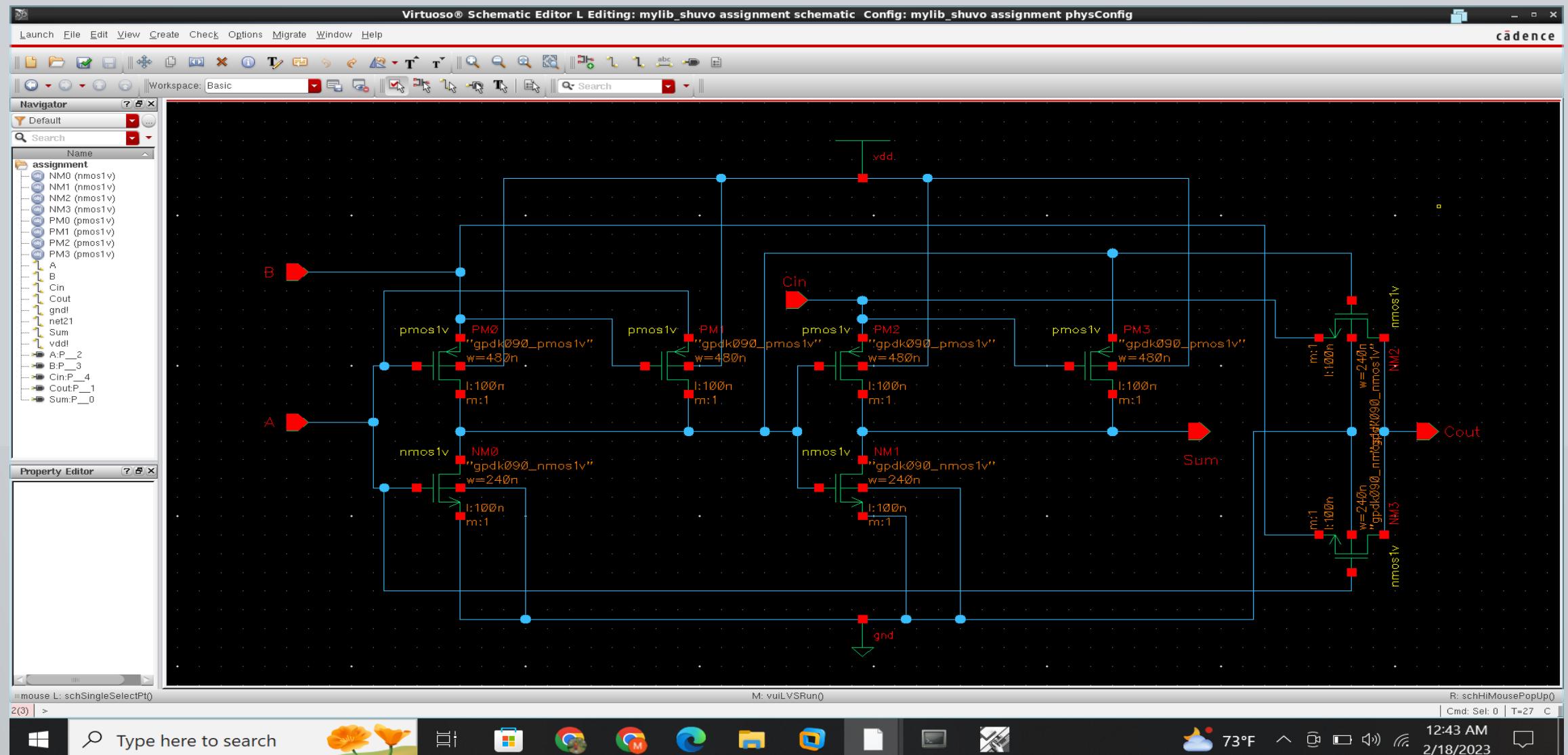
$$\text{Sum} = A \oplus B \oplus C_{in}$$

$$C_{out} = C_{in} (A \oplus B) + AB$$

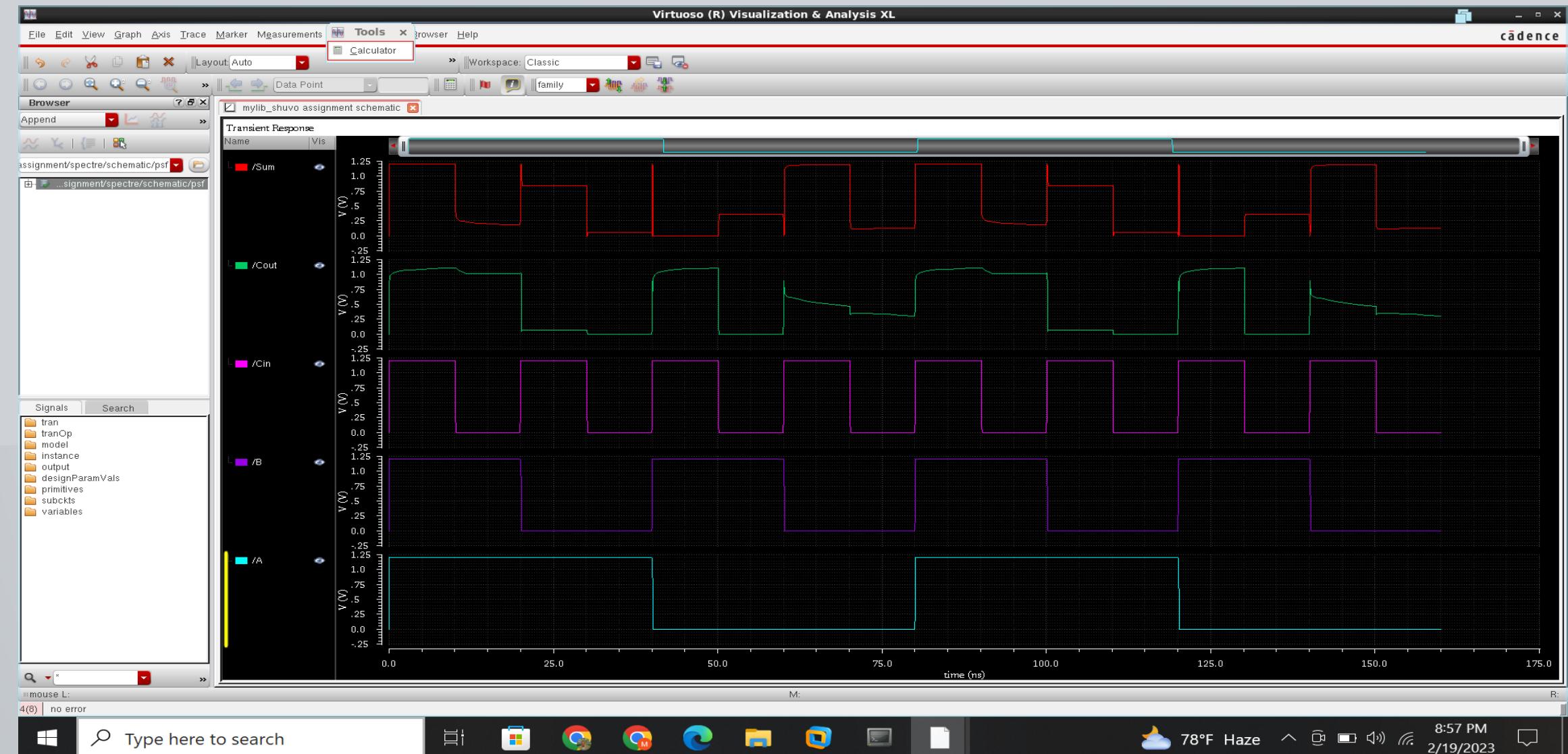
8T Full-Adder | Circuit Diagram



8T Full-Adder | Schematic



8T Full-Adder | Input-Output Graph



8T Full-Adder | Delay Calculations

Virtuoso (R) Visualization & Analysis XL calculator

In Context Results DB: /home/buet/simulation/assignment/spectre/schematic/psf

vt vf vdc vs op var vn sp vswr hp zm
it if idc is opt mp vn2 zp yp gd data
Off Family Wave Clip Append Rectangular

Key ... 19.3E-12

Stack

```
delay(?wf1 VT("/Cin"), ?value1 0.6, ?edge1 "rising", ?nth1 3, ?td1 0.0, ?wf2 VT("/Sum"), ?value2 0.6, ?edge2 "rising", ?nth2 3, ?td2 nil, ?stop nil, ?multiple nil)
-39.36E-9
```

Function Panel

Special Functions

PN	dftbb	harmonic	phaseNoise	spectralPower
a2d	dnl	harmonicFreq	pow	spectrum
abs_jitter	dutyCycle	histo	prms	spectrumMeas
average	evmQAM	iinteg	psd	stddev
bandwidth	evmQpsk	integ	psddb	tangent
clip	eyeDiagram	intersect	pstddev	thd
compare	fallTime	ipn	pzbode	unityGainFreq
compression	flip	ipnVRI	pzfilter	value
compressionVRI	fourEval	loadpull	riseTime	xmax
convolve	freq	lshift	rms	xmin
cross	freq_jitter	overshoot	rmsNoise	xval
d2a	frequency	pavg	root	ymax
dBm	gainBwProd	peak	rshift	ymin
delay	gainMargin	peakToPeak	sample	
deriv	getAsciiWave	period_jitter	settlingTime	
dft	groupDelay	phaseMargin	slewRate	

Function Panel Expression Editor Memories

Successful evaluation

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8T Full-Adder | Average Power Calculations

Virtuoso (R) Visualization & Analysis XL calculator

In Context Results DB: /home/buet/simulation/assignment/spectre/schematic/psf

File Tools View Options Constants Help

vt vf vdc vs op var vn sp vswr hp zm
it if idc is opt mp vn2 zp yp gd data
Off Family Wave Clip Append Rectangular |

Key ... 82.0E-6

Stack

```
average(getData(":pwr" ?result "tran"))
19.3E-12
delay(?wf1 VT("/Cin"), ?value1 0.6, ?edge1 "rising", ?nth1 3, ?td1 0.0, ?wf2 VT("/Sum"), ?value2 0.6, ?edge2 "rising", ?nth2 3, ?td2 nil, ?stop nil, ?multiple nil)
-39.98E-9
```

Function Panel

Special Functions

PN	compressionVRI	dffbb	fourEval	harmonic	loadpull	phaseNoise	riseTime	spectralPower	xmax
a2d	convolve	dnl	freq	harmonicFreq	lshift	pow	rms	spectrum	xmin
abs_litter	cross	dutyCycle	freq_litter	histo	overshoot	prms	rmsNoise	spectrumMeas	xval
average	d2a	evmQAM	frequency	iinteg	pavg	psd	root	stddev	ymax
bandwidth	dBm	evmQpsk	gainBwProd	integ	peak	psdbb	rshift	tangent	ymin
clip	delay	eyeDiagram	gainMargin	intersect	peakToPeak	pstddev	sample	thd	
compare	deriv	fallTime	getAsciiWave	ipn	period_jitter	pzbode	settlingTime	unityGainFreq	
compression	dft	flip	groupDelay	ipnVRI	phaseMargin	pzfilter	slewRate	value	

Function Panel Expression Editor Memories

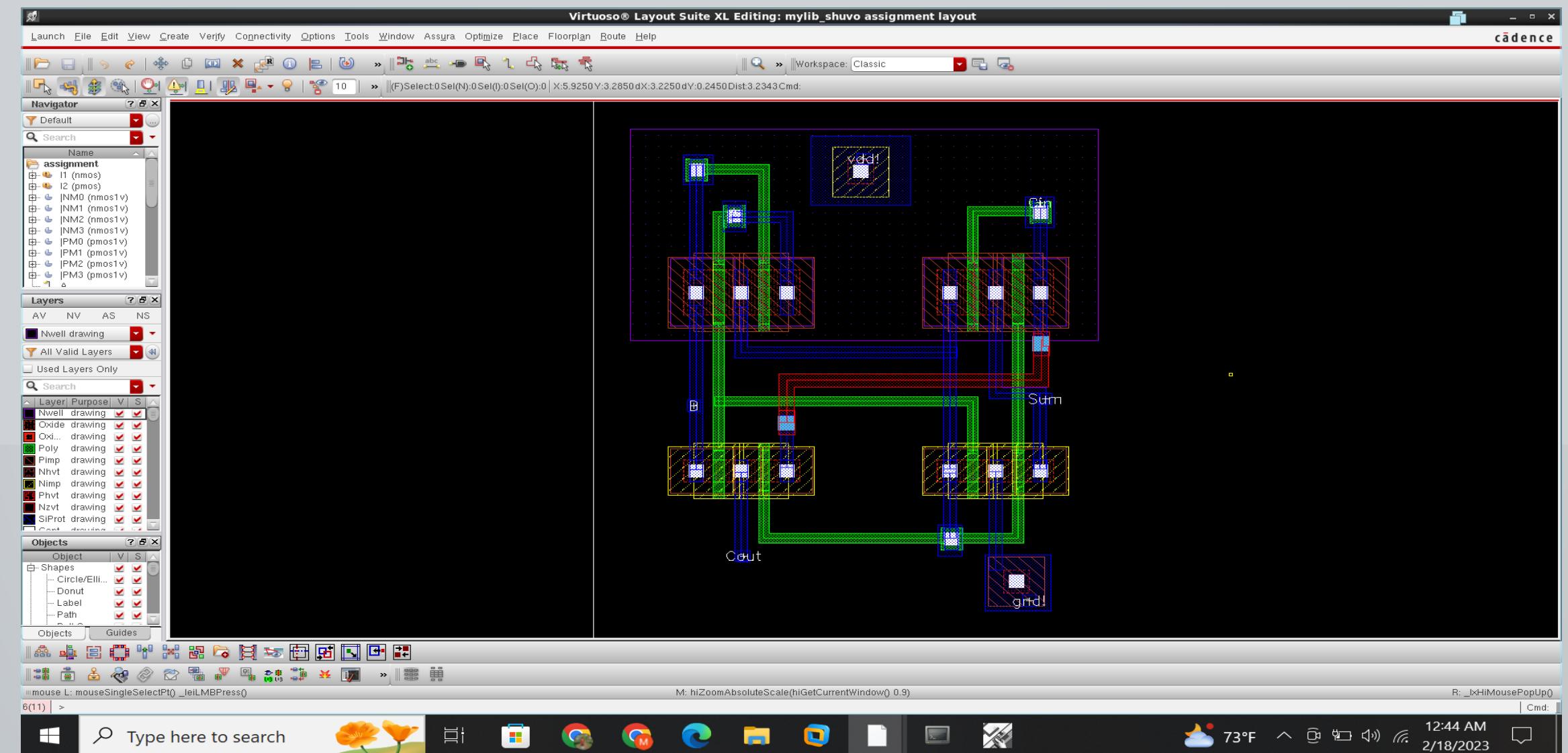
Successful evaluation

10 |

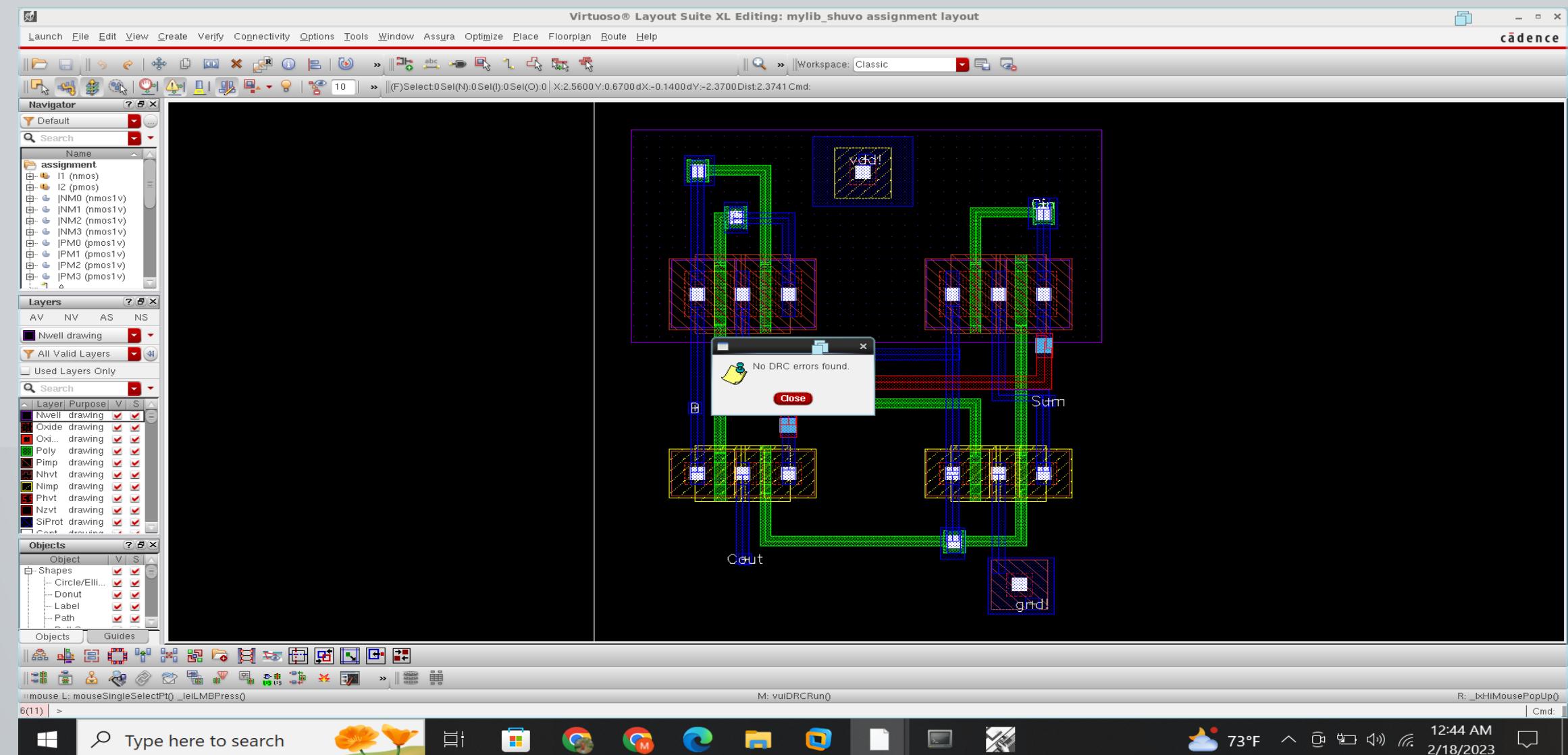
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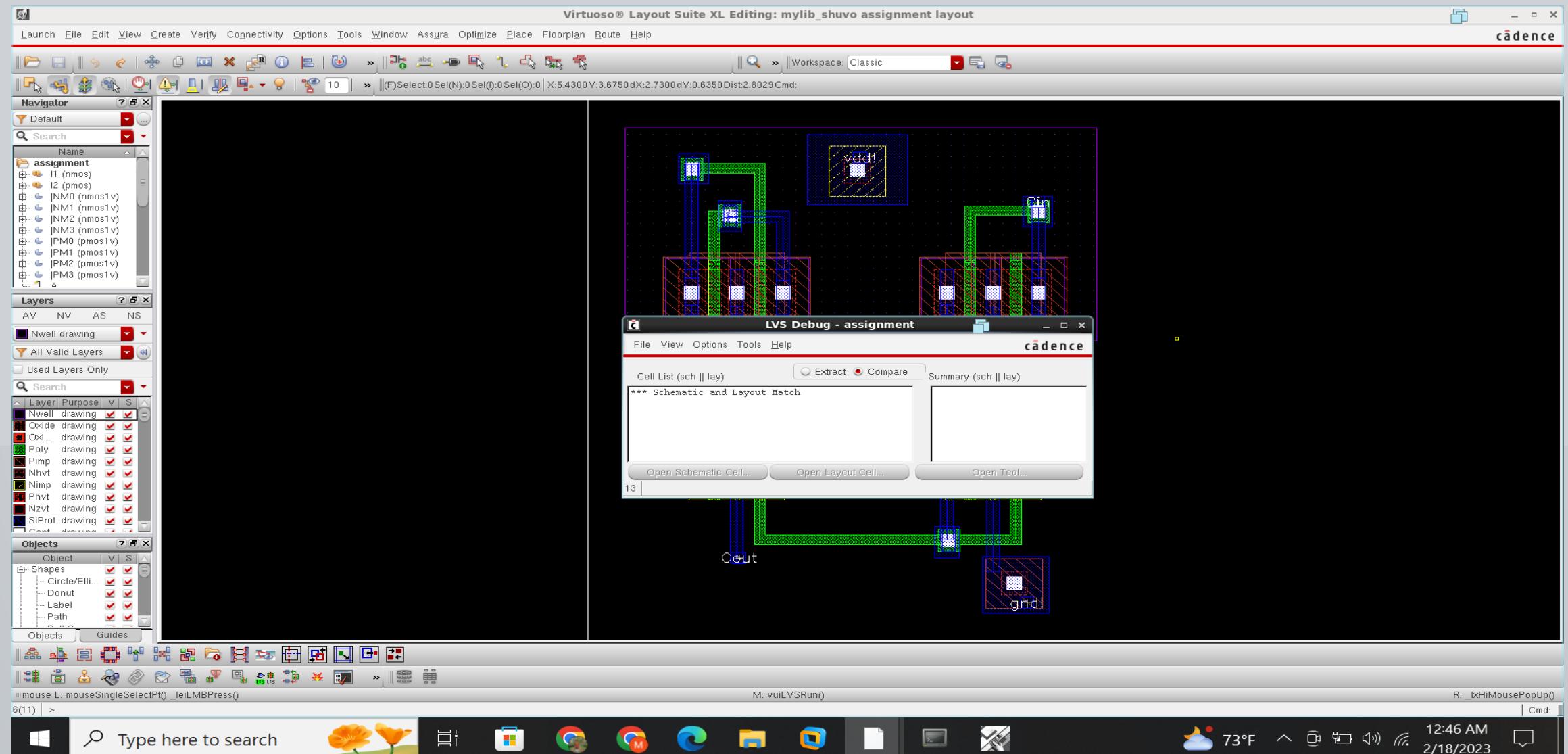
8T Full-Adder | Layout



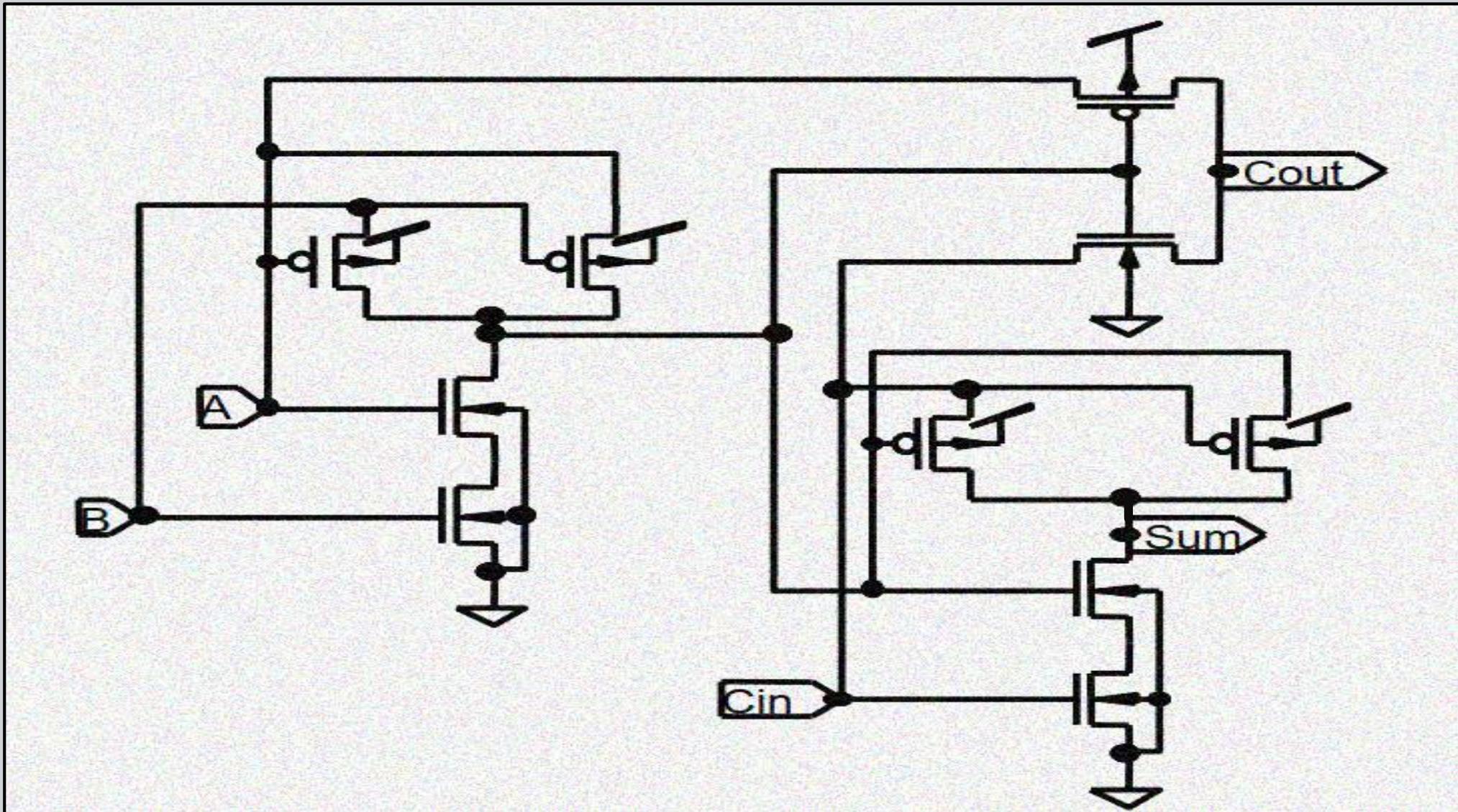
8T Full-Adder | Layout | No DRC



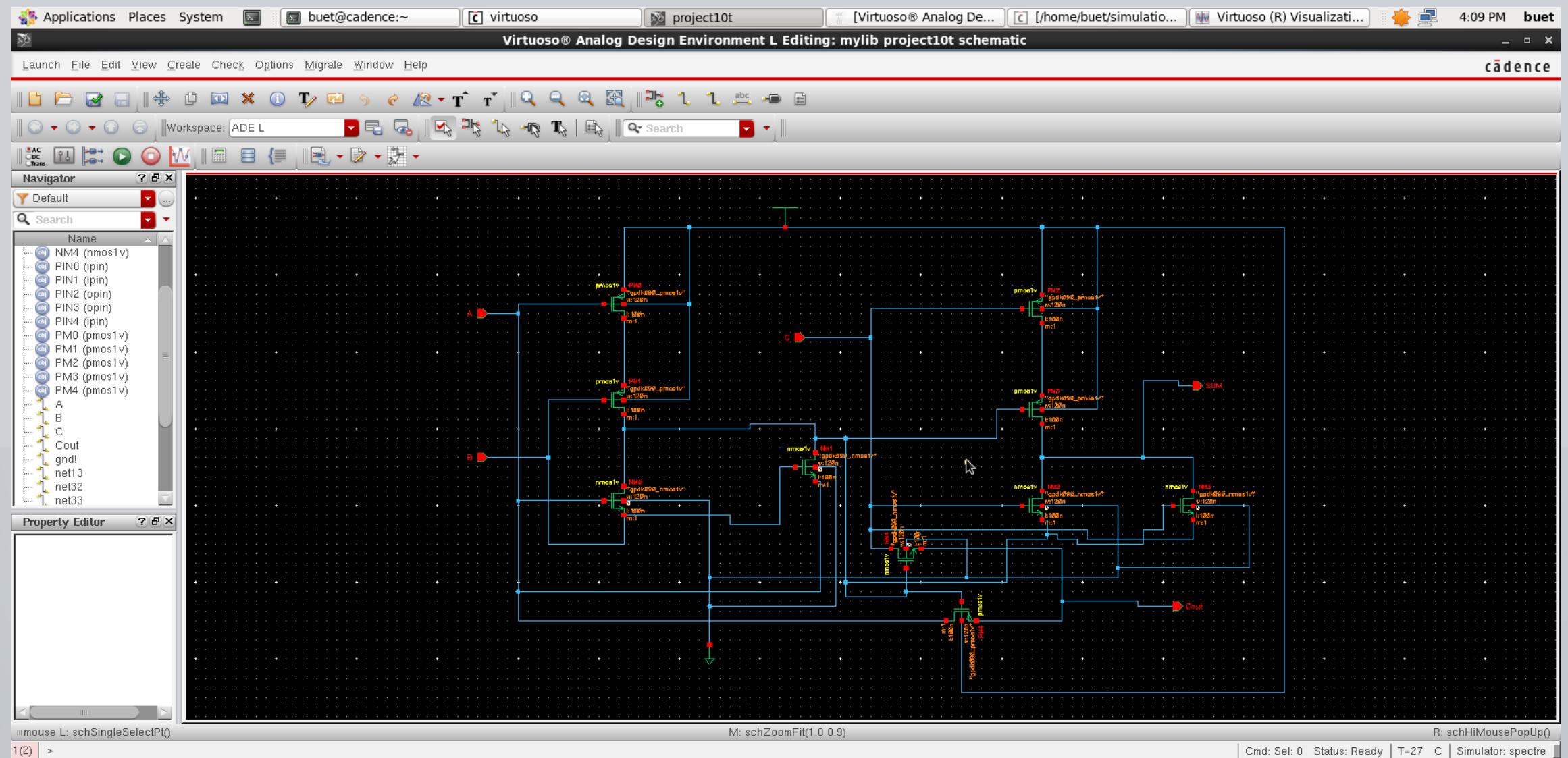
8T Full-Adder | Schematic Layout Match



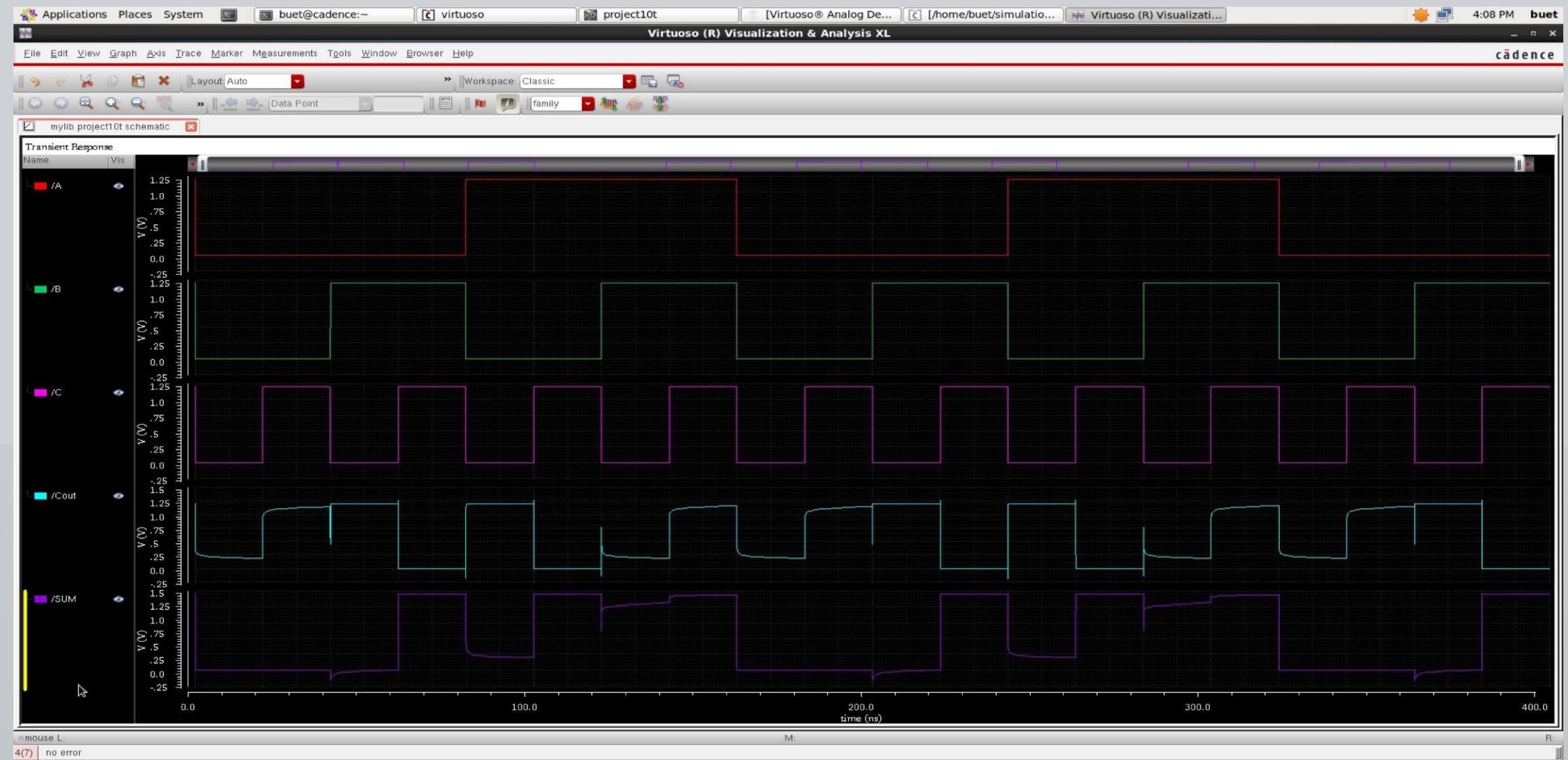
10T Full-Adder | Circuit Diagram



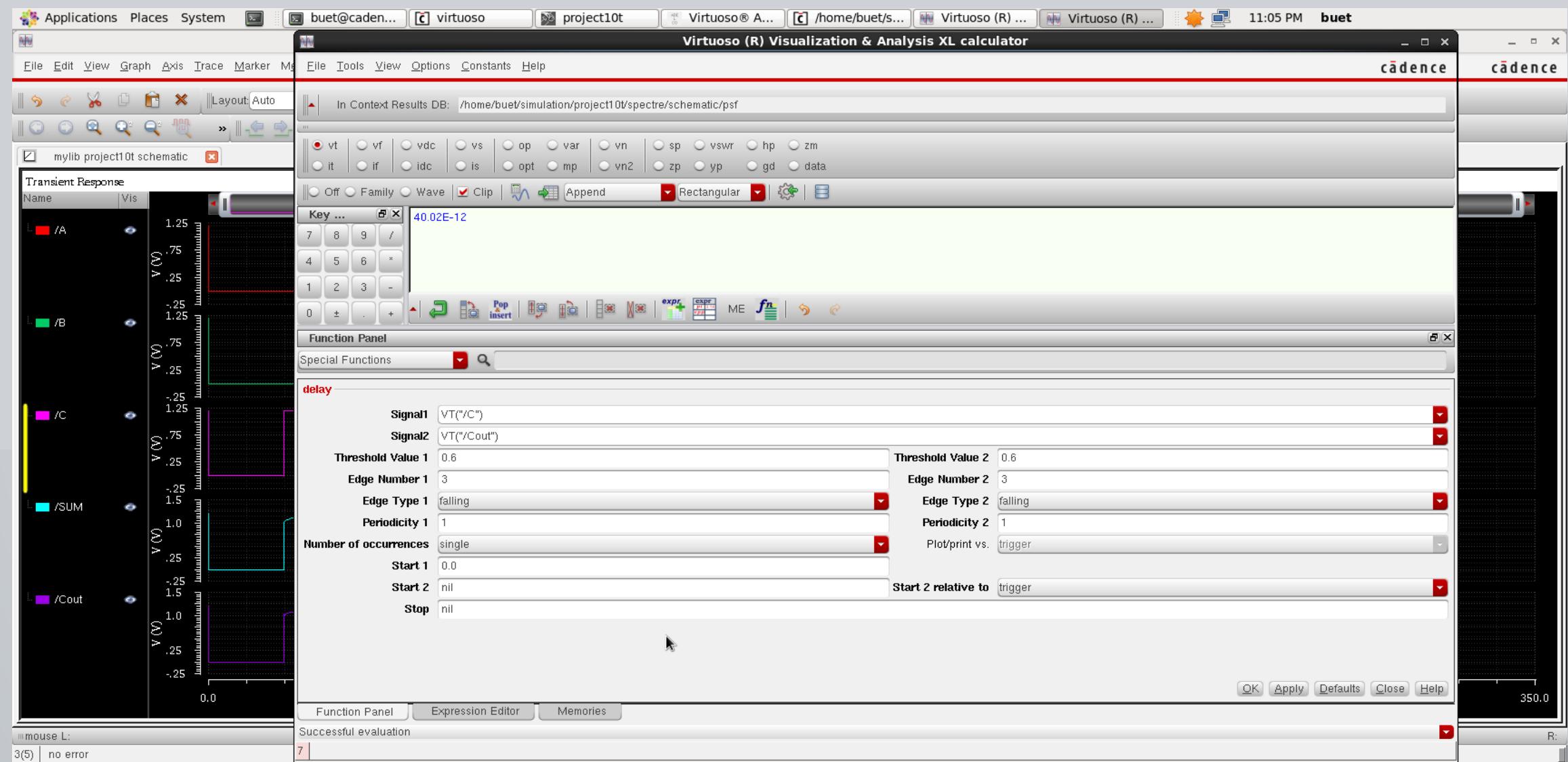
10T Full-Adder | Schematic



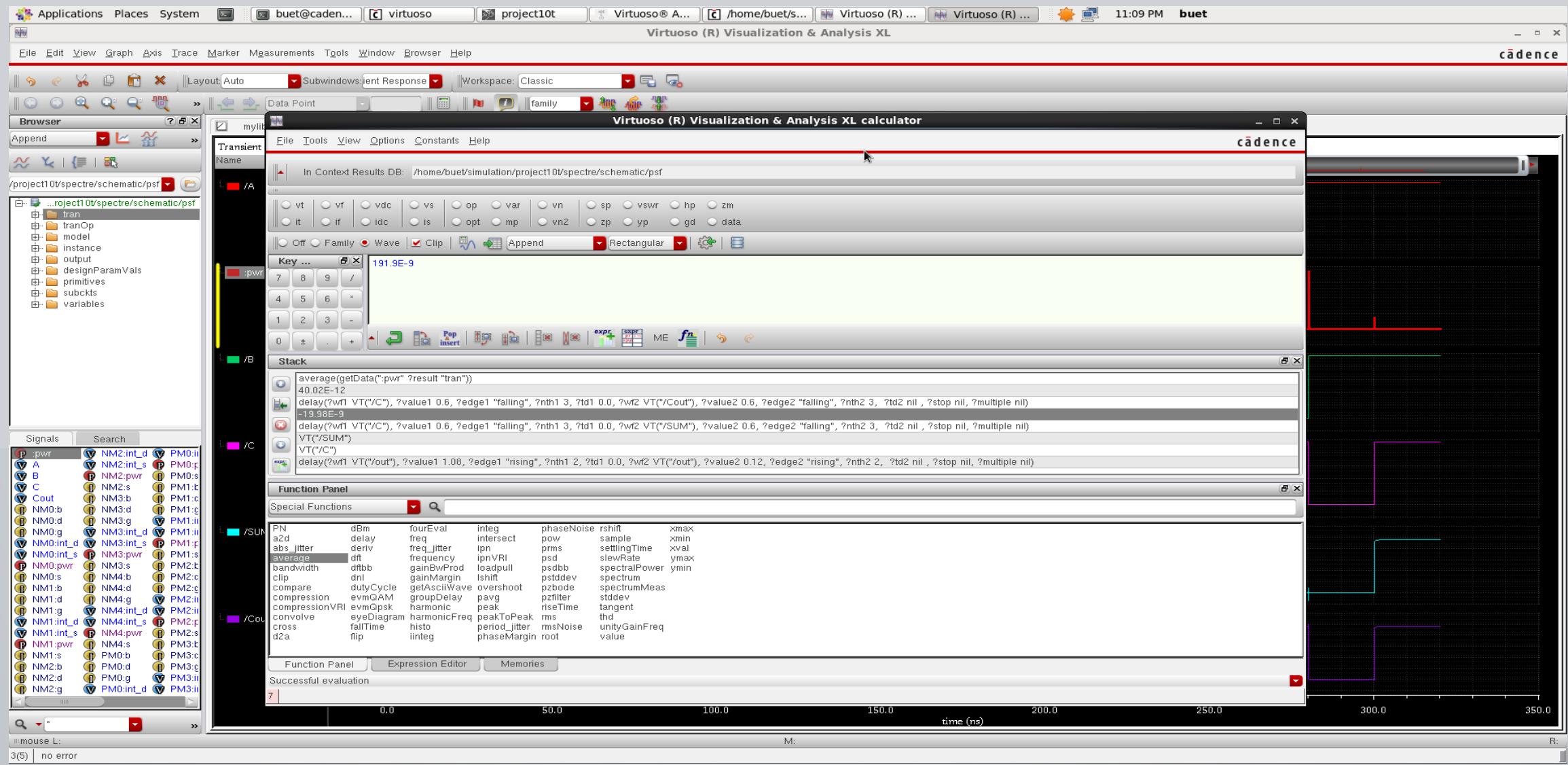
10T Full-Adder | Input-Output Graph



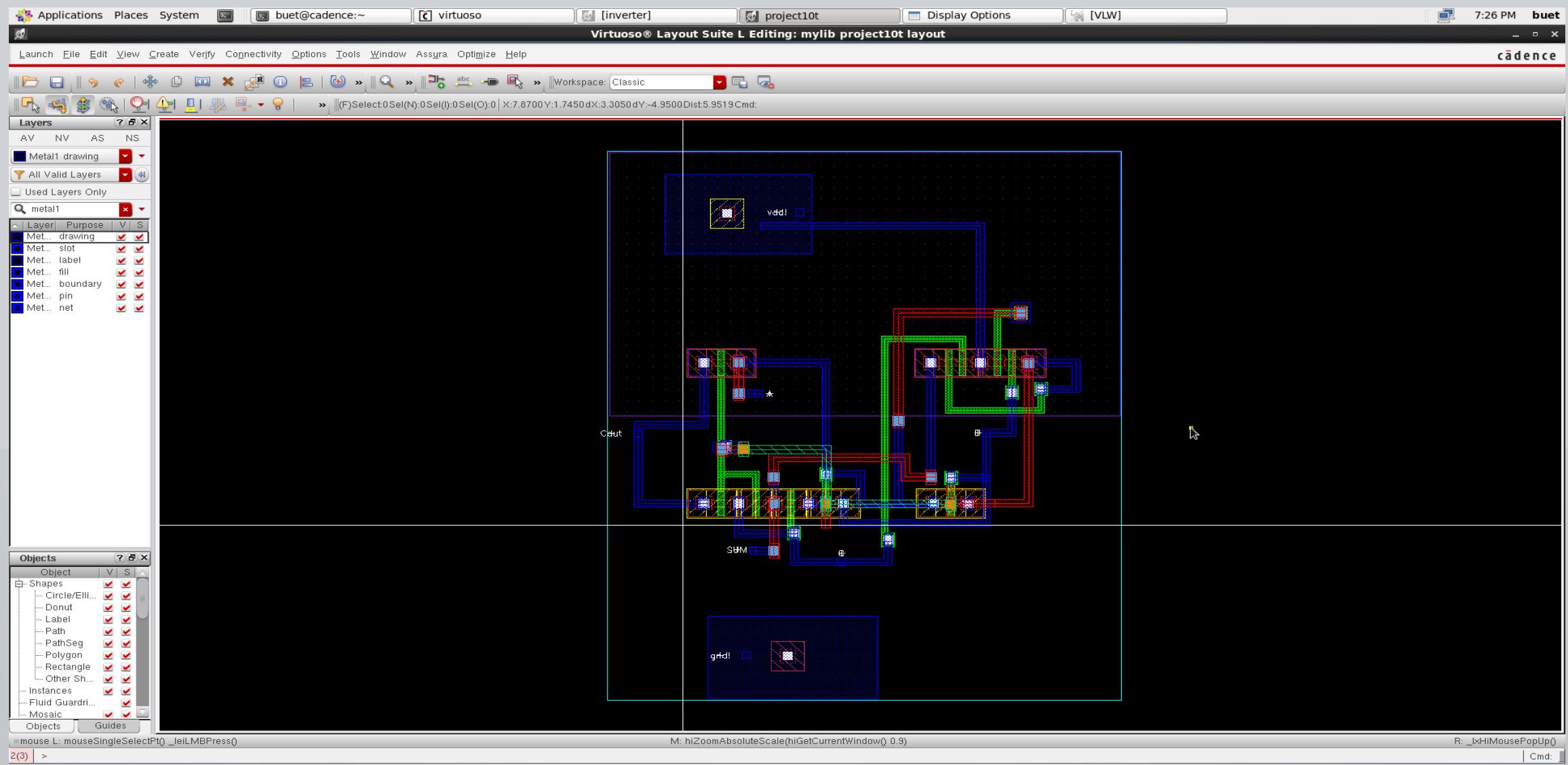
10T Full-Adder | Delay Calculations



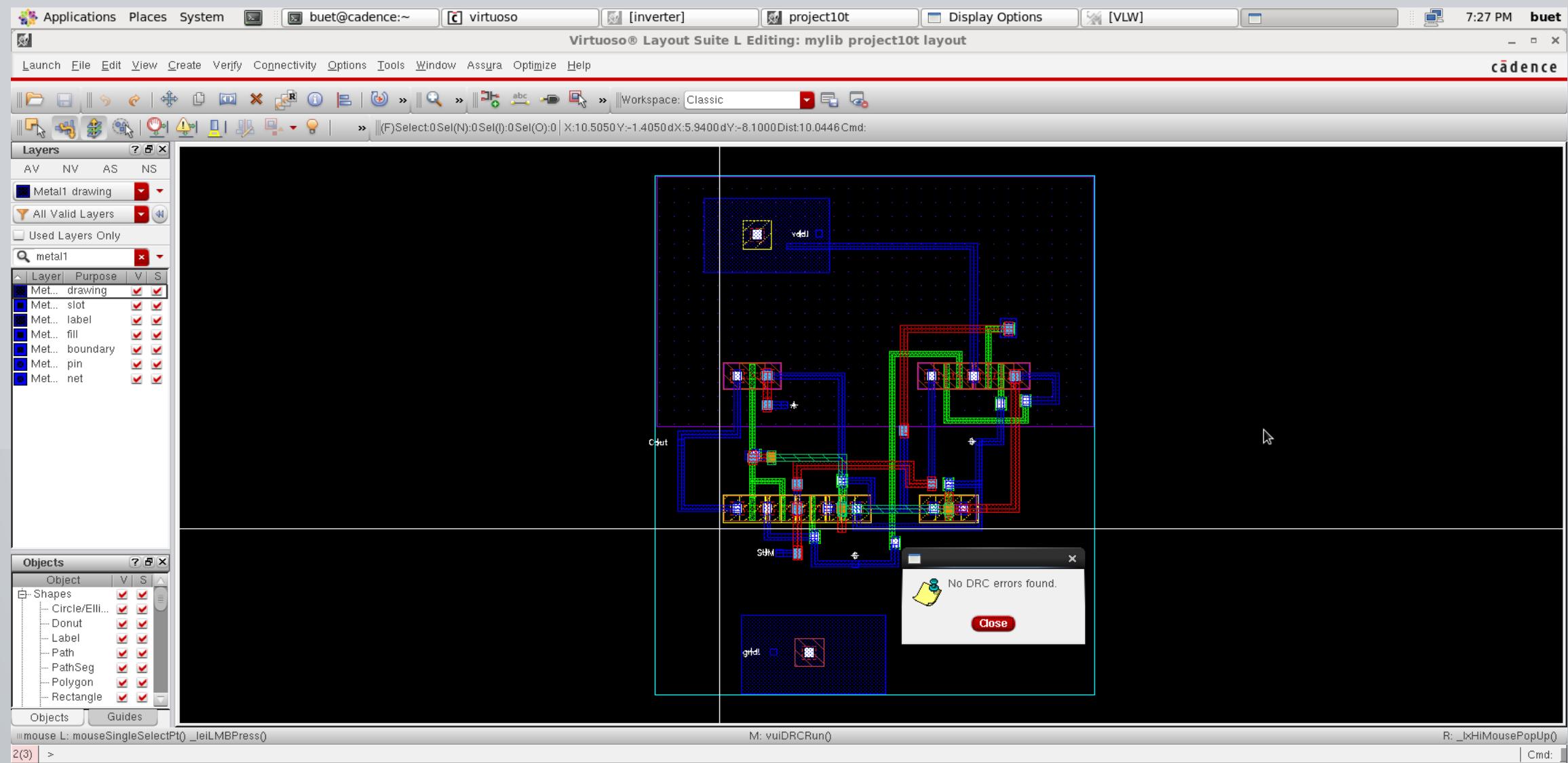
10T Full-Adder | Average Power Calculations



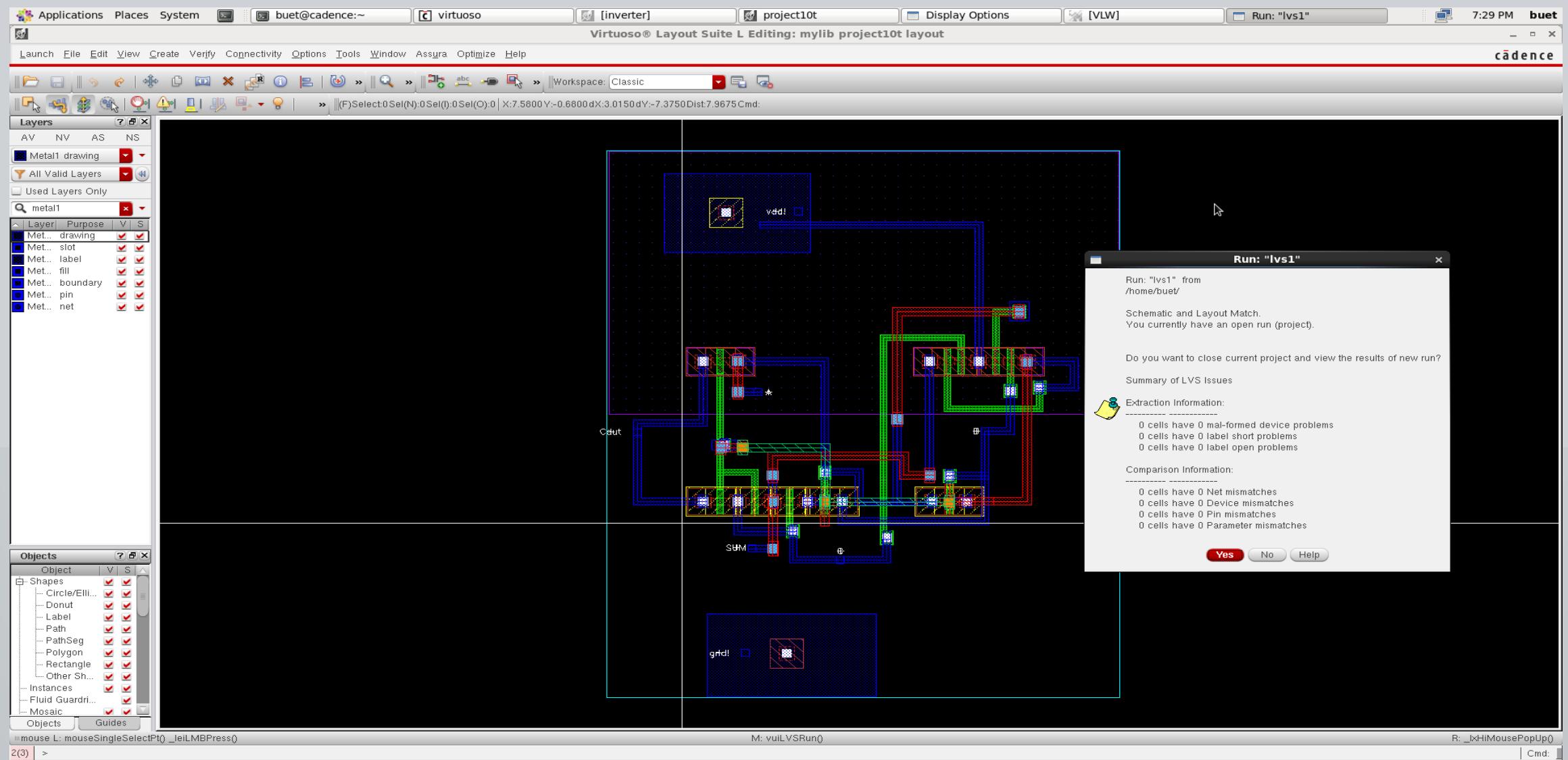
10T Full-Adder | Layout



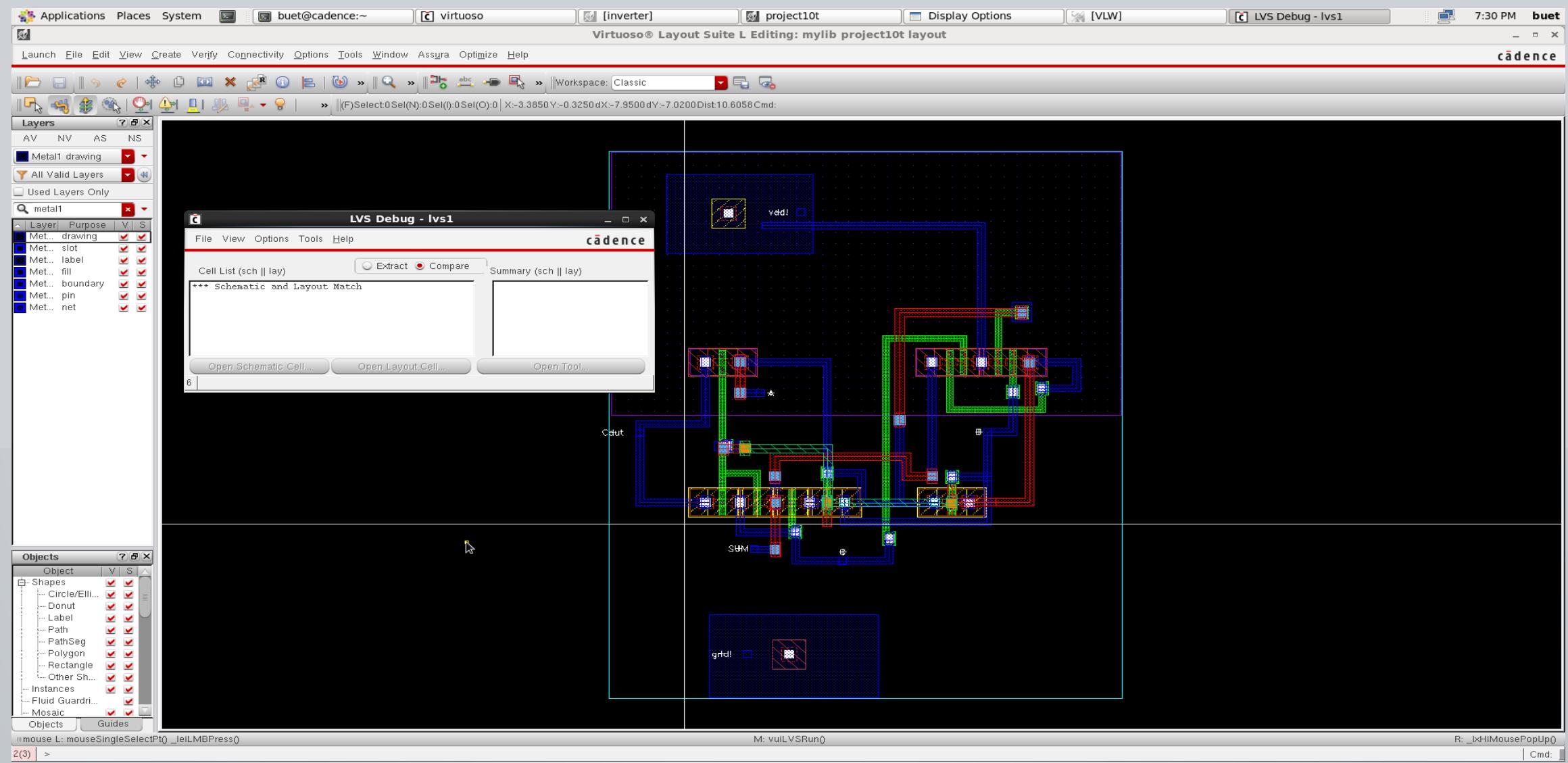
10T Full-Adder | Layout | No DRC



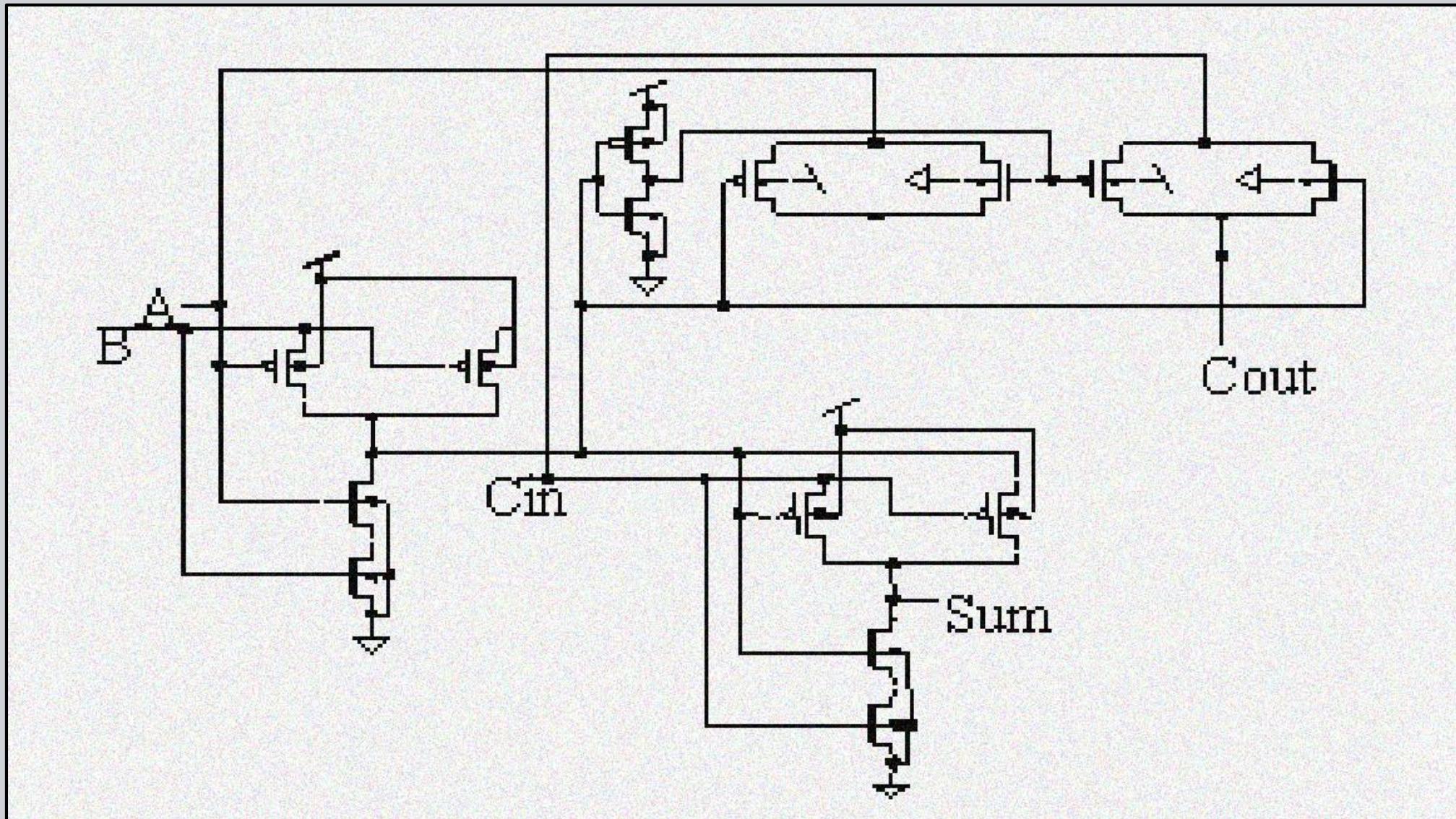
10T Full-Adder | Layout | No LVS



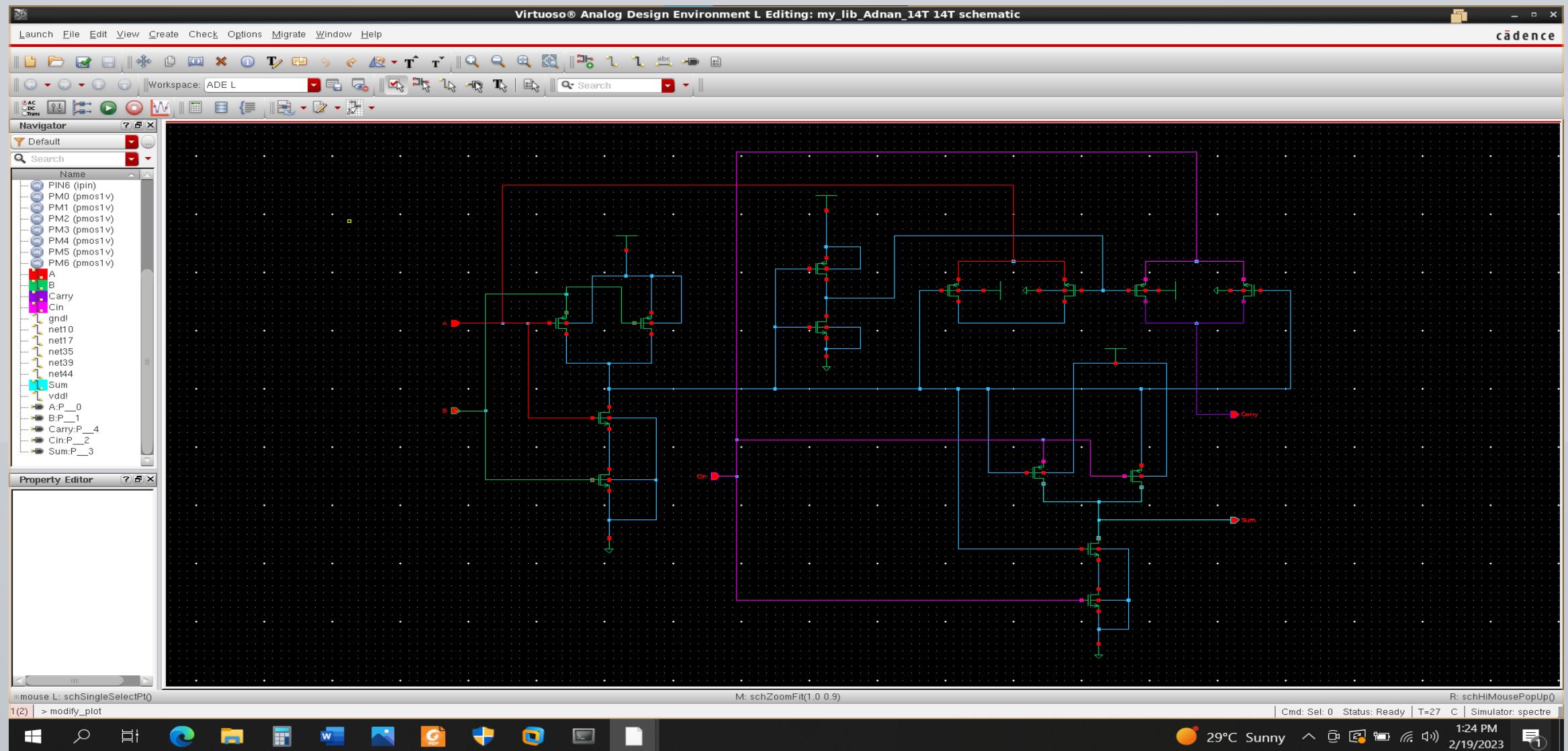
10T Full-Adder | Schematic Layout Match



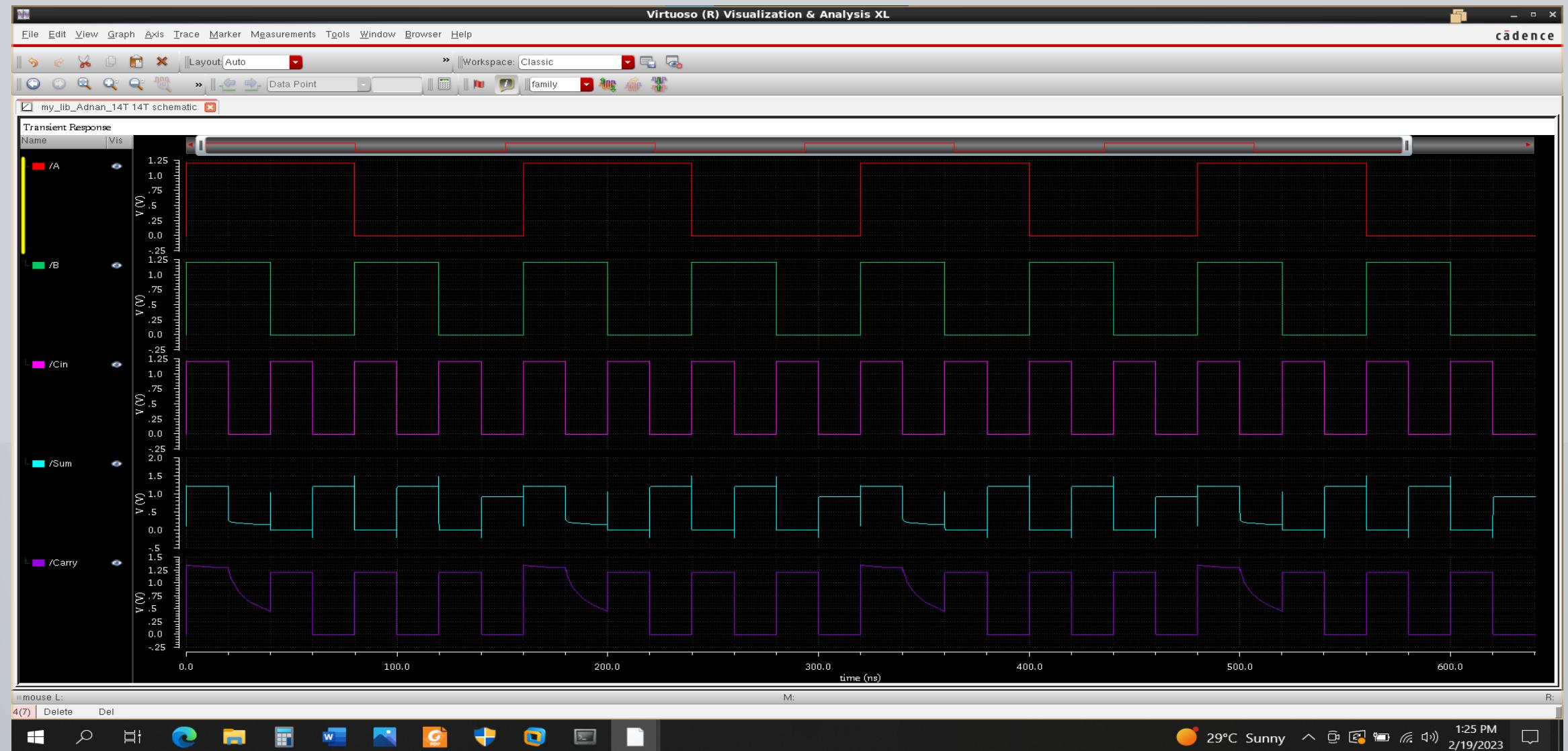
14T Full-Adder | Circuit Diagram



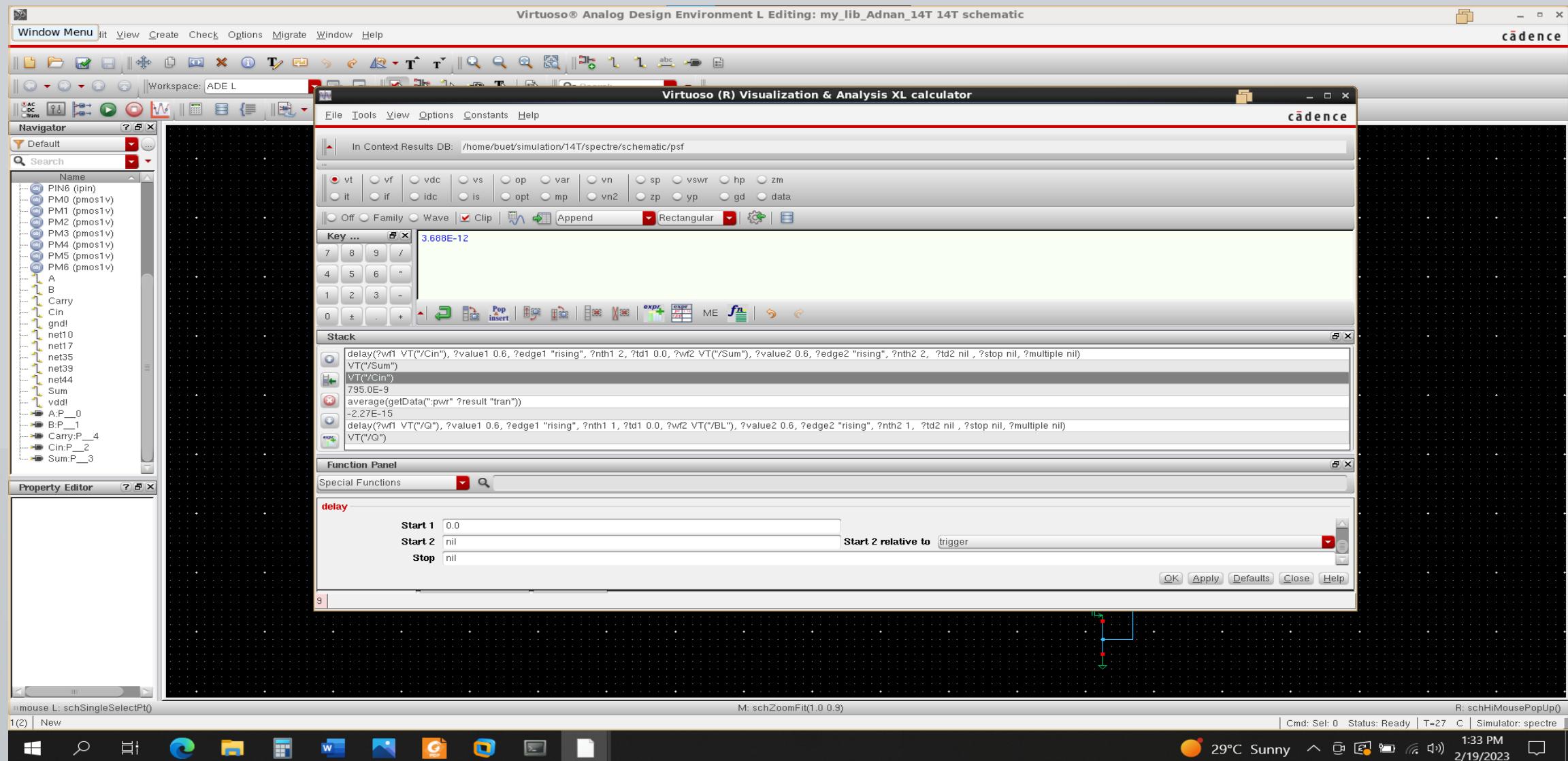
14T Full-Adder | Schematic



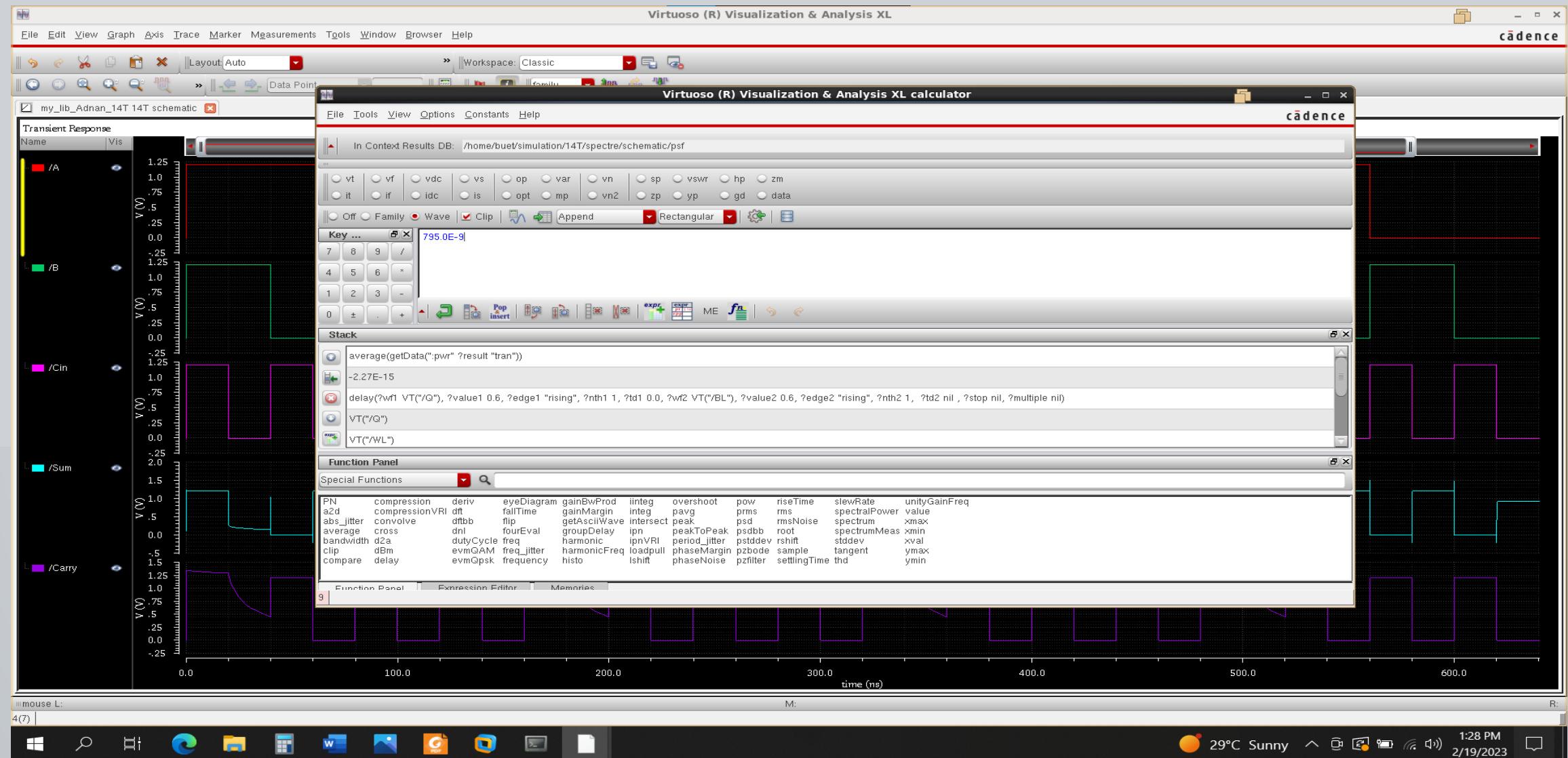
14T Full-Adder | Input-Output Graph



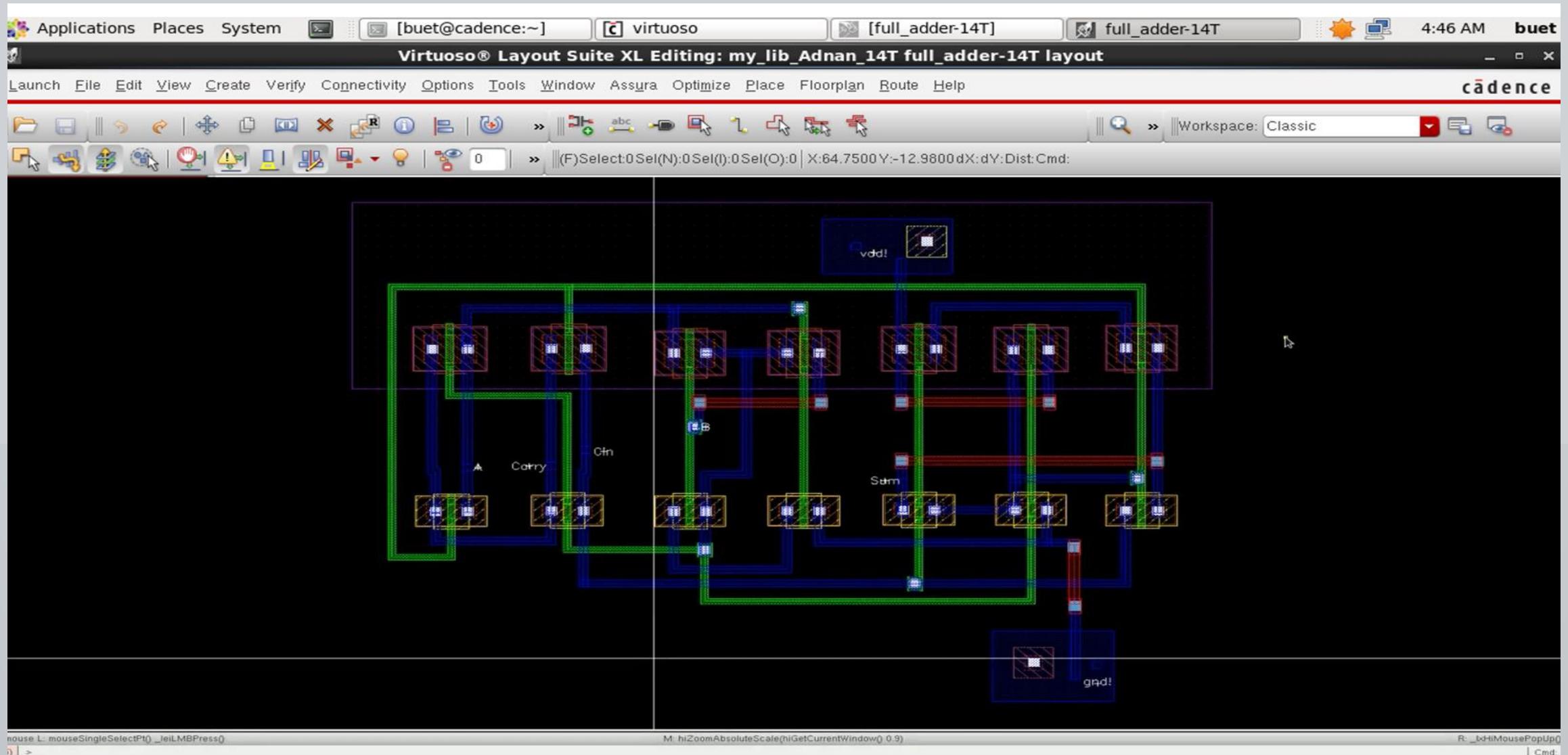
14T Full-Adder | Delay Calculations



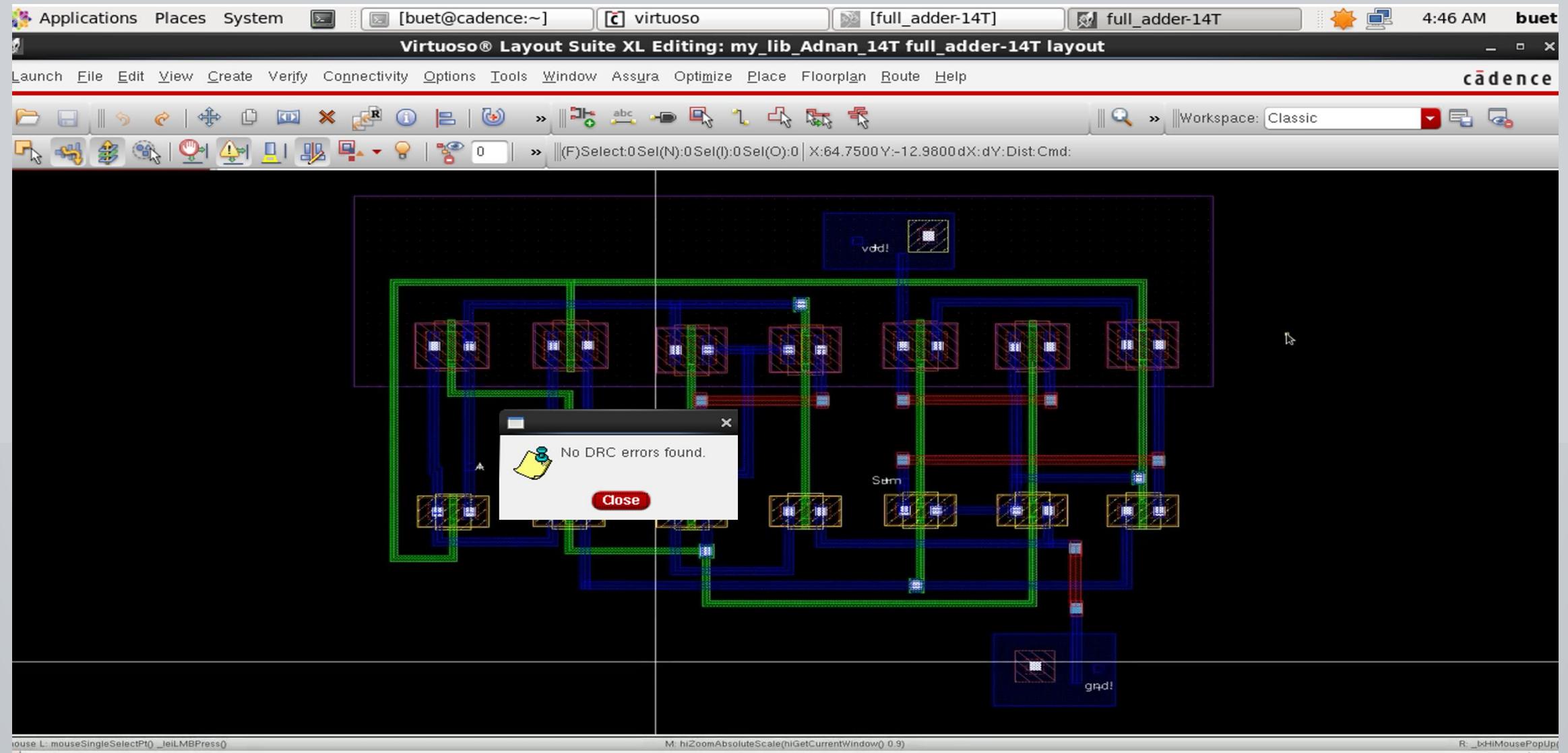
14T Full-Adder | Average Power Calculations



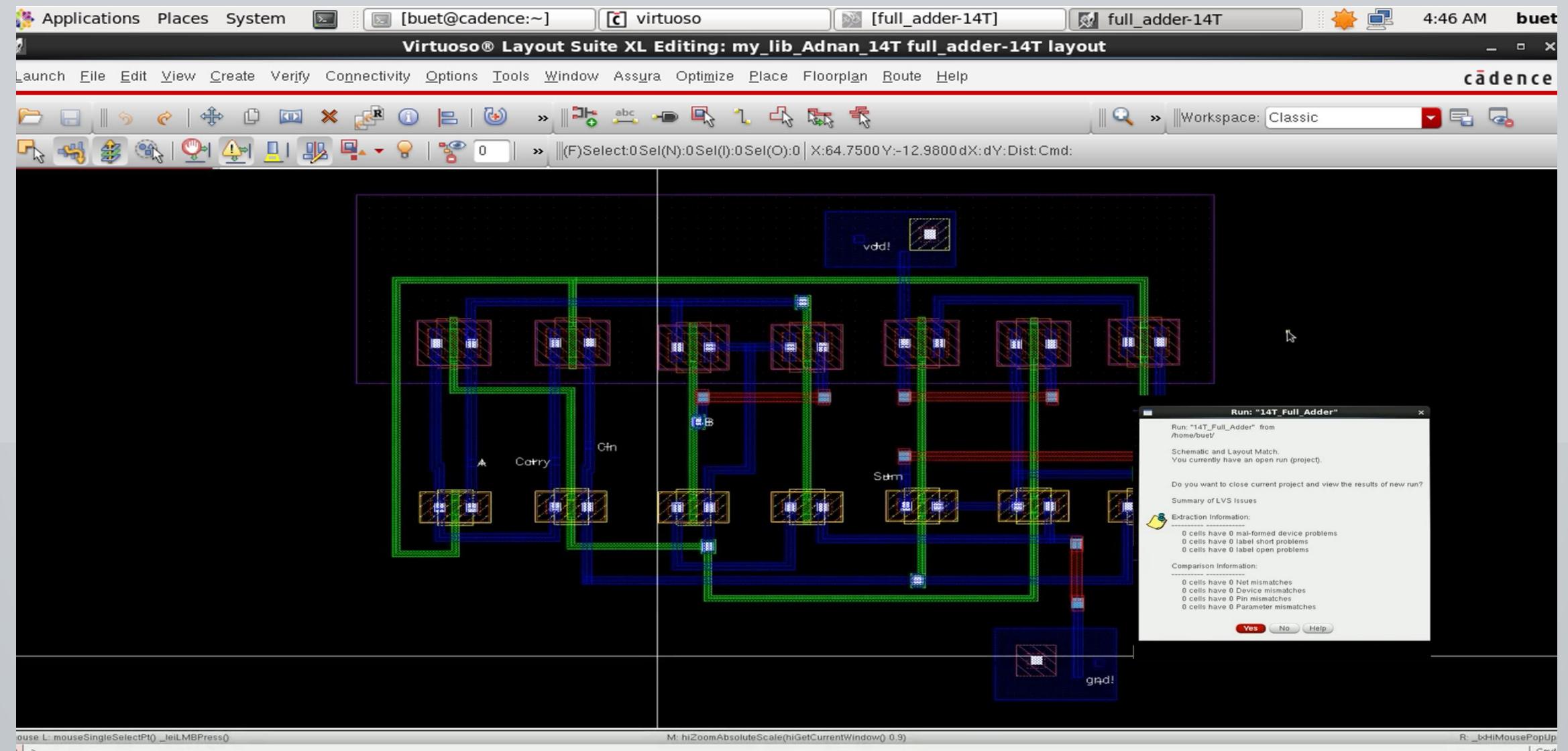
14T Full-Adder | Layout



14T Full-Adder | Layout | No DRC



14T Full-Adder | Layout | No LVS



Full-Adder | Comparison Table

Full Adder	8T	10T	14T
Propagation Delay	19.3E-12	40.02E-12	3.688E-12
Average Power	82.0E-9	191.9E-9	795.0E-9
Power Delay Product	1.5826E-18	7.6798E-18	2.9319E-18
Cell Area	22.6157	78.4458	68.1674
No of Transistors	8	10	14
No of DRC Error	0	0	0
No of LVS Mismatched	0	0	0

CONCLUSION

- The performance analysis of 1-bit full adders is an important research area in the field of VLSI design.
- In this study, we compared the 8T, 10T and 14T full adders using various metrics, including power consumption, delay, and area.
- Our simulation results showed that the 10T full adder had the lowest power consumption and delay, while the 8T full adder had the smallest area.
- The choice of the best full adder for a particular application depends on the design requirements and constraints.
- Overall, the analysis of 1-bit full adders is critical for the development of efficient and high-performance digital circuits in VLSI design.



THANK YOU