Pin	Signal	Description
1	CS	Chip Select
2	NC	Not Connected
3	SDO	Master-In-Slave-Out
4	SCK	Serial Clock
5	GND	Power Supply Ground
6	VCC	Power Supply

Table 1. Connector J1- Pin Descriptions as labeled on the Pmod.

The PmodALS reports to the host board when the ADC081S021 is placed in normal mode by bringing the CS pin low, and delivers a single reading in 16 SCLK clock cycles. The PmodALS requires the frequency of the SCLK to be between 1 MHz and 4 MHz. The bits of information, placed on the falling edge of the SCLK and valid on the subsequent rising edge of SCLK, consist of three leading zeroes, the eight bits of information with the MSB first, and four trailing zeroes.

Any external power applied to the PmodALS must be within 2.7V and 5.25V; however, it is recommended that Pmod is operated at 3.3V.

3 Physical Dimensions

The pins on the pin header are spaced 100 mil apart. The PCB is 0.8 inches long on the sides parallel to the pins on the pin header and 0.8 inches long on the sides perpendicular to the pin header.

4 Additional Information

The schematics of the PmodALS are available for download from the product page. Additional information about the ADC, including communication modes and specific timings of the chip, can be found by checking out its datasheet available from Texas Instruments. Similarly, the datasheet for the ambient light sensor can be found on the website for Vishay.

More specific information about how to use the PmodALS can be found by checking out our user guide. Example code demonstrating how to get information from the PmodALS can be found here.

If you have any questions or comments about the PmodALS, feel free to post them under the appropriate section ("Add-on Boards") of the Digilent Forum.

ADC081S021 Single Channel, 50 to 200 ksps, 8-Bit A/D Converter

Check for Samples: ADC081S021

FEATURES

- **Specified Over a Range of sample Rates.**
- **6-lead WSON and SOT-23 Packages**
- **Variable Power Management**
- **Single Power Supply with 2.7V - 5.25V Range**
- **SPI™/QSPI™/MICROWIRE/DSP Compatible**

KEY SPECIFICATIONS

- **DNL: +0.04/-0.03 LSB (typ)**
- **INL: +0.04/-0.03 LSB (typ)**
- **SNR: 49.6 dB (typ)**
- **Power Consumption**
  - **3.6V Supply: 1.3 mW (typ)**
  - **5.25V Supply: 7.7 mW (typ)**

APPLICATIONS

- **Portable Systems**
- **Remote Data Acquisition**
- **Instrumentation and Control Systems**

DESCRIPTION

The ADC081S021 is a low-power, single channel CMOS 8-bit analog-to-digital converter with a high-speed serial interface. Unlike the conventional practice of specifying performance at a single sample rate only, the ADC081S021 is fully specified over a sample rate range of 50 ksps to 200 ksps. The converter is based upon a successive-approximation register architecture with an internal track-and-hold circuit.

The output serial data is straight binary, and is compatible with several standards, such as SPI, QSPI, MICROWIRE, and many common DSP serial interfaces.

The ADC081S021 operates with a single supply that can range from +2.7V to +5.25V. Normal power consumption using a +3.6V or +5.25V supply is 1.3 mW and 7.7 mW, respectively. The power-down feature reduces the power consumption to as low as 2.6 µW using a +5.25V supply.

The ADC081S021 is packaged in 6-lead WSON and SOT-23 packages. Operation over the industrial temperature range of −40°C to +85°C is ensured.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Pin-Compatible Alternatives by Resolution and Speed(1)

Resolution	Specified for Sample Rate Range of:		
	50 to 200 ksps	**200 to 500 ksps**	**500 ksps to 1 Msps**
12-bit	ADC081S021121S021	ADC081S021121S051	ADC081S021121S101
10-bit	ADC081S021101S021	ADC081S021101S051	ADC081S021101S101
8-bit	**ADC081S021**	ADC081S021081S051	ADC081S021081S101

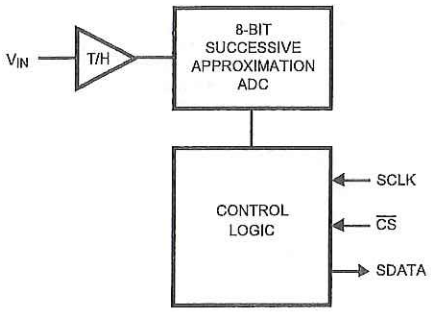
(1) All devices are fully pin and function compatible.

Connection Diagram

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Block Diagram



PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS

Pin No.	Symbol	Description
ANALOG I/O		
3	V_{IN}	Analog input. This signal can range from 0V to V_A.
DIGITAL I/O		
4	SCLK	Digital clock input. This clock directly controls the conversion and readout processes.
5	SDATA	Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.
6	$\overline{CS}$	Chip select. On the falling edge of $\overline{CS}$, a conversion process begins.
POWER SUPPLY		
1	V_A	Positive supply pin. This pin should be connected to a quiet +2.7V to +5.25V source and bypassed to GND with a 1 µF capacitor and a 0.1 µF monolithic capacitor located within 1 cm of the power pin.
2	GND	The ground return for the supply and signals.
PAD	GND	For package suffix CISD(X) only, it is recommended that the center pad should be connected to ground.

Absolute Maximum Ratings (1) (2) (3)

Analog Supply Voltage V_A		−0.3V to 6.5V
Voltage on Any Analog Pin to GND		−0.3V to (V_A +0.3V)
Voltage on Any Digital Pin to GND		−0.3V to 6.5V
Input Current at Any Pin (4)		±10 mA
Package Input Current (4)		±20 mA
Power Consumption at T_A = 25°C		See (5)
ESD Susceptibility (6)	Human Body Model	3500V
	Machine Model	300V
Junction Temperature		+150°C
Storage Temperature		−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

(3) If Military/Aerospace specified devices are required, please contact the TI Office/Distributors for availability and specifications.

(4) When the input voltage at any pin exceeds the power supply (that is, V_{IN} < GND or V_{IN} > V_A), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two. The Absolute Maximum Rating specification does not apply to the V_A pin. The current into the V_A pin is limited by the Analog Supply Voltage specification.

(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through zero ohms

ADC081S021 Converter Electrical Characteristics[1][2] (continued)

The following specifications apply for V_A = +2.7V to 5.25V, f_{SCLK} = 1 MHz to 4 MHz, f_{SAMPLE} = 50 ksps to 200 ksps, C_L = 15 pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Typical	Limits[2]	Units
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA	V_A – 0.07	**V_A – 0.2**	V (min)
		I_{SOURCE} = 1 mA	V_A – 0.1		V
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA	0.03	**0.4**	V (max)
		I_{SINK} = 1 mA	0.1		V
I_{OZH}, I_{OZL}	TRI-STATE Leakage Current		±0.1	**±10**	µA (max)
C_{OUT}	TRI-STATE Output Capacitance		2	**4**	pF (max)
	Output Coding		Straight (Natural) Binary		
POWER SUPPLY CHARACTERISTICS					
V_A	Supply Voltage			**2.7**	V (min)
				5.25	V (max)
I_A	Supply Current, Normal Mode (Operational, $\overline{CS}$ low)	V_A = +5.25V, f_{SAMPLE} = 200 ksps	1.47	**2.2**	mA (max)
		V_A = +3.6V, f_{SAMPLE} = 200 ksps	0.36	**0.9**	mA (max)
	Supply Current, Shutdown ($\overline{CS}$ high)	f_{SCLK} = 0 MHz, V_A = +5.25V f_{SAMPLE} = 0 ksps	500		nA
		V_A = +5.25V, f_{SCLK} = 4 MHz, f_{SAMPLE} = 0 ksps	60		µA
P_D	Power Consumption, Normal Mode (Operational, $\overline{CS}$ low)	V_A = +5.25V	7.7	**11.6**	mW (max)
		V_A = +3.6V	1.3	**3.24**	mW (max)
	Power Consumption, Shutdown ($\overline{CS}$ high)	f_{SCLK} = 0 MHz, V_A = +5.25V f_{SAMPLE} = 0 ksps	2.6		µW
		f_{SCLK} = 4 MHz, V_A = +5.25V, f_{SAMPLE} = 0 ksps	315		µW
AC ELECTRICAL CHARACTERISTICS					
f_{SCLK}	Clock Frequency	See[3]		**1.0**	MHz (min)
				4.0	MHz (max)
f_S	Sample Rate	See[3]		**50**	ksps (min)
				200	ksps (max)
t_{HOLD}	Hold Time			**13**	SCLK Falling Edges
DC	SCLK Duty Cycle	f_{SCLK} = 4 MHz	50	**40**	% (min)
				60	% (max)
t_{ACQ}	Minimum Timre Required for Acquisition			**350**	ns (max)
t_{QUIET}	See[4]			**50**	ns (min)
t_{AD}	Aperture Delay		3		ns
t_{AJ}	Aperture Jitter		30		ps

(3) This is the frequency range over which the electrical performance is ensured. The device is functional over a wider range which is specified under Operating Ratings.
(4) Minimum Quiet Time required by bus relinquish and the start of the next conversion.

ADC081S021 Timing Specifications

The following specifications apply for V_A = +2.7V to 5.25V, GND = 0V, f_{SCLK} = 1.0 MHz to 4.0 MHz, C_L = 25 pF, f_{SAMPLE} = 50 ksps to 200 ksps, **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Typical	Limits	Units
t_{CS}	Minimum $\overline{CS}$ Pulse Width			**10**	ns (min)
t_{CSSU}	$\overline{CS}$ Setup Time prior to SCLK Falling Edge (1)			**10**	ns (min)
t_{CSH}	$\overline{CS}$ Hold Time after SCLK Falling Edge (1)			**1**	ns (min)
t_{EN}	Delay from $\overline{CS}$ Until SDATA TRI-STATE Disabled (2)			**20**	ns (max)
t_{ACC}	Data Access Time after SCLK Falling Edge (3)	V_A = +2.7V to +3.6V		**40**	ns (max)
		V_A = +4.75V to +5.25V		**20**	ns (max)
t_{CL}	SCLK Low Pulse Width			**0.4 x t_{SCLK}**	ns (min)
t_{CH}	SCLK High Pulse Width			**0.4 x t_{SCLK}**	ns (min)
t_H	SCLK to Data Valid Hold Time	V_A = +2.7V to +3.6V		**7**	ns (min)
		V_A = +4.75V to +5.25V		**5**	ns (min)
t_{DIS}	SCLK Falling Edge to SDATA High Impedance (4)	V_A = +2.7V to +3.6V		**25** **6**	ns (max) ns (min)
		V_A = +4.75V to +5.25V		**25** **5**	ns (max) ns (min)
$t_{POWER-UP}$	Power-Up Time from Full Power-Down		1		µs

(1) Data sheet min/max specification limits are specified by design, test, or statistical analysis.
(2) Measured with the timing test circuit shown in Figure 1 and defined as the time taken by the output signal to cross 1.0V.
(3) Measured with the timing test circuit shown in Figure 1 and defined as the time taken by the output signal to cross 1.0V or 2.0V.
(4) t_{DIS} is derived from the time taken by the outputs to change by 0.5V with the timing test circuit shown in Figure 1. The measured number is then adjusted to remove the effects of charging or discharging the output capacitance. This means that t_{DIS} is the true bus relinquish time, independent of the bus loading.

Timing Diagrams

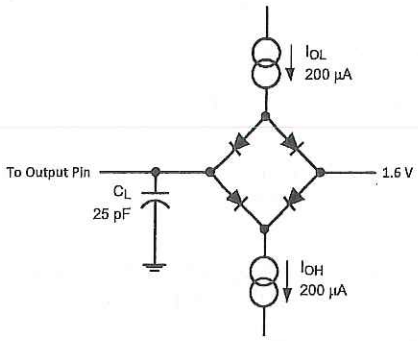


Figure 1. Timing Test Circuit

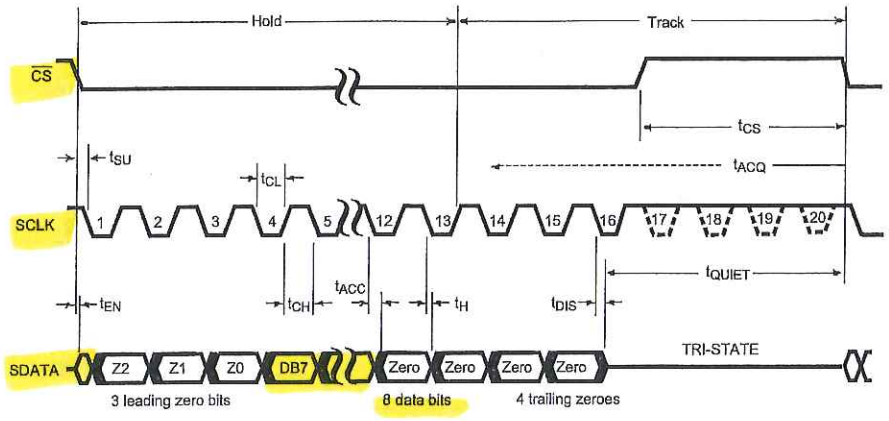


Figure 2. ADC081S021 Serial Timing Diagram

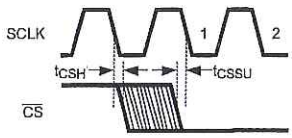


Figure 3. SCLK and $\overline{CS}$ Timing Parameters

Specification Definitions

ACQUISITION TIME is the time required to acquire the input voltage. That is, it is time required for the hold capacitor to charge up to the input voltage. Acquisition time is measured backwards from the falling edge of $\overline{CS}$ when the signal is sampled and the part moves from track to hold. The start of the time interval that contains T_{ACQ} is the 13th rising edge of SCLK of the previous conversion when the part moves from hold to track. The user must ensure that the time between the 13th rising edge of SCLK and the falling edge of the next $\overline{CS}$ is not less than T_{ACQ} to meet performance specifications.

APERTURE DELAY is the time after the falling edge of $\overline{CS}$ when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC081S021 to convert the input voltage to a digital word. This is from the falling edge of $\overline{CS}$ when the input signal is sampled to the 16th falling edge of SCLK when the SDATA output goes into TRI-STATE.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC081S021 of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal (V_{REF} − 1 LSB), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from

MODES OF OPERATION

The ADC has two possible modes of operation: normal mode, and shutdown mode. The ADC enters normal mode (and a conversion process is begun) when $\overline{CS}$ is pulled low. The device will enter shutdown mode if $\overline{CS}$ is pulled high before the tenth falling edge of SCLK after $\overline{CS}$ is pulled low, or will stay in normal mode if $\overline{CS}$ remains low. Once in shutdown mode, the device will stay there until $\overline{CS}$ is brought low again. By varying the ratio of time spent in the normal and shutdown modes, a system may trade-off throughput for power consumption, with a sample rate as low as zero.

Normal Mode

The fastest possible throughput is obtained by leaving the ADC in normal mode at all times, so there are no power-up delays. To keep the device in normal mode continuously, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK after the start of a conversion (remember that a conversion is initiated by bringing $\overline{CS}$ low).

If $\overline{CS}$ is brought high after the 10th falling edge, but before the 16th falling edge, the device will remain in normal mode, but the current conversion will be aborted, and SDATA will return to TRI-STATE (truncating the output word).

Sixteen SCLK cycles are required to read all of a conversion word from the device. After sixteen SCLK cycles have elapsed, $\overline{CS}$ may be idled either high or low until the next conversion. If $\overline{CS}$ is idled low, it must be brought high again before the start of the next conversion, which begins when $\overline{CS}$ is again brought low.

After sixteen SCLK cycles, SDATA returns to TRI-STATE. Another conversion may be started, after t_{QUIET} has elapsed, by bringing $\overline{CS}$ low again.

Shutdown Mode

Shutdown mode is appropriate for applications that either do not sample continuously, or it is acceptable to trade throughput for power consumption. When the ADC is in shutdown mode, all of the analog circuitry is turned off.

To enter shutdown mode, a conversion must be interrupted by bringing $\overline{CS}$ high anytime between the second and tenth falling edges of SCLK, as shown in Figure 23. Once $\overline{CS}$ has been brought high in this manner, the device will enter shutdown mode, the current conversion will be aborted and SDATA will enter TRI-STATE. If $\overline{CS}$ is brought high before the second falling edge of SCLK, the device will not change mode; this is to avoid accidentally changing mode as a result of noise on the $\overline{CS}$ line.

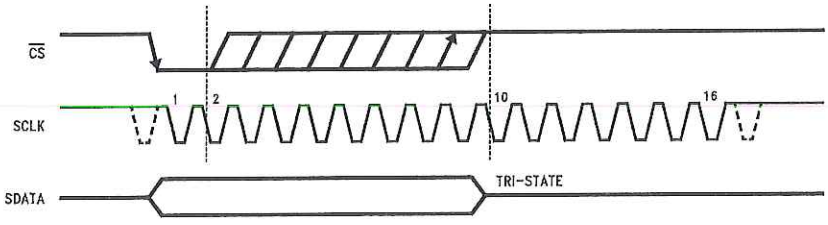


Figure 23. Entering Shutdown Mode

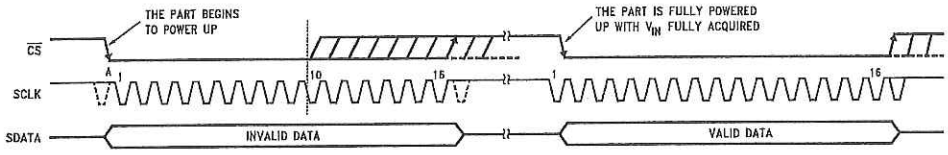


Figure 24. Entering Normal Mode

To exit shutdown mode, bring $\overline{CS}$ back low. Upon bringing $\overline{CS}$ low, the ADC will begin powering up (power-up time is specified in the Timing Specifications table). This microsecond of power-up delay results in the first conversion result being unusable. The second conversion performed after power-up, however, is valid, as shown in Figure 24.