HW/SW co-design of Face Detection & Recognition on Virtual Platform

Mi-Young Lee, Young-Seok Baek, Seong-Min Kim, Hyuk Kim, Bon-Tae Koo, Joo-Hyun Lee
Electronics and Telecommunications Research Institute, Daejeon, Korea
{sharav, ysbaek, smkim, haggy, koobt, juehyun}@etri.re.kr

Abstract

In this paper, we present a FPGA implementation of face detection hardware (HW) and also address face recognition software (SW) on virtual platform. We apply very deeply-cascaded classifier which is composed of heterogeneous feature-classifiers to capture various characteristics of images. We use 2 step classifiers, the first searches for the coarse features and the second for the fine features. Both of the features are composed of HAAR like feature classifiers and Gabor classifiers while the 1st coarse classifier uses 700 classifiers and the 2nd uses 1350 classifiers. For the very-deeply cascaded face detector, we developed dedicated HW engine to process a feature per a cycle. The face detection is implemented in a Xilinx Virtex-7 device. For face recognition SW co-design, we also developed a virtual platform (VP). We co-verified face detection engine and face recognition SW running on a conventional operating system (OS) using the VP. Face detector operates over 30 frame/s at 50 MHz frequency for real-time applications up-to 640x480 size image.

Keywords: Face Detection, Face Recognition

1. Introduction

Face detection and recognition system has gotten much interest recently because in the various applications the technique is highly demanded.

For the various sized-face detection, pyramid image processing is mandatory and computation load is huge. For the HD image, the computation load gets much larger.

In 2012, S. Jin implemented a pipelined data-path hardware with 307 frames/s throughput for standard VGA scene [1]. N. Wang proposed a multi-face detection system which can operates in a frame rate of 30fps [2]. C. Kumar presented the generator storing the integral window [3]. S. Kumar realized a hybrid FPGA-GPU based embedded platform [4].

To solve computational complexity, we used very deep-cascaded feature classifier which shows powerful classification accuracy and have regular scheme likely to be implemented as HW efficiently.

This paper organized as follows. In section 2, we present the hardware architecture. Experimental results are described in Section 3. Finally conclusions are drawn and the further works are discussed in Section 4.

2. System Architecture

Figure 1 shows the face detection algorithm flow. It includes image scaler, integral image generator, coarse-grain classifier, fine-grain classifier, face grouper and average face generator. The coarse-grained classifier searches for coarse-grained scale with stride 5 having 700 cascaded feature classifiers.

The fine-grained classifier searches for fine-grained scale with stride 1 having 1350 cascaded feature classifiers. Both of them are composed of HAAR like feature classifiers and Gabor classifiers.

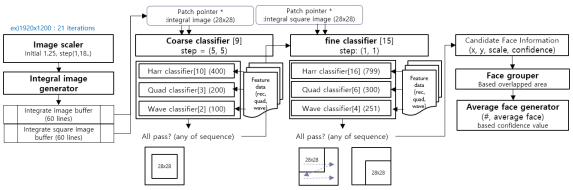

Figure 1. Face Detector Architecture

The face detection accuracy of algorithm is 99.7% using the extended Multi Modal Verification for Teleservices and Security applications (M2VTS) database. The recognition accuracy using same DB is 95.1%.

Figure 1 shows the face detector architecture. It is composed of gray convertor, resizer, integral image generator, candidate patch controller, classifiers and face grouper. For the throughput, we use parallelized searching engine for image pyramids by 4.

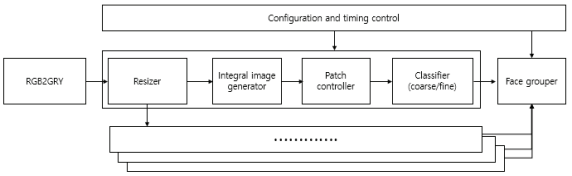

Figure 2. Face Detector Architecture

978-1-5090-2743-9/16/$31.00 ©2016 IEEE

Figure 3 shows the classifier architecture. It is composed of HAAR classifier, HAAR2 classifier and Gabor classifier, each of which has own lookup table for feature parameters. After passing all coarse classifiers, a patch candidate is pushed to fine classifier.

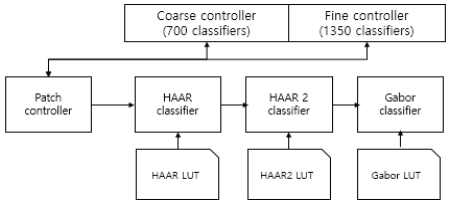

Figure 3. Classifier Architecture

3. Experimental Results

Figure 4 shows the HW/SW co-design scheme using a VP. We target developed face detection engine into FPGA device. We implement the VP which represents ARM's Versatile Express development board. On the VP, we port Ubuntu-nano 13.08, commonly used in the embedded system. Recognition SW is developed on this VP environment. Through bus functional model (BFM) connector's transaction level model (TLM) which models USB3.0, we implement VP connected with face detection FPGA board.

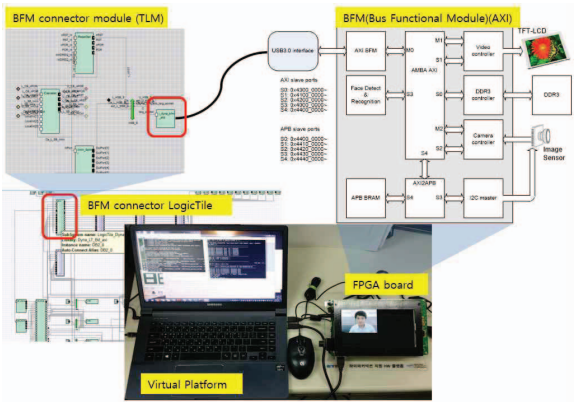

Figure 4. HW-SW co-design scheme using the VP and FPGA board

We use Xilinx XC7V2000T device to verify the face detection hardware engine and design the floating/fixed modeling using C/C++ programming. The hardware is descripted using System Verilog and synthesized using Xilinx Vivado 2015.3. Table I presents a utilization of hardware.

Table 1: Hardware utilization

Component	Available	Used	Utilization (%)
Slice LUTs	1,221,600	302,497	24.8
Slice Registers	2,443,200	138,189	5.6
Block RAMs	1,292	969	75
DSPs	2,160	622	28.8

The total latency of the proposed design is 101 msec from input of the image data to a face-detected output. The estimated maximum clock cycle is 108 MHz. Face detector operates over 30 frame/s at 50 MHz frequency for real-time applications up-to 640x480 size image.

4. Conclusion

In this paper, we presented the hardware engine for fast face detection with efficient area. The hard ware acceleration including resizer, integral image generator, candidate patch controller, classifiers and face grouper which can process a single image in 101 msec. Therefore the overall system can operates 30 frame/s at 50MHz for real time processing.

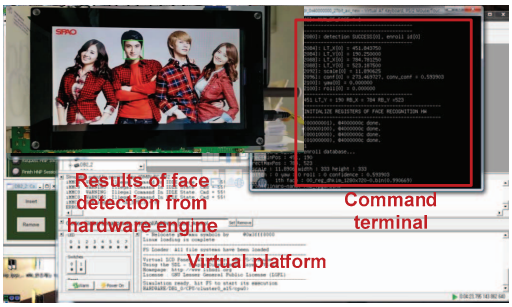

Figure 5. Test bed to verify the fast face detector

ACKNOWLEDGMENT

This work was supported by Institute for Information & communications Technology Promotion(IITP) grant funded by the Korea government(MSIP) (No. B0101-15-0155, The Core Technology Development of SW-SoC Convergence Platform for Hyper-Connection Services among Smart Devices based on Heterogeneous Multi-core Clusters)

References

[1] S. Jin, et al. "Design and implementation of a pipelined datapath for high-speed face detection using FPGA." *IEEE Transactions on Industrial Informatics* 8.1, pp. 158-167, 2012

[2] N. Wang, et al. "A real-time multi-face detection system implemented on FPGA." International Symposium on Intelligent Signal Processing and Communications Systems (ISPACS), 2012

[3] C. Kumar, et al. "A novel architecture for dynamic Integral Image generation for Haar-based face detection on FPGA." TENCON Region 10 Conference, 2014.

[4] S. Rethinagiri, et al. "An energy efficient hybrid FPGA-GPU based embedded platform to accelerate face recognition application." Symposium on Low-Power and High-Speed Chips, 2015.