

# **Product Specification**

Product Name: VGM128064C9A06

**Product Code: M01536** 

	Customer			
		Approved by Customer		
Approved	Date:			

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# REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
D01	Initial release.	2014-03-03	



#### 1 Overview

VGM128064C9A06 is an area color OLED display module with 128×64 dot matrix. The characteristics of this display module are high brightness, self-emission, high contrast ratio, slim/thin outline, wide viewing angle, wide temperature range, and low power consumption.

#### 2 Features

➤ Display Color: Yellow & Blue

Dot Matrix:128×64Driver IC: SSD1306ZC

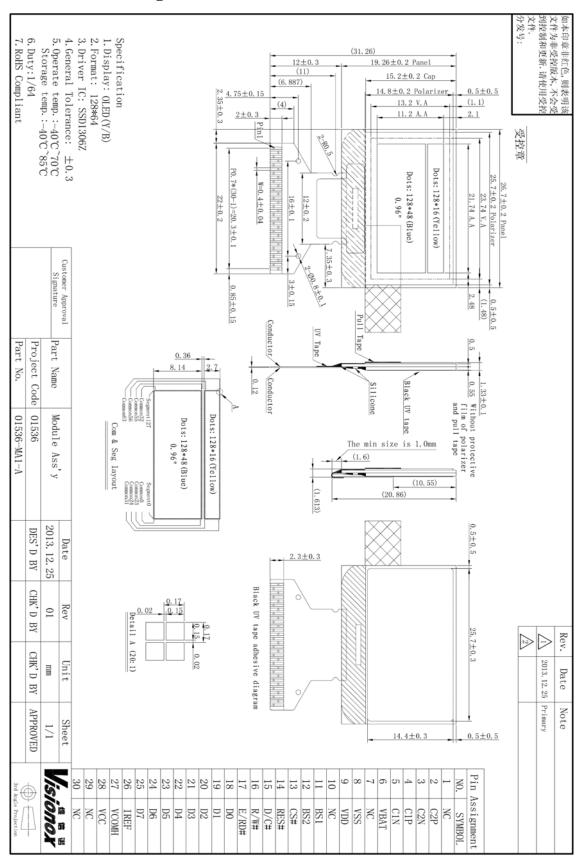
Interface: 8-bit 6800、8-bit 8080、I<sup>2</sup>C 、 4-Wire SPI
 Wide range of operating temperature: -40°C to 70°C

#### 3 Mechanical Data

NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128(W)×64(H)	-
2	Dot Size	0.15(W)×0.15 (H)	mm <sup>2</sup>
3	Dot Pitch	0.17(W)×0.17 (H)	mm <sup>2</sup>
4	Aperture Rate	78	%
5	Active Area	21.74(W)×11.2 (H)	$mm^2$
6	Panel Size	26.7(W)×19.26(H)×1.05(T)	mm <sup>3</sup>
7	Module Size	26.7(W)×31.26(H)×1.33(T)	mm <sup>3</sup>
8	Diagonal A/A Size	0.96	inch
9	Module Weight	1.28±10%	gram



# 4 Mechanical Drawing





# **5** Module Interface

PIN NO.	PIN NAME	DESCRIPTION					
1	NC	No Connection	1.				
2	C2P	The Div Court		C	41		
3	C2N	The Pin for ch	arge pump capacitor	, Connect to each o	ther with a capacitor.		
4	C1P	The Din Const.		C	41		
5	C1N	The Pin for ch	The Pin for charge pump capacitor; Connect to each other with a capacitor.				
6	VBAT	Power supply	for charge pump reg	ulator circuit.			
		Status	VBAT	VDD	VCC		
		Enable	Connect to	Connect to	A capacitor should be		
		charge	external VBAT	external VCC	connected between this pin		
		pump	source	source	and VSS		
		Disable	Keep float	Connect to	Connect to external VCC		
		charge		external VCC	source		
		pump		source			
7	NC	No Connection	1.				
8	VSS	Ground.					
9	VDD		oin for core logic op	eration.			
10	NC	No Connection	1.				
11	BS1	Table 5-1					
12	BS2						
13	CS#	Chip Select, ac					
	22011		et signal input. Whe	n the pin is pulled I	OW, initialization of the chip is		
14	RES#	executed.	HOH (	TIDD) 1 :			
			HIGH (i.e. connect t				
		This is Data/Command control pin. When it is pulled HIGH (i.e. connect to VI					
15	D/C#	the data at D[7:0] is treated as data. When it is pulled LOW, the data at D[7:0] will be					
		transferred to the command register. In I <sup>2</sup> C mode, this pin acts as SA0 for slave address selection.					
			write control input p				
					s pin will be used as Read/Write		
					t when this pin is pulled HIGH		
16	R/W#		VDD) and write m		t when this pin is puned fright		
10	10 11				e the Write (WR#) input. Data		
					W and the chip is selected.		
					be connected to VSS.		
					s pin will be used as the Enable		
					pin is pulled HIGH (i.e. connect		
			he chip is selected.		- ` ` ` ` ` ` `		
17	E/RD#	When connect	ing to an 8080-serie	s microprocessor, th	nis pin receives the Read (RD#)		
		signal. Read of	peration is initiated	when this pin is pul	led LOW and the chip is		
		selected.	2				
					be connected to VSS.		
			t bi-directional data	bus to be connected	d to the microprocessor's data		
		bus.					
18~25	D0~D7	When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC.					
			When I <sup>2</sup> C mode is selected, D2, D1 should be tied together and serve as SDAout,				
26	IDEE	SDAin in application and D0 is the serial clock input, SCL.  Segment output current reference pin					
26	IREF				annaitar ta VCC		
27	VCOMH VCC		al deselected voltage		гсарасног ю у 88.		
28	NC		for panel driving vo	nage.			
29~30	NU	No Connection	l.				



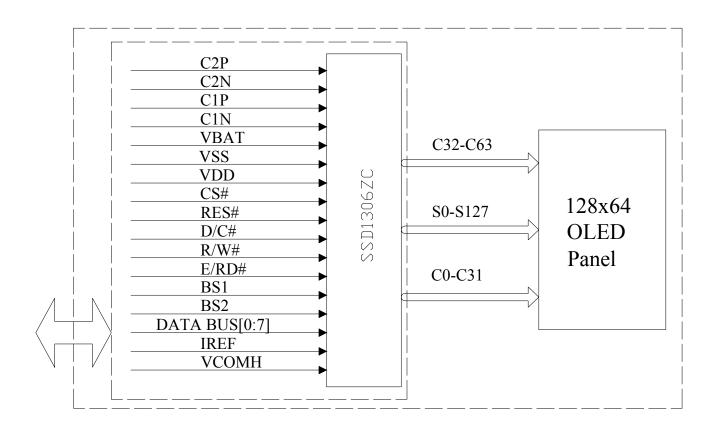
Table 5-1: MCU Bus Interface Pin Selection

Pin Name	$I^2C$	6800	8080	4-SPI
BS1	1	0	1	0
BS2	0	1	1	0

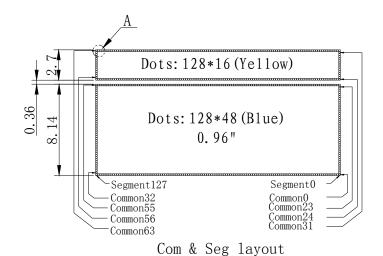


# 6 Function Block Diagram

#### 6.1 Function Block Diagram



#### 6.2 Panel Layout Diagram





# 7 Absolute Maximum Ratings

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
Logic supply voltage	VDD	-0.3	4	V	IC maximum rating
Charge Pump Regulator Supply Voltage	VBAT	-0.3	5.0	V	IC maximum rating
OLED Operating voltage	VCC	0	16	V	IC maximum rating
Operating Temp.	Тор	-40	70	$^{\circ}$	-
Storage Temp	Tstg	-40	85	$^{\circ}$ C	-

Note (1): All of the voltages are on the basis of "VSS = 0V".

Note (2): Permanent breakage of module may occur if the module is used beyond the maximum rating. The module can be normal operated under the conditions according to Section 8 "Electrical Characteristics". Malfunctioning of the module may occur and the reliability of the module may deteriorate if the module is used beyond the conditions.

#### 8 Electrical Characteristics

#### 8.1 DC Electrical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	ТҮРЕ	MAX	UNIT
Logic Supply Voltage	VDD	22±3°C, 55±15%R.H	1.65	3.0	3.3	V
OLED Driver Supply Voltage (Supply Externally)	VCC	22±3°C, 55±15%R.H	7	7.2	7.5	V
OLED Driver Supply Voltage (Generated by Internal DC/DC)	VCC	22±3°C, 55±15%R.H	7	7.2	7.5	V
Charge Pump Regulator Supply Voltage	VBAT	22±3°C, 55±15%R.H	3.3	3.7	4.2	V
High-level Input Voltage	$V_{\mathrm{IH}}$	-	$0.8 \times \text{VDD}$	-	-	V
Low-level Input Voltage	$V_{\mathrm{IL}}$	-	-	-	$0.2 \times \text{VDD}$	V
High-level Output Voltage	$V_{\mathrm{OH}}$	-	$0.9 \times VDD$	-	-	V
Low-level Output Voltage	$V_{\mathrm{OL}}$	-	-	-	$0.1 \times VDD$	V

Note: The VCC input must be kept in a stable value; ripple and noise are not allowed.





## **8.2** Electro-optical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	ТҮРЕ	MAX	UNIT
Normal Mode Brightness	$L_{br}$	All pixels ON(1) (VCC generated by internal DC/DC)	80	100	-	cd/m <sup>2</sup>
ICC,Sleep mode Current	ICC,SLEEP	VDD = 1.65V~3.3V, VCC = 7V~15V Display OFF, No panel attached	-	-	20	uA
IDD,Sleep mode Current	IDD,SLEEP	VDD = 1.65V~3.3V, VCC = 7V~15V Display OFF, No panel attached	-	-	20	uA
Normal Mode Power Consumption	Pt	All pixels ON(1)	-	111	133.2	mW
C.I.E(Blue)	(x)		0.13	0.16	0.19	-
C.I.E(Blue)	(y)	x,y(CIE1931)	0.24	0.27	0.30	-
C.I.E(Yellow)	(x)	x,y(CIL1751)	0.48	0.51	0.54	-
C.I.E( Ichow)	(y)		0.45	0.48	0.51	-
Dark Room Contrast	CR	-	≥2000:1	-	-	-
Response Time	-	-	-	10	-	μs
View Angle	-	-	≥160	-	-	Degree

Note(1): Normal Mode test conditions are as follows:

- Driving voltage: 7.2V(VCC Supplied Externally) or VBAT:3.7V(VCC Generated by Internal DC/DC).

- Contrast setting : 0XCF

Frame rate: 105HzDuty setting: 1/64



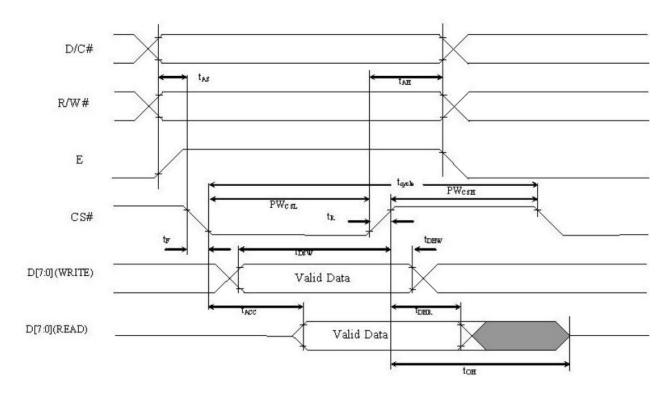
#### **8.3** AC Electrical Characteristics

#### (1)6800-Series MPU Parallel Interface Timing Characteristics

 $(VDD - VSS = 1.65V \text{ to } 3.3V, TA = 25^{\circ}C)$ 

Symbol	Parameter	Min	Тур	Max	Unit
$t_{\rm cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	0	-	-	ns
t <sub>AH</sub>	Address Hold Time	0	-	-	ns
$t_{\rm DSW}$	Write Data Setup Time	40	-	-	ns
$t_{\rm DHW}$	Write Data Hold Time	7	-	-	ns
t <sub>DHR</sub>	Read Data Hold Time	20	-	-	ns
t <sub>OH</sub>	Output Disable Time	-	-	70	ns
t <sub>ACC</sub>	Access Time	-	-	140	ns
$PW_{CSL}$	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
$PW_{CSH}$	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
$t_R$	Rise Time	-	-	40	ns
t <sub>F</sub>	Fall Time	-	-	40	ns

#### 6800-series MCU parallel interface characteristics





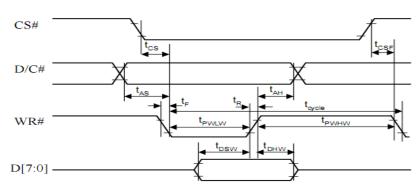
#### (2)8080-Series MPU Parallel Interface Timing Characteristics

 $(VDD - VSS = 1.65V \text{ to } 3.3V, TA = 25^{\circ}C)$ 

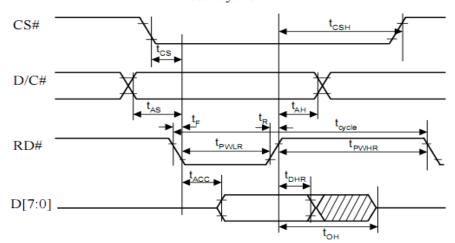
Symbol	Parameter	Min	Тур	Max	Unit
t <sub>cycle</sub>	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	10	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{ m DSW}$	Write Data Setup Time	40	-	-	ns
$t_{ m DHW}$	Write Data Hold Time	7	-	-	ns
t <sub>DHR</sub>	Read Data Hold Time	20	-	-	ns
t <sub>OH</sub>	Output Disable Time	-	-	70	ns
t <sub>ACC</sub>	Access Time	-	-	140	ns
t <sub>PWLR</sub>	Read Low Time	120	-	-	ns
$t_{\mathrm{PWLW}}$	Write Low Time	60	-	-	ns
t <sub>PWHR</sub>	Read High Time	60	-	-	ns
$t_{\mathrm{PWHW}}$	Write High Time	60	-	-	ns
t <sub>R</sub>	Rise Time	-	-	40	ns
t <sub>F</sub>	Fall Time	-	-	40	ns
t <sub>CS</sub>	Chip select setup time	0	-	-	ns
t <sub>CSH</sub>	Chip select hold time to read signal	0	-	-	ns
t <sub>CSF</sub>	Chip select hold time	20	-	-	ns

#### 8080-series parallel interface characteristics

#### Write Cycle



#### Read cycle



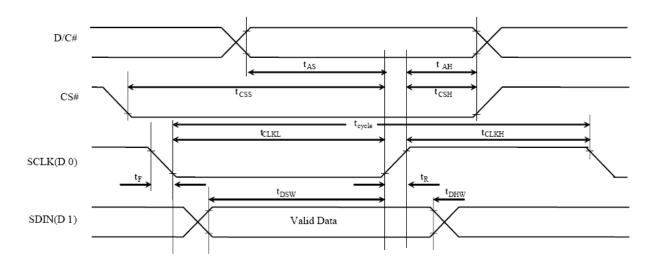


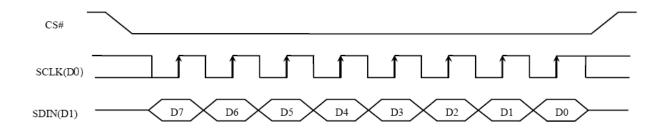
#### (3)4-Wire Series Interface Timing Characteristics

 $(VDD - VSS = 1.65V \text{ to } 3.3V, TA = 25^{\circ}C)$ 

Symbol	Parameter	Min	Тур	Max	Unit
t <sub>cycle</sub>	Clock Cycle Time	100	-	-	ns
t <sub>AS</sub>	Address Setup Time	15	-	-	ns
t <sub>AH</sub>	Address Hold Time	15	-	-	ns
tcss	Chip Select Setup Time	20	-	-	ns
t <sub>CSH</sub>	Chip Select Hold Time	10	-	-	ns
t <sub>DSW</sub>	Write Data Setup Time	15	-	-	ns
$t_{\mathrm{DHW}}$	Write Data Hold Time	15	-	-	ns
t <sub>CLKL</sub>	Clock Low Time	20	-	-	ns
tclkh	Clock High Time	20	-	-	ns
t <sub>R</sub>	Rise Time	-	-	40	ns
t <sub>F</sub>	Fall Time	-	-	40	ns

#### 4-wire Serial interface characteristics





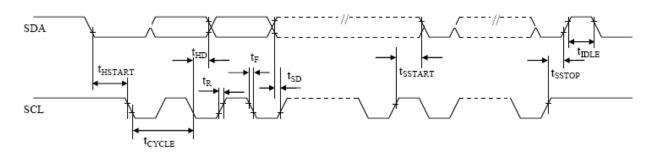


# (4) I<sup>2</sup>C Interface Timing Characteristics

 $(VDD - VSS = 1.65V \text{ to } 3.3V, TA = 25^{\circ}C)$ 

Symbol	Parameter	Min	Тур	Max	Unit
t <sub>cycle</sub>	Clock Cycle Time	2.5	-	-	us
t <sub>HSTART</sub>	Start condition Hold Time	0.6	-	-	us
t <sub>HD</sub>	Data Hold Time (for "SDA <sub>OUT</sub> " pin)	0	-	-	ns
	Data Hold Time (for "SDA <sub>IN</sub> " pin)	300	-	-	ns
t <sub>SD</sub>	Data Setup Time	100	-	-	ns
t <sub>SSTART</sub>	Start condition Setup Time (Only relevant for a repeated Start condition)		-	-	us
t <sub>SSTOP</sub>	Stop condition Setup Time	0.6	-	-	us
t <sub>R</sub>	Rise Time for data and clock pin	-	-	300	ns
t <sub>F</sub>	Fall Time for data and clock pin	-	-	300	ns
t <sub>IDLE</sub>	Idle Time before a new transmission can start	1.3	-	-	us

## I<sup>2</sup>C Interface Timing Characteristics



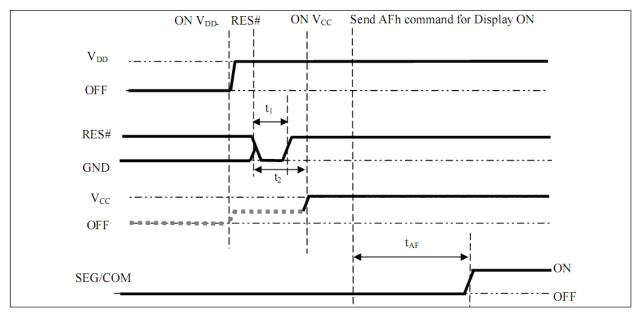


#### 9 Functional Specification and Application Circuit

#### 9.1 Power ON and Power OFF Sequence with External VCC

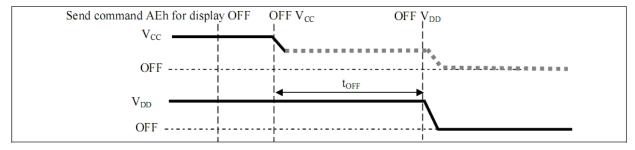
#### **Power ON Sequence:**

- 1. Power ON VDD
- 2. After VDD become stable, set RES# pin LOW (logic low) for at least  $3us(t_1)^{(4)}$  and then HIGH (logic high).
- 3. After set RES# pin LOW (logic low), wait for at least 3us (t<sub>2</sub>). Then Power ON VCC<sup>(1)</sup>
- 4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after  $100 ms(t_{AF})$ .



#### **Power OFF Sequence:**

- 1. Send command AEh for display OFF.
- 2. Power OFF VCC<sup>(1),(2),(3)</sup>.
- 3. Power OFF VDD after t<sub>OFF</sub>. (5) (Typical t<sub>OFF</sub>=100ms)



#### Note:

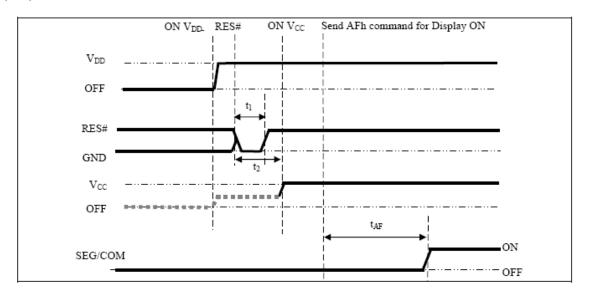
- (1)Since an ESD protection circuit is connected between VDD and VCC, VCC becomes lower than VDD whenever VDD is ON and VCC is OFF as shown in the dotted line of VCC in above figures.
- (2) V<sub>CC</sub> should be kept float (disable) when it is OFF.
- (3) Power Pins(VDD, VCC) can never be pulled to ground under any circumstance.
- (4) The register values are reset after  $t_1$ .
- (5) VDD should not be Power OFF before VCC Power OFF



#### 9.2 Power ON and OFF sequence with Charge Pump Application

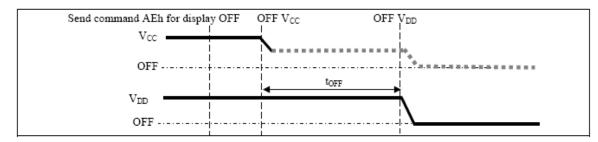
Power ON sequence:

- 1. Power ON VDD
- 2. After VDD become stable, set RES# pin LOW (logic low) for at least 3us (t1) <sup>(4)</sup> and then HIGH (logic high).
- 3. After set RES# pin LOW (logic low), wait for at least 3us (t2). Then Power ON VCC. (1)
- 4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (tAF).



Power OFF sequence:

- 1. Send command AEh for display OFF.
- 2. Power OFF VCC. (1), (2), (3)
- 3. Power OFF VDD after tOFF. (5) (Typical tOFF=100ms)



#### Note:

(1) Since an ESD protection circuit is connected between VDD and VCC, VCC becomes lower than VDD whenever VDD is

ON and VCC is OFF as shown in the dotted line of VCC in above figures. (2)

VCC should be kept float (i.e. disable) when it is OFF.

- (3) Power Pins (VDD, VCC) can never be pulled to ground under any circumstance.
- (4) The register values are reset after t1.
- (5) VDD should not be Power OFF before VCC Power OFF.

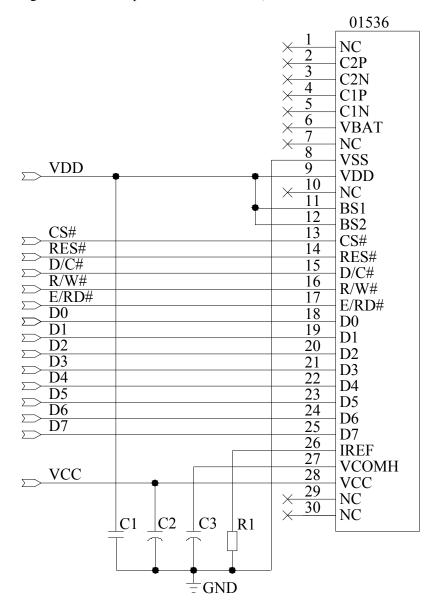


#### 9.3 Application Circuit

9.3.1 Under external VCC Mode, the charge Pump Setting (8Dh) must be set as follow:

8Dh:Charge Pump Setting 10h:Disable Charge Pump

(1). The configuration for 8080-parallel interface mode, external VCC is shown in the following diagram



Pin connected to MCU interface: D[0:7], E/RD#, R/W#, D/C#, RES#, CS#

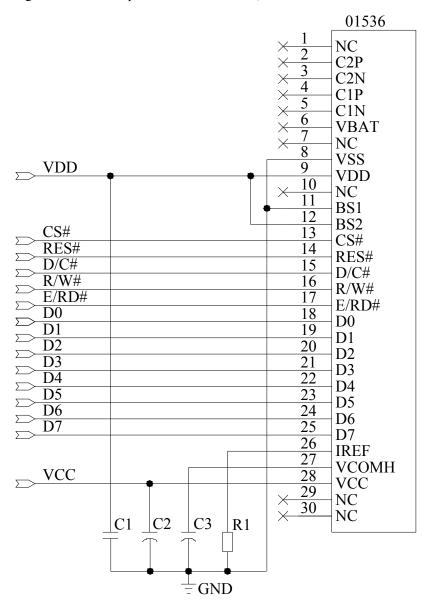
#### **Recommended components**

 $C1: 0.1 uF-0603-X7R\pm10\%.RoHS$ 

C2,C3: 4.7µF/25V.RoHS (Tantalum Capacitors)



(2). The configuration for 6800-parallel interface mode, external VCC is shown in the following diagram



Pin connected to MCU interface: D[0:7], E/RD#, R/W#, D/C#, RES#, CS#

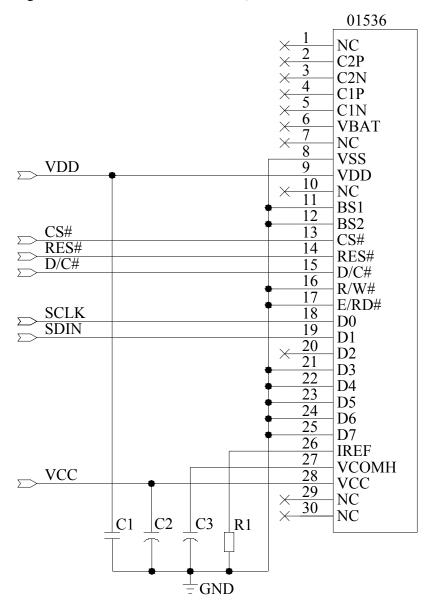
#### **Recommended components**

 $C1: 0.1 uF-0603-X7R\pm10\%.RoHS$ 

C2,C3: 4.7µF/25V.RoHS (Tantalum Capacitors)



(3). The configuration for 4-wire-SPI interface mode, external VCC is shown in the following diagram



Pin connected to MCU interface: SDIN, SCLK, D/C#, RES#, CS#

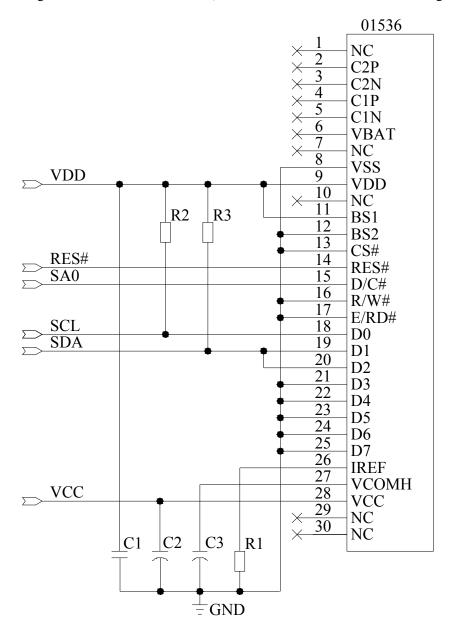
#### **Recommended components**

 $C1: 0.1 uF-0603-X7R\pm10\%.RoHS$ 

C2,C3: 4.7µF/25V.RoHS (Tantalum Capacitors)



(4). The configuration for I<sup>2</sup>C interface mode, external VCC is shown in the following diagram



Pin connected to MCU interface: SCL,SDA,SA0, RES#

SA0	Slave address
0	0X78
1	0X7A

#### **Recommended components**

 $C1: 0.1 uF-0603-X7R\pm10\%.RoHS$ 

C2,C3: 4.7µF/25V.RoHS (Tantalum Capacitors)

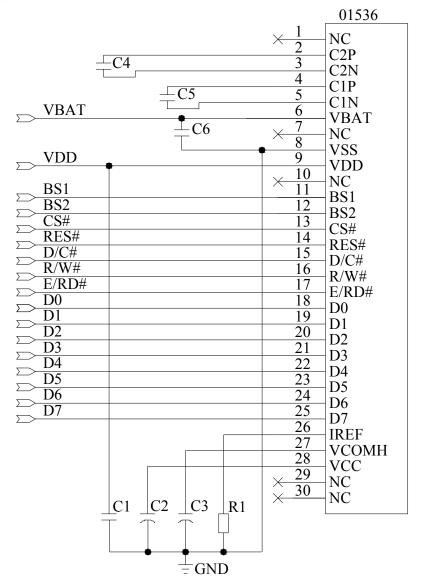
R1: 0603 1/10W +/-5% 390K ohm.RoHS R2,R3: 0603 1/10W +/-5% 10K ohm.RoHS



9.3.2 Under Internal DC/DC Mode, the charge Pump Setting (8Dh) must be set as follow:

8Dh:Charge Pump Setting 14h:Enable Charge Pump

The configuration for VCC Generated by Internal DC/DC Circuit is shown in the following diagram:



MCU interface Selection: BS1,BS2

Pin connected to MCU interface: D[0:7], E/RD#, R/W#, D/C#, RES#, CS#

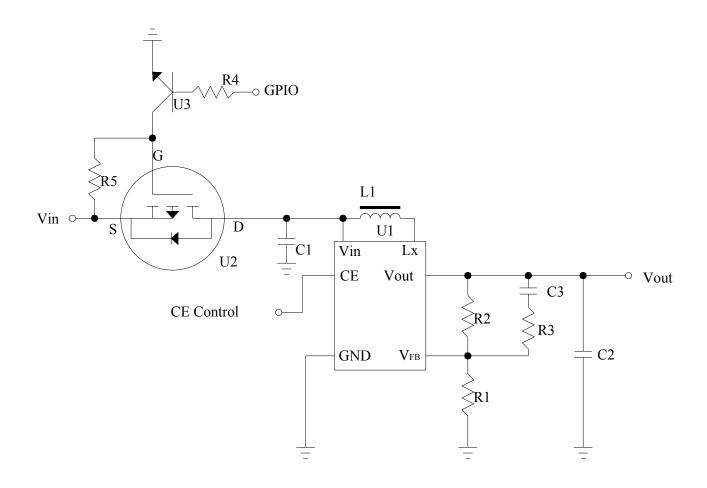
#### **Recommended components**

C1, C4, C5, C6: 1uF-0603-X7R±10%.RoHS

C2,C3: 4.7µF/25V.RoHS (Tantalum Capacitors)



## 9.4 External DC-DC application circuit



## Recommend component

The C1 : 1 uF-0603-X7R±10%.RoHS

The C2 : 1 uF-0603-X7R±10%.RoHS

The C3 : 220pF-0603-X7R±10%.RoHS

The R1 : 0603 1/10W +/-5% 10Kohm.RoHS

The R2 : 0603 1/10W +/-5% 62Kohm.RoHS

The R3 : 0603 1/10W +/-5% 2Kohm.RoHS

The R4 : 0603 1/10W +/-5% 1Kohm.RoHS

The R5 : 0603 1/10W +/-5% 10Kohm.RoHS

The L1 : 22uH

The U1 : R1200

The U2 : FDN338P

The U3 : 8050



#### 9.5 Display Control Instruction

Refer to SSD1306ZC IC Specification.

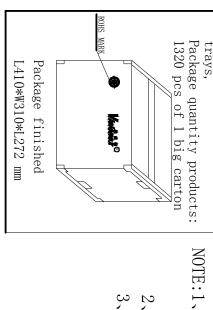
#### 9.6 Recommended Software Initialization

In order to ensure the reliability and stability of the module, the module must initialized use the following code, Malfunctioning of the module may occur and the reliability of the module may deteriorate if the module is used beyond the initialize code.

```
void Init IC()
    Write Command(0xAE);
                              //Set Display Off
    Write Command(0xD5);
                              //Display divide ratio/osc. freq. mode
    Write Command(0x80);
    Write Command(0xA8);
                              //Multiplex ration mode:63
    Write Command(0x3F);
    Write Command(0xD3);
                              //Set Display Offset
    Write Command(0x00);
    Write Command(0x40);
                              //Set Display Start Line
    Write Command(0x8D);
                              //Charge Pump Setting
    Write Command(0x14);
                              //Enable charge pump during display on
    //Write Command(0x10);
                              //Disable charge pump(RESET)
    Write Command(0xA1);
                               //Segment Remap
    Write Command(0xC8);
                              //Set COM Output Scan Direction
    Write Command(0xDA);
                              //Common pads hardware: alternative
    Write Command(0x12);
    Write_Command(0x81);
                              //Contrast control
    Write Command(0xCF);
    Write Command(0xD9);
                              //Set pre-charge period
    Write Command(0xF1);
    Write Command(0xDB);
                              //VCOM deselect level mode
    Write Command(0x40);
                              //Set Vcomh
                              //Set Entire Display On/Off
    Write Command(0xA4);
    Write Command(0xA6);
                              //Set Normal Display
    Clear Screen();
    Write Command(0xAF);
                              //Set Display On
}
```



# **10** Package Specification



marking at 🕲

the inner carton and master carton need adhesive new RoHS

needs

with

the

RoHS making,

2 ယ

Fill up the gap

with

tray.

If the customer has special

The inner carton

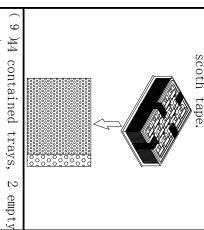
and

master carton must

be

sealed with

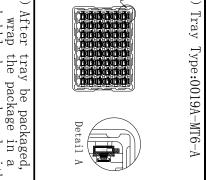
adhesive tape.



oubble bag and seal with

6

TRAY



Controlled Seal

Packing Process(1)~(9)

2

) order(1),

 $\bigcirc$ 

Use vaccum bag to package

the tray and add 5 bags

fix trays with tape





180°













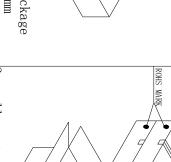






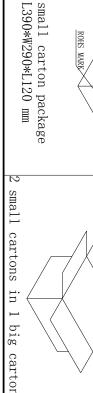


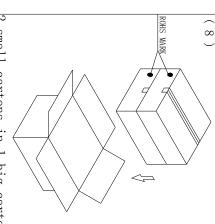




ROHS MARI

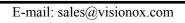












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#### 11 Reliability

#### 11.1 Reliability Test

NO.	ITEM	CONDITION	QUANTITY
1	High Temperature (Non-operation)	85℃,240hrs	4
2	Low Temperature (Non-operation)	-40°C,240hrs	4
3	High Temperature (Operation)	70°C,240hrs	4
4	Low Temperature (Operation)	-40°C,240hrs	4
5	High Temperature / High Humidity (Operation)	60°C,90%RH,240hrs	4
6	Thermal shock (Non-operation)	-40 °C ~85 °C (-40 °C /30min;transit/3min;85 °C /30min;transit/3min) 1 cycle: 66min,30 cycles	4
7	Vibration	Frequency: 5~50Hz,0.5G Scan rate: 1 oct/min Time: 2 hrs/axis Test axis: X,Y, Z	1 Carton
8	Drop	Height: 100 cm Sequence: 1 angle, 3 edges and 6 faces	1 Carton

#### **Test and measurement conditions**

- 1. All measurements shall not be started until the specimens attain to temperature stability, the stable time is at least 15 minutes.
- 2. The degradation of polarizer is ignored for item 5.
- 3. The tolerance of temperature is  $\pm 3^{\circ}$ C, and the tolerance of relative humidity is  $\pm 5\%$ .

#### **Evaluation criteria**

- 1. The function test is OK.
- 2. No observable defects.
- 3. Luminance: ≥50% of initial value.
- 4. Current consumption: within  $\pm$  50% of initial value.

#### 11.2 Lifetime

End of lifetime is specified as 50% of initial brightness and the test pattern at operating condition is 50% alternating checkerboard.

ITEM	MIN	MAX	UNIT	CONDITION
Operation Life Time	20,000	-	hrs	100 cd/m <sup>2</sup> , 50% alternating checkerboard, 22±3°C, 55±15% RH

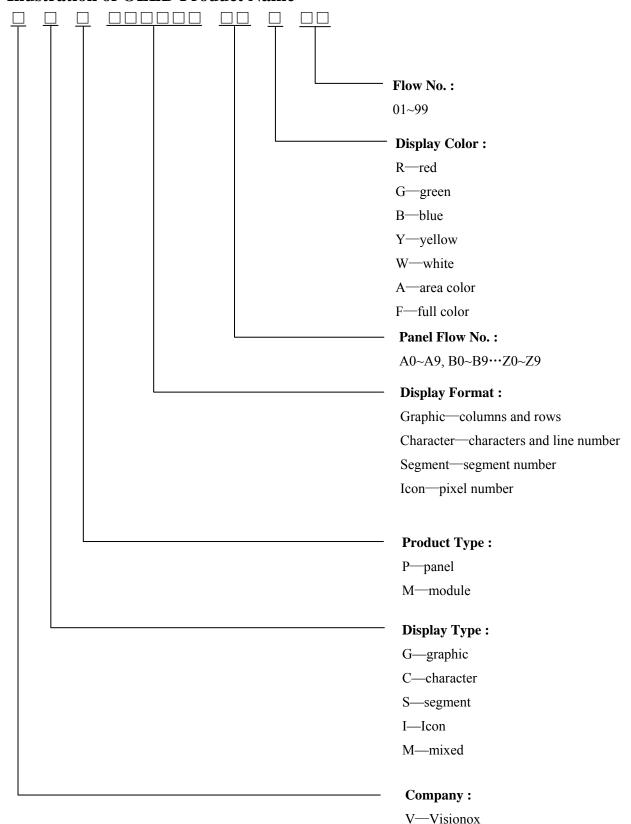
Note: The lifetime of yellow is 40,000 hours. The lifetime of blue is 20,000 hours.

#### 11.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 22±3°C; 55±15% RH.



#### 12 Illustration of OLED Product Name





# 13 Outgoing Quality Control Specifications

#### 13.1 Sampling Method

(1) GB/T 2828.1-2003/ISO2859-1: 1999, inspection level II, normal inspection, single sample inspection

(2) AQL: Major 0.65; Minor 1.0

#### 13.2 Inspection Conditions

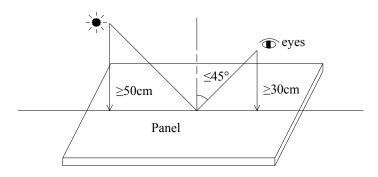
The environmental conditions for test and measurement are performed as follows.

Temperature: 22±3°C Humidity: 55±15%R.H Fluorescent Lamp: 30W

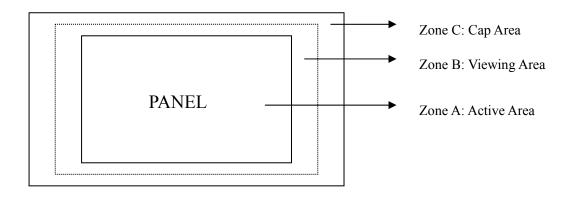
Distance between the Panel & Lamp: ≥50cm Distance between the Panel & Eyes: ≥30cm

Viewing angle from the vertical in each direction: ≤45°

(See the sketch below)



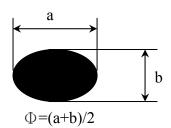
#### 13.3 Quality Assurance Zones

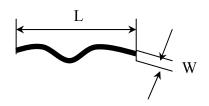




# 13.4 Inspection Standard

Definition of Φ&L&W (Unit: mm)





# I . Appearance Defects

NO.	ITEM	CRITERIA				CLASSIFICATION	
1	Polarizer Black or White spot, Dirty spot, Foreign matter, Dent on the polarizer	Average Diameter (mm) Φ≤0.15 0.15<Φ≤0.30 Φ>0.30	Zone	$\mathcal{E}$		Zone C	Minor
2	Scratch/line on the glass/Polarizer	Width (mm) W≤0.03 0.03 <w≤0.08 W&gt;0.08</w≤0.08 	Length (mm) L≤5.0	Accep Zone A Ignor 3	,B	Number Zone C Ignore	Minor
3	Polarizer Bubble			Minor			
4	Any Dirt & Scratch on Polarizer's Protective Film	Ignore for not affect the polarizer.				Minor	
5	Any Dirt on Cap Glass	Average Diameter (mm)  Φ≤0.5  0.5<Φ≤1.0  Φ>1.0		(mm)Acceptable Number $\Phi \leq 0.5$ Ignore $0.5 < \Phi \leq 1.0$ 3		Minor	

Propagation crack is not acceptable.  Propagation crack is not acceptable.  Propagation crack is not acceptable.  Minor    Feet   Feet	6	Glass Crack		Major
Temporaria   Tem			Propagation crack is not acceptable.	
Accept a≤2.0mm or b≤2.0mm, e≤t  8	7	Corner Chip		Minor
Teglass thickness  Accept  a≤1.5mm or b≤1.5mm, c≤t  Pad  Chip on Contact  Pad  Chip on Face of Display  Teglass thickness  Accept  a≤3.0mm or b≤1.5mm, c≤t (on the contact pin)  Teglass thickness  Accept  a≤1.5mm or b≤1.5mm, c≤t (outside of the contact pin)  Minor  Teglass thickness  Accept  a≤1.5mm or b≤1.5mm, c≤t  Accept  a≤1.5mm or b≤1.5mm, c≤t  a≤1.5mm or b≤1.5mm, c≤t  Accept			Accept	
Accept  a≤1.5mm or b≤1.5mm, c≤t  Pad  Chip on Contact Pad  t= Glass thickness Accept a≤3.0mm or b≤0.8mm, c≤t (on the contact pin) a≤3.0mm or b≤1.5mm, c≤t (outside of the contact pin)  This play  t= Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t (outside of the contact pin)  This play  t= Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t  a≤1.5mm or b≤1.5mm, c≤t  This play	8		Class this lyness	Minor
9 Chip on Contact Pad  10 Chip on Face of Display  11 Chip on Cap Glass  12 Stain on Surface  13 TCP/FPC Damage  14 Dimension  15 Chip on Contact Pad  16 Chip on Face of Display  17 E Glass thickness Accept a≤3.0mm or b≤0.8mm, c≤t (on the contact pin) a≤3.0mm or b≤1.5mm, c≤t (outside of the contact pin)  10 Chip on Face of Display  11 Chip on Cap Glass  12 Stain on Surface  13 TCP/FPC Damage  14 Dimension  15 Chip on Sourface  16 Chip on Cap Glass  17 E Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t  18 Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t  19 Minor  10 Chip on Cap Glass  11 Chip on Cap Glass  12 Stain on Surface  13 TCP/FPC Damage  14 Dimension  15 Chip on Cap Glass  16 Chip on Cap Glass  17 E Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t  18 Minor  Minor  Minor  Minor  Minor  Minor  Major		Cup Glass		
Pad    Pad				
Accept a≤3.0mm or b≤0.8mm, c≤t (on the contact pin) a≤3.0mm or b≤1.5mm, c≤t (outside of the contact pin)  10 Chip on Face of Display  11 Chip on Cap Glass  12 Stain on Surface 13 TCP/FPC Damage 14 Dimension  Accept a≤1.5mm or b≤1.5mm, c≤t  16 Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t  17 Glass thickness Accept a≤3.0mm or b≤3.0mm, c≤t/2 a≤1.5mm or b≤1.5mm, t/2≤c≤t  18 Minor  Minor  Minor  Minor  19 Orack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection.  Major	9		t= Glass thickness	Minor
Display  t = Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t  11 Chip on Cap Glass  Minor  t = Glass thickness Accept a≤3.0mm or b≤3.0mm, c≤t/2 a≤1.5mm or b≤1.5mm, t/2≤c≤t  12 Stain on Surface Stain removable by soft cloth or air blow is acceptable.  13 TCP/FPC Damage  (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection.  Major		Tuu	a $\leq$ 3.0mm or b $\leq$ 0.8mm, c $\leq$ t (on the contact pin) a $\leq$ 3.0mm or b $\leq$ 1.5mm, c $\leq$ t	
Accept  a≤1.5mm or b≤1.5mm, c≤t  11 Chip on Cap Glass  Minor  t= Glass thickness  Accept  a≤3.0mm or b≤3.0mm, c≤t/2  a≤1.5mm or b≤1.5mm, t/2≤c≤t  12 Stain on Surface  Stain removable by soft cloth or air blow is acceptable.  Minor  TCP/FPC Damage  (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable.  (2) Terminal lead twisted or broken is not allowable.  (3) Copper exposed is not allowed by naked eye inspection.  Major	10			Minor
a≤1.5mm or b≤1.5mm, c≤t    11		Display		
t= Glass thickness  Accept  a≤3.0mm or b≤3.0mm, c≤t/2  a≤1.5mm or b≤1.5mm, t/2≤c≤t  12 Stain on Surface Stain removable by soft cloth or air blow is acceptable.  13 TCP/FPC Damage (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable.  (2) Terminal lead twisted or broken is not allowable.  (3) Copper exposed is not allowed by naked eye inspection.  14 Dimension Checking by mechanical drawing Major				
Accept  a≤3.0mm or b≤3.0mm, c≤t/2  a≤1.5mm or b≤1.5mm, t/2≤c≤t  12 Stain on Surface Stain removable by soft cloth or air blow is acceptable.  13 TCP/FPC Damage (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable.  (2) Terminal lead twisted or broken is not allowable.  (3) Copper exposed is not allowed by naked eye inspection.  14 Dimension Checking by mechanical drawing Major	11	Chip on Cap Glass		Minor
a≤3.0mm or b≤3.0mm, c≤t/2 a≤1.5mm or b≤1.5mm, t/2≤c≤t  12 Stain on Surface Stain removable by soft cloth or air blow is acceptable.  13 TCP/FPC Damage (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable.  (2) Terminal lead twisted or broken is not allowable.  (3) Copper exposed is not allowed by naked eye inspection.  14 Dimension Checking by mechanical drawing Major				
a≤1.5mm or b≤1.5mm, t/2≤c≤t  12 Stain on Surface Stain removable by soft cloth or air blow is acceptable.  13 TCP/FPC Damage (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable.  (2) Terminal lead twisted or broken is not allowable.  (3) Copper exposed is not allowed by naked eye inspection.  14 Dimension Checking by mechanical drawing Major				
13 TCP/FPC Damage (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection.  14 Dimension Checking by mechanical drawing Major				
13 TCP/FPC Damage (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection.  14 Dimension Checking by mechanical drawing Major	12	Stain on Surface	Stain removable by soft cloth or air blow is accontable	Minor
(2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection.  14 Dimension Checking by mechanical drawing Major			(1) Crack, deep scratch, deep hole and deep pressure mark on	
14 Dimension Checking by mechanical drawing Major			(2) Terminal lead twisted or broken is not allowable.	
	14	Dimension Unconformity		Major





# **II. Displaying Defects**

NO.	ITEM		CLASSIFICATION		
1	Black/White spot Dirty spot Foreign matter	Average Diameter (mm)  Φ≤0.10  0.10<Φ≤0.20  Φ>0.20	Pieces Permitted Zone A,B Zone C Ignore 3 Ignore 0		Minor
2	No Display	N	Major		
3	Irregular Display	N	Major		
4	Missing Line (row or column)	N	Major		
5	Short	Not allowable.			Major
6	Flicker	Not allowable.			Major
7	Abnormal Color	Ref	Major		
8	Luminance NG	Ref	Major		
9	Over Current	Ref	Major		



### 14 Precautions for operation and Storage

#### 14.1 Precautions for Operation

- (1) Since OLED panel is made of glass, do not apply any mechanical shock or impact or excessive force to it when installing the OLED module. Any strong mechanical impact due to falling dropping etc. may cause damage (breakage or cracking).
- (2) The polarizer on the OLED surface is made of soft material and is easily scratched. Please take most care when handing. When the surface of the polarizer of OLED Module is contaminated, please wipe it off gently by using moisten soft cloth with isopropyl alcohol, do not use water, ketone or aromatics. If there is saliva or water on the OLED surface, please wipe it off immediately.
- (3) When handling OLED module, please be sure that the body and the tools are properly grounded. And do not touch I/O pins with bare hands or contaminate I/O pins, it will cause disconnection or defective insulation of terminals.
- (4) Do not attempt to disassemble or process the OLED module.
- (5) OLED module should be used under recommended operating conditions shown in the specification. Since the higher voltage leads to the shorter lifetime, be sure to use the specified operating voltage.
- (6) Foggy dew, moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage, the deteriorated display quality and electrochemical reaction then leads to shorter life time and permanent damage to the module probably. Please pay attention to the environmental temperature and humidity.
- (7) An afterimage is created by the difference in brightness between unused dot and the fixed dot, according to the decrease of brightness of the emitting time. Therefore, to avoid having an afterimage, the full set should be thoroughly used instead of using a fixed dot. When the fixed dot emits, an afterimage can be created.
- (8) Flicker could be come out at full on display. And it disappears when frame frequency increase, but brightness decreases too.

#### 14.2 Soldering

- (1) Soldering should be performed only on the I/O terminals.
- (2) Use soldering irons with proper grounding and no leakage.
- (3) Iron: no higher than 300°C and 3~4 sec during soldering.

#### 14.3 Precautions for Storage

- (1) Please store OLED module in a dark place. Avoid exposure to sunlight, the light of fluorescent lamp or any ultraviolet ray.
- (2) Keep the environment temperature between 10°C and 35°C and the relative humidity less than 60%. Avoid high temperature and high humidity.
- (3) Keep the OLED modules stored in the container when shipped from supplier before using them is recommended.
- (4) Do not leave any article on the OLED module surface for an extended period of time.

#### 14.4 Warranty period

Visionox warrants for a period of 12 months from the shipping date when stored or used under normal condition.