UUT Report

Station ID:	**JPREWITT5**
Serial Number:	**3**
Date:	**Thursday, May 16, 2019**
Time:	**12:23:49 PM**
Operator:	**administrator**
Execution Time:	**5.3601858 seconds**
Number of Results:	**20**
UUT Result:	**Passed**

Begin Sequence: MainSequence
(C:\Users\jprewitt\Documents\GitHub\teststand-executor\TestStand Examples\Computer Motherboard Tests\Computer Motherboard Tests.seq)

Statement	
Status:	Done
Get Simulation Data	
Status:	Done
Simulation Dialog	
Status:	Skipped
Turn Vacuum Table On	
Status:	Done
Module Time:	0.0001044
Powerup Test	
Status:	Passed
Module Time:	9.24e-05
Wait	
Status:	Done
If {True}	
Status:	Done

CPU Test	
Status:	Passed
Module Time:	0.0467415

Begin Sequence: CPU Test
(C:\Users\jprewitt\Documents\GitHub\teststand-executor\TestStand Examples\Computer Motherboard Tests\Computer Motherboard Tests.seq)

Register Test	
Status:	Passed
Module Time:	9.27e-05
Instruction Set Test	
Status:	Passed
Module Time:	7.6e-05
Cache Test	
Status:	Passed
Module Time:	8.21e-05

FPU Test	
Status:	Passed
Module Time:	8.89e-05

End Sequence: CPU Test

ROM Test	
Status:	Passed
Module Time:	0.0001073
RAM Test	
Status:	Passed
Module Time:	6.89e-05
Video Test	
Status:	Passed
Measurement:	1
Limits:	
Low:	0
High:	10
Comparison Type:	GTLT (> <)
Module Time:	9.03e-05
Keyboard Test	
Status:	Passed
Measurement:	6
Limits:	
Low:	5
Comparison Type:	GT (>)
Module Time:	0.0002205
If {False}	
Status:	Done
End If	
Status:	Done

End If	
Status:	Done
Turn Vacuum Table Off	
Status:	Done
Module Time:	0.0001202

End Sequence: MainSequence

End UUT Report