HiWire™ LP CLOS AEC

LP CLOS AEC Specification

800G (8x106G) QSFP-DD PAM4 to 800G (8x106G) QSFP-DD PAM4

Plug & Play Active Electrical Cable for In-Rack Ethernet Applications in Distributed, Disaggregated Chassis (DDC)

Description

Credo's HiWire™ Low Power CLOS Active Electrical Cable (LP CLOS AEC) is a thin, low power 800G AEC specifically designed for in-rack applications replacing backplanes in Distributed, Disaggregated Chassis (DDC) implementations. Plug & Play LP CLOS AECs consume up to 75% less power and take 75% less volume than DACs, enabling interconnect densities of up to 1,000 cables per rack.

Credo's **CAC8XX321D1D-A0-HW HiWire LP CLOS AEC** is designed for telecom and data center use. It can sustain 8 lanes of 106G-PAM4 signal in each direction, providing bi-directional 800Gbps traffic per cable. The use and replacement of this AEC is simple and straightforward as it adopts standard QSFP-DD type 2 form factor and complies to MSA specifications.

Product Features

The following are the key features of the HiWire LP CLOS AEC:

- Recognizable, purple PVC jacket
- 800G to 800G data rate
- Built-in diagnostic features
- CMIS 4.0 compliant
- Single 3.3V power supply
- Typ. 10W power dissipation each end
- BER < $10^{\wedge -15}$ (post FEC)
- Hot pluggable
- RoHS2 compliant
- I^2C management interface
- Operating case temperature range: 0^o to $+70^oC$

1:1 Direct LP CLOS AEC

Product Selections

Part Number	Length	AWG	Weight
CAC4XX321D1D-C0-HW	0.5m	32	275g
CAC4xx321D1D-D0-HW	1.0m	32	300g
CAC4xx321D1D-A0-HW	1.5m	32	325g
CAC4xx321D1D-D0-HW	2.0m	32	350g
CAC4xx321D1D-A0-HW	2.5m	32	350g

Mechanicals

Parameter	Cable Type	Typical	Length
Diameter	16P 32AWG	6.8mm	0.5 - 2.5m

Supported Standards

The following are the key features of the HiWire cable:

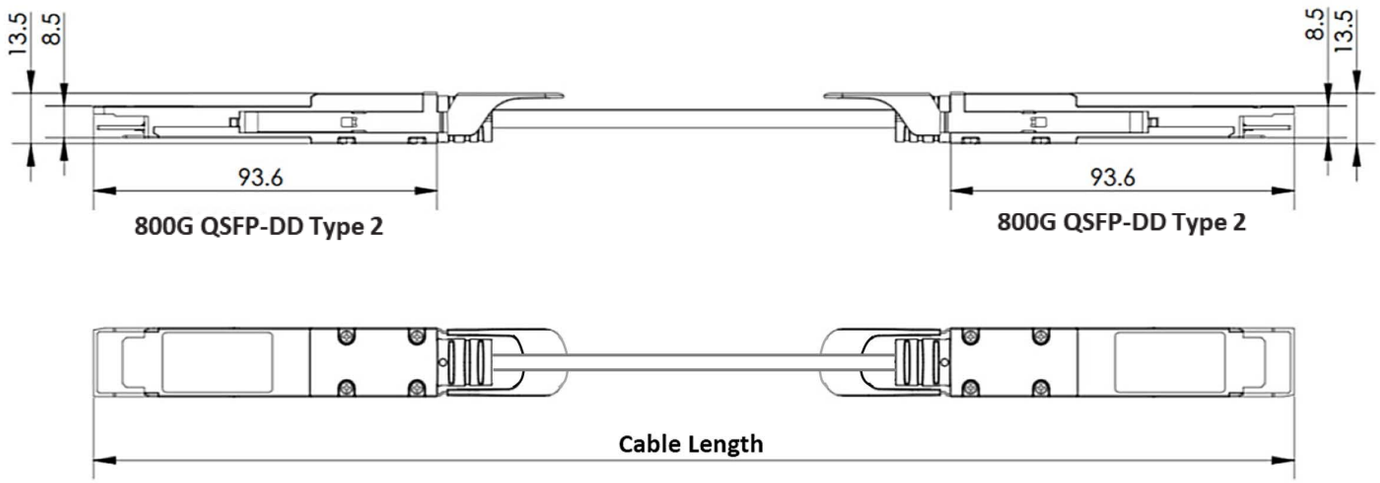
- Common Management Interface Specification (CMIS) v4.0
- QSFP-DD MSA v5.0

LP CLOS AEC

800G (8x106G) QSFP-DD PAM4 to 800G (8x106G) QSFP-DD PAM4

General Product Characteristics

Parameter	Value
Module Form Factor	QSFP-DD type 2
Number of Data Lanes	8 TX and 8 RX per module (PAM4)
Maximum Aggregate Data Rate	800Gbps
Nominal Data Rate per Lane	106.25Gbps (PAM4)
Electrical Interface and Pin-out	76-pin edge connector
Pin Description	Per QSFP-DD Hardware Specification
Management Interface	I^2C, serial, timing per Common Management Interface Specification for 8X/16X Pluggable Transceivers (QSFP-DD)
Length of Copper AEC	0.5m - 2.5m in 0.5m increments
BER (Pre-FEC)*	Typ. $<10^{-8}$ * Tested with QPRBS31 pattern
BER (Post-FEC)*	$<10^{-15}$ * Tested with QPRBS31 pattern



For more information please visit **www.credosemi.com/hiwire-aec** or email **hiwire@credosemi.com**

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