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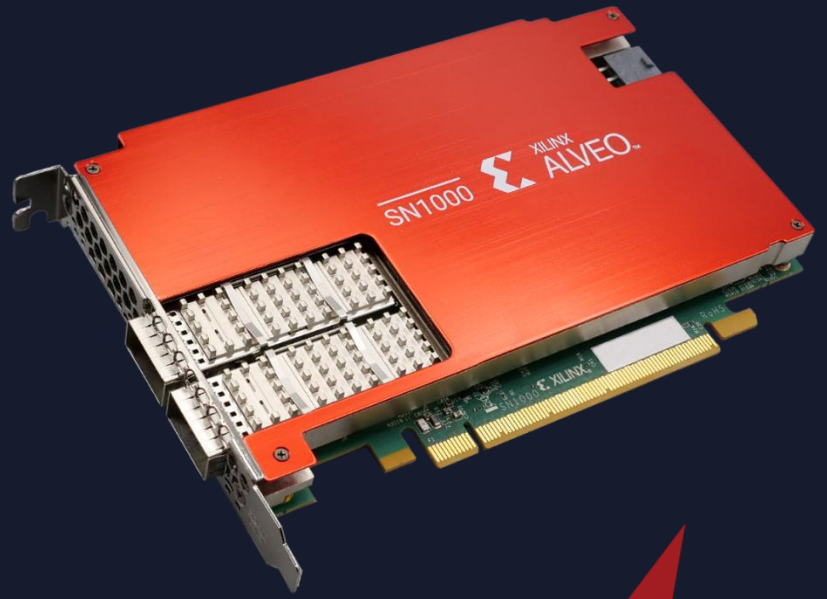


Alveo SN1000 SmartNIC

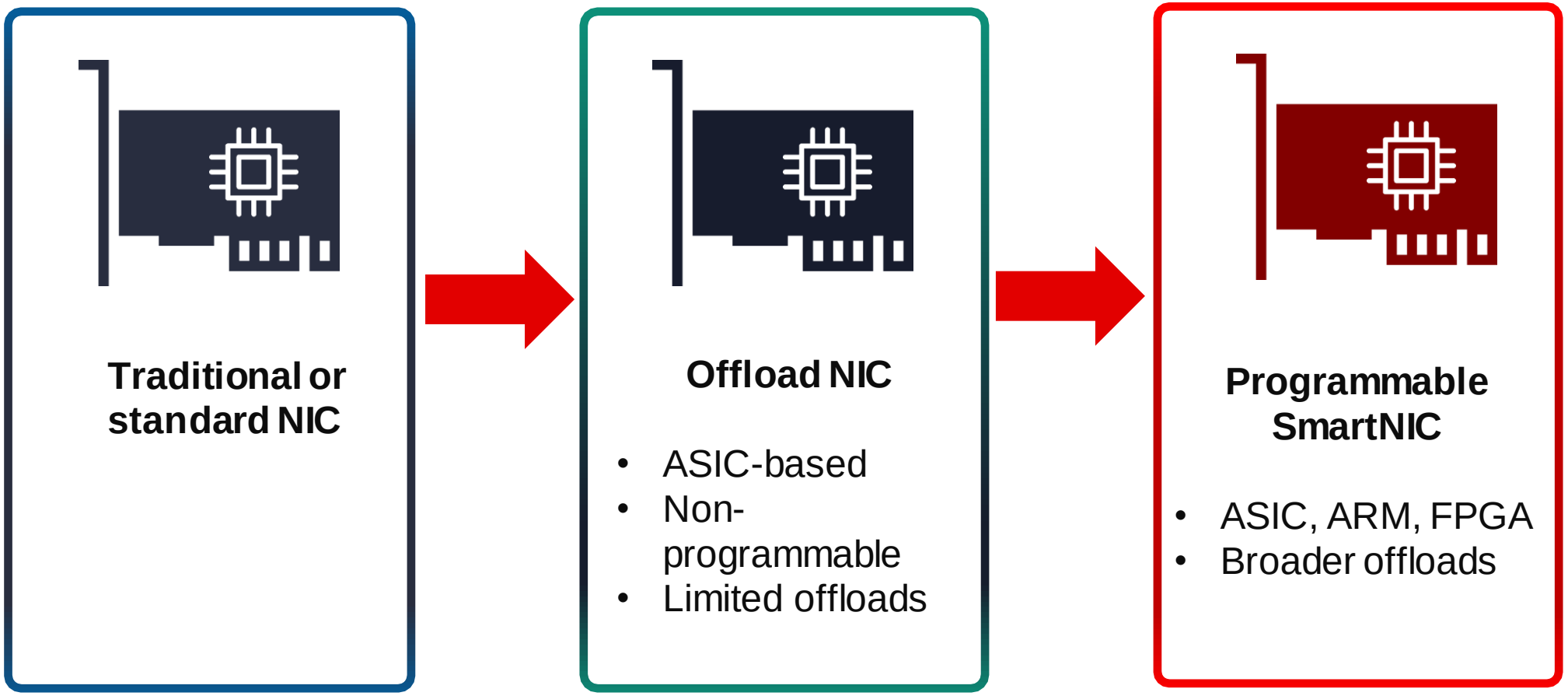
Product Overview

February 2021

Agenda

- SmartNIC Evolution
- Alveo SN1000 SmartNIC Overview
- Schedule & Ordering

Evolution of the Smart NIC



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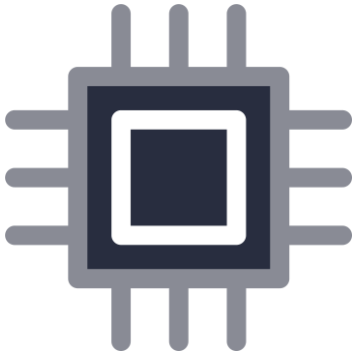
SmartNICs: Emerging Limitations

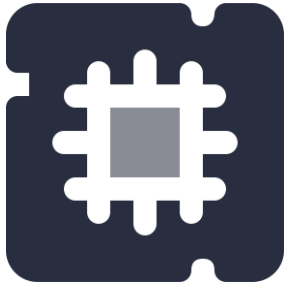
Cloud providers need both performance *and* adaptability

- Continuous feature innovation and velocity
  - Virtualization offloads
  - Security ciphers
  - Low latency transport
- Custom workloads at line-rate hardware acceleration

BUT…



ASIC implementations lack customization capabilities



CPU/SOC implementations suffer performance hits at scale

Common Offload Types

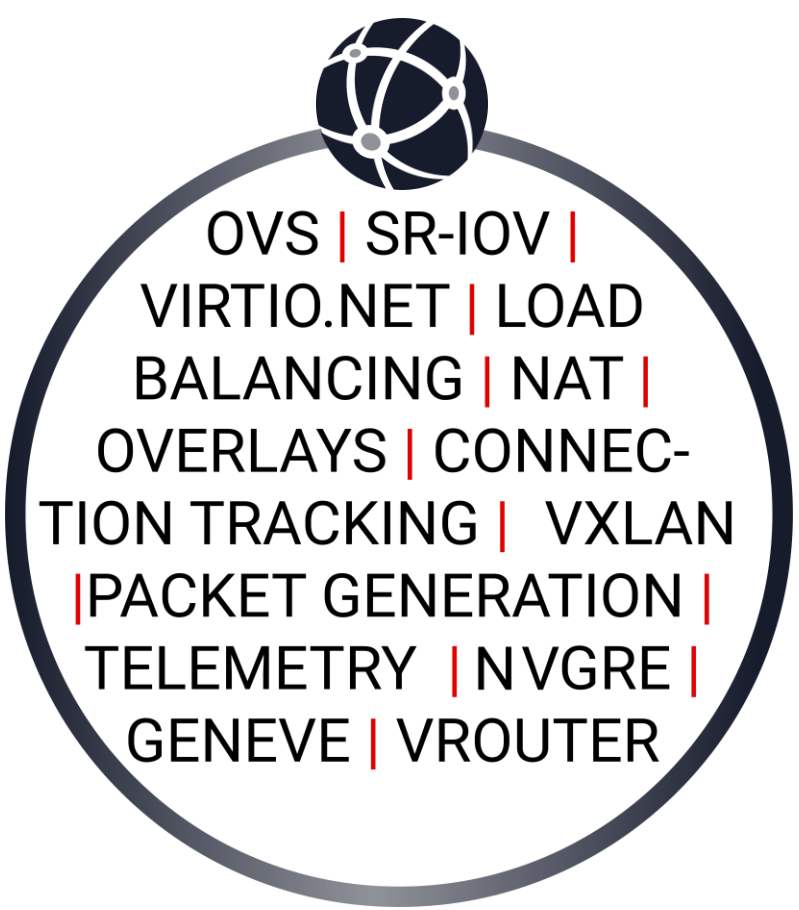
NETWORKING

SECURITY

STORAGE

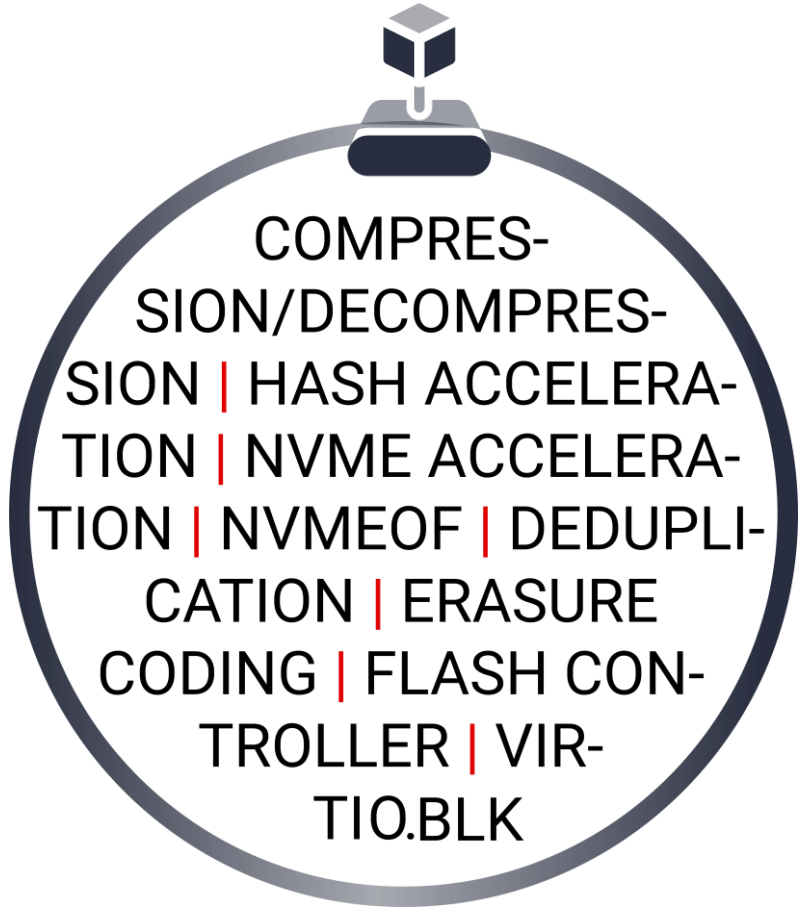
XILINX.

Common Offload Types



NETWORKING

SECURITY



STORAGE

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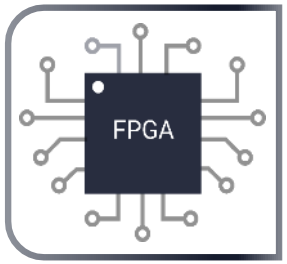
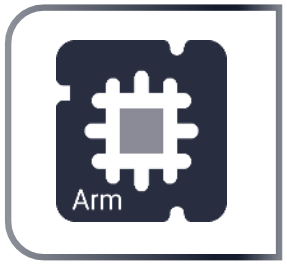
Alveo SN1000 SmartNIC Overview

Introducing The Xilinx Alveo SN1000 SmartNIC Family



The Adaptability of Xilinx FPGAs

+



Isolated Control and Data Planes

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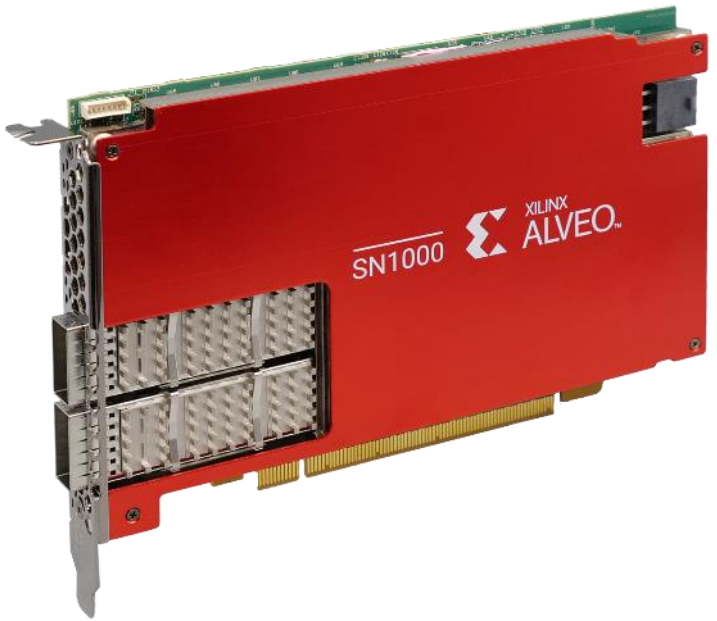
Vitis Networking:
P4, C, C++ Programming

=

The Industry's First SmartNIC with *Composable Hardware*



- 2x100Gb
- PCIe Gen 4
- 100Mpps
- 75w

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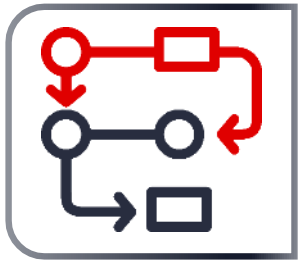
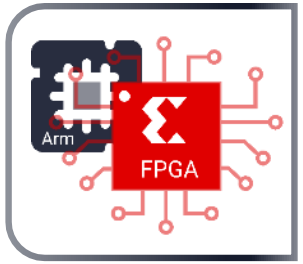
The Alveo SN1000 SmartNIC Family Difference

Software-defined hardware acceleration for all offloads



Application specific data paths at line-rate performance

P4 , C, C++ programming for fast, adaptable hardware acceleration



Heterogeneous architecture with control and data plane isolation

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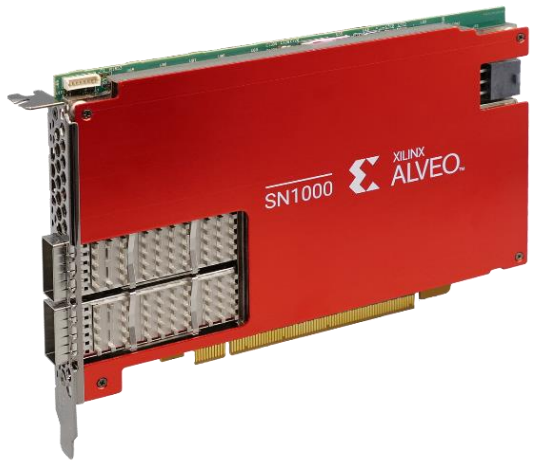
Alveo SN1022 SmartNIC Summary

- **Fully composable and programmable**
  - Versatile solution for containerized virtualized, bare metal deployment
  - Comprehensive suite of Security offloads including IPSec, kTLS and SSL/TLS
  - Storage acceleration for NVMe/TCP, Ceph and services including compression and crypto
- **Deploy custom plugins programmed in P4, HLS, or RTL**
  - Adapt to changing requirements without replacing hardware
- **Hardware root of trust**



Hardware
- PCIe Gen 4 x8 or Gen 3 x16
- 2x100G QSFP28 DA copper or optical transceiver
- XCU26 FPGA based on Xilinx 16nm UltraScale+ architecture
- On-board CPU: 16 64-bit Arm Cortex®-A72 cores at 2.0 GHz with 8 MB cache
- 1x 4GB x 72 DDR4-2666 (Processor)
- 2x 4GB x 72 DDR4-2666 (FPGA)

General Networking
- TCP/UDP Checksum Offload (CSO), TCP Segmentation Offload (TSO), Generic Send Offload (GSO)
- Generic Receive Offload (GRO), Receive Side Scaling (RSS)
- VLAN Insertion/Removal
- VLAN Q-in-Q Insertion/Stripping
- Jumbo Frames (up to 9KB)

Traffic Steering
- TCP/UDP/IP, MAC, VLAN, RSS filtering Accelerated Receive Flow Steering (ARFS), Transmit Packet Steering (XPS)

Virtualization
- Linux Multi-queue
- Single Root I/O Virtualization (SR-IOV)
- Tunneling offloads; adaptable to custom overlays.

Software and FPGA Extensibility
- Support for custom plug-ins to enable new functionality; programmed via P4, HLS, or RTL.

Manageability and Remote Boot
- UEFI
- Secure Firmware Upgrade and Hardware Root of Trust
- NC-SI, PLDM Monitoring and Control, PLDM Firmware Update and MCTP support
- MCTP transports support SMBUS and PCIe VDM

OS Support
- Red Hat RHEL, CentOS, Ubuntu for Host CPU
- Ubuntu and Yocto Linux for on-board Arm CPU

Network Acceleration
- Onload®/ TCPDirect - TCP/UDP
- Open Virtual Switch (OVS)
- DPDK Poll Mode Driver
- Hardware Offloaded Virtio-net
  - Virtio v0.9.5 and later
  - CSO, TSO
  - Multi-queue
  - vDPA (Virtual Data Path Acceleration)

Hardware-based Packet Processing
- Wildcard match-action flow tables
- Tunnel encap/decap – VXLAN, NVGRE
- Connection Tracking
- Packet Replication
- Header rewrite/NAT
- Per-rule packet and byte counters
- MAC Address rewriting
- 4 M stateful connections and up to 20K Megaflows with wildcard match support

Storage Acceleration
- Ceph RBD Client Offload
- Hardware Offloaded Virtio-net
  - Virtio v0.9.5 and later
  - Multi-queue

Environmental Requirements[2]
- Temperature:
  - Operating: ≤ 30°C (86°F)
  - Storage: –40°C to 75°C (–40°F to 167°F)
- Humidity:
  - Operating: 8% to 90%, and a dew point of –12°C
  - Storage: 5% to 95%

Physical Dimensions (without bracket)
- Full Height Half Length PCIe CEM
- L: 6.59 inch (167.5 mm)
- W: 4.38 inch (111.15 mm)
- H: 0.72 inch (18.3 mm)

Ordering Information
- A-SN1022-P4N-PQ: Encryption Disabled
- A-SN1022-P4E-PQ Encryption Enabled

Notes:
Feature availability is software release dependent. Please check release notes or contact Xilinx Support for more information.
1. Performance is driver dependent. Please check release notes or contact Xilinx Support for more information.
2. Environmental specs are preliminary.

TAKE THE NEXT STEP > www.xilinx.com/smartnic

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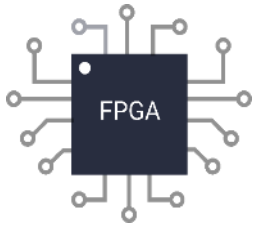
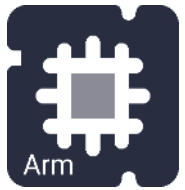
Adaptable. Intelligent.

Alveo SN1022 SmartNIC Performance



Xilinx
UltraScale+



NXP
LX2162A

Performance	SN1022
Connectivity	2x100 QSFP28 Ports
Full Duplex Throughput	200Gbps
Packet Rate	100Mpps
TCP Throughput	100Gbps
Latency (1/2 RTT)	<3us
OVS Performance*	100Gbps
Flow Table Entries	4 M stateful connections
IPsec Encryption Throughput	100Gbps (AES-GCM)
Power	75W

Sampling Today; Shipping March '21

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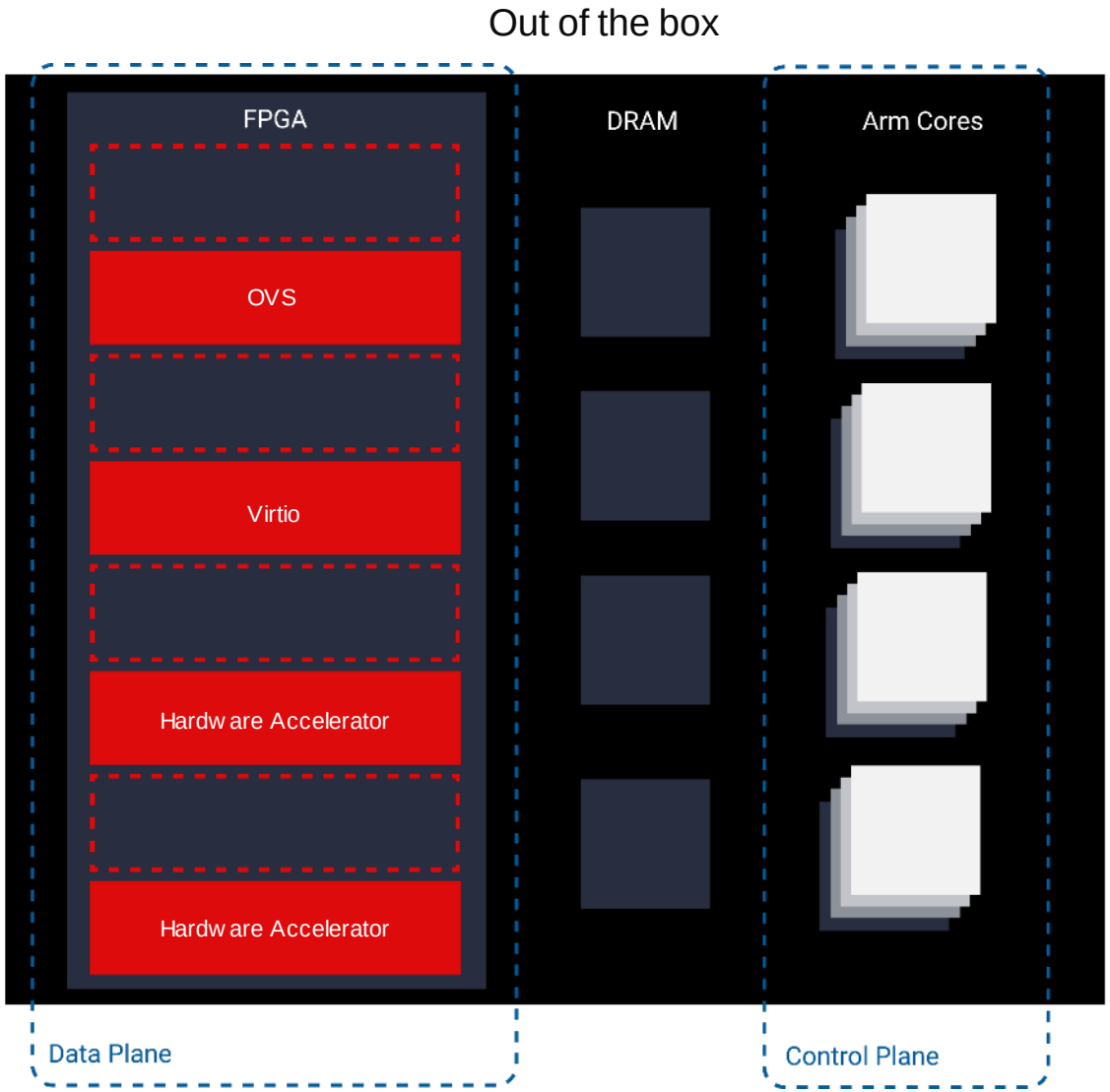
Introducing The Xilinx Alveo SN1000

- **Software-defined hardware acceleration**
- Application specific data paths
- Build **custom offloads** or **extend existing offloads** to handle new protocols and applications



XILINX.

Introducing The Xilinx Alveo SN1000

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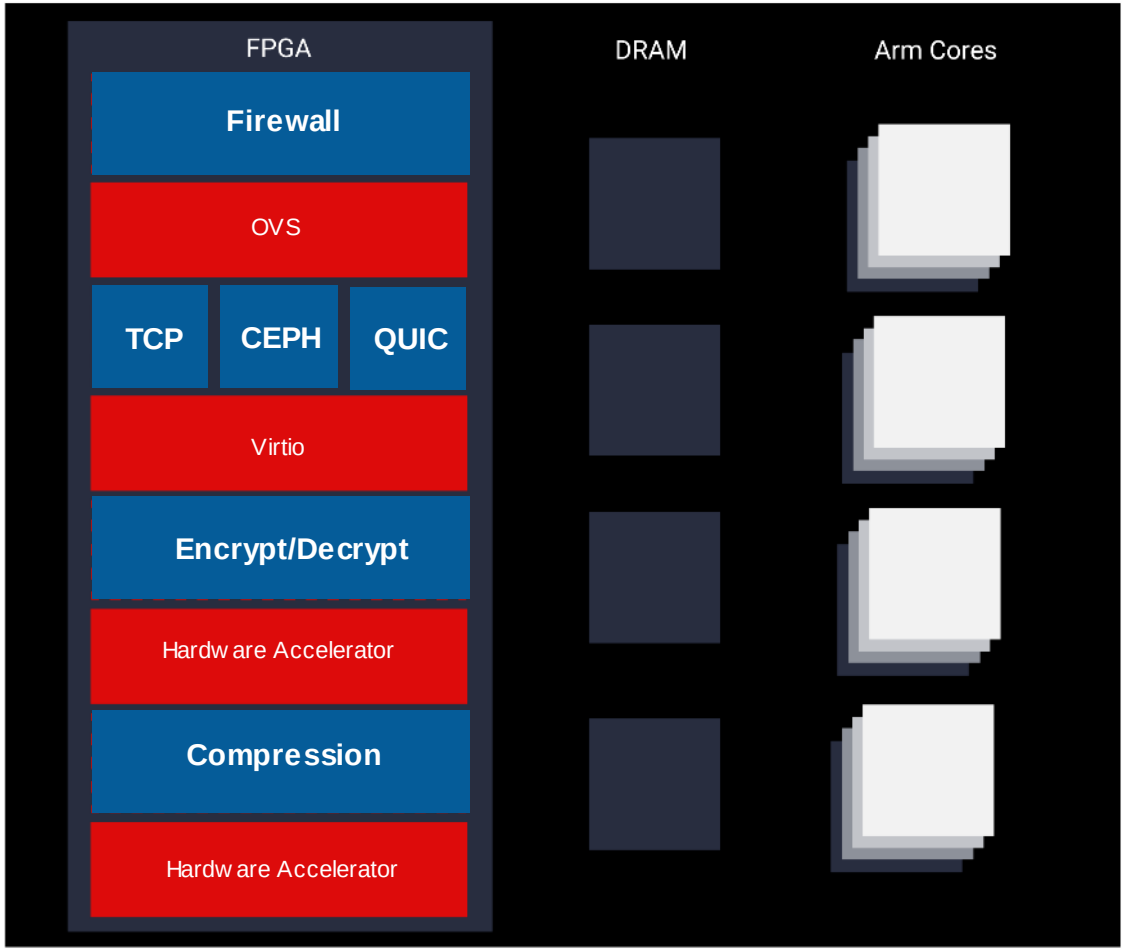
Example 1



XILINX.

Introducing The Xilinx Alveo SN1000

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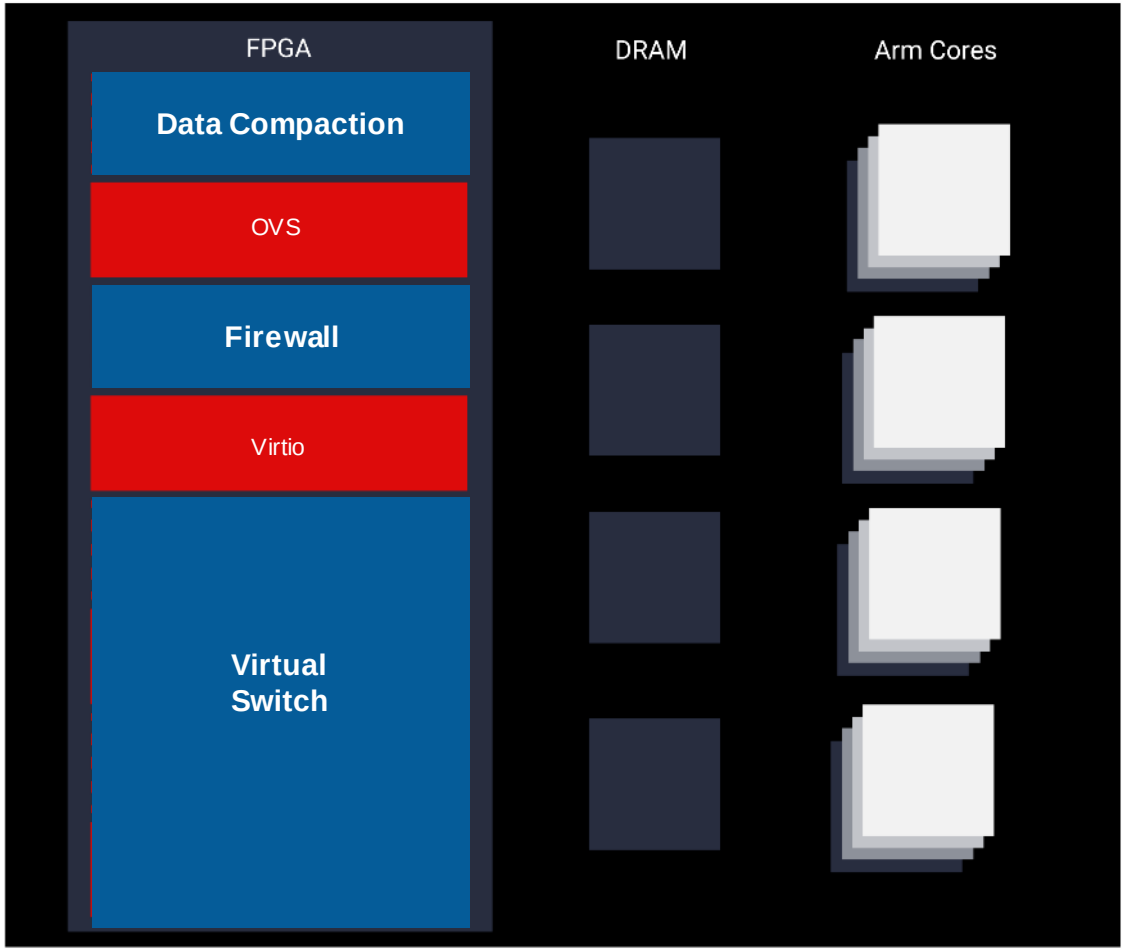
Example 2



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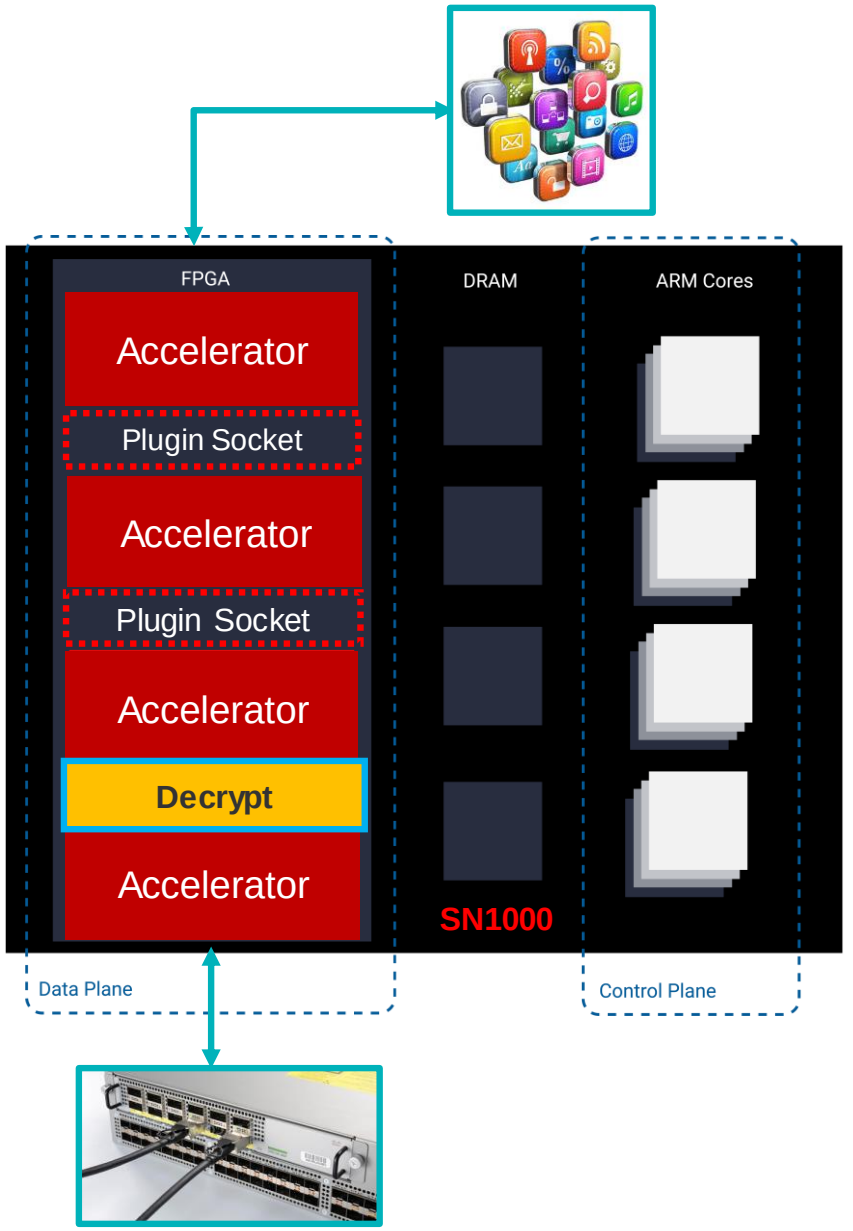
SN1000 SmartNIC Composability

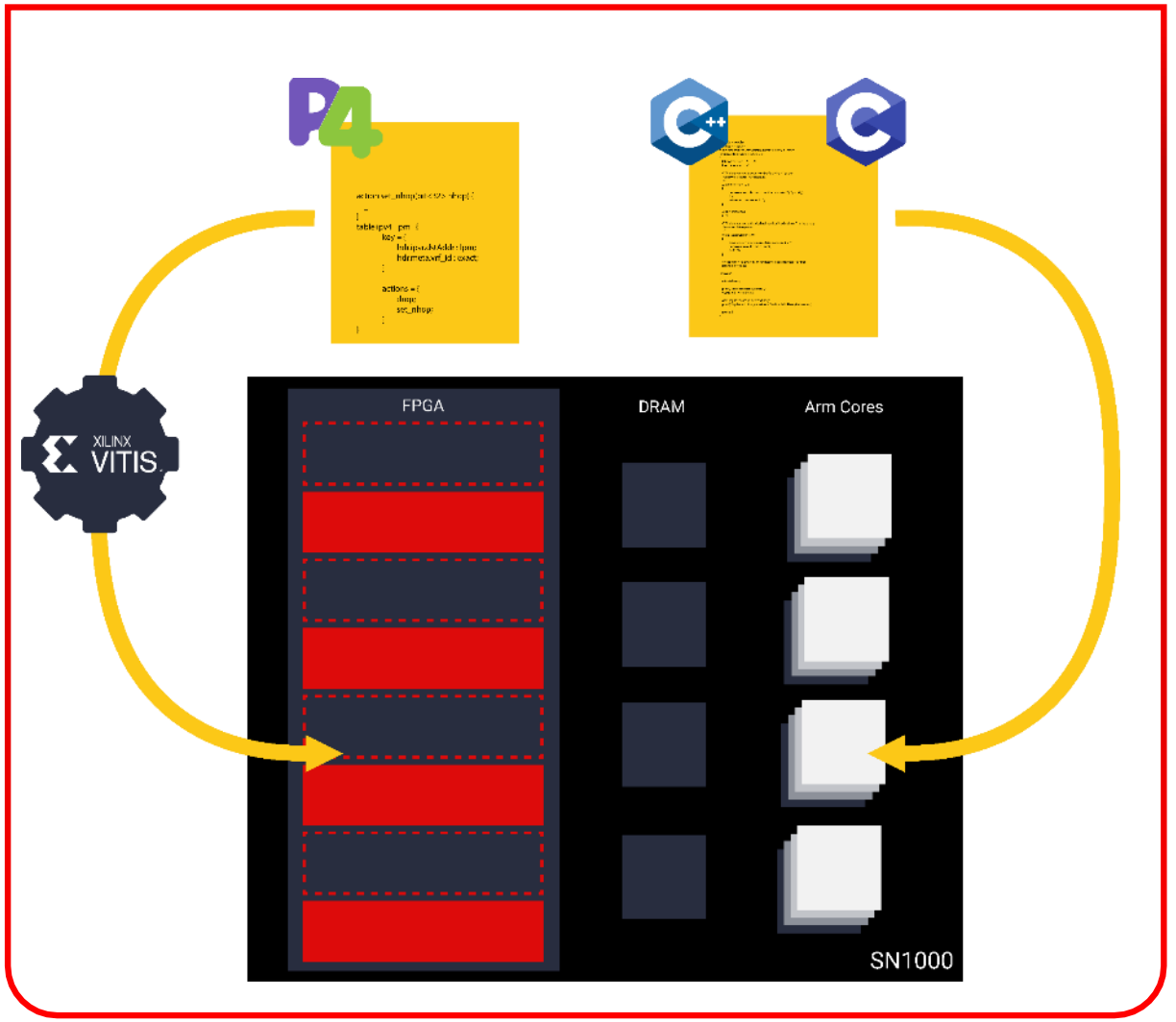
- Isolated data and control planes
- Use P4/HLS/RTL to “compose” custom application specific kernels, or plugins, or augment existing plugins
- Open platform for Xilinx-provided, ISV provided, or customer-built plugins
- Tailor per-application data path through plugin framework for streamlined packet processing



Vitis Networking

- **Customize with ease, without sacrificing performance**
- **P4: the perfect match for "Match-Action" processing**
  - Tailored for high-performance networking
  - Includes high performance algorithmic CAM technologies
- **Vitis RTL/HLS-** Mature developer tools for any compute or storage offloads at HW speeds with powerful high level language support
- **Xilinx SmartNIC Plug-In Framework**
  - Customizations can be easily embedded into the powerful SN1000 SmartNIC flow

Software-Defined Hardware Acceleration



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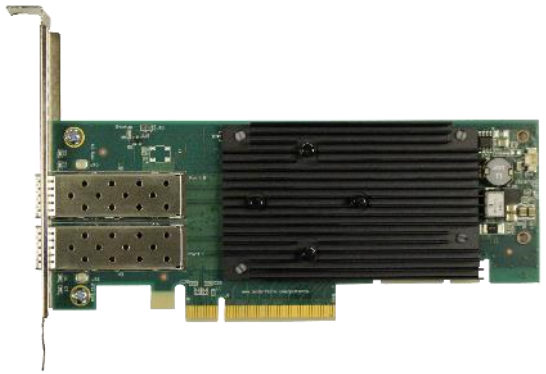
Xilinx NIC Family



X2

10/25/100Gb Offload NIC

U25

25Gb SmartNIC

SN1000

100Gb SmartNIC

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Xilinx SmartNIC Products

Alveo™ SmartNIC Data Center Accelerator Cards

	Feature	Alveo U25	Alveo SN1022
Dimensions	Width	Single Slot	Single Slot
	Form Factor	Half Height, ½ Length	**Full Height, ½ Length**
Logic Resources[1]	Look-Up Tables	523K	**1,030K**
	Registers	1,045K	**2,059K**
DRAM Memory	DDR Format	- 1x 2GB x 40 DDR4-2400 - 1x 4GB x 72 DDR4-2400	- **1x 4GB x 72 DDR4-2666 (Arm® Processor)** - **2x 4GB x 72 DDR4-2666 (FPGA)**
Interfaces	PCI Express®	Gen3 x16, 2xGen3 x8	**Gen 3 x16, Gen 4 x8**
	Link Speeds	10/25GbE	**100GbE**
	Network Interface	2x SFP28	**2x QSFP28**
	Arm Processor	Integrated Quad-core Cortex®-A53 Processor	**Discrete 16-core Cortex-A72 Processor**
Power and Thermal	Thermal Cooling	Passive	Passive
	Thermal Design Power	40W	70W
	Total Power	75W	75W
Networking	Stateless Offloads	Yes	Yes
	Tunneling Offloads	VXLAN, Geneve, Custom	VXLAN, NVGRE, Custom
	SR-IOV	Yes	Yes
	Advanced Packet Filtering	Yes	Yes
	Acceleration / Offloads	DPDK, Onload®	**DPDK, Onload®, Open Virtual Switch (OVS), Virtio-net, Virtio-blk, vDPA, Ceph RBD Client offload**
Manageability	PMCI Protocols	NC-SI, PLDM Monitoring and Control, PLDM MCTP	NC-SI, PLDM Monitoring and Control, PLDM MCTP
	PMCI Transports	MCTP SMBus, MCTP PCIe VDM	MCTP SMBus, MCTP PCIe VDM
	Boot Support	PXE and UEFI	UEFI
Software Plugins	Software and FPGA Extensibility and Composability via Dynamically Loadable Plugins	No	**Yes**
Tool Support	Vitis™ Developer Environment	Yes	Yes

Notes:
1. Logic resources shown without platform usage; refer to card user guides for platform resource usage.

Schedule and Ordering

CY2021 Feature Roadmap

Product	Launch (Feb 2021)	Mar	Q2	Q3
	1x100G Early Access • OVS • Virtio-net • Virtio-blk • PCIe G3 x16 / G4 x8	1x100G Production • OVS • Virtio-net • Virtio-blk Ceph/TCP Plugin EA	2x100G Production 2x25G EA/Production PCIe Gen 4 x8 Production Ceph/TCP Plugin Production IPsec Plugin EA	IPsec Plugin Production
XILINX VITIS Networking	Plugin Framework with P4, RTL/HLS Early Access	Plugin Framework with P4, RTL/HLS Production	Vitis + P4 Ease of Use enhancements	

For questions on the product and schedule, please contact Sameer Shurpalekar

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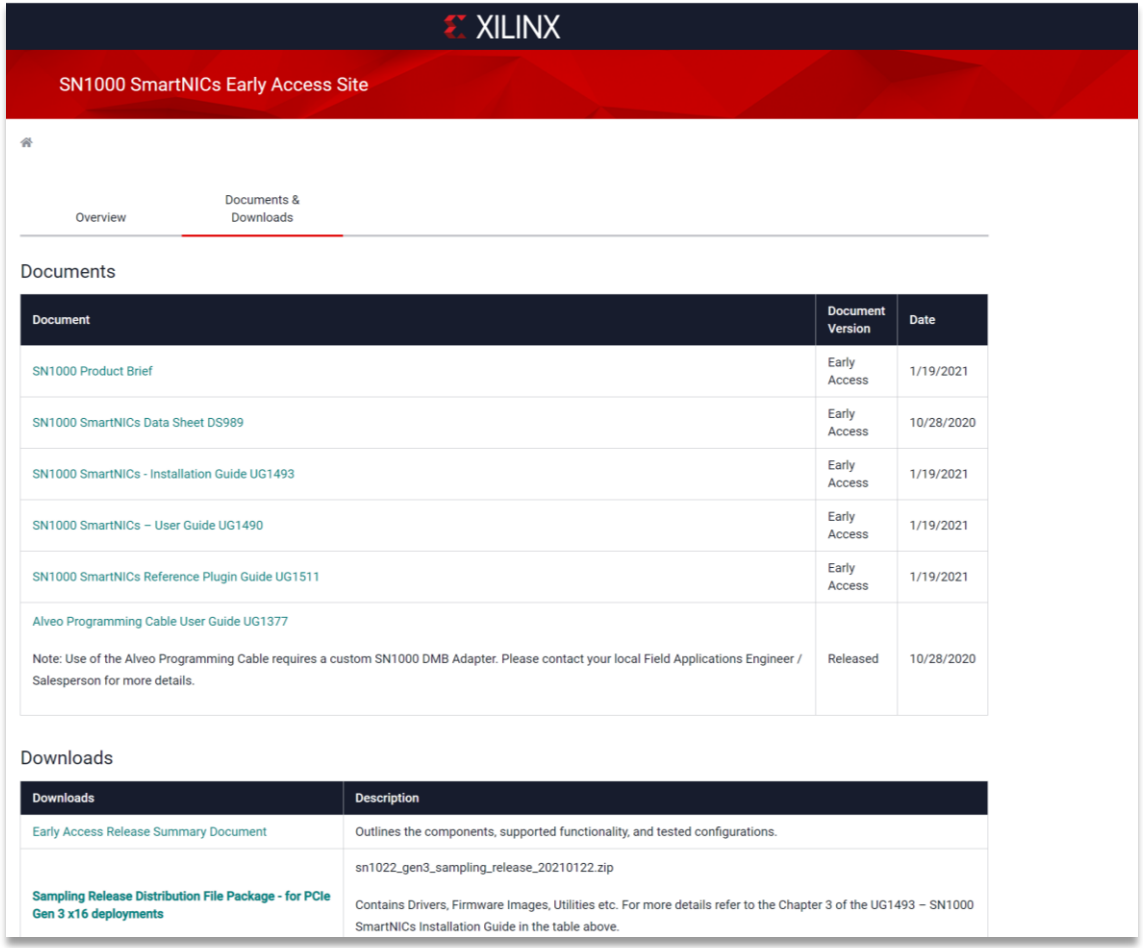
SN1000 Downloads and Documentation

- SN1000 Early Access Lounge
  - www.xilinx.com/member/sn1000-ea.html
  - Install Guide
  - User Guide
  - Plugin Reference Guide
  - Software Downloads
- Public Documentation
  - Product Brief
  - Technical Brief
  - Datasheet



SN1000 Ordering Information

Product	Part Number	Description	OOE	FCS	1 - unit SRP
Alveo SN1022	A-SN1022-P4N-PQ	2 x QSFP28, single slot, FHHL, 75W, SoC+SuC Encryption DISABLED	Now	March '21	$3150
	A-SN1022-P4E-PQ	2 x QSFP28, single slot, FHHL, 75W, SoC+SuC Encryption ENABLED	Contact Marketing		$3150

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Thank You