

INTRODUCTION

CS3021/3421 Computer Architecture II

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BACS/MCS and BAI/MAI students

BACS/MCS YEAR 3 TIMETABLE

School of Computer Science and Statistics
Integrated Computer Science: Year 3 Timetable 2017-18

Time	Monday	Tuesday	Wednesday	Thursday	Friday
09.00 – 10.00			MT: CS3012: Lect LB04		
10.00 – 11.00	MT: CS3021: Lect LB08 HT: CS3031: Lect LB08	MT: CS3071: Lect LB01 HT: CS3031: Lect LB01	MT: CS3011: Lect LB01 HT: CS3061: Lect LB04	MT: CS3021: Lect: LB08 HT: CS3031: Lect LB08	HT: CS3081: Lect LB01
11.00 – 12.00					
12.00 – 13.00	MT: CS3012: Lect Joly	HT: CS3061: Lect LB04		MT: CS3071: Lect LB01	
13.00 – 14.00	MT: CS3011: Lect LTEE1	MT: CS3012: Lect Goldhall HT: CS3013: Lect LB01/ M20 (2hrs)	HT: ST3009: Lab: LG12/35/36		
14.00 – 15.00	MT: CS3016 Lect LB01/ICT1/2 HT: CS3061 Lect LB04	MT: CS3011: Lect LG12 HT: CS3013: Lect LB01/M20	MT: CS3041: Lect LB01	MT: CS3016: Lect LB04/ICT1 HT: CS3014: Lect LB04/ICTLab2 (2hrs)	HT: CS3081: Tut: LB01
15.00 – 16.00			MT: CS3021: Lect M17 HT: ST3009: Lect: LB01 (2hrs)	HT: CS3014: Lect LB04	MT: CS3016: Lect LB01
16.00 – 17.00	MT: CS3011: Lab LG12	HT: CS3014: Lect LB04	HT: ST3009: Lect: LB01 MT: CS3071: Lab ICT Lab1/2	MT: CS3041: Lect LB08	
17.00 – 18.00					

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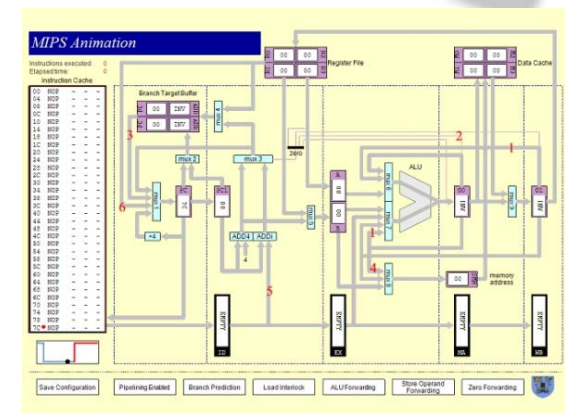
BAI/MAI YEAR 4 TIMETABLE

SENIOR SOPHISTER ENGINEERING, 2017/18 - ELECTRONIC AND COMPUTER ENGINEERING										
										Date of issue: 12th September, 2017
DAY	SEMESTER	0900 - 1000	1000 - 1100	1100 - 1200	1200 - 1300	1300 - 1400	1400 - 1500	1500 - 1600	1600 - 1700	1700 - 1800
MONDAY	First semester	4C16 [M20]	CS3421 [LB08]	4C7 [AP4.03] CS4400 [LB04]	4C4 [LB04]		4C4 [LB08]	CS4052 [LB04]	4C7 [M21]	4E1 [HAM4]
	Second semester	4B9 tutorial [M17]		CS7434 [LB01]	4C15 [M21]	4C8 [M20]	4B12 [M17]		CS4407 [LB04]	
TUESDAY	First semester	4C5 [M17]	CS4053 [LB08]	CS4052 [LB04/ICTLAB1/ICTLAB2]		CS4053 [LB04 and ICTLAB1]		CS4404 [HAM3]	4E1 [HAM4]	
	Second semester	4C8 [CADLAB]		CS4D2B [M21]	4C15 [M21]	4B9 [LB04]	4B9 laboratories [MECH LAB]		4B9 [2037]	
WEDNESDAY	First semester	4C16 [CADLAB]			4C5 [M20] CS4404 [HAM4]	CS4053 [LB01 and ICTLAB1]	CS4D2A [LB01]	CS3421 [M17]	4C16 [M21]	CS4404 (weeks 3 - 6, 9, 10) [LB04]
	Second semester	CS4D2B [M20]	4C15 [AP2.04]	4B9 [2039]	CS7434 [LB01]	CS7434 [LB01 and ICTLAB2]	CS4D2B [LB01]	CS4405 [LB08]		
THURSDAY	First semester	4C7 [M20]	CS3421 [LB08]	4C16 [CLT]	4C4 [LB04]		4C7 [M17] CS4400 [LB08]		CS4D2A [LB08]	
	Second semester	CS4407 [LB01]	4C8 [M17]	4C15 [M21]	4B12 [DO]		CS4405 [LB01]		CS4D2B [LB08]	
FRIDAY	First semester	Electronic Engineering laboratories/projects (C and CD stream) [EE LABS]					4C5 [M20]			
	Second semester	Electronic Engineering laboratories/projects (C and CD stream) [EE LABS]					4C8 [M21]		CS4406 [LB01]	

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SYLLABUS

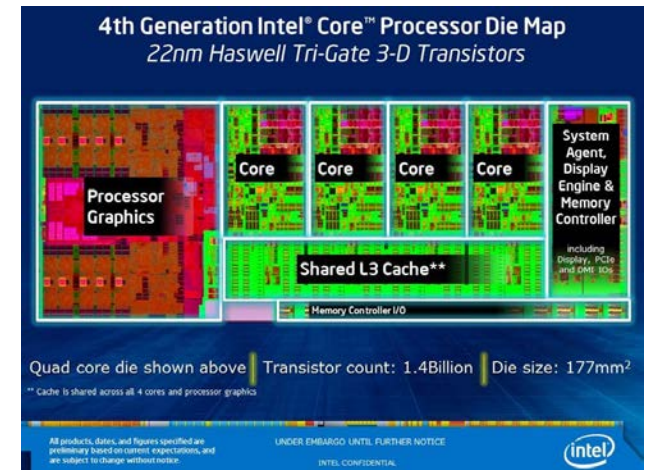
- IA32 and x64 assembly language programming
- IA32 and x64 procedure calling conventions
- RISC vs CISC
- RISC-1 design criteria and architecture
- Register windows and delayed jumps
- Instruction level pipelining
- DLX/MIPS pipeline
- Resolving data, load and control hazards
- Virtual Memory
- Memory management units [MMUs]
- Multi-level page tables and TLBs
- MMU integration with an OS



INTRODUCTION

SYLLABUS ...

- Cache organisation (L, K and N)
 - Cache operation and performance
 - The 3 Cs
 - Virtual vs physical caches
 - Pseudo LRU and LRU replacement policies
 - Address trace analysis
-
- Multiprocessor architectures
 - Cache coherency
 - Cache coherency protocols [write-through, write-once, Firefly and MESI]



INTRODUCTION

ASSESSMENT

Coursework: 20%

- 5 or 6 tutorials + a coursework project

Examination: 80%

- January 2018
- answer 3 out of 4 questions in 2 hours



INTRODUCTION

COURSE WEB PAGE

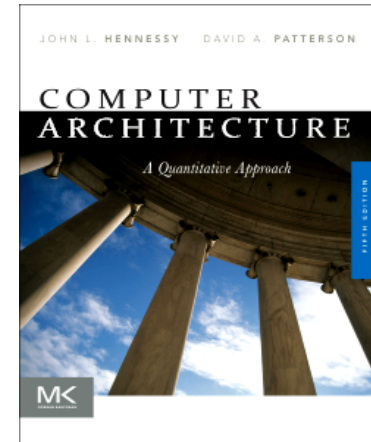
<https://www.scss.tcd.ie/Jeremy.Jones/CS3021/CS3021.htm>

For

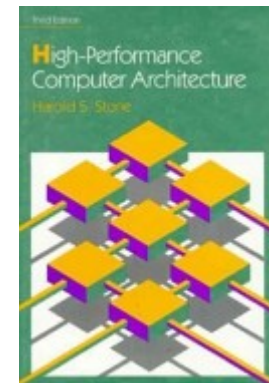
- Lecture notes
- Tutorials (questions, answers and marks)
- Coursework
- Miscellaneous materials

Useful Books

Computer Architecture - a Quantitative Approach
John Hennessey and David Patterson



High Performance Computer Architecture
Harold S. Stone
[for address trace analysis]



Get Started on Wednesday @ 3pm M17

See you there!