



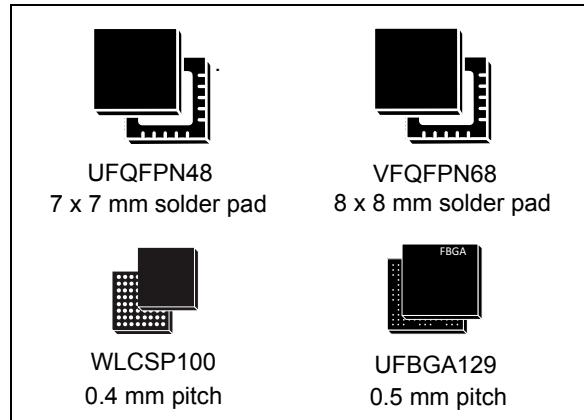
STM32WB55xx STM32WB35xx

Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® 5.2 and 802.15.4 radio solution

Datasheet - production data

Features

- Include ST state-of-the-art patented technology
- Radio
 - 2.4 GHz
 - RF transceiver supporting Bluetooth® 5.2 specification, IEEE 802.15.4-2011 PHY and MAC, supporting Thread and Zigbee® 3.0
 - RX sensitivity: -96 dBm (Bluetooth® Low Energy at 1 Mbps), -100 dBm (802.15.4)
 - Programmable output power up to +6 dBm with 1 dB steps
 - Integrated balun to reduce BOM
 - Support for 2 Mbps
 - Dedicated Arm® 32-bit Cortex® M0+ CPU for real-time Radio layer
 - Accurate RSSI to enable power control
 - Suitable for systems requiring compliance with radio frequency regulations ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15 and ARIB STD-T66
 - Support for external PA
 - Available integrated passive device (IPD) companion chip for optimized matching solution (MLPF-WB-01E3 or MLPF-WB-02E3)
- Ultra-low-power platform
 - 1.71 to 3.6 V power supply
 - 40 °C to 85 / 105 °C temperature ranges
 - 13 nA shutdown mode
 - 600 nA Standby mode + RTC + 32 KB RAM
 - 2.1 μA Stop mode + RTC + 256 KB RAM
 - Active-mode MCU: < 53 μA / MHz when RF and SMPS on
 - Radio: Rx 4.5 mA / Tx at 0 dBm 5.2 mA



- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, adaptive real-time accelerator (ART Accelerator) allowing 0-wait-state execution from Flash memory, frequency up to 64 MHz, MPU, 80 DMIPS and DSP instructions
- Performance benchmark
 - 1.25 DMIPS/MHz (Drystone 2.1)
 - 219.48 CoreMark® (3.43 CoreMark/MHz at 64 MHz)
- Energy benchmark
 - 303 ULPMark™ CP score
- Supply and reset management
 - High efficiency embedded SMPS step-down converter with intelligent bypass mode
 - Ultra-safe, low-power BOR (brownout reset) with five selectable thresholds
 - Ultra-low-power POR/PDR
 - Programmable voltage detector (PVD)
 - V_{BAT} mode with RTC and backup registers
- Clock sources
 - 32 MHz crystal oscillator with integrated trimming capacitors (Radio and CPU clock)
 - 32 kHz crystal oscillator for RTC (LSE)
 - Internal low-power 32 kHz (±5%) RC (LSI1)
 - Internal low-power 32 kHz (stability ±500 ppm) RC (LSI2)



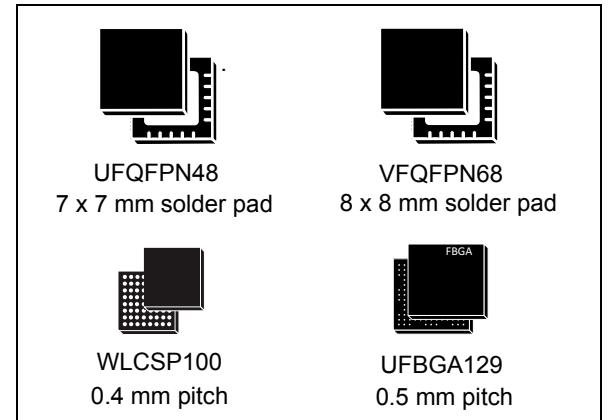
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Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 FPU, Bluetooth® 5.2 and 802.15.4 radio solution

Datasheet - production data

功能

- Include ST state-of-the-art patented technology
- 射频
 - 2.4 GHz- RF收发器支持蓝牙® 5.2规范, IEEE 802.15.4-2011 PHY和MAC, 支持Thread和Zigbee® 3.0- RX灵敏度: -96 dBm (蓝牙® 低功耗于1 Mbps), -100 dBm (802.15.4)- 可编程输出功率高达+6 dBm, 步长1dB- 集成平衡变压器以减少BOM- 支持2Mbps- 专用Arm® 32-bit Cortex® M0+ CPU用于实时射频层- 准确的RSSI用于启用功率控制- 适用于需要符合射频规定的系统ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15和ARIB STD-T66- 支持外部放大器- 可用集成被动元件(IPD)伴随芯片用于优化匹配解决方案(MLPF-WB-01E3或MLPF-WB-02E3)超低功耗平台- 1.71到3.6 V电源- -40 °C到85/105 °C温度范围- 13 nA关闭模式- 600 nA待机模式 + RTC + 32 KB RAM- 2.1 μA停止模式 + RTC + 256 KB RAM- 主动模式MCU: < 53 μA / MHz在RF和SMPS开启时- 射频: 接收4.5mA/传输0dBm 5.2mA
- 核心: Arm® 32-位 Cortex®-M4 CPU配 FPU, 适应实时加速器 (ART 加速器) 允许从闪存内存执行 0 等待状态, 频率高达 64 MHz, MPU, 80 DMIPS 和 DSP 指令
- Performance benchmark
 - 1.25 DMIPS/兆赫 (Drystone 2.1)- 219.48 CoreMark® (3.43 CoreMark/兆赫 在 64 MHz)
- 能量基准- 303 LPMark™ CP 分数
- 供电和复位管理
 - 高效集成 SMPS 降压转换器与智能绕过模式- 超安全, 低功耗 BOR (脱落复位) 具有五个可选阈值- 超低功耗 POR/PDR- 可编程电压探测器 (PVD)- VBAT 模式与 RTC 和备份寄存器
- 时钟源
 - 32 兆赫 晶体 振荡器, 集成 校准 电容器 (射频和 CPU 时钟)- 32 kHz 晶体 振荡器 用于 RTC (LSE)- 内部 低功耗 32 kHz (±5%) RC (LSI1)- 内部 低功耗 32 kHz (稳定性±500 ppm) RC (LSI2)



STM32WB55xx STM32WB35xx

- Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than $\pm 0.25\%$ accuracy)
- High speed internal 16 MHz factory trimmed RC ($\pm 1\%$)
- 2x PLL for system clock, USB, SAI and ADC
- Memories
 - Up to 1 MB Flash memory with sector protection (PCROP) against R/W operations, enabling radio stack and application
 - Up to 256 KB SRAM, including 64 KB with hardware parity check
 - 20x32-bit backup register
 - Boot loader supporting USART, SPI, I2C and USB interfaces
 - OTA (over the air) Bluetooth® Low Energy and 802.15.4 update
 - Quad SPI memory interface with XIP
 - 1 Kbyte (128 double words) OTP
- Rich analog peripherals (down to 1.62 V)
 - 12-bit ADC 4.26 Msps, up to 16-bit with hardware oversampling, 200 μ A/Msp
 - 2x ultra-low-power comparator
 - Accurate 2.5 V or 2.048 V reference voltage buffered output
- System peripherals
 - Inter processor communication controller (IPCC) for communication with Bluetooth® Low Energy and 802.15.4
 - HW semaphores for resources sharing between CPUs
 - 2x DMA controllers (7x channels each) supporting ADC, SPI, I2C, USART, QSPI, SAI, AES, timers
 - 1x USART (ISO 7816, IrDA, SPI Master, Modbus and Smartcard mode)
 - 1x LPUART (low power)
 - 2x SPI 32 Mbit/s
 - 2x I2C (SMBus/PMBus)
 - 1x SAI (dual channel high quality audio)
- 1x USB 2.0 FS device, crystal-less, BCD and LPM
- Touch sensing controller, up to 18 sensors
- LCD 8x40 with step-up converter
- 1x 16-bit, four channels advanced timer
- 2x 16-bit, two channels timer
- 1x 32-bit, four channels timer
- 2x 16-bit ultra-low-power timer
- 1x independent Systick
- 1x independent watchdog
- 1x window watchdog
- Security and ID
 - Secure firmware installation (SFI) for Bluetooth® Low Energy and 802.15.4 SW stack
 - 3x hardware encryption AES maximum 256-bit for the application, the Bluetooth® Low Energy and IEEE802.15.4
 - Customer key storage / key manager services
 - HW public key authority (PKA)
 - Cryptographic algorithms: RSA, Diffie-Helman, ECC over GF(p)
 - True random number generator (RNG)
 - Sector protection against R/W operation (PCROP)
 - CRC calculation unit
 - Die information: 96-bit unique ID
 - IEEE 64-bit unique ID. Possibility to derive 802.15.4 64-bit and Bluetooth® Low Energy 48-bit EUI
- Up to 72 fast I/Os, 70 of them 5 V-tolerant
- Development support
 - Serial wire debug (SWD), JTAG for the application processor
 - Application cross trigger with input / output
 - Embedded Trace Macrocell™ for application
- All packages are ECOPACK2 compliant

Table 1. Device summary

Reference	Part numbers
STM32WB55xx	STM32WB55CC, STM32WB55CE, STM32WB55CG, STM32WB55RC, STM32WB55RE, STM32WB55RG, STM32WB55VC, STM32WB55VE, STM32WB55VG, STM32WB55VY
STM32WB35xx	STM32WB35CC, STM32WB35CE



STM32WB55xx STM32WB35xx

- Internal multispeed 100 kHz to 48 MHz 振荡器, auto-trimmed by LSE (better than $\pm 0.25\%$ 精度)- High speed internal 16 MHz factory trimmed RC ($\pm 1\%$)- 2x PLL for system clock, USB, SAI and ADC
- 内存
 - Up to 1 MB 闪存内存 with sector protection (PCROP) against R/W operations, enabling radio stack and application- Up to 256 KB SRAM, including 64 KB with hardware parity check- 20x32-bit backup register- Boot loader supporting USART, SPI, I2C and USB interfaces- OTA (over the air) 蓝牙® Low Energy and 802.15.4 update- Quad SPI memory interface with XIP- 1 Kbyte (128 double words) OTP• Rich analog peripherals (down to 1.62 V)- 12-bit ADC 4.26 兆赫, up to 16-bit with hardware oversampling, 200 μ A/Msp- 2x ultra-low-power comparator- Accurate 2.5 V or 2.048 V reference voltage buffered output• System peripherals- I nter processor communication controller (IPCC) for communication with Bluetooth® Low Energy and 802.15.4- HW semaphores for resources sharing between CPUs- 2x DMA controllers (7x channels each) supporting ADC, SPI, I2C, USART, QSPI, SAI, AES, timers- 1x USART (ISO 7816, IrDA, SPI Master, Modbus and Smartcard mode)- 1x LPUART (low power)- 2x SPI 32 Mbit/s- 2x I2C (SMBus/PMBus)- 1x SAI (dual channel high quality audio)
- Security and ID
 - Secure firmware installation (SFI) for Bluetooth® Low Energy and 802.15.4 SW stack
 - 3x hardware encryption AES maximum 256-bit for the application, the Bluetooth® Low Energy and IEEE802.15.4
 - Customer key storage / key manager services
 - HW public key authority (PKA)
 - Cryptographic algorithms: RSA, Diffie-Helman, ECC over GF(p)
 - True random number generator (RNG)
 - Sector protection against R/W operation (PCROP)
 - CRC calculation unit
 - Die information: 96-bit unique ID
 - IEEE 64-bit unique ID. Possibility to derive 802.15.4 64-bit and Bluetooth® Low Energy 48-bit EUI
- Up to 72 fast I/Os, 70 of them 5 V-tolerant
- Development support
 - Serial wire debug (SWD), JTAG for the application processor
 - Application cross trigger with input / output
 - Embedded Trace Macrocell™ for application
- All packages are ECOPACK2 compliant

表格 1. 设备摘要

Reference	Part numbers
STM32WB55xx	STM32WB55CC, STM32WB55CE, STM32WB55CG, STM32WB55RC, STM32WB55RE, STM32WB55RG, STM32WB55VC, STM32WB55VE, STM32WB55VG, STM32WB55VY
STM32WB35xx	STM32WB35CC, STM32WB35CE



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1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32WB55xx and STM32WB35xx microcontrollers, based on Arm® cores^(a).

This document must be read in conjunction with the reference manual (RM0434), available from the STMicroelectronics website www.st.com.

For information on the device errata with respect to the datasheet and reference manual refer to the STM32WB55xx and STM32WB35xx errata sheet (ES0394), available from the STMicroelectronics website www.st.com.

For information on the Arm® Cortex®-M4 and Cortex®-M0+ cores, refer, respectively, to the Cortex®-M4 Technical Reference Manual and to the Cortex®-M0+ Technical Reference Manual, both available on the www.arm.com website.

For information on 802.15.4 refer to the IEEE website (www.ieee.org).

For information on Bluetooth® refer to www.bluetooth.com.



1 Introduction

本文档提供了STM32WB55xx和STM32WB35xx微控制器的订购信息和机械设备特性，基于Arm® 核心(a)。

此文档必须与参考手册同时阅读 (RM0434)，可以从 STMicroelectronics 网站获得 www.st.com。

有关设备 errata 信息，与数据手册和参考手册相比，请参考 STM32WB55xx 和 STM32WB35xx errata 表格 (ES0394)，可以从 STMicroelectronics 网站获得 www.st.com。

有关 Cortex-M4 和 Cortex-M0+ 核心的信息，请分别参考 Cortex-M4 技术参考手册和 Cortex-M0+ 技术参考手册，两者都可在 www.arm.com 网站上获得。

有关 802.15.4 的信息，请参考 IEEE 网站 (www.ieee.org)。

有关 蓝牙 的信息，请参考 www.bluetooth.com。



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e US and/or elsewhere.

STM32WB55xx STM32WB35xx	Description	STM32WB55xx STM32WB35xx	描述
<h2>2 Description</h2> <p>The STM32WB55xx and STM32WB35xx multiprotocol wireless and ultra-low-power devices embed a powerful and ultra-low-power radio compliant with the Bluetooth® Low Energy SIG specification 5.2 and with IEEE 802.15.4-2011. They contain a dedicated Arm® Cortex®-M0+ for performing all the real-time low layer operation.</p> <p>The devices are designed to be extremely low-power and are based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 64 MHz. This core features a Floating point unit (FPU) single precision that supports all Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) that enhances application security.</p> <p>Enhanced inter-processor communication is provided by the IPCC with six bidirectional channels. The HSEM provides hardware semaphores used to share common resources between the two processors.</p> <p>The devices embed high-speed memories (up to 1 Mbyte of Flash memory for STM32WB55xx, up to 512 Kbytes for STM32WB35xx, up to 256 Kbytes of SRAM for STM32WB55xx, 96 Kbytes for STM32WB35xx), a Quad-SPI Flash memory interface (available on all packages) and an extensive range of enhanced I/Os and peripherals.</p> <p>Direct data transfer between memory and peripherals and from memory to memory is supported by fourteen DMA channels with a full flexible channel mapping by the DMAMUX peripheral.</p> <p>The devices feature several mechanisms for embedded Flash memory and SRAM: readout protection, write protection and proprietary code readout protection. Portions of the memory can be secured for Cortex® -M0+ exclusive access.</p> <p>The two AES encryption engines, PKA and RNG enable lower layer MAC and upper layer cryptography. A customer key storage feature may be used to keep the keys hidden.</p> <p>The devices offer a fast 12-bit ADC and two ultra-low-power comparators associated with a high accuracy reference voltage generator.</p> <p>These devices embed a low-power RTC, one advanced 16-bit timer, one general-purpose 32-bit timer, two general-purpose 16-bit timers, and two 16-bit low-power timers.</p> <p>In addition, up to 18 capacitive sensing channels are available for STM32WB55xx (not on UFQFPN48 package). The STM32WB55xx also embed an integrated LCD driver up to 8x40 or 4x44, with internal step-up converter.</p> <p>The STM32WB55xx and STM32WB35xx also feature standard and advanced communication interfaces, namely one USART (ISO 7816, IrDA, Modbus and Smartcard mode), one low-power UART (LPUART), two I2Cs (SMBus/PMBus), two SPIs (one for STM32WB35xx) up to 32 MHz, one serial audio interface (SAI) with two channels and three PDMs, one USB 2.0 FS device with embedded crystal-less oscillator, supporting BCD and LPM and one Quad-SPI with execute-in-place (XIP) capability.</p> <p>The STM32WB55xx and STM32WB35xx operate in the -40 to +105 °C (+125 °C junction) and -40 to +85 °C (+105 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes enables the design of low-power applications.</p> <p>The devices include independent power supplies for analog input for ADC.</p>	<h2>2 描述</h2> <p>The STM32WB55xx and STM32WB35xx multiprotocol wireless and ultra-low-power devices embed a powerful and ultra-low-power radio compliant with the Bluetooth® Low Energy SIG specification 5.2 and with IEEE 802.15.4-2011. They contain a dedicated Arm® Cortex®-M0+ for performing all the real-time low layer operation.</p> <p>这些设备设计用于极低功耗，基于高性能的 Arm® Cortex®-M4 32 RISC 核心，在频率达到 64 MHz 的情况下运行。此核心具有 Floating point unit (FPU) single precision，支持所有 Arm® single-precision 数据处理指令和数据类型。它还实现了完整的 DSP 指令集和内存保护单元 (MPU)，以提高应用安全性。</p> <p>增强的跨处理器通信由 IPCC 提供，具有六个双向通道。HSEM 提供硬件信号量，用于在两个处理器之间共享公共资源。</p> <p>这些设备嵌入了高速内存 (最多 1 Mbyte 的闪存内存用于 STM32WB55xx，最多 512 Kbytes 于 STM32WB35xx，最多 256 Kbytes 的 SRAM 于 STM32WB55xx，96 Kbytes 于 STM32WB35xx)，一个 Quad-SPI 闪存接口(可在所有包装)上使用，并且具有广泛的增强输入/输出和外围设备。</p> <p>Direct data transfer between memory and peripherals and from memory to memory is supported by fourteen DMA channels with a full flexible channel mapping by the DMAMUX peripheral.</p> <p>The devices feature several mechanisms for embedded Flash memory and SRAM: readout protection, write protection and proprietary code readout protection. Portions of the memory can be secured for Cortex® -M0+ exclusive access.</p> <p>The two AES encryption engines, PKA and RNG enable lower layer MAC and upper layer cryptography. A customer key storage feature may be used to keep the keys hidden.</p> <p>The devices offer a fast 12-bit ADC and two ultra-low-power comparators associated with a high accuracy reference voltage generator.</p> <p>These devices embed a low-power RTC, one advanced 16-bit timer, one general-purpose 32-bit timer, two general-purpose 16-bit timers, and two 16-bit low-power timers.</p> <p>In addition, up to 18 capacitive sensing channels are available for STM32WB55xx (not on UFQFPN48 package). The STM32WB55xx also embed an integrated LCD driver up to 8x40 or 4x44, with internal step-up converter.</p> <p>STM32WB55xx 和 STM32WB35xx 也具有标准和高级的通信接口，分别为一个 USART (ISO 7816, IrDA, Modbus 和 Smartcard mode), 低功耗 UART (LPUART), 一个 I2C (SMBus/PMBus), 一个 SPI (用于 STM32WB35xx) 最高 32 MHz, 一个串行音频接口 (SAI) 带有两个通道和三个 PDMs, 一个 USB 2.0 FS 设备带有嵌入式无晶体振荡器，支持 BCD 和 LPM，以及一个 Quad-SPI 带有执行在原地 (XIP) 功能。</p> <p>STM32WB55xx 和 STM32WB35xx 在 -40 到 +105 °C (+125 °C 节点) 和 -40 到 +85 °C (+105 °C 节点) 温度范围内运行，电源为 1.71V 到 3.6V 电源。一套全面的电源省电模式可以实现低功耗应用的设计。</p> <p>设备包括模拟输入的独立电源，用于ADC。</p>		

Description	STM32WB55xx	STM32WB35xx	描述	STM32WB55xx	STM32WB35xx								
The STM32WB55xx and STM32WB35xx integrate a high efficiency SMPS step-down converter with automatic bypass mode capability when the V_{DD} falls below V_{BORx} ($x=1, 2, 3, 4$) voltage level (default is 2.0 V). It includes independent power supplies for analog input for ADC and comparators, as well as a 3.3 V dedicated supply input for USB.			The STM32WB55xx and STM32WB35xx integrate a high efficiency SMPS 下降转换器 with automatic bypass mode capability when the V_{DD} falls below V_{BORx} ($=1 2 3 \times, 4$) ⁴⁾ , voltage level default is .V. It includes independent power supplies for analog input for ADC and comparators, as well as a 3.3伏 dedicated supply input for USB.										
A V_{BAT} dedicated supply allows the devices to back up the LSE 32.768 kHz oscillator, the RTC and the backup registers, thus enabling the STM32WB55xx and STM32WB35xx to supply these functions even if the main V_{DD} is not present through a CR2032-like battery, a Supercap or a small rechargeable battery.			A V_{BAT} dedicated supply allows the devices to back up the LSE 32.768 kHz oscillator, the RTC and the backup registers, thus enabling the STM32WB55xx and STM32WB35xx to supply these functions even if the main V_{DD} is not present through a CR2032-like battery, a Supercap or a small rechargeable battery.										
The STM32WB55xx offer four packages, from 48 to 129 pins. The STM32WB35xx offer one package, 48 pins.			STM32WB55xx 提供四种包装，引脚数从48到129个。STM32WB35xx 提供一种包装，48个引脚。	e									
Table 2. STM32WB55xx and STM32WB35xx devices features and peripheral counts													
Feature	STM32WB55Cx			STM32WB55Rx			STM32WB55Vx			STM32WB35Cx			
Memory density (bytes)	Flash	256 K	512 K	1 M	256 K	512 K	1 M	256 K	512 K	1 M	640 K	256 K	512 K
	SRAM	128 K	256 K	256 K	128 K	256 K	256 K	128 K	256 K	256 K	256 K	96 K	
	SRAM1	64 K	192 K	64 K	192 K	64 K	192 K	64 K	192 K	64 K	192 K	32 KB	
	SRAM2	64 K											
BLE	5.2 (2 Mbps)												
802.15.4	Yes												
Timers	Advanced	1 (16 bits)											
	General purpose	2 (16 bits) + 1 (32 bits)											
	Low power	2 (16 bits)											
	SysTick	1											
Communication interfaces	SPI	1	2	2	1								
	I2C	2											
	USART ⁽¹⁾	1											
	LPUART	1											
	SAI	2 channels											
	USB FS	Yes											
	QSPI	1											
RTC	1												
Tamper pin	1	3	3	1									
Wakeup pin	2	5	5	2									
LCD, COMxSEG	Yes, 4x13	Yes, 4x28	Yes, 8x40 or 4x44	No									
GPIOs	30	49	72	30									
Capacitive sensing	No	6	18	No									
12-bit ADC Number of channels	13 channels (incl. 3 internal)	19 channels (incl. 3 internal)	13 channels (incl. 3 internal)										
Internal V_{ref}	Yes												

Table 2. STM32WB55xx and STM32WB35xx devices features and peripheral counts (continued)

Feature	STM32WB55Cx	STM32WB55Rx	STM32WB55Vx	STM32WB35Cx	Description
Analog comparator			2		
Max CPU frequency			64 MHz		
Operating temperature	Ambient	-40 to +85 and -40 to +105 °C	-40 to +85 °C	-40 to +85 and -40 to +105 °C	
	Junction	-40 to +105 and -40 to +125 °C	-40 to +105 °C	-40 to +105 and -40 to +125 °C	
Operating voltage			1.71 to 3.6 V		
Package	UFQFPN48 7 mm x 7 mm 0.5 mm pitch, solder pad	VFQFPN68 8 mm x 8 mm 0.4 mm pitch, solder pad	WLCSP100 0.4 mm pitch	UFQFPN48 7 mm x 7 mm 0.5 mm pitch, solder pad	
			UFBGA129 0.5 mm pitch	-	

1. USART peripheral can be used as SPI.

表2. STM32WB55xx 和 STM32WB35xx 设备功能和外围设备计数 (继续)

Feature	STM32WB55Cx	STM32WB55Rx	STM32WB55Vx	STM32WB35Cx	Description
Analog comparator			2		
Max CPU frequency			64 MHz		
Operating temperature	Ambient	-40 to +85 and -40 to +105 °C	-40 to +85 °C	-40 to +85 and -40 to +105 °C	
	Junction	-40 to +105 and -40 to +125 °C	-40 to +105 °C	-40 to +105 and -40 to +125 °C	
Operating voltage			1.71 to 3.6 V		
Package	UFQFPN48 7 mm x 7 mm 0.5 mm pitch, solder pad	VFQFPN68 8 mm x 8 mm 0.4 mm pitch, solder pad	WLCSP100 0.4 mm pitch	UFQFPN48 7 mm x 7 mm 0.5 mm pitch, solder pad	
			UFBGA129 0.5 mm pitch	-	

1. USART peripheral can be used as SPI.

Figure 1. STM32WB55xx block diagram

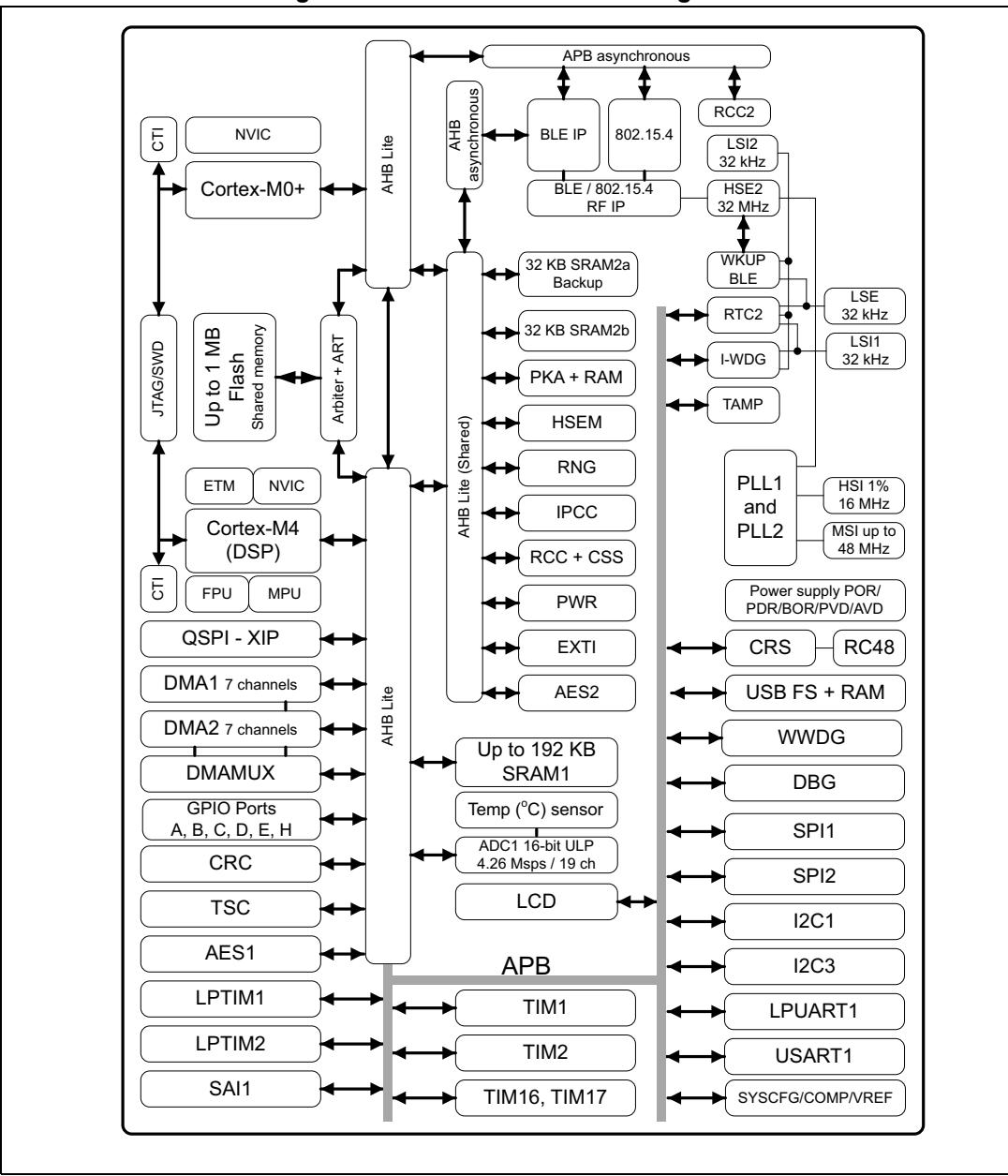


图 1. STM32WB55xx 块图

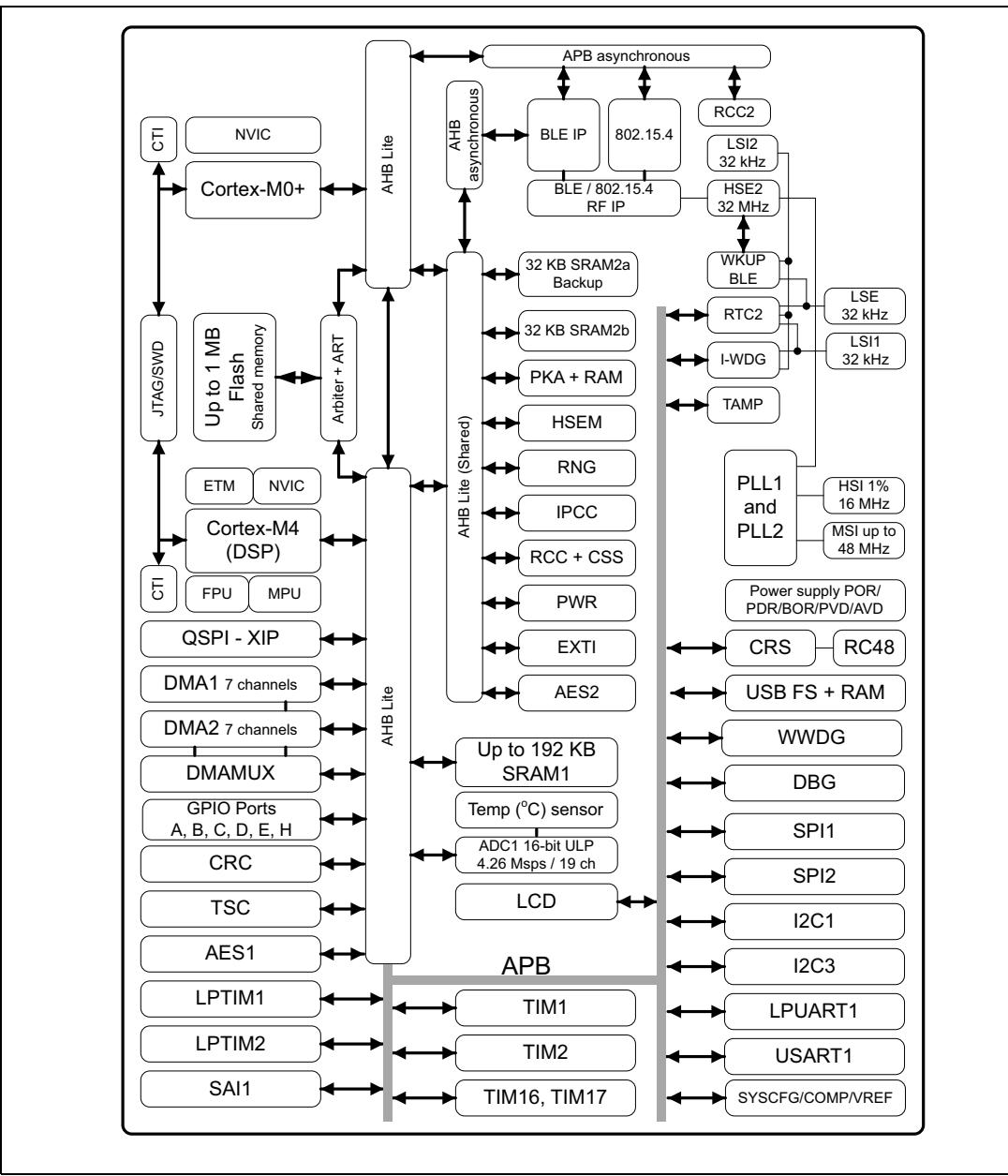


Figure 2. STM32WB35xx block diagram

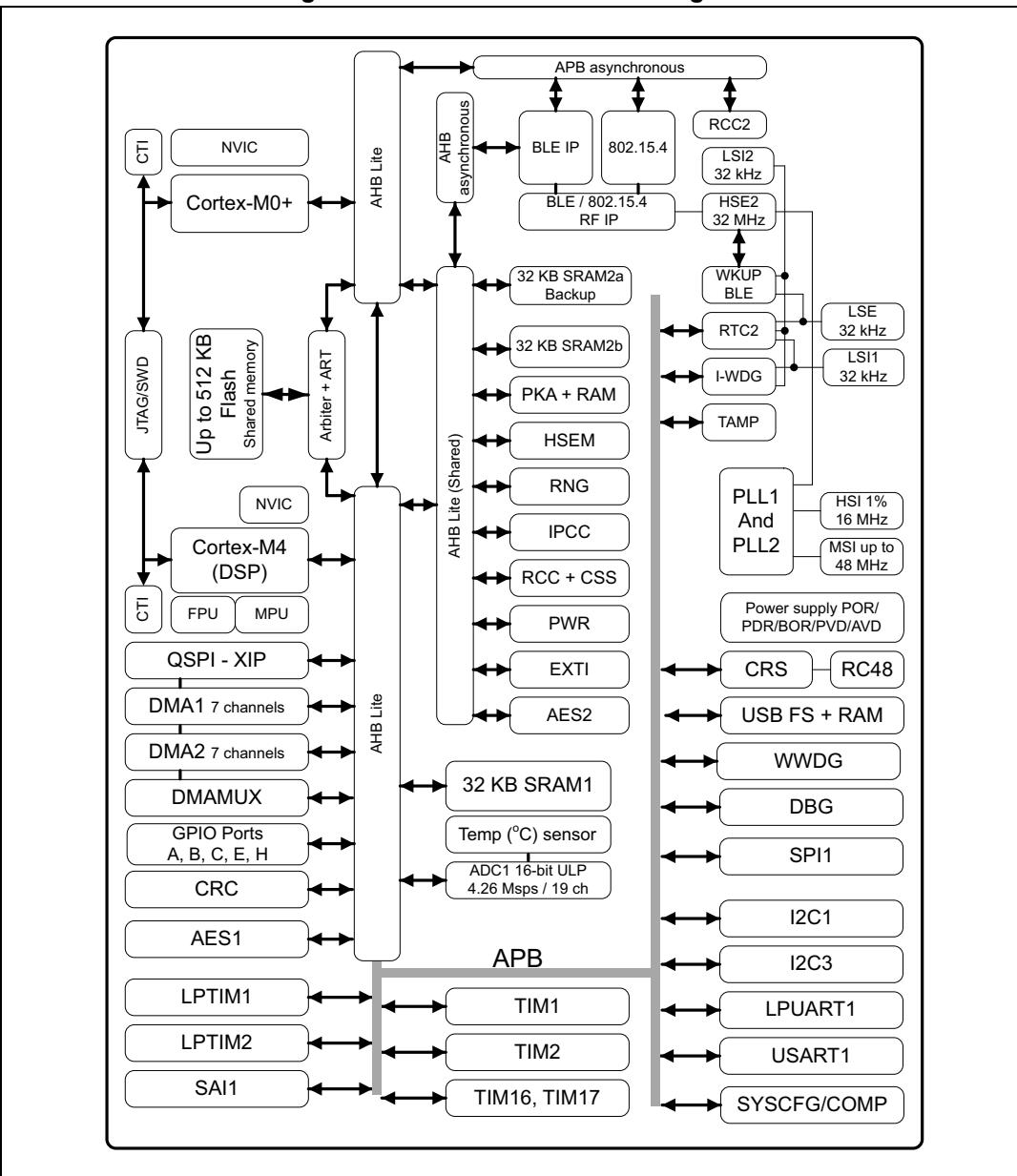
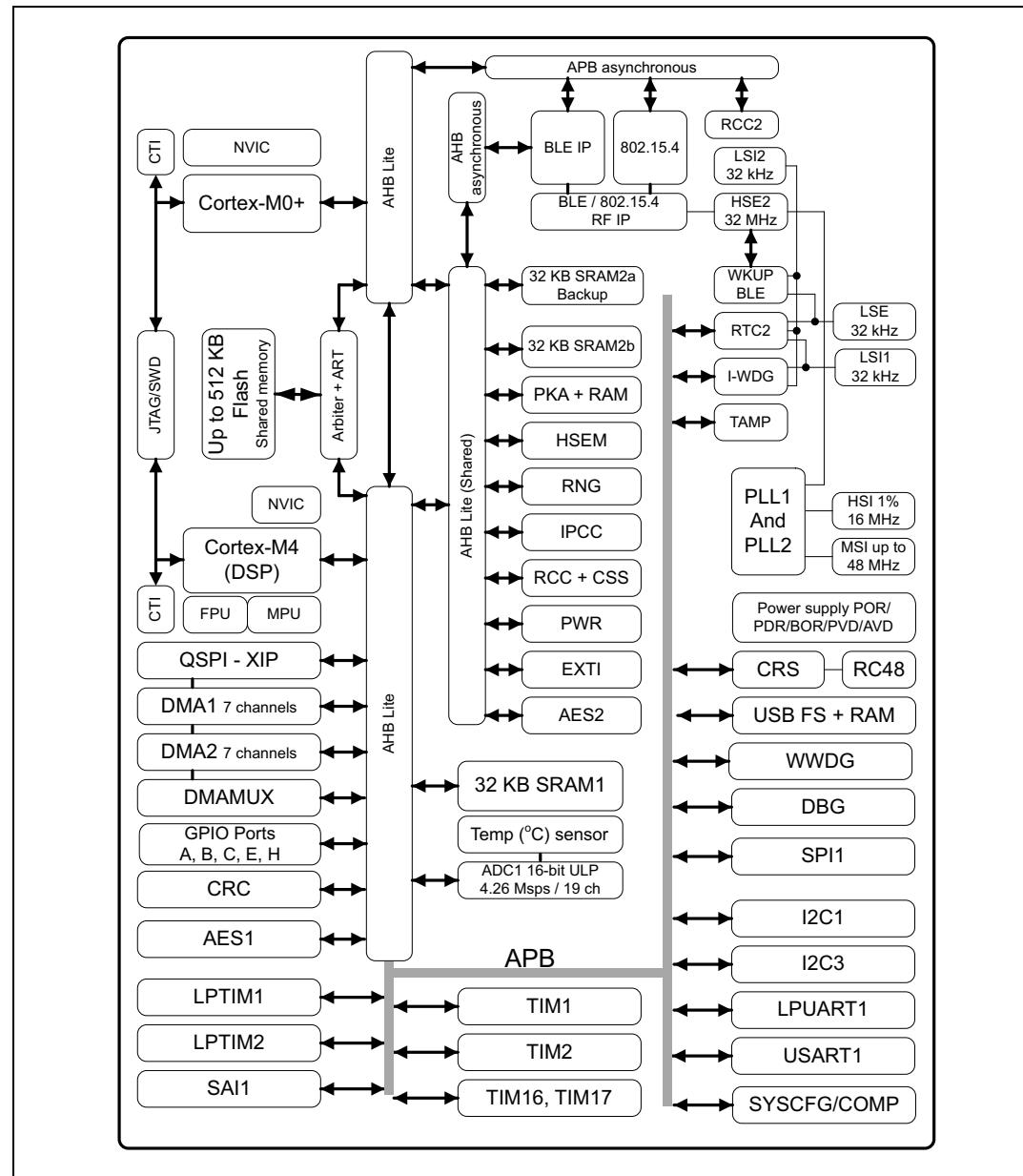


图2. STM32WB35xx 块图



3 Functional overview

3.1 Architecture

The STM32WB55xx and STM32WB35xx multiprotocol wireless devices embed a BLE and an 802.15.4 RF subsystem that interfaces with a generic microcontroller subsystem using an Arm® Cortex®-M4 CPU (called CPU1) on which the host application resides.

The RF subsystem is composed of an RF analog front end, BLE and 802.15.4 digital MAC blocks as well as of a dedicated Arm® Cortex®-M0+ microcontroller (called CPU2), plus proprietary peripherals. The RF subsystem performs all of the BLE and 802.15.4 low layer stack, reducing the interaction with the CPU1 to high level exchanges.

Some functions are shared between the RF subsystem CPU (CPU2) and the Host CPU (CPU1):

- Flash memories
- SRAM1, SRAM2a and SRAM2b (SRAM2a can be retained in Standby mode)
- Security peripherals (RNG, AES1, PKA)
- Clock RCC
- Power control (PWR)

The communication and the sharing of peripherals between the RF subsystem and the Cortex®-M4 CPU is performed through a dedicated inter processor communication controller (IPCC) and semaphore mechanism (HSEM).

3.2 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU is a processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm® core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions enabling efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded Arm® core, the STM32WB55xx and STM32WB35xx are compatible with all Arm® tools and software.

[Figure 1](#) and [Figure 2](#) show the general block diagram of, respectively, the STM32WB55xx and STM32WB35xx devices.

3 功能概述

3.1 架构

STM32WB55xx 和 STM32WB35xx 多协议无线设备集成了一个蓝牙和 802.15.4 无线电子子系统，通过 Arm® Cortex®-M4 CPU (称为 CPU1) 的通用微控制器子系统进行接口，主机应用程序运行在此上。

无线电子子系统由一个无线电模拟前端、蓝牙和 802.15.4 数字MAC块以及一个专门的 Arm® Cortex®-M0+ 微控制器 (称为 CPU2)组成，还包含专有外设。无线电子子系统执行所有蓝牙和 802.15.4 低层堆叠，减少了与 CPU1 的交互，只保留高电平交互。

一些函数在无线电子子系统 CPU (CPU2) 和主机 CPU(CPU1)之间共享：

- 闪存内存
- SRAM1, SRAM2a 和 SRAM2b (SRAM2a 可以在待机模式下保持不变)
- 安全外设 (随机数生成器, AES1, PKA)
- 时钟RCC
- 电源控制 (PWR)

The communication and the sharing of peripherals between the RF subsystem and the Cortex®-M4 CPU is performed through a dedicated inter processor communication controller (IPCC) and semaphore mechanism (HSEM).

3.2 Arm® Cortex®-M4 核心配备浮点单元

The Arm® Cortex®-M4 with FPU is a processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32位精简指令集处理器 features exceptional code-efficiency, delivering the high-performance expected from an Arm® core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions enabling efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded Arm® core, the STM32WB55xx and STM32WB35xx are compatible with all Arm® tools and software.

[Figure 1](#) and [Figure 2](#) show the general block diagram of, respectively, the STM32WB55xx and STM32WB35xx devices.

3.3 Memories

3.3.1 Adaptive real-time memory accelerator (ART Accelerator)

The ART Accelerator is a memory accelerator optimized for STM32 industry-standard Arm® Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, which normally require the processor to wait for the Flash memory at higher frequencies.

To release the processor near 80 DMIPS performance at 64 MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 64 MHz.

3.3.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU1 accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to eight protected areas, which can be divided up into eight subareas. The protection area sizes are between 32 bytes and the whole 4 Gbytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code must be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location prohibited by the MPU, the RTOS detects it and takes action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.3.3 Embedded Flash memory

The STM32WB55xx and STM32WB35xx devices feature, respectively, up to 1 Mbyte and 512 Kbytes of embedded Flash memory available for storing programs and data, as well as some customer keys.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
 - Level 0: no readout protection
 - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in SRAM or bootloader is selected
 - Level 2: chip readout protection: debug features (Cortex®-M4 and Cortex®-M0+ JTAG and serial wire), boot in SRAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

3.3 内存

3.3.1 适应实时内存加速器 (ART 加速器)

ART 加速器是一种为 STM32 业标 Arm® Cortex®-M4 处理器优化的内存加速器。它平衡了 Arm® Cortex®-M4 对闪存技术的固有性能优势，后者通常需要处理器在更高频率下等待闪存。

为了在 64 MHz 下释放接近 80 DMIPS 的性能，该加速器实现了指令预取队列和分支缓存，从而提高了从 64 位闪存中执行程序的速度。基于 CoreMark 基准测试，由 ART 加速器实现的性能相当于在 CPU 频率最高为 64 MHz 时从闪存中进行 0 等待状态程序执行。

3.3.2 内存保护单元

内存保护单元 (MPU) 用于管理 CPU1 对内存的访问，以防止一个任务意外损坏其他任何活动任务使用的内存或资源。此内存区域组织成多达八个受保护区域，这些区域可以分割成八个子区域。受保护区域的大小介于 32 字节和可寻址的整个 4 GB 内存之间。

MPU 尤其适用于需要保护一些关键或认证代码免受其他任务不当行为影响的应用程序。通常由实时操作系统 (real-time operating system) 管理。如果一个程序访问了 MPU 禁止访问的内存位置，RTOS 将检测到并采取行动。在 RTOS 环境中，内核可以根据要执行的进程动态更新 MPU 配置区域。

MPU 是可选的，并且可以为不需要它的应用程序进行绕过。

3.3.3 嵌入式闪存内存

STM32WB55xx 和 STM32WB35xx 设备分别提供最多 1 Mbyte 和 512 Kbytes 的嵌入式闪存内存，用于存储程序和数据，以及一些客户密钥。

通过选项字节可以配置灵活的保护措施：

- 阅读保护 (RDP) 用于保护整个内存。有三个水平可用：
 - 级别 0: 无阅读保护 – 级别 1: 内存阅读保护: 如果调试功能连接，或者在 SRA M 中启动或选择引导加载程序，则无法从或向 Flash 内存进行读取 – 级别 2: 芯片阅读保护: 调试功能 (Cortex®-M4 和 Cortex®-M0+JTAG 和 串行线缆)，在 SRAM 中启动和引导加载程序选择被禁用 (JTAG 熔丝)。这个选择是不可逆的。

Table 3. Access status vs. readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from SRAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No ⁽¹⁾	No ⁽¹⁾	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A ⁽²⁾	No	No	N/A ⁽²⁾
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2a SRAM2b	1	Yes	Yes	Yes ⁽²⁾	No	No	No ⁽²⁾
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. The option byte can be modified by the RF subsystem.

2. Erased when RDP changes from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas can be selected, with 4-Kbyte granularity.
- Proprietary code readout protection (PCROP): two parts of the Flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. Two areas can be selected, with 2-Kbyte granularity. An additional option bit (PCROP_RDP) makes possible to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

A section of the Flash memory is secured for the RF subsystem CPU2, and cannot be accessed by the host CPU1.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- single error detection and correction
- double error detection
- the address of the ECC fail can be read in the ECC register

The embedded Flash memory is shared between CPU1 and CPU2 on a time sharing basis. A dedicated HW mechanism allows both CPUs to perform Write/Erase operations.

表 3. 访问状态与读取保护级别和执行模式

Area	Protection level	User execution			Debug, boot from SRAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No ⁽¹⁾	No ⁽¹⁾	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A ⁽²⁾	No	No	N/A ⁽²⁾
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2a SRAM2b	1	Yes	Yes	Yes ⁽²⁾	No	No	No ⁽²⁾
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. The option byte can be modified by the RF subsystem.

2. Erased when RDP changes from Level 1 to Level 0.

- 写入保护 (WRP): 受保护区域对擦除和编程进行了保护。可以选择两个区域，具有 4-K 字节粒度。
- Proprietary code readout protection (PCROP): 闪存内存的两部分可以对第三方的读取和写入进行保护。受保护区域是只执行的：它只能由 STM32 CPU 访问，作为指令代码，而所有其他访问 (DMA, debug and CPU data read, write and erase) 都被严格禁止。可以选择两个区域，具有 2-K 字节粒度。一个附加的选项位 (PCROP_RDP) 允许选择当 RDP 保护从 级别 1 更改为 级别 0 时，PCROP 区域是否被擦除。

闪存内存的一部分用于 RF 子系统 CPU2，并且不能被主机 CPU1 访问。

T整个非易失性内存嵌入了错误修复码 (ECC) 功能，支持：

- 单错误检测和修复
- 双错误检测
- ECC 失败的地址可以在 ECC 寄存器中读取

嵌入式闪存内存存在 CPU1 和 CPU2 之间共享，基于时间共享基础。一个专门的硬件机制允许两个 CPU 执行写/擦除操作。

3.3.4 Embedded SRAM

The STM32WB55xx devices feature up to 256 Kbytes of embedded SRAM, split in three blocks:

- **SRAM1:** up to 192 Kbytes mapped at address 0x2000 0000
- **SRAM2a:** 32 Kbytes located at address 0x2003 0000 also mirrored at 0x1000 0000, with hardware parity check (this SRAM can be retained in Standby mode)
- **SRAM2b:** 32 Kbytes located at address 0x2003 8000 (contiguous with SRAM2a) and mirrored at 0x1000 8000 with hardware parity check

The STM32WB35xx devices feature 96 Kbytes of embedded SRAM, split in three blocks:

- **SRAM1:** 32 Kbytes mapped at address 0x2000 0000
- **SRAM2a:** 32 Kbytes located at address 0x2003 0000 also mirrored at 0x1000 0000, with hardware parity check (this SRAM can be retained in Standby mode)
- **SRAM2b:** 32 Kbytes located at address 0x2003 8000 (contiguous with SRAM2a) and mirrored at 0x1000 8000 with hardware parity check

SRAM2a and SRAM2b can be write-protected, with 1-Kbyte granularity. A section of the SRAM2a and SRAM2b is secured for the RF sub-system and cannot be accessed by the host CPU1.

The SRAMs can be accessed in read/write with 0 wait states for all CPU1 and CPU2 clock speeds.

3.4 Security and safety

The STM32WB55xx and STM32WB35xx contain many security blocks both for the BLE or IEEE 802.15.4 and the Host application.

It includes:

- Customer storage of the BLE and 802.15.4 keys
- Secure Flash memory partition for RF subsystem-only access
- Secure SRAM partition, that can be accessed only by the RF subsystem
- True random number generator (RNG)
- Advance encryption standard hardware accelerators (AES-128bit and AES-256bit, supporting chaining modes ECB, CBC, CTR, GCM, GMAC, CCM)
- Private key acceleration (PKA) including:
 - Modular arithmetic including exponentiation with maximum modulo size of 3136 bits
 - Elliptic curves over prime field scalar multiplication, ECDSA signature, ECDSA verification with maximum modulo size of 521 bits
- Cyclic redundancy check calculation unit (CRC)

A specific mechanism is in place to ensure that all the code executed by the RF subsystem CPU2 can be secure, whatever the Host application. For the AES1 a customer key can be managed by the CPU2 and used by the CPU1 to encrypt/decrypt data.

3.3.4 内置SRAM

The STM32WB55xx devices feature up to 256 Kbytes of embedded SRAM, split in three blocks:

- **SRAM1:** 最多 192 Kbytes 映射在地址 0x2000 0000• **SRAM2a:** 32 Kbytes 位于地址 0x2003 0000, 也镜像在 0x1000 0000, 配备硬件奇偶校验 (这个 SRAM 可以在待机模式下保留)• **SRAM2b:** 32 Kbytes 位于地址 0x2003 8000 (与 SRAM2a 连续) 并镜像在 0x1000 8000, 配备硬件奇偶校验

STM32WB35xx 设备具有 96 Kbytes 的内置SRAM, 分为三个块:

- **SRAM1:** 32 Kbytes 映射在地址 0x2000 0000• **SRAM2a:** 32 Kbytes 位于地址 0x2003 0000 也镜像在 0x1000 0000, 配备硬件奇偶校验 (这个 SRAM 可以在待机模式下保留)• **SRAM2b:** 32 Kbytes 位于地址 0x2003 8000 (与 SRAM2a 连续) 并镜像在 0x1000 8000, 配备硬件奇偶校验

SRAM2a 和 SRAM2b 可以被写保护, 粒度为 1-Kbyte。SRAM2a 和 SRAM2b 的一部分用于 RF子系统, 并且不能被主机 CPU1 访问。

内存可以以 0 等待状态在所有 CPU1 和 CPU2 时钟速度下进行读/写访问。

3.4 安全性和安全性

STM32WB55xx 和 STM32WB35xx 包含了 BLE 和 IEEE 802.15.4 以及主机应用程序的许多安全块。 r

它包括:

- BLE 和 802.15.4 密钥的客户存储• 仅限无线电子子系统访问的安全闪存内存分区
- 仅能由 RF子系统 访问的安全 SRAM 分区• 真正的随机数生成器 (RNG)• 高级加密标准硬件加速器 (AES-128 位和 AES-256 位, 支持链式模式 ECB, CBC, CTR, GCM, GMAC, CCM)• 私加速 (PKA) 包括:- 最大模大小为3136位的模运算, 包括幂运算- 椭圆曲线在素域上的标数乘法, ECDSA 签名, ECDSA 验证, 最大模大小为 521 位
- 循环冗余校验计算单元 (CRC)

为了确保无论主机应用程序如何, RF子系统 CPU2 执行的所有代码都是安全的, 已经实施了一种特定机制。对于 AES1, 客户密钥可以由 CPU2 管理, 并由 CPU1 用于加密/解密数据。

3.5 Boot modes and FW update

At startup, BOOT0 pin and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The devices always boot on CPU1 core. The embedded bootloader code makes it possible to boot from various peripherals:

- USB
- UART
- I2C
- SPI

Secure Firmware update (especially BLE and 802.15.4) from system boot and over the air is provided.

3.6 RF subsystem

The STM32WB55xx and STM32WB35xx embed an ultra-low power multi-standard radio Bluetooth® Low Energy (BLE) and 802.15.4 network processor, compliant with Bluetooth® specification 5.2 and IEEE® 802.15.4-2011. The BLE features 1 Mbps and 2 Mbps transfer rates, supports multiple roles simultaneously acting at the same time as BLE sensor and hub device, embeds Elliptic Curve Diffie-Hellman (ECDH) key agreement protocol, thus ensuring a secure connection.

The BLE stack and 802.15.4 Low Level layer run on an embedded Arm® Cortex®-M0+ core (CPU2). The stack is stored on the embedded Flash memory, which is also shared with the Arm® Cortex®-M4 (CPU1) application, making it possible in-field stack update.

3.6.1 RF front-end block diagram

The RF front-end is based on a direct modulation of the carrier in Tx, and uses a low IF architecture in Rx mode.

Thanks to an internal transformer at RF pins, the circuit directly interfaces the antenna (single ended connection, impedance close to $50\ \Omega$). The natural bandpass behavior of the internal transformer, simplifies outside circuitry aimed for harmonic filtering and out of band interferer rejection.

In Transmit mode, the maximum output power is user selectable through the programmable LDO voltage of the power amplifier. A linearized, smoothed analog control offers clean power ramp-up.

In receive mode the circuit can be used in standard high performance or in reduced power consumption (user programmable). The Automatic gain control (AGC) is able to reduce the chain gain at both RF and IF locations, for optimized interference rejection. Thanks to the use of complex filtering and highly accurate I/Q architecture, high sensitivity and excellent linearity can be achieved.

The bill of material is reduced thanks to the high degree of integration. The radio frequency source is synthesized from an external 32 MHz crystal that does not need any external

3.5 启动模式和固件更新

At startup, BOOT0 引脚 and BOOT1 选项位 are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

设备总是在 CPU1 核心上启动。内置引导加载程序代码使其能够从各种外围设备启动：

- USB
- UART
- I2C
- SPI

Secure Firmware update (especially BLE and 802.15.4) from system boot and over the air is provided.

3.6 RF subsystem

STM32WB55xx 和 STM32WB35xx 集成了一个超低功耗的多协议射频 Bluetooth® Low Energy (BLE) 和 802.15.4 网络处理器，符合 Bluetooth® 规范 5.2 和 IEEE® 802.15.4-2011。BLE 功能包括 1 Mbps 和 2 Mbps 的传输速率，支持同时扮演 BLE 传感器和中心设备的多个角色，集成了椭圆曲线 Diffie-Hellman (ECDH) 密钥协商协议，从而确保安全连接。

蓝牙堆栈和 802.15.4 低层次层运行在嵌入式 Arm® Cortex®-M0+ core(CPU2) 上。堆栈存储在嵌入式闪存内存中，这也与 Arm® Cortex®-M4 (CPU1) 应用共享，使得现场堆栈更新成为可能。

3.6.1 RF 前端块图

RF 前端基于 Tx 中载波的直接调制，并在 Rx 模式下使用低中间频率架构。

感谢 RF 接口上的内部变压器，电路直接通过单端连接将天线(连接到阻抗接近 $50\ \Omega$)的位置。内部变压器的自然带通行为简化了旨在进行谐波滤波和外带干扰拒绝的外部电路。

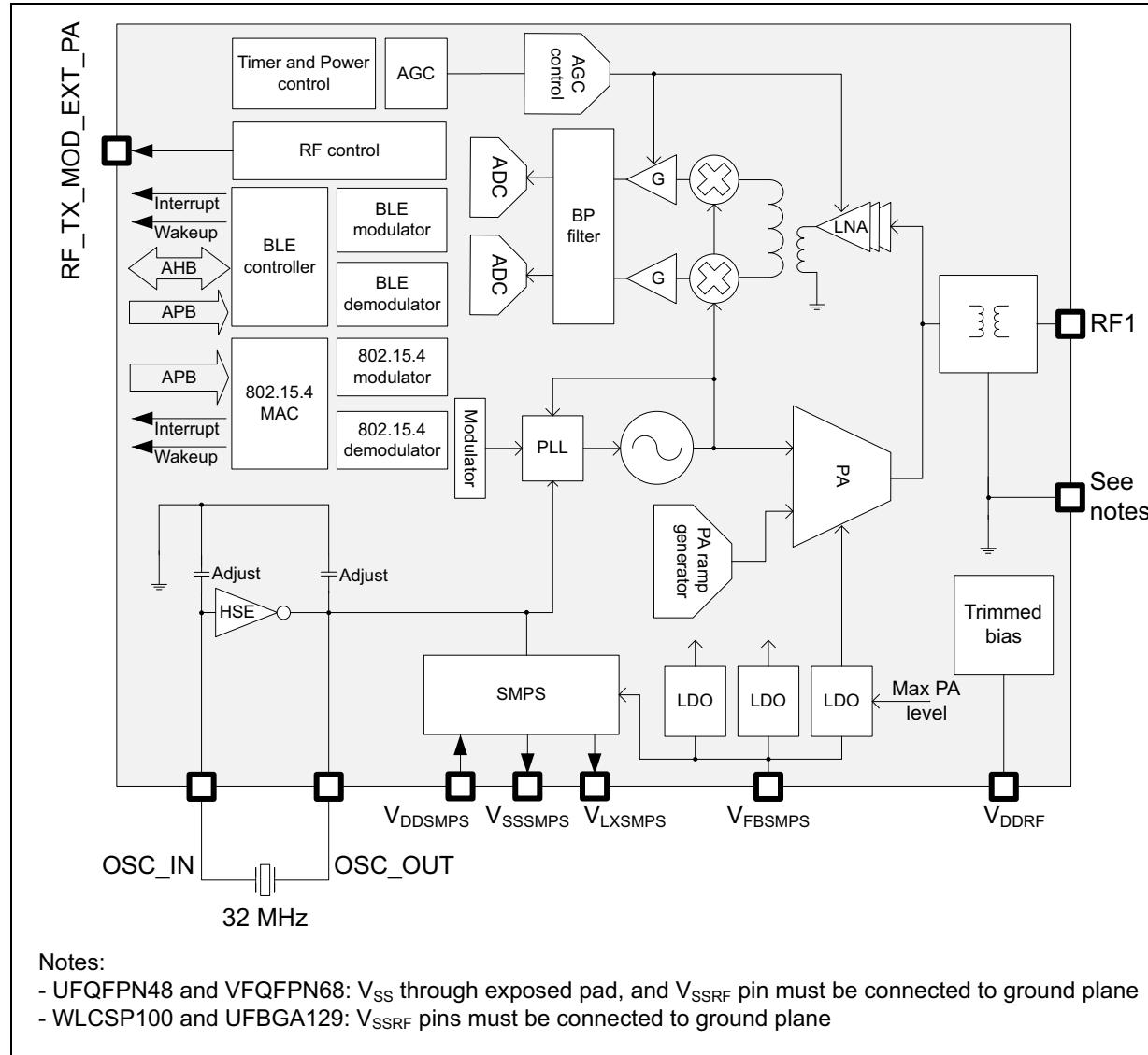
在发送模式下，最大输出功率可以通过功率放大器的可编程 LDO 电压由用户可选择。线性化、平滑的模拟控制提供清洁的功率上升。

在接收模式下，电路可以用于标准的高性能或降低的功耗 (用户可编程)。自动增益控制 (AGC) 可以在 RF 和 IF 位置上降低链路增益，以优化干扰拒绝。感谢使用复杂滤波和高精度 I/Q 架构，可以实现高灵敏度和优秀的线性。

物料清单减少是因为集成程度很高。无线电频率来源是从外部 32 MHz 晶体振荡器合成的，它不需要任何外部

trimming capacitor network thanks to a dual network of user programmable integrated capacitors.

Figure 3. STM32WB55xx and STM32WB35xx RF front-end block diagram

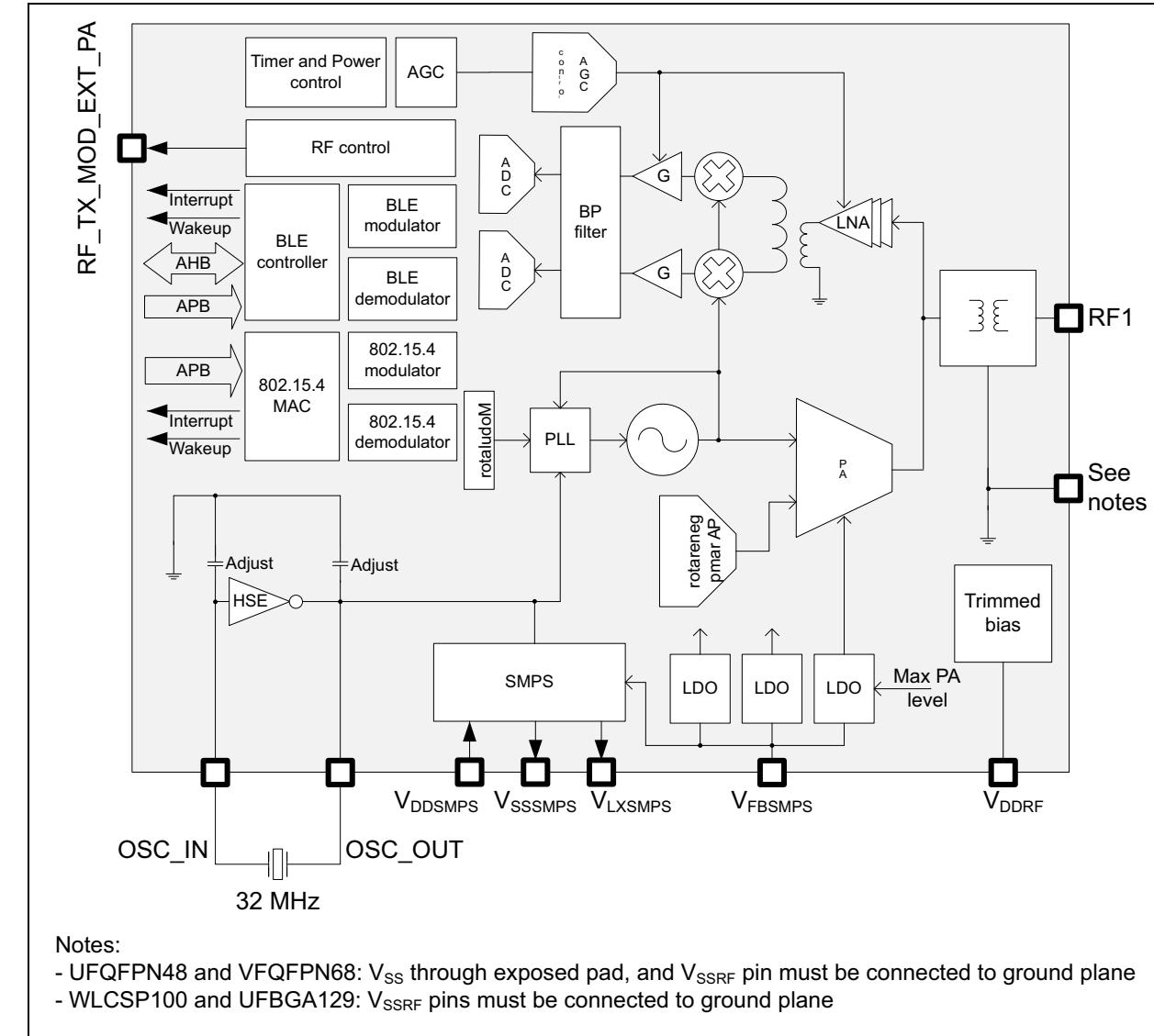


3.6.2 BLE general description

The BLE block is a master/slave processor, compliant with Bluetooth specification 5.2 standard (2 Mbps).

通过用户可编程集成电容器的双重网络，实现了调节电容网络。

Figure 3. STM32WB55xx and STM32WB35xx lock diagram



3.6.2 BLE 通用描述

BLE块是一个主从处理器，遵循蓝牙规范5.2标准 (2 Mbps)。

It integrates a 2.4 GHz RF transceiver and a powerful Cortex®-M0+ core, on which a complete power-optimized stack for Bluetooth Low Energy protocol runs, providing master / slave role support

- GAP: central, peripheral, observer or broadcaster roles
- ATT/GATT: client and server
- SM: privacy, authentication and authorization
- L2CAP
- Link layer: AES-128 encryption and decryption

In addition, according to Bluetooth specification 5.2, the BLE block provides:

- Multiple roles simultaneous support
- Master/slave and multiple roles simultaneously
- LE data packet length extension (making it possible to reach 800 kbps at application level)
- LE privacy 1.2
- LE secure connections
- Flexible Internet connectivity options
- High data rate (2 Mbps)

The device allows the applications to meet the tight peak current requirements imposed by the use of standard coin cell batteries. When the high efficiency embedded SMPS step-down converter is used, the RF front end consumption (I_{tmax}) is only 8.1 mA at the highest output power (+6 dBm).

The power efficiency of the subsystem is optimized: while running with the radio and the applicative cores simultaneously using the SMPS, the Cortex®-M4 core consumption reaches 53 μ A / MHz in active mode.

Ultra-low-power sleep modes and very short transition time between operating modes result in very low average current consumption during real operating conditions, resulting in longer battery life.

The BLE block integrates a full bandpass balun, thus reducing the need for external components.

The link between the Cortex®-M4 application processor (CPU1) running the application, and the BLE stack running on the dedicated Cortex®-M0+ (CPU2) is performed through a normalized API, using a dedicated IPCC.

它集成了一个2.44 GHz RF收发器和一个强大的 Cortex®-M0+ 核心，上面运行着完整的 Bluetooth Low Energy 协议的电源优化栈，提供主/从角色支持

- GAP: central, peripheral, observer or broadcaster roles
- ATT/GATT: client and server
- SM: privacy, authentication and authorization
- L2CAP
- Link layer: AES-128 encryption and decryption

此外，根据蓝牙规范 5.2，BLE块提供：

- 同时支持多个角色
- 主从和多个角色同时存在
- LE 数据包长度扩展 (使得能够在应用水平达到 800 kbps)
- LE 隐私 1.2
- LE 安全连接
- 灵活的互联网连接选项
- 高数据速率 (2 Mbps)

该设备允许应用程序满足由标准硬币电池使用所施加的严格峰值电流要求。当使用高效的集成 SMPS 降压转换器时，无线电前端消耗 (I_{tmax}) 仅为最高输出功率 (+6 dBm) 下的 8.1 mA。

子系统的电源效率已优化：在同时运行射频和应用核心时使用 SMPS，Cortex®-M4 核心消耗在活跃模式下达到 53 μ A / MHz。

超低功耗睡眠模式和操作模式之间的非常短过渡时间导致在真实工作条件下的非常低的平均电流消耗，从而延长电池寿命。

BLE块集成了一个完整的带通 balun，因此减少了对外部组件的需求。

Cortex®-M4应用处理器 (CPU1) 运行应用程序，以及在专用 Cortex®-M0+ (CPU2) 上运行的 BLE堆栈之间的连接通过一个标准化的 API 进行，使用一个专用的 IPCC。

3.6.3 802.15.4 general description

The STM32WB55xx and STM32WB35xx embed a dedicated 802.15.4 hardware MAC:

- Support for 802.15.4 release 2011
- Advanced MAC frame filtering; hardwired firewall: Programmable filters based on source/destination addresses, frame version, security enabled, frame type
- 256-byte RX FIFO; Up to 8 frames capacity, additional frame information (timing, mean RSSI, LQI)
- 128-byte TX FIFO with retention
 - Content not lost, retransmissions possible under CPU2 control
- Automatic frame acknowledgment, with programmable delay
- Advanced channel access features
 - Full CSMA-CA support
 - Superframe timer
 - Beacons support (require LSE)
 - Flexible TX control with programmable delay
- Configuration registers with retention available down to Standby mode for software/auto-restore
- Autonomous sniffer, Wakeup based on timer or CPU2 request
- Automatic frame transmission/reception/sleep periods, Interrupt to the CPU2 on particular events

3.6.4 RF pin description

The RF block contains dedicated pins, listed in [Table 4](#).

Table 4. RF pin list

Name	Type	Description
RF1	I/O	RF Input/output, must be connected to the antenna through a low-pass matching network
OSC_OUT		32 MHz main oscillator, also used as HSE source
OSC_IN		
RF_TX_MOD_EXT_PA		External PA transmit control
VDDRF	V _{DD}	Dedicated supply, must be connected to V _{DD}
VSSRF ⁽¹⁾	V _{SS}	To be connected to GND

1. On packages with exposed pad, this pad must be connected to GND plane for correct RF operation.

3.6.5 Typical RF application schematic

The schematic in [Figure 4](#) and the external components listed in [Table 4](#) are purely indicative. For more details refer to the “Reference design” provided in separate documents.

3.6.3 802.15.4 通用描述

The STM32WB55xx and STM32WB35xx embed a dedicated 802.15.4 硬件MAC:

- 支持802.15.4 release 2011
- 高级MAC帧过滤; 硬件防火墙: 基于源/目的地地址、帧版本、安全性启用、帧类型的可编程过滤器
- 256-字节接收FIFO; 最大8帧容量, 额外帧信息(时序, 平均RSSI, LQI)
- 128-字节发送FIFO具有保留功能— 内容不丢失, 可以在CPU2控制下重传
- 自动帧确认, 具有可编程延迟
- 高级信道访问特性— 完整的CSMA-CA支持
- 超帧计时器— 定位信号支持(需要LSE)— 灵活的发送控制具有可编程延迟
- 具有保留功能的配置寄存器, 可降低到待机模式以进行软件/自动恢复
- 独立嗅探器, 基于计时器或CPU2请求唤醒
- 自动帧发送/接收/睡眠周期, 中断到CPU2在特定事件

3.6.4 RF引脚描述

RF块包含专用引脚, 列在 [表4](#).

表4. RF引脚列表

Name	Type	Description
RF1	I/O	RF Input/output, must be connected to the antenna through a low-pass matching network
OSC_OUT		32 MHz main oscillator, also used as HSE source
OSC_IN		
RF_TX_MOD_EXT_PA		External PA transmit control
VDDRF	V _{DD}	Dedicated supply, must be connected to V _{DD}
VSSRF ⁽¹⁾	V _{SS}	To be connected to GND

1. On packages with exposed pad, this pad must be connected to GND plane for correct RF operation.

典型RF应用图形

图式图在 [图4](#)和表4中列出的外部组件表4纯粹是指示性的。有关更多详, 信息, 请参阅“参考设计”提供在单独文档中。

Figure 4. External components for the RF part

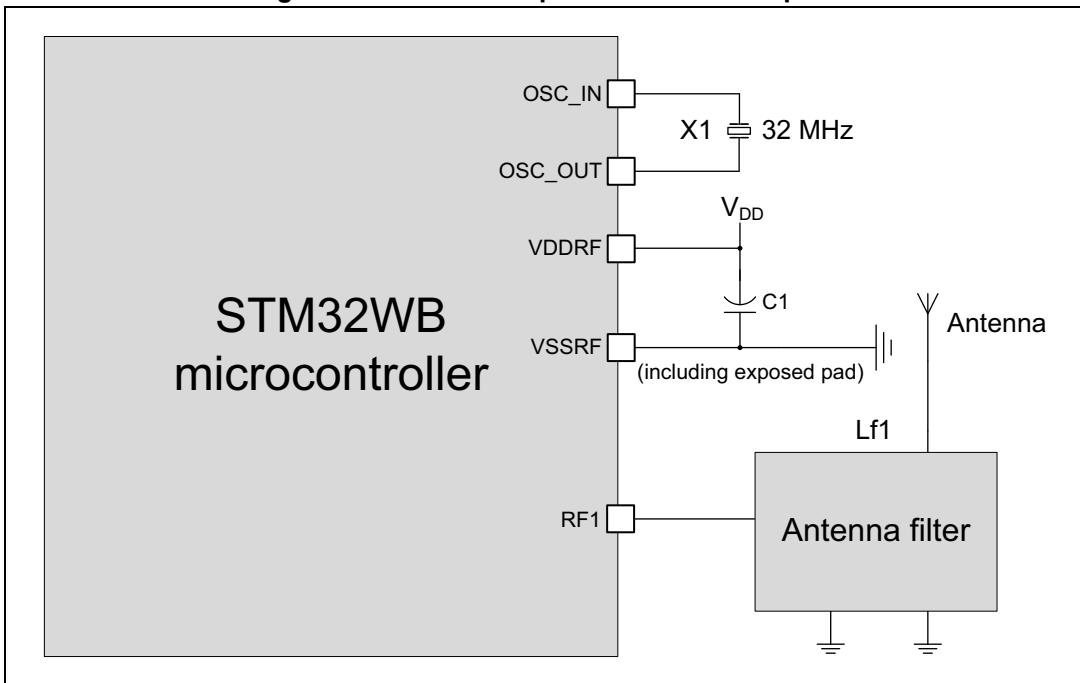


图4. 无线电部分的外部组件

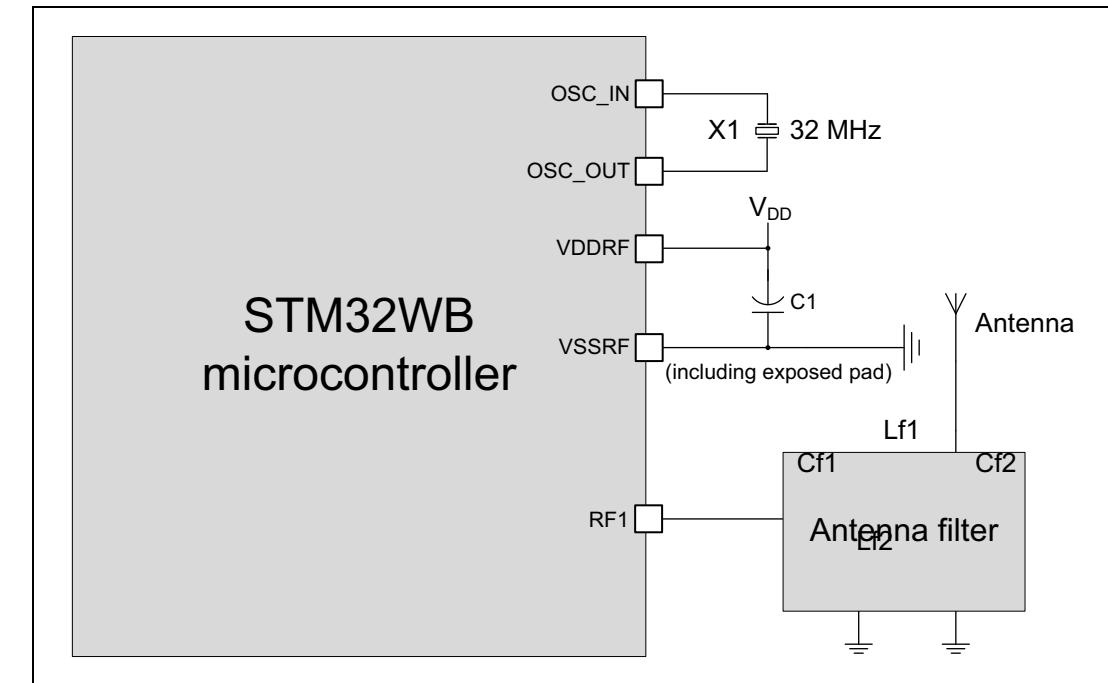


Table 5. Typical external components

Component	Description	Value
C1	Decoupling capacitance for RF	100 nF // 100 pF
X1	32 MHz crystal ⁽¹⁾	32 MHz
Antenna filter	Antenna filter and matching network	Refer to AN5165, on www.st.com
Antenna	2.4 GHz band antenna	-

1. e.g. NDK reference: NX2016SA 32 MHz EXS00A-CS06654.

Note: For more details refer to AN5165 “Development of RF hardware using STM32WB microcontrollers” available on www.st.com.

3.7 Power supply management

3.7.1 Power supply distribution

The device integrates an SMPS step-down converter to improve low power performance when the V_{DD} voltage is high enough. This converter has an intelligent mode that automatically enters bypass mode when the V_{DD} voltage falls below a specific BOR x ($x = 1, 2, 3$ or 4) voltage.

By default, at Reset the SMPS is in bypass mode.

The device can be operated without the SMPS by just wiring its output to V_{DD} . This is the case for applications where the voltage is low, or where the power consumption is not critical.

表 5. 典型外部组件

Component	Description	Value
C1	Decoupling capacitance for RF	100 nF // 100 pF
X1	32 MHz crystal ⁽¹⁾	32 MHz
Antenna filter	Antenna filter and matching network	Refer to AN5165, on www.st.com
Antenna	2.4 GHz band antenna	-

1. e.g. NDK reference: NX2016SA 32 MHz EXS00A-CS06654.

Note: For more details refer to AN5165 “使用 STM32WB 微控制器开发无线电硬件” available on www.st.com.

3.7 电源管理

3.7.1 电源分配

设备集成了SMPS下降转换器，以提高 V_{DD} 电压足够高时的低功耗性能。该转换器具有智能模式，当 V_{DD} 电压低于特定的BOR x （ $= 1, 2, 3, 4$ ）或电压时，会自动进入绕过模式。

默认情况下，复位时，SMPS在绕过模式中。

通过将其输出连接到 V_{DD} ，可以在没有SMPS的情况下运行设备。这适用于电压低或功耗不关键的应用场景。

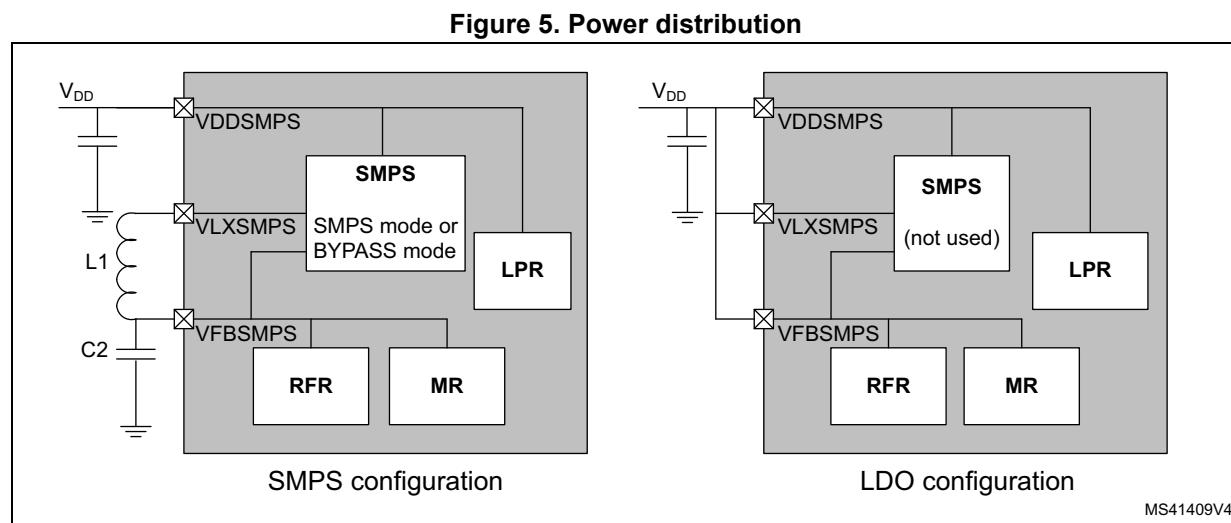


Table 6. Power supply typical components

Component	Description		Value
C2	SMPS output capacitor ⁽¹⁾		4.7 μ F
L1 ⁽²⁾	SMPS inductance	For 8 MHz ⁽³⁾	2.2 μ H
		For 4 MHz ⁽⁴⁾	10 μ H

1. e.g. GRM155R60J475KE19.

2. An extra 10 nH inductor in series with L1 is needed to improve the receiver performance, e.g. Murata LQG15WZ10NJ02D

3. e.g. Wurth 74479774222.

4. e.g. Murata LQM21FN100M70L.

The SMPS can also be switched on or set in bypass mode at any time by the application software, for example when very accurate ADC measurement are needed.

3.7.2 Power supply schemes

The devices have different voltage supplies (see [Figure 7](#) and [Figure 8](#)) and can operate within the following voltage ranges:

- $V_{DD} = 1.71$ to 3.6 V: external power supply for I/Os (V_{DDIO}), the internal regulator and system functions such as RF, SMPS, reset, power management and internal clocks. It is provided externally through VDD pins. V_{DDRF} and V_{DDSMPS} must be always connected to VDD pins.
- $V_{DDA} = 1.62$ (ADC/COMPs) to 3.6 V: external analog power supply for ADC, comparators and voltage reference buffer. The V_{DDA} voltage level can be independent from the V_{DD} voltage. When not used V_{DDA} must be connected to V_{DD} .
- $V_{DDUSB} = 3.0$ to 3.6 V: external independent power supply for USB transceivers. When not used V_{DDUSB} must be connected to V_{DD} .
- $V_{LCD} = 2.5$ to 3.6 V: the LCD controller can be powered either externally through the VLCD pin, or internally from an internal voltage generated by the embedded step-up converter. This converter can generate a V_{LCD} voltage up to 3.6 V if V_{DD} is higher than 2.0 V. Note that the LCD is available only on STM32WB55xx devices.

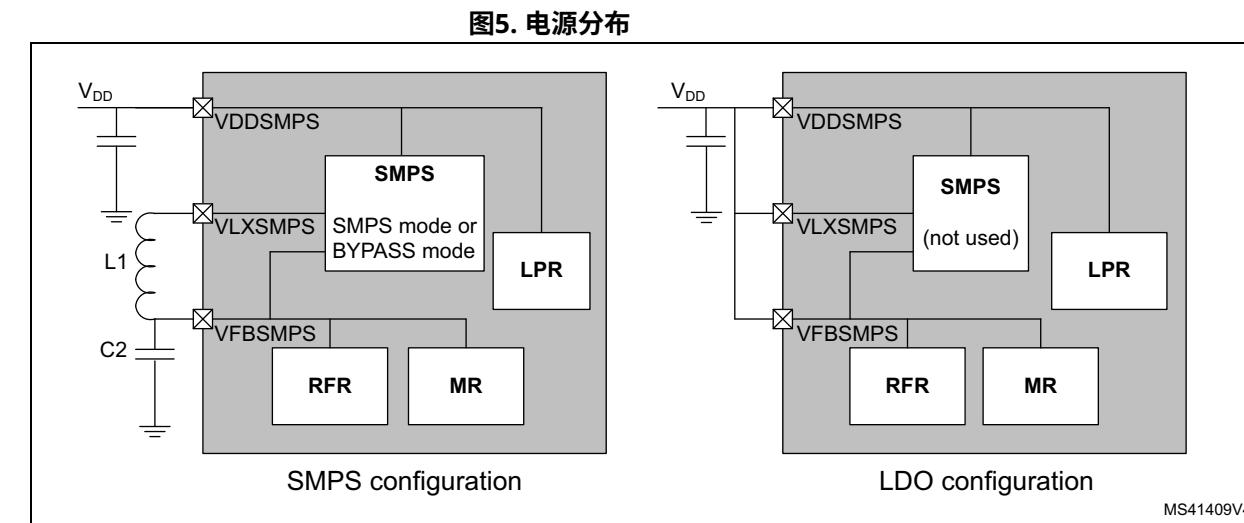


表6. 电源典型组成部分

Component	Description		Value
C2	SMPS output capacitor ⁽¹⁾		4.7 μ F
L1 ⁽²⁾	SMPS inductance	For 8 MHz ⁽³⁾	2.2 μ H
		For 4 MHz ⁽⁴⁾	10 μ H

1. e.g. GRM155R60J475KE19.

2. An extra 10 nH inductor in series with L1 is needed to improve the receiver performance, e.g. Murata LQG15WZ10NJ02D

3. e.g. Wurth 74479774222.

4. e.g. Murata LQM21FN100M70L.

SMPS 可以在任何时候由应用软件开启或设置为绕过模式，例如当需要非常准确的 ADC 测量时。

3.7.2 电源方案

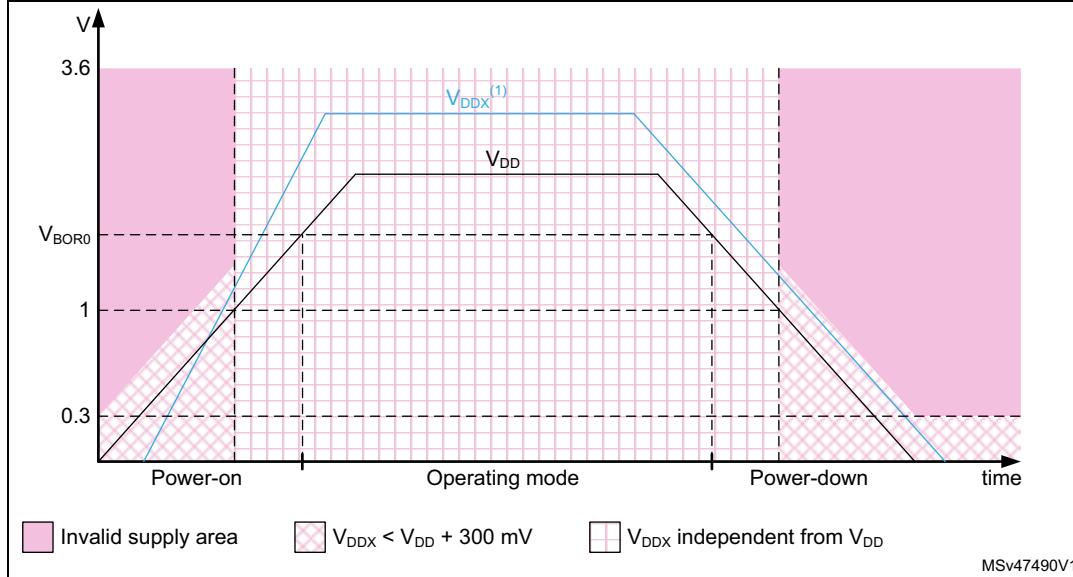
设备有不同的电压供应(看图7和图8)可以在以下电压范围内运行:

- $V_{DD} = 1.71$ to 3.6 V: external power supply for I/Os (V_{DDIO}), the internal regulator and system functions such as RF, SMPS, reset, power management and internal clocks. It is provided externally through VDD pins. V_{DDRF} and V_{DDSMPS} must be always connected to VDD pins.
- $V_{DDA} = 1.62$ (ADC/COMPs) to 3.6 V: external analog power supply for ADC, comparators and voltage reference buffer. The V_{DDA} voltage level can be independent from the V_{DD} voltage. When not used V_{DDA} must be connected to V_{DD} .
- $V_{DDUSB} = 3.0$ to 3.6 V: external independent power supply for USB transceivers. When not used V_{DDUSB} must be connected to V_{DD} .
- $V_{LCD} = 2.5$ to 3.6 V: the LCD controller can be powered either externally through the VLCD pin, or internally from an internal voltage generated by the embedded step-up converter. This converter can generate a V_{LCD} voltage up to 3.6 V if V_{DD} is higher than 2.0 V. Note that the LCD is available only on STM32WB55xx devices.

During power up/down, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V the other power supplies (V_{DDA} , V_{DDUSB} , V_{LCD}), must remain below $V_{DD} + 300$ mV
- When V_{DD} is above 1 V all power supplies are independent.

Figure 6. Power-up/down sequence



1. V_{DDX} refers to any power supply among V_{DDA} , V_{DDUSB} and V_{LCD} .

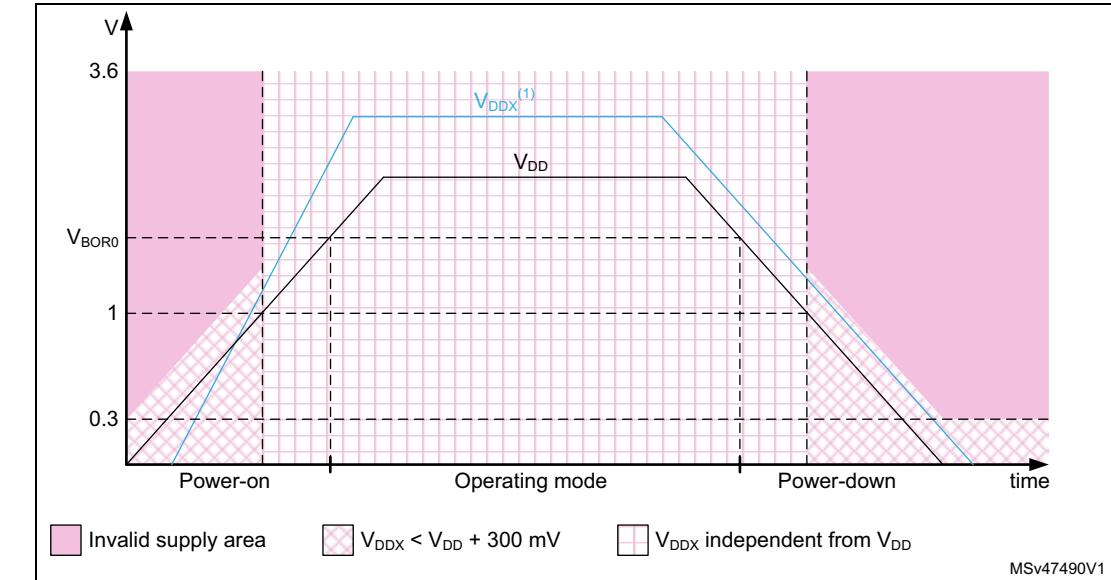
During the power down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows the external decoupling capacitors to be discharged with different time constants during the power down transient phase.

Note: V_{DD} , V_{DDRF} and V_{DDSMPS} must be wired together, so they can follow the same voltage sequence.

During power up/down, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V the other power supplies (V_{DDA} , V_{DDUSB} , V_{LCD}), must remain below $V_{DD} + 300$ mV
- When V_{DD} is above 1 V all power supplies are independent.

图6. 上电/下电序列

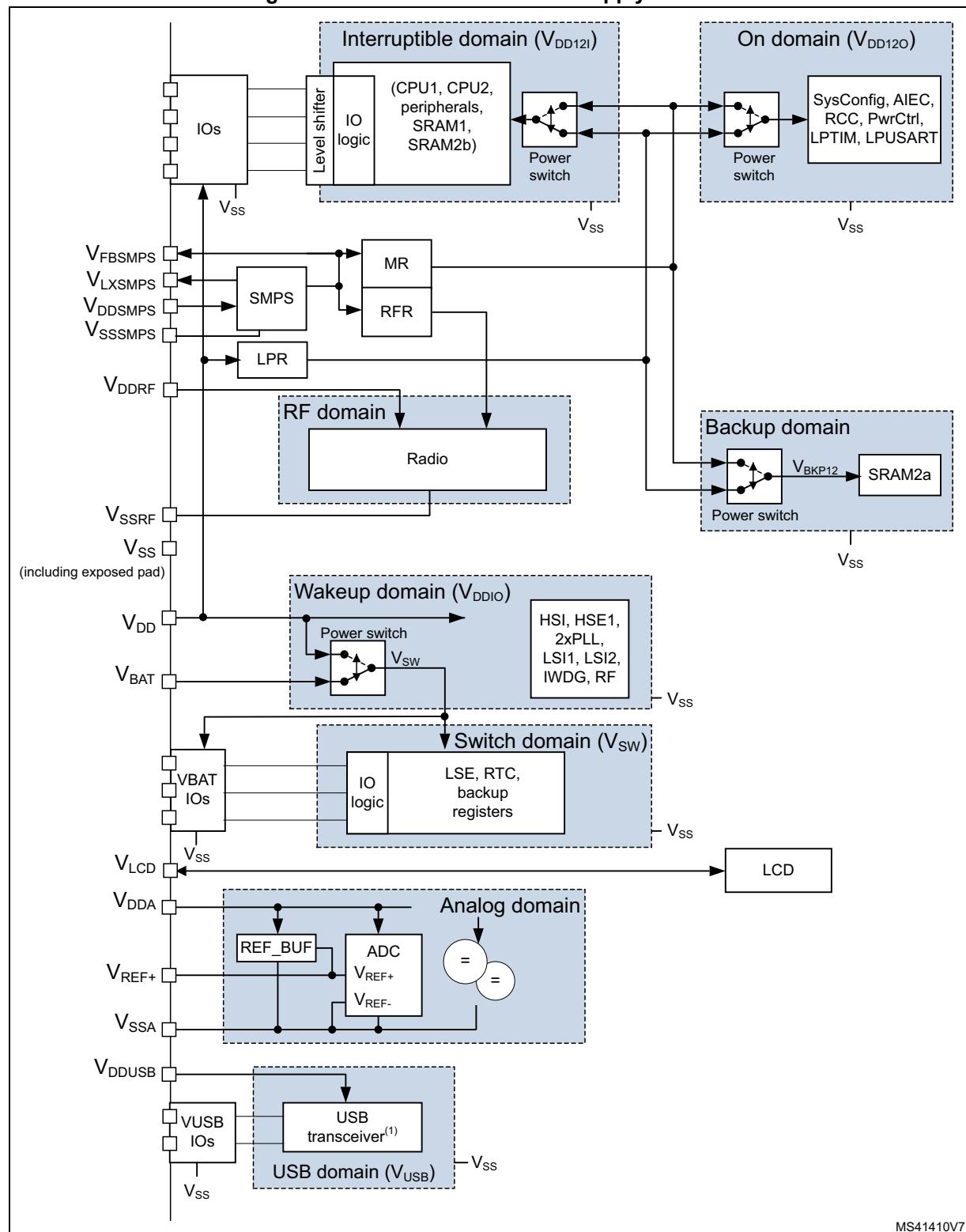


1. VDDX 指的是 VDDA, VDDUSB 和 VLCD 中的任何一个电源。

在断电阶段， V_{DD} 可能暂时低于其他电源，只要为 MCU 提供的能量低于 1 mJ。这允许外部耦合电容器以不同的时间常数在断电瞬变阶段放电。

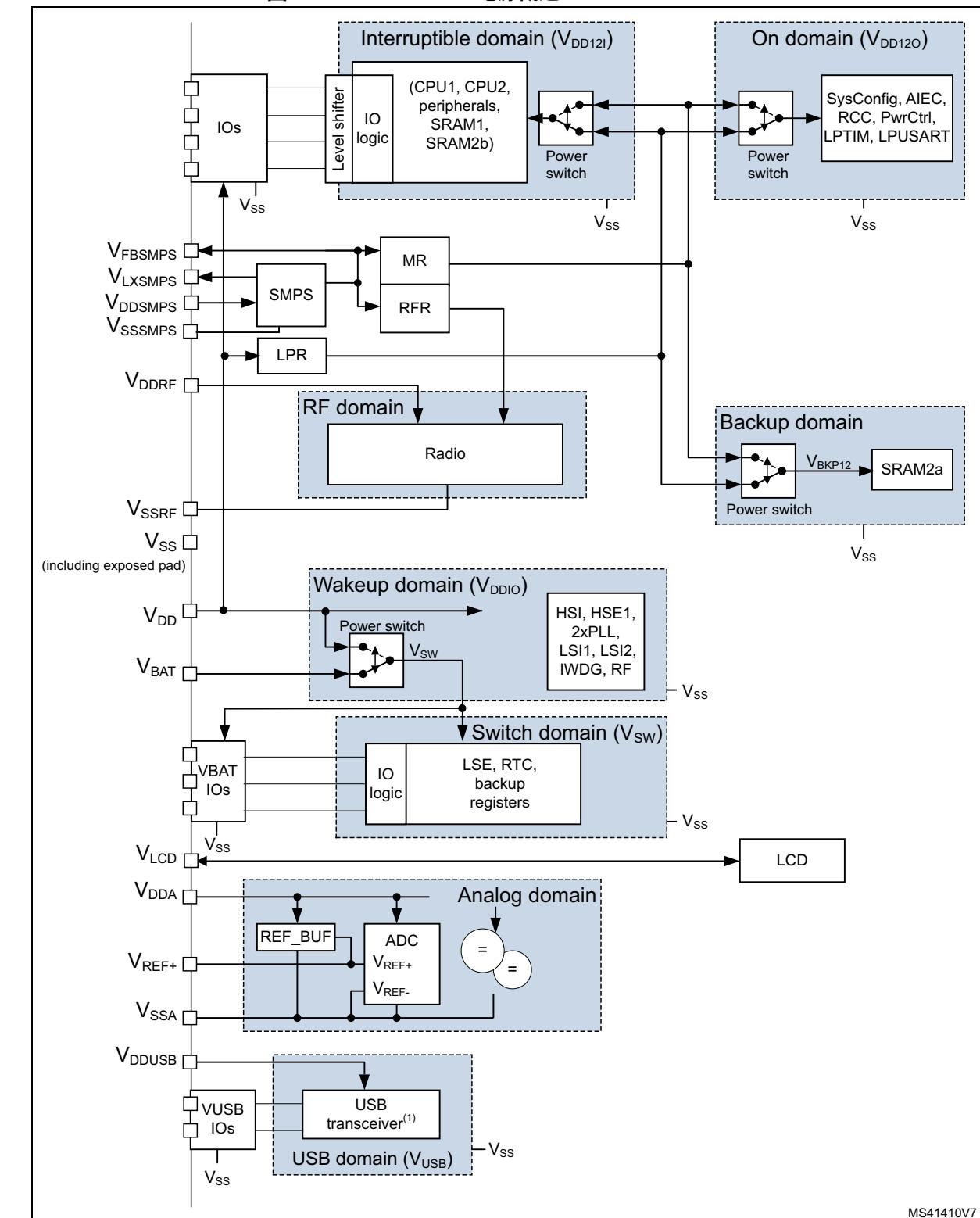
Note: V_{DD} , V_{DDRF} 和 V_{DDSMPS} 必须连接在一起，以便它们可以跟随相同的电压序列。

Figure 7. STM32WB55xx - Power supply overview



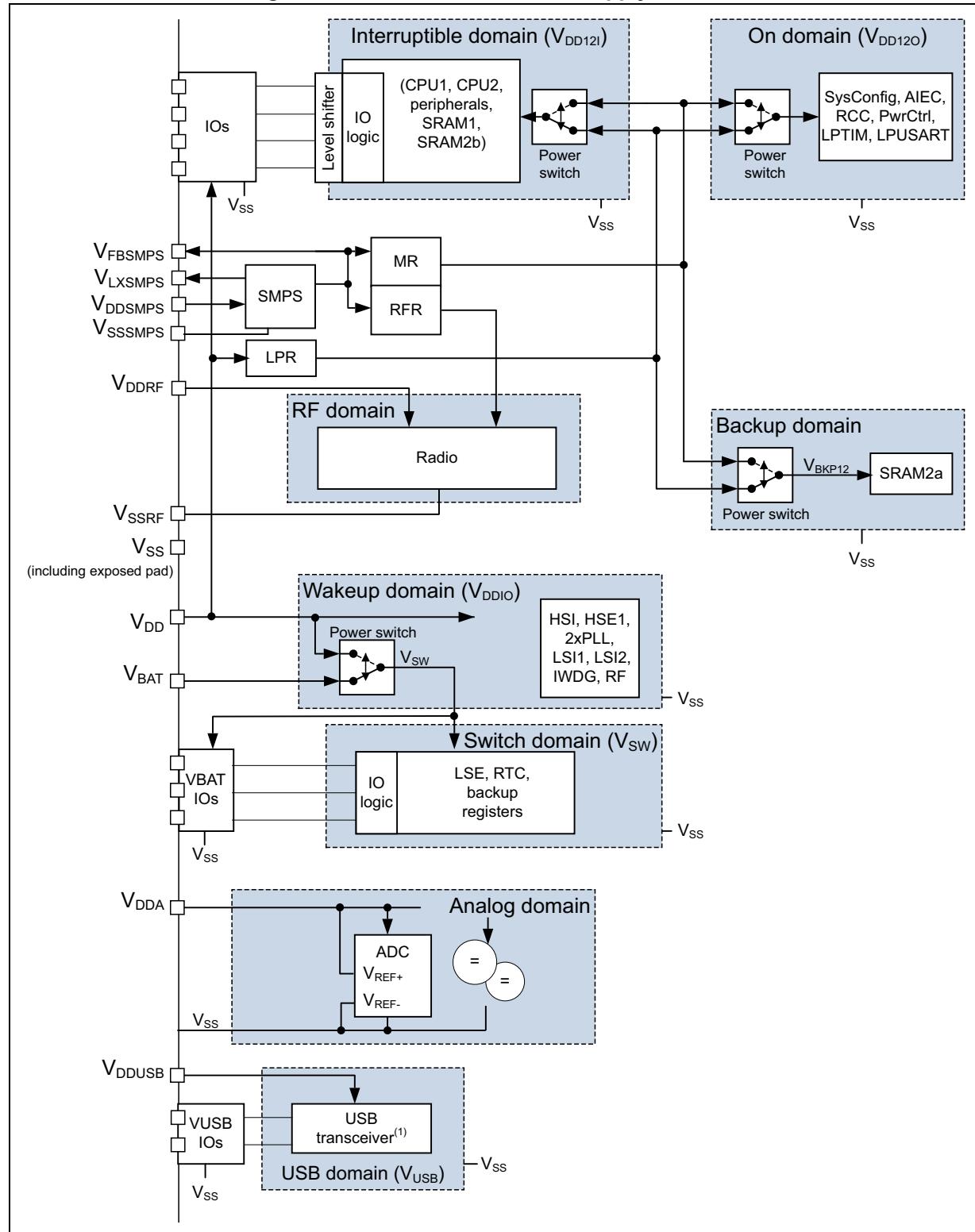
1. The USB transceiver is powered by V_{DDUSB} , and the GPIOs associated with USB are powered by V_{DPUUSB} when USB alternate function (PA11 and PA12) is selected. When USB alternate function is not selected the GPIOs associated with USB are powered as standard GPIOs.

图7. STM32WB55xx - 电源概述



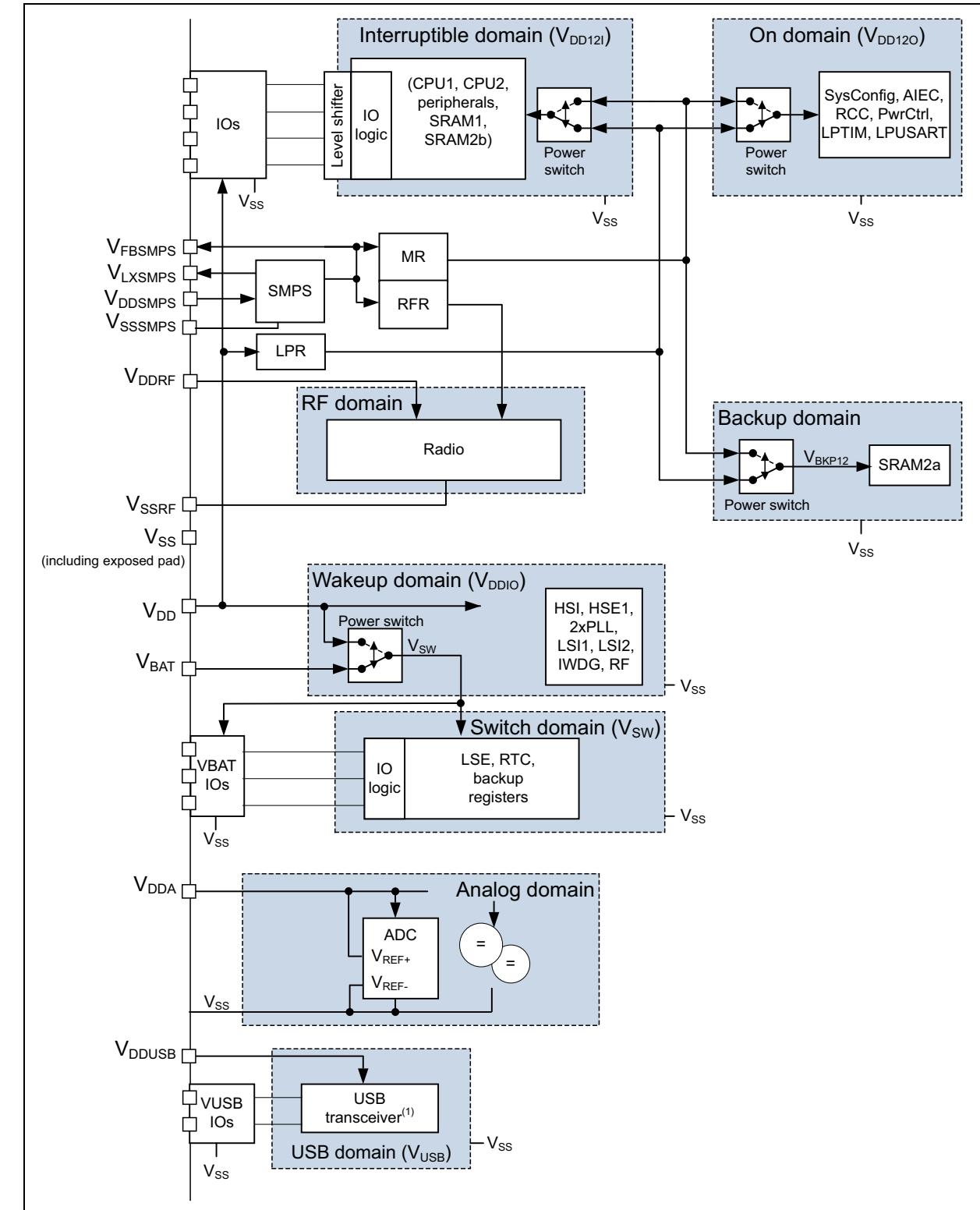
1. USB 适配器由 V_{DDUSB} 供电, 当选择 USB 替代功能 (PA11 和 PA12) 时, 与 USB 相关的 GPIOs 由 V_{DPUUSB} 供电。当未选择 USB 替代功能时, 与 USB 相关的 GPIOs 作为标准 GPIOs 供电。

Figure 8. STM32WB35xx - Power supply overview



- The USB transceiver is powered by V_{DDUSB} , and the GPIOs associated with USB are powered by V_{DDPUSB} when USB alternate function (PA11 and PA12) is selected. When USB alternate function is not selected the GPIOs associated with USB are powered as standard GPIOs.

图8. STM32WB35xx - 电源概述



- USB 适配器由 V_{DDUSB} 供电, 当选择 USB 替代功能 (PA11 和 PA12) 时, 与 USB 相关的 GPIOs 由 V_{DDUSB} 供电。当未选择 USB 替代功能时, 与 USB 相关的 GPIOs 以标准 GPIOs 的方式供电。

3.7.3 Linear voltage regulator

Three embedded linear voltage regulators supply most of the digital and RF circuitries, the main regulator (MR), the low-power regulator (LPR) and the RF regulator (RFR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-Power Run, Low-Power Sleep, Stop 1 and Stop 2 modes. It is also used to supply the SRAM2a in Standby with retention.
- The RFR is used to supply the RF analog part, its activity is automatically managed by the RF subsystem.

All the regulators are in power-down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down, inducing zero consumption.

The ultralow-power STM32WB55xx and STM32WB35xx support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the main regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.

There are two voltage and frequency ranges:

- Range 1, with the CPU running up to 64 MHz
- Range 2, with a maximum CPU frequency of 16 MHz (note that HSE can be active in this mode). All peripheral clocks are also limited to 16 MHz.

VCORE can also be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode. In this case the CPU is running at up to 2 MHz, and peripherals with independent clock can be clocked by HSI16 (in this mode the RF subsystem is not available).

3.7.4 Power supply supervisor

An integrated ultra-low-power brown-out reset (BOR) is active in all modes except Shutdown ensuring proper operation after power-on and during power down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes. The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it with the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor (PVM) that compares the independent supply voltage V_{DDA} with a fixed threshold to ensure that the peripheral is in its functional supply range.

Any BOR level can also be used to automatically switch the SMPS step-down converter in bypass mode when the V_{DD} voltage drops below a given voltage level. The mode of operation is selectable by register bit, the BOR level is selectable by option byte.

3.7.5 Low-power modes

These ultra-low-power devices support several low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources.

3.7.3 线性电压调节器

Three embedded linear voltage regulators supply most of the digital and RF circuitries, the main regulator (MR), the low-power regulator (LPR) and the RF regulator (RFR).

- 主调节器在运行模式和休眠模式以及停止0模式中使用。 • 低功耗调节器用于低功耗运行、低功耗睡眠、停止1和停止2模式。它还用于为保持状态下的保留提供SRAM2a。 • 无线电调节器用于为无线电模拟部分供电，其活动由无线电子系统自动管理。

所有调节器在待机和关闭模式下处于关闭状态：调节器输出处于高阻抗状态，内核电路断电，导致零消耗。

超低功耗STM32WB55xx和STM32WB35xx支持动态电压缩放以优化运行模式下的功耗。来自自主调节器的电压，该调节器为逻辑(VCORE)供电，可以根据系统的最大操作频率进行调整。

有两个电压和频率范围：

- 范围1，CPU运行至64 MHz • 范围2，最大CPU频率为16 MHz (请注意，在此模式下HSE可以激活。)所有外设时钟也限制为16 MHz。

VCORE 也可以由低功耗调节器供电，主调节器关闭。系统则进入低功耗运行模式。在这种情况下，CPU以最高2兆赫的速度运行，独立时钟的外围设备可以由HSI16 (在此模式下供电，无线电子系统不可用)。

3.7.4 Power supply supervisor

集成的超低功耗 brown-out reset (BOR) 在所有模式除关机之外都有效，确保上电和断电期间的正常运行。监测到的供电电压VDD低于指定阈值时，设备将保持复位模式，无需外部复位电路。

最低的BOR级别为上电时的1.71 V，其他更高的阈值可以通过选项字节进行选择。该设备具有内置的可编程电压检测器(PVD)，它监测VDD电源并将其与VPVD阈值进行比较。当VDD低于VPVD阈值且/或VDD高于VPVD阈值时，可以生成中断。中断服务例程随后可以生成警告消息且/将MCU放入安全状态。PVD通过软件启用。

此外，设备内置了一个外围电压监控器 (PVM)，它将独立供电电压 VDDA 与固定阈值进行比较，以确保外围设备处于其功能供电范围内。

任何 BOR 级别也可以用来在 VDD 电压低于给定电压水平时自动将 SMPS 下降转换器切换到绕过模式。操作模式可通过寄存器位选择，BOR 级别可通过选项字节选择。

3.7.5 低功耗模式

这些超低功耗设备支持多种低功耗模式，以实现低功耗、短启动时间、可用外围设备和可用唤醒源之间的最佳折衷。

By default, the microcontroller is in Run mode, Range 1, after a system or a power on Reset. It is up to the user to select one of the low-power modes described below:

- **Sleep**

In Sleep mode, only the CPU1 is stopped. All peripherals, including the RF subsystem, continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run**

This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator operating current. The code can be executed from SRAM or from the Flash memory, and the CPU1 frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16. The RF subsystem is not available in this mode and must be OFF.

- **Low-power sleep**

This mode is entered from the low-power run mode. Only the CPU1 clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the low-power run mode. The RF subsystem is not available in this mode and must be OFF.

- **Stop 0, Stop 1 and Stop 2**

Stop modes achieve the lowest power consumption while retaining the content of all the SRAM and registers. The LSE (or LSI) is still running.

The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

Some peripherals with wakeup capability can enable the HSI16 RC during Stop modes to detect their wakeup condition.

Three modes are available: Stop 0, Stop 1 and Stop 2. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode the main regulator remains ON, allowing a very fast wakeup time but with higher consumption.

In these modes the RF subsystem can wait for incoming events in all Stop modes.

The system clock when exiting from Stop 0, Stop1 or Stop2 modes can be either MSI up to 48 MHz or HSI16 if the RF subsystem is disabled. If the RF subsystem or the SMPS is used the exits must be set to HSI16 only. If used, the SMPS is restarted automatically.

- **Standby**

The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off.

The RTC can remain active (Standby mode with RTC).

The brown-out reset (BOR) always remains active in Standby mode.

The state of each I/O during standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

After entering Standby mode, SRAM1, SRAM2b and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2a can be retained in Standby mode, supplied by the low-power regulator (Standby with 32 KB SRAM2a retention mode).

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE, or from the RF system wakeup).

默认情况下，微控制器在系统或电源复位后处于运行模式，范围1。用户可以从以下描述的低功耗模式中选择一个：

- **睡眠**

在睡眠模式下，只停止了CPU1。所有外围设备，包括无线电子子系统，继续运行并可以在中断/事件发生时唤醒CPU。

- **低功耗运行**

此模式通过由低功耗调节器供电的VCORE实现，以最小化调节器运行电流。代码可以从SRAM或闪存内存执行，并且CPU1频率限制为2兆赫。独立时钟的外围设备可以由HSI16时钟。在此模式下，无线电子子系统不可用且必须关闭。

- **低功耗睡眠**

此模式从低功耗运行模式进入。只停止了CPU1时钟。当唤醒由事件或中断触发时，系统恢复到低功耗运行模式。在此模式下，无线电子子系统不可用且必须关闭。

- **停止模式 0、停止模式 1 和停止模式 2**

Stop modes achieve the lowest power consumption while retaining the content of all the SRAM and registers. The LSE (or LSI) is still running.

The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

一些具有唤醒能力的外围设备可以在停止模式下启用HSI16 RC，以检测它们的唤醒条件。

Three modes are available: Stop 0, Stop 1 and Stop 2. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode the main regulator remains ON, allowing a very fast wakeup time but with higher consumption.

In these modes the RF subsystem can wait for incoming events in all Stop modes.

退出Stop 0, Stop1或Stop2模式后，系统时钟可以是MSI（最大48兆赫）或HSI16（如果无线电子子系统已禁用）。如果使用无线电子子系统或SMPS，则必须设置为HSI16。如果使用，则SMPS将自动重新启动。

- **待机**

待机模式用于通过BOR达到最低功耗。内部调节器将关闭，因此VCORE域将断电。

RTC可以在RTC的待机模式下保持活跃。

brown-out-out复位(BOR)在待机模式下总是保持活跃。

每个I/O在待机模式下的状态可以由软件选择：带有内部上拉、内部下拉或浮动的I/O。

After entering待机模式，SRAM1, SRAM2b和register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2a can be retained in待机模式，supplied by the low-power regulator (Standby with 32 KB SRAM2a retention mode).

The device exits待机模式when an external reset (NRST引脚)，an IWDG复位，WKUP引脚事件（configurable rising or falling edge），or an RTC事件occurs（alarm，periodic wakeup，timestamp，tamper）or a failure is detected on LSE（CSS on LSE，or from the无线电系统唤醒）。

The system clock after wakeup is 16 MHz, derived from the HSI16. If used, the SMPS is restarted automatically.

In this mode the RF can be used.

- **Shutdown**

The Shutdown mode allows to achieve the ultimate lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off.

The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

SRAM1, SRAM2a, SRAM2b and register contents are lost except for registers in the Backup domain.

The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

The system clock after wakeup is 4 MHz, derived from the MSI.

In this mode the RF is no longer operational.

When the RF subsystem is active, it changes the power state according to its needs (Run, Stop, Standby). This operation is transparent for the CPU1 host application and managed by a dedicated HW state machine. At any given time the effective power state reached is the higher one needed by both the CPU1 and RF sub-system.

[Table 7](#) summarizes the peripheral features over all available modes. Wakeup capability is detailed in gray cells.

Table 7. Features over all modes⁽¹⁾

Peripheral ⁽²⁾	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1	Stop 2	Standby	Shutdown	VBAT
CPU1	Y	-	Y	-	-	-	-	-	-	-
CPU2	Y	-	Y	-	-	-	-	-	-	-
Radio system (BLE, 802.15.4)	Y	Y ⁽³⁾	Y	-	-	Y	Y	Y ⁽⁴⁾	Y ⁽⁴⁾	
Flash memory	Y ⁽⁵⁾	Y	O ⁽⁶⁾	O ⁽⁶⁾	R	-	R	-	R	R
SRAM1	Y	Y ⁽⁷⁾	Y	Y ⁽⁷⁾	R	-	R	-	-	-
SRAM2a	Y	Y ⁽⁷⁾	Y	Y ⁽⁷⁾	R	-	R	-	R ⁽⁸⁾	-
SRAM2b	Y	Y ⁽⁷⁾	Y	Y ⁽⁷⁾	R	-	R	-	-	-
Quad-SPI	O	O	O	O	-	-	-	-	-	-
Backup registers	Y	Y	Y	Y	R	-	R	-	R	R
Brown-out reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	-	-

唤醒后的系统时钟为 16 MHz，来自 HSI16。如果使用，则 SMPS 会自动重新启动。

在此模式下，RF 可以被使用。

- **关闭模式**

关闭模式允许实现最低的功耗。内部调节器被关闭，以便VCORE域也被关闭。

RTC可以在带有RTC的关闭模式下保持活动(关闭模式{带有RTC}v2)

BOR在关闭模式下不可用。在这种模式下无法进行电压监控，因此切换到备份域不受支持。SRAM1、SRAM2a、SRAM2b和寄存器内容丢失，除了位于

备份域。

设备在外部复位(NRST 引脚)或WKUP引脚时退出关闭模式。

事件 {可配置的上升或下降沿v2}, 或者发生 RTC 事件 (报警, 周期性唤醒唤醒, 时间戳, 篡改).

唤醒后的系统时钟为 4 MHz，来自 MSI.

在这种模式下, RF 不再工作

当 RF 子系统活跃时, 它会根据需要更改电源状态 (运行, 停止, 待机). 这个操作对 CPU1 主机应用程序是透明的, 由一个专门的硬件状态机管理. 在任何给定时间, 实际达到的电源状态是 CPU1 和 RF子子都需要的较高的状态.

[表7](#)总结了所有可用模式下的外围功能。唤醒能力详细信息在灰色单元格中。

表7. 所有模式的功能⁽¹⁾

Peripheral ⁽²⁾	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1	Stop 2	Standby	Shutdown	VBAT
CPU1	Y	-	Y	-	-	-	-	-	-	-
CPU2	Y	-	Y	-	-	-	-	-	-	-
Radio system (BLE, 802.15.4)	Y	Y ⁽³⁾	Y	-	-	Y	Y	Y ⁽⁴⁾	Y ⁽⁴⁾	
Flash memory	Y ⁽⁵⁾	Y	O ⁽⁶⁾	O ⁽⁶⁾	R	-	R	-	R	R
SRAM1	Y	Y ⁽⁷⁾	Y	Y ⁽⁷⁾	R	-	R	-	-	-
SRAM2a	Y	Y ⁽⁷⁾	Y	Y ⁽⁷⁾	R	-	R	-	R ⁽⁸⁾	-
SRAM2b	Y	Y ⁽⁷⁾	Y	Y ⁽⁷⁾	R	-	R	-	-	-
Quad-SPI	O	O	O	O	-	-	-	-	-	-
Backup registers	Y	Y	Y	Y	R	-	R	-	R	R
Brown-out reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	-

Table 7. Features over all modes⁽¹⁾ (continued)

Peripheral ⁽²⁾	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1	Stop 2	Standby	Shutdown	VBAT
Programmable voltage detector (PVD)	O	O	O	O	O	O	O	-	-	-
Peripheral voltage monitor PVMx (x=1, 3)	O	O	O	O	O	O	O	-	-	-
SMPS	O	O	O	O	O ⁽⁹⁾	-	-	-	-	-
DMAx (x = 1, 2)	O	O	O	O	-	-	-	-	-	-
High speed internal (HSI16)	O	O	O	O	O ⁽¹⁰⁾	-	-	-	-	-
Oscillator HSI48	O	O	-	-	-	-	-	-	-	-
High speed external (HSE) ⁽¹¹⁾	O	O	O	O	-	-	-	-	-	-
Low speed internal (LSI1 or LSI2)	O	O	O	O	O	-	O	-	-	-
Low speed external (LSE)	O	O	O	O	O	-	O	-	O	O
Multi-speed internal (MSI) ⁽¹²⁾	48	24	O	48	O	-	-	-	-	-
PLLx VCO maximum frequency	344	128	O	-	-	-	-	-	-	-
Clock security system (CSS)	O	O	O	O	O	O ⁽¹³⁾	O	O ⁽¹³⁾	-	-
Clock security system on LSE	O	O	O	O	O	O	O	O	-	-
RTC / Auto wakeup	O	O	O	O	O	O	O	O	O	O
Number of RTC tamper pins	3	3	3	3	3	O	3	O	3	O
LCD	O	O	O	O	O	O	O	-	-	-
USB FS	O	-	O	-	-	O	-	-	-	-
USART1	O	O	O	O	O ⁽¹⁴⁾	O ⁽¹⁴⁾	-	-	-	-
Low-power UART (LPUART1)	O	O	O	O	O ⁽¹⁴⁾	O ⁽¹⁴⁾	O ⁽¹⁴⁾	O ⁽¹⁴⁾	-	-
I2C1	O	O	O	O	O ⁽¹⁵⁾	O ⁽¹⁵⁾	-	-	-	-
I2C3	O	O	O	O	O ⁽¹⁵⁾	O ⁽¹⁵⁾	O ⁽¹⁵⁾	O ⁽¹⁵⁾	-	-
SPIx (x=1, 2)	O	O	O	O	-	-	-	-	-	-
SAI1	O	O	O	O	-	-	-	-	-	-

表7. 所有模式的功能⁽¹⁾ (继续)

Peripheral ⁽²⁾	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1	Stop 2	Standby	Shutdown	VBAT
Programmable voltage detector (PVD)	O	O	O	O	O	O	O	-	-	-
Peripheral voltage monitor PVMx (x=1, 3)	O	O	O	O	O	O	O	-	-	-
SMPS	O	O	O	O	O ⁽⁹⁾	-	-	-	-	-
DMAx (x = 1, 2)	O	O	O	O	-	-	-	-	-	-
High speed internal (HSI16)	O	O	O	O	O ⁽¹⁰⁾	-	-	-	-	-
Oscillator HSI48	O	O	-	-	-	-	-	-	-	-
High speed external (HSE) ⁽¹¹⁾	O	O	O	O	-	-	-	-	-	-
Low speed internal (LSI1 or LSI2)	O	O	O	O	O	O	-	O	-	-
Low speed external (LSE)	O	O	O	O	O	O	-	O	-	O
Multi-speed internal (MSI) ⁽¹²⁾	48	24	O	48	O	-	-	-	-	-
PLLx VCO maximum frequency	344	128	O	-	-	-	-	-	-	-
Clock security system (CSS)	O	O	O	O	O	O ⁽¹³⁾	O	O ⁽¹³⁾	-	-
Clock security system on LSE	O	O	O	O	O	O	O	O	-	-
RTC / Auto wakeup	O	O	O	O	O	O	O	O	O	O
Number of RTC tamper pins	3	3	3	3	3	O	3	O	3	O
LCD	O	O	O	O	O	O	O	O	-	-
USB FS	O	-	O	-	-	O	-	-	-	-
USART1	O	O	O	O	O ⁽¹⁴⁾	O ⁽¹⁴⁾	-	-	-	-
Low-power UART (LPUART1)	O	O	O	O	O ⁽¹⁴⁾	O ⁽¹⁴⁾	O ⁽¹⁴⁾	O ⁽¹⁴⁾	-	-
I2C1	O	O	O	O	O ⁽¹⁵⁾	O ⁽¹⁵⁾	-	-	-	-
I2C3	O	O	O	O	O ⁽¹⁵⁾	O ⁽¹⁵⁾	O ⁽¹⁵⁾	O ⁽¹⁵⁾	-	-
SPIx (x=1, 2)	O	O	O	O	-	-	-	-	-	-
SAI1	O	O	O	O	-	-	-	-	-	-

Table 7. Features over all modes⁽¹⁾ (continued)

Peripheral ⁽²⁾	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1	Stop 2	Standby	Shutdown	VBAT
ADC1	O	O	O	O	-	-	-	-	-	-
VREFBUF	O	O	O	O	O	-	-	-	-	-
COMPx (x=1, 2)	O	O	O	O	O	O	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-
Timers TIMx (x=1, 2, 16, 17)	O	O	O	O	-	-	-	-	-	-
Low-power Timer 1 (LPTIM1)	O	O	O	O	O	O	-	-	-	-
Low-power Timer 2 (LPTIM2)	O	O	O	O	O	O	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-
True random number generator (RNG)	O	-	O	-	-	-	-	-	-	-
AES2 hardware accelerator	O	O	O	O	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-
IPCC	O	-	O	-	-	-	-	-	-	-
HSEM	O	-	O	-	-	-	-	-	-	-
PKA	O	O	O	O	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	(16) 5 pins	(17) 5 pins	-	-

1. Legend: Y = Yes (Enabled), O = Optional (Disabled by default, can be enabled by software), R = Data retained, - = Not available.
2. Available peripherals depend upon package, STM32WB35xx features one SPI, no LCD, no TSC and two wakeup pins. See [Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts](#) for more details.
3. Bluetooth® Low Energy not possible in this mode.
4. Standby with SRAM2a retention mode only.
5. Flash memory programming only possible in Range 1 voltage, not in Range 2 and not in Low Power mode.
6. The Flash memory can be configured in Power-down mode. By default, it is not in Power-down mode.
7. The SRAM clock can be gated on or off.

表7. 所有模式的功能⁽¹⁾ (继续)

Peripheral ⁽²⁾	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1	Stop 2	Standby	Shutdown	VBAT
ADC1	O	O	O	O	-	-	-	-	-	-
VREFBUF	O	O	O	O	O	O	-	-	-	-
COMPx (x=1, 2)	O	O	O	O	O	O	O	O	O	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-
Timers TIMx (x=1, 2, 16, 17)	O	O	O	O	-	-	-	-	-	-
Low-power Timer 1 (LPTIM1)	O	O	O	O	O	O	O	O	O	-
Low-power Timer 2 (LPTIM2)	O	O	O	O	O	O	O	O	O	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-
True random number generator (RNG)	O	-	O	-	-	-	-	-	-	-
AES2 hardware accelerator	O	O	O	O	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-
IPCC	O	-	O	-	-	-	-	-	-	-
HSEM	O	-	O	-	-	-	-	-	-	-
PKA	O	O	O	O	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(16) 5 pins	(17) 5 pins

1. Legend: Y = Yes (Enabled), O = Optional (Disabled by default, can be enabled by software), R = Data retained, - = Not available.
2. Available peripherals depend upon package, STM32WB35xx features one SPI, no LCD, no TSC and two wakeup pins. See [Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts](#) for more details.
3. Bluetooth® Low Energy not possible in this mode.
4. Standby with SRAM2a retention mode only.
5. Flash memory programming only possible in Range 1 voltage, not in Range 2 and not in Low Power mode.
6. The Flash memory can be configured in Power-down mode. By default, it is not in Power-down mode.
7. The SRAM clock can be gated on or off.

Functional overview**STM32WB55xx STM32WB35xx**

8. SRAM2a content is preserved when the bit RRS is set in PWR_CR3 register.
9. Stop 0 only. SMPS is automatically switched to Bypass or Open mode during Low power operation.
10. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
11. The HSE can be used by the RF subsystem according with the need to perform RF operation (Tx or Rx).
12. MSI maximum frequency.
13. In case RF will be used and HSE will fail.
14. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
15. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
16. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
17. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

功能概述**STM32WB55xx STM32WB35xx**

8. SRAM2a content is preserved when the bit RRS is set in PWR_CR3 register.
9. Stop 0 only. SMPS is automatically switched to Bypass or Open mode during Low power operation.
10. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
11. The HSE can be used by the RF subsystem according with the need to perform RF operation (Tx or Rx).
12. MSI maximum frequency.
13. In case RF will be used and HSE will fail.
14. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
15. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
16. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
17. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

Table 8. STM32WB55xx and STM32WB35xx modes overview

Mode	Regulator	CPU1	Flash	SRAM	Clocks	DMA and peripherals ⁽¹⁾	Wakeup source	Consumption ⁽²⁾	Wakeup time
Run	Range 1	Yes	ON ⁽³⁾⁽⁴⁾	ON	Any	All	N/A	107 µA/MHz	N/A
	Range 2					All except RNG and USB-FS		100 µA/MHz	
LPRun	LPR	Yes	ON ⁽³⁾	ON	Any except PLL	All except RF, RNG and USB-FS	N/A	103 µA/MHz	15.33 µs
Sleep	Range 1	No	ON ⁽³⁾	ON ⁽⁵⁾	Any	All	Any interrupt or event	41 µA/MHz	9 cycles
	Range 2					All except RNG and USB-FS		46 µA/MHz	
LPSleep	LPR	No	ON ⁽³⁾	ON ⁽⁵⁾	Any except PLL	All except RF, RNG and USB-FS	Any interrupt or event	45 µA/MHz	9 cycles
Stop 0	Range 1	No	OFF	ON	LSE, LSI, HSE ⁽⁶⁾ , HSI16 ⁽⁷⁾	RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 ⁽⁸⁾ LPUART1 ⁽⁸⁾ I2Cx (x=1, 3) ⁽⁹⁾ LPTIMx (x=1, 2), SMPS All other peripherals are frozen.	Reset pin, all I/Os, RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 LPUART1 I2Cx (x=1, 3) LPTIMx (x=1, 2) USB	100 µA	1.7 µs
	Range 2								
Stop 1	LPR	No	OFF	ON	LSE, LSI, HSE ⁽⁶⁾ , HSI16 ⁽⁷⁾	RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 ⁽⁸⁾ LPUART1 ⁽⁸⁾ I2Cx (x=1, 3) ⁽⁹⁾ LPTIMx (x=1, 2) All other peripherals are frozen.	Reset pin, all I/Os RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 LPUART1 I2Cx (x=1, 3) LPTIMx (x=1, 2) USB	9.2 µA w/o RTC 9.6 µA w RTC	4.7 µs

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Functional overview

Table 8. STM32WB55xx and STM32WB35xx modes overview

Mode	Regulator	CPU1	Flash	SRAM	Clocks	DMA and peripherals ⁽¹⁾	Wakeup source	Consumption ⁽²⁾	Wakeup time
Run	Range 1	Yes	ON ⁽³⁾⁽⁴⁾	ON	Any	All	N/A	107 µA/MHz	N/A
	Range 2					All except RNG and USB-FS		100 µA/MHz	
LPRun	LPR	Yes	ON ⁽³⁾	ON	Any except PLL	All except RF, RNG and USB-FS	N/A	103 µA/MHz	15.33 µs
Sleep	Range 1	No	ON ⁽³⁾	ON ⁽⁵⁾	Any	All	Any interrupt or event	41 µA/MHz	9 cycles
	Range 2					All except RNG and USB-FS		46 µA/MHz	
LPSleep	LPR	No	ON ⁽³⁾	ON ⁽⁵⁾	Any except PLL	All except RF, RNG and USB-FS	Any interrupt or event	45 µA/MHz	9 cycles
Stop 0	Range 1	No	OFF	ON	LSE, LSI, HSE ⁽⁶⁾ , HSI16 ⁽⁷⁾	RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 ⁽⁸⁾ LPUART1 ⁽⁸⁾ I2Cx (x=1, 3) ⁽⁹⁾ LPTIMx (x=1, 2), SMPS All other peripherals are frozen.	Reset pin, all I/Os, RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 LPUART1 I2Cx (x=1, 3) LPTIMx (x=1, 2) USB	100 µA	1.7 µs
	Range 2								
Stop 1	LPR	No	OFF	ON	LSE, LSI, HSE ⁽⁶⁾ , HSI16 ⁽⁷⁾	RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 ⁽⁸⁾ LPUART1 ⁽⁸⁾ I2Cx (x=1, 3) ⁽⁹⁾ LPTIMx (x=1, 2) All other peripherals are frozen.	Reset pin, all I/Os RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 LPUART1 I2Cx (x=1, 3) LPTIMx (x=1, 2) USB	9.2 µA w/o RTC 9.6 µA w RTC	4.7 µs

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Table 8. STM32WB55xx and STM32WB35xx modes overview (continued)

Mode	Regulator	CPU1	Flash	SRAM	Clocks	DMA and peripherals ⁽¹⁾	Wakeup source	Consumption ⁽²⁾	Wakeup time
Stop 2	LPR	No	OFF	ON	LSE, LSI	RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) LPUART1 ⁽⁸⁾ I2C3 ⁽⁹⁾ LPTIM1 All other peripherals are frozen.	Reset pin, all I/Os RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) LPUART1 I2C3 LPTIM1	1.85 µA w/o RTC 2.1 µA w RTC	5.71 µs
Standby	LPR	No	OFF	SRAM2a ON ⁽¹⁰⁾	LSE, LSI	RF, BOR, RTC, IWDG All other peripherals are powered off. I/O configuration can be floating, pull-up or pull-down	RF, Reset pin 5 I/Os (WKUPx) ⁽¹¹⁾ BOR, RTC, IWDG	0.32 µA w/o RTC 0.60 µA w RTC 0.11 µA w/o RTC 0.390 µA w RTC	51 µs
	OFF			OFF					
Shutdown	OFF	No	OFF	OFF	LSE	RTC All other peripherals are powered off. I/O configuration can be floating, pull-up or pull-down ⁽¹²⁾	5 I/Os (WKUPx) ⁽¹¹⁾ , RTC	0.028 µA w/o RTC 0.315 µA w/ RTC	-

- Available peripherals depend upon package, STM32WB35xx features one SPI, no LCD, no TSC and two wakeup pins. See [Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts](#) for more details.
- Typical current at $V_{DD} = 1.8$ V, 25 °C. for STOPx, SHUTDOWN and Standby, else $V_{DD} = 3.3$ V, 25 °C.
- The Flash memory controller can be placed in power-down mode if the RF subsystem is not in use and all the program is run from the SRAM.
- Flash memory programming is only possible in Range 2 voltage.
- The SRAM1 and SRAM2 clocks can be gated off independently.
- HSE (32 MHz) automatically used when RF activity is needed by the RF subsystem.
- HSI16 (16 MHz) automatically used by some peripherals.
- U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, Address match or Received frame event.
- I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
- SRAM1 and SRAM2b are OFF.
- I/Os with wakeup from Standby/Shutdown capability: PA0, PC13, PC12, PA2, PC5.
- I/Os can be configured with internal pull-up, pull-down or floating but the configuration is lost immediately when exiting the Shutdown mode.



Functional overview

Table 8. STM32WB55xx and STM32WB35xx modes overview (continued)

Mode	Regulator	CPU1	Flash	SRAM	Clocks	DMA and peripherals ⁽¹⁾	Wakeup source	Consumption ⁽²⁾	Wakeup time
Stop 2	LPR	No	OFF	ON	LSE, LSI	RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) LPUART1 ⁽⁸⁾ I2C3 ⁽⁹⁾ LPTIM1 All other peripherals are frozen.	Reset pin, all I/Os RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) LPUART1 I2C3 LPTIM1	1.85 µA w/o RTC 2.1 µA w RTC	5.71 µs
Standby	LPR	No	OFF	SRAM2a ON ⁽¹⁰⁾	LSE, LSI	RF, BOR, RTC, IWDG All other peripherals are powered off. I/O configuration can be floating, pull-up or pull-down	RF, Reset pin 5 I/Os (WKUPx) ⁽¹¹⁾ BOR, RTC, IWDG	0.32 µA w/o RTC 0.60 µA w RTC	51 µs
	OFF			OFF				0.11 µA w/o RTC 0.390 µA w RTC	
Shutdown	OFF	No	OFF	OFF	LSE	RTC All other peripherals are powered off. I/O configuration can be floating, pull-up or pull-down ⁽¹²⁾	5 I/Os (WKUPx) ⁽¹¹⁾ , RTC	0.028 µA w/o RTC 0.315 µA w/ RTC	-

- Available peripherals depend upon package, STM32WB35xx features one SPI, no LCD, no TSC and two wakeup pins. See [Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts](#) for more details.
- Typical current at $V_{DD} = 1.8$ V, 25 °C. for STOPx, SHUTDOWN and Standby, else $V_{DD} = 3.3$ V, 25 °C.
- The Flash memory controller can be placed in power-down mode if the RF subsystem is not in use and all the program is run from the SRAM.
- Flash memory programming is only possible in Range 2 voltage.
- The SRAM1 and SRAM2 clocks can be gated off independently.
- HSE (32 MHz) automatically used when RF activity is needed by the RF subsystem.
- HSI16 (16 MHz) automatically used by some peripherals.
- U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, Address match or Received frame event.
- I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
- SRAM1 and SRAM2b are OFF.
- I/Os with wakeup from Standby/Shutdown capability: PA0, PC13, PC12, PA2, PC5.
- I/Os can be configured with internal pull-up, pull-down or floating but the configuration is lost immediately when exiting the Shutdown mode.



3.7.6 Reset mode

To improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O Schmitt trigger is disabled). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.8 VBAT operation

The VBAT pin allows to power the device VBAT domain (RTC, LSE and Backup registers) from an external battery, an external supercapacitor, or from V_{DD} when no external battery nor an external supercapacitor are present. Three anti-tamper detection pins are available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied only from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

3.9 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU1 resources and, consequently, reducing power supply consumption. In addition, these hardware connections result in fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run and Sleep, Stop 0, Stop 1 and Stop 2 modes.

Table 9. STM32WB55xx and STM32WB35xx CPU1 peripherals interconnect matrix

Source	Destination	Action	Run	Sleep	Low-power run	Low-power	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADC1	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-
COMPx	TIM1 TIM2	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	⁽¹⁾
ADC1	TIM1	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-

3.7.6 复位模式

为了改善复位时的消耗，复位前后的 I/Os 状态是“模拟状态”(I/O 施密特触发器被禁用)。此外，当复位源是内部时，内部复位上拉被关闭。

3.8 VBAT操作

VBAT引脚允许从外部电池、外部超级电容或在没有外部电池或外部超级电容时从VDD供电设备VBAT领域(RTC, LSE和备份寄存器)。在VBAT模式下，可用三个防篡改检测引脚。

VBAT操作在VDD不存在时会自动激活。

内置了一个内部VBAT电池充电电路，可以在VDD存在时激活。

注意：当微控制器仅从VBAT供电时，外部中断和RTC警报/事件不会退出VBAT操作。

3.9 互连矩阵

多个外围设备之间有直接的硬件连接。这允许外围设备之间进行自主通信，节省 CPU1 资源，并且从而降低电源消耗。此外，这些硬件连接会导致速度快且可预测的延迟。

根据外围设备，这些互连可以在 Run、Sleep、Low-power run 和 Sleep、Stop 0、Stop 1 和 Stop 2 模式下运行。

表9. STM32WB55xx 和 STM32WB35xx CPU1 外设互连矩阵

Source	Destination	Action	Run	Sleep	Low-power run	Low-power	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADC1	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-
COMPx	TIM1 TIM2	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	⁽¹⁾
ADC1	TIM1	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-

Table 9. STM32WB55xx and STM32WB35xx CPU1 peripherals interconnect matrix (continued)

Source	Destination	Action	Run	Sleep	Low-power run	Low-power	Stop 0 / Stop 1	Stop 2
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y ⁽¹⁾
All clock sources (internal and external)	TIM2 TIM16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-	-
CSS CPU (hard fault) SRAM (parity error) Flash memory (ECC error) COMPx PVD	TIM1 TIM16,17	Timer break	Y	Y	Y	Y	-	-
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y ⁽¹⁾
	ADC1	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 only.

表9. STM32WB55xx 和 STM32WB35xx CPU1 外设互连矩阵 (继续)

Source	Destination	Action	Run	Sleep	Low-power run	Low-power	Stop 0 / Stop 1	Stop 2
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y ⁽¹⁾
All clock sources (internal and external)	TIM2 TIM16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-	-
CSS CPU (hard fault) SRAM (parity error) Flash memory (ECC error) COMPx PVD	TIM1 TIM16,17	Timer break	Y	Y	Y	Y	-	-
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y ⁽¹⁾
	ADC1	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 only.

3.10 Clocks and startup

The STM32WB55xx and STM32WB35xx devices integrate several clock sources:

- LSE: 32.768 kHz external oscillator, for accurate RTC and calibration with other embedded RC oscillators
- LSI1: 32 kHz on-chip low-consumption RC oscillator
- LSI2: almost 32 kHz, on-chip high-stability RC oscillator, used by the RF subsystem
- HSE: high quality 32 MHz external oscillator with trimming, needed by the RF subsystem
- HSI16: 16 MHz high accuracy on-chip RC oscillator
- MSI: 100 kHz to 48 MHz multiple speed on-chip low power oscillator, can be trimmed using the LSE signal
- HSI48: 48 MHz on-chip RC oscillator, for USB crystal-less purpose

The clock controller (see [Figure 9](#)) distributes the clocks coming from the different oscillators to the core and the peripherals including the RF subsystem. It also manages clock gating for low power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
 - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
 - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than $\pm 0.25\%$ accuracy. The MSI can supply a PLL.
 - System PLL that can be fed by HSE, HSI16 or MSI, with a maximum frequency of 64 MHz.
- **Auxiliary clock source:** two ultralow-power clock sources that can be used to drive the LCD controller and the real-time clock:
 - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
 - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is $\pm 5\%$. The LSI source can be either the LSI1 or the LSI2 on-chip oscillator.
- **Peripheral clock sources:** Several peripherals (RNG, SAI, USARTs, I2Cs, LPTimers, ADC) have their own independent clock whatever the system clock. Two PLLs, each

3.10 时钟和启动

The STM32WB55xx and STM32WB35xx devices integrate several clock sources:

STM32WB55xx STM32WB35xx3.10 Clocks and startup
LSE: 32.768 kHz 外部晶体振荡器，用于精确的 RTC 和与其他嵌入式 RC 振荡器的校准。 LSI1: 32 kHz 上片低功耗 RC 振荡器。
LSI2: 接近 32 kHz，上片高稳定性 RC 振荡器，由无线电子子系统使用。 HSE: 高质量 32 MHz 外部晶体振荡器，可调整，由无线电子子系统需求。 HSI16: 16 MHz 高精度上片 RC 振荡器。 MSI: 100 kHz 到 48 MHz 多速上片低功耗振荡器，可以使用 LSE 信号调整。 HSI48: 48 MHz 上片 RC 振荡器，用于 USB 晶体无需情况。

时钟控制器(参见图9)将来自不同振荡器的时钟分配给核心和外围设备，包括无线电子子系统。它还管理低功耗模式的时钟屏蔽，并确保时钟的鲁棒性。它具有以下功能：

- **时钟预分频器:** 为了在速度和电流消耗之间获得最佳折衷，可以通过可编程的预分频器来调整给 CPU 和外设备时时频率。
- **安全时钟切换:** 在运行模式下，可以通过配置寄存器在不停机的情况下安全地更改时钟源。
- **时钟管理:** 为了减少功耗，时钟控制器可以停止向核心、单独的外围设备或内存供应时钟。
- **系统时钟源:** 可以使用四种不同的时钟源来驱动主时钟 SYSCLK:– 16 兆赫高速内部 RC 晶体振荡器 (HSI16)，可以通过软件进行校准，能够为 PLL – 提供时。(兆赫多速度内部 RC 晶体振荡器)MSI(，可以通过软件进行校准，能够生成 12 种频率，从 100 kHz 到 48 MHz。当系统中存在)LSE±0 32.768 kHz 时钟源时，MSI 频率可以通过硬件自动校准，以达到超过 – .25% 的精度。 MSI 能够为 PLL – 提供时。
- **{V24}辅助时钟源:** 两个超低功耗的时钟源，可以用来驱动 LCD 控制器和实时时钟:– 322.768 kHz 低速外部晶体 (LSE)，支持四种驱动能力模式。 LSE 也可以配置为绕过模式，以便使用外部时钟。 – 32 kHz 低速内部 RC (LSI)，也用于驱动独立看门狗。 LSI 时钟精度为 $\pm 5\%$ 。 LSI 时钟源可以是芯片上的 LSI1 或 LSI2 晶体振荡器。
- **外围设备时钟源:** 几个外围设备 (RNG, SAI, USARTs, I2C, LPTimers, ADC) 无论系统时钟如何，都有自己的独立时钟。两个 PLL，每个

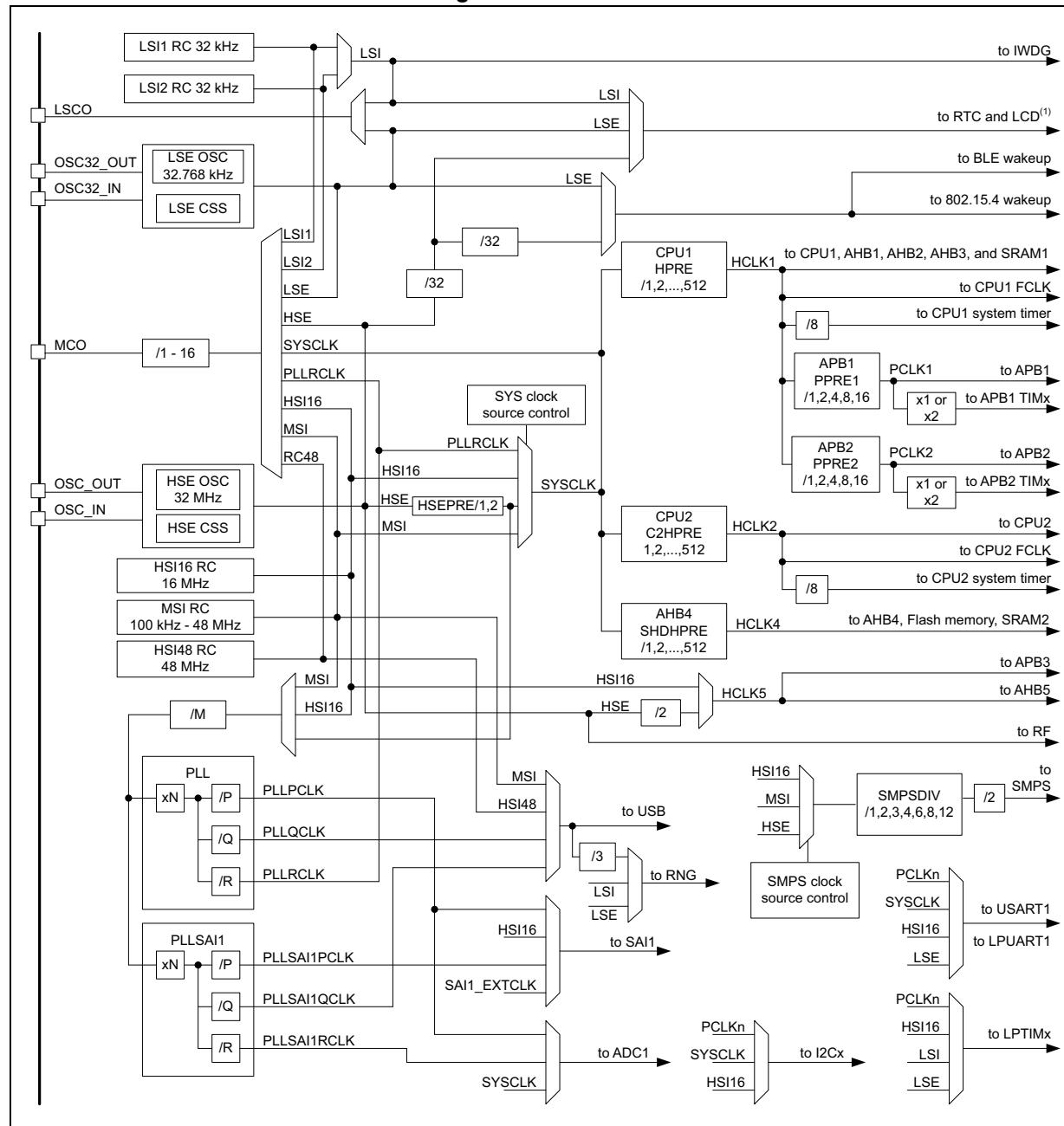
- having three independent outputs for the highest flexibility, can generate independent clocks for the ADC, the RNG and the SAI.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
 - **Clock security system (CSS):** this feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software interrupt is generated if enabled. LSE failure can also be detected and an interrupt generated.
 - Clock-out capability:
 - **MCO: microcontroller clock output:** it outputs one of the internal clocks for external use by the application. Low frequency clocks (LSIx, LSE) are available down to Stop 1 low power state.
 - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes down to Standby.

Several prescalers allow the user to configure the AHB frequencies, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 64 MHz.

- having three independent outputs for the highest flexibility, can generate independent clocks for the ADC, the RNG and the SAI.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
 - **Clock security system (CSS):** this feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software interrupt is generated if enabled. LSE failure can also be detected and an interrupt generated.
 - Clock-out capability:
 - **MCO: microcontroller clock output:** it outputs one of the internal clocks for external use by the application. Low frequency clocks (LSIx, LSE) are available down to Stop 1 low power state.
 - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes down to Standby.

几个预分频器允许用户配置 AHB 频率、高速 APB(APB2) 和低速 APB (APB1) 域。AHB 和 APB 域的最大频率为 64 MHz。

Figure 9. Clock tree

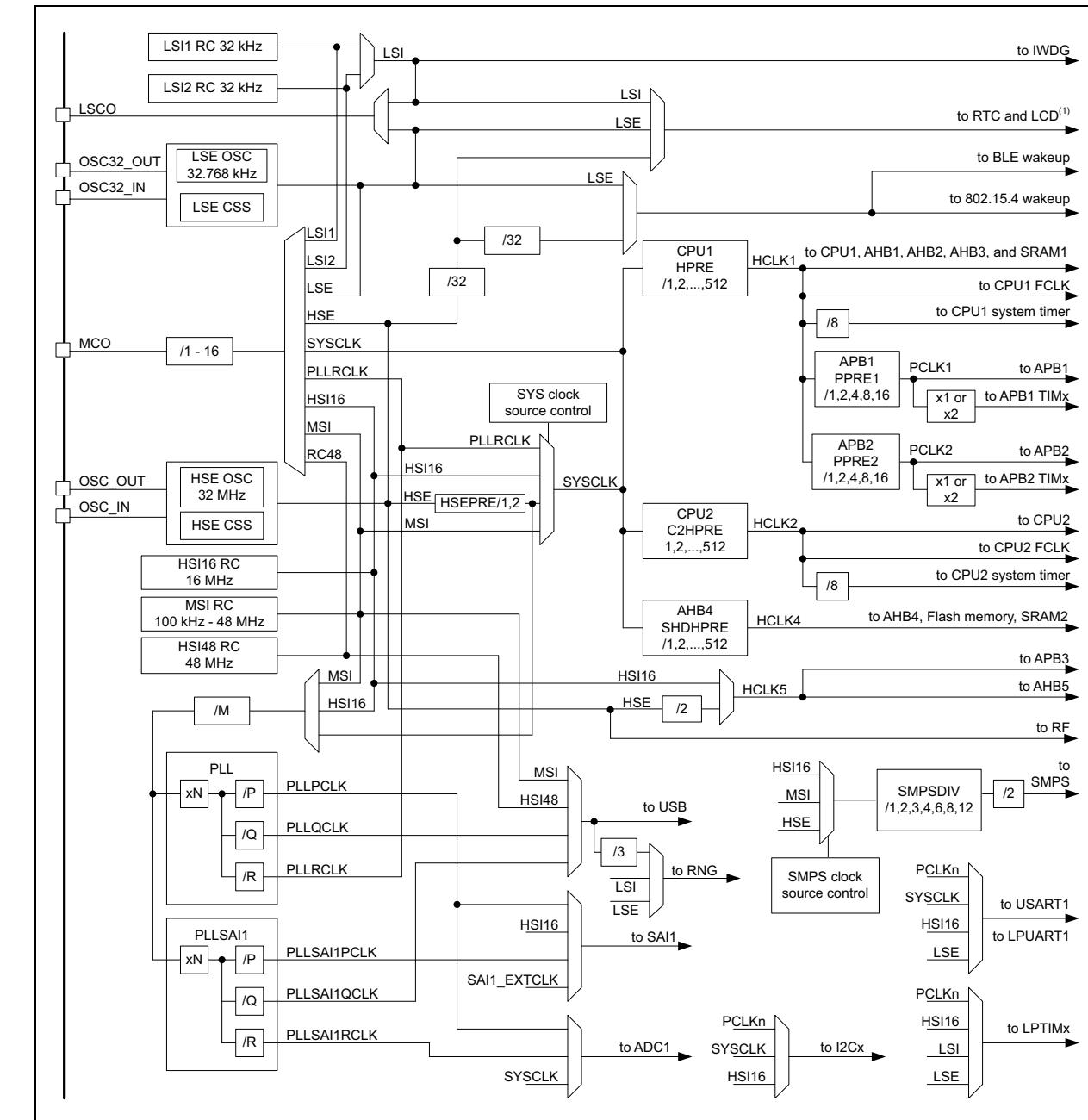


1. The LCD is not available on STM32WB35xx devices.

3.11 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

图9. 时钟树



1. LCD 在 M32WB35xx 设备上不可用。

3.11 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (推挽或开漏), as input (带或不带拉高或拉低) 或作为外设替代功能。大多数 GPIO 引脚与数字或模拟替代功能共享。通过将其映射到 AHB2 总线，可以实现快速 I/O 切换。

The I/Os alternate function configuration can be locked, if needed, following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.12 Direct memory access controller (DMA)

The device embeds two DMAs. Refer to [Table 10](#) for the features implementation.

Direct memory access (DMA) is used to provide high-speed data transfer between peripherals and memory as well as between memories. Data can be quickly moved by DMA without any CPU action. This keeps CPU resources free for other operations.

The two DMA controllers have fourteen channels in total, a full cross matrix allows any peripheral to be mapped on any of the available DMA channels. Each DMA has an arbiter for handling the priority between DMA requests.

The DMA supports:

- fourteen independently configurable channels (requests)
- A full cross matrix between peripherals and all the DMA channels exist. There is also a HW trigger possibility through the DMAMUX.
- Priorities between requests from DMA channels are software programmable (four levels consisting in very high, high, medium and low) or hardware in case of equality (request 1 has priority over request 2, etc.).
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management.
- Three event flags (DMA half transfer, DMA transfer complete and DMA transfer error) logically OR-ed together in a single interrupt request for each channel.
- Memory-to-memory transfer.
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers.
- Access to Flash memory, SRAM, APB and AHB peripherals as source and destination.
- Programmable number of data to be transferred: up to 65536.

Table 10. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	7	7

A DMAMUX block makes it possible to route any peripheral source to any DMA channel.

3.13 Interrupts and events

3.13.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 63 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

The I/Os alternate function configuration can be locked, if needed, following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.12 Direct memory access controller (DMA)

该设备集成了两个DMAs。参考 [表 10](#)以获取功能实现。

Direct memory access (DMA) 是用于在外围设备和内存之间以及在内存之间提供高速数据传输的。数据可以快速由 DMA 移动，而无需任何 CPU 行为。这将 CPU 资源保持自由，以便进行其他操作。

两个 DMA 控制器共有十四个通道，一个完整的交叉矩阵允许任何外围设备映射到可用的 DMA 通道上。每个 DMA 都有一个仲裁器来处理 DMA 请求之间的优先级。

The DMA supports:

- fourteen 配置的通道 (requests)• A full cross matrix between peripherals and all the DMA channels exist. There is also a HW trigger possibility through the DMAMUX. • Priorities between requests from DMA channels are software programmable (four levels consisting in very high, high, medium and low) or hardware in case of equality(request 1 has priority over request 2, etc.). • Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size. • Support for circular buffer management. • Three event flags (DMA half transfer, DMA transfer complete and DMA transfer error) logically OR-ed together in a single interrupt request for each channel. • Memory-to-memory transfer. • Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers. • Access to Flash memory, SRAM, APB and AHB peripherals as source and destination. • Programmable number of data to be transferred: up to 65536.

表 10. DMA 实现

DMA features	DMA1	DMA2
Number of regular channels	7	7

A DMAMUX 块使得可以将任何外围设备源路由到任何 DMA 通道。

3.13 中断和事件

3.13.1 嵌套向量中断控制器 (NVIC)

这些设备嵌入了一个能够管理 16 优先级别的嵌套向量中断控制器，能够处理高达 63 个可屏蔽中断通道加上 Cortex®-M4 的 16 中断线，其中包含 FPU。

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.13.2 Extended interrupts and events controller (EXTI)

The EXTI manages wakeup through configurable and direct event inputs. It provides wake-up requests to the Power control, and generates interrupt requests to the CPUx NVIC and events to the CPUx event input.

Configurable events/interrupts come from peripherals able to generate a pulse, and make it possible to select the Event/Interrupt trigger edge and/or a SW trigger.

Direct events/interrupts are coming from peripherals having their own clearing mechanism.

3.14 Analog to digital converter (ADC)

The device embeds a successive approximation analog-to-digital converter with the following features:

- 12-bit native resolution, with built-in calibration
- Up to 16-bit resolution with 256 oversampling ratio
- 4.26 Msps maximum conversion rate with full resolution
 - Down to 39 ns sampling time
 - Increased conversion rate for lower resolution (up to 7.11 Msps for 6-bit resolution)
- Up to sixteen external channels and three internal channels: internal reference voltages, temperature sensor
- Single-ended and differential mode inputs
- Low-power design
 - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
 - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
 - Single-shot or continuous/discontinuous sequencer-based scan mode: two groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
 - The ADC supports multiple trigger inputs for synchronization with on-chip timers and external signals
 - Results stored into three data register or in SRAM with DMA controller support

NVIC 的优势如下:

- 紧密耦合的 NVIC 给出低延迟的中断处理
- 中断入口向量表地址直接传递给核心
- 允许早期处理中断
- 处理晚到达的更高优先级中断
- 支持尾随链接
- 自动保存处理器状态
- 在中断退出时恢复中断入口, 无指令开销

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.13.2 扩展中断和事件控制器 (EXTI)

The EXTI manages wakeup through configurable and direct event inputs. It provides wake-up requests to the Power control, and generates interrupt requests to the CPUx NVIC and events to the CPUx event input.

Configurable events/interrupts come from peripherals able to generate a pulse, and make it possible to select the Event/Interrupt trigger edge and/or a SW trigger.

Direct events/interrupts are coming from peripherals having their own clearing mechanism.

3.14 Analog to digital converter (ADC)

该设备集成了具有以下功能的逐级逼近模拟到数字转换器:

- 12-bit原生分辨率, 带有内置校准
- 最高16位分辨率, 256超采样比例
- 4.26 Msps最大转换速率, 全分辨率—采样时间低至39 ns—低分辨率下的转换速率增加(最高6位分辨率为7.11 Msps)
- 最高十六个外部通道和三个内部通道: 内部参考电压, 温度传感器
- 单端和差分模式输入
- 低功耗设计—在低转换速率下可进行低电流运行(消耗随速度线性降低)
- 双时钟域架构: ADC速度与CPU频率无关
- 非常灵活的数字接口
- 单脉冲或连续/不连续序列器基于扫描模式: 两组模拟信号转换可以编程来区分背景和高优先级实时转换
- ADC支持多个触发输入用于与片上计数器和外部信号同步
- 结果存储在三个数据寄存器或使用DMA控制器支持的SRAM中

- Data pre-processing: left/right alignment and per channel offset compensation
- Built-in oversampling unit for enhanced SNR
- Channel-wise programmable sampling time
- Three analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
- Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.14.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN17 input channel, which is used to convert the sensor output voltage into a digital value.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored in the system memory area, accessible in read-only mode.

Table 11. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.14.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and the comparators. V_{REFINT} is internally connected to the ADC1_IN0 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 12. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.6$ V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

- 数据预处理：左右对齐和每通道偏移补偿
- 内置过采样单元用于增强的信号噪声比
- 通道可编程采样时间
- 三个模拟看门狗用于自动电压监控，生成中断
- 和为选择的计时器设置触发
- 硬件助手准备注入通道的上下文以允许快速上下文切换

3.14.1 温度传感器

温度传感器 (TS) 生成一个与温度线性变化的电压 V_{TS} 。

温度传感器内部连接到 ADC1_IN17 输入通道，用于将传感器输出电压转换为数字值。

为了提高温度传感器测量的精度，每个设备都由 ST 个工厂校准。温度传感器工厂校准数据是存储在系统内存区域中，以只读模式访问。

表11. 温度传感器校准值

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.14.2 内部电压参考 (V_{REFINT}) (V_{REFINT})

内部电压参考 (V_{REFINT}) (V_{REFINT}) 为 ADC 和 比较器 提供一个稳定的 (带隙) 电压输出。 V_{REFINT} 内部连接到 ADC1_IN0 输入通道。 V_{REFINT} 的精确电压由 ST 在生产测试期间为每个部件 量并存储在系统内存区域中。它以只读模式访问。

表 12. 内部电压参考校准值

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.6$ V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.15 Voltage reference buffer (VREFBUF)

The STM32WB55xx devices embed a voltage reference buffer that can be used as voltage reference for the ADC and also as voltage reference for external components through the VREF+ pin. The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off. The VREF+ pin is double-bonded with VDDA on UFQFPN48 package, hence the internal voltage reference buffer is not available on a dedicated pin, but user can still use the V_{DDA} value.

3.16 Comparators (COMP)

The STM32WB55xx and STM32WB35xx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.17 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric such as glass or plastic. The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library (free to use) and enables reliable touch sensing functionality in the end application.

3.15 Voltage reference buffer (VREFBUF)

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3.16 Comparators (COMP)

The STM32WB55xx and STM32WB35xx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

所有比较器都可以从停止模式唤醒，生成中断并为定时器提供中断，并且还可以组合成一个窗口比较器。

3.17 触摸控制器 (TSC)

触摸控制器提供了一种简单的解决方案，用于向任何应用程序添加电容式感应功能。电容式感应技术能够检测手指靠近受绝缘体（如玻璃或塑料）保护的电极附近的存在。手指引入的电容变化（或任何导电对象）通过基于表面电荷传输获取原则的经过验证的实现进行测量。

触摸控制器完全得到 STMTouch 触摸感应固件库（免费使用）的支持，并使最终应用程序中的可靠触摸感应功能得以实现。

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 18 capacitive sensing channels
- Up to six capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to three capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent upon the package (not available on QFPN48) and subject to I/O availability.

触摸控制器的主要功能如下：

- 成熟且可靠的表面电荷传输获取原则
- 支持高达18个电容式传感器通道
- 最多可以并行采集六个电容式传感器通道，提供非常好的响应时间
- 扩频功能，提高嘈杂环境下系统的鲁棒性
- 完全硬件管理电荷转移采集序列
- 可编程的电荷转移频率
- 可编程的采样电容器I/O引脚
- 可编程的通道I/O引脚
- 可编程的最大计数值，避免在通道故障时进行长时间采集
- 专用的采集结束和最大计数错误标志带中断能力
- 一个采样电容器可用于减少三个电容式传感器通道
- 兼近距离、触摸按键、线性和旋转触摸传感器实现
- 设计用于与 STMTouch 触摸感应固件库一起工作

注意：电容式传感器通道的数量取决于包（不可用于 QFPN48）并且受到 I/O 可用性的影响。

3.18 Liquid crystal display controller (LCD)

The STM32WB55xx devices embed an LCD controller with the following characteristics:

- Highly flexible frame rate control.
- Supports Static, 1/2, 1/3, 1/4 and 1/8 duty.
- Supports Static, 1/2, 1/3 and 1/4 bias.
- Double buffered memory allows data in LCD_RAM registers to be updated at any time by the application firmware without affecting the integrity of the data displayed.
 - LCD data RAM of up to 16 x 32-bit registers which contain pixel information (active/inactive)
- Software selectable LCD output voltage (contrast) from VLCD_{min} to VLCD_{max}.
- No need for external analog components:
 - A step-up converter is embedded to generate an internal VLCD voltage higher than V_{DD} (up to 3.6 V if V_{DD} > 2.0 V)
 - Software selection between external and internal VLCD voltage source. In case of an external source, the internal boost circuit is disabled to reduce power consumption
 - A resistive network is embedded to generate intermediate VLCD voltages
 - The structure of the resistive network is configurable by software to adapt the power consumption to match the capacitive charge required by the LCD panel
 - Integrated voltage output buffers for higher LCD driving capability.
- The contrast can be adjusted using two different methods:
 - When using the internal step-up converter, the software can adjust VLCD between VLCD_{min} and VLCD_{max}
 - Programmable dead time (up to eight phase periods) between frames.
- Full support of low-power modes: the LCD controller can be displayed in Sleep, Low-power run, Low-power sleep and Stop modes, or can be fully disabled to reduce power consumption.
- Built in phase inversion for reduced power consumption and EMI (electromagnetic interference).
- Start of frame interrupt to synchronize the software when updating the LCD data RAM.
- Blink capability:
 - 1, 2, 3, 4, 8 or all pixels can be programmed to blink at a configurable frequency
 - Software adjustable blink frequency to achieve around 0.5 Hz, 1 Hz, 2 Hz or 4 Hz.

Used LCD segment and common pins should be configured as GPIO alternate functions and unused segment and common pins can be used for general purpose I/O or for another peripheral alternate function.

Note: When the LCD relies on the internal step-up converter, the VLCD pin should be connected to V_{SS} with a capacitor. Its typical value is 1 μ F.

3.19 True random number generator (RNG)

The devices embed a true RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.18 液晶显示控制器 (LCD)

The STM32WB55xx devices embed an LCD controller with the following characteristics:

- 高度灵活的帧率控制。• 支持静态、1/2、1/3、1/4和1/8占空比。• 支持静态、1/2、1/3和1/4偏置。• 双缓冲存储允许应用程序件随时更新LCD_RAM 寄存器中的数据，而无需影响显示数据的完整性。– LCD 数据 RAM 最多为 16 x 32 位寄存器，包含像素信息。(active/inactive)• 软件可选择的 LCD 输出电压。(对比度。)从 VLCD_{min} 到 VLCD_{max}。• 无需外部模拟组件：– 集成了一个升压转换器来生成高于 VDD 的内部 VLCD 电压。(高达 3.6 V 如果 VDD > 2.0 V。)– 软件可选择外部和内部 VLCD 电压来源。在使用外部来源时，内部升压电路被禁用以降低功耗。– 集成了一个阻性网络来生成中间 VLCD 电压。– 阻性网络的结构可以通过软件进行配置以适应 LCD 面板所需的电容充电，从而降低功耗。– 集成的电压输出缓冲器用于提高 LCD 驱动能力。• 对比度可以使用两种不同的方法进行调整：– 使用内部升压转换器时，软件可以调整 VLCD 在 VLCD_{min} 和 VLCD_{max} 之间。– 可编程死时间。(最大到八个相反转换周期。)帧之间。• 完全支持低功耗模式：LCD 控制器可以处于睡眠、低功耗运行、低功耗睡眠和停止模式，或者可以完全禁用以降低功耗。• 集成了相反转换以降低功耗和 EMI。(电磁干扰。)• 帧开始中断用于在更新 LCD 数据 RAM 时同步软件。• 闪烁功能：– 1, 2, 3, 4, 8 或所有像素都可以编程在可配置的频率上闪烁。– 软件可调整的闪烁频率可以实现大约 0.5 Hz、1 Hz、2 Hz 或 4 Hz。

用于 LCD 段和公共引脚应配置为 GPIO 替代功能，未使用的段和公共引脚可以用于通用输入/输出或另一个外围替代功能。

Note: 当 LCD 依赖于内部升压转换器时，VLCD 引脚应连接到 VSS，并附上电容器。其典型值为 1 μ F。

3.19 真随机数生成器 (RNG)

设备集成了一个真正的 RNG，它通过集成的模拟电路生成 32 位随机数。

3.20 Timers and watchdogs

The STM32WB55xx and STM32WB35xx include one advanced 16-bit timer, one general-purpose 32-bit timer, two 16-bit basic timers, two low-power timers, two watchdog timers and a SysTick timer. [Table 13](#) compares the features of the advanced control, general purpose and basic timers.

Table 13. Timer features

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bits	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General purpose	TIM2	32-bits	Up, down, Up/down			4	No
General purpose	TIM16	16-bits	Up			2	1
General purpose	TIM17	16-bits	Up			2	1
Low power	LPTIM1 LPTIM2	16-bits	Up			1	1

3.20.1 Advanced-control timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0 to 100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in [Section 3.20.2](#)) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.20.2 General-purpose timers (TIM2, TIM16, TIM17)

There are up to three synchronizable general-purpose timers embedded in the STM32WB55xx and STM32WB35xx (see [Table 13](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2
 - Full-featured general-purpose timer

3.20 定时器和看门狗

The STM32WB55xx and STM32WB35xx include one advanced 16-bit timer, one general-purpose 32-bit timer, two 16-bit basic timers, two low-power timers, two watchdog timers and a SysTick timer. [Table 13](#) compares the features of the advanced control, general purpose and basic timers.

表 13. 定时器功能

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bits	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General purpose	TIM2	32-bits	Up, down, Up/down			4	No
General purpose	TIM16	16-bits	Up			2	1
General purpose	TIM17	16-bits	Up			2	1
Low power	LPTIM1 LPTIM2	16-bits	Up			1	1

3.20.1 Advanced-control timer (TIM1)

高级控制定时器可以看作是在六个通道上复用的三相 PWM。它们具有可编程插入死时间的互补 PWM 输出。它们也可以看作是完整的通用计时器。这四个独立通道可以用于：

- 输入捕获
- 输出比较
- PWM 生成 (边缘或中心对齐模式) 具全范围调制能力 (0 到 100%)
- 单脉冲模式输出

在调试模式下，高级控制定时器计数器可以被冻结，并且 PWM 输出可以被禁用以关闭由这些输出驱动的任何电源开关。

许多功能与通用 TIMx 计时器共享(描述 [第 3.20 节 2](#)) 使用相同的架构，因此高级控制定时器可以通过计时器链接功能与 TIMx 计时器一起工作，进行同步或事件链式。

3.20.2 通用计时器 (TIM2, TIM16, TIM17)

STM32WB55xxxx STM32WB35xx 中嵌入了最多三个可同步的通用计时器 (参见 [表 13](#) 以查看差异)。每个通用计时器都可以用来生成 PWM 输出，或者作为简单的时间基准。

- TIM2 – 完整功能的通用计时器

- Features four independent channels for input capture/output compare, PWM or one-pulse mode output. Can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.
- The counter can be frozen in debug mode.
- Independent DMA request generation, support of quadrature encoders.
- TIM16 and TIM17
 - General-purpose timers with mid-range features:
 - 16-bit auto-reload upcounters and 16-bit prescalers.
 - 1 channel and 1 complementary channel.
 - All channels can be used for input capture/output compare, PWM or one-pulse mode output.
 - The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.
 - The counters can be frozen in debug mode.

3.20.3 Low-power timer (LPTIM1 and LPTIM2)

The devices embed two low-power timers, having an independent clock running in Stop mode if they are clocked by LSE, LSIX or by an external clock. They are able to wakeup the system from Stop mode.

LPTIM1 is active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 modes.

The low-power timers support the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
 - Internal clock sources: LSE, either LSI1 or LSI2, HSI16 or APB clock
 - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application)
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only)

3.20.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

- 具有四个独立通道，用于输入捕获/输出比较、PWM或单脉冲模式输出。可以共同工作，或者通过计时器链接功能与其他通用计时器进行同步或事件链式连接。
- 计数器可以在调试模式下冻结。
- 独立的DMA请求生成，支持四象限编码器。
- TIM16和TIM17
 - 通用计时器具有中等级特性：- 16-bit 自动重装载上计数器和 16位预分频器。
 - 1 通道和 1 个补充通道。
 - 所有通道都可以用于输入捕获/输出比较、PWM 或单脉冲模式输出。
 - 计时器可以通过计时器链接功能进行同步或事件链式。
 - 计时器具有独立的 DMA 请求生成。
 - 计数器可以在调试模式下冻结。

3.20.3 低功耗计时器 (LPTIM1 和 LPTIM2)

设备集成了两个低功耗计时器，如果由 LSE、LSIx 或外部时钟驱动，则在停止模式下以独立时钟运行。它们能够从停止模式唤醒系统。

LPTIM1 在停止模式 0、停止模式 1 和停止模式 2 下有效。

LPTIM2 在停止模式 0 和停止模式 1 下有效。

低功耗计时器支持以下功能：

- 16-bit 上计数器，配备 16-bit 自动重载寄存器
- 16-bit 比较寄存器
- 可配置输出：脉冲，PWM
- 连续/单脉冲模式
- 可选软件/硬件输入触发
- 可选时钟源
 - 内部时钟源：LSE，LSI1 或 LSI2，HSI16 或 APB 时钟
 - 通过LPTIM输入的外部时钟源（即使没有运行内部时钟源也能工作，用于脉冲计数器应用）
- 可编程数字杂散滤波器
- 编码器模式（仅适用于 LPTIM1）

3.20.4 独立看门狗 (IWDG)

独立看门狗基于 12位下计数器和 8位预分频器。它从独立的 32 kHz 内部 RC LSI(LSI) 获取时钟，并且由于它与主时钟独立运行，因此可以在停止和待机模式下运行。它可以用作看门狗来在出现问题时复位设备，或者用作应用程序超时管理的自由运行定时器。它可以通过选项字节进行硬件或软件配置。计数器可以在调试模式下冻结。

3.20.5 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.20.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- a maskable system interrupt generation when the counter reaches 0
- a programmable clock source.

3.21 Real-time clock (RTC) and backup registers

The RTC is an independent BCD timer/counter, supporting the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature, which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 20 backup registers are supplied through a switch that takes power either from the V_{DD} supply (when present) or from the VBAT pin.

The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby or Shutdown mode.

The RTC clock sources can be:

- a 32.768 kHz external crystal (LSE)
- an external resonator or oscillator (LSE)
- one of the internal low power RC oscillators (LSI1 or LSI2, with typical frequency of 32 kHz)
- the high-speed external clock (HSE) divided by 32.

3.20.5 System window watchdog (WWDG)

窗口看门狗基于一个可以设置为自由运行的7位下计数器。它可以作为看门狗使用，当发生问题时复位设备。它从主时钟获取时钟信号。它具有早期警告中断功能，计数器可以在调试模式下冻结。

3.20.6 SysTick 定时器

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24位下计数器
- 自动重载功能
- a 可屏蔽的系统中断生成当计数器达到 0
- a 可编程的时钟源.

3.21 实时时钟 (RTC) 和备份寄存器

STM32WB55xx STM32WB35xx 3.21 实时时钟 (RTC) 和备份寄存器 RTC 是一个独立的 BCD 计时器/计数器，支持以下功能：

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature, which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

RTC 和 20 个备份寄存器通过一个开关供电，该开关从 V_{DD} 供电（存在）或 VBAT 引脚供电。

备份寄存器是 32 位寄存器，用于在没有 V_{DD} 电源时存储 80 字节的用户应用数据。它们不会由系统复位或电源复位，也不会在设备从待机或关闭模式唤醒时复位。

RTC 时钟源可以是：

- 一 2.768 kHz 外部晶体 (LSE)
- 一个外部共振器或振荡器 (LSE)
- 一个内部低功耗 RC 振荡器 (LSI1 或 LSI2, 典型频率 32 kHz)
- 高速外部时钟 (HSE) 除以 32。

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by one of the LSIs, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (alarm, wakeup timer, timestamp or tamper) can generate an interrupt and wakeup the device from the low-power modes.

3.22 Inter-integrated circuit interface (I2C)

The devices embed two I2Cs. Refer to [Table 14](#) for the features implementation.

The I²C bus interface handles communications between the microcontroller and the serial I²C bus. It controls all I²C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I²C-bus specification and user manual rev. 5 compatibility:
 - Slave and master modes, multimaster capability
 - Standard-mode (Sm), with a bitrate up to 100 kbit/s
 - Fast-mode (Fm), with a bitrate up to 400 kbit/s
 - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
 - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
 - Programmable setup and hold times
 - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
 - Hardware PEC (packet error checking) generation and verification with ACK control
 - Address resolution protocol (ARP) support
 - SMBus alert
- Power System Management Protocol (PMBusTM) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to [Figure 9: Clock tree](#).
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 14. I2C implementation

I2C features ⁽¹⁾	I2C1	I2C3
Standard-mode (up to 100 kbit/s)	X	X
Fast-mode (up to 400 kbit/s)	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X
Programmable analog and digital noise filters	X	X
SMBus/PMBus hardware support	X	X

RTC 在 VBAT 模式下以及在所有低功耗模式下都可用，当它由 LSE 调制时。当它由其中一个内部低频晶体振荡器调制时，RTC 不可用于 VBAT 模式，但在所有低功耗模式下均可用，除了关闭模式。

所有 RTC 事件 (报警、唤醒计数器、时间戳或篡改) 都可以生成中断并从低功耗模式唤醒设备。

3.22 Inter-integrated circuit interface (I2C)

The devices embed two I2Cs. Refer to [Table 14](#) for the features implementation.

I2C总线接口处理微控制器与串行I2C总线之间的通信。它控制所有I2C总线特定的序列化、协议、仲裁和时序。

The I2C peripheral supports:

STM32WB55xx STM32WB35xx3.22 Inter-integrated circuit interface (I2C) specification and user manual rev. 5 compatibility:从机和主机模式，多主机能力标准模式 SM，比特率高达 100 kbit/s快速模式 Fm，比特率高达 400 kbit/s快速模式加 Fm，比特率高达 1 Mbit/s且具有 20 mA 输出驱动的输入/输出

STM32WB55xx STM32WB35xx3.22 Inter-integrated circuit interface (I2C)– 7-bit 和 10-bit 地址模式，多个 7-bit 从机地址 – 可编程设置和保持时间 – 可选的时钟拉长 • 系统管理总线 (SMBusTM) 规范 rev 2.0 兼容性： – 硬件 PEC (数据包错误检测) 与 ACK 控制一起的生成和验证 – 地址分辨率协议 (ARP) 支持 – SMBus 警告 • 电源管理协议 (PMBusTM) 规范 rev 1.1 兼容性 • 独立时钟：选择独立时钟源，使 I2C 通信速度可以独立于 PCLK 重编程。参考 图9：时钟树。 • 在地址匹配时从停止模式唤醒 • 可编程模拟和数字噪声过滤器 • 1字节缓冲区具有 DMA 能力

表 14. I2C 实现

I2C features ⁽¹⁾	I2C1	I2C3
Standard-mode (up to 100 kbit/s)	X	X
Fast-mode (up to 400 kbit/s)	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X
Programmable analog and digital noise filters	X	X
SMBus/PMBus hardware support	X	X

Table 14. I2C implementation (continued)

I2C features ⁽¹⁾	I2C1	I2C3
Independent clock	X	X
Wakeup from Stop 0 / Stop 1 mode on address match	X	X
Wakeup from Stop 2 mode on address match	-	X

1. X: supported

3.23 Universal synchronous/asynchronous receiver transmitter (USART)

The devices embed one universal synchronous receiver transmitter.

This interface provides asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and has LIN Master/Slave capability. It provides hardware management of the CTS and RTS signals, and RS485 driver enable.

The USART is able to communicate at speeds of up to 4 Mbit/s, and also provides Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

The USART supports synchronous operation (SPI mode), and can be used as an SPI master.

The USART has a clock domain independent from the CPU clock, allowing it to wake up the MCU from Stop mode using baudrates up to 200 kbaud. The wake up events from Stop mode are programmable and can be:

- the start bit detection
- any received data frame
- a specific programmed data frame.

The USART interface can be served by the DMA controller.

3.24 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART, enabling asynchronous serial communication with minimum power consumption. The LPUART supports half duplex single wire communication and modem operations (CTS/RTS), allowing multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode using baudrates up to 220 kbaud. The wake up events from Stop mode are programmable and can be:

- the start bit detection
- any received data frame
- a specific programmed data frame.

Only a 32.768 kHz clock (LSE) is needed for LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an

表 14. I2C 实现 (继续)

I2C features ⁽¹⁾	I2C1	I2C3
Independent clock	X	X
Wakeup from Stop 0 / Stop 1 mode on address match	X	X
Wakeup from Stop 2 mode on address match	-	X

1. X: supported

3.23 通用同步/异步接收-发送器 (USART)

设备集成了一个通用同步接收发送器。

此接口提供异步通信, IrDA SIR ENDEC 支持, 多处理器通信模式, 单线半双工通信模式, 并具有 LIN 主从机功能。它提供 CTS 和 RTS 信号的硬件管理, 并启用 RS485 驱动器。

USART 能够以高达 4 Mbit/s 的速度进行通信, 并提供符合 ISO 7816 的智能卡模式和 SPI 相似通信能力。

USART 支持 (SPI 模式)的同步操作, 并可作为 SPI 主机使用。

USART 具有与 CPU 时钟独立的时钟域, 允许在使用高达 200 kbaud 的波特率时从停止模式唤醒 MCU。停止模式的唤醒事件是可编程的, 并且可以是:

- 起始位检测
- 任何接收数据帧
- 一个特定的编程数据帧。

The USART interface can be served by the DMA controller.

3.24 低功耗异步接收发送器(LPUART)

The device embeds one Low-Power UART, enabling asynchronous serial communication with minimum power consumption. The LPUART supports half duplex single wire communication and modem operations (CTS/RTS), allowing multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode using baudrates up to 220 kbaud. The wake up events from Stop mode are programmable and can be:

- the start bit detection
- any received data frame
- a specific programmed data frame.

Only a 32.768 kHz 时钟 (LSE) is needed for LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an



extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

The LPUART interfaces can be served by the DMA controller.

3.25 Serial peripheral interface (SPI1, SPI2)

Two SPI interfaces enable communication up to 32 Mbit/s in master and up to 24 Mbit/s in slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation.

The SPI interfaces can be served by the DMA controller.

3.26 Serial audio interfaces (SAI1)

The device embeds a dual channel SAI peripheral that supports full duplex audio operation. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

The SAI peripheral supports:

- One independent audio sub-block that can be a transmitter or a receiver, with the respective FIFO
- 8-word integrated FIFOs
- Synchronous or asynchronous mode
- Master or slave configuration
- Clock generator to target independent audio frequency sampling when audio sub-block is configured in master mode
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF out
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame
- Number of bits by frame may be configurable
- Frame synchronization active level configurable (offset, bit length, level)
- First active bit position in the slot is configurable
- LSB first or MSB first for data transfer
- Mute mode
- Stereo/Mono audio frame capability
- Communication clock strobing edge configurable (SCK)
- Error flags with associated interrupts if enabled respectively
 - Overrun and underrun detection
 - Anticipated frame synchronization signal detection in slave mode
 - Late frame synchronization signal detection in slave mode
 - Codec not ready for the AC'97 mode in reception

极低的能量消耗。更高速度的时钟可以用于实现更高的波特率。

LPUART接口可以由DMA控制器提供服务。

3.25 串行外围接口 (SPI1, SPI2)

两个 SPI 接口支持主机模式下的最高 32 Mbit/s 的通信速度，以及从机模式下的最高 24 Mbit/s 的通信速度，支持半双工、全双工和单工模式。3位预分频器提供 8 个主机模式频率，帧大小可以配置为 4 位到 16 位。SPI 接口支持 NSS 脉冲模式、TI 模式和硬件CRC计算。

SPI 接口可以由 DMA 控制器提供服务。

3.26 串行音频接口 (SAI1)

设备集成了一个支持全双工音频操作的双通道SAI外围设备。SAI总线接口处理微控制器和串行音频协议之间的通信。

SAI外围设备支持：

- 一个独立的音频子块，可以是发射器或接收器，具有相应的FIFO• 8-字集成FIFOs
- 同步或异步模式• 主或从配置• 在音频子块配置为主模式时，时钟生成器可用于目标独立的音频频率采样• 数据大小可配置：8-, 10-, 16-, 20-, 24-, 32-bit• 具有大量可配置性和灵活性的外围设备，允许将其作为示例目标以下音频协议：I2S, LSB或MSB对齐, PCM/DSP, TDM, AC'97 以及 SPDIF 输出• 最多可用 16 个插槽，具有可配置的大小，并且可以选择哪些在音频帧中激活• 每帧的比特数可能可配置• 帧同步有效水平可配置（偏移, 比特长度, 水平）• 插槽中的首个有效比特位置可配置• LSB先或MSB先用于数据传输• 静音模式• 立体声/单声道音频帧能力• 通信时钟扫描边缘可配置 (SCK)• 如果启用则存在的错误标志与相关的中断— 溢出和未溢出检测— 从机模式下的预期帧同步信号检测— 从机模式下的延迟帧同步信号检测— Codec不准备处理AC'97 接收模式

- Interruption sources when enabled:
 - Errors
 - FIFO requests
- DMA interface with two dedicated channels to handle access to the dedicated integrated FIFO of the SAI audio sub-block.

The PDM (Pulse Density Modulation) block allows the user to manage up to three digital microphone pairs (with two different clocks). This block performs Right and Left microphone de-interleaving and time alignment through programmable delay lines in order to properly feed the SAI.

3.27 Quad-SPI memory interface (QUADSPI)

The Quad-SPI is a specialized communication interface targeting single, dual or quad SPI Flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash memory is mapped and is seen by the system as if it were an internal memory. This mode can be used for the Execute In Place (XIP)

The Quad-SPI interface supports:

- Three functional modes: indirect, status-polling, and memory-mapped
- SDR and DDR support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
- Each of the five following phases can be configured independently (enable, length, single/dual/quad communication)
 - Instruction phase
 - Address phase
 - Alternate bytes phase
 - Dummy cycles phase
 - Data phase
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Programmable masking for external Flash memory flag management
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

- Interruption sources when enabled:
 - Errors
 - FIFO requests
- DMA interface with two dedicated channels to handle access to the dedicated integrated FIFO of the SAI audio sub-block.

The PDM (Pulse Density Modulation) block allows the user to manage up to three digital microphone pairs (with two different clocks). This block performs Right and Left microphone de-interleaving and time alignment through programmable delay lines in order to properly feed the SAI.

3.27 四线SPI 内存接口 (四线SPI)

四线SPI是一种专门用于单线、双线或四线闪存内存的通信接口。它可以在以下三种模式中运行：

- 间接模式：所有操作都使用QUADSPI寄存器进行
- 状态轮询模式：外部内存状态寄存器会被周期性地读取，并且可以生成中断
- 内存映射模式：外部闪存内存被映射，并且系统将其视为内部内存。此模式可用于执行在原地 (XIP)

四线SPI接口支持：

- 三种功能模式：间接、状态轮询和内存映射
- SDR和DDR支持
- 完全可编程的指令代码，适用于间接和内存映射模式
- 完全可编程的帧格式，适用于间接和内存映射模式
- 每个以下五个阶段都可以独立配置 (使能、长度、单线/双线/四线通信)
 - 指令阶段
 - 地址阶段
 - 交替字节阶段
 - 哨兵周期阶段
 - 数据阶段
- 集成FIFO用于接收和传输
- 8, 16 和 32 位数据访问被允许
- DMA通道用于间接模式操作
- 完全可编程的掩码用于外部闪存内存标志管理
- 超时管理
- 基于FIFO阈值、超时、状态匹配、操作完成和访问错误的中断生成

3.28 Development support

3.28.1 Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using only two pins instead of the five required by the JTAG (JTAG pins can then be reused as GPIOs with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.28.2 Embedded Trace Macrocell™

The Arm® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32WB55xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

3.28 开发支持

3.28.1 串行线 JTAG 调试端口 (SWJ-DP)

Arm® 串行线 JTAG 调试端口是嵌入式的，它是一个结合了 JTAG 和 串行调试 的端口，可以连接连接连接行调调或或 或探到目标。

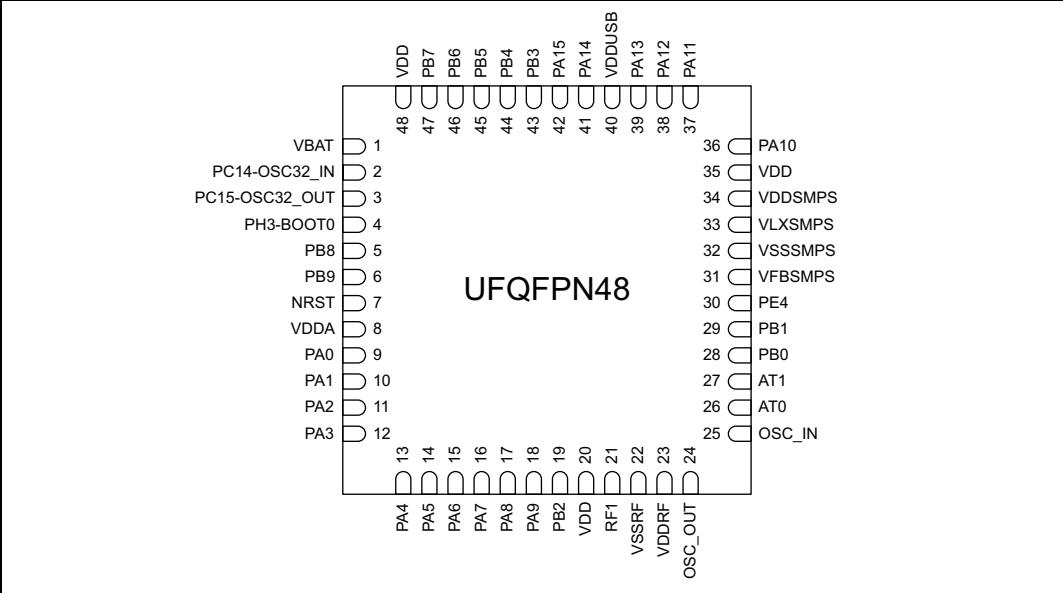
调试使用两个引脚而不是 JTAG 需要的五个引脚进行。然后，JTAG 引脚可以作为具有替代功能的 GPIOs 被重用：JTAG TMS 和 TCK 引脚分别与 SWDIO 和 SWCLK 共享，而在 TMS 引脚上的特定序列用于在 JTAG-DP 和 SW-DP 之间切换。

3.28.2 Embedded Trace Macrocell™

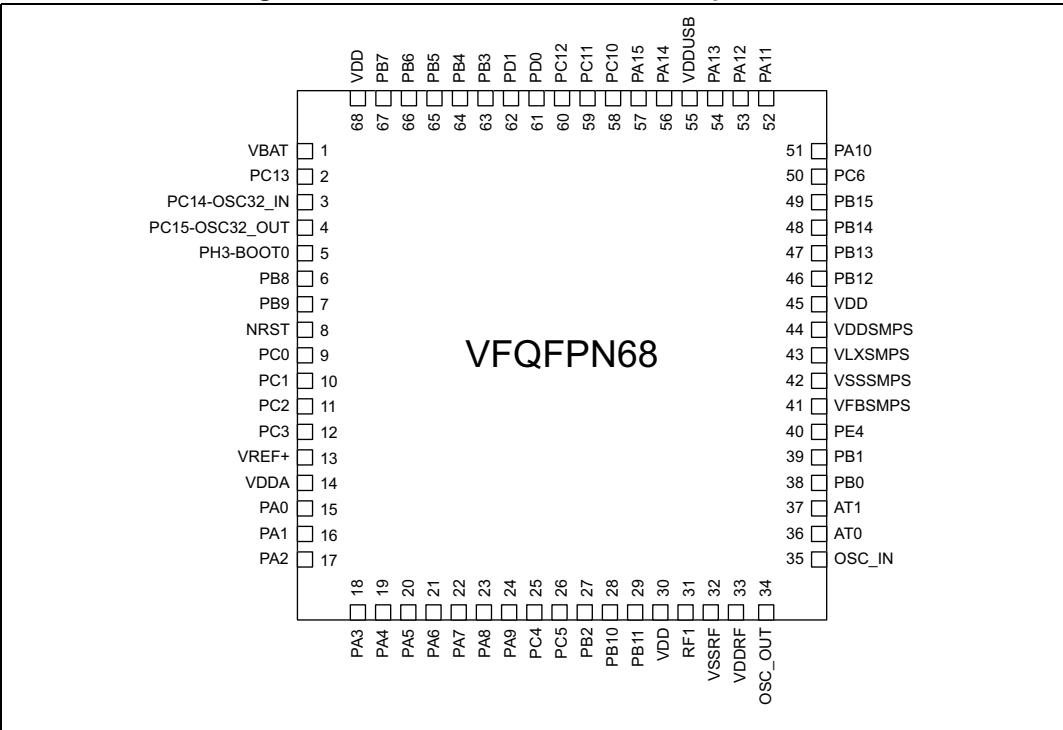
Arm 嵌入式跟踪宏单元提供了对CPU核心内部指令和数据流的更高可见性，通过从 STM32WB55xx 通过少量ETM引脚以非常高的速率流动压缩数据到外部硬件跟踪分析器。实时指令和数据流可以被记录并格式化用于显示在运行调试软件的主机计算机上。TPA硬件由常见的开发工具供应商提供。

嵌入式跟踪宏单元与第三方调试软件工具一起工作。

4 Pinouts and pin description

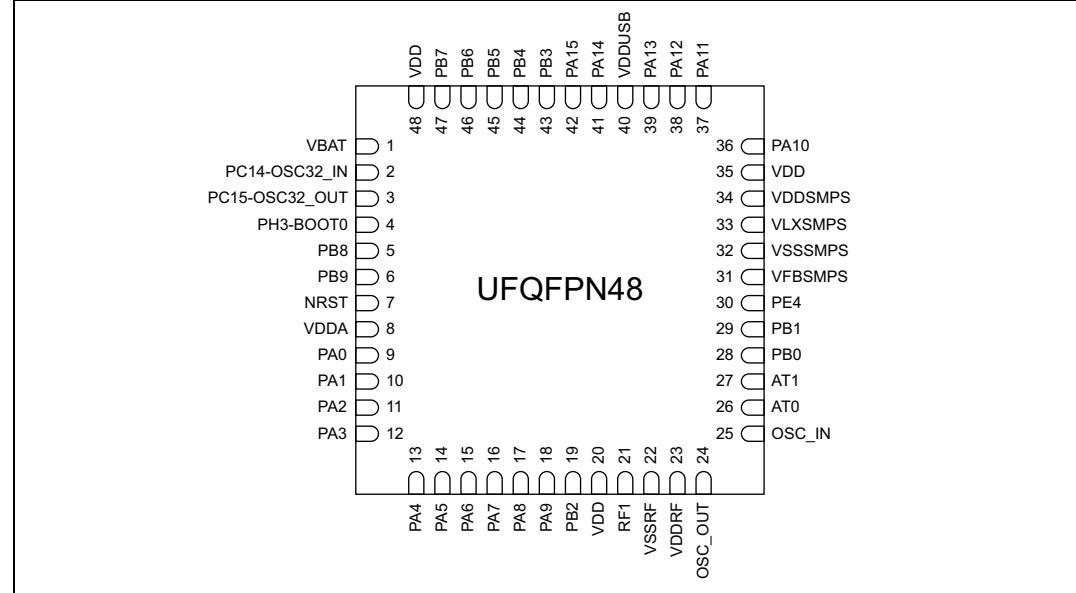
Figure 10. STM32WB55Cx and STM32WB35Cx UFQFPN48 pinout⁽¹⁾⁽²⁾

1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

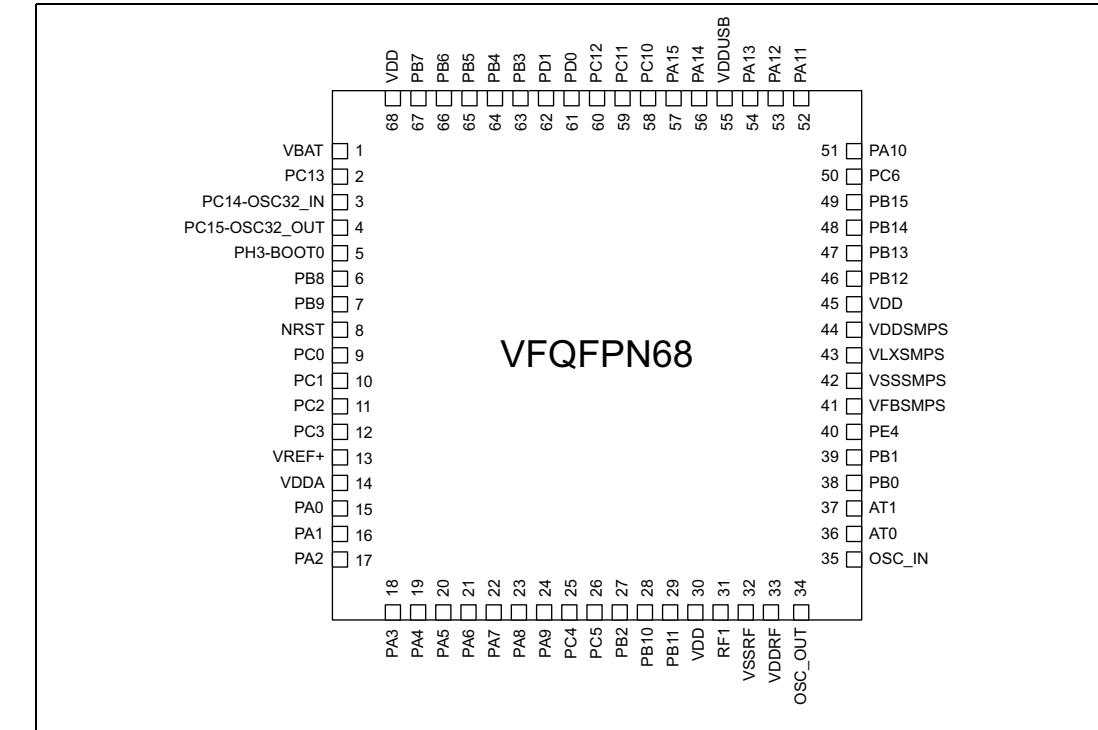
Figure 11. STM32WB55Rx VFQFPN68 pinout⁽¹⁾⁽²⁾

1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

4 引脚布局和引脚描述

图10. STM32WB55Cx 和 STM32WB35Cx UFQFPN48 引脚排列⁽¹⁾⁽²⁾

1. 上图显示封装顶视。2. 暴露的铜箔必须连接到地平面。

Figure 11. STM32WB55Rx VFQFPN68 引脚排列⁽¹⁾⁽²⁾

1. 上图显示封装顶视。2. 暴露的铜箔必须连接到地平面。

Figure 12. STM32WB55Vx WLCSP100 ballout⁽¹⁾

	1	2	3	4	5	6	7	8	9	10
A	PA11	PA12	PA14	PA15	PA13	PC10	PD2	PD7	PB3	VDD
B	VDD	VSS	VDDUSB	PC9	PA10	PC11	PD5	PD12	VSS	PE1
C	PB13	PD3	PD1	PD0	PC12	PD6	PB4	PE0	PD13	VBAT
D	VDDSMPS	PC6	PD4	PD8	PD9	PB5	PB7	PD14	PC15-OSC32_OUT	PC14-OSC32_IN
E	VLXSMPS	PB14	PC7	PD10	PD11	PE2	PD15	PH3-BOOT0	PH1	PH0
F	VSSSMPS	VFBSMPS	PB15	PC8	PB6	PA2	PB8	PC0	NRST	PB9
G	PE4	PE3	PB12	PC4	PC13	PA1	PA0	PC1	PC2	PC3
H	PB1	PB0	AT0	AT1	PC5	PA7	PA6	VREF+	VDDA	VSSA
J	OSC_IN	OSC_OUT	VDDRF	VSSRF	VSS	PB11	PA8	PA3	VSS	VDD
K	VSSRF	VSSRF	VSSRF	RF1	VDD	PB10	PB2	PA9	PA5	PA4

Radio USB SMPS VDD VSS

MS42407V3

- The above figure shows the package top view.

Figure 13. STM32WB55Vx UFBGA129 ballout⁽¹⁾

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PE1	PB6	PB5	X	X	PD5	PD10	VDD_DCAP4	X	X	PA13	VDDUSB	PA12
B	PE2	PE0	PB4	PD12	PD11	PD8	PD2	VSS_DCAP4	PC10	PC12	PD0	VSS	PA11
C	PD13	PD15	PB7	PB3	PD7	PD4	PD1	PC11	PA15	PA14	VSS	PA10	PC9
D	X	X	VBAT	PD14	PD9	X	X	PD6	X	X	PC6	PC8	PC7
E	X	X	PC15-OSC32_OUT	PC14-OSC32_IN	X	X	X	VSS	X	X	PB14	PB13	X
F	PH0	VDD_DCAP1	VSS_DCAP1	PC13	VDD	VDD	VDD	PB15	VLXSMPS	VDDSMPS	VDDSMPS		
G	PH3-BOOT0	PH1	PB8	X	X	VSS	X	X	VLXSMPS	VSSSMPS	VSSSMPS		
H	PC1	NRST	PC0	PB9	X	VDD	VDD	PB12	VFBSMPS	PE3	PE4		
J	X	X	PC2	PC3	X	VSS	X	X	VSS_DCAP3	VDD_DCAP3	X		
K	X	X	VSSA	VDDA	VSS	X	X	VSSRF	AT0	AT1	X		
L	VREF+	PA1	PA4	PA9	PC5	PB10	VSSRF	VSSRF	VSSRF	PB1	PB0		
M	PA0	PA3	PA6	PA8	PC4	PB11	VSS_DCAP2	VSSRF	RF1	VSSRF	VSSRF	OSC_IN	
N	PA2	PA5	PA7	X	X	PB2	VDD_DCAP2	VSSRF	X	X	VSSRF	VDDRF	OSC_OUT

No pin Power supply SMPS USB Radio

- The above figure shows the package top view.

图12. STM32WB55Vx WLCSP100 ballout⁽¹⁾

	1	2	3	4	5	6	7	8	9	10
A	PA11	PA12	PA14	PA15	PA13	PC10	PD2	PD7	PB3	VDD
B	VDD	VSS	VDDUSB	PC9	PA10	PC11	PD5	PD12	VSS	PE1
C	PB13	PD3	PD1	PD0	PC12	PD6	PB4	PE0	PD13	VBAT
D	VDDSMPS	PC6	PD4	PD8	PD9	PB5	PB7	PD14	PC15-OSC32_OUT	PC14-OSC32_IN
E	VLXSMPS	PB14	PC7	PD10	PD11	PE2	PD15	PH3-BOOT0	PH1	PH0
F	VSSSMPS	VFBSMPS	PB15	PC8	PB6	PA2	PB8	PC0	NRST	PB9
G	PE4	PE3	PB12	PC4	PC13	PA1	PA0	PC1	PC2	PC3
H	PB1	PB0	AT0	AT1	PC5	PA7	PA6	VREF+	VDDA	VSSA
J	OSC_IN	OSC_OUT	VDDRF	VSSRF	VSS	PB11	PA8	PA3	VSS	VDD
K	VSSRF	VSSRF	VSSRF	RF1	VDD	PB10	PB2	PA9	PA5	PA4

Radio USB SMPS VDD VSS

MS42407V3

- The above figure shows the package top view.

图13. STM32WB55Vx UFBGA129 球阵排列⁽¹⁾

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PE1	PB6	PB5	X	X	PD5	PD10	VDD_DCAP4	X	X	PA13	VDDUSB	PA12
B	PE2	PE0	PB4	PD12	PD11	PD8	PD2	VSS_DCAP4	PC10	PC12	PD0	VSS	PA11
C	PD13	PD15	PB7	PB3	PD7	PD4	PD1	PC11	PA15	PA14	VSS	PA10	PC9
D	X	X	VBAT	PD14	PD9	X	X	PD6	X	X	PC6	PC8	PC7
E	X	X	PC15-OSC32_OUT	PC14-OSC32_IN	X	X	X	VSS	X	X	PB14	PB13	X
F	PH0	VDD_DCAP1	VSS_DCAP1	PC13	VDD	VDD	VDD	PB15	VLXSMPS	VDDSMPS	VDDSMPS		
G	PH3-BOOT0	PH1	PB8	X	X	VSS	X	X	VLXSMPS	VSSSMPS	VSSSMPS		
H	PC1	NRST	PC0	PB9	X	VDD	VDD	PB12	VFBSMPS	PE3	PE4		
J	X	X	PC2	PC3	X	VSS	X	X	VSS_DCAP3	VDD_DCAP3	X		
K	X	X	VSSA	VDDA	VSS	X	X	VSSRF	AT0	AT1	X		
L	VREF+	PA1	PA4	PA9	PC5	PB10	VSSRF	VSSRF	VSSRF	PB1	PB0		
M	PA0	PA3	PA6	PA8	PC4	PB11	VSS_DCAP2	VSSRF	RF1	VSSRF	VSSRF	OSC_IN	
N	PA2	PA5	PA7	X	X	PB2	VDD_DCAP2	VSSRF	X	X	VSSRF	VDDRF	OSC_OUT

No pin Power supply SMPS USB Radio

- 上述图显示封装顶视。

Table 15. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TT	3.6 V tolerant I/O
	RF	RF I/O
	RST	Bidirectional reset pin with weak pull-up resistor
	Option for TT or FT I/Os	
	_f ⁽¹⁾	I/O, Fm+ capable
	l ⁽²⁾	I/O, with LCD function supplied by V{LCD}
	u ⁽³⁾	I/O, with USB function supplied by V{DDUSB}
	a ^{(4) (5)}	I/O, with Analog switch function supplied by V{DDA}
Notes	Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers
	Additional functions	Functions directly selected/enabled through peripheral registers

1. The related I/O structures in [Table 16](#) are: FT_f, FT_fa, FT_fl, FT_fla.
2. The related I/O structures in [Table 16](#) are: FT_l, FT_fl, FT_lu.
3. The related I/O structures in [Table 16](#) are: FT_u, FT_lu.
4. The related I/O structures in [Table 16](#) are: FT_a, FT_la, FT_fa, FT_fla, TT_a, TT_la.
5. Analog switch for the TSC function is supplied by V_{DD} .

表15. 在引脚表中使用的图例/缩写

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TT	3.6 V tolerant I/O
	RF	RF I/O
	RST	Bidirectional reset pin with weak pull-up resistor
	Option for TT or FT I/Os	
	_f ⁽¹⁾	I/O, Fm+ capable
	l ⁽²⁾	I/O, with LCD function supplied by V{LCD}
	u ⁽³⁾	I/O, with USB function supplied by V{DDUSB}
	a ^{(4) (5)}	I/O, with Analog switch function supplied by V{DDA}
Notes	Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers
	Additional functions	Functions directly selected/enabled through peripheral registers

1. The related I/O structures in [Table 16](#) are: FT_f, FT_fa, FT_fl, FT_fla.
2. The related I/O structures in [Table 16](#) are: FT_l, FT_fl, FT_lu.
3. The related I/O structures in [Table 16](#) are: FT_u, FT_lu.
4. The related I/O structures in [Table 16](#) are: FT_a, FT_la, FT_fa, FT_fla, TT_a, TT_la.
5. Analog switch for the TSC function is supplied by V_{DD} .

Table 16. STM32WB55xx pin and ball definitions

Pin number		Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68						
-	-	C8	B2	PE0	I/O	FT_I	-
						TIM1_ETR, TSC_G7_IO3, LCD SEG36, TIM16_CH1, CM4_EVENTOUT	-
-	-	B10	A1	PE1	I/O	FT_I	-
						TSC_G7_IO2, LCD SEG37, TIM17_CH1, CM4_EVENTOUT	-
-	-	E6	B1	PE2	I/O	FT_I	-
						TRACECK, SAI1_PDM_CK1, TSC_G7_IO1, LCD SEG38, SAI1_MCLK_A, CM4_EVENTOUT	-
-	-	C9	C1	PD13	I/O	FT_I	-
						TSC_G6_IO4, LCD SEG33, LPTIM2_OUT, CM4_EVENTOUT	-
-	-	D8	D3	PD14	I/O	FT_I	-
						TIM1_CH1, LCD SEG34, CM4_EVENTOUT	-
-	-	E7	C2	PD15	I/O	FT_I	-
						TIM1_CH2, LCD SEG35, CM4_EVENTOUT	-
1	1	C10	D2	VBAT	S	-	-
							-
-	2	G5	F4	PC13	I/O	FT	(1) (2) CM4_EVENTOUT
							RTC_TAMP1/RTC_TS/ RTC_OUT/WKUP2
2	3	D10	E3	PC14- OSC32_IN	I/O	FT	(1) (2) CM4_EVENTOUT
							OSC32_IN
3	4	D9	E2	PC15- OSC32_OUT	I/O	FT	(1) (2) CM4_EVENTOUT
							OSC32_OUT
-	-	-	E5	VSS	S	-	-
							-
-	-	-	F6	VDD	S	-	-
							-
-	-	E10	F1	PH0	I/O	FT	-
						CM4_EVENTOUT	-
-	-	E9	G2	PH1	I/O	FT	-
						CM4_EVENTOUT	-
4	5	E8	G1	PH3-BOOT0	I/O	FT	-
						CM4_EVENTOUT, LSCO ⁽³⁾	-
5	6	F7	G3	PB8	I/O	FT_fl	-
						TIM1_CH2N, SAI1_PDM_CK1, I2C1_SCL, QUADSPI_BK1_IO1, LCD SEG16, SAI1_MCLK_A, TIM16_CH1, CM4_EVENTOUT	-

表16. STM32WB55xx 引脚和球定义

Pin number		Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68						
-	-	C8	B2	PE0	I/O	FT_I	-
						TIM1_ETR, TSC_G7_IO3, LCD SEG36, TIM16_CH1, CM4_EVENTOUT	-
-	-	B10	A1	PE1	I/O	FT_I	-
						TSC_G7_IO2, LCD SEG37, TIM17_CH1, CM4_EVENTOUT	-
-	-	E6	B1	PE2	I/O	FT_I	-
						TRACECK, SAI1_PDM_CK1, TSC_G7_IO1, LCD SEG38, SAI1_MCLK_A, CM4_EVENTOUT	-
-	-	C9	C1	PD13	I/O	FT_I	-
						TSC_G6_IO4, LCD SEG33, LPTIM2_OUT, CM4_EVENTOUT	-
-	-	D8	D3	PD14	I/O	FT_I	-
						TIM1_CH1, LCD SEG34, CM4_EVENTOUT	-
-	-	E7	C2	PD15	I/O	FT_I	-
						TIM1_CH2, LCD SEG35, CM4_EVENTOUT	-
1	1	C10	D2	VBAT	S	-	-
							-
-	2	G5	F4	PC13	I/O	FT	(1) (2) CM4_EVENTOUT
							RTC_TAMP1/RTC_TS/ RTC_OUT/WKUP2
2	3	D10	E3	PC14- OSC32_IN	I/O	FT	(1) (2) CM4_EVENTOUT
							OSC32_IN
3	4	D9	E2	PC15- OSC32_OUT	I/O	FT	(1) (2) CM4_EVENTOUT
							OSC32_OUT
-	-	-	E5	VSS	S	-	-
							-
-	-	-	F6	VDD	S	-	-
							-
-	-	E10	F1	PH0	I/O	FT	-
						CM4_EVENTOUT	-
-	-	E9	G2	PH1	I/O	FT	-
						CM4_EVENTOUT	-
4	5	E8	G1	PH3-BOOT0	I/O	FT	-
						CM4_EVENTOUT, LSCO ⁽³⁾	-
5	6	F7	G3	PB8	I/O	FT_fl	-
						TIM1_CH2N, SAI1_PDM_CK1, I2C1_SCL, QUADSPI_BK1_IO1, LCD SEG16, SAI1_MCLK_A, TIM16_CH1, CM4_EVENTOUT	-

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VQFPN68	WL CSP100	UFBGA129						
6	7	F10	H4	PB9	I/O	FT_fla	-	TIM1_CH3N, SAI1_PDM_DI2, I2C1_SDA, SPI2_NSS, IR_OUT, TSC_G7_IO4, QUADSPI_BK1_IO0, LCD_COM3, SAI1_FS_A, TIM17_CH1, CM4_EVENTOUT	-
7	8	F9	H2	NRST	I/O	RST	-	-	-
-	9	F8	H3	PC0	I/O	FT_fla	-	LPTIM1_IN1, I2C3_SCL, LPUART1_RX, LCD_SEG18, LPTIM2_IN1, CM4_EVENTOUT	ADC1_IN1
-	10	G8	H1	PC1	I/O	FT_fla	-	LPTIM1_OUT, SPI2_MOSI, I2C3_SDA, LPUART1_TX, LCD_SEG19, CM4_EVENTOUT	ADC1_IN2
-	11	G9	J2	PC2	I/O	FT_la	-	LPTIM1_IN2, SPI2_MISO, LCD_SEG20, CM4_EVENTOUT	ADC1_IN3
-	-	-	E7	VSS	S	-	-	-	-
-	-	-	H6	VDD	S	-	-	-	-
-	12	G10	J3	PC3	I/O	FT_a	-	LPTIM1_ETR, SAI1_PDM_DI1, SPI2_MOSI, LCD_VLCD, SAI1_SD_A, LPTIM2_ETR, CM4_EVENTOUT	ADC1_IN4
-	-	H10	K2	VSSA	S	-	-	-	-
-	13	H8	L1	VREF+	S	-	-	-	VREFBUF_OUT
8	14	H9	K3	VDDA	S	-	(4)	-	-
-	-	J9	E9	VSS	S	-	-	-	-
-	-	J10	F8	VDD	S	-	-	-	-
9	15	G7	M1	PA0	I/O	FT_a	-	TIM2_CH1, COMP1_OUT, SAI1_EXTCLK, TIM2_ETR, CM4_EVENTOUT	COMP1_INM, ADC1_IN5, RTC_TAMP2/WKUP1
10	16	G6	L2	PA1	I/O	FT_la	-	TIM2_CH2, I2C1_SMBA, SPI1_SCK, LCD_SEG0, CM4_EVENTOUT	COMP1_INP, ADC1_IN6

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VQFPN68	WL CSP100	UFBGA129						
6	7	F10	H4	PB9	I/O	FT_fla	-	TIM1_CH3N, SAI1_PDM_DI2, I2C1_SDA, SPI2_NSS, IR_OUT, TSC_G7_IO4, QUADSPI_BK1_IO0, LCD_COM3, SAI1_FS_A, TIM17_CH1, CM4_EVENTOUT	-
7	8	F9	H2	NRST	I/O	RST	-	-	-
-	9	F8	H3	PC0	I/O	FT_fla	-	LPTIM1_IN1, I2C3_SCL, LPUART1_RX, LCD_SEG18, LPTIM2_IN1, CM4_EVENTOUT	ADC1_IN1
-	10	G8	H1	PC1	I/O	FT_fla	-	LPTIM1_OUT, SPI2_MOSI, I2C3_SDA, LPUART1_TX, LCD_SEG19, CM4_EVENTOUT	ADC1_IN2
-	11	G9	J2	PC2	I/O	FT_la	-	LPTIM1_IN2, SPI2_MISO, LCD_SEG20, CM4_EVENTOUT	ADC1_IN3
-	-	-	E7	VSS	S	-	-	-	-
-	-	-	H6	VDD	S	-	-	-	-
-	12	G10	J3	PC3	I/O	FT_a	-	LPTIM1_ETR, SAI1_PDM_DI1, SPI2_MOSI, LCD_VLCD, SAI1_SD_A, LPTIM2_ETR, CM4_EVENTOUT	ADC1_IN4
-	-	H10	K2	VSSA	S	-	-	-	-
-	13	H8	L1	VREF+	S	-	-	-	VREFBUF_OUT
8	14	H9	K3	VDDA	S	-	(4)	-	-
-	-	J9	E9	VSS	S	-	-	-	-
-	-	J10	F8	VDD	S	-	-	-	-
9	15	G7	M1	PA0	I/O	FT_a	-	TIM2_CH1, COMP1_OUT, SAI1_EXTCLK, TIM2_ETR, CM4_EVENTOUT	COMP1_INM, ADC1_IN5, RTC_TAMP2/WKUP1
10	16	G6	L2	PA1	I/O	FT_la	-	TIM2_CH2, I2C1_SMBA, SPI1_SCK, LCD_SEG0, CM4_EVENTOUT	COMP1_INP, ADC1_IN6

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VQFPN68	WLCSP100	UFBGA129						
11	17	F6	N1	PA2	I/O	FT_Ia	-	LSCO ⁽³⁾ , TIM2_CH3, LPUART1_TX, QUADSPI_BK1_NCS, LCD SEG1, COMP2_OUT, CM4_EVENTOUT	COMP2_INM, ADC1_IN7, WKUP4
12	18	J8	M2	PA3	I/O	FT_Ia	-	TIM2_CH4, SAI1_PDM_CK1, LPUART1_RX, QUADSPI_CLK, LCD SEG2, SAI1_MCLK_A, CM4_EVENTOUT	COMP2_INP, ADC1_IN8
13	19	K10	L3	PA4	I/O	FT_a	-	SPI1 NSS, SAI1_FS_B, LPTIM2_OUT, LCD SEG5, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN9
14	20	K9	N2	PA5	I/O	FT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, LPTIM2_ETR, SAI1_SD_B, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN10
15	21	H7	M3	PA6	I/O	FT_Ia	-	TIM1_BKIN, SPI1_MISO, LPUART1_CTS, QUADSPI_BK1_IO3, LCD SEG3, TIM16_CH1, CM4_EVENTOUT	ADC1_IN11
16	22	H6	N3	PA7	I/O	FT_fla	-	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, LCD SEG4, COMP2_OUT, TIM17_CH1, CM4_EVENTOUT	ADC1_IN12
17	23	J7	M4	PA8	I/O	FT_Ia	-	MCO, TIM1_CH1, SAI1_PDM_CK2, USART1_CK, LCD_COM0, SAI1_SCK_A, LPTIM2_OUT, CM4_EVENTOUT	ADC1_IN15
18	24	K8	L4	PA9	I/O	FT_fla	-	TIM1_CH2, SAI1_PDM_DI2, I2C1_SCL, SPI2_SCK, USART1_TX, LCD_COM1, SAI1_FS_A, CM4_EVENTOUT	COMP1_INM, ADC1_IN16
-	25	G4	M5	PC4	I/O	FT_Ia	-	LCD SEG22, CM4_EVENTOUT	COMP1_INM, ADC1_IN13
-	-	-	F3	VSS_DCAP1	S	-	-	-	-
-	-	-	G7	VDD	S	-	-	-	-

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VQFPN68	WLCSP100	UFBGA129						
11	17	F6	N1	PA2	I/O	FT_Ia	-	LSCO ⁽³⁾ , TIM2_CH3, LPUART1_TX, QUADSPI_BK1_NCS, LCD SEG1, COMP2_OUT, CM4_EVENTOUT	COMP2_INM, ADC1_IN7, WKUP4
12	18	J8	M2	PA3	I/O	FT_Ia	-	TIM2_CH4, SAI1_PDM_CK1, LPUART1_RX, QUADSPI_CLK, LCD SEG2, SAI1_MCLK_A, CM4_EVENTOUT	COMP2_INP, ADC1_IN8
13	19	K10	L3	PA4	I/O	FT_a	-	SPI1 NSS, SAI1_FS_B, LPTIM2_OUT, LCD SEG5, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN9
14	20	K9	N2	PA5	I/O	FT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, LPTIM2_ETR, SAI1_SD_B, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN10
15	21	H7	M3	PA6	I/O	FT_Ia	-	TIM1_BKIN, SPI1_MISO, LPUART1_CTS, QUADSPI_BK1_IO3, LCD SEG3, TIM16_CH1, CM4_EVENTOUT	ADC1_IN11
16	22	H6	N3	PA7	I/O	FT_fla	-	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, LCD SEG4, COMP2_OUT, TIM17_CH1, CM4_EVENTOUT	ADC1_IN12
17	23	J7	M4	PA8	I/O	FT_Ia	-	MCO, TIM1_CH1, SAI1_PDM_CK2, USART1_CK, LCD_COM0, SAI1_SCK_A, LPTIM2_OUT, CM4_EVENTOUT	ADC1_IN15
18	24	K8	L4	PA9	I/O	FT_fla	-	TIM1_CH2, SAI1_PDM_DI2, I2C1_SCL, SPI2_SCK, USART1_TX, LCD_COM1, SAI1_FS_A, CM4_EVENTOUT	COMP1_INM, ADC1_IN16
-	25	G4	M5	PC4	I/O	FT_Ia	-	LCD SEG22, CM4_EVENTOUT	COMP1_INM, ADC1_IN13
-	-	-	F3	VSS_DCAP1	S	-	-	-	-
-	-	-	G7	VDD	S	-	-	-	-

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
-	26	H5	L5	PC5	I/O	FT_Ia	-	SAI1_PDM_DI3, LCD SEG23, CM4_EVENTOUT	COMP1_INP, ADC1_IN14, WKUP5
19	27	K7	N6	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, SPI1_NSS, LCD_VLCD, SAI1_EXTCLK, CM4_EVENTOUT	COMP1_INP
-	28	K6	L6	PB10	I/O	FT_fl	-	TIM2_CH3, I2C3_SCL, SPI2_SCK, LPUART1_RX, TSC_SYNC, QUADSPI_CLK, LCD_SEG10, COMP1_OUT, SAI1_SCK_A, CM4_EVENTOUT	-
-	29	J6	M6	PB11	I/O	FT_fl	-	TIM2_CH4, I2C3_SDA, LPUART1_TX, QUADSPI_BK1_NCS, LCD_SEG11, COMP2_OUT, CM4_EVENTOUT	-
-	-	-	G5	VSS	S	-	-	-	-
-	-	-	G9	VSS	S	-	-	-	-
20	30	K5	H8	VDD	S	-	-	-	-
-	-	-	N8	VSSRF	S	-	-	-	-
-	-	-	J4	VSSRF	S	-	-	-	-
-	-	-	L8	VSSRF	S	-	-	-	-
-	-	-	M8	VSSRF	S	-	-	-	-
21	31	K4	M9	RF1	I/O	RF	(5)	-	-
22	32	K3	M10	VSSRF	S	-	-	-	-
-	-	K2	M11	VSSRF	S	-	-	-	-
-	-	-	K8	VSSRF	S	-	-	-	-
-	-	-	L9	VSSRF	S	-	-	-	-
-	-	-	L10	VSSRF	S	-	-	-	-
-	-	-	N11	VSSRF	S	-	-	-	-
23	33	J3	N12	VDDRF	S	-	-	-	-
-	-	K1	K10	VSSRF	S	-	-	-	-
-	-	-	M12	VSSRF	S	-	-	-	-
24	34	J2	N13	OSC_OUT	O	RF	(6)	-	-

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
-	26	H5	L5	PC5	I/O	FT_Ia	-	SAI1_PDM_DI3, LCD SEG23, CM4_EVENTOUT	COMP1_INP, ADC1_IN14, WKUP5
19	27	K7	N6	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, SPI1_NSS, LCD_VLCD, SAI1_EXTCLK, CM4_EVENTOUT	COMP1_INP
-	28	K6	L6	PB10	I/O	FT_fl	-	TIM2_CH3, I2C3_SCL, SPI2_SCK, LPUART1_RX, TSC_SYNC, QUADSPI_CLK, LCD_SEG10, COMP1_OUT, SAI1_SCK_A, CM4_EVENTOUT	-
-	29	J6	M6	PB11	I/O	FT_fl	-	TIM2_CH4, I2C3_SDA, LPUART1_TX, QUADSPI_BK1_NCS, LCD_SEG11, COMP2_OUT, CM4_EVENTOUT	-
-	-	-	G5	VSS	S	-	-	-	-
-	-	-	G9	VSS	S	-	-	-	-
20	30	K5	H8	VDD	S	-	-	-	-
-	-	-	N8	VSSRF	S	-	-	-	-
-	-	-	J4	VSSRF	S	-	-	-	-
-	-	-	L8	VSSRF	S	-	-	-	-
-	-	-	M8	VSSRF	S	-	-	-	-
21	31	K4	M9	RF1	I/O	RF	(5)	-	-
22	32	K3	M10	VSSRF	S	-	-	-	-
-	-	K2	M11	VSSRF	S	-	-	-	-
-	-	-	K8	VSSRF	S	-	-	-	-
-	-	-	L9	VSSRF	S	-	-	-	-
-	-	-	L10	VSSRF	S	-	-	-	-
-	-	-	N11	VSSRF	S	-	-	-	-
23	33	J3	N12	VDDRF	S	-	-	-	-
-	-	K1	K10	VSSRF	S	-	-	-	-
-	-	-	M12	VSSRF	S	-	-	-	-
24	34	J2	N13	OSC_OUT	O	RF	(6)	-	-

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number		Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions		
UFQFPN48	VFQFPN68								
25	35	J1	M13	OSC_IN	I	RF	(6)	-	-
-	-	-	L11	VSSRF	S	-	-	-	-
26	36	H3	K11	AT0	O	RF	(7)	-	-
27	37	H4	K12	AT1	O	RF	(7)	-	-
28	38	H2	L13	PB0	I/O	TT	(8)	COMP1_OUT, CM4_EVENTOUT, RF_TX_MOD_EXT_PA	-
29	39	H1	L12	PB1	I/O	TT	(8)	LPUART1_RTS_DE, LPTIM2_IN1, CM4_EVENTOUT	-
-	-	J5	-	VSS	S	-	-	-	-
-	-	-	M7	VSS_DCAP2	S	-	-	-	-
-	-	G2	H12	PE3	I/O	FT	-	CM4_EVENTOUT	-
30	40	G1	H13	PE4	I/O	FT	-	CM4_EVENTOUT	-
31	41	F2	H11	VFBSMPS	S	-	-	-	-
-	-	-	G13	VSSSMPS	S	-	-	-	-
32	42	F1	G12	VSSSMPS	S	-	-	-	-
33	43	E1	F11	VLXSMPS	S	-	-	-	-
-	-	-	G11	VLXSMPS	S	-	-	-	-
34	44	D1	F12	VDDSMPS	S	-	-	-	-
-	-	-	F13	VDDSMPS	S	-	-	-	-
-	-	-	K4	VSS	S	-	-	-	-
35	45	B1	-	VDD	S	-	-	-	-
-	46	G3	H10	PB12	I/O	FT_I	-	TIM1_BKIN, I2C3_SMBA, SPI2_NSS, LPUART1_RTS, TSC_G1_IO1, LCD_SEG12, SAI1_FS_A, CM4_EVENTOUT	-
-	47	C1	E12	PB13	I/O	FT_fI	-	TIM1_CH1N, I2C3_SCL, SPI2_SCK, LPUART1_CTS, TSC_G1_IO2, LCD_SEG13, SAI1_SCK_A, CM4_EVENTOUT	-

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number		Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions		
UFQFPN48	VFQFPN68								
25	35	J1	M13	OSC_IN	I	RF	(6)	-	-
-	-	-	L11	VSSRF	S	-	-	-	-
26	36	H3	K11	AT0	O	RF	(7)	-	-
27	37	H4	K12	AT1	O	RF	(7)	-	-
28	38	H2	L13	PB0	I/O	TT	(8)	COMP1_OUT, CM4_EVENTOUT, RF_TX_MOD_EXT_PA	-
29	39	H1	L12	PB1	I/O	TT	(8)	LPUART1_RTS_DE, LPTIM2_IN1, CM4_EVENTOUT	-
-	-	J5	-	VSS	S	-	-	-	-
-	-	-	M7	VSS_DCAP2	S	-	-	-	-
-	-	G2	H12	PE3	I/O	FT	-	CM4_EVENTOUT	-
30	40	G1	H13	PE4	I/O	FT	-	CM4_EVENTOUT	-
31	41	F2	H11	VFBSMPS	S	-	-	-	-
-	-	-	G13	VSSSMPS	S	-	-	-	-
32	42	F1	G12	VSSSMPS	S	-	-	-	-
33	43	E1	F11	VLXSMPS	S	-	-	-	-
-	-	-	G11	VLXSMPS	S	-	-	-	-
34	44	D1	F12	VDDSMPS	S	-	-	-	-
-	-	-	F13	VDDSMPS	S	-	-	-	-
-	-	-	K4	VSS	S	-	-	-	-
35	45	B1	-	VDD	S	-	-	-	-
-	46	G3	H10	PB12	I/O	FT_I	-	TIM1_BKIN, I2C3_SMBA, SPI2_NSS, LPUART1_RTS, TSC_G1_IO1, LCD_SEG12, SAI1_FS_A, CM4_EVENTOUT	-
-	47	C1	E12	PB13	I/O	FT_fI	-	TIM1_CH1N, I2C3_SCL, SPI2_SCK, LPUART1_CTS, TSC_G1_IO2, LCD_SEG13, SAI1_SCK_A, CM4_EVENTOUT	-

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
-	48	E2	E11	PB14	I/O	FT_fl	-	TIM1_CH2N, I2C3_SDA, SPI2_MISO, TSC_G1_IO3, LCD_SEG14, SAI1_MCLK_A, CM4_EVENTOUT	-
-	49	F3	F10	PB15	I/O	FT_l	-	RTC_REFIN, TIM1_CH3N, SPI2_MOSI, TSC_G1_IO4, LCD_SEG15, SAI1_SD_A, CM4_EVENTOUT	-
-	50	D2	D10	PC6	I/O	FT_l	-	TSC_G4_IO1, LCD_SEG24, CM4_EVENTOUT	-
-	-	E3	D12	PC7	I/O	FT_l	-	TSC_G4_IO2, LCD_SEG25, CM4_EVENTOUT	-
-	-	F4	D11	PC8	I/O	FT_l	-	TSC_G4_IO3, LCD_SEG26, CM4_EVENTOUT	-
-	-	B4	C13	PC9	I/O	FT_l	-	TIM1_BKIN, TSC_G4_IO4, USB_NOE, LCD_SEG27, SAI1_SCK_B, CM4_EVENTOUT	-
-	-	-	K6	VSS	S	-	-	-	-
-	-	B2	-	VSS	S	-	-	-	-
36	51	B5	C12	PA10	I/O	FT_fl	-	TIM1_CH3, SAI1_PDM_DI1, I2C1_SDA, USART1_RX, USB_CRS_SYNC, LCD_COM2, SAI1_SD_A, TIM17_BKIN, CM4_EVENTOUT	-
37	52	A1	B13	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS, USB_DM, CM4_EVENTOUT	-
38	53	A2	A13	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, LPUART1_RX, USART1_RTS_DE, USB_DP, CM4_EVENTOUT	-
39	54	A5	A11	PA13 (JTMS_SWDIO)	I/O	FT_u	(9)	JTMS-SWDIO, IR_OUT, USB_NOE, SAI1_SD_B, CM4_EVENTOUT	-
40	55	B3	A12	VDDUSB	S	-	-	-	-
-	-	-	C11	VSS	S	-	-	-	-

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
-	48	E2	E11	PB14	I/O	FT_fl	-	TIM1_CH2N, I2C3_SDA, SPI2_MISO, TSC_G1_IO3, LCD_SEG14, SAI1_MCLK_A, CM4_EVENTOUT	-
-	49	F3	F10	PB15	I/O	FT_l	-	RTC_REFIN, TIM1_CH3N, SPI2_MOSI, TSC_G1_IO4, LCD_SEG15, SAI1_SD_A, CM4_EVENTOUT	-
-	50	D2	D10	PC6	I/O	FT_l	-	TSC_G4_IO1, LCD_SEG24, CM4_EVENTOUT	-
-	-	E3	D12	PC7	I/O	FT_l	-	TSC_G4_IO2, LCD_SEG25, CM4_EVENTOUT	-
-	-	F4	D11	PC8	I/O	FT_l	-	TSC_G4_IO3, LCD_SEG26, CM4_EVENTOUT	-
-	-	B4	C13	PC9	I/O	FT_l	-	TIM1_BKIN, TSC_G4_IO4, USB_NOE, LCD_SEG27, SAI1_SCK_B, CM4_EVENTOUT	-
-	-	-	K6	VSS	S	-	-	-	-
-	-	B2	-	VSS	S	-	-	-	-
36	51	B5	C12	PA10	I/O	FT_fl	-	TIM1_CH3, SAI1_PDM_DI1, I2C1_SDA, USART1_RX, USB_CRS_SYNC, LCD_COM2, SAI1_SD_A, TIM17_BKIN, CM4_EVENTOUT	-
37	52	A1	B13	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS, USB_DM, CM4_EVENTOUT	-
38	53	A2	A13	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, LPUART1_RX, USART1_RTS_DE, USB_DP, CM4_EVENTOUT	-
39	54	A5	A11	PA13 (JTMS_SWDIO)	I/O	FT_u	(9)	JTMS-SWDIO, IR_OUT, USB_NOE, SAI1_SD_B, CM4_EVENTOUT	-
40	55	B3	A12	VDDUSB	S	-	-	-	-
-	-	-	C11	VSS	S	-	-	-	-

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WL CSP100	UF BGA129						
41	56	A3	C10	PA14 (JTCK_SWCLK)	I/O	FT_I	(9)	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, LCD SEG5, SAI1_FS_B, CM4_EVENTOUT	-
42	57	A4	C9	PA15 (JTDI)	I/O	FT_I	(9)	JTDI, TIM2_CH1, TIM2_ETR, SPI1 NSS, TSC_G3_IO1, LCD SEG17, CM4_EVENTOUT, MCO	-
-	-	-	J11	VSS_DCAP3	S	-	-	-	-
-	58	A6	B9	PC10	I/O	FT_I	-	TRACED1, TSC_G3_IO2, LCD COM4/LCD SEG28/ LCD SEG40, CM4_EVENTOUT	-
-	59	B6	C8	PC11	I/O	FT_I	-	TSC_G3_IO3, LCD COM5/LCD SEG29/ LCD SEG41, CM4_EVENTOUT	-
-	60	C5	B10	PC12	I/O	FT_I	-	LSCO ⁽³⁾ , TRACED3, TSC_G3_IO4, LCD COM6/LCD SEG30/ LCD SEG42, CM4_EVENTOUT	RTC_TAMP3/WKUP3
-	61	C4	B11	PD0	I/O	FT	-	SPI2 NSS, CM4_EVENTOUT	-
-	62	C3	C7	PD1	I/O	FT	-	SPI2_SCK, CM4_EVENTOUT	-
-	-	A7	B7	PD2	I/O	FT_I	-	TRACED2, TSC_SYNC, LCD COM7/LCD SEG31/LC D SEG43, CM4_EVENTOUT	-
-	-	C2	D8	PD3	I/O	FT	-	SPI2_SCK, SPI2_MISO, QUADSPI_BK1_NCS, CM4_EVENTOUT	-
-	-	D3	C6	PD4	I/O	FT	-	SPI2_MOSI, TSC_G5_IO1, QUADSPI_BK1_IO0, CM4_EVENTOUT	-
-	-	B7	A6	PD5	I/O	FT	-	TSC_G5_IO2, QUADSPI_BK1_IO1, SAI1_MCLK_B, CM4_EVENTOUT	-

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WL CSP100	UF BGA129						
41	56	A3	C10	PA14 (JTCK_SWCLK)	I/O	FT_I	(9)	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, LCD SEG5, SAI1_FS_B, CM4_EVENTOUT	-
42	57	A4	C9	PA15 (JTDI)	I/O	FT_I	(9)	JTDI, TIM2_CH1, TIM2_ETR, SPI1 NSS, TSC_G3_IO1, LCD SEG17, CM4_EVENTOUT, MCO	-
-	-	-	J11	VSS_DCAP3	S	-	-	-	-
-	58	A6	B9	PC10	I/O	FT_I	-	TRACED1, TSC_G3_IO2, LCD COM4/LCD SEG28/ LCD SEG40, CM4_EVENTOUT	-
-	59	B6	C8	PC11	I/O	FT_I	-	TSC_G3_IO3, LCD COM5/LCD SEG29/ LCD SEG41, CM4_EVENTOUT	-
-	60	C5	B10	PC12	I/O	FT_I	-	LSCO ⁽³⁾ , TRACED3, TSC_G3_IO4, LCD COM6/LCD SEG30/ LCD SEG42, CM4_EVENTOUT	RTC_TAMP3/WKUP3
-	61	C4	B11	PD0	I/O	FT	-	SPI2 NSS, CM4_EVENTOUT	-
-	62	C3	C7	PD1	I/O	FT	-	SPI2_SCK, CM4_EVENTOUT	-
-	-	A7	B7	PD2	I/O	FT_I	-	TRACED2, TSC_SYNC, LCD COM7/LCD SEG31/LC D SEG43, CM4_EVENTOUT	-
-	-	C2	D8	PD3	I/O	FT	-	SPI2_SCK, SPI2_MISO, QUADSPI_BK1_NCS, CM4_EVENTOUT	-
-	-	D3	C6	PD4	I/O	FT	-	SPI2_MOSI, TSC_G5_IO1, QUADSPI_BK1_IO0, CM4_EVENTOUT	-
-	-	B7	A6	PD5	I/O	FT	-	TSC_G5_IO2, QUADSPI_BK1_IO1, SAI1_MCLK_B, CM4_EVENTOUT	-

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WL CSP100	UF BGA129						
-	-	C6	D6	PD6	I/O	FT	-	SAI1_PDM_DI1, TSC_G5_IO3, QUADSPI_BK1_IO2, SAI1_SD_A, CM4_EVENTOUT	-
-	-	A8	C5	PD7	I/O	FT_I	-	TSC_G5_IO4, QUADSPI_BK1_IO3, LCD_SEG39, CM4_EVENTOUT	-
-	-	B9	B12	VSS	S	-	-	-	-
-	-	D4	B6	PD8	I/O	FT_I	-	TIM1_BKIN2, LCD_SEG28, CM4_EVENTOUT	-
-	-	D5	D4	PD9	I/O	FT_I	-	TRACED0, LCD_SEG29, CM4_EVENTOUT	-
-	-	E4	A7	PD10	I/O	FT_I	-	TRIG_INOUT, TSC_G6_IO1, LCD_SEG30, CM4_EVENTOUT	-
-	-	E5	B5	PD11	I/O	FT_I	-	TSC_G6_IO2, LCD_SEG31, LPTIM2_ETR, CM4_EVENTOUT	-
-	-	B8	B4	PD12	I/O	FT_I	-	TSC_G6_IO3, LCD_SEG32, LPTIM2_IN1, CM4_EVENTOUT	-
43	63	A9	C4	PB3 (JTDO)	I/O	FT_Ia	(9)	JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, USART1_RTS_DE, LCD_SEG7, SAI1_SCK_B, CM4_EVENTOUT	COMP2_INM
44	64	C7	B3	PB4 (NJTRST)	I/O	FT_fla	(9)	NJTRST, I2C3_SDA, SPI1_MISO, USART1_CTS, TSC_G2_IO1, LCD_SEG8, SAI1_MCLK_B, TIM17_BKIN, CM4_EVENTOUT	COMP2_INP
45	65	D6	A3	PB5	I/O	FT_I	-	LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, USART1_CK, LPUART1_TX, TSC_G2_IO2, LCD_SEG9, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, CM4_EVENTOUT	-

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WL CSP100	UF BGA129						
-	-	C6	D6	PD6	I/O	FT	-	SAI1_PDM_DI1, TSC_G5_IO3, QUADSPI_BK1_IO2, SAI1_SD_A, CM4_EVENTOUT	-
-	-	A8	C5	PD7	I/O	FT_I	-	TSC_G5_IO4, QUADSPI_BK1_IO3, LCD_SEG39, CM4_EVENTOUT	-
-	-	B9	B12	VSS	S	-	-	-	-
-	-	D4	B6	PD8	I/O	FT_I	-	TIM1_BKIN2, LCD_SEG28, CM4_EVENTOUT	-
-	-	D5	D4	PD9	I/O	FT_I	-	TRACED0, LCD_SEG29, CM4_EVENTOUT	-
-	-	E4	A7	PD10	I/O	FT_I	-	TRIG_INOUT, TSC_G6_IO1, LCD_SEG30, CM4_EVENTOUT	-
-	-	E5	B5	PD11	I/O	FT_I	-	TSC_G6_IO2, LCD_SEG31, LPTIM2_ETR, CM4_EVENTOUT	-
-	-	B8	B4	PD12	I/O	FT_I	-	TSC_G6_IO3, LCD_SEG32, LPTIM2_IN1, CM4_EVENTOUT	-
43	63	A9	C4	PB3 (JTDO)	I/O	FT_Ia	(9)	JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, USART1_RTS_DE, LCD_SEG7, SAI1_SCK_B, CM4_EVENTOUT	COMP2_INM
44	64	C7	B3	PB4 (NJTRST)	I/O	FT_fla	(9)	NJTRST, I2C3_SDA, SPI1_MISO, USART1_CTS, TSC_G2_IO1, LCD_SEG8, SAI1_MCLK_B, TIM17_BKIN, CM4_EVENTOUT	COMP2_INP
45	65	D6	A3	PB5	I/O	FT_I	-	LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, USART1_CK, LPUART1_TX, TSC_G2_IO2, LCD_SEG9, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, CM4_EVENTOUT	-

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WL CSP100	UF BGA129						
46	66	F5	A2	PB6	I/O	FT_fla	-	LPTIM1_ETR, I2C1_SCL, USART1_TX, TSC_G2_IO3, LCD SEG6, SAI1_FS_B, TIM16_CH1N, MCO, CM4_EVENTOUT	COMP2_INP
47	67	D7	C3	PB7	I/O	FT_fla	-	LPTIM1_IN2, TIM1_BKIN, I2C1_SDA, USART1_RX, TSC_G2_IO4, LCD SEG21, TIM17_CH1N, CM4_EVENTOUT	COMP2_INM, PVD_IN
-	-	-	J5	VSS	S	-	-	-	-
-	-	-	J7	VSS	S	-	-	-	-
-	-	-	J9	VSS	S	-	-	-	-
-	-	-	B8	VSS_DCAP4	S	-	-	-	-
48	68	A10	-	VDD	S	-	-	-	-
-	-	-	A8	VDD_DCAP4	S	-	-	-	-
-	-	-	F2	VDD_DCAP1	S	-	-	-	-
-	-	-	J12	VDD_DCAP3	S	-	-	-	-
-	-	-	N7	VDD_DCAP2	S	-	-	-	-

- PC13, PC14 and PC15 are supplied through the power switch. As this switch only sinks a limited amount of current (3 mA), the use of the PC13, PC14 and PC15 GPIOs in output mode is limited:
 - the speed must not exceed 2 MHz with a maximum load of 30 pF
 - these GPIOs must not be used as current sources (e.g. to drive a LED).
- After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers that are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the reference manual RM0434, available on www.st.com.
- The clock on LSCO is available in Run and Stop modes, and on PA2 in Standby and Shutdown modes.
- On UFQFPN48 VDDA is connected to VREF+.
- RF pin, use the nominal PCB layout.
- 32 MHz oscillator pins, use the nominal PCB layout according to reference design (see AN5165).
- Reserved, must be kept unconnected.
- High frequency (above 32 kHz) may impact the RF performance. Set output speed GPIOB_OSPEEDRy[1:0] to 00 (y = 0 and 1) during RF operation.
- After reset these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13 and PB4 pins and the internal pull-down on PA14 pin are activated.

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WL CSP100	UF BGA129						
46	66	F5	A2	PB6	I/O	FT_fla	-	LPTIM1_ETR, I2C1_SCL, USART1_TX, TSC_G2_IO3, LCD SEG6, SAI1_FS_B, TIM16_CH1N, MCO, CM4_EVENTOUT	COMP2_INP
47	67	D7	C3	PB7	I/O	FT_fla	-	LPTIM1_IN2, TIM1_BKIN, I2C1_SDA, USART1_RX, TSC_G2_IO4, LCD SEG21, TIM17_CH1N, CM4_EVENTOUT	COMP2_INM, PVD_IN
-	-	-	J5	VSS	S	-	-	-	-
-	-	-	J7	VSS	S	-	-	-	-
-	-	-	J9	VSS	S	-	-	-	-
-	-	-	B8	VSS_DCAP4	S	-	-	-	-
48	68	A10	-	VDD	S	-	-	-	-
-	-	-	A8	VDD_DCAP4	S	-	-	-	-
-	-	-	F2	VDD_DCAP1	S	-	-	-	-
-	-	-	J12	VDD_DCAP3	S	-	-	-	-
-	-	-	N7	VDD_DCAP2	S	-	-	-	-

- PC13, PC14 and PC15 are supplied through the power switch. As this switch only sinks a limited amount of current (3 mA), the use of the PC13, PC14 and PC15 GPIOs in output mode is limited:
 - the speed must not exceed 2 MHz with a maximum load of 30 pF
 - these GPIOs must not be used as current sources (e.g. to drive a LED).
- After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers that are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the reference manual RM0434, available on www.st.com.
- The clock on LSCO is available in Run and Stop modes, and on PA2 in Standby and Shutdown modes.
- On UFQFPN48 VDDA is connected to VREF+.
- RF引脚，使用标准PCB布局。
- 32 MHz 振荡器引脚，按照参考设计(see AN5165) 使用标准PCB布局。
- 保留，必须保持未连接。
- 高频(above 32 kHz)可能影响RF性能。Set output speed GPIOB_OSPEEDRy[1:0] to 00 (y = 0 and1) during RF operation.
- After reset these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13 and PB4 pins and the internal pull-down on PA14 pin are activated.

Table 17. STM32WB35xx pin and ball definitions

Pin		Pin type	I/O structures	Notes	Alternate functions	Additional functions
Number	Name (function after reset)					
1	VBAT	S	-	-	-	-
2	PC14-OSC32_IN	I/O	FT	(1) (2)	CM4_EVENTOUT	OSC32_IN
3	PC15-OSC32_OUT	I/O	FT	(1) (2)	CM4_EVENTOUT	OSC32_OUT
4	PH3-BOOT0	I/O	FT	-	CM4_EVENTOUT, LSCO ⁽³⁾	-
5	PB8	I/O	FT_f	-	TIM1_CH2N, SAI1_PDM_CK1, I2C1_SCL, QUADSPI_BK1_IO1, SAI1_MCLK_A, TIM16_CH1, CM4_EVENTOUT	-
6	PB9	I/O	FT_f	-	TIM1_CH3N, SAI1_PDM_DI2, I2C1_SDA, IR_OUT, QUADSPI_BK1_IO0, SAI1_FS_A, TIM17_CH1, CM4_EVENTOUT	-
7	NRST	I/O	RST	-	-	-
8	VDDA	S	-	-	-	-
9	PA0	I/O	FT_a	-	TIM2_CH1, COMP1_OUT, SAI1_EXTCLK, TIM2_ETR, CM4_EVENTOUT	COMP1_INM, ADC1_IN5, RTC_TAMP2/WKUP1
10	PA1	I/O	FT_a	-	TIM2_CH2, I2C1_SMBA, SPI1_SCK, CM4_EVENTOUT	COMP1_INP, ADC1_IN6
11	PA2	I/O	FT_a	-	LSCO ⁽³⁾ , TIM2_CH3, LPUART1_TX, QUADSPI_BK1_NCS, COMP2_OUT, CM4_EVENTOUT	COMP2_INM, ADC1_IN7, WKUP4
12	PA3	I/O	FT_a	-	TIM2_CH4, SAI1_PDM_CK1, LPUART1_RX, QUADSPI_CLK, SAI1_MCLK_A, CM4_EVENTOUT	COMP2_INP, ADC1_IN8
13	PA4	I/O	FT_a	-	SPI1 NSS, SAI1_FS_B, LPTIM2_OUT, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN9
14	PA5	I/O	FT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, LPTIM2_ETR, SAI1_SD_B, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN10
15	PA6	I/O	FT_a	-	TIM1_BKIN, SPI1_MISO, LPUART1_CTS, QUADSPI_BK1_IO3, TIM16_CH1, CM4_EVENTOUT	ADC1_IN11
16	PA7	I/O	FT_fa	-	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, COMP2_OUT, TIM17_CH1, CM4_EVENTOUT	ADC1_IN12
17	PA8	I/O	FT_a	-	MCO, TIM1_CH1, SAI1_PDM_CK2, USART1_CK, SAI1_SCK_A, LPTIM2_OUT, CM4_EVENTOUT	ADC1_IN15

表17. STM32WB35xx 引脚和球定义

Pin		Pin type	I/O structures	Notes	Alternate functions	Additional functions
Number	Name (function after reset)					
1	VBAT	S	-	-	-	-
2	PC14-OSC32_IN	I/O	FT	(1) (2)	CM4_EVENTOUT	OSC32_IN
3	PC15-OSC32_OUT	I/O	FT	(1) (2)	CM4_EVENTOUT	OSC32_OUT
4	PH3-BOOT0	I/O	FT	-	CM4_EVENTOUT, LSCO ⁽³⁾	-
5	PB8	I/O	FT_f	-	TIM1_CH2N, SAI1_PDM_CK1, I2C1_SCL, QUADSPI_BK1_IO1, SAI1_MCLK_A, TIM16_CH1, CM4_EVENTOUT	-
6	PB9	I/O	FT_f	-	TIM1_CH3N, SAI1_PDM_DI2, I2C1_SDA, IR_OUT, QUADSPI_BK1_IO0, SAI1_FS_A, TIM17_CH1, CM4_EVENTOUT	-
7	NRST	I/O	RST	-	-	-
8	VDDA	S	-	-	-	-
9	PA0	I/O	FT_a	-	TIM2_CH1, COMP1_OUT, SAI1_EXTCLK, TIM2_ETR, CM4_EVENTOUT	COMP1_INM, ADC1_IN5, RTC_TAMP2/WKUP1
10	PA1	I/O	FT_a	-	TIM2_CH2, I2C1_SMBA, SPI1_SCK, CM4_EVENTOUT	COMP1_INP, ADC1_IN6
11	PA2	I/O	FT_a	-	LSCO ⁽³⁾ , TIM2_CH3, LPUART1_TX, QUADSPI_BK1_NCS, COMP2_OUT, CM4_EVENTOUT	COMP2_INM, ADC1_IN7, WKUP4
12	PA3	I/O	FT_a	-	TIM2_CH4, SAI1_PDM_CK1, LPUART1_RX, QUADSPI_CLK, SAI1_MCLK_A, CM4_EVENTOUT	COMP2_INP, ADC1_IN8
13	PA4	I/O	FT_a	-	SPI1 NSS, SAI1_FS_B, LPTIM2_OUT, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN9
14	PA5	I/O	FT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, LPTIM2_ETR, SAI1_SD_B, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN10
15	PA6	I/O	FT_a	-	TIM1_BKIN, SPI1_MISO, LPUART1_CTS, QUADSPI_BK1_IO3, TIM16_CH1, CM4_EVENTOUT	ADC1_IN11
16	PA7	I/O	FT_fa	-	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, COMP2_OUT, TIM17_CH1, CM4_EVENTOUT	ADC1_IN12
17	PA8	I/O	FT_a	-	MCO, TIM1_CH1, SAI1_PDM_CK2, USART1_CK, SAI1_SCK_A, LPTIM2_OUT, CM4_EVENTOUT	ADC1_IN15

Table 17. STM32WB35xx pin and ball definitions (continued)

Pin		Pin type	I/O structures	Notes	Alternate functions	Additional functions
Number	Name (function after reset)					
18	PA9	I/O	FT_fa	-	TIM1_CH2, SAI1_PDM_DI2, I2C1_SCL, USART1_TX, SAI1_FS_A, CM4_EVENTOUT	COMP1_INM, ADC1_IN16
19	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, SPI1_NSS, SAI1_EXTCLK, CM4_EVENTOUT	COMP1_INP
20	VDD	S	-	-	-	-
21	RF1	I/O	RF	(4)	-	-
22	VSSRF	S	-	-	-	-
23	VDDRF	S	-	-	-	-
24	OSC_OUT	O	RF	(5)	-	-
25	OSC_IN	I	RF	(5)	-	-
26	AT0	O	RF	(6)	-	-
27	AT1	O	RF	(6)	-	-
28	PB0	I/O	TT	(7)	COMP1_OUT, CM4_EVENTOUT, RF_TX_MOD_EXT_PA	-
29	PB1	I/O	TT	(7)	LPUART1_RTS_DE, LPTIM2_IN1, CM4_EVENTOUT	-
30	PE4	I/O	FT	-	CM4_EVENTOUT	-
31	VFBSPS	S	-	-	-	-
32	VSSSPS	S	-	-	-	-
33	VLXSPS	S	-	-	-	-
34	VDDSPS	S	-	-	-	-
35	VDD	S	-	-	-	-
36	PA10	I/O	FT_f	-	TIM1_CH3, SAI1_PDM_DI1, I2C1_SDA, USART1_RX, USB_CRS_SYNC, SAI1_SD_A, TIM17_BKIN, CM4_EVENTOUT	-
37	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS, USB_DM, CM4_EVENTOUT	-
38	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, LPUART1_RX, USART1_RTS_DE, USB_DP, CM4_EVENTOUT	-
39	PA13 (JTMS-SWDIO)	I/O	FT	(8)	JTMS-SWDIO, IR_OUT, USB_NOE, SAI1_SD_B, CM4_EVENTOUT	-
40	VDDUSB	S	-	-	-	-

表17. STM32WB35xx 引脚和球定义 (继续)

Pin		Pin type	I/O structures	Notes	Alternate functions	Additional functions
Number	Name (function after reset)					
18	PA9	I/O	FT_fa	-	TIM1_CH2, SAI1_PDM_DI2, I2C1_SCL, USART1_TX, SAI1_FS_A, CM4_EVENTOUT	COMP1_INM, ADC1_IN16
19	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, SPI1_NSS, SAI1_EXTCLK, CM4_EVENTOUT	COMP1_INP
20	VDD	S	-	-	-	-
21	RF1	I/O	RF	(4)	-	-
22	VSSRF	S	-	-	-	-
23	VDDRF	S	-	-	-	-
24	OSC_OUT	O	RF	(5)	-	-
25	OSC_IN	I	RF	(5)	-	-
26	AT0	O	RF	(6)	-	-
27	AT1	O	RF	(6)	-	-
28	PB0	I/O	TT	(7)	COMP1_OUT, CM4_EVENTOUT, RF_TX_MOD_EXT_PA	-
29	PB1	I/O	TT	(7)	LPUART1_RTS_DE, LPTIM2_IN1, CM4_EVENTOUT	-
30	PE4	I/O	FT	-	CM4_EVENTOUT	-
31	VFBSPS	S	-	-	-	-
32	VSSSPS	S	-	-	-	-
33	VLXSPS	S	-	-	-	-
34	VDDSPS	S	-	-	-	-
35	VDD	S	-	-	-	-
36	PA10	I/O	FT_f	-	TIM1_CH3, SAI1_PDM_DI1, I2C1_SDA, USART1_RX, USB_CRS_SYNC, SAI1_SD_A, TIM17_BKIN, CM4_EVENTOUT	-
37	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS, USB_DM, CM4_EVENTOUT	-
38	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, LPUART1_RX, USART1_RTS_DE, USB_DP, CM4_EVENTOUT	-
39	PA13 (JTMS-SWDIO)	I/O	FT	(8)	JTMS-SWDIO, IR_OUT, USB_NOE, SAI1_SD_B, CM4_EVENTOUT	-
40	VDDUSB	S	-	-	-	-

Table 17. STM32WB35xx pin and ball definitions (continued)

Pin		Pin type	I/O structures	Notes	Alternate functions	Additional functions
Number	Name (function after reset)					
41	PA14 (JTCK-SWCLK)	I/O	FT	(8)	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, SAI1_FS_B, CM4_EVENTOUT	-
42	PA15 (JTDI)	I/O	FT	(8)	JTDI, TIM2_CH1, TIM2_ETR, SPI1 NSS, CM4_EVENTOUT, MCO	-
43	PB3 (JTDO)	I/O	FT_a	-	JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, USART1 RTS_DE, SAI1_SCK_B, CM4_EVENTOUT	COMP2_INM
44	PB4 (NJTRST)	I/O	FT_fa	(8)	NJTRST, I2C3_SDA, SPI1_MISO, USART1_CTS, SAI1_MCLK_B, TIM17_BKIN, CM4_EVENTOUT	COMP2_INP
45	PB5	I/O	FT_a	-	LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, USART1_CK, LPUART1_TX, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, CM4_EVENTOUT	-
46	PB6	I/O	FT_fa	-	LPTIM1_ETR, I2C1_SCL, USART1_TX, SAI1_FS_B, TIM16_CH1N, MCO, CM4_EVENTOUT	COMP2_INP
47	PB7	I/O	FT_fa	-	LPTIM1_IN2, TIM1_BKIN, I2C1_SDA, USART1_RX, TIM17_CH1N, CM4_EVENTOUT	COMP2_INM, PVD_IN
48	VDD	S	-	-	-	-

- PC14 and PC15 are supplied through the power switch. As this switch only sinks a limited amount of current (3 mA), the use of the PC14 and PC15 GPIOs in output mode is limited:
 - the speed must not exceed 2 MHz with a maximum load of 30 pF
 - these GPIOs must not be used as current sources (e.g. to drive a LED).
- After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers that are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the reference manual RM0434, available on www.st.com.
- The clock on LSCO is available in Run and Stop modes, and on PA2 in Standby and Shutdown modes.
- RF pin, use the nominal PCB layout.
- 32 MHz oscillator pins, use the nominal PCB layout according to reference design (see AN5165).
- Reserved, must be kept unconnected.
- High frequency (above 32 kHz) may impact the RF performance. Set output speed GPIOB_OSPEEDRy[1:0] to 00 (y = 0 and 1) during RF operation.
- After reset these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13 and PB4 pins and the internal pull-down on PA14 pin are activated.

表17. STM32WB35xx 引脚和球定义 (继续)

Pin		Pin type	I/O structures	Notes	Alternate functions	Additional functions
Number	Name (function after reset)					
41	PA14 (JTCK-SWCLK)	I/O	FT	(8)	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, SAI1_FS_B, CM4_EVENTOUT	-
42	PA15 (JTDI)	I/O	FT	(8)	JTDI, TIM2_CH1, TIM2_ETR, SPI1 NSS, CM4_EVENTOUT, MCO	-
43	PB3 (JTDO)	I/O	FT_a	-	JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, USART1 RTS_DE, SAI1_SCK_B, CM4_EVENTOUT	COMP2_INM
44	PB4 (NJTRST)	I/O	FT_fa	(8)	NJTRST, I2C3_SDA, SPI1_MISO, USART1_CTS, SAI1_MCLK_B, TIM17_BKIN, CM4_EVENTOUT	COMP2_INP
45	PB5	I/O	FT_a	-	LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, USART1_CK, LPUART1_TX, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, CM4_EVENTOUT	-
46	PB6	I/O	FT_fa	-	LPTIM1_ETR, I2C1_SCL, USART1_TX, SAI1_FS_B, TIM16_CH1N, MCO, CM4_EVENTOUT	COMP2_INP
47	PB7	I/O	FT_fa	-	LPTIM1_IN2, TIM1_BKIN, I2C1_SDA, USART1_RX, TIM17_CH1N, CM4_EVENTOUT	COMP2_INM, PVD_IN
48	VDD	S	-	-	-	-

- PC14 and PC15 are supplied through the power switch. As this switch only sinks a limited amount of current (3 mA), the use of the PC14 and PC15 GPIOs in output mode is limited:
 - the speed must not exceed 2 MHz with a maximum load of 30 pF
 - these GPIOs must not be used as current sources (e.g. to drive a LED).
- After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers that are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the reference manual RM0434, available on www.st.com.
- LSCO 上的时钟在运行模式和停止模式下可用，并且在待机模式和关闭模式下在 PA2 上可用。
- RF引脚，使用标准 PCB 布局。
- 32 MHz振荡器引脚，使用参考设计 (看 AN5165) 中的标准 PCB 布局。
- 保留，必须保持未连接。
- 高频 (超过 32 kHz) 可能会影响 RF 性能。在 RF 操作期间，将输出速度 GPIOB_OSPEEDRy[1:0] 设置为 00 (y = 0 和 1)。
- 复位后，这些引脚被配置为 JTAG/SW 调试替代功能，并且 PA15、PA13 和 PB4 引脚上的内部上拉以及 PA14 引脚上的内部下拉被激活。



Table 18. Alternate functions (STM32WB55xx)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
	SYS_AF	TIM1/TIM2/LPTIM1	TIM1/TIM2	SPI2/SAI1/TIM1	I2C1/I2C3	SPI1/SPI2	RF	USART1	LPUART1	TSC	USB/QUADSPI	LCD	COMP1/COMP2/TIM1	SAI1	TIM2/TIM16/TIM17/LPTIM2	EVENTOUT	
A	PA0	-	TIM2_CH1	-	-	-	-	-	-	-	-	COMP1_OUT	SAI1_EXTCLK	TIM2_ETR	CM4_EVENTOUT		
	PA1	-	TIM2_CH2	-	-	I2C1_SMB \bar{A}	SPI1_SCK	-	-	-	LCD_SEG0	-	-	-	-	CM4_EVENTOUT	
	PA2	LSCO	TIM2_CH3	-	-	-	-	-	LPUART1_TX	-	QUADSPI_BK1_NCS	LCD_SEG1	COMP2_OUT	-	-	CM4_EVENTOUT	
	PA3	-	TIM2_CH4	-	SAI1_PDM_CK1	-	-	-	LPUART1_RX	-	QUADSPI_CLK	LCD_SEG2	-	SAI1_MCLK_A	-	CM4_EVENTOUT	
	PA4	-	-	-	-	SPI1_NSS	-	-	-	-	LCD_SEG5	-	SAI1_FS_B	LPTIM2_OUT	-	CM4_EVENTOUT	
	PA5	-	TIM2_CH1	TIM2_ETR	-	SPI1_SCK	-	-	-	-	-	-	SAI1_SD_B	LPTIM2_ETR	-	CM4_EVENTOUT	
	PA6	-	TIM1_BKIN	-	-	SPI1_MISO	-	-	LPUART1_CTS	-	QUADSPI_BK1_IO3	LCD_SEG3	TIM1_BKIN	-	TIM16_CH1	CM4_EVENTOUT	
	PA7	-	TIM1_CH1N	-	-	I2C3_SCL	SPI1_MOSI	-	-	-	QUADSPI_BK1_IO2	LCD_SEG4	COMP2_OUT	-	TIM17_CH1	CM4_EVENTOUT	
	PA8	MCO	TIM1_CH1	-	SAI1_PDM_CK2	-	-	USART1_CK	-	-	LCD_COM0	-	SAI1_SCK_A	LPTIM2_OUT	-	CM4_EVENTOUT	
	PA9	-	TIM1_CH2	-	SAI1_PDM_D12	I2C1_SCL	SPI2_SCK	-	USART1_TX	-	-	LCD_COM1	-	SAI1_FS_A	-	CM4_EVENTOUT	
	PA10	-	TIM1_CH3	-	SAI1_PDM_D11	I2C1_SDA	-	-	USART1_RX	-	-	USB_CRS_SYNC	LCD_COM2	-	SAI1_SD_A	TIM17_BKIN	CM4_EVENTOUT
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	SPI1_MISO	-	USART1_CTS	-	-	USB_DM	-	TIM1_BKIN2	-	-	CM4_EVENTOUT	
	PA12	-	TIM1_ETR	-	-	SPI1_MOSI	-	USART1_RTS_D \bar{E}	LPUART1_RX	-	USB_DP	-	-	-	-	CM4_EVENTOUT	
	PA13	JTMS-SWDIO	-	-	-	-	-	IR_OUT	-	USB_NOE	-	-	SAI1_SD_B	-	-	CM4_EVENTOUT	
	PA14	JTCK-SWCLK	LPTIM1_OUT	-	-	I2C1_SMB \bar{A}	-	-	-	-	LCD_SEG5	-	SAI1_FS_B	-	-	CM4_EVENTOUT	
	PA15	JTDI	TIM2_CH1	TIM2_ETR	-	SPI1_NSS	MCO	-	-	-	LCD_SEG17	-	-	-	-	CM4_EVENTOUT	

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Table 18. Alternate functions (STM32WB55xx)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
	SYS_AF	TIM1/TIM2/LPTIM1	TIM1/TIM2	SPI2/SAI1/TIM1	I2C1/I2C3	SPI1/SPI2	RF	USART1	LPUART1	TSC	USB/QUADSPI	LCD	COMP1/COMP2/TIM1	SAI1	TIM2/TIM16/TIM17/LPTIM2	EVENTOUT	
A	PA0	-	TIM2_CH1	-	-	-	-	-	-	-	-	-	COMP1_OUT	SAI1_EXTCLK	TIM2_ETR	CM4_EVENTOUT	
	PA1	-	TIM2_CH2	-	-	I2C1_SMB \bar{A}	SPI1_SCK	-	-	-	-	-	LCD_SEG0	-	-	CM4_EVENTOUT	
	PA2	LSCO	TIM2_CH3	-	-	-	-	-	-	-	-	-	QUADSPI_BK1_NCS	LCD_SEG1	COMP2_OUT	-	CM4_EVENTOUT
	PA3	-	TIM2_CH4	-	SAI1_PDM_CK1	-	-	-	LPUART1_RX	-	QUADSPI_CLK	LCD_SEG2	-	SAI1_MCLK_A	-	CM4_EVENTOUT	
	PA4	-	-	-	-	SPI1_NSS	-	-	-	-	LCD_SEG5	-	SAI1_FS_B	LPTIM2_OUT	-	CM4_EVENTOUT	
	PA5	-	TIM2_CH1	TIM2_ETR	-	SPI1_SCK	-	-	-	-	-	-	-	SAI1_SD_B	LPTIM2_ETR	CM4_EVENTOUT	
	PA6	-	TIM1_BKIN	-	-	SPI1_MISO	-	-	LPUART1_CTS	-	QUADSPI_BK1_IO3	LCD_SEG3	TIM1_BKIN	-	TIM16_CH1	CM4_EVENTOUT	
	PA7	-	TIM1_CH1N	-	-	I2C3_SCL	SPI1_MOSI	-	-	-	QUADSPI_BK1_IO2	LCD_SEG4	COMP2_OUT	-	TIM17_CH1	CM4_EVENTOUT	
	PA8	MCO	TIM1_CH1	-	SAI1_PDM_CK2	-	-	USART1_CK	-	-	LCD_COM0	-	SAI1_SCK_A	LPTIM2_OUT	-	CM4_EVENTOUT	
	PA9	-	TIM1_CH2	-	SAI1_PDM_D12	I2C1_SCL	SPI2_SCK	-	USART1_TX	-	-	LCD_COM1	-	SAI1_FS_A	-	CM4_EVENTOUT	
	PA10	-	TIM1_CH3	-	SAI1_PDM_D11	I2C1_SDA	-	-	USART1_RX	-	-	USB_CRS_SYNC	LCD_COM2	-	SAI1_SD_A	TIM17_BKIN	CM4_EVENTOUT
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	SPI1_MISO	-	USART1_CTS	-	-	USB_DM	-	TIM1_BKIN2	-	-	CM4_EVENTOUT	
	PA12	-	TIM1_ETR	-	-	SPI1_MOSI	-	USART1_RTS_D \bar{E}	LPUART1_RX	-	USB_DP	-	-	-	-	CM4_EVENTOUT	
	PA13	JTMS-SWDIO	-	-	-	-	-	IR_OUT	-	USB_NOE	-	-	SAI1_SD_B	-	-	CM4_EVENTOUT	
	PA14	JTCK-SWCLK	LPTIM1_OUT	-	-	I2C1_SMB \bar{A}	-	-	-	-	-	-	SAI1_FS_B	-	-	CM4_EVENTOUT	
	PA15	JTDI	TIM2_CH1	TIM2_ETR	-	SPI1_NSS	MCO	-	-	-	-	-	LCD_SEG17	-	-	CM4_EVENTOUT	

Pinouts and pin description



Table 18. Alternate functions (STM32WB55xx) (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
	SYS_AF	TIM1/TIM2/LPTIM1	TIM1/TIM2	SPI2/SAI1/TIM1	I2C1/I2C3	SPI1/SPI2	RF	USART1	LPUART1	TSC	USB/QUADSPI	LCD	COMP1/COMP2/TIM1	SAI1	TIM2/TIM16/TIM17/LPTIM2	EVENTOUT	
B	PB0	-	-	-	-	-	-	RF_TX_MOD_EXT_PA	-	-	-	-	COMP1_OUT	-	-	CM4_EVENTOUT	
	PB1	-	-	-	-	-	-	-	LPUART1_RTS_DE	-	-	-	-	LPTIM2_IN1	-	CM4_EVENTOUT	
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	SPI1_NSS	-	-	-	-	LCD_VLCD	-	SAI1_EXTCLK	-	CM4_EVENTOUT	
	PB3	JTDO-TRACE SWO	TIM2_CH2	-	-	SPI1_SCK	-	USART1_RTS_DE	-	-	-	LCD_SEG7	-	SAI1_SCK_B	-	CM4_EVENTOUT	
	PB4	NJTRST	-	-	-	I2C3_SDA	SPI1_MISO	-	USART1_CTS	-	TSC_G2_IO1	-	LCD_SEG8	-	SAI1_MCLK_B	TIM17_BKIN	CM4_EVENTOUT
	PB5	-	LPTIM1_IN1	-	-	I2C1_SMBA	SPI1_MOSI	-	USART1_CK	LPUART1_TX	TSC_G2_IO2	-	LCD_SEG9	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	CM4_EVENTOUT
	PB6	MCO	LPTIM1_ETR	-	-	I2C1_SCL	-	-	USART1_TX	-	TSC_G2_IO3	-	LCD_SEG6	-	SAI1_FS_B	TIM16_CH1N	CM4_EVENTOUT
	PB7	-	LPTIM1_IN2	-	TIM1_BKIN	I2C1_SDA	-	-	USART1_RX	-	TSC_G2_IO4	-	LCD_SEG21	-	-	TIM17_CH1N	CM4_EVENTOUT
	PB8	-	TIM1_CH2N	-	SAI1_PDM_CK1	I2C1_SCL	-	-	-	-	QUADSPI_BK1_IO1	LCD_SEG16	-	SAI1_MCLK_A	TIM16_CH1	CM4_EVENTOUT	
	PB9	-	TIM1_CH3N	-	SAI1_PDM_D12	I2C1_SDA	SPI2_NSS	-	-	IR_OUT	TSC_G7_IO4	QUADSPI_BK1_IO0	LCD_COM3	-	SAI1_FS_A	TIM17_CH1	CM4_EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C3_SCL	SPI2_SC_K	-	-	LPUART1_RX	TSC_SYNC	QUADSPI_CLK	LCD_SEG10	COMP1_OUT	SAI1_SCK_A	-	CM4_EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C3_SDA	-	-	LPUART1_TX	-	QUADSPI_BK1_NCS	LCD_SEG11	COMP2_OUT	-	-	-	CM4_EVENTOUT
	PB12	-	TIM1_BKIN	-	TIM1_BKIN	I2C3_SMBA	SPI2_NSS	-	-	LPUART1_RTS	TSC_G1_IO1	-	LCD_SEG12	-	SAI1_FS_A	-	CM4_EVENTOUT
	PB13	-	TIM1_CH1N	-	-	I2C3_SCL	SPI2_SCK	-	-	USART1_CTS	TSC_G1_IO2	-	LCD_SEG13	-	SAI1_SCK_A	-	CM4_EVENTOUT
	PB14	-	TIM1_CH2N	-	-	I2C3_SDA	SPI2_MISO	-	-	-	TSC_G1_IO3	-	LCD_SEG14	-	SAI1_MCLK_A	-	CM4_EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	-	SPI2_MOSI	-	-	-	TSC_G1_IO4	-	LCD_SEG15	-	SAI1_SD_A	-	CM4_EVENTOUT	

Pinouts and pin description

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
	SYS_AF	TIM1/TIM2/LPTIM1	TIM1/TIM2	SPI2/SAI1/TIM1	I2C1/I2C3	SPI1/SPI2	RF	USART1	LPUART1	TSC	USB/QUADSPI	LCD	COMP1/COMP2/TIM1	SAI1	TIM2/TIM16/TIM17/LPTIM2	EVENTOUT	
B	PB0	-	-	-	-	-	-	-	-	RF_TX_MOD_EXT_PA	-	-	-	COMP1_OUT	-	-	CM4_EVENTOUT
	PB1	-	-	-	-	-	-	-	-	LPUART1_RTS_DE	-	-	-	-	-	-	CM4_EVENTOUT
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	SPI1_NSS	-	-	-	-	-	-	SAI1_EXTCLK	-	-	CM4_EVENTOUT
	PB3	JTDO-TRACE SWO	TIM2_CH2	-	-	SPI1_SCK	-	USART1_RTS_DE	-	-	-	-	-	LCD_VLCD	-	-	CM4_EVENTOUT
	PB4	NJTRST	-	-	-	I2C3_SDA	SPI1_MISO	-	USART1_CTS	-	TSC_G2_IO1	-	LCD_SEG8	-	SAI1_MCLK_B	TIM17_BKIN	CM4_EVENTOUT
	PB5	-	LPTIM1_IN1	-	-	I2C1_SMBA	SPI1_MOSI	-	USART1_CK	LPUART1_TX	TSC_G2_IO2	-	LCD_SEG9	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	CM4_EVENTOUT
	PB6	MCO	LPTIM1_ETR	-	-	I2C1_SCL	-	-	USART1_TX	-	TSC_G2_IO3	-	LCD_SEG6	-	SAI1_FS_B	TIM16_CH1N	CM4_EVENTOUT
	PB7	-	LPTIM1_IN2	-	TIM1_BKIN	I2C1_SDA	-	-	USART1_RX	-	TSC_G2_IO4	-	LCD_SEG21	-	-	TIM17_CH1N	CM4_EVENTOUT
	PB8	-	TIM1_CH2N	-	SAI1_PDM_CK1	I2C1_SCL	-	-	-	-	QUADSPI_BK1_IO1	LCD_SEG16	-	SAI1_MCLK_A	TIM16_CH1	CM4_EVENTOUT	
	PB9	-	TIM1_CH3N	-	SAI1_PDM_D12	I2C1_SDA	SPI2_NSS	-	-	IR_OUT	TSC_G7_IO4	QUADSPI_BK1_IO0	LCD_COM3	-	SAI1_FS_A	TIM17_CH1	CM4_EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C3_SCL	SPI2_SC_K	-	-	LPUART1_RX	TSC_SYNC	QUADSPI_CLK	LCD_SEG10	COMP1_OUT	SAI1_SCK_A	-	CM4_EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C3_SDA	-	-	LPUART1_TX	-	QUADSPI_BK1_NCS	LCD_SEG11	COMP2_OUT	-	-	-	CM4_EVENTOUT
	PB12	-	TIM1_BKIN	-	TIM1_BKIN	I2C3_SMBA	SPI2_NSS	-	-	LPUART1_RTS	TSC_G1_IO1	-	LCD_SEG12	-	SAI1_FS_A	-	CM4_EVENTOUT
	PB13	-	TIM1_CH1N	-	-	I2C3_SCL	SPI2_SCK	-	-	USART1_CTS	TSC_G1_IO2	-	LCD_SEG13	-	SAI1_SCK_A	-	CM4_EVENTOUT
	PB14	-	TIM1_CH2N	-	-	I2C3_SDA	SPI2_MISO	-	-	-	TSC_G1_IO3	-	LCD_SEG14	-	SAI1_MCLK_A	-	CM4_EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	-	SPI2_MOSI	-	-	-	TSC_G1_IO4	-	LCD_SEG15	-	SAI1_SD_A	-	CM4_EVENTOUT	



Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
Port		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
C	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	-	-	LPUART1_RX	-	-	LCD SEG18	-	-	LPTIM2_IN1	CM4_EVENTOUT	
	PC1	-	LPTIM1_OUT	-	SPI2_MOSI	I2C3_SDA	-	-	-	LPUART1_TX	-	-	LCD SEG19	-	-	CM4_EVENTOUT	
	PC2	-	LPTIM1_IN2	-	-	SPI2_MISO	-	-	-	-	-	LCD SEG20	-	-	-	CM4_EVENTOUT	
	PC3	-	LPTIM1_ETR	-	SAI1_PDM_DI1	-	SPI2_MOSI	-	-	-	-	LCD_VLCD	-	SAI1_SD_A	LPTIM2_ETR	CM4_EVENTOUT	
	PC4	-	-	-	-	-	-	-	-	-	-	LCD SEG22	-	-	-	CM4_EVENTOUT	
	PC5	-	-	-	SAI1_PDM_DI3	-	-	-	-	-	-	LCD SEG23	-	-	-	CM4_EVENTOUT	
	PC6	-	-	-	-	-	-	-	-	-	TSC_G4_IO1	-	LCD SEG24	-	-	CM4_EVENTOUT	
	PC7	-	-	-	-	-	-	-	-	-	TSC_G4_IO2	-	LCD SEG25	-	-	CM4_EVENTOUT	
	PC8	-	-	-	-	-	-	-	-	-	TSC_G4_IO3	-	LCD SEG26	-	-	CM4_EVENTOUT	
	PC9	-	-	-	TIM1_BKIN	-	-	-	-	-	TSC_G4_IO4	USB_NOE	LCD SEG27	-	SAI1_SCK_B	-	CM4_EVENTOUT
	PC10	TRACE_D1	-	-	-	-	-	-	-	-	TSC_G3_IO2	-	LCD COM4 LCD SEG28 LCD SEG40	-	-	-	CM4_EVENTOUT
	PC11	-	-	-	-	-	-	-	-	-	TSC_G3_IO3	-	LCD COM5 LCD SEG29 LCD SEG41	-	-	-	CM4_EVENTOUT
	PC12	TRACE_D3	-	-	-	-	-	-	-	-	TSC_G3_IO4	-	LCD COM6 LCD SEG30 LCD SEG42	-	-	-	CM4_EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
Port		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
C	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	-	-	LPUART1_RX	-	-	LCD SEG18	-	-	LPTIM2_IN1	CM4_EVENTOUT	
	PC1	-	LPTIM1_OUT	-	SPI2_MOSI	I2C3_SDA	-	-	-	LPUART1_TX	-	-	LCD SEG19	-	-	CM4_EVENTOUT	
	PC2	-	LPTIM1_IN2	-	-	SPI2_MISO	-	-	-	-	-	LCD SEG20	-	-	-	CM4_EVENTOUT	
	PC3	-	LPTIM1_ETR	-	SAI1_PDM_DI1	-	SPI2_MOSI	-	-	-	-	LCD_VLCD	-	SAI1_SD_A	LPTIM2_ETR	CM4_EVENTOUT	
	PC4	-	-	-	-	-	-	-	-	-	-	LCD SEG22	-	-	-	CM4_EVENTOUT	
	PC5	-	-	-	SAI1_PDM_DI3	-	-	-	-	-	-	LCD SEG23	-	-	-	CM4_EVENTOUT	
	PC6	-	-	-	-	-	-	-	-	-	TSC_G4_IO1	-	LCD SEG24	-	-	CM4_EVENTOUT	
	PC7	-	-	-	-	-	-	-	-	-	TSC_G4_IO2	-	LCD SEG25	-	-	CM4_EVENTOUT	
	PC8	-	-	-	-	-	-	-	-	-	TSC_G4_IO3	-	LCD SEG26	-	-	CM4_EVENTOUT	
	PC9	-	-	-	TIM1_BKIN	-	-	-	-	-	TSC_G4_IO4	USB_NOE	LCD SEG27	-	SAI1_SCK_B	-	CM4_EVENTOUT
	PC10	TRACE_D1	-	-	-	-	-	-	-	-	TSC_G3_IO2	-	LCD COM4 LCD SEG28 LCD SEG40	-	-	-	CM4_EVENTOUT
	PC11	-	-	-	-	-	-	-	-	-	TSC_G3_IO3	-	LCD COM5 LCD SEG29 LCD SEG41	-	-	-	CM4_EVENTOUT
	PC12	TRACE_D3	-	-	-	-	-	-	-	-	TSC_G3_IO4	-	LCD COM6 LCD SEG30 LCD SEG42	-	-	-	CM4_EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	



Table 18. Alternate functions (STM32WB55xx) (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
D	PD0	-	-	-	-	-	SPI2_NSS	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PD1	-	-	-	-	-	SPI2_SCK	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PD2	TRACE_D2	-	-	-	-	-	-	-	TSC_SYNC	-	LCD_COM7 LCD_SEG31 LCD_SEG43	-	-	-	CM4_EVENTOUT
	PD3	-	-	-	SPI2_SCK	-	SPI2_MISO	-	-	-	QUADSPI_BK1_NCS	-	-	-	-	CM4_EVENTOUT
	PD4	-	-	-	-	-	SPI2_MOSI	-	-	-	TSC_G5_IO1	QUADSPI_BK1_IO0	-	-	-	CM4_EVENTOUT
	PD5	-	-	-	-	-	-	-	-	TSC_G5_IO2	QUADSPI_BK1_IO1	-	-	SAI1_MCLK_B	-	CM4_EVENTOUT
	PD6	-	-	-	SAI1_PDM_DI1	-	-	-	-	TSC_G5_IO3	QUADSPI_BK1_IO2	-	-	SAI1_SD_A	-	CM4_EVENTOUT
	PD7	-	-	-	-	-	-	-	-	TSC_G5_IO4	QUADSPI_BK1_IO3	LCD SEG39	-	-	-	CM4_EVENTOUT
	PD8	-	-	-	TIM1_BKIN2	-	-	-	-	-	LCD SEG28	-	-	-	-	CM4_EVENTOUT
	PD9	TRACE_D0	-	-	-	-	-	-	-	-	LCD SEG29	-	-	-	-	CM4_EVENTOUT
	PD10	TRIG_INOUT	-	-	-	-	-	-	-	TSC_G6_IO1	-	LCD SEG30	-	-	-	CM4_EVENTOUT
	PD11	-	-	-	-	-	-	-	-	TSC_G6_IO2	-	LCD SEG31	-	-	LPTIM2_ETR	CM4_EVENTOUT
	PD12	-	-	-	-	-	-	-	-	TSC_G6_IO3	-	LCD SEG32	-	-	LPTIM2_IN1	CM4_EVENTOUT
	PD13	-	-	-	-	-	-	-	-	TSC_G6_IO4	-	LCD SEG33	-	-	LPTIM2_OUT	CM4_EVENTOUT
	PD14	-	TIM1_CH1	-	-	-	-	-	-	-	LCD SEG34	-	-	-	-	CM4_EVENTOUT
	PD15	-	TIM1_CH2	-	-	-	-	-	-	-	LCD SEG35	-	-	-	-	CM4_EVENTOUT

Pinouts and pin description

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
D	PD0	-	-	-	-	-	SPI2_NSS	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PD1	-	-	-	-	-	SPI2_SCK	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PD2	TRACE_D2	-	-	-	-	-	-	-	TSC_SYNC	-	LCD_COM7 LCD_SEG31 LCD_SEG43	-	-	-	CM4_EVENTOUT
	PD3	-	-	-	SPI2_SCK	-	SPI2_MISO	-	-	-	QUADSPI_BK1_NCS	-	-	-	-	CM4_EVENTOUT
	PD4	-	-	-	-	-	SPI2_MOSI	-	-	-	TSC_G5_IO1	QUADSPI_BK1_IO0	-	-	-	CM4_EVENTOUT
	PD5	-	-	-	-	-	-	-	-	TSC_G5_IO2	QUADSPI_BK1_IO1	-	-	SAI1_MCLK_B	-	CM4_EVENTOUT
	PD6	-	-	-	SAI1_PDM_DI1	-	-	-	-	TSC_G5_IO3	QUADSPI_BK1_IO2	-	-	SAI1_SD_A	-	CM4_EVENTOUT
	PD7	-	-	-	-	-	-	-	-	TSC_G5_IO4	QUADSPI_BK1_IO3	LCD SEG39	-	-	-	CM4_EVENTOUT
	PD8	-	-	-	TIM1_BKIN2	-	-	-	-	-	LCD SEG28	-	-	-	-	CM4_EVENTOUT
	PD9	TRACE_D0	-	-	-	-	-	-	-	-	LCD SEG29	-	-	-	-	CM4_EVENTOUT
	PD10	TRIG_INOUT	-	-	-	-	-	-	-	TSC_G6_IO1	-	LCD SEG30	-	-	-	CM4_EVENTOUT
	PD11	-	-	-	-	-	-	-	-	TSC_G6_IO2	-	LCD SEG31	-	-	LPTIM2_ETR	CM4_EVENTOUT
	PD12	-	-	-	-	-	-	-	-	TSC_G6_IO3	-	LCD SEG32	-	-	LPTIM2_IN1	CM4_EVENTOUT
	PD13	-	-	-	-	-	-	-	-	TSC_G6_IO4	-	LCD SEG33	-	-	LPTIM2_OUT	CM4_EVENTOUT
	PD14	-	TIM1_CH1	-	-	-	-	-	-	-	LCD SEG34	-	-	-	-	CM4_EVENTOUT
	PD15	-	TIM1_CH2	-	-	-	-	-	-	-	LCD SEG35	-	-	-	-	CM4_EVENTOUT



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Table 18. Alternate functions (STM32WB55xx) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
E	PE0	-	TIM1_ ETR	-	-	-	-	-	-	TSC_G7_I03	-	LCD_SEG36	-	-	TIM16_ CH1	CM4_ EVENTOUT	
	PE1	-	-	-	-	-	-	-	-	TSC_G7_I02	-	LCD_SEG37	-	-	TIM17_ CH1	CM4_ EVENTOUT	
	PE2	TRACECK	-	-	SAI1_ PDM_CK1	-	-	-	-	TSC_G7_I01	-	LCD_SEG38	-	SAI1_MCLK_A	-	CM4_ EVENTOUT	
	PE3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT	
	PE4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT	
	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT	
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT	
	PH3	LSCO	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT	

Table 18. Alternate functions (STM32WB55xx) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
E	PE0	-	TIM1_ ETR	-	-	-	-	-	-	TSC_G7_I03	-	LCD_SEG36	-	-	TIM16_ CH1	CM4_ EVENTOUT	
	PE1	-	-	-	-	-	-	-	-	TSC_G7_I02	-	LCD_SEG37	-	-	TIM17_ CH1	CM4_ EVENTOUT	
	PE2	TRACECK	-	-	SAI1_ PDM_CK1	-	-	-	-	TSC_G7_I01	-	LCD_SEG38	-	SAI1_MCLK_A	-	CM4_ EVENTOUT	
	PE3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT	
	PE4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT	
	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT	
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT	
	PH3	LSCO	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT	

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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF10	AF12	AF13	AF14	AF15
SYS_AF		TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SAI1/ I2C3	I2C1/ I2C3	SPI1	RF	USART1	LPUART1	USB/ QUADSPI	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT	
A	PA0	-	TIM2_ CH1	-	-	-	-	-	-	COMP1_ OUT	SAI1_ EXTCLK	TIM2_ ETR	CM4_ EVENTOUT		
	PA1	-	TIM2_ CH2	-	-	I2C1_ SMBA	SPI1_ SCK	-	-	-	-	-	CM4_ EVENTOUT		
	PA2	LSCO	TIM2_ CH3	-	-	-	-	-	LPUART1_ TX	QUADSPI_ BK1_NCS	COMP2_ OUT	-	-	CM4_ EVENTOUT	
	PA3	-	TIM2_ CH4	-	SAI1_ PDM_CK1	-	-	-	LPUART1_ RX	QUADSPI_ CLK	-	SAI1_ MCLK_A	-	CM4_ EVENTOUT	
	PA4	-	-	-	-	SPI1_ NSS	-	-	-	-	-	SAI1_ FS_B	LPTIM2_ OUT	CM4_ EVENTOUT	
	PA5	-	TIM2_ CH1	TIM2_ ETR	-	SPI1_ SCK	-	-	-	-	-	SAI1_ SD_B	LPTIM2_ ETR	CM4_ EVENTOUT	
	PA6	-	TIM1_ BKIN	-	-	SPI1_ MISO	-	-	LPUART1_ CTS	QUADSPI_ BK1_IO3	TIM1_ BKIN	-	TIM16_ CH1	CM4_ EVENTOUT	
	PA7	-	TIM1_ CH1N	-	-	I2C3_ SCL	SPI1_ MOSI	-	-	QUADSPI_ BK1_IO2	COMP2_ OUT	-	TIM17_ CH1	CM4_ EVENTOUT	
	PA8	MCO	TIM1_ CH1	-	SAI1_ PDM_CK2	-	-	USART1_ CK	-	-	SAI1_ SCK_A	LPTIM2_ OUT	CM4_ EVENTOUT		
	PA9	-	TIM1_ CH2	-	SAI1_ PDM_DI2	I2C1_ SCL	-	-	USART1_ TX	-	-	SAI1_ FS_A	-	CM4_ EVENTOUT	
	PA10	-	TIM1_ CH3	-	SAI1_ PDM_DI1	I2C1_ SDA	-	-	USART1_ RX	-	USB_CRS_ SYNC	-	SAI1_ SD_A	TIM17_ BKIN	CM4_ EVENTOUT
	PA11	-	TIM1_ CH4	TIM1_ BKIN2	-	-	SPI1_ MISO	-	USART1_ CTS	-	USB_DM	TIM1_ BKIN2	-	-	CM4_ EVENTOUT
	PA12	-	TIM1_ ETR	-	-	-	SPI1_ MOSI	-	USART1_ RTS_DE	LPUART1_ RX	USB_DP	-	-	-	CM4_ EVENTOUT
	PA13	JTMS- SWDIO	-	-	-	-	-	-	IR_OUT	USB_NOE	-	SAI1_ SD_B	-	CM4_ EVENTOUT	
	PA14	JTCK- SWCLK	LPTIM1_ OUT	-	-	I2C1_ SMBA	-	-	-	-	SAI1_ FS_B	-	CM4_ EVENTOUT		
	PA15	JTDI	TIM2_ CH1	TIM2_ ETR	-		SPI1_ NSS	MCO	-	-	-	-	-	-	CM4_ EVENTOUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF10	AF12	AF13	AF14	AF15
SYS_AF		TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SAI1/ I2C3	I2C1/ I2C3	SPI1	RF	USART1	LPUART1	USB/ QUADSPI	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT	
A	PA0	-	TIM2_ CH1	-	-	-	-	-	-	-	-	COMP1_ OUT	SAI1_ EXTCLK	TIM2_ ETR	CM4_ EVENTOUT
	PA1	-	TIM2_ CH2	-	-	I2C1_ SMBA	SPI1_ SCK	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PA2	LSCO	TIM2_ CH3	-	-	-	-	-	LPUART1_ TX	QUADSPI_ BK1_NCS	COMP2_ OUT	-	-	-	CM4_ EVENTOUT
	PA3	-	TIM2_ CH4	-	SAI1_ PDM_CK1	-	-	-	LPUART1_ RX	QUADSPI_ CLK	-	SAI1_ MCLK_A	-	CM4_ EVENTOUT	
	PA4	-	-	-	-	SPI1_ NSS	-	-	-	-	-	SAI1_ FS_B	LPTIM2_ OUT	CM4_ EVENTOUT	
	PA5	-	TIM2_ CH1	TIM2_ ETR	-	SPI1_ SCK	-	-	-	-	-	SAI1_ SD_B	LPTIM2_ ETR	CM4_ EVENTOUT	
	PA6	-	TIM1_ BKIN	-	-	SPI1_ MISO	-	-	LPUART1_ CTS	QUADSPI_ BK1_IO3	TIM1_ BKIN	-	TIM16_ CH1	CM4_ EVENTOUT	
	PA7	-	TIM1_ CH1N	-	-	I2C3_ SCL	SPI1_ MOSI	-	-	QUADSPI_ BK1_IO2	COMP2_ OUT	-	TIM17_ CH1	CM4_ EVENTOUT	
	PA8	MCO	TIM1_ CH1	-	SAI1_ PDM_CK2	-	-	USART1_ CK	-	-	SAI1_ SCK_A	LPTIM2_ OUT	CM4_ EVENTOUT		
	PA9	-	TIM1_ CH2	-	SAI1_ PDM_DI2	I2C1_ SCL	-	-	USART1_ TX	-	-	SAI1_ FS_A	-	CM4_ EVENTOUT	
	PA10	-	TIM1_ CH3	-	SAI1_ PDM_DI1	I2C1_ SDA	-	-	USART1_ RX	-	USB_CRS_ SYNC	-	SAI1_ SD_A	TIM17_ BKIN	CM4_ EVENTOUT
	PA11	-	TIM1_ CH4	TIM1_ BKIN2	-	-	SPI1_ MISO	-	USART1_ CTS	-	USB_DM	TIM1_ BKIN2	-	-	CM4_ EVENTOUT
	PA12	-	TIM1_ ETR	-	-	-	SPI1_ MOSI	-	USART1_ RTS_DE	LPUART1_ RX	USB_DP	-	-	-	CM4_ EVENTOUT
	PA13	JTMS- SWDIO	-	-	-	-	-	-	IR_OUT	USB_NOE	-	SAI1_ SD_B	-	CM4_ EVENTOUT	
	PA14	JTCK- SWCLK	LPTIM1_ OUT	-	-	I2C1_ SMBA	-	-	-	-	SAI1_ FS_B	-	CM4_ EVENTOUT		
	PA15	JTDI	TIM2_ CH1	TIM2_ ETR	-		SPI1_ NSS	MCO	-	-	-	-	-	-	CM4_ EVENTOUT

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Table 19. Alternate functions (STM32WB35xx) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF10	AF12	AF13	AF14	AF15
	SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SAI1/ I2C3	I2C1/ I2C3	SPI1	RF	USART1	LPUART1	USB/ QUADSPI	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT	
B	PB0	-	-	-	-	-	RF_TX_MOD_EXT_PA	-	-	COMP1_OUT	-	-	CM4_EVENTOUT		
	PB1	-	-	-	-	-	-	-	LPUART1_RTS_DE	-	-	-	LPTIM2_IN1	CM4_EVENTOUT	
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	SPI1_NSS	-	-	-	-	SAI1_EXTCLK	-	CM4_EVENTOUT	
	PB3	JTDO-TRACE SWO	TIM2_CH2	-	-	-	SPI1_SCK	-	USART1_RTS_DE	-	-	SAI1_SCK_B	-	CM4_EVENTOUT	
	PB4	NJTRST	-	-	-	I2C3_SDA	SPI1_MISO	-	USART1_CTS	-	-	SAI1_MCLK_B	TIM17_BKIN	CM4_EVENTOUT	
	PB5	-	LPTIM1_IN1	-	-	I2C1_SMBA	SPI1_MOSI	-	USART1_CK	LPUART1_TX	-	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	CM4_EVENTOUT
	PB6	MCO	LPTIM1_ETR	-	-	I2C1_SCL	-	-	USART1_TX	-	-	SAI1_FS_B	TIM16_CH1N	CM4_EVENTOUT	
	PB7	-	LPTIM1_IN2	-	TIM1_BKIN	I2C1_SDA	-	-	USART1_RX	-	-	-	TIM17_CH1N	CM4_EVENTOUT	
	PB8	-	TIM1_CH2N	-	SAI1_PDM_CK1	I2C1_SCL	-	-	-	QUADSPI_BK1_IO1	-	SAI1_MCLK_A	TIM16_CH1	CM4_EVENTOUT	
	PB9	-	TIM1_CH3N	-	SAI1_PDM_DI2	I2C1_SDA	-	-	-	IR_OUT	QUADSPI_BK1_IO0	-	SAI1_FS_A	TIM17_CH1	CM4_EVENTOUT
C	PC14	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	
	E	PE4	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	
H	PH3	LSCO	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	

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Table 19. Alternate functions (STM32WB35xx) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF10	AF12	AF13	AF14	AF15
	SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SAI1/ I2C3	I2C1/ I2C3	SPI1	RF	USART1	LPUART1	USB/ QUADSPI	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT	
B	PB0	-	-	-	-	-	-	-	RF_TX_MOD_EXT_PA	-	-	-	COMP1_OUT	-	CM4_EVENTOUT
	PB1	-	-	-	-	-	-	-	LPUART1_RTS_DE	-	-	-	-	LPTIM2_IN1	CM4_EVENTOUT
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	SPI1_NSS	-	-	-	-	-	SAI1_EXTCLK	-	CM4_EVENTOUT
	PB3	JTDO-TRACE SWO	TIM2_CH2	-	-	-	SPI1_SCK	-	USART1_RTS_DE	-	-	SAI1_SCK_B	-	CM4_EVENTOUT	
	PB4	NJTRST	-	-	-	I2C3_SDA	SPI1_MISO	-	USART1_CTS	-	-	SAI1_MCLK_B	TIM17_BKIN	CM4_EVENTOUT	
	PB5	-	LPTIM1_IN1	-	-	I2C1_SMBA	SPI1_MOSI	-	USART1_CK	LPUART1_TX	-	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	CM4_EVENTOUT
	PB6	MCO	LPTIM1_ETR	-	-	I2C1_SCL	-	-	USART1_TX	-	-	SAI1_FS_B	TIM16_CH1N	CM4_EVENTOUT	
	PB7	-	LPTIM1_IN2	-	TIM1_BKIN	I2C1_SDA	-	-	USART1_RX	-	-	-	TIM17_CH1N	CM4_EVENTOUT	
	PB8	-	TIM1_CH2N	-	SAI1_PDM_CK1	I2C1_SCL	-	-	-	QUADSPI_BK1_IO1	-	SAI1_MCLK_A	TIM16_CH1	CM4_EVENTOUT	
	PB9	-	TIM1_CH3N	-	SAI1_PDM_DI2	I2C1_SDA	-	-	-	IR_OUT	QUADSPI_BK1_IO0	-	SAI1_FS_A	TIM17_CH1	CM4_EVENTOUT
C	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	E	PE4	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
H	PH3	LSCO	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT

引脚布局和引脚说明

5 Memory mapping

The STM32WB55xx and STM32WB35xx devices feature a single physical address space that can be accessed by the application processor and by the RF subsystem.

A part of the Flash memory and of the SRAM2a and SRAM2b memories are made secure, exclusively accessible by the CPU2, protected against execution, read and write from CPU1 and DMA.

In case of shared resources the SW should implement arbitration mechanism to avoid access conflicts. This happens for peripherals Reset and Clock Controller (RCC), Power Controller (PWC), EXTI and Flash interface, and can be implemented using the built-in semaphore block (HSEM).

By default the RF subsystem and CPU2 operate in secure mode. This implies that part of the Flash and of the SRAM2 memories can only be accessed by the RF subsystem and by the CPU2. In this case the Host processor (CPU1) has no access to these resources.

The detailed memory map and the peripheral mapping can be found in the reference manual RM0434.

5 内存映射

STM32WB55xx 和 STM32WB35xx 设备具有一个单一的物理地址空间，可以由应用处理器和无线电子系统访问。

一部分闪存内存和SRAM2a和SRAM2b内存被保护，仅可由CPU2访问，对于CPU1和DMA的执行、读取和写入进行了保护。

在共享资源的情况下，软件应实现仲裁机制以避免访问冲突。这发生在外围设备复位和时钟控制器(RCC)、电源控制器(PWC)、扩展中断和事件控制器和闪存接口上，并可以使用内置的信号量块(HSEM)来实现。

默认情况下，无线电子系统和CPU2以安全模式运行。这意味着闪存的一部分和SRAM2内存的一部分仅可由无线电子系统和CPU2访问。在这种情况下，主处理器(CPU1)无法访问这些资源。

详细的内存映射和外围设备映射可以在参考手册 RM0434 中找到。

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25^\circ\text{C}$ and $T_A = T_{A\max}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on $V_{DD} = V_{DDA} = V_{DDRF} = 3\text{ V}$ and $T_A = 25^\circ\text{C}$. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

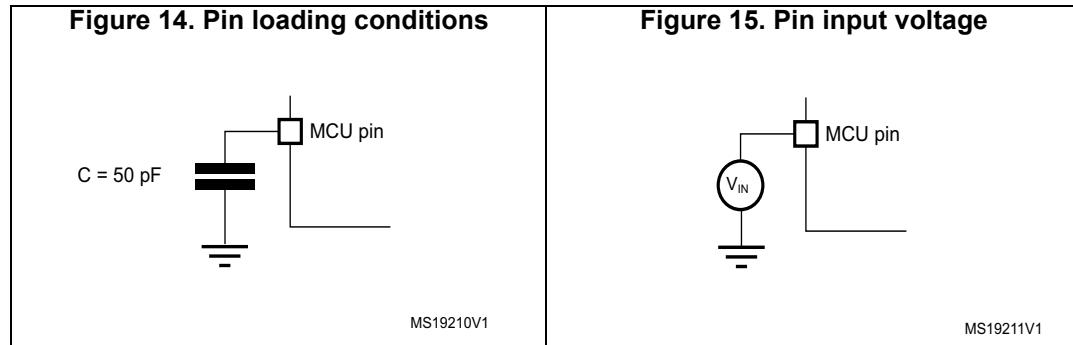
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 14](#).

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 15](#).



6 电气特性

6.1 参数条件

除非另有说明，所有电压均参考 V_{SS} .

6.1.1 最小和最大值

除非另有说明，最小和最大值在最差的环境温度、供电电压和频率条件下通过生产中的测试来保证，测试范围内100%的设备，环境温度为 $TA = 25^\circ\text{C}$ 和 $TA = T_{A\max}$ (由选择的温度范围)给出。

基于特性化结果、设计模拟和/或技术特性的数据在表脚注中标明，且不在生产中进行测试。
基于特性化，最小和最大值指的是样本测试，并表示平均值加减三倍的标准差 (mean $\pm 3\sigma$).

6.1.2 典型值

除非另有说明，典型数据基于 $V_{DD} = V_{DDA} = V_{DDRF} = 3\text{ V}$ 和 $TA = 25^\circ\text{C}$ 。它们仅用作设计指南，并未进行测试。

典型 ADC 精度值由对标准扩散批次中样本批次的特征化确定，覆盖完整温度范围，其中 95% 的设备错误小于或等于 (mean $\pm 2\sigma$) 值。

6.1.3 典型曲线

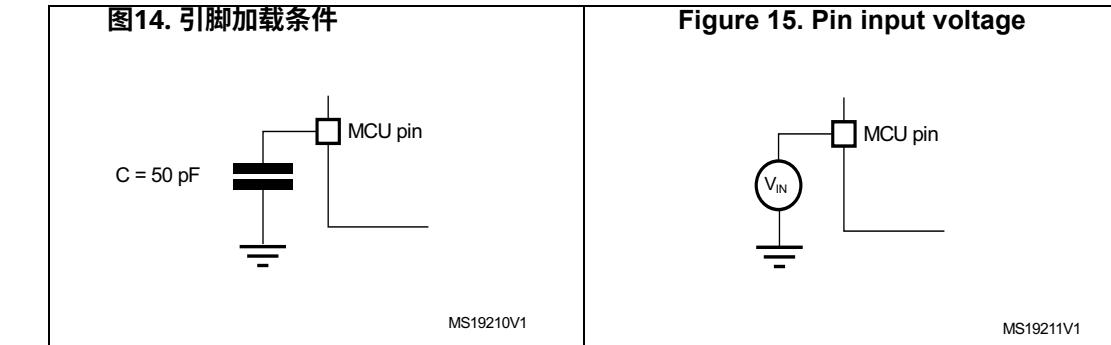
除非另有说明，所有典型曲线仅用作设计指南，并未进行测试。

6.1.4 载流器电容器

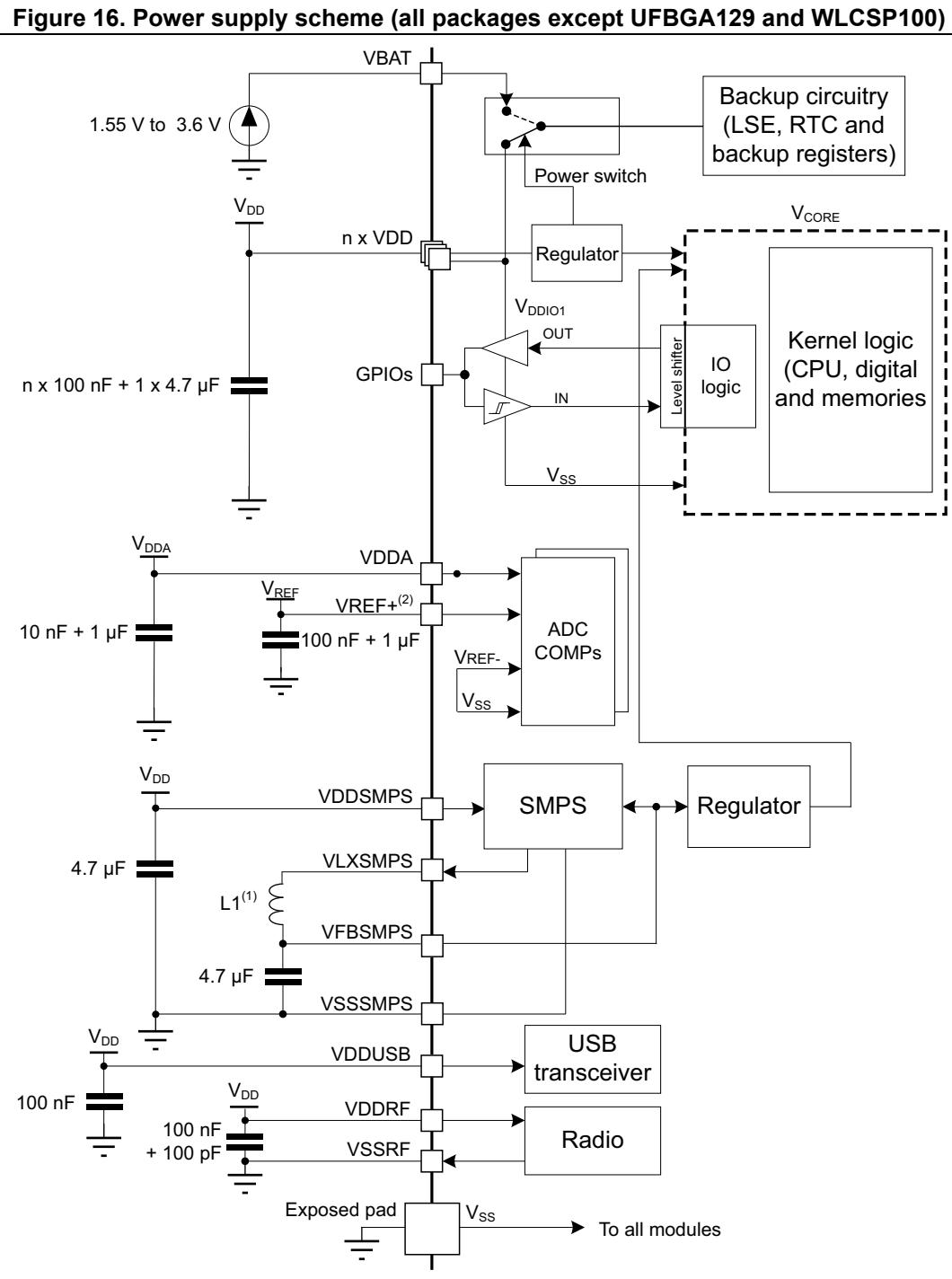
用于引脚参数测量的加载条件如下所示：[图14](#).

6.1.5 引脚输入电压

设备上引脚的输入电压测量在 [图15](#).



6.1.6 Power supply scheme

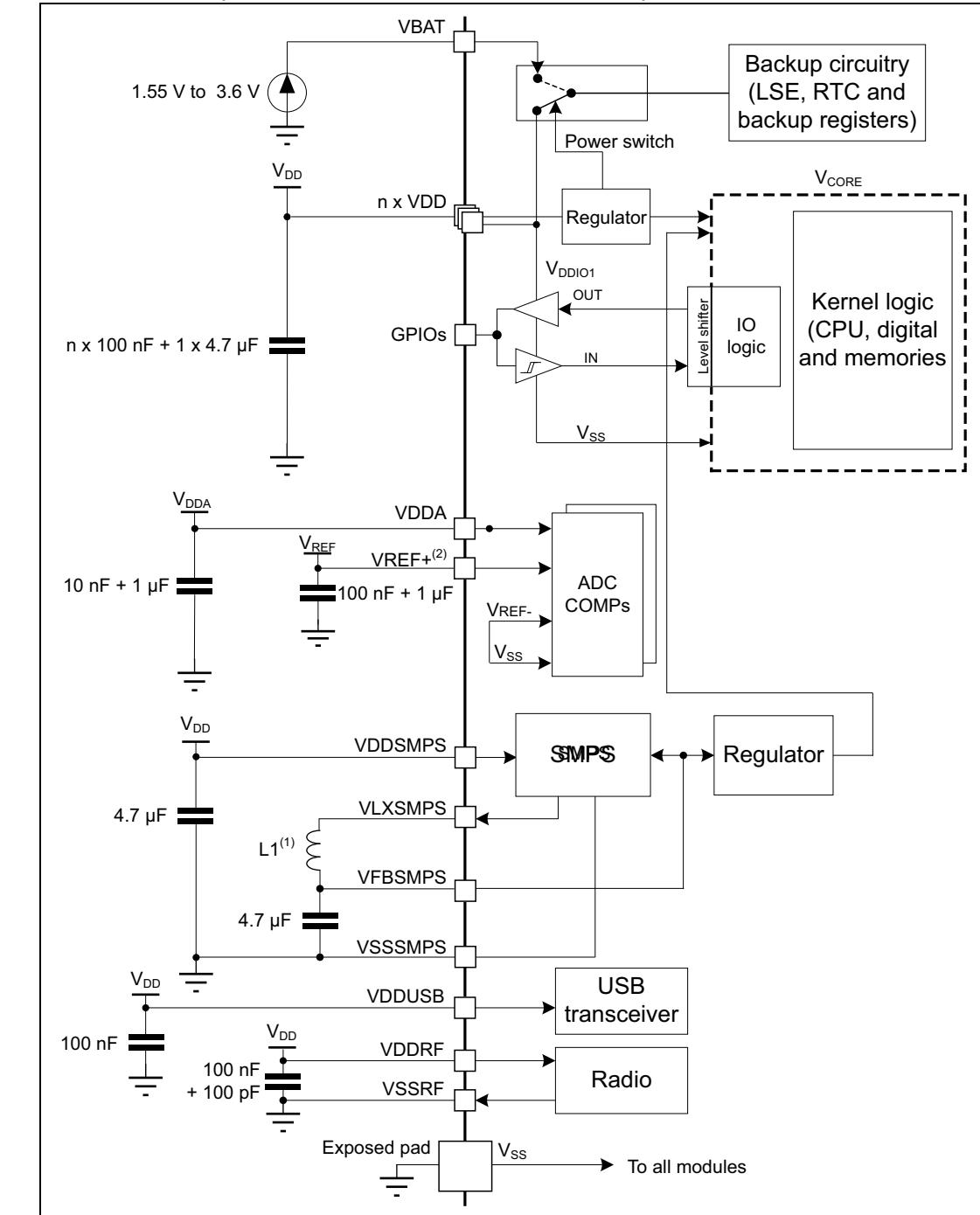


1. The value of L1 depends upon the frequency, as indicated in [Table 6](#).

2. VREF+ connection is not available on UFQFPN48 package.

6.1.6 电源方案

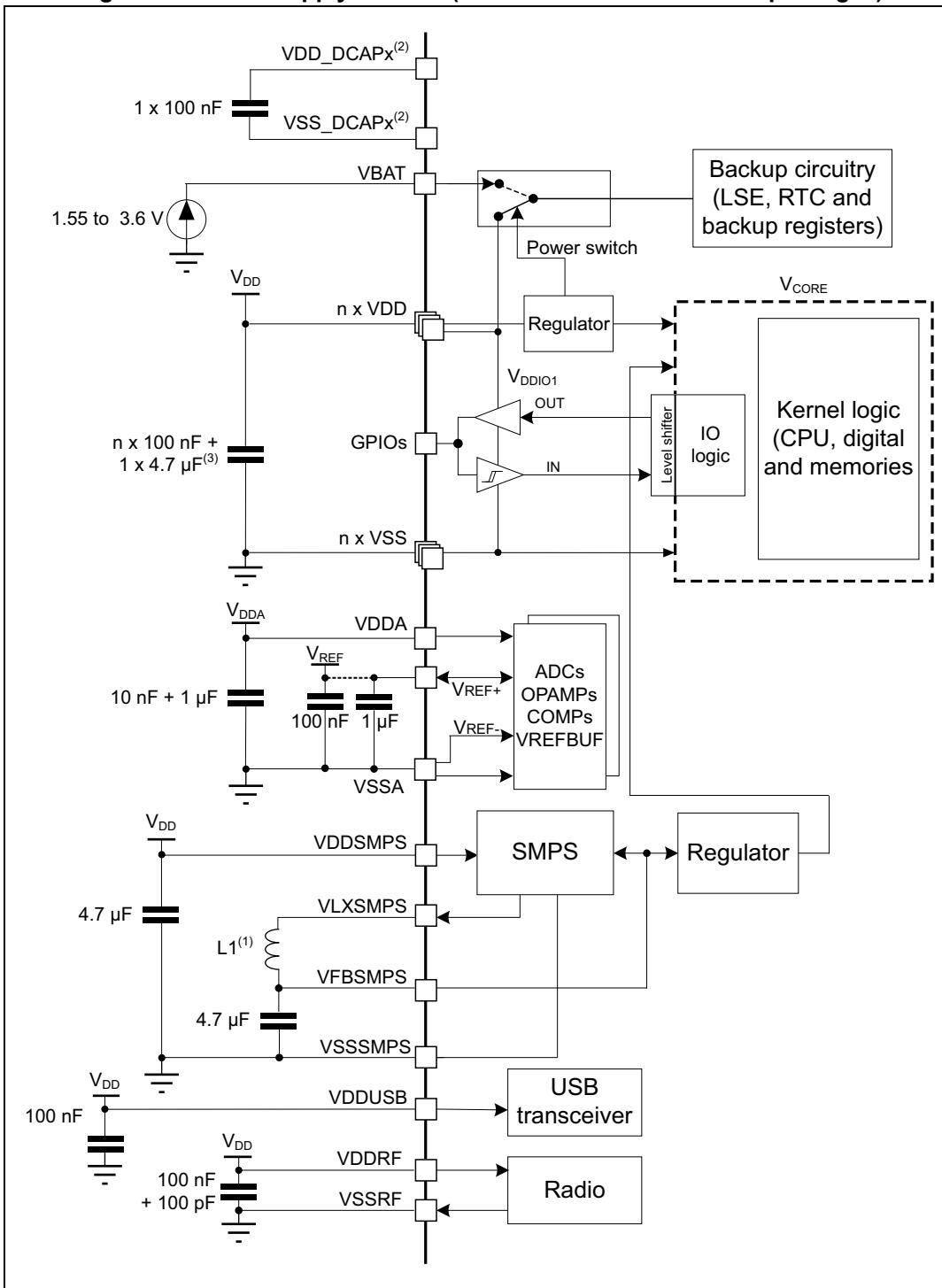
图16. 电源方案 (所有包装除了 UFBGA129 和 WLCSP100)



1. L1的值取决于频率，如表格中所示。表6. 2. VREF+ 连接不可用于

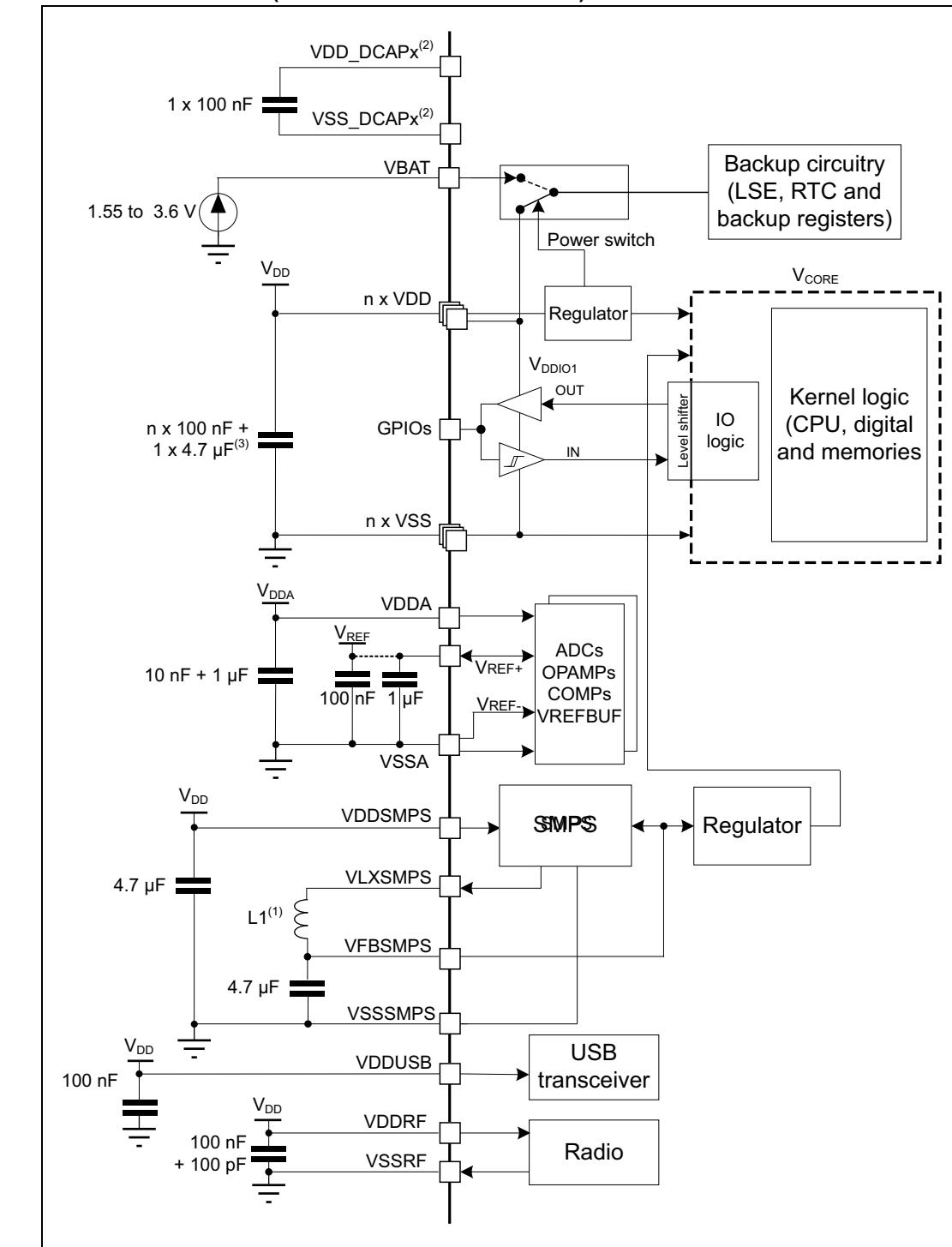
UFQFPN48包装。

Figure 17. Power supply scheme (UFBGA129 and WLCSP100 packages)



1. The value of L1 depends upon the frequency, as indicated in [Table 6](#).
2. For UFBGA129 package VDD_DCAPx and VSS_DCAPx balls are connected to V_{DD} and V_{SS} internally, to simplify the 2-layer board layout and especially the ground plane below the BGA. V_{DD} power supply can be made with a single connection to the center of the BGA on the board bottom layer. The decoupling 100 nF capacitors are connected without cutting the board ground plane.
3. $n \times 100 \text{ nF}$ only for WLCSP package.

图17. 电源方案 (UFBGA129和WLCSP100封装)

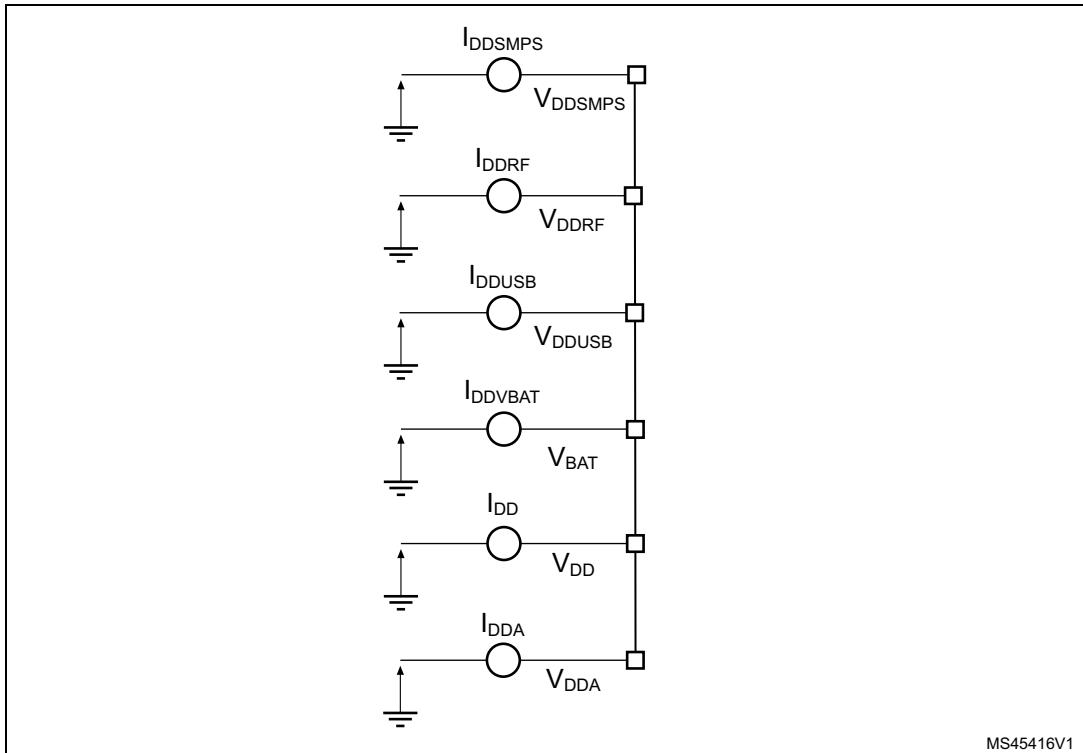


1. The value of L1 depends upon the frequency, as indicated in [Table 6](#).
2. For UFBGA129 package VDD_DCAPx and VSS_DCAPx balls are connected to V_{DD} and V_{SS} internally, to simplify the 2-layer board layout and especially the ground plane below the BGA. V_{DD} power supply can be made with a single connection to the center of the BGA on the board bottom layer. The decoupling 100 nF capacitors are connected without cutting the board ground plane.
3. $n \times 100 \text{ nF}$ only for WLCSP package.

Caution: Each power supply pair (V_{DD} / V_{SS} , V_{DDA} / V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown in [Figure 16](#). These capacitors must be placed as close as possible to (or below) the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

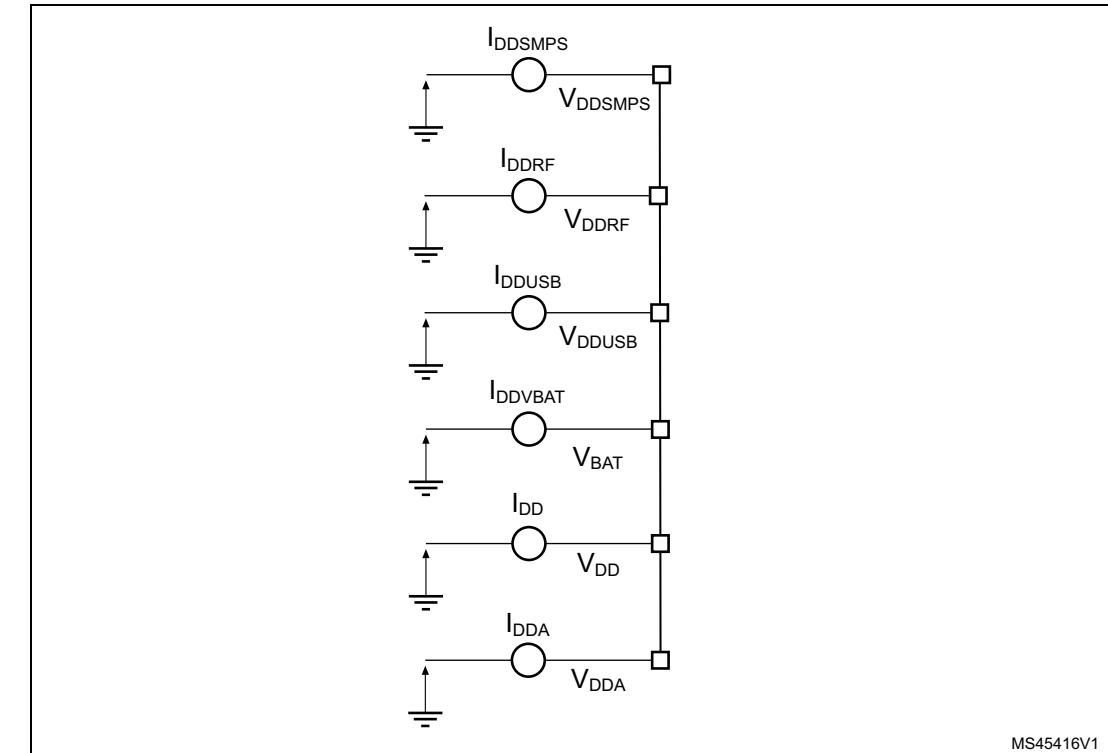
Figure 18. Current consumption measurement scheme



注意: 每组电源供应对 (V_{DD} / V_{SS} , V_{DDA} / V_{SSA} 等) 必须通过陶瓷滤波电容进行去耦，如图 [16](#) 所示。这些电容必须尽可能靠近 (或在下方) 相应引脚的 PCB 底面放置，以确保设备的良好功能。

6.1.7 电流消耗测量

Figure 18. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 20](#), [Table 21](#) and [Table 22](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

6.2 绝对最大额定值

超出表20、表21和表22中列出的绝对最大额定值的应力可能会对设备造成永久性损害。这些只是应力额定值，设备在这些条件下的功能操作不在此范围内。长时间暴露在最大额定值条件下可能会影响设备的可靠性。

Device mission profile (应用条件) 符合 JEDEC JESD47 认证标准，扩展任务配置文件可按需提供。

Table 20. Voltage characteristics⁽¹⁾

Symbol	Ratings	Min	Max	Unit
$V_{DDX} - V_{SS}$	External main supply voltage (including V_{DD} , V_{DDA} , V_{DDUSB} , V_{LCD} , V_{DDRF} , V_{DDSMPS} , V_{BAT} , V_{REF+})	-0.3	4.0	V
$V_{IN}^{(2)}$	Input voltage on FT_xxx pins	$V_{SS}-0.3$	min (V_{DD} , V_{DDA} , V_{DDUSB} , V_{LCD} , V_{DDRF} , V_{DDSMPS}) + 4.0 ⁽³⁾⁽⁴⁾	V
	Input voltage on TT_xx pins		4.0	
	Input voltage on any other pin		4.0	
$ \Delta V_{DDx} $	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$ V_{SSx}-V_{SSl} $	Variations between all the different ground pins ⁽⁵⁾	-	50	
$V_{REF+} - V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V

1. All main power (V_{DD} , V_{DDRF} , V_{DDA} , V_{DDUSB} , V_{LCD} , V_{BAT}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. V_{IN} maximum must always be respected. Refer to [Table 21](#) for the maximum allowed injected current values.

3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.

4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.

5. Include VREF- pin.

Table 21. Current characteristics

Symbol	Ratings	Max	Unit
ΣI_{DD}	Total current into sum of all V_{DD} power lines (source) ⁽¹⁾	130	
ΣI_{SS}	Total current out of sum of all V_{SS} ground lines (sink) ⁽¹⁾	130	
$I_{V_{DD}(PIN)}$	Maximum current into each V_{DD} power pin (source) ⁽¹⁾	100	
$I_{V_{SS}(PIN)}$	Maximum current out of each V_{SS} ground pin (sink) ⁽¹⁾	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins ⁽²⁾	100	
	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	100	
$I_{INJ(PIN)}^{(3)}$	Injected current on FT_xxx, TT_xx, RST and B pins, except PB0 and PB1	-5 / +0 ⁽⁴⁾	
	Injected current on PB0 and PB1	-5/0	
$\Sigma I_{INJ(PIN)} $	Total injected current (sum of all I/Os and control pins) ⁽⁵⁾	25	

1. All main power (V_{DD} , V_{DDRF} , V_{DDA} , V_{DDUSB} , V_{BAT}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.

2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count packages.

3. Positive injection (when $V_{IN} > V_{DD}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.

4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to [Table 20: Voltage characteristics](#) for the maximum allowed input voltage values.

表20. 电压特性⁽¹⁾

Symbol	Ratings	Min	Max	Unit
$V_{DDX} - V_{SS}$	External main supply voltage (including V_{DD} , V_{DDA} , V_{DDUSB} , V_{LCD} , V_{DDRF} , V_{DDSMPS} , V_{BAT} , V_{REF+})	-0.3	4.0	V
$V_{IN}^{(2)}$	Input voltage on FT_xxx pins	$V_{SS}-0.3$	min (V_{DD} , V_{DDA} , V_{DDUSB} , V_{LCD} , V_{DDRF} , V_{DDSMPS}) + 4.0 ⁽³⁾⁽⁴⁾	V
	Input voltage on TT_xx pins		4.0	
	Input voltage on any other pin		4.0	
$ \Delta V_{DDx} $	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$ V_{SSx}-V_{SSl} $	Variations between all the different ground pins ⁽⁵⁾	-	50	
$V_{REF+} - V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V

1. All main power (V_{DD} , V_{DDRF} , V_{DDA} , V_{DDUSB} , V_{LCD} , V_{BAT}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. V_{IN} maximum must always be respected. Refer to [Table 21](#) for the maximum allowed injected current values.

3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.

4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.

5. Include VREF- pin.

表21. 电流特性

Symbol	Ratings	Max	Unit
ΣI_{DD}	Total current into sum of all V_{DD} power lines (source) ⁽¹⁾	130	
ΣI_{SS}	Total current out of sum of all V_{SS} ground lines (sink) ⁽¹⁾	130	
$I_{V_{DD}(PIN)}$	Maximum current into each V_{DD} power pin (source) ⁽¹⁾	100	
$I_{V_{SS}(PIN)}$	Maximum current out of each V_{SS} ground pin (sink) ⁽¹⁾	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins ⁽²⁾	100	
	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	100	
$I_{INJ(PIN)}^{(3)}$	Injected current on FT_xxx, TT_xx, RST and B pins, except PB0 and PB1	-5 / +0 ⁽⁴⁾	
	Injected current on PB0 and PB1	-5/0	
$\Sigma I_{INJ(PIN)} $	Total injected current (sum of all I/Os and control pins) ⁽⁵⁾	25	

1. All main power (V_{DD} , V_{DDRF} , V_{DDA} , V_{DDUSB} , V_{BAT}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.

2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count packages.

3. Positive injection (when $V_{IN} > V_{DD}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.

4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to [Table 20: Voltage characteristics](#) for the maximum allowed input voltage values.

Electrical characteristics**STM32WB55xx STM32WB35xx**

5. When several inputs are submitted to a current injection, the maximum $\sum_{inj} |I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 22. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	130	

电气特性**STM32WB55xx STM32WB35xx**

5. W当多个输入被提交到一个电流注入时，最大的 $\sum_{inj} |I_{INJ(PIN)}|$ 是负载电流 (瞬时值) 的绝对总和。

e

表22. 热特性

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	130	

6.3 Operating conditions

6.3.1 Summary of main performance

Table 23. Main performance at $V_{DD} = 3.3$ V

Parameter		Test conditions	Typ	Unit
I_{CORE}	Core current consumption	VBAT ($V_{BAT} = 1.8$ V, $V_{DD} = 0$ V)	0.002	μ A
		Shutdown ($V_{DD} = 1.8$ V)	0.013	
		Standby ($V_{DD} = 1.8$ V, 32 Kbytes RAM retention)	0.320	
		Stop2	1.85	
		Sleep (16 MHz)	740	
		LP run (2 MHz)	320	
		Run (64 MHz)	5000	
		Radio RX ⁽¹⁾	4500	
		Radio TX 0 dBm output power ⁽¹⁾	5200	
I_{PERI}	Peripheral current consumption	Advertising with Stop 2 ⁽²⁾ (Tx = 0 dBm; Period 1.28 s; 31 bytes, 3 channels)	13	μ A
		Advertising with Stop 2 ⁽²⁾ (Tx = 0 dBm, 6 bytes; period 10.24 s, 3 channels)	4	
		LP timers	-	
		I2C3	-	
		LPUART	-	
		RTC	-	

1. Power consumption including RF subsystem and digital processing.

2. Power consumption integrated over 100 s, including Cortex-M4, RF subsystem, digital processing and Cortex-M0+.

6.3.2 General operating conditions

Table 24. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit	
f_{HCLK}	Internal AHB clock frequency	-	0	64	MHz	
f_{PCLK1}	Internal APB1 clock frequency	-	0	64		
f_{PCLK2}	Internal APB2 clock frequency	-	0	64		
V_{DD}	Standard operating voltage	-	1.71 ⁽¹⁾⁽²⁾	3.6	V	
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6		
		VREFBUF used	2.4			
		ADC, COMP, VREFBUF not used	0			
V_{BAT}	Backup operating voltage	-	1.55	3.6		

6.3 工作条件

6.3.1 主要性能总结

表23. 主要性能在 $VDD = 3.3$ V

Parameter		Test conditions	Typ	Unit
I_{CORE}	Core current consumption	VBAT ($V_{BAT} = 1.8$ V, $V_{DD} = 0$ V)	0.002	μ A
		Shutdown ($V_{DD} = 1.8$ V)	0.013	
		Standby ($V_{DD} = 1.8$ V, 32 Kbytes RAM retention)	0.320	
		Stop2	1.85	
		Sleep (16 MHz)	740	
		LP run (2 MHz)	320	
		Run (64 MHz)	5000	
		Radio RX ⁽¹⁾	4500	
		Radio TX 0 dBm output power ⁽¹⁾	5200	
I_{PERI}	Peripheral current consumption	Advertising with Stop 2 ⁽²⁾ (Tx = 0 dBm; Period 1.28 s; 31 bytes, 3 channels)	13	μ A
		Advertising with Stop 2 ⁽²⁾ (Tx = 0 dBm, 6 bytes; period 10.24 s, 3 channels)	4	
		LP timers	-	
		I2C3	-	
		LPUART	-	
		RTC	-	

1. Power consumption including RF subsystem and digital processing.

2. Power consumption integrated over 100 s, including Cortex-M4, RF subsystem, digital processing and Cortex-M0+.

6.3.2 通用运行条件

表24. 通用工作条件

Symbol	Parameter	Conditions	Min	Max	Unit	
f_{HCLK}	Internal AHB clock frequency	-	0	64	MHz	
f_{PCLK1}	Internal APB1 clock frequency	-	0	64		
f_{PCLK2}	Internal APB2 clock frequency	-	0	64		
V_{DD}	Standard operating voltage	-	1.71 ⁽¹⁾⁽²⁾	3.6	V	
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6		
		VREFBUF used	2.4			
		ADC, COMP, VREFBUF not used	0			
V_{BAT}	Backup operating voltage	-	1.55	3.6		

Table 24. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{FBMPS}	SMPS Feedback voltage	-	1.4	3.6	V
V_{DDRF}	Minimum RF voltage	-	1.71	3.6	
V_{DDUSB}	USB supply voltage	USB used	3.0	3.6	
		USB not used	0	3.6	
V_{IN}	I/O input voltage	TT_xx I/O	-0.3	$V_{DD} + 0.3$	mW
		All I/O except TT_xx	-0.3	$\min(\min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) + 3.6 \text{ V}, 5.5 \text{ V})^{(3)(4)}$	
P_D	Power dissipation at $T_A = 85^\circ\text{C}$ for suffix 6 or $T_A = 105^\circ\text{C}$ for suffix 7 ⁽⁵⁾	UFQFPN48	-	803	
		VFQFPN68	-	425	
		WL CSP100	-	558	
		UFBGA129	-	481	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	85	°C
		Low-power dissipation ⁽⁶⁾		105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	-40	105	
		Low-power dissipation ⁽⁶⁾		125	
T_J	Junction temperature range	Suffix 6 version	-40	105	
		Suffix 7 version		125	

- When RESET is released functionality is guaranteed down to V_{BOR0} Min.
- When V_{DDmin} is lower than 1.95 V, the SMPS operation mode must be conditioned by enabling the BORH configuration to force SMPS bypass mode, or the SMPS must not be enabled.
- This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between $\min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) + 3.6 \text{ V}$ and 5.5V.
- For operation with voltage higher than $\min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) + 0.3 \text{ V}$, the internal pull-up and pull-down resistors must be disabled.
- If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see [Section 7.5: Thermal characteristics](#)).
- In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see [Section 7.5: Thermal characteristics](#)).

6.3.3 RF BLE characteristics

RF characteristics are given at 1 Mbps, unless otherwise specified.

Table 25. RF transmitter BLE characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_{op}	Frequency operating range	-	2402	-	2480	MHz
F_{xtal}	Crystal frequency	-	-	32	-	
ΔF	Delta frequency	-	-	250	-	

表24. 通用工作条件 (继续)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{FBMPS}	SMPS Feedback voltage	-	1.4	3.6	V
V_{DDRF}	Minimum RF voltage	-	1.71	3.6	
V_{DDUSB}	USB supply voltage	USB used	3.0	3.6	
		USB not used	0	3.6	
V_{IN}	I/O input voltage	TT_xx I/O	-0.3	$V_{DD} + 0.3$	mW
		All I/O except TT_xx	-0.3	$\min(\min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) + 3.6 \text{ V}, 5.5 \text{ V})^{(3)(4)}$	
P_D	Power dissipation at $T_A = 85^\circ\text{C}$ for suffix 6 or $T_A = 105^\circ\text{C}$ for suffix 7 ⁽⁵⁾	UFQFPN48	-	803	
		VFQFPN68	-	425	
		WL CSP100	-	558	
		UFBGA129	-	481	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	85	°C
		Low-power dissipation ⁽⁶⁾		105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	-40	105	
		Low-power dissipation ⁽⁶⁾		125	
T_J	Junction temperature range	Suffix 6 version	-40	105	
		Suffix 7 version		125	

- When RESET is released functionality is guaranteed down to V_{BOR0} Min.
- 当 V_{DDmin} 于 1.95 V 时, SMPS 的运行模式必须通过启用 BORH 配置来强制进入 SMPS 绕过模式, 或者 SMPS 不应该被启用。
- 此公式只能应用于与由引脚定义表描述的 IO 结构相关的电源供应商。
最大 I/O 输入电压是 $(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) + 3.6 \text{ V}$ 和 5.5V 之间的最小值。
- 对于高于 $\min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) + 0.3 \text{ V}$, 内部上拉下拉电阻必须禁用。
- 如果 T_A 较低, 更高的 P_D 值被允许, 只要 T_J 不超过 T_{Jmax} (参见 [第 7.5 节: Thermal 特性](#))。
在低功耗散状态下, T 可以扩展到这个范围, 只要 J 不超过 J_{max} 。见节 7.5: 热特性)。

6.3.3 RF BLE 特性

RF 特性在 1 Mbps 下给出, 除非另有说明。

表25. RF 发送器 BLE 特性

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_{op}	Frequency operating range	-	2402	-	2480	MHz
F_{xtal}	Crystal frequency	-	-	32	-	
ΔF	Delta frequency	-	-	250	-	

Table 25. RF transmitter BLE characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Rgfsk	On Air data rate	-	-	1	2	Mbps
PLLres	RF channel spacing	-	-	2	-	MHz

Table 26. RF transmitter BLE characteristics (1 Mbps)⁽¹⁾

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
P_{rf}	Maximum output power	SMPS Bypass or ON ($V_{FBMPS} = 1.7 \text{ V}$ and $V_{DD} > 1.95 \text{ V}$) ⁽²⁾	-	6.0	-	dBm
		SMPS Bypass ($V_{DD} > 1.71 \text{ V}$) or ON ($V_{FBMPS} = 1.4 \text{ V}$ and $V_{DD} > 1.95 \text{ V}$), Code 29 ⁽²⁾	-	3.7	-	
	0 dBm output power	-	-	0	-	
	Minimum output power	-	-	-20	-	
P_{band}	Output power variation over the band	$Tx = 0 \text{ dBm}$ - Typical	-0.5	-	0.4	dB
BW6dB	6 dB signal bandwidth	$Tx = \text{maximum output power}$	-	670	-	kHz
IBSE	In band spurious emission	2 MHz Bluetooth® Low Energy: -20 dBm	-	-50	-	dBm
		$\geq 3 \text{ MHz}$ Bluetooth® Low Energy: -30 dBm	-	-53	-	
f_d	Frequency drift	Bluetooth® Low Energy: $\pm 50 \text{ kHz}$	-50	-	+50	kHz
maxdr	Maximum drift rate	Bluetooth® Low Energy: $\pm 20 \text{ kHz} / 50 \mu\text{s}$	-20	-	+20	kHz/ 50 μs
fo	Frequency offset	Bluetooth® Low Energy: $\pm 150 \text{ kHz}$	-150	-	+150	kHz
Δf_1	Frequency deviation average	Bluetooth® Low Energy: between 225 and 275 kHz	225	-	275	
Δf_a	Frequency deviation Δf_2 (average) / Δf_1 (average)	Bluetooth® Low Energy: > 0.80	0.80	-	-	-
OBSE ⁽³⁾	Out of band spurious emission	< 1 GHz	-	-61	-	dBm
		$\geq 1 \text{ GHz}$	-	-46	-	

- Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50Ω antenna.
- V_{FBMPS} and V_{DD} must be set to different voltage levels, depending upon the desired TX signal (see AN5246 *Usage of SMPS on STM32WB Series microcontrollers*, available on www.st.com).
- Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

表25. RF 发送器 BLE 特性 (继续)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Rgfsk	On Air data rate	-	-	1	2	Mbps
PLLres	RF channel spacing	-	-	2	-	MHz

表26. RF 发送器 BLE 特性 (1 Mbps)⁽¹⁾

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
P_{rf}	Maximum output power	SMPS Bypass or ON ($V_{FBMPS} = 1.7 \text{ V}$ and $V_{DD} > 1.95 \text{ V}$) ⁽²⁾	-	6.0	-	dBm
		SMPS Bypass ($V_{DD} > 1.71 \text{ V}$) or ON ($V_{FBMPS} = 1.4 \text{ V}$ and $V_{DD} > 1.95 \text{ V}$), Code 29 ⁽²⁾	-	3.7	-	
	0 dBm output power	-	-	0	-	
	Minimum output power	-	-	-20	-	
P_{band}	Output power variation over the band	$Tx = 0 \text{ dBm}$ - Typical	-0.5	-	0.4	dB
BW6dB	6 dB signal bandwidth	$Tx = \text{maximum output power}$	-	670	-	kHz
IBSE	In band spurious emission	2 MHz Bluetooth® Low Energy: -20 dBm	-	-50	-	dBm
		$\geq 3 \text{ MHz}$ Bluetooth® Low Energy: -30 dBm	-	-53	-	
f_d	Frequency drift	Bluetooth® Low Energy: $\pm 50 \text{ kHz}$	-50	-	+50	kHz
maxdr	Maximum drift rate	Bluetooth® Low Energy: $\pm 20 \text{ kHz} / 50 \mu\text{s}$	-20	-	+20	kHz/ 50 μs
fo	Frequency offset	Bluetooth® Low Energy: $\pm 150 \text{ kHz}$	-150	-	+150	kHz
Δf_1	Frequency deviation average	Bluetooth® Low Energy: between 225 and 275 kHz	225	-	275	
Δf_a	Frequency deviation Δf_2 (average) / Δf_1 (average)	Bluetooth® Low Energy: > 0.80	0.80	-	-	-
OBSE ⁽³⁾	Out of band spurious emission	< 1 GHz	-	-61	-	dBm
		$\geq 1 \text{ GHz}$	-	-46	-	

- Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50Ω antenna.
- V_{FBMPS} and V_{DD} must be set to different voltage levels, depending upon the desired TX signal (see AN5246 *Usage of SMPS on STM32WB Series microcontrollers*, available on www.st.com).
- Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

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Table 27. RF transmitter BLE characteristics (2 Mbps)⁽¹⁾

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
P_{rf}	Maximum output power		SMPS Bypass or ON ($V_{FBSPS} = 1.7 \text{ V}$ and $V_{DD} > 1.95 \text{ V}$) ⁽²⁾	-	6.0	-	dBm
			SMPS Bypass or ON ($V_{FBSPS} = 1.4 \text{ V}$ and $V_{DD} > 1.71 \text{ V}$), Code 29 ⁽²⁾	-	3.7	-	
	0 dBm output power		-	-	0	-	
	Minimum output power		-	-	-20	-	
P_{band}	Output power variation over the band		Tx = 0 dBm - Typical	-0.5	-	0.4	dB
BW6dB	6 dB signal bandwidth		Tx = maximum output power	-	670	-	kHz
IBSE	In band spurious emission	4 MHz	Bluetooth® Low Energy: -20 dBm	-	-56	-	dBm
		5 MHz	Bluetooth® Low Energy: -20 dBm	-	-57	-	
		$\geq 6 \text{ MHz}$	Bluetooth® Low Energy: -30 dBm		-58		
f_d	Frequency drift		Bluetooth® Low Energy: $\pm 50 \text{ kHz}$	-50	-	50	kHz
maxdr	Maximum drift rate		Bluetooth® Low Energy: $\pm 20 \text{ kHz} / 50 \mu\text{s}$	-20	-	20	kHz/ 50 μs
fo	Frequency offset		Bluetooth® Low Energy: $\pm 150 \text{ kHz}$	-150	-	150	kHz
Δf_1	Frequency deviation average		Bluetooth® Low Energy: between 450 and 550 kHz	450	-	550	
Δf_a	Frequency deviation Δf_2 (average) / Δf_1 (average)		Bluetooth® Low Energy: > 0.80	0.80	-	-	-
OBSE ⁽³⁾	Out of band spurious emission	< 1 GHz	-	-	-61	-	dBm
		$\geq 1 \text{ GHz}$	-	-	-46	-	

1. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50Ω antenna.
2. V_{FBSPS} and V_{DD} must be set to different voltage levels, depending upon the desired TX signal (see AN5246 *Usage of SMPS on STM32WB Series microcontrollers*, available on www.st.com).
3. Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

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表27. RF 发送器 BLE 特性 (2 Mbps)⁽¹⁾

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
P_{rf}	Maximum output power		SMPS Bypass or ON ($V_{FBSPS} = 1.7 \text{ V}$ and $V_{DD} > 1.95 \text{ V}$) ⁽²⁾	-	6.0	-	dBm
			SMPS Bypass or ON ($V_{FBSPS} = 1.4 \text{ V}$ and $V_{DD} > 1.71 \text{ V}$), Code 29 ⁽²⁾	-	3.7	-	
	0 dBm output power		-	-	0	-	
	Minimum output power		-	-	-20	-	
P_{band}	Output power variation over the band		Tx = 0 dBm - Typical	-0.5	-	0.4	dB
BW6dB	6 dB signal bandwidth		Tx = maximum output power	-	670	-	kHz
IBSE	In band spurious emission	4 MHz	Bluetooth® Low Energy: -20 dBm	-	-56	-	dBm
		5 MHz	Bluetooth® Low Energy: -20 dBm	-	-57	-	
		$\geq 6 \text{ MHz}$	Bluetooth® Low Energy: -30 dBm		-58		
f_d	Frequency drift		Bluetooth® Low Energy: $\pm 50 \text{ kHz}$	-50	-	50	kHz
maxdr	Maximum drift rate		Bluetooth® Low Energy: $\pm 20 \text{ kHz} / 50 \mu\text{s}$	-20	-	20	kHz/ 50 μs
fo	Frequency offset		Bluetooth® Low Energy: $\pm 150 \text{ kHz}$	-150	-	150	kHz
Δf_1	Frequency deviation average		Bluetooth® Low Energy: between 450 and 550 kHz	450	-	550	
Δf_a	Frequency deviation Δf_2 (average) / Δf_1 (average)		Bluetooth® Low Energy: > 0.80	0.80	-	-	-
OBSE ⁽³⁾	Out of band spurious emission	< 1 GHz	-	-	-61	-	dBm
		$\geq 1 \text{ GHz}$	-	-	-46	-	

1. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50Ω antenna.
2. V_{FBSPS} and V_{DD} must be set to different voltage levels, depending upon the desired TX signal (see AN5246 *Usage of SMPS on STM32WB Series microcontrollers*, available on www.st.com).
3. Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

Table 28. RF receiver BLE characteristics (1 Mbps)

Symbol	Parameter	Test conditions	Typ	Unit
Prx_max	Maximum input signal	PER <30.8% Bluetooth® Low Energy: min -10 dBm	0	dBm
Psens ⁽¹⁾	High sensitivity mode (SMPS Bypass)	PER <30.8%	-96	
	High sensitivity mode (SMPS ON)	Bluetooth® Low Energy: max -70 dBm	-95.5	
Rssi_maxrange	RSSI maximum value	-	-7	
Rssi_minrange	RSSI minimum value	-	-94	
Rssi_accu	RSSI accuracy	-	2	
C/Ico	Co-channel rejection	Bluetooth® Low Energy: 21 dB	8	
C/I	Adjacent channel interference	Adj ≥ 5 MHz Bluetooth® Low Energy: -27 dB	-53	
		Adj ≤ -5 MHz Bluetooth® Low Energy: -27 dB	-53	
		Adj = 4 MHz Bluetooth® Low Energy: -27 dB	-48	
		Adj = -4 MHz Bluetooth® Low Energy: -15 dB	-33	
		Adj = 3 MHz Bluetooth® Low Energy: -27 dB	-46	
		Adj = 2 MHz Bluetooth® Low Energy: -17 dB	-39	
		Adj = -2 MHz Bluetooth® Low Energy: -15 dB	-35	
		Adj = 1 MHz Bluetooth® Low Energy: 15 dB	-2	
		Adj = -1 MHz Bluetooth® Low Energy: 15 dB	2	
C/Image	Image rejection ($F_{image} = -3 \text{ MHz}$)	Bluetooth® Low Energy: -9 dB	-29	
P_IMD	Intermodulation	f2-f1 = 3 MHz Bluetooth® Low Energy: -50 dBm	-34	dBm
		f2-f1 = 4 MHz Bluetooth® Low Energy: -50 dBm	-30	
		f2-f1 = 5 MHz Bluetooth® Low Energy: -50 dBm	-32	

表28. 无线电接收器 蓝牙特性 (1 Mbps)

Symbol	Parameter	Test conditions	Typ	Unit
Prx_max	Maximum input signal	PER <30.8% Bluetooth® Low Energy: min -10 dBm	0	dBm
Psens ⁽¹⁾	High sensitivity mode (SMPS Bypass)	PER <30.8%	-96	
	High sensitivity mode (SMPS ON)	Bluetooth® Low Energy: max -70 dBm	-95.5	
Rssi_maxrange	RSSI maximum value	-	-7	
Rssi_minrange	RSSI minimum value	-	-94	
Rssi_accu	RSSI accuracy	-	2	
C/Ico	Co-channel rejection	Bluetooth® Low Energy: 21 dB	8	
C/I	Adjacent channel interference	Adj ≥ 5 MHz Bluetooth® Low Energy: -27 dB	-53	
		Adj ≤ -5 MHz Bluetooth® Low Energy: -27 dB	-53	
		Adj = 4 MHz Bluetooth® Low Energy: -27 dB	-48	
		Adj = -4 MHz Bluetooth® Low Energy: -15 dB	-33	
		Adj = 3 MHz Bluetooth® Low Energy: -27 dB	-46	
		Adj = 2 MHz Bluetooth® Low Energy: -17 dB	-39	
		Adj = -2 MHz Bluetooth® Low Energy: -15 dB	-35	
		Adj = 1 MHz Bluetooth® Low Energy: 15 dB	-2	
		Adj = -1 MHz Bluetooth® Low Energy: 15 dB	2	
C/Image	Image rejection ($F_{image} = -3 \text{ MHz}$)	Bluetooth® Low Energy: -9 dB	-29	
P_IMD	Intermodulation	f2-f1 = 3 MHz Bluetooth® Low Energy: -50 dBm	-34	dBm
		f2-f1 = 4 MHz Bluetooth® Low Energy: -50 dBm	-30	
		f2-f1 = 5 MHz Bluetooth® Low Energy: -50 dBm	-32	

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Table 28. RF receiver BLE characteristics (1 Mbps) (continued)

Symbol	Parameter	Test conditions	Typ	Unit
P_OBB	Out of band blocking	30 to 2000 MHz Bluetooth® Low Energy: -30 dBm	-3	dBm
		2003 to 2399 MHz Bluetooth® Low Energy: -35 dBm	-5	
		2484 to 2997 MHz Bluetooth® Low Energy: -35 dBm	-2	
		3 to 12.75 GHz Bluetooth® Low Energy: -30 dBm	7	

1. With ideal TX.

Table 29. RF receiver BLE characteristics (2 Mbps)

Symbol	Parameter	Test conditions	Typ	Unit
Prx_max	Maximum input signal	PER <30.8% Bluetooth® Low Energy: min -10 dBm	0	dBm
Psens ⁽¹⁾	High sensitivity mode (SMPS Bypass)	PER <30.8%	-93	
	High sensitivity mode (SMPS ON)	Bluetooth® Low Energy: max -70 dBm	-92.5	
Rssi_maxrange	RSSI maximum value	-	-7	
Rssi_minrange	RSSI minimum value	-	-94	dB
Rssi_accu	RSSI accuracy	-	2	
C/Ico	Co-channel rejection	Bluetooth® Low Energy spec: 21 dB	9	
C/I	Adjacent channel interference	Adj ≥ 8MHz Bluetooth® Low Energy: -27 dB	-53	
		Adj ≤ -8 MHz Bluetooth® Low Energy: -27 dB	-50	
		Adj = 6 MHz Bluetooth® Low Energy: -27 dB	-49	
		Adj = -6 MHz Bluetooth® Low Energy: -15 dB	-46	
		Adj = 4 MHz Bluetooth® Low Energy: -17 dB	-42	
		Adj = 2 MHz Bluetooth® Low Energy: 15 dB	-3	
		Adj = -2 MHz Bluetooth® Low Energy: 15 dB	-3	
C/Image	Image rejection ($F_{image} = -4$ MHz)	Bluetooth® Low Energy: -9 dB	-26	

Electrical characteristics
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Table 28. RF receiver 蓝牙特性 (1 Mbps) (continued)

Symbol	Parameter	Test conditions	Typ	Unit
P_OBB	Out of band blocking	30 to 2000 MHz Bluetooth® Low Energy: -30 dBm	-3	dBm
		2003 to 2399 MHz Bluetooth® Low Energy: -35 dBm	-5	
		2484 to 2997 MHz Bluetooth® Low Energy: -35 dBm	-2	
		3 to 12.75 GHz Bluetooth® Low Energy: -30 dBm	7	

1. With ideal TX.

Table 29. RF receiver 蓝牙特性 (2 Mbps)

Symbol	Parameter	Test conditions	Typ	Unit
Prx_max	Maximum input signal	PER <30.8% Bluetooth® Low Energy: min -10 dBm	0	dBm
Psens ⁽¹⁾	High sensitivity mode (SMPS Bypass)	PER <30.8%	-93	
	High sensitivity mode (SMPS ON)	Bluetooth® Low Energy: max -70 dBm	-92.5	
Rssi_maxrange	RSSI maximum value	-	-7	
Rssi_minrange	RSSI minimum value	-	-94	dB
Rssi_accu	RSSI accuracy	-	2	
C/Ico	Co-channel rejection	Bluetooth® Low Energy spec: 21 dB	9	
C/I	Adjacent channel interference	Adj ≥ 8MHz Bluetooth® Low Energy: -27 dB	-53	
		Adj ≤ -8 MHz Bluetooth® Low Energy: -27 dB	-50	
		Adj = 6 MHz Bluetooth® Low Energy: -27 dB	-49	
		Adj = -6 MHz Bluetooth® Low Energy: -15 dB	-46	
		Adj = 4 MHz Bluetooth® Low Energy: -17 dB	-42	
		Adj = 2 MHz Bluetooth® Low Energy: 15 dB	-3	
		Adj = -2 MHz Bluetooth® Low Energy: 15 dB	-3	
C/Image	Image rejection ($F_{image} = -4$ MHz)	Bluetooth® Low Energy: -9 dB	-26	

Table 29. RF receiver BLE characteristics (2 Mbps) (continued)

Symbol	Parameter	Test conditions	Typ	Unit
P_IMD	Intermodulation	f2-f1 = 6 MHz Bluetooth® Low Energy: -50 dBm	-29	dBm
		f2-f1 = 8 MHz Bluetooth® Low Energy: -50 dBm	-30	
		f2-f1 = 10 MHz Bluetooth® Low Energy: -50 dBm	-29	
P_OBB	Out of band blocking	30 to 2000 MHz Bluetooth® Low Energy: -30 dBm	-3	dBm
		2003 to 2399 MHz Bluetooth® Low Energy: -35 dBm	-9	
		2484 to 2997 MHz Bluetooth® Low Energy: -35 dBm	-3	
		3 to 12.75 GHz Bluetooth® Low Energy: -30 dBm	4	

1. With ideal TX.

Table 30. RF BLE power consumption for $V_{DD} = 3.3$ V⁽¹⁾

Symbol	Parameter	Typ	Unit
I _{txmax}	TX maximum output power consumption (SMPS Bypass)	12.7	mA
	TX maximum output power consumption (SMPS On, $V_{FB\text{SMPS}} = 1.7$ V)	7.8	
I _{tx0dbm}	TX 0 dBm output power consumption (SMPS Bypass)	8.8	mA
	TX 0 dBm output power consumption (SMPS On, $V_{FB\text{SMPS}} = 1.4$ V)	5.2	
I _{rxlo}	Rx consumption (SMPS Bypass)	7.9	mA
	Rx consumption (SMPS On, $V_{FB\text{SMPS}} = 1.4$ V)	4.5	

1. Power consumption including RF subsystem and digital processing.

6.3.4 RF 802.15.4 characteristics

Table 31. RF transmitter 802.15.4 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F _{op}	Frequency operating range	-	2405	-	2480	MHz
F _{xtal}	Crystal frequency	-	-	32	-	
ΔF	Delta frequency	-	-	5	-	
Roqpsk	On air data rate	-	-	250	-	
PLLres	RF channel spacing	-	-	5	-	

表29. 射频接收器 蓝牙特性 (2 Mbps) (continued)

Symbol	Parameter	Test conditions	Typ	Unit
P_IMD	Intermodulation	f2-f1 = 6 MHz Bluetooth® Low Energy: -50 dBm	-29	dBm
		f2-f1 = 8 MHz Bluetooth® Low Energy: -50 dBm	-30	
		f2-f1 = 10 MHz Bluetooth® Low Energy: -50 dBm	-29	
P_OBB	Out of band blocking	30 to 2000 MHz Bluetooth® Low Energy: -30 dBm	-3	dBm
		2003 to 2399 MHz Bluetooth® Low Energy: -35 dBm	-9	
		2484 to 2997 MHz Bluetooth® Low Energy: -35 dBm	-3	
		3 to 12.75 GHz Bluetooth® Low Energy: -30 dBm	4	

1. With ideal TX.

表30. $V_{DD} = 3.3$ V⁽¹⁾ 蓝牙 无线电 功耗

Symbol	Parameter	Typ	Unit
I _{txmax}	TX maximum output power consumption (SMPS Bypass)	12.7	mA
	TX maximum output power consumption (SMPS On, $V_{FB\text{SMPS}} = 1.7$ V)	7.8	
I _{tx0dbm}	TX 0 dBm output power consumption (SMPS Bypass)	8.8	mA
	TX 0 dBm output power consumption (SMPS On, $V_{FB\text{SMPS}} = 1.4$ V)	5.2	
I _{rxlo}	Rx consumption (SMPS Bypass)	7.9	mA
	Rx consumption (SMPS On, $V_{FB\text{SMPS}} = 1.4$ V)	4.5	

1. Power consumption including RF subsystem and digital processing.

6.3.4 RF 802.15.4 特性

表31. 无线电发射器 802.15.4 特性

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F _{op}	Frequency operating range	-	2405	-	2480	MHz
F _{xtal}	Crystal frequency	-	-	32	-	
ΔF	Delta frequency	-	-	5	-	
Roqpsk	On air data rate	-	-	250	-	
PLLres	RF channel spacing	-	-	5	-	

Table 31. RF transmitter 802.15.4 characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Prf	Maximum output power ⁽¹⁾	SMPS Bypass or ON ($V_{FBSMPS} = 1.7 \text{ V}$ and $V_{DD} > 1.95 \text{ V}$)	-	5.7	-	dBm
		SMPS Bypass ($V_{DD} > 1.71 \text{ V}$) or ON ($V_{FBSMPS} = 1.4 \text{ V}$ and $V_{DD} > 1.95 \text{ V}$)	-	3.7	-	
	0 dBm output power	-	-	0	-	
	Minimum output power	-	-	-20	-	
Pband	Output power variation over the band	Tx = 0 dBm - Typical	-0.5	-	0.4	dB
EVMrms	EVM rms	Pmax	-	8	-	%
Txpd	Transmit power density	$ f - fc > 3.5 \text{ MHz}$	-	-35	-	dB

1. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50Ω antenna.

Table 32. RF receiver 802.15.4 characteristics

Symbol	Parameter	Conditions	Typ	Unit
Prx_max	Maximum input signal	Min: -20 dBm and PER < 1%	-10	dBm
Rsens	Sensitivity (SMPS Bypass)	Max: -85 dBm and PER < 1%	-100	
	Sensitivity (SMPS ON)		-98	
C/adj	Adjacent channel rejection	-	35	dB
C/alt	Alternate channel rejection	-	46	

Figure 19. Typical link quality indicator code vs. Rx level

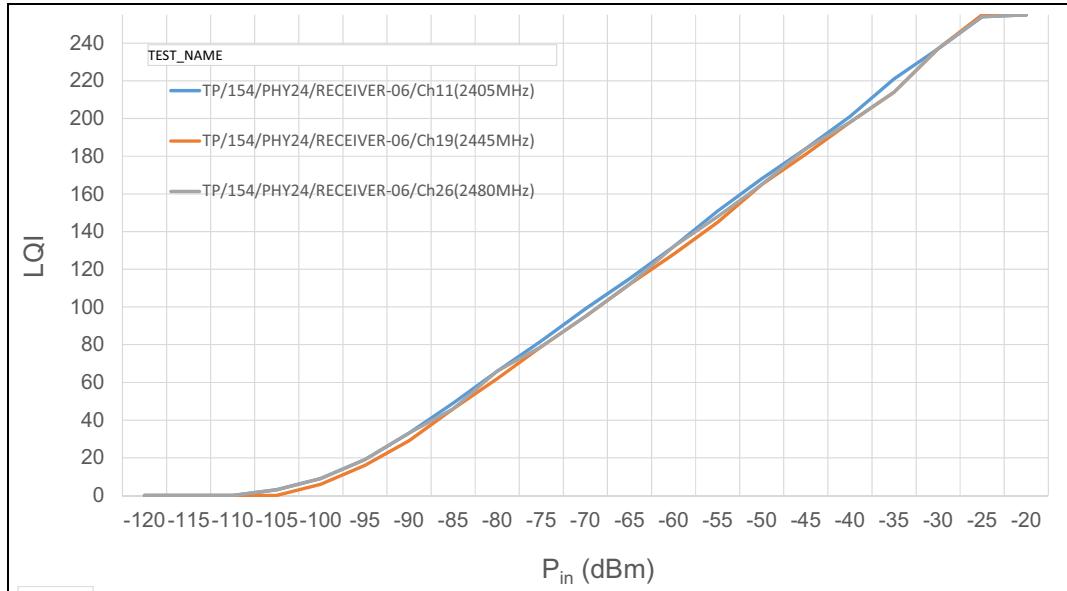


表31. RF 发射器 802.15.4 特性 (继续)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Prf	Maximum output power ⁽¹⁾	SMPS Bypass or ON ($V_{FBSMPS} = 1.7 \text{ V}$ and $V_{DD} > 1.95 \text{ V}$)	-	5.7	-	dBm
		SMPS Bypass ($V_{DD} > 1.71 \text{ V}$) or ON ($V_{FBSMPS} = 1.4 \text{ V}$ and $V_{DD} > 1.95 \text{ V}$)	-	3.7	-	
	0 dBm output power	-	-	0	-	
	Minimum output power	-	-	-20	-	
Pband	Output power variation over the band	Tx = 0 dBm - Typical	-0.5	-	0.4	dB
EVMrms	EVM rms	Pmax	-	8	-	%
Txpd	Transmit power density	$ f - fc > 3.5 \text{ MHz}$	-	-35	-	dB

1. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50Ω antenna.

表32. RF 接收器 802.15.4 特性

Symbol	Parameter	Conditions	Typ	Unit
Prx_max	Maximum input signal	Min: -20 dBm and PER < 1%	-10	dBm
Rsens	Sensitivity (SMPS Bypass)	Max: -85 dBm and PER < 1%	-100	
	Sensitivity (SMPS ON)		-98	
C/adj	Adjacent channel rejection	-	35	dB
C/alt	Alternate channel rejection	-	46	

图19. 典型链路质量指标代码与接收级别比较

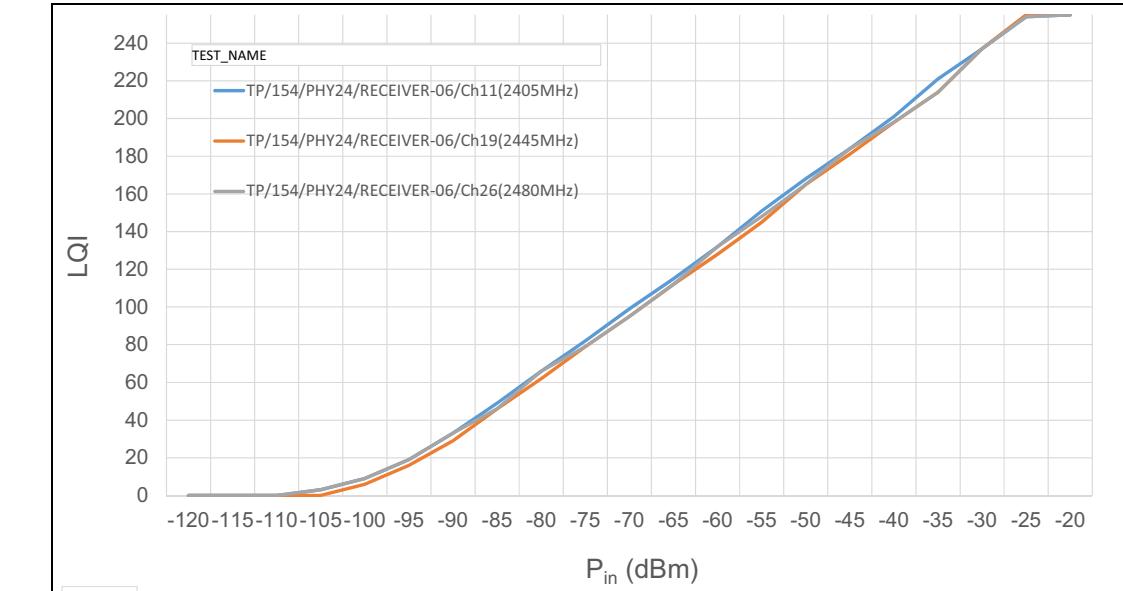
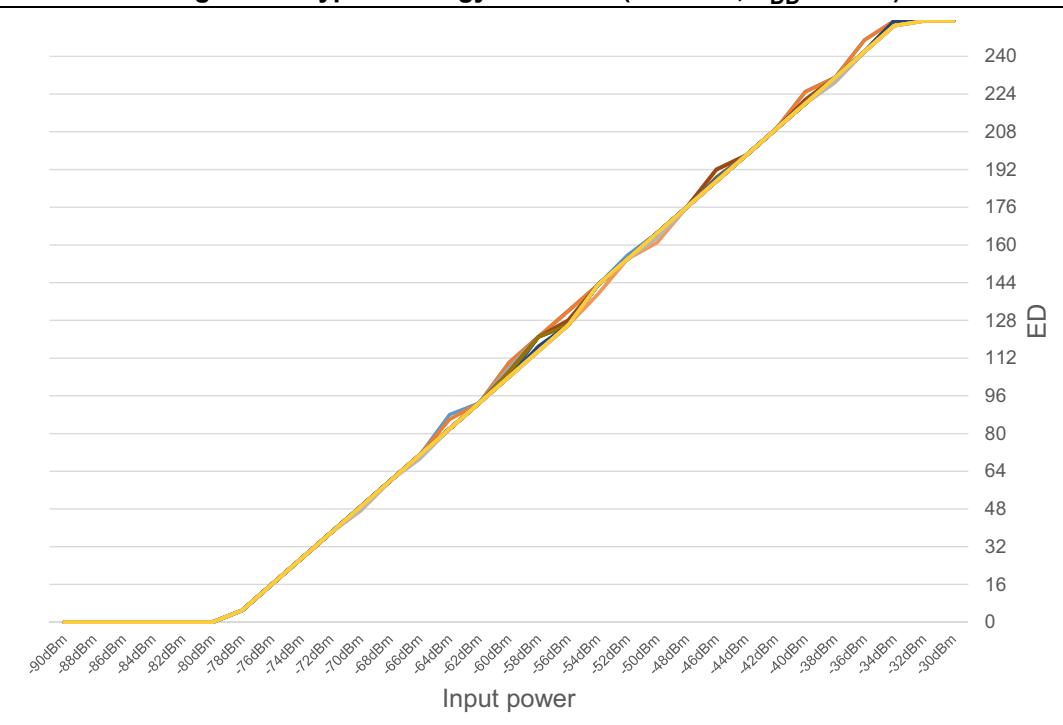
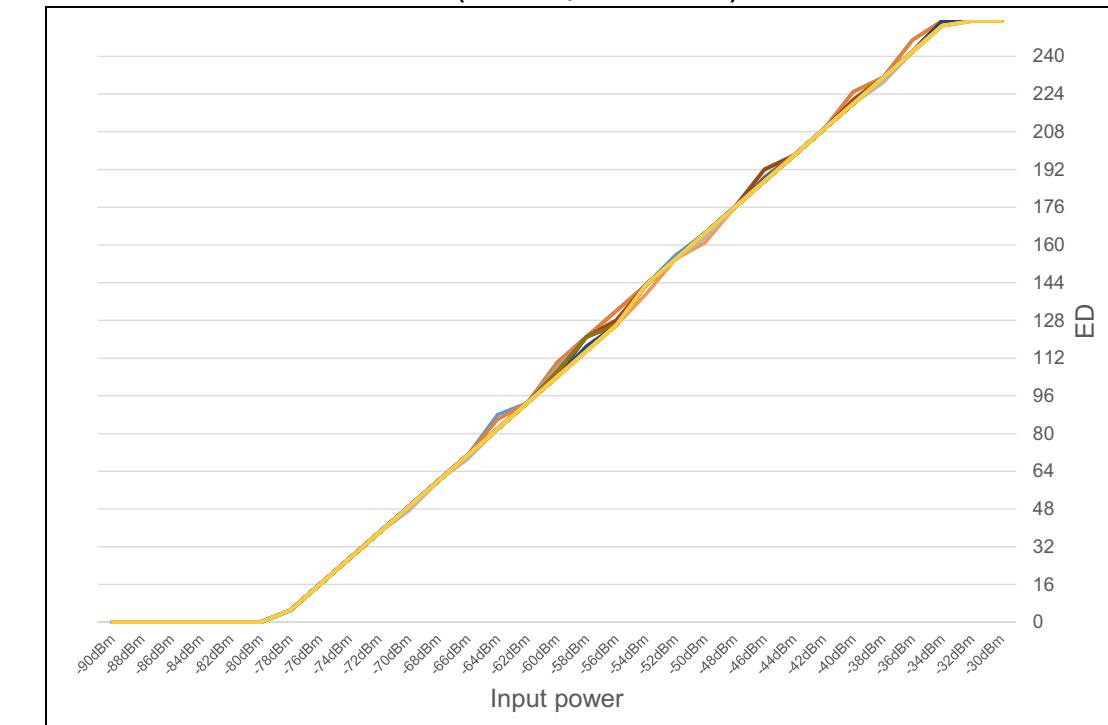


Figure 20. Typical energy detection ($T = 27^\circ\text{C}$, $V_{\text{DD}} = 3.3 \text{ V}$)Table 33. RF 802.15.4 power consumption for $V_{\text{DD}} = 3.3 \text{ V}^{(1)}$

Symbol	Parameter	Typ	Unit
I_{txmax}	TX maximum output power consumption (SMPS Bypass)	11.7	mA
	TX maximum output power consumption (SMPS On, $V_{\text{FBSPS}} = 1.7 \text{ V}$)	6.5	
I_{tx0dbm}	TX 0 dBm output power consumption (SMPS Bypass)	9.1	mA
	TX 0 dBm output power consumption (SMPS On, $V_{\text{FBSPS}} = 1.4 \text{ V}$)	4.5	
I_{rxlo}	Rx consumption (SMPS Bypass)	9.2	mA
	Rx consumption (SMPS On)	4.5	

1. Power consumption including RF subsystem and digital processing.

图20. 典型能量检测 ($T = 27^\circ\text{C}$, $V_{\text{DD}} = 3.3 \text{ V}$)表33. RF 802.15.4 功率消耗 для $V_{\text{DD}} = 3.3 \text{ V}^{(1)}$

Symbol	Parameter	Typ	Unit
I_{txmax}	TX maximum output power consumption (SMPS Bypass)	11.7	mA
	TX maximum output power consumption (SMPS On, $V_{\text{FBSPS}} = 1.7 \text{ V}$)	6.5	
I_{tx0dbm}	TX 0 dBm output power consumption (SMPS Bypass)	9.1	mA
	TX 0 dBm output power consumption (SMPS On, $V_{\text{FBSPS}} = 1.4 \text{ V}$)	4.5	
I_{rxlo}	Rx consumption (SMPS Bypass)	9.2	mA
	Rx consumption (SMPS On)	4.5	

1. Power consumption including RF subsystem and digital processing.

6.3.5 Operating conditions at power-up / power-down

The parameters given in [Table 34](#) are derived from tests performed under the ambient temperature condition summarized in [Table 24](#).

Table 34. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	-	∞	$\mu s/V$
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	$\mu s/V$
	V_{DDA} fall time rate		10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	-	0	∞	$\mu s/V$
	V_{DDUSB} fall time rate		10	∞	
t_{VDDRF}	V_{DDRF} rise time rate	-	-	∞	$\mu s/V$
	V_{DDRF} fall time rate		-	∞	

6.3.6 Embedded reset and power control block characteristics

The parameters given in [Table 35](#) are derived from tests performed under the ambient temperature conditions summarized in [Table 24: General operating conditions](#).

Table 35. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Unit	
$t_{RSTTEMPO}^{(2)}$	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	μs	
$V_{BOR0}^{(2)}$	Brown-out reset threshold 0		Rising edge	1.62	1.66	1.70	
			Falling edge	1.60	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1		Rising edge	2.06	2.10	2.14	
			Falling edge	1.96	2.00	2.04	
V_{BOR2}	Brown-out reset threshold 2		Rising edge	2.26	2.31	2.35	
			Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3		Rising edge	2.56	2.61	2.66	
			Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4		Rising edge	2.85	2.90	2.95	
			Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0		Rising edge	2.10	2.15	2.19	
			Falling edge	2.00	2.05	2.10	
V_{PVD1}	PVD threshold 1		Rising edge	2.26	2.31	2.36	
			Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2		Rising edge	2.41	2.46	2.51	
			Falling edge	2.31	2.36	2.41	

6.3.5 上电/下电工作条件

The parameters given in [表 34](#) are derived from tests performed under the ambienttemperature condition summarized in [表 24](#).

Table 34. 上电/下电工作条件

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	-	∞	$\mu s/V$
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	$\mu s/V$
	V_{DDA} fall time rate		10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	-	0	∞	$\mu s/V$
	V_{DDUSB} fall time rate		10	∞	
t_{VDDRF}	V_{DDRF} rise time rate	-	-	∞	$\mu s/V$
	V_{DDRF} fall time rate		-	∞	

6.3.6 嵌入式复位和电源控制块特性

给定的参数表35是在表24：通用运行条件中概述的环境温度条件下进行的测试中获得的。

Table 35. 嵌入式复位和电源控制块特性

Symbol	Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Unit	
$t_{RSTTEMPO}^{(2)}$	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	μs	
$V_{BOR0}^{(2)}$	Brown-out reset threshold 0		Rising edge	1.62	1.66	1.70	
			Falling edge	1.60	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1		Rising edge	2.06	2.10	2.14	
			Falling edge	1.96	2.00	2.04	
V_{BOR2}	Brown-out reset threshold 2		Rising edge	2.26	2.31	2.35	
			Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3		Rising edge	2.56	2.61	2.66	
			Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4		Rising edge	2.85	2.90	2.95	
			Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0		Rising edge	2.10	2.15	2.19	
			Falling edge	2.00	2.05	2.10	
V_{PVD1}	PVD threshold 1		Rising edge	2.26	2.31	2.36	
			Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2		Rising edge	2.41	2.46	2.51	
			Falling edge	2.31	2.36	2.41	

Table 35. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Unit
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	
$I_{DD}(\text{BOR_PVD})^{(2)}$	BOR ⁽³⁾ (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	μA
V_{PVM1}	V_{DDUSB} peripheral voltage monitoring	-	1.18	1.22	1.26	V
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	
		Falling edge	1.6	1.64	1.68	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM1}	PVM1 hysteresis	-	-	10	-	
$I_{DD}(\text{PVM1})^{(2)}$	PVM1 consumption from V_{DD}	-	-	0.2	-	μA
$I_{DD}(\text{PVM3})^{(2)}$	PVM3 consumption from V_{DD}	-	-	2	-	

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

2. Guaranteed by design.

3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

表35. 嵌入式复位和电源控制块特性 (继续)

Symbol	Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Unit
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	
$I_{DD}(\text{BOR_PVD})^{(2)}$	BOR ⁽³⁾ (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	μA
V_{PVM1}	V_{DDUSB} peripheral voltage monitoring	-	1.18	1.22	1.26	V
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	
		Falling edge	1.6	1.64	1.68	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM1}	PVM1 hysteresis	-	-	10	-	
$I_{DD}(\text{PVM1})^{(2)}$	PVM1 consumption from V_{DD}	-	-	0.2	-	μA
$I_{DD}(\text{PVM3})^{(2)}$	PVM3 consumption from V_{DD}	-	-	2	-	

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

2. Guaranteed by design.

3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

6.3.7 Embedded voltage reference

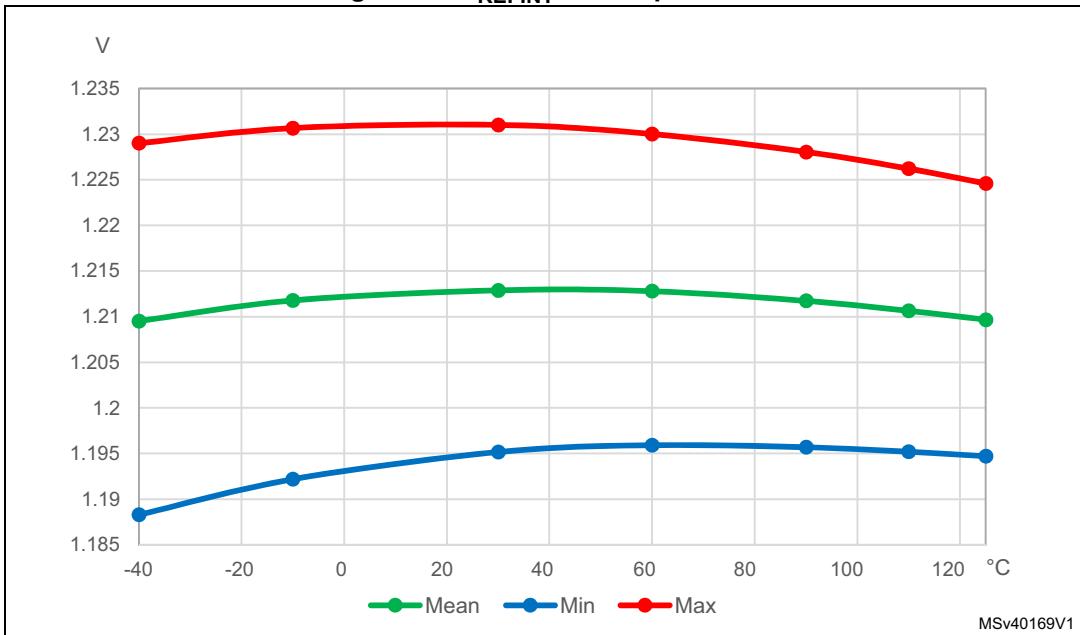
The parameters given in [Table 36](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 36. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$	1.182	1.212	1.232	V
$t_{S_vrefint}^{(1)}$	ADC sampling time when reading the internal reference voltage	-	4 ⁽²⁾	-	-	μs
$t_{start_vrefint}$	Start time of reference voltage buffer when ADC is enabled	-	-	8	12 ⁽²⁾	
$I_{DD(V_{REFINTBUF})}$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20 ⁽²⁾	μA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	$V_{DD} = 3\text{ V}$	-	5	7.5 ⁽²⁾	mV
T_{Coeff}	Temperature coefficient	$-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$	-	30	50 ⁽²⁾	ppm/°C
A_{Coeff}	Long term stability	1000 hours, $T = 25^{\circ}\text{C}$	-	300	1000 ⁽²⁾	ppm
$V_{DDCoeff}$	Voltage coefficient	$3.0\text{ V} < V_{DD} < 3.6\text{ V}$	-	250	1200 ⁽²⁾	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	%
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	V_{REFINT}

1. The shortest sampling time can be determined in the application by multiple iterations.

2. Guaranteed by design.

Figure 21. V_{REFINT} vs. temperature

6.3.7 内置电压参考

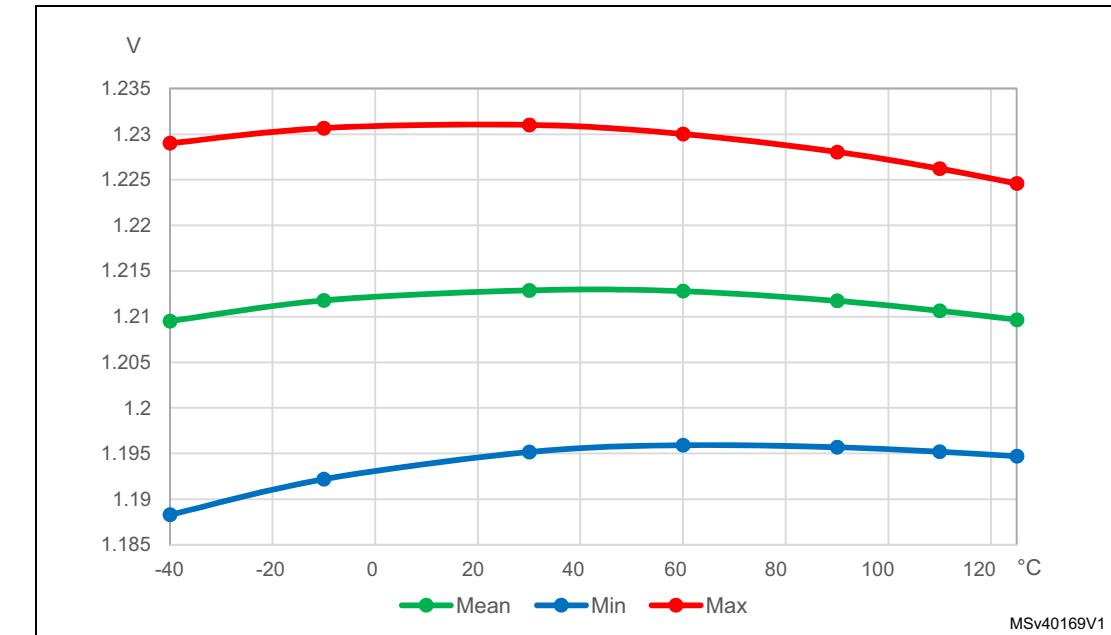
给定的参数在表 36 中，是在表 24：通用运行条件中总结的环境温度和供电电压条件下进行测试获得的。

表 36. 嵌入式内部电压参考

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$	1.182	1.212	1.232	V
$t_{S_vrefint}^{(1)}$	ADC sampling time when reading the internal reference voltage	-	4 ⁽²⁾	-	-	μs
$t_{start_vrefint}$	Start time of reference voltage buffer when ADC is enabled	-	-	8	12 ⁽²⁾	
$I_{DD(V_{REFINTBUF})}$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20 ⁽²⁾	μA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	$V_{DD} = 3\text{ V}$	-	5	7.5 ⁽²⁾	mV
T_{Coeff}	Temperature coefficient	$-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$	-	30	50 ⁽²⁾	ppm/°C
A_{Coeff}	Long term stability	1000 hours, $T = 25^{\circ}\text{C}$	-	300	1000 ⁽²⁾	ppm
$V_{DDCoeff}$	Voltage coefficient	$3.0\text{ V} < V_{DD} < 3.6\text{ V}$	-	250	1200 ⁽²⁾	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	%
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	V_{REFINT}

1. The shortest sampling time can be determined in the application by multiple iterations.

2. Guaranteed by design.

图 21. V_{REFINT} 与温度比较

6.3.8 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 18: Current consumption measurement scheme](#).

Typical and maximum current consumption

The MCU is put under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$
- For Flash memory and shared peripherals $f_{PCLK} = f_{HCLK} = f_{HCLKS}$

The parameters given in [Table 37](#) to [Table 48](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

6.3.8 电源电流特性

电流消耗是一个函数，取决于多个参数和因素，例如工作电压、环境温度、I/O引脚负载、设备软件配置、工作频率、I/O引脚切换速率、程序在内存中的位置和执行的二进制代码。

The current consumption is measured as described in [Figure 18: Current consumption measurement scheme](#).

Typical and maximum current consumption

The MCU is put under the following conditions:

STM32WB55xx STM32WB35xx典型和最大电流消耗
 • 所有 I/O 引脚都处于模拟输入模式
 • 除非明确说明，否则所有外围设备都已禁用
 • 闪存内存访问时间根据 f_{HCLK} 频率调整为最小的等待状态数(参考表“CPU 时钟对应的等待状态数(HCLK 频率”在参考手册中可用))。
 • 当外围设备启用时, $f_{PCLK} = f_{HCLK}$
 • 为闪存内存和共享外围设备, $f_{PCLK} = f_{HCLK} = f_{HCLKS}$

The parameters given in [Table 37](#) to [Table 48](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 37. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF), $V_{DD} = 3.3$ V

Symbol	Parameter	Conditions		Typ				Max ⁽¹⁾			Unit	
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
$I_{DD}(\text{Run})$	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HCLK} = f_{HSE} = 32$ MHz $f_{HSI16} + \text{PLL ON}$ above 32 MHz All peripherals disabled	Range 2	16 MHz	1.90	1.90	2.00	2.20	2.40	2.52	2.96	mA
				2 MHz	0.960	0.985	1.10	1.25	1.25	1.57	2.05	
			Range 1	64 MHz	8.15	8.25	8.40	8.60	9.30	9.60	10.02	
				32 MHz	4.20	4.25	4.40	4.65	4.25	4.63	5.17	
				16 MHz	2.25	2.30	2.40	2.65	2.65	2.91	3.52	
			SMPS Range 1	64 MHz	5.00	5.00	5.10	5.20	-	-	-	
				32 MHz	3.15	3.15	3.25	3.35	-	-	-	
				16 MHz	2.30	2.30	2.35	2.45	-	-	-	
$I_{DD}(\text{LPRun})$	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled	2 MHz	0.335	0.360	0.470	0.670	0.480	0.910	1.47	mA	
			1 MHz	0.170	0.210	0.325	0.520	0.270	0.730	1.31		
			400 kHz	0.0815	0.120	0.230	0.425	0.140	0.590	1.18		
			100 kHz	0.0415	0.076	0.190	0.385	0.070	0.550	1.14		

1. Guaranteed by characterization results, unless otherwise specified.



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Table 37. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF), $V_{DD} = 3.3$ V

Symbol	Parameter	Conditions		Typ				Max ⁽¹⁾			Unit	
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
$I_{DD}(\text{Run})$	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HCLK} = f_{HSE} = 32$ MHz $f_{HSI16} + \text{PLL ON}$ above 32 MHz All peripherals disabled	Range 2	16 MHz	1.90	1.90	2.00	2.20	2.40	2.52	2.96	mA
				2 MHz	0.960	0.985	1.10	1.25	1.25	1.57	2.05	
			Range 1	64 MHz	8.15	8.25	8.40	8.60	9.30	9.60	10.02	
				32 MHz	4.20	4.25	4.40	4.65	4.25	4.63	5.17	
				16 MHz	2.25	2.30	2.40	2.65	2.65	2.91	3.52	
			SMPS Range 1	64 MHz	5.00	5.00	5.10	5.20	-	-	-	
				32 MHz	3.15	3.15	3.25	3.35	-	-	-	
				16 MHz	2.30	2.30	2.35	2.45	-	-	-	
$I_{DD}(\text{LPRun})$	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled	2 MHz	0.335	0.360	0.470	0.670	0.480	0.910	1.47	mA	
			1 MHz	0.170	0.210	0.325	0.520	0.270	0.730	1.31		
			400 kHz	0.0815	0.120	0.230	0.425	0.140	0.590	1.18		
			100 kHz	0.0415	0.076	0.190	0.385	0.070	0.550	1.14		

1. Guaranteed by characterization results unless otherwise specified.



Table 38. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, $V_{DD} = 3.3\text{ V}$

Symbol	Parameter	Conditions			Typ			Max ⁽¹⁾			Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	
$I_{DD(\text{Run})}$	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HCLK} = f_{HSE} = 32\text{ MHz}$ $f_{HSI16} + \text{PLL ON}$ above 32 MHz All peripherals disabled	Range 2	16 MHz	2.00	2.05	2.15	2.30	2.57	3.04	3.64
				2 MHz	0.970	1.00	1.10	1.25	1.62	1.90	2.55
			Range 1	64 MHz	8.80	8.90	9.00	9.20	10.50	10.80	11.30
				32 MHz	4.50	4.55	4.70	4.90	4.63	4.89	5.62
			SMPS Range 1	16 MHz	2.40	2.40	2.55	2.70	2.50	2.70	3.21
				64 MHz	5.25	5.30	5.35	5.45	-	-	-
				32 MHz	3.25	3.25	3.35	3.45	-	-	-
				16 MHz	2.35	2.35	2.40	2.45	-	-	-
			Supply current in Low-power run mode	2 MHz	0.265	0.285	0.385	0.550	0.440	0.940	1.620
				1 MHz	0.135	0.170	0.270	0.430	0.290	0.760	1.480
				400 kHz	0.066	0.097	0.195	0.360	0.200	0.670	1.380
				100 kHz	0.031	0.0625	0.160	0.325	0.170	0.470	1.330

1. Guaranteed by characterization results, unless otherwise specified.

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Table 38. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, $V_{DD} = 3.3\text{ V}$

Symbol	Parameter	Conditions			Typ			Max ⁽¹⁾			Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	
$I_{DD(\text{Run})}$	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HCLK} = f_{HSE} = 32\text{ MHz}$ $f_{HSI16} + \text{PLL ON}$ above 32 MHz All peripherals disabled	Range 2	16 MHz	2.00	2.05	2.15	2.30	2.57	3.04	3.64
				2 MHz	0.970	1.00	1.10	1.25	1.62	1.90	2.55
			Range 1	64 MHz	8.80	8.90	9.00	9.20	10.50	10.80	11.30
				32 MHz	4.50	4.55	4.70	4.90	4.63	4.89	5.62
			SMPS Range 1	16 MHz	2.40	2.40	2.55	2.70	2.50	2.70	3.21
				64 MHz	5.25	5.30	5.35	5.45	-	-	-
				32 MHz	3.25	3.25	3.35	3.45	-	-	-
				16 MHz	2.35	2.35	2.40	2.45	-	-	-
			Supply current in Low-power run mode	2 MHz	0.265	0.285	0.385	0.550	0.440	0.940	1.620
				1 MHz	0.135	0.170	0.270	0.430	0.290	0.760	1.480
				400 kHz	0.066	0.097	0.195	0.360	0.200	0.670	1.380
				100 kHz	0.031	0.0625	0.160	0.325	0.170	0.470	1.330

1. Guaranteed by characterization results, unless otherwise specified.

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Table 39. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF), V_{DD}= 3.3 V

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I _{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HSI16} + PLL$ ON above 32 MHz All peripherals disable	Range 1, SMPS On $f_{HCLK} = 64$ MHz, When RF Tx level = 0 dBm ⁽²⁾	Range 1, SMPS On $f_{HCLK} = 64$ MHz	Range 2 $f_{HCLK} = 16$ MHz	mA	Reduced code ⁽¹⁾	1.90
							Coremark	1.85
							Dhrystone 2.1	1.85
							Fibonacci	1.75
							While(1)	1.60
			mA	Range 1 $f_{HCLK} = 64$ MHz	Range 2 $f_{HCLK} = 16$ MHz	μA/MHz	Reduced code ⁽¹⁾	8.15
							Coremark	8.00
							Dhrystone 2.1	8.10
							Fibonacci	7.60
							While(1)	6.85
I _{DD} (LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI} = 2$ MHz All peripherals disable	$f_{HCLK} = f_{MSI} = 2$ MHz All peripherals disable	$f_{HCLK} = f_{MSI} = 2$ MHz When RF Tx level = 0 dBm ⁽²⁾	Range 1, SMPS On $f_{HCLK} = 64$ MHz, When RF Tx level = 0 dBm ⁽²⁾	Range 1, SMPS On $f_{HCLK} = 64$ MHz	Range 2 $f_{HCLK} = 16$ MHz	μA/MHz

1. Reduced code used for characterization results provided in [Table 37](#) and [Table 38](#).

2. Value computed. MCU consumption when RF TX and SMPS are ON.

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表39. 典型电流消耗在运行和低功率运行模式下，不同代码从闪存运行，ART启用 (缓存开启预取关闭)，VDD= 3.3 V

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I _{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HSI16} + PLL$ ON above 32 MHz All peripherals disable	Range 1, SMPS On $f_{HCLK} = 64$ MHz, When RF Tx level = 0 dBm ⁽²⁾	Range 1, SMPS On $f_{HCLK} = 64$ MHz	Range 2 $f_{HCLK} = 16$ MHz	mA	Reduced code ⁽¹⁾	1.90
							Coremark	1.85
							Dhrystone 2.1	1.85
							Fibonacci	1.75
							While(1)	1.60
			mA	Range 1 $f_{HCLK} = 64$ MHz	Range 2 $f_{HCLK} = 16$ MHz	μA/MHz	Reduced code ⁽¹⁾	8.15
							Coremark	8.00
							Dhrystone 2.1	8.10
							Fibonacci	7.60
							While(1)	6.85
I _{DD} (LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI} = 2$ MHz All peripherals disable	$f_{HCLK} = f_{MSI} = 2$ MHz All peripherals disable	$f_{HCLK} = f_{MSI} = 2$ MHz When RF Tx level = 0 dBm ⁽²⁾	Range 1, SMPS On $f_{HCLK} = 64$ MHz, When RF Tx level = 0 dBm ⁽²⁾	Range 1, SMPS On $f_{HCLK} = 64$ MHz	Range 2 $f_{HCLK} = 16$ MHz	μA/MHz

1. Reduced code used for characterization results provided in [Table 37](#) and [Table 38](#).

2. Value computed. MCU consumption when RF TX and SMPS are ON.

Table 40. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1, $V_{DD} = 3.3\text{ V}$

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
$I_{DD}(\text{Run})$	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HSI16} + \text{PLL ON}$ above 32 MHz All peripherals disable	Range 2 $f_{HCLK} = 16\text{ MHz}$	Reduced code ⁽¹⁾	2.00	mA	125	$\mu\text{A}/\text{MHz}$
				Coremark	1.75		109	
				Dhrystone 2.1	1.95		122	
				Fibonacci	1.85		116	
				While(1)	1.85		116	
			Range 1 $f_{HCLK} = 64\text{ MHz}$	Reduced code ⁽¹⁾	8.80	mA	138	$\mu\text{A}/\text{MHz}$
				Coremark	7.50		117	
				Dhrystone 2.1	8.60		134	
				Fibonacci	7.90		123	
				While(1)	8.00		125	
			Range 1, SMPS On $f_{HCLK} = 64\text{ MHz}$	Reduced code ⁽¹⁾	5.25	mA	82	$\mu\text{A}/\text{MHz}$
				Coremark	4.65		73	
				Dhrystone 2.1	5.15		80	
				Fibonacci	4.85		76	
				While(1)	4.90		77	
			Range 1, SMPS On $f_{HCLK} = 64\text{ MHz}$, When RF TX level = 0 dBm ⁽²⁾	Reduced code ⁽¹⁾	4.39	mA	69	$\mu\text{A}/\text{MHz}$
				Coremark	3.74		58	
				Dhrystone 2.1	4.29		67	
				Fibonacci	3.94		62	
				While(1)	3.99		62	
$I_{DD}(\text{LPRun})$	Supply current in Low-power run	$f_{HCLK} = f_{MSI} = 2\text{ MHz}$ All peripherals disable	μA	Reduced code ⁽¹⁾	255		128	$\mu\text{A}/\text{MHz}$
				Coremark	205		103	
				Dhrystone 2.1	250		125	
				Fibonacci	230		115	
				While(1)	220		110	

1. Reduced code used for characterization results provided in [Table 37](#) and [Table 38](#).

2. Value computed. MCU consumption when RF TX and SMPS are ON.

表40. 典型电流消耗在运行和低功率运行模式下，不同代码从SRAM1运行， $V_{DD} = 3.3\text{ V}$

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
$I_{DD}(\text{Run})$	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HSI16} + \text{PLL ON}$ above 32 MHz All peripherals disable	Range 2 $f_{HCLK} = 16\text{ MHz}$	Reduced code ⁽¹⁾	2.00	mA	125	$\mu\text{A}/\text{MHz}$
				Coremark	1.75		109	
				Dhrystone 2.1	1.95		122	
				Fibonacci	1.85		116	
				While(1)	1.85		116	
			Range 1 $f_{HCLK} = 64\text{ MHz}$	Reduced code ⁽¹⁾	8.80	mA	138	$\mu\text{A}/\text{MHz}$
				Coremark	7.50		117	
				Dhrystone 2.1	8.60		134	
				Fibonacci	7.90		123	
				While(1)	8.00		125	
			Range 1, SMPS On $f_{HCLK} = 64\text{ MHz}$	Reduced code ⁽¹⁾	5.25	mA	82	$\mu\text{A}/\text{MHz}$
				Coremark	4.65		73	
				Dhrystone 2.1	5.15		80	
				Fibonacci	4.85		76	
				While(1)	4.90		77	
			Range 1, SMPS On $f_{HCLK} = 64\text{ MHz}$, When RF TX level = 0 dBm ⁽²⁾	Reduced code ⁽¹⁾	4.39	mA	69	$\mu\text{A}/\text{MHz}$
				Coremark	3.74		58	
				Dhrystone 2.1	4.29		67	
				Fibonacci	3.94		62	
				While(1)	3.99		62	
$I_{DD}(\text{LPRun})$	Supply current in Low-power run	$f_{HCLK} = f_{MSI} = 2\text{ MHz}$ All peripherals disable	μA	Reduced code ⁽¹⁾	255		128	$\mu\text{A}/\text{MHz}$
				Coremark	205		103	
				Dhrystone 2.1	250		125	
				Fibonacci	230		115	
				While(1)	220		110	

1. Reduced code used for characterization results provided in [Table 37](#) and [Table 38](#).

2. Value computed. MCU consumption when RF TX and SMPS are ON.

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Table 41. Current consumption in Sleep and Low-power sleep modes, Flash memory ON

Symbol	Parameter	Conditions			TYP				MAX ⁽¹⁾			Unit
		-	Voltage scaling	f _{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I _{DD} (Sleep)	Supply current in sleep mode, f _{HCLK} = f _{HSI16} up to 16 MHz included, f _{HCLK} = f _{HSE} up to 32 MHz f _{HSI16} + PLL ON above 32 MHz	Range 2	16 MHz	0.740	0.765	0.865	1.05	0.840	1.210	1.810		mA
			64 MHz	2.65	2.70	2.80	3.00	3.00	3.33	3.91		
		Range 1	32 MHz	1.40	1.45	1.60	1.80	1.55	1.86	2.49		
			16 MHz	0.845	0.875	0.990	1.20	0.970	1.40	2.02		
		SMPS Range 1	64 MHz	2.60	2.60	2.65	2.75	-	-	-		
			32 MHz	1.90	1.95	2.00	2.10	-	-	-		
		All peripherals disabled	16 MHz	1.70	1.70	1.75	1.80	-	-	-		
			2 MHz	0.090	0.125	0.235	0.430	0.130	0.600	1.19		
I _{DD} (LPSleep)	Supply current in low-power sleep mode f _{HCLK} = f _{MSI} All peripherals disabled	2 MHz	0.058	0.093	0.205	0.400	0.090	0.570	1.16			mA
			1 MHz	0.044	0.0725	0.185	0.380	0.070	0.540	1.11		
		400 kHz	400 kHz	0.0315	0.0635	0.0175	0.370	0.055	0.530	1.13		

1. Guaranteed by characterization results, unless otherwise specified.

Table 42. Current consumption in Low-power sleep modes, Flash memory in Power down

Symbol	Parameter	Conditions		TYP				MAX ⁽¹⁾			Unit
		-	f _{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I _{DD} (LPSleep)	Supply current in low-power sleep mode f _{HCLK} = f _{MSI} All peripherals disabled	2 MHz	94.0	115	200	335	135	610	1201		μA
			1 MHz	56.5	86.0	170	305	94.2	560	1171	
		400 kHz	40.5	66.5	150	285	68.0	540	1129		
			100 kHz	27.5	57.5	140	275	54.6	539	1131	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 41. Current consumption in Sleep and Low-power sleep modes Flash memory ON

Symbol	Parameter	Conditions			TYP				MAX ⁽¹⁾			Unit
		-	Voltage scaling	f _{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I _{DD} (Sleep)	Supply current in sleep mode, f _{HCLK} = f _{HSI16} up to 16 MHz included, f _{HCLK} = f _{HSE} up to 32 MHz f _{HSI16} + PLL ON above 32 MHz	Range 2	16 MHz	0.740	0.765	0.865	1.05	0.840	1.210	1.810		mA
			64 MHz	2.65	2.70	2.80	3.00	3.00	3.33	3.91		
		Range 1	32 MHz	1.40	1.45	1.60	1.80	1.55	1.86	2.49		
			16 MHz	0.845	0.875	0.990	1.20	0.970	1.40	2.02		
		SMPS Range 1	64 MHz	2.60	2.60	2.65	2.75	-	-	-		
			32 MHz	1.90	1.95	2.00	2.10	-	-	-		
		All peripherals disabled	16 MHz	1.70	1.70	1.75	1.80	-	-	-		
			2 MHz	0.090	0.125	0.235	0.430	0.130	0.600	1.19		
I _{DD} (LPSleep)	Supply current in low-power sleep mode f _{HCLK} = f _{MSI} All peripherals disabled	2 MHz	0.058	0.093	0.205	0.400	0.090	0.570	1.16			mA
			1 MHz	0.044	0.0725	0.185	0.380	0.070	0.540	1.11		

1. Guaranteed by characterization results, unless otherwise specified.

Table 42. Current consumption in Low-power sleep modes, Flash memory in Power down

Symbol	Parameter	Conditions		TYP				MAX ⁽¹⁾			Unit
		-	f _{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I _{DD} (LPSleep)	Supply current in low-power sleep mode f _{HCLK} = f _{MSI} All peripherals disabled	2 MHz	94.0	115	200	335	135	610	1201		μA
			1 MHz	56.5	86.0	170	305	94.2	560	1171	
		400 kHz	40.5	66.5	150	285	68.0	540	1129		
			100 kHz	27.5	57.5	140	275	54.6	539	1131	

1. Guaranteed by characterization results, unless otherwise specified.





Table 43. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions		TYP					MAX ⁽¹⁾				Unit	
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I _{DD} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	LCD disabled BLE disabled	1.8 V	1.00	1.85	3.15	5.95	21.5	50.0	1.58	4.12	56.9	132.7	μA
			2.4 V	1.10	1.85	3.20	6.00	22.0	51.0	-	-	-	-	
			3.0 V	1.10	1.85	3.25	6.10	22.0	52.0	1.60	4.17	57.9	135.6	
			3.6 V	1.15	1.95	3.35	6.25	23.0	53.0	1.69	4.40	58.6	135.7	
		LCD enabled ⁽²⁾ and clocked by LSI BLE disabled	1.8 V	1.20	2.00	3.35	6.10	22.0	50.5	1.76	4.30	57.1	133.3	
			2.4 V	1.20	2.00	3.40	6.20	22.0	51.0	-	-	-	-	
			3.0 V	1.25	2.10	3.45	6.30	22.5	52.0	1.85	4.41	58.1	135.8	
			3.6 V	1.30	2.15	3.60	6.55	23.0	53.5	1.97	4.66	59.4	136.6	
I _{DD} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled, BLE disabled	RTC clocked by LSI, LCD disabled	1.8 V	1.30	2.10	3.45	6.25	22.0	50.5	1.91	4.50	57.2	133.0	μA
			2.4 V	1.45	2.25	3.55	6.40	22.5	51.5	-	-	-	-	
			3.0 V	1.50	2.30	3.70	6.55	22.5	52.5	2.11	4.64	58.3	136.1	
			3.6 V	1.75	2.50	3.95	6.85	23.5	53.5	2.26	5.12	59.7	136.9	
		RTC clocked by LSI, LCD enabled ⁽²⁾	1.8 V	1.35	2.20	3.55	6.30	22.0	50.5	1.99	4.57	57.4	133.8	
			2.4 V	1.50	2.35	3.65	6.50	22.5	51.5	-	-	-	-	
			3.0 V	1.70	2.45	3.85	6.65	23.0	52.5	2.17	4.87	58.4	136.3	
			3.6 V	1.80	2.60	4.05	6.95	23.5	54.0	2.41	5.11	59.9	137.1	
		RTC clocked by LSE quartz ⁽³⁾ in low drive mode	1.8 V	1.35	2.20	3.50	6.25	22.0	50.5	1.91	4.29	57.1	133.5	
			2.4 V	1.45	2.25	3.65	6.40	22.5	51.5	-	-	-	-	
			3.0 V	1.55	2.45	3.80	6.65	23.0	52.5	2.01	4.31	58.0	135.9	
			3.6 V	1.70	2.55	4.05	6.95	23.5	54.0	2.16	4.40	81.6	137.0	

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Table 43. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions		TYP					MAX ⁽¹⁾				Unit	
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I _{DD} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	LCD disabled BLE disabled	1.8 V	1.00	1.85	3.15	5.95	21.5	50.0	1.58	4.12	56.9	132.7	μA
			2.4 V	1.10	1.85	3.20	6.00	22.0	51.0	-	-	-	-	
			3.0 V	1.10	1.85	3.25	6.10	22.0	52.0	1.60	4.17	57.9	135.6	
			3.6 V	1.15	1.95	3.35	6.25	23.0	53.0	1.69	4.40	58.6	135.7	
		LCD enabled ⁽²⁾ and clocked by LSI BLE disabled	1.8 V	1.20	2.00	3.35	6.10	22.0	50.5	1.76	4.30	57.1	133.3	
			2.4 V	1.20	2.00	3.40	6.20	22.0	51.0	-	-	-	-	
			3.0 V	1.25	2.10	3.45	6.30	22.5	52.0	1.85	4.41	58.1	135.8	
			3.6 V	1.30	2.15	3.60	6.55	23.0	53.5	1.97	4.66	59.4	136.6	
I _{DD} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled, BLE disabled	RTC clocked by LSI, LCD disabled	1.8 V	1.30	2.10	3.45	6.25	22.0	50.5	1.91	4.50	57.2	133.0	μA
			2.4 V	1.45	2.25	3.55	6.40	22.5	51.5	-	-	-	-	
			3.0 V	1.50	2.30	3.70	6.55	22.5	52.5	2.11	4.64	58.3	136.1	
			3.6 V	1.75	2.50	3.95	6.85	23.5	53.5	2.26	5.12	59.7	136.9	
		RTC clocked by LSI, LCD enabled ⁽²⁾	1.8 V	1.35	2.20	3.55	6.30	22.0	50.5	1.99	4.57	57.4	133.8	
			2.4 V	1.50	2.35	3.65	6.50	22.5	51.5	-	-	-	-	
			3.0 V	1.70	2.45	3.85	6.65	23.0	52.5	2.17	4.87	58.4	136.3	
			3.6 V	1.80	2.60	4.05	6.95	23.5	54.0	2.41	5.11	59.9	137.1	
		RTC clocked by LSE quartz ⁽³⁾ in low drive mode	1.8 V	1.35	2.20	3.50	6.25	22.0	50.5	1.91	4.29	57.1	133.5	
			2.4 V	1.45	2.25	3.65	6.40	22.5	51.5	-	-	-	-	
			3.0 V	1.55	2.45	3.80	6.65	23.0	52.5	2.01	4.31	58.0	135.9	
			3.6 V	1.70	2.55	4.05	6.95	23.5	54.0	2.16	4.40	81.6	137.0	

Symbol	Parameter	Conditions		TYP					MAX ⁽¹⁾					Unit
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I _{DD} (wakeup from Stop 2)	Supply current during wakeup from Stop 2 mode bypass mode	Wakeup clock is HSI16, voltage Range 2. See ⁽⁴⁾ .	3.0 V	-	389	-	-	-	-	-	-	-	-	μA
		Wakeup clock is MSI = 32 MHz, voltage Range 1. See ⁽⁴⁾ .	3.0 V	-	320	-	-	-	-	-	-	-	-	
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See ⁽⁴⁾ .	3.0 V	-	528	-	-	-	-	-	-	-	-	

- Guaranteed based on test during characterization, unless otherwise specified.
- LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}
- Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
- Wakeup with code execution from Flash memory. Average value given for a typical wakeup time as specified in [Table 51: Low-power mode wakeup timings](#).

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Symbol	Parameter	Conditions		TYP					MAX ⁽¹⁾					Unit
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I _{DD} (wakeup from Stop 2)	Supply current during wakeup from Stop 2 mode bypass mode	Wakeup clock is HSI16, voltage Range 2. See ⁽⁴⁾ .	3.0 V	-	389	-	-	-	-	-	-	-	-	μA
		Wakeup clock is MSI = 32 MHz, voltage Range 1. See ⁽⁴⁾ .	3.0 V	-	320	-	-	-	-	-	-	-	-	
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See ⁽⁴⁾ .	3.0 V	-	528	-	-	-	-	-	-	-	-	

- Guaranteed based on test during characterization, unless otherwise specified.
- LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}
- Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
- Wakeup with code execution from Flash memory. Average value given for a typical wakeup time as specified in [Table 51: Low-power mode wakeup timings](#).

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Symbol	Parameter	Conditions		TYP						MAX ⁽¹⁾				Unit	
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C		
I _{DD} (Stop 1)	Supply current in Stop 1 mode, RTC disabled	BLE disabled LCD disabled	1.8 V	5.05	9.20	15.5	28.0	96.0	210	7.00	28.4	343.7	738.6	μA	
			2.4 V	5.10	9.25	15.5	28.5	96.5	215	-	-	-	-		
			3.0 V	5.15	9.30	15.5	28.5	97.0	215	7.07	28.5	346.8	746.0		
			3.6 V	5.25	9.45	16.0	29.0	97.5	215	7.30	28.8	351.0	749.4		
		BLE disabled LCD enabled ⁽²⁾ , clocked by LSI	1.8 V	5.05	9.30	15.5	28.5	96.0	210	7.10	28.7	344.4	739.0		
			2.4 V	5.10	9.35	16.0	28.5	96.5	215	-	-	-	-		
			3.0 V	5.20	9.65	16.0	28.5	97.0	215	7.26	29.6	345.0	747.0		
			3.6 V	5.55	9.85	16.0	29.0	98.5	215	7.62	29.8	349.0	750.8		
	I _{DD} (Stop 1 with RTC)	Supply current in Stop 1 mode, RTC enabled, BLE disabled	RTC clocked by LSI LCD disabled	1.8 V	5.30	9.35	16.0	28.5	96.5	215	7.30	29.5	343.7	739.2	μA
				2.4 V	5.40	9.45	16.0	28.5	97.0	215	-	-	-	-	
				3.0 V	5.70	9.55	16.5	29.0	98.5	220	7.69	29.7	347.2	746.1	
				3.6 V	5.85	10.0	16.5	29.5	96.5	215	8.08	29.8	349.9	751.1	
			RTC clocked by LSI LCD enabled ⁽²⁾	1.8 V	5.25	9.60	16.0	28.5	96.5	215	7.10	29.0	344.3	739.9	
				2.4 V	5.30	9.75	16.0	29.0	97.0	215	-	-	-	-	
				3.0 V	5.85	9.80	16.5	29.0	97.5	215	7.53	29.8	347.4	746.2	
				3.6 V	5.90	10.5	16.5	29.0	98.5	220	8.18	29.9	350.6	751.8	
		RTC clocked by LSE quartz ⁽³⁾ in Low drive mode	1.8 V	5.35	9.55	16.0	28.5	96.5	215	6.00	28.7	343.9	738.7		
			2.4 V	5.40	9.70	16.0	29.0	96.5	215	-	-	-	-		
			3.0 V	5.75	9.70	16.0	29.0	97.5	215	7.40	28.9	346.6	743.8		
			3.6 V	5.90	10.0	16.5	29.5	99.0	220	7.58	29.2	349.0	749.9		

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Symbol	Parameter	Conditions		TYP						MAX ⁽¹⁾				Unit	
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C		
I _{DD} (Stop 1)	Supply current in Stop 1 mode, RTC disabled	BLE disabled LCD disabled	1.8 V	5.05	9.20	15.5	28.0	96.0	210	7.00	28.4	343.7	738.6	μA	
			2.4 V	5.10	9.25	15.5	28.5	96.5	215	-	-	-	-		
			3.0 V	5.15	9.30	15.5	28.5	97.0	215	7.07	28.5	346.8	746.0		
			3.6 V	5.25	9.45	16.0	29.0	97.5	215	7.30	28.8	351.0	749.4		
		BLE disabled LCD enabled ⁽²⁾ , clocked by LSI	1.8 V	5.05	9.30	15.5	28.5	96.0	210	7.10	28.7	344.4	739.0		
			2.4 V	5.10	9.35	16.0	28.5	96.5	215	-	-	-	-		
			3.0 V	5.20	9.65	16.0	28.5	97.0	215	7.26	29.6	345.0	747.0		
			3.6 V	5.55	9.85	16.0	29.0	98.5	215	7.62	29.8	349.0	750.8		
	I _{DD} (Stop 1 with RTC)	Supply current in Stop 1 mode, RTC enabled, BLE disabled	RTC clocked by LSI LCD disabled	1.8 V	5.30	9.35	16.0	28.5	96.5	215	7.30	29.5	343.7	739.2	μA
				2.4 V	5.40	9.45	16.0	28.5	97.0	215	-	-	-	-	
				3.0 V	5.70	9.55	16.5	29.0	98.5	220	7.69	29.7	347.2	746.1	
				3.6 V	5.85	10.0	16.5	29.5	96.5	215	8.08	29.8	349.9	751.1	
			RTC clocked by LSI LCD enabled ⁽²⁾	1.8 V	5.25	9.60	16.0	28.5	96.5	215	7.10	29.0	344.3	739.9	
				2.4 V	5.30	9.75	16.0	29.0	97.0	215	-	-	-	-	
				3.0 V	5.85	9.80	16.5	29.0	97.5	215	7.53	29.8	347.4	746.2	
				3.6 V	5.90	10.5	16.5	29.0	98.5	220	8.18	29.9	350.6	751.8	
	I _{DD} (Stop 1 with RTC)	RTC clocked by LSE quartz ⁽³⁾ in Low drive mode	1.8 V	5.35	9.55	16.0	28.5	96.5	215	6.00	28.7	343.9	738.7	μA	
			2.4 V	5.40	9.70	16.0	29.0	96.5	215	-	-	-	-		
			3.0 V	5.75	9.70	16.0	29.0	97.5	215	7.40	28.9	346.6	743.8		
			3.6 V	5.90	10.0	16.5	29.5	99.0	220	7.58	29.2	349.0	749.9		

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Table 44. Current consumption in Stop 1 mode (continued)

Symbol	Parameter	Conditions		TYP					MAX ⁽¹⁾					Unit
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I _{DD} (wakeup from Stop1)	Supply current during wakeup from Stop 1 bypass mode	Wakeup clock HSI16, voltage Range 2. See ⁽⁴⁾ .	3.0 V	-	129	-	-	-	-	-	-	-	-	µA
		Wakeup clock MSI = 32 MHz, voltage Range 1. See ⁽⁴⁾ .	3.0 V	-	124	-	-	-	-	-	-	-	-	µA
		Wakeup clock MSI = 4 MHz, voltage Range 2. See ⁽⁴⁾ .	3.0 V	-	207	-	-	-	-	-	-	-	-	µA

1. Guaranteed based on test during characterization, unless otherwise specified.

2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}

3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in [Table 51: Low-power mode wakeup timings](#).

Table 44. Current consumption in Stop 1 mode (continued)

Symbol	Parameter	Conditions		TYP					MAX ⁽¹⁾					Unit
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I _{DD} (wakeup from Stop1)	Supply current during wakeup from Stop 1 bypass mode	Wakeup clock HSI16, voltage Range 2. See ⁽⁴⁾ .	3.0 V	-	129	-	-	-	-	-	-	-	-	µA
		Wakeup clock MSI = 32 MHz, voltage Range 1. See ⁽⁴⁾ .	3.0 V	-	124	-	-	-	-	-	-	-	-	µA
		Wakeup clock MSI = 4 MHz, voltage Range 2. See ⁽⁴⁾ .	3.0 V	-	207	-	-	-	-	-	-	-	-	µA

1. Guaranteed based on test during characterization, unless otherwise specified.

2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}

3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in [Table 51: Low-power mode wakeup timings](#).

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Table 45. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions		TYP					MAX ⁽¹⁾				Unit	
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I _{DD} (Stop 0)	Supply current in Stop 0 mode, RTC disabled, BLE disabled, LCD disabled	--	1.8 V	95.5	100	110	120	195	315	110.0	114.2	458.1	874.8	μA
			2.4 V	97.5	105	110	125	195	315	-	-	-	-	
			3.0 V	98.5	105	110	125	195	320	117.3	134.3	461.8	880.0	
			3.6 V	100	105	115	125	200	320	165.0	135.7	494.0	884.1	
	Supply current during wakeup from Stop 0 Bypass mode	Wakeup clock HSI16, voltage Range 2. See ⁽²⁾ .	3.0 V	-	331	-	-	-	-	-	-	-	-	
			3.0 V	-	349	-	-	-	-	-	-	-	-	
		Wakeup clock is MSI = 32 MHz, voltage Range 1. See ⁽²⁾ .	3.0 V	-	196	-	-	-	-	-	-	-	-	
			3.0 V	-	196	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

2. Wakeup with code execution from Flash memory. Average value given for a typical wakeup time as specified in [Table 51: Low-power mode wakeup timings](#).**STM32WB55xx STM32WB35xx****Table 45. Current consumption in Stop 0 mode**

Symbol	Parameter	Conditions		TYP					MAX ⁽¹⁾				Unit	
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I _{DD} (Stop 0)	Supply current in Stop 0 mode, RTC disabled, BLE disabled, LCD disabled	--	1.8 V	95.5	100	110	120	195	315	110.0	114.2	458.1	874.8	μA
			2.4 V	97.5	105	110	125	195	315	-	-	-	-	
			3.0 V	98.5	105	110	125	195	320	117.3	134.3	461.8	880.0	
			3.6 V	100	105	115	125	200	320	165.0	135.7	494.0	884.1	
	Supply current during wakeup from Stop 0 Bypass mode	Wakeup clock HSI16, voltage Range 2. See ⁽²⁾ .	3.0 V	-	331	-	-	-	-	-	-	-	-	
			3.0 V	-	349	-	-	-	-	-	-	-	-	
		Wakeup clock is MSI = 32 MHz, voltage Range 1. See ⁽²⁾ .	3.0 V	-	196	-	-	-	-	-	-	-	-	
			3.0 V	-	196	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

2. Wakeup with code execution from Flash memory. Average value given for a typical wakeup time as specified in [Table 51: Low-power mode wakeup timings](#).

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Table 46. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP					MAX ⁽¹⁾					Unit
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I _{DD} (Standby)	Supply current in Standby mode (backup registers and SRAM2a retained), RTC disabled	BLE disabled No independent watchdog	1.8 V	0.270	0.320	0.515	0.920	3.45	8.20	0.300	0.828	7.850	19.300	μA
			2.4 V	0.270	0.350	0.540	0.955	3.50	8.80	-	-	-	-	
			3.0 V	0.270	0.370	0.575	1.00	3.85	9.50	0.380	0.945	8.505	21.200	
			3.6 V	0.300	0.410	0.645	1.15	4.20	10.50	0.400	1.040	8.980	22.400	
		BLE disabled With independent watchdog	1.8 V	0.265	0.525	0.710	1.10	3.90	8.40	0.520	1.095	8.041	19.500	
			2.4 V	0.280	0.595	0.790	1.20	4.00	9.05	-	-	-	-	
			3.0 V	0.290	0.670	0.855	1.35	4.15	9.80	0.730	1.253	8.774	21.400	
			3.6 V	0.295	0.770	0.990	1.50	4.60	11.00	0.851	1.356	9.360	22.840	
I _{DD} (Standby with RTC)	Supply current in Standby mode (backup registers and SRAM2a retained), RTC enabled BLE disabled	RTC clocked by LSI, no independent watchdog	1.8 V	0.500	0.600	0.780	1.20	3.70	8.45	0.680	1.165	8.143	19.660	μA
			2.4 V	0.630	0.705	0.910	1.30	3.80	9.10	-	-	-	-	
			3.0 V	0.725	0.825	1.050	1.50	3.95	9.90	0.930	1.463	8.977	21.440	
			3.6 V	0.860	0.970	1.200	1.70	4.25	11.00	1.050	1.628	9.634	23.080	
		RTC clocked by LSI, with independent watchdog	1.8 V	0.565	0.655	0.830	1.25	3.75	8.55	0.734	1.196	8.187	19.710	
			2.4 V	0.635	0.790	0.975	1.40	4.10	9.20	-	-	-	-	
			3.0 V	0.725	0.915	1.100	1.55	4.50	10.00	1.028	1.573	9.072	21.810	
			3.6 V	0.870	1.050	1.300	1.80	4.90	11.00	1.144	1.723	9.730	23.200	
		RTC clocked by LSE quartz ⁽²⁾ in low drive mode	1.8 V	0.525	0.625	0.840	1.25	3.75	8.60	0.600	1.061	8.029	19.610	
			2.4 V	0.665	0.755	0.960	1.35	4.05	9.25	-	-	-	-	
			3.0 V	0.775	0.880	1.100	1.55	4.40	10.00	0.600	1.100	8.719	21.570	
			3.6 V	0.935	1.050	1.300	1.80	5.00	11.00	0.750	1.171	9.460	23.030	

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Table 46. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP					MAX ⁽¹⁾					Unit
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I _{DD} (Standby)	Supply current in Standby mode (backup registers and SRAM2a retained), RTC disabled	BLE disabled No independent watchdog	1.8 V	0.270	0.320	0.515	0.920	3.45	8.20	0.300	0.828	7.850	19.300	μA
			2.4 V	0.270	0.350	0.540	0.955	3.50	8.80	-	-	-	-	
			3.0 V	0.270	0.370	0.575	1.00	3.85	9.50	0.380	0.945	8.505	21.200	
			3.6 V	0.300	0.410	0.645	1.15	4.20	10.50	0.400	1.040	8.980	22.400	
		BLE disabled With independent watchdog	1.8 V	0.265	0.525	0.710	1.10	3.90	8.40	0.520	1.095	8.041	19.500	
			2.4 V	0.280	0.595	0.790	1.20	4.00	9.05	-	-	-	-	
			3.0 V	0.290	0.670	0.855	1.35	4.15	9.80	0.730	1.253	8.774	21.400	
			3.6 V	0.295	0.770	0.990	1.50	4.60	11.00	0.851	1.356	9.360	22.840	
	RTC clocked by LSI, no independent watchdog	RTC clocked by LSI, with independent watchdog	1.8 V	0.500	0.600	0.780	1.20	3.70	8.45	0.680	1.165	8.143	19.660	
			2.4 V	0.630	0.705	0.910	1.30	3.80	9.10	-	-	-	-	
			3.0 V	0.725	0.825	1.050	1.50	3.95	9.90	0.930	1.463	8.977	21.440	
			3.6 V	0.860	0.970	1.200	1.70	4.25	11.00	1.050	1.628	9.634	23.080	
		RTC clocked by LSE quartz ⁽²⁾ in low drive mode	1.8 V	0.565	0.655	0.830	1.25	3.75	8.55	0.734	1.196	8.187	19.710	
			2.4 V	0.635	0.790	0.975	1.40	4.10	9.20	-	-	-	-	
			3.0 V	0.725	0.915	1.100	1.55	4.50	10.00	1.028	1.573	9.072	21.810	
			3.6 V	0.870	1.050	1.300	1.80	4.90	11.00	1.144	1.723	9.730	23.200	
			1.8 V	0.525	0.625	0.840	1.25	3.75	8.60	0.600	1.061	8.029	19.610	
I _{DD} (Standby with RTC)	Supply current in Standby mode (backup registers and SRAM2a retained), RTC enabled BLE disabled	RTC clocked by LSI, with independent watchdog	1.8 V	0.565	0.655	0.830	1.25	3.75	8.55	0.734	1.196	8.187	19.710	μA
			2.4 V	0.635	0.790	0.975	1.40	4.10	9.20	-	-	-		

Table 46. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP						MAX ⁽¹⁾				Unit
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I _{DD} (SRAM2a) ⁽³⁾	Supply current to be subtracted in Standby mode when SRAM2a is not retained	-	1.8 V	0.160	0.210	0.380	0.660	2.30	5.15	-	-	-	-	μA
			2.4 V	0.165	0.245	0.375	0.650	2.15	5.20	-	-	-	-	
			3.0 V	0.155	0.250	0.385	0.630	2.25	5.20	-	-	-	-	
			3.6 V	0.155	0.235	0.375	0.670	2.20	5.20	-	-	-	-	
I _{DD} (wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is HSI16. See ⁽⁴⁾ . SMPS OFF	3.0 V	-	1.73	-	-	-	-	-	-	-	-	mA

- Guaranteed by characterization results, unless otherwise specified.
- Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
- The supply current in Standby with SRAM2a mode is: I_{DD}(Standby) + I_{DD}(SRAM2a). The supply current in Standby with RTC with SRAM2a mode is: I_{DD}(Standby + RTC) + I_{DD}(SRAM2a).
- Wakeup with code execution from Flash memory. Average value given for a typical wakeup time as specified in [Table 51](#).

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Table 46. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP						MAX ⁽¹⁾				Unit
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I _{DD} (SRAM2a) ⁽³⁾	Supply current to be subtracted in Standby mode when SRAM2a is not retained	-	1.8 V	0.160	0.210	0.380	0.660	2.30	5.15	-	-	-	-	μA
			2.4 V	0.165	0.245	0.375	0.650	2.15	5.20	-	-	-	-	
			3.0 V	0.155	0.250	0.385	0.630	2.25	5.20	-	-	-	-	
			3.6 V	0.155	0.235	0.375	0.670	2.20	5.20	-	-	-	-	
I _{DD} (wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is HSI16. See ⁽⁴⁾ . SMPS OFF	3.0 V	-	1.73	-	-	-	-	-	-	-	-	mA

- Guaranteed by characterization results, unless otherwise specified.
- Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
- The supply current in Standby with SRAM2a mode is: I_{DD}(Standby) + I_{DD}(SRAM2a). The supply current in Standby with RTC with SRAM2a mode is: I_{DD}(Standby + RTC) + I_{DD}(SRAM2a).
- Wakeup with code execution from Flash memory. Average value given for a typical wakeup time as specified in [Table 51](#).

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Table 47. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP						MAX ⁽¹⁾				Unit
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I _{DD} (Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	1.8 V	0.039	0.013	0.030	0.100	0.635	1.950	-	-	2.099	6.200	μA
			2.4 V	0.059	0.014	0.055	0.120	0.785	2.350	-	-	-	-	
			3.0 V	0.064	0.037	0.070	0.180	1.000	2.900	-	0.185	2.670	7.490	
			3.6 V	0.071	0.093	0.140	0.280	1.300	3.700	-	0.247	3.120	8.450	
I _{DD} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE quartz ⁽²⁾ in low drive mode	1.8 V	0.320	0.315	0.355	0.420	0.985	2.300	-	0.572	2.702	6.180	μA
			2.4 V	0.425	0.405	0.460	0.540	1.200	2.800	-	-	-	-	
			3.0 V	0.535	0.535	0.595	0.700	1.500	3.450	-	0.664	2.990	7.800	
			3.6 V	0.695	0.720	0.790	0.940	2.000	4.350	-	0.790	3.730	9.140	

1. Guaranteed by characterization results, unless otherwise specified.

2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 48. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP						MAX ⁽¹⁾				Unit	
		-	V _{BAT}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	40 °C	55 °C	85 °C	
I _{DD(VBAT)}	Backup domain supply current	RTC disabled	1.8 V	1.00	2.00	4.00	10.0	52.0	145	-	-	-	-	-	nA
			2.4 V	1.00	2.00	5.00	12.0	60.0	165	-	-	-	-	-	
			3.0 V	2.00	4.00	7.00	16.0	75.0	225	-	-	-	-	-	
			3.6 V	7.00	15.0	23.0	42.0	170	450	-	-	-	-	-	
	RTC enabled and clocked by LSE quartz ⁽²⁾	RTC enabled and clocked by LSE quartz ⁽²⁾	1.8 V	295	305	315	325	380	480	-	-	-	-	-	nA
			2.4 V	385	395	400	415	475	595	-	-	-	-	-	
			3.0 V	495	505	515	530	600	765	-	-	-	-	-	
			3.6 V	630	645	660	685	830	1150	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

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Table 47. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP						MAX ⁽¹⁾				Unit
		-	V _{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I _{DD} (Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	1.8 V	0.039	0.013	0.030	0.100	0.635	1.950	-	-	2.099	6.200	μA
			2.4 V	0.059	0.014	0.055	0.120	0.785	2.350	-	-	-	-	
			3.0 V	0.064	0.037	0.070	0.180	1.000	2.900	-	0.185	2.670	7.490	
			3.6 V	0.071	0.093	0.140	0.280	1.300	3.700	-	0.247	3.120	8.450	
I _{DD} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE quartz ⁽²⁾ in low drive mode	1.8 V	0.320	0.315	0.355	0.420	0.985	2.300	-	0.572	2.702	6.180	μA
			2.4 V	0.425	0.405	0.460	0.540	1.200	2.800	-	-	-	-	
			3.0 V	0.535	0.535	0.595	0.700	1.500	3.450	-	0.664	2.990	7.800	
			3.6 V	0.695	0.720	0.790	0.940	2.000	4.350	-	0.790	3.730	9.140	

1. Guaranteed by characterization results, unless otherwise specified.

2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 48. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP						MAX ⁽¹⁾				Unit	
		-	V _{BAT}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	40 °C	55 °C	85 °C	
I _{DD(VBAT)}	Backup domain supply current	RTC disabled	1.8 V	1.00	2.00	4.00	10.0	52.0	145	-	-	-	-	-	nA
			2.4 V	1.00	2.00	5.00	12.0	60.0	165	-	-	-	-	-	
			3.0 V	2.00	4.00	7.00	16.0	75.0	225	-	-	-	-	-	
			3.6 V	7.00	15.0	23.0	42.0								

Table 49. Current under Reset condition

Symbol	Conditions	TYP						MAX ⁽¹⁾						Unit
		0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	
$I_{DD(RST)}$	1.8 V	-	410	-	-	-	-	-	-	-	-	-	-	μA
	2.4 V	-	-	-	-	-	-	-	-	-	-	-	-	
	3.0 V	-	550	-	-	-	-	750	-	-	-	-	-	
	3.6 V	-	750	-	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

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Symbol	Conditions	TYP						MAX ⁽¹⁾						Unit
		0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	
$I_{DD(RST)}$	1.8 V	-	410	-	-	-	-	-	-	-	-	-	-	μA
	2.4 V	-	-	-	-	-	-	-	-	-	-	-	-	
	3.0 V	-	550	-	-	-	-	-	-	-	-	-	-	
	3.6 V	-	750	-	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

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I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 72: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see [Table 50: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DD} is the I/O supply voltage
- f_{SW} is the I/O switching frequency
- C is the total capacitance seen by the I/O pin: $C = C_{IO} + C_{EXT}$
- C_{IO} is the I/O pin capacitance
- C_{EXT} is the PCB board capacitance plus any connected external device pin capacitance.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

所有用作带上拉的输入的 I/O 都会在引脚被外部保持低电压时产生电流消耗。这个电流消耗的值可以简单地通过使用 表72: I/O静态特性 中给出的上拉/下拉电阻值来计算。

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

额外的I/O电流消耗是由于I/Os配置为输入时，外部应用了中间电压水平所致。这种电流消耗是由于使用输入施密特触发器电路来判别输入值而引起的。除非应用需要此特定配置，否则可以通过将这些I/Os配置为模拟模式来避免此电源电流消耗。这尤其适用于ADC输入引脚，它们应该配置为模拟输入。

注意：

任何浮动输入引脚都可以定定到中间电压水平，或者由于外部电磁噪声而意外切换。为了避免与浮动引脚相关的电流消耗，必须将其配置为模拟模式，或者强制内部设置为确定的数字值。这可以通过使用上拉/下拉电阻来实现，或者将引脚配置为输出模式。

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see [Table 50: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DD} is the I/O supply voltage
- f_{SW} is the I/O switching frequency
- C is the total capacitance seen by the I/O pin: $C = C_{IO} + C_{EXT}$
- C_{IO} is the I/O pin capacitance
- C_{EXT} is the PCB board capacitance plus any connected external device pin capacitance.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in [Table 50](#). The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
 - when the peripheral is clocked on
 - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in [Table 20: Voltage characteristics](#)
- The power consumption of the digital part of the on-chip peripherals is given in [Table 50](#). The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 50. Peripheral current consumption

Peripheral	Range 1	Range 2	Low-power run and sleep	Unit
AHB1	Bus matrix ⁽¹⁾	2.40	2.00	1.80
	TSC	1.25	1.05	1.05
	CRC	0.465	0.375	0.380
	DMA1	1.90	1.55	1.80
	DMA2	2.00	1.65	1.80
	DMAMUX	4.15	3.40	4.45
	All AHB1 peripherals	12.0	10.0	11.5
AHB2 ⁽²⁾	AES1	4.00	3.30	3.90
	ADC1 independent clock domain	2.55	2.10	2.10
	ADC1 clock domain	2.25	1.90	1.90
	All AHB2 peripherals	7.45	6.20	6.60
AHB3	QSPI	7.60	6.25	7.10
AHB Shared	TRNG independent clock domain	3.80	N/A	N/A
	TRNG clock domain	2.00	N/A	N/A
	SRAM2	1.70	1.35	1.35
	FLASH	8.35	6.90	8.45
	AES2	6.95	5.75	7.00
	PKA	4.40	3.65	4.25
	All AHB shared peripherals	17.5	14.5	16.0

μA/MHz

片上外设电流消耗

外围设备的电流消耗在 [表50](#)中给出。MCU在以下条件下安装：

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
 - when the peripheral is clocked on
 - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in [Table 20: Voltage characteristics](#)
- The power consumption of the digital part of the on-chip peripherals is given in [Table 50](#). The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 50. Peripheral current consumption

Peripheral	Range 1	Range 2	Low-power run and sleep	Unit
AHB1	Bus matrix ⁽¹⁾	2.40	2.00	1.80
	TSC	1.25	1.05	1.05
	CRC	0.465	0.375	0.380
	DMA1	1.90	1.55	1.80
	DMA2	2.00	1.65	1.80
	DMAMUX	4.15	3.40	4.45
	All AHB1 peripherals	12.0	10.0	11.5
AHB2 ⁽²⁾	AES1	4.00	3.30	3.90
	ADC1 independent clock domain	2.55	2.10	2.10
	ADC1 clock domain	2.25	1.90	1.90
	All AHB2 peripherals	7.45	6.20	6.60
AHB3	QSPI	7.60	6.25	7.10
AHB Shared	TRNG independent clock domain	3.80	N/A	N/A
	TRNG clock domain	2.00	N/A	N/A
	SRAM2	1.70	1.35	1.35
	FLASH	8.35	6.90	8.45
	AES2	6.95	5.75	7.00
	PKA	4.40	3.65	4.25
	All AHB shared peripherals	17.5	14.5	16.0

Table 50. Peripheral current consumption (continued)

Peripheral	Range 1	Range 2	Low-power run and sleep	Unit
APB1	RTCA	1.10	0.88	1.25
	CRS	0.24	0.20	0.20
	USB FS independent clock domain	3.20	N/A	N/A
	USB FS clock domain	2.05	N/A	N/A
	I2C1 independent clock domain	2.50	4.40	4.40
	I2C1 clock domain	4.80	4.00	5.50
	I2C3 independent clock domain	2.10	3.50	3.55
	I2C3 clock domain	3.70	3.10	3.55
	LCD	1.35	1.10	2.10
	SPI2	1.65	1.40	2.25
	LPTIM1 independent clock domain	2.10	3.40	3.00
	LPTIM1 clock domain	3.60	3.00	3.80
	TIM2	5.65	4.70	4.90
	LPUART1 independent clock domain	2.70	4.15	3.85
	LPUART1 clock domain	4.45	3.70	5.25
	LPTIM2 clock domain	3.95	3.25	4.50
	LPTIM2 independent clock domain	2.20	3.70	3.80
	WWDG	0.335	0.285	0.965
	All APB1 peripherals	27.0	22.5	25.5
APB2	AHB to APB2 ⁽³⁾	1.10	0.885	1.35
	TIM1	8.20	6.80	7.25
	TIM17	2.85	2.40	2.40
	TIM16	2.75	2.30	2.55
	USART1 independent clock domain	4.40	7.80	7.00
	USART1 clock domain	8.80	7.30	7.75
	SPI1	1.75	1.45	1.45
	SAI1 independent clock domain	2.50	1.50	3.50
	SAI1 clock domain	2.40	N/A	N/A
	All APB2 on	28.0	23.0	25.5
	ALL	97.5	80.5	90.0

μA/MHz

- The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
- GPIOs consumption during read and write accesses.
- The AHB to APB2 bridge is automatically active when at least one peripheral is ON on the APB2.

表 50. 外设电流消耗 (继续)

Peripheral	Range 1	Range 2	Low-power run and sleep	Unit
APB1	RTCA	1.10	0.88	1.25
	CRS	0.24	0.20	0.20
	USB FS independent clock domain	3.20	N/A	N/A
	USB FS clock domain	2.05	N/A	N/A
	I2C1 independent clock domain	2.50	4.40	4.40
	I2C1 clock domain	4.80	4.00	5.50
	I2C3 independent clock domain	2.10	3.50	3.55
	I2C3 clock domain	3.70	3.10	3.55
	LCD	1.35	1.10	2.10
	SPI2	1.65	1.40	2.25
	LPTIM1 independent clock domain	2.10	3.40	3.00
	LPTIM1 clock domain	3.60	3.00	3.80
	TIM2	5.65	4.70	4.90
	LPUART1 independent clock domain	2.70	4.15	3.85
	LPUART1 clock domain	4.45	3.70	5.25
	LPTIM2 clock domain	3.95	3.25	4.50
	LPTIM2 independent clock domain	2.20	3.70	3.80
	WWDG	0.335	0.285	0.965
	All APB1 peripherals	27.0	22.5	25.5
APB2	AHB to APB2 ⁽³⁾	1.10	0.885	1.35
	TIM1	8.20	6.80	7.25
	TIM17	2.85	2.40	2.40
	TIM16	2.75	2.30	2.55
	USART1 independent clock domain	4.40	7.80	7.00
	USART1 clock domain	8.80	7.30	7.75
	SPI1	1.75	1.45	1.45
	SAI1 independent clock domain	2.50	1.50	3.50
	SAI1 clock domain	2.40	N/A	N/A
	All APB2 on	28.0	23.0	25.5
	ALL	97.5	80.5	90.0

μA/MHz

- The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
- GPIOs consumption during read and write accesses.
- The AHB to APB2 bridge is automatically active when at least one peripheral is ON on the APB2.

6.3.9 Wakeup time from Low-power modes and voltage scaling transition times

The wakeup times given in [Table 51](#) are the latency between the event and the execution of the first user instruction.

The device goes in Low-power mode after the WFE (Wait For Event) instruction.

Table 51. Low-power mode wakeup timings⁽¹⁾

Symbol	Parameter	Conditions		Typ	Max	Unit
t _{WUSLEEP}	Wakeup time from Sleep mode to Run mode	-		9	10	No. of CPU cycles
t _{WULPSLEEP}	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with memory in power-down during low-power sleep mode (FPDS = 1 in PWR_CR1) and with clock MSI = 2 MHz		9	10	
t _{WUSTOP0}	Wake up time from Stop 0 mode to Run mode in Flash memory	Range 1	Wakeup clock MSI = 32 MHz	2.38	2.96	μs
			Wakeup clock HSI16 = 16 MHz	1.69	2.00	
		Range 2	Wakeup clock HSI16 = 16 MHz	1.70	2.01	
			Wakeup clock MSI = 4 MHz	7.43	8.59	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 32 MHz	2.63	3.00	
			Wakeup clock HSI16 = 16 MHz	1.80	2.00	
		Range 2	Wakeup clock HSI16 = 16 MHz	1.82	2.02	
			Wakeup clock MSI = 4 MHz	7.58	8.70	
t _{WUSTOP1}	Wake up time from Stop 1 mode to Run in Flash memory SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	4.67	5.56	μs
			Wakeup clock HSI16 = 16 MHz	5.09	6.03	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.08	6.00	
			Wakeup clock MSI = 4 MHz	8.36	9.28	
	Wake up time from Stop 1 mode to Run in SRAM1 SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	4.88	5.55	
			Wakeup clock HSI16 = 16 MHz	5.29	5.95	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.28	5.96	
			Wakeup clock MSI = 4 MHz	8.49	9.30	
	Wake up time from Stop 1 mode to Low-power run mode in Flash memory	Regulator in Low-power mode (LPR = 1 in PWR_CR1)	Wakeup clock MSI = 4 MHz		7.96	9.59
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1		Wakeup clock MSI = 4 MHz		8.00	9.47

6.3.9 从低功耗模式和电压缩放唤醒时间 过渡时间

给出的唤醒时间在[表51](#)是事件和第一个用户指令执行之间的延迟。

设备在 WFE (Wait For Event) 指令后进入低功模式。

Table 51. Low-power mode wakeup timings⁽¹⁾

Symbol	Parameter	Conditions		Typ	Max	Unit
t _{WUSLEEP}	Wakeup time from Sleep mode to Run mode	-		9	10	No. of CPU cycles
t _{WULPSLEEP}	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with memory in power-down during low-power sleep mode (FPDS = 1 in PWR_CR1) and with clock MSI = 2 MHz		9	10	
t _{WUSTOP0}	Wake up time from Stop 0 mode to Run mode in Flash memory	Range 1	Wakeup clock MSI = 32 MHz	2.38	2.96	μs
			Wakeup clock HSI16 = 16 MHz	1.69	2.00	
		Range 2	Wakeup clock HSI16 = 16 MHz	1.70	2.01	
			Wakeup clock MSI = 4 MHz	7.43	8.59	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 32 MHz	2.63	3.00	
			Wakeup clock HSI16 = 16 MHz	1.80	2.00	
		Range 2	Wakeup clock HSI16 = 16 MHz	1.82	2.02	
			Wakeup clock MSI = 4 MHz	7.58	8.70	
	Wake up time from Stop 1 mode to Run in Flash memory SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	4.67	5.56	
			Wakeup clock HSI16 = 16 MHz	5.09	6.03	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.08	6.00	
			Wakeup clock MSI = 4 MHz	8.36	9.28	
t _{WUSTOP1}	Wake up time from Stop 1 mode to Run in SRAM1 SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	4.88	5.55	μs
			Wakeup clock HSI16 = 16 MHz	5.29	5.95	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.28	5.96	
			Wakeup clock MSI = 4 MHz	8.49	9.30	
	Wake up time from Stop 1 mode to Low-power run mode in Flash memory	Regulator in Low-power mode (LPR = 1 in PWR_CR1)	Wakeup clock MSI = 4 MHz		7.96	9.59
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1		Wakeup clock MSI = 4 MHz		8.00	9.47

Table 51. Low-power mode wakeup timings⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
tWUSTOP2	Wake up time from Stop 2 mode to Run mode in Flash memory SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	5.27	6.07	μs
			Wakeup clock HSI16 = 16 MHz	5.71	6.52	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.72	6.52	
			Wakeup clock MSI = 4 MHz	9.10	9.93	
	Wake up time from Stop 2 mode to Run mode in SRAM1 SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	5.20	5.94	
			Wakeup clock HSI16 = 16 MHz	5.64	6.42	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.64	6.43	
			Wakeup clock MSI = 4 MHz	9.05	9.85	
tWUSTBY	Wakeup time from Standby mode to Run mode SMPS Bypassed	Range 1	Wakeup clock HSI16 = 16 MHz	51.0	58.1	μs

1. Guaranteed by characterization results ($V_{DD} = 3$ V, $T = 25$ °C).Table 52. Regulator modes transition times⁽¹⁾

Symbol	Parameter	Conditions	Typ	Max	Unit
tWULPRUN	Wakeup time from Low-power run mode to Run mode ⁽²⁾	Code run with MSI 2 MHz	15.33	16.30	μs
tVOST	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2 ⁽³⁾	Code run with HSI16	21.4	28.9	

1. Guaranteed by characterization results ($V_{DD} = 3$ V, $T = 25$ °C).

2. Time until REGLPF flag is cleared in PWR_SR2.

3. Time until VOSF flag is cleared in PWR_SR2.

Table 53. Wakeup time using USART/LPUART⁽¹⁾

Symbol	Parameter	Conditions	Typ	Max	Unit
tWUUSART tWULPUART	Wakeup time needed to calculate the maximum USART/LPUART baud rate allowing to wakeup from Stop modes when USART/LPUART clock source is HSI16	Stop mode 0	-	1.7	μs
		Stop mode 1/2	-	8.5	

1. Guaranteed by design.

Table 51. Low-power mode wakeup timings⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
tWUSTOP2	Wake up time from Stop 2 mode to Run mode in Flash memory SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	5.27	6.07	μs
			Wakeup clock HSI16 = 16 MHz	5.71	6.52	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.72	6.52	
			Wakeup clock MSI = 4 MHz	9.10	9.93	
	Wake up time from Stop 2 mode to Run mode in SRAM1 SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	5.20	5.94	
			Wakeup clock HSI16 = 16 MHz	5.64	6.42	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.64	6.43	
			Wakeup clock MSI = 4 MHz	9.05	9.85	
tWUSTBY	Wakeup time from Standby mode to Run mode SMPS Bypassed	Range 1	Wakeup clock HSI16 = 16 MHz	51.0	58.1	μs

1. Guaranteed by characterization results ($V_{DD} = 3$ V, $T = 25$ °C).

表 52. 调节器模式过渡时间 (1)

Symbol	Parameter	Conditions	Typ	Max	Unit
tWULPRUN	Wakeup time from Low-power run mode to Run mode ⁽²⁾	Code run with MSI 2 MHz	15.33	16.30	μs
tVOST	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2 ⁽³⁾	Code run with HSI16	21.4	28.9	

1. Guaranteed by characterization results ($V_{DD} = 3$ V, $T = 25$ °C).

2. Time until REGLPF flag is cleared in PWR_SR2.

3. Time until VOSF flag is cleared in PWR_SR2.

表53. 使用 USART/LPUART(1) 唤醒时间

Symbol	Parameter	Conditions	Typ	Max	Unit
tWUUSART tWULPUART	Wakeup time needed to calculate the maximum USART/LPUART baud rate allowing to wakeup from Stop modes when USART/LPUART clock source is HSI16	Stop mode 0	-	1.7	μs
		Stop mode 1/2	-	8.5	

1. Guaranteed by design.

6.3.10 External clock source characteristics

High-speed external user clock generated from an external source

The high-speed external (HSE) clock is supplied with a 32 MHz crystal oscillator or a sine or a square wave.

The devices include internal programmable capacitances that can be used to tune the crystal frequency in order to compensate the PCB parasitic one.

The characteristics in [Table 54](#) and [Table 55](#) are measured over recommended operating conditions, unless otherwise specified. Typical values are referred to $T_A = 25^\circ\text{C}$ and $V_{DD} = 3.0\text{ V}$.

Table 54. HSE crystal requirements⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{NOM}	Oscillator frequency	-	-	32	-	MHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance.	-	-	(2)	ppm
C_L	Load capacitance	-	6	-	8	pF
ESR	Equivalent series resistance	-	-	-	100	Ω

1. 32 MHz XTAL is specified for two specific references: NX2016SA and NX1612SA.

2. Refer to the standard specification: 50 ppm for BLE, 40 ppm for 802.15.4 and when both BLE and 802.15.4 are used.

Table 55. HSE clock source requirements⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	-	32	-	MHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature and aging.	-	-	(2)	ppm
V_{HSE}	Clock input voltage limits	Sine or square wave, AC-coupled ⁽³⁾	0.4	-	1.6	V_{PP}
DuC(HSE)	Duty cycle	-	45	50	55	%
t_r, t_f	Rise and fall times	10% - 90% square wave	-	-	$15 * V_{PP}$	ns
$\Phi_n(HSE)$	Phase noise for 32 MHz	Offset = 10 kHz	-	-	-127	dBc/Hz
		Offset = 100 kHz	-	-	-135	
		Offset = 1 MHz	-	-	-138	

1. Guaranteed by design.

2. Refer to the standard specification: 50 ppm for BLE, 40 ppm for 802.15.4 and when both BLE and 802.15.4 are used.

3. Only AC coupled is supported (capacitor 470 pF to 100 nF).

6.3.10 外部时钟源特性

高速外部用户时钟从外部来源生成

The high-speed external (HSE) clock is supplied with a 32 MHz crystal oscillator or a sine or a square wave.

The devices include internal programmable capacitances that can be used to tune the crystal frequency in order to compensate the PCB parasitic one.

The characteristics in [Table 54](#) and [Table 55](#) are measured over recommended operating conditions, unless otherwise specified. Typical values are referred to $T_A = 25^\circ\text{C}$ and $V_{DD} = 3.0\text{ V}$.

表54. HSE 晶体要求⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{NOM}	Oscillator frequency	-	-	32	-	MHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance.	-	-	(2)	ppm
C_L	Load capacitance	-	6	-	8	pF
ESR	Equivalent series resistance	-	-	-	100	Ω

1. 32 MHz XTAL is specified for two specific references: NX2016SA and NX1612SA.

2. Refer to the standard specification: 50 ppm for BLE, 40 ppm for 802.15.4 and when both BLE and 802.15.4 are used.

表55. HSE 时钟源要求(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	-	32	-	MHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature and aging.	-	-	(2)	ppm
V_{HSE}	Clock input voltage limits	Sine or square wave, AC-coupled ⁽³⁾	0.4	-	1.6	V_{PP}
DuC(HSE)	Duty cycle	-	45	50	55	%
t_r, t_f	Rise and fall times	10% - 90% square wave	-	-	$15 * V_{PP}$	ns
$\Phi_n(HSE)$	Phase noise for 32 MHz	Offset = 10 kHz	-	-	-127	dBc/Hz
		Offset = 100 kHz	-	-	-135	
		Offset = 1 MHz	-	-	-138	

1. Guaranteed by design.

2. Refer to the standard specification: 50 ppm for BLE, 40 ppm for 802.15.4 and when both BLE and 802.15.4 are used.

3. Only AC coupled is supported (capacitor 470 pF to 100 nF).

Table 56. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SUA(HSE)}$	Startup time for 80% amplitude stabilization	V_{DDRF} stabilized, XOTUNE=000000, -40 to +125 °C range	-	1000	-	μs
$t_{SUR(HSE)}$	Startup time for XOREADY signal		-	250	-	
$I_{DDRF(HSE)}$	HSE current consumption	HSEGMC=000, XOTUNE=000000	-	50	-	μA
$XOT_g(HSE)$	XOTUNE granularity	Capacitor bank	-	1	5	ppm
$XOT_{fp}(HSE)$	XOTUNE frequency pulling		±20	±40	-	
$XOT_{nb}(HSE)$	XOTUNE number of tuning bits		-	6	-	bit
$XOT_{st}(HSE)$	XOTUNE setting time		-	-	0.1	ms

Note: For information about oscillator trimming refer to AN5165 "Development of RF hardware using STM32WB microcontrollers", available from www.st.com.

Low-speed external user clock generated from an external source

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. The information provided in this section is based on design simulation results obtained with typical external components specified in [Table 57](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time.

Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 57. Low-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$G_{mcritmax}$	Maximum critical crystal g_m	LSEDRV[1:0] = 00 Low drive capability	-	-	0.50	μA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.70	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.70	
$t_{SU(LSE)}^{(2)}$	Startup time	V_{DD} stabilized	-	2	-	s

表 56. HSE 振荡器特性

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SUA(HSE)}$	Startup time for 80% amplitude stabilization	V_{DDRF} stabilized, XOTUNE=000000, -40 to +125 °C range	-	1000	-	μs
$t_{SUR(HSE)}$	Startup time for XOREADY signal		-	250	-	
$I_{DDRF(HSE)}$	HSE current consumption	HSEGMC=000, XOTUNE=000000	-	50	-	μA
$XOT_g(HSE)$	XOTUNE granularity	Capacitor bank	-	1	5	ppm
$XOT_{fp}(HSE)$	XOTUNE frequency pulling		±20	±40	-	
$XOT_{nb}(HSE)$	XOTUNE number of tuning bits		-	6	-	bit
$XOT_{st}(HSE)$	XOTUNE setting time		-	-	0.1	ms

Note: For information about oscillator trimming refer to AN5165 "Development of RF hardware using STM32WB microcontrollers", available from www.st.com.

从外部来源生成的低速外部用户时钟

低速外部(LSE)时钟可以由32.768 kHz晶体共振振荡器供电。本节中提供的信息基于在表 57 中指定的典型外部组件上进行的设计模拟结果。在应用中，共振器和负载电容必须尽可能靠近振荡器引脚放置，以减少输出失真和启动稳定时间。

Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

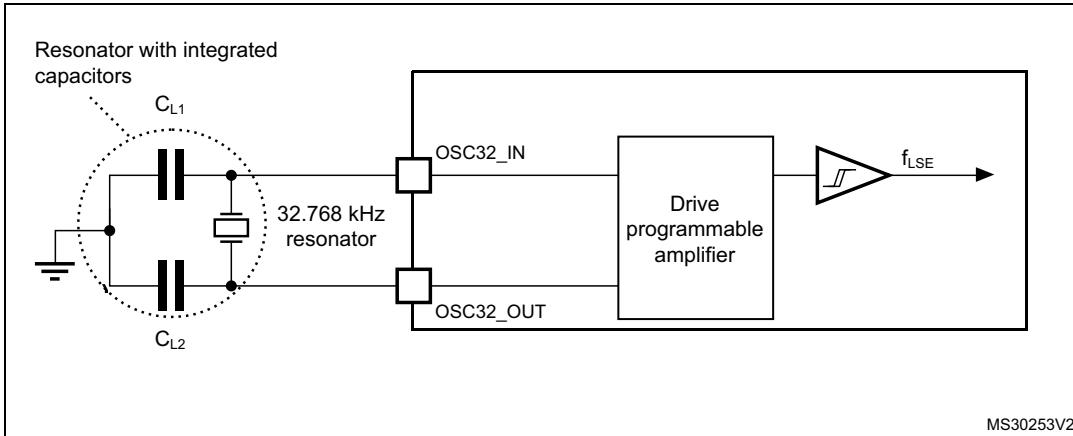
表 57. 低速外部用户时钟特性(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$G_{mcritmax}$	Maximum critical crystal g_m	LSEDRV[1:0] = 00 Low drive capability	-	-	0.50	μA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.70	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.70	
$t_{SU(LSE)}^{(2)}$	Startup time	V_{DD} stabilized	-	2	-	s

- Guaranteed by design.
- $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) until a stable 32 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal refer to application note AN2867 "Oscillator design guide for STM8S, STM8A and STM32 microcontrollers" available from www.st.com.

Figure 22. Typical application with a 32.768 kHz crystal

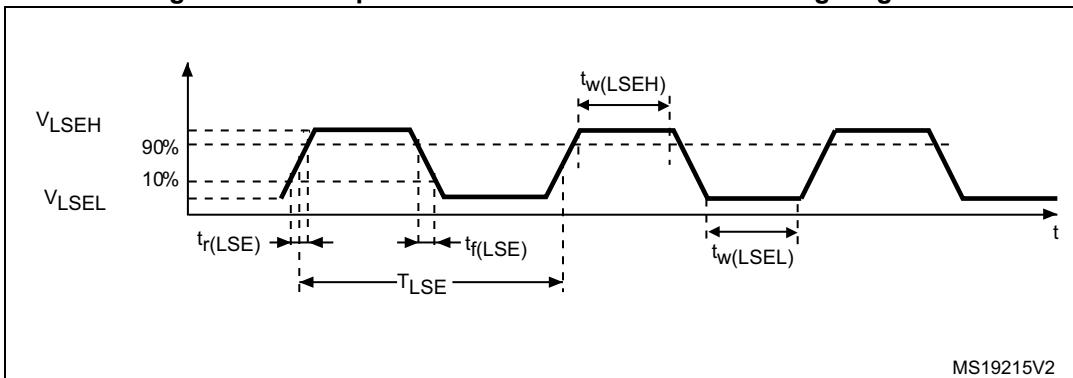


Note: No external resistors are required between OSC32_IN and OSC32_OUT, and it is forbidden to add one.

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics detailed in [Section 6.3.17](#). The recommend clock input waveform is shown in [Figure 23](#).

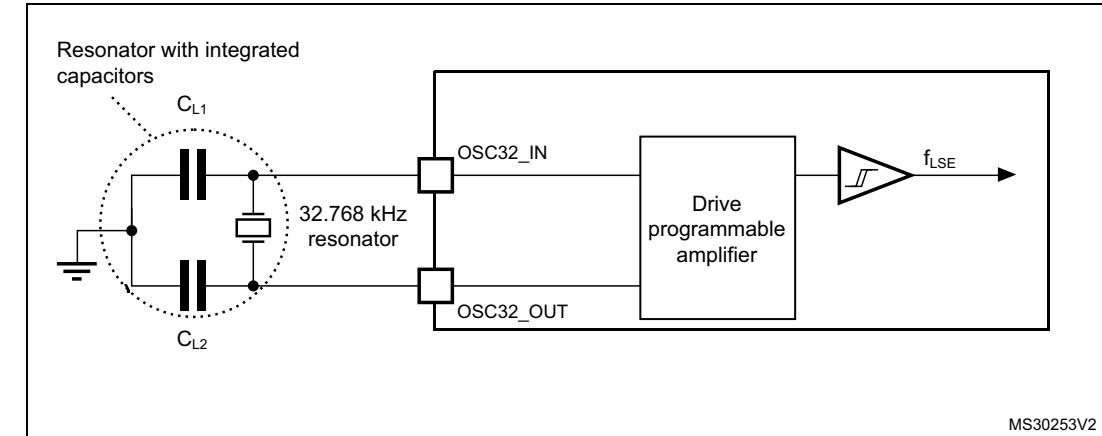
Figure 23. Low-speed external clock source AC timing diagram



- Guaranteed by design.
- $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) until a stable 32 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: 有关选择晶体的信息, 请参考应用笔记AN2867 “STM8S、STM8A和STM32微控制器的振荡器设计指南” 可从 www.st.com.

Figure 22. Typical application with a 32.768 kHz crystal



Note: No external resistors are required between OSC32_IN and OSC32_OUT, and it is forbidden to add one.

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics detailed in [Section 6.3.17](#). The recommend clock input waveform is shown in [Figure 23](#).

Figure 23. Low-speed external clock source AC timing diagram

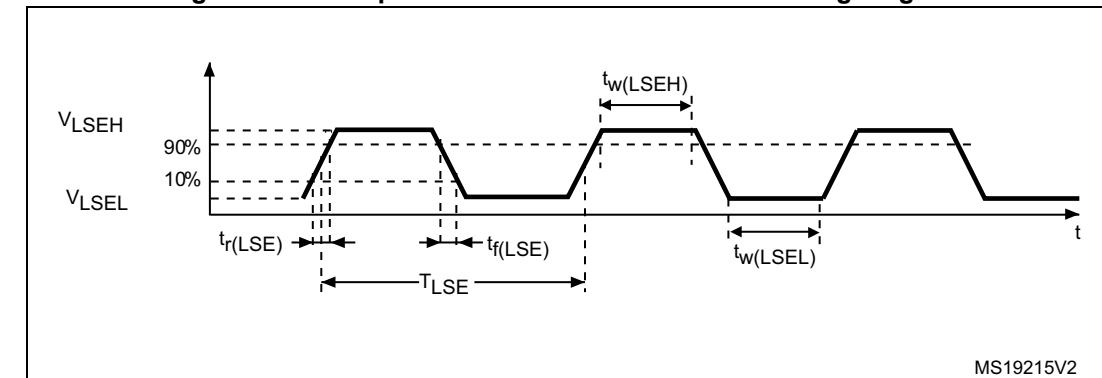


Table 58. Low-speed external user clock characteristics⁽¹⁾ – Bypass mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{LSE_ext}	User external clock source frequency	-	21.2	32.768	44.4	kHz
V _{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V _{DDx}	-	V _{DDx}	V
V _{LSEL}	OSC32_IN input pin low level voltage	-	V _{SS}	-	0.3 V _{DDx}	
t _{w(LSEH)} t _{w(LSEL)}	OSC32_IN high or low time	-	250	-	-	ns
f _{tolLSE}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling	-500	-	+500	ppm

1. Guaranteed by design.

6.3.11 Internal clock source characteristics

The parameters given in [Table 59](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#). The provided curves are characterization results, not tested in production.

High-speed internal (HSI16) RC oscillator

Table 59. HSI16 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{HSI16}	HSI16 Frequency	V _{DD} =3.0 V, T _A =30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16) ⁽²⁾	Duty Cycle	-	45	-	55	
Δ _{Temp} (HSI16)	HSI16 oscillator frequency drift over temperature	T _A = 0 to 85 °C	-1	-	1	
		T _A = -40 to 125 °C	-2	-	1.5	
Δ _{VDD} (HSI16)	HSI16 oscillator frequency drift over V _{DD}	V _{DD} =1.62 V to 3.6 V	-0.1	-	0.05	
t _{su} (HSI16) ⁽²⁾	HSI16 oscillator start-up time	-	-	0.8	1.2	μs
t _{stab} (HSI16) ⁽²⁾	HSI16 oscillator stabilization time	-	-	3	5	
I _{DD} (HSI16) ⁽²⁾	HSI16 oscillator power consumption	-	-	155	190	μA

1. Guaranteed by characterization results.

2. Guaranteed by design.

表 58. 低速外部用户时钟特性⁽¹⁾ – 绕过模式

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{LSE_ext}	User external clock source frequency	-	21.2	32.768	44.4	kHz
V _{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V _{DDx}	-	V _{DDx}	V
V _{LSEL}	OSC32_IN input pin low level voltage	-	V _{SS}	-	0.3 V _{DDx}	
t _{w(LSEH)} t _{w(LSEL)}	OSC32_IN high or low time	-	250	-	-	ns
f _{tolLSE}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling	-500	-	+500	ppm

1. Guaranteed by design.

6.3.11 Internal clock source characteristics

给定的参数在表 59是在环境温度和供电电压条件下进行的测试中得出的这些条件总结在表 24: 通用运行条件。提供的曲线是特征化结果，不是在生产中进行的测试。

High-speed internal (HSI16) RC oscillator

表 59. HSI16 振荡器特性⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{HSI16}	HSI16 Frequency	V _{DD} =3.0 V, T _A =30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16) ⁽²⁾	Duty Cycle	-	45	-	55	
Δ _{Temp} (HSI16)	HSI16 oscillator frequency drift over temperature	T _A = 0 to 85 °C	-1	-	1	
		T _A = -40 to 125 °C	-2	-	1.5	
Δ _{VDD} (HSI16)	HSI16 oscillator frequency drift over V _{DD}	V _{DD} =1.62 V to 3.6 V	-0.1	-	0.05	
t _{su} (HSI16) ⁽²⁾	HSI16 oscillator start-up time	-	-	0.8	1.2	μs
t _{stab} (HSI16) ⁽²⁾	HSI16 oscillator stabilization time	-	-	3	5	
I _{DD} (HSI16) ⁽²⁾	HSI16 oscillator power consumption	-	-	155	190	μA

1. Guaranteed by characterization results.

2. Guaranteed by design.

Figure 24. HSI16 frequency vs. temperature

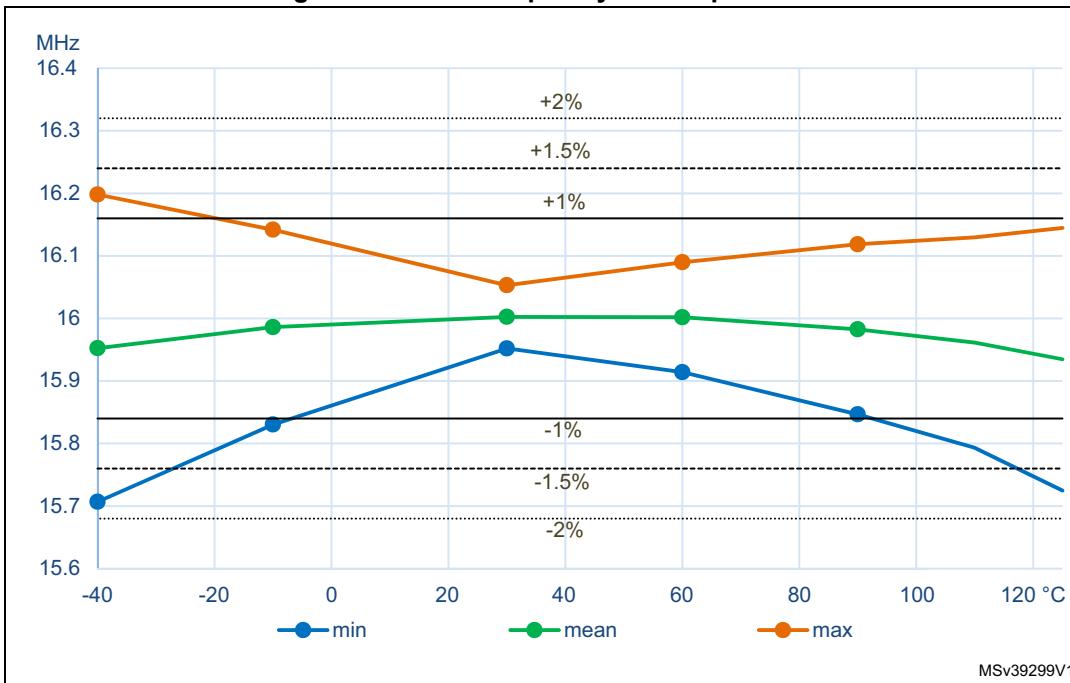
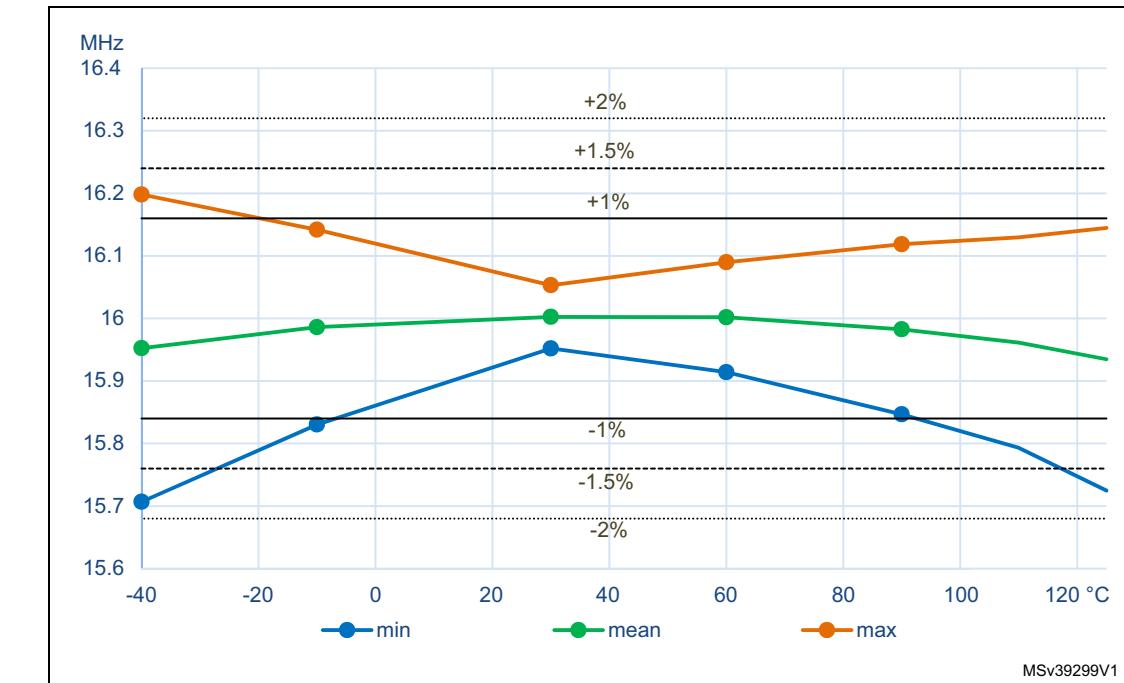


图24. HSI16频率与温度



Multi-speed internal (MSI) RC oscillator

Table 60. MSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at $V_{DD}=3$ V and $T_A=30$ °C	MSI mode	Range 0	98.7	100	101.3	kHz
			Range 1	197.4	200	202.6	
			Range 2	394.8	400	405.2	
			Range 3	789.6	800	810.4	
			Range 4	0.987	1	1.013	
			Range 5	1.974	2	2.026	
			Range 6	3.948	4	4.052	
			Range 7	7.896	8	8.104	
			Range 8	15.79	16	16.21	
			Range 9	23.69	24	24.31	
			Range 10	31.58	32	32.42	
			Range 11	47.38	48	48.62	
		PLL mode XTAL= 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	
			Range 5	-	1.999	-	
			Range 6	-	3.998	-	
			Range 7	-	7.995	-	
			Range 8	-	15.991	-	
			Range 9	-	23.986	-	
			Range 10	-	32.014	-	
			Range 11	-	48.005	-	
$\Delta_{TEMP}(MSI)^{(2)}$	MSI oscillator frequency drift over temperature	MSI mode	$T_A = -0$ to 85 °C	-3.5	-	3	%
			$T_A = -40$ to 125 °C	-8	-	6	

内部多速度RC振荡器

表 60. MSI 振荡器特性⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at $V_{DD}=3$ V and $T_A=30$ °C	MSI mode	Range 0	98.7	100	101.3	kHz
			Range 1	197.4	200	202.6	
			Range 2	394.8	400	405.2	
			Range 3	789.6	800	810.4	
			Range 4	0.987	1	1.013	
			Range 5	1.974	2	2.026	
			Range 6	3.948	4	4.052	
			Range 7	7.896	8	8.104	
			Range 8	15.79	16	16.21	
			Range 9	23.69	24	24.31	
			Range 10	31.58	32	32.42	
			Range 11	47.38	48	48.62	
		PLL mode XTAL= 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	
			Range 5	-	1.999	-	
			Range 6	-	3.998	-	
			Range 7	-	7.995	-	
			Range 8	-	15.991	-	
			Range 9	-	23.986	-	
			Range 10	-	32.014	-	
			Range 11	-	48.005	-	
$\Delta_{TEMP}(MSI)^{(2)}$	MSI oscillator frequency drift over temperature	MSI mode	$T_A = -0$ to 85 °C	-3.5	-	3	%
			$T_A = -40$ to 125 °C	-8	-	6	

Table 60. MSI oscillator characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit	
$\Delta V_{DD}(\text{MSI})^{(2)}$	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	$V_{DD} = 1.62$ to 3.6 V	-1.2	-	0.5	%	
				$V_{DD} = 2.4$ to 3.6 V	-0.5	-			
			Range 4 to 7	$V_{DD} = 1.62$ to 3.6 V	-2.5	-	0.7		
				$V_{DD} = 2.4$ to 3.6 V	-0.8	-			
		Range 8 to 11	Range 8 to 11	$V_{DD} = 1.62$ to 3.6 V	-5	-	1		
				$V_{DD} = 2.4$ to 3.6 V	-1.6	-			
$\Delta F_{\text{SAMPLING}}(\text{MSI})^{(2)(6)}$	Frequency variation in sampling mode ⁽³⁾	MSI mode	$T_A = -40$ to 85 °C		-	1	2	ns	
			$T_A = -40$ to 125 °C		-	2	4		
			For next transition	-	-	-	3.458		
$P_{\text{USB Jitter}}(\text{MSI})^{(6)}$	Period jitter for USB clock ⁽⁴⁾	PLL mode Range 11	For paired transition	-	-	-	3.916	ns	
			For next transition	-	-	-	2		
$MT_{\text{USB Jitter}}(\text{MSI})^{(6)}$	Medium term jitter for USB clock ⁽⁵⁾	PLL mode Range 11	For paired transition	-	-	-	1	ns	
			For next transition	-	-	-	2		
$CC_{\text{jitter}}(\text{MSI})^{(6)}$	RMS cycle-to-cycle jitter	PLL mode Range 11	-	-	60	-	ps	ps	
$P_{\text{jitter}}(\text{MSI})^{(6)}$	RMS period jitter	PLL mode Range 11	-	-	50	-			
$t_{\text{SU}}(\text{MSI})^{(6)}$	MSI oscillator start-up time	Range 0	-	-	10	20	μs	μs	
			-	-	5	10			
			-	-	4	8			
			-	-	3	7			
			-	-	3	6			
			-	-	2.5	6			
$t_{\text{STAB}}(\text{MSI})^{(6)}$	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	0.25	0.5	ms	ms	
			5 % of final frequency	-	0.5	1.25			
			1 % of final frequency	-	-	-			

表 60. MSI 振荡器特性⁽¹⁾ (继续)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit	
$\Delta V_{DD}(\text{MSI})^{(2)}$	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	$V_{DD} = 1.62$ to 3.6 V	-1.2	-	0.5	%	
				$V_{DD} = 2.4$ to 3.6 V	-0.5	-			
			Range 4 to 7	$V_{DD} = 1.62$ to 3.6 V	-2.5	-	0.7		
				$V_{DD} = 2.4$ to 3.6 V	-0.8	-			
		Range 8 to 11	Range 8 to 11	$V_{DD} = 1.62$ to 3.6 V	-5	-	1		
				$V_{DD} = 2.4$ to 3.6 V	-1.6	-			
$\Delta F_{\text{SAMPLING}}(\text{MSI})^{(2)(6)}$	Frequency variation in sampling mode ⁽³⁾	MSI mode	$T_A = -40$ to 85 °C		-	1	2	ns	
			$T_A = -40$ to 125 °C		-	2	4		
			For next transition	-	-	-	3.458		
$P_{\text{USB Jitter}}(\text{MSI})^{(6)}$	Period jitter for USB clock ⁽⁴⁾	PLL mode Range 11	For paired transition	-	-	-	3.916	ns	
			For next transition	-	-	-	2		
$MT_{\text{USB Jitter}}(\text{MSI})^{(6)}$	Medium term jitter for USB clock ⁽⁵⁾	PLL mode Range 11	For paired transition	-	-	-	1	ns	
			For next transition	-	-	-	2		
$CC_{\text{jitter}}(\text{MSI})^{(6)}$	RMS cycle-to-cycle jitter	PLL mode Range 11			-	-	60	ps	
$P_{\text{jitter}}(\text{MSI})^{(6)}$	RMS period jitter	PLL mode Range 11			-	-	50		
$t_{\text{SU}}(\text{MSI})^{(6)}$	MSI oscillator start-up time	Range 0	-	-	10	20	μs	μs	
			-	-	5	10			
			-	-	4	8			
			-	-	3	7			
			-	-	3	6			
			-	-	2.5	6			
$t_{\text{STAB}}(\text{MSI})^{(6)}$	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms	
			5 % of final frequency	-	-	0.5	1.25		
			1 % of final frequency	-	-	-	2.5		

Electrical characteristics

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Table 60. MSI oscillator characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DD(MSI)}^{(6)}$	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1
			Range 1	-	-	0.8	1.2
			Range 2	-	-	1.2	1.7
			Range 3	-	-	1.9	2.5
			Range 4	-	-	4.7	6
			Range 5	-	-	6.5	9
			Range 6	-	-	11	15
			Range 7	-	-	18.5	25
			Range 8	-	-	62	80
			Range 9	-	-	85	110
			Range 10	-	-	110	130
			Range 11	-	-	155	190

μA

Electrical characteristics

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表 60. MSI 振荡器特性⁽¹⁾ (继续)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DD(MSI)}^{(6)}$	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1
			Range 1	-	-	0.8	1.2
			Range 2	-	-	1.2	1.7
			Range 3	-	-	1.9	2.5
			Range 4	-	-	4.7	6
			Range 5	-	-	6.5	9
			Range 6	-	-	11	15
			Range 7	-	-	18.5	25
			Range 8	-	-	62	80
			Range 9	-	-	85	110
			Range 10	-	-	110	130
			Range 11	-	-	155	190

μA

1. Guaranteed by characterization results.
2. This is a deviation for an individual part once the initial frequency has been measured.
3. Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.
4. Average period of MSI at 48 MHz is compared to a real 48 MHz clock over 28 cycles. It includes frequency tolerance + jitter of MSI at 48 MHz clock.
5. Only accumulated jitter of MSI at 48 MHz is extracted over 28 cycles.
For next transition: min. and max. jitter of 2 consecutive frame of 28 cycles of the MSI at 48 MHz, for 1000 captures over 28 cycles.
For paired transitions: min. and max. jitter of 2 consecutive frame of 56 cycles of the MSI at 48 MHz, for 1000 captures over 56 cycles.
6. Guaranteed by design.

1. Guaranteed by characterization results.
2. This is a deviation for an individual part once the initial frequency has been measured.
3. Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.
4. Average period of MSI at 48 MHz is compared to a real 48 MHz clock over 28 cycles. It includes frequency tolerance + jitter of MSI at 48 MHz clock.
5. Only accumulated jitter of MSI at 48 MHz is extracted over 28 cycles.
For next transition: min. and max. jitter of 2 consecutive frame of 28 cycles of the MSI at 48 MHz, for 1000 captures over 28 cycles.
For paired transitions: min. and max. jitter of 2 consecutive frame of 56 cycles of the MSI at 48 MHz, for 1000 captures over 56 cycles.
6. Guaranteed by design.

Figure 25. Typical current consumption vs. MSI frequency

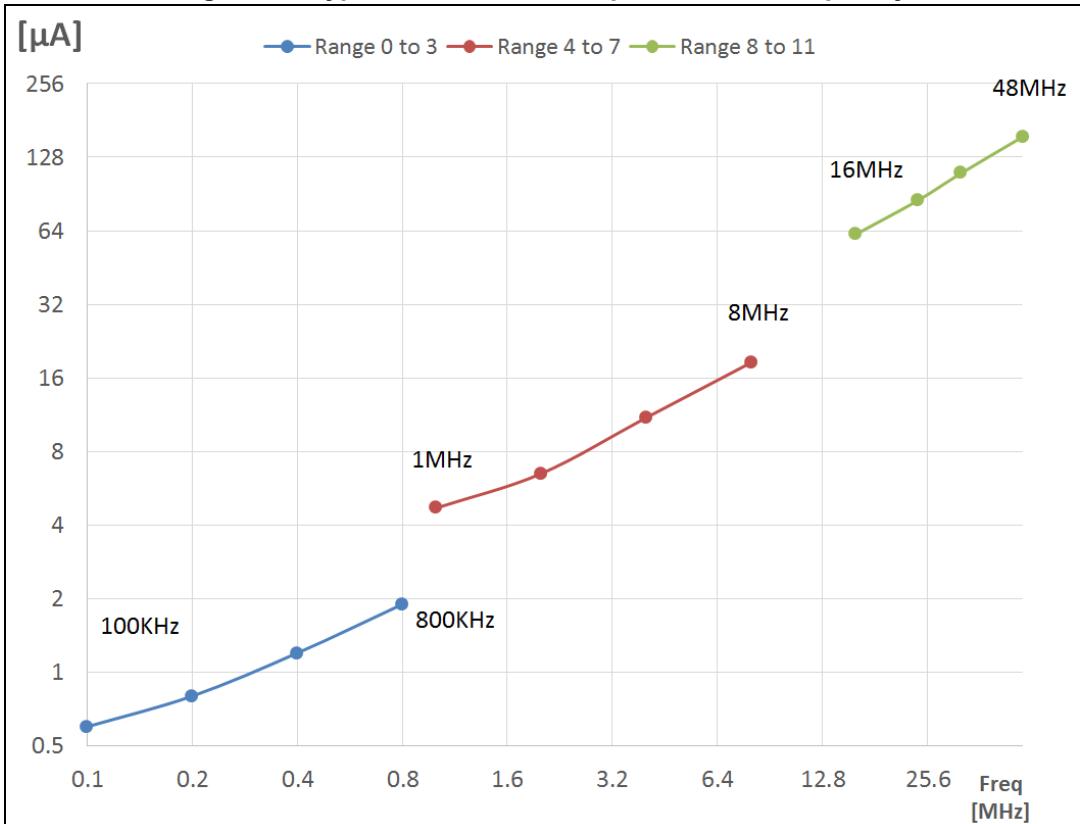
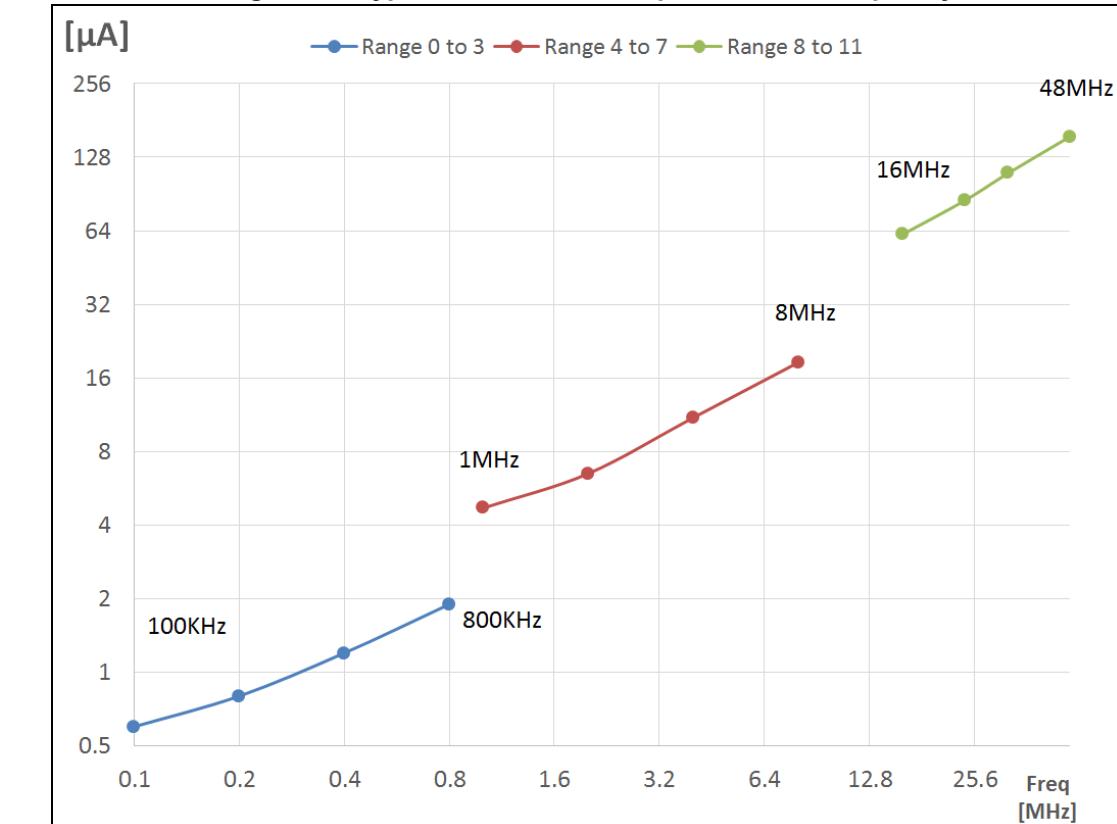


Figure 25. Typical current consumption vs. MSI frequency



High-speed internal 48 MHz (HSI48) RC oscillator

Table 61. HSI48 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{HSI48}	HSI48 frequency	V _{DD} = 3.0 V, T _A = 30 °C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11 ⁽²⁾	0.18 ⁽²⁾	
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3 ⁽³⁾	±3.5 ⁽³⁾	-	%
DuC(y)(HSI48)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	
ACC _{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V _{DD} = 3.0 V to 3.6 V, T _A = -15 to 85 °C	-	-	±3 ⁽³⁾	%
		V _{DD} = 1.65 V to 3.6 V, T _A = -40 to 125 °C	-	-	±4.5 ⁽³⁾	
D _{VDD(HSI48)}	HSI48 oscillator frequency drift with V _{DD}	V _{DD} = 3 V to 3.6 V	-	0.025 ⁽³⁾	0.05 ⁽³⁾	
		V _{DD} = 1.65 V to 3.6 V	-	0.05 ⁽³⁾	0.1 ⁽³⁾	
t _{su} (HSI48)	HSI48 oscillator start-up time	-	2.5 ⁽²⁾	6 ⁽²⁾	μs	
I _{DD(HSI48)}	HSI48 oscillator power consumption	-	340 ⁽²⁾	380 ⁽²⁾	µA	

High-speed internal 48 MHz (HSI48) RC oscillator

Table 61. HSI48 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{HSI48}	HSI48 frequency	V _{DD} = 3.0 V, T _A = 30 °C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11 ⁽²⁾	0.18 ⁽²⁾	
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3 ⁽³⁾	±3.5 ⁽³⁾	-	%
DuC(y)(HSI48)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	
ACC _{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V _{DD} = 3.0 V to 3.6 V, T _A = -15 to 85 °C	-	-	±3 ⁽³⁾	%
		V _{DD} = 1.65 V to 3.6 V, T _A = -40 to 125 °C	-	-	±4.5 ⁽³⁾	
D _{VDD(HSI48)}	HSI48 oscillator frequency drift with V _{DD}	V _{DD} = 3 V to 3.6 V	-	0.025 ⁽³⁾	0.05 ⁽³⁾	
		V _{DD} = 1.65 V to 3.6 V	-	0.05 ⁽³⁾	0.1 ⁽³⁾	
t _{su} (HSI48)	HSI48 oscillator start-up time	-	2.5 ⁽²⁾	6 ⁽²⁾	μs	
I _{DD(HSI48)}	HSI48 oscillator power consumption	-	340 ⁽²⁾	380 ⁽²⁾	µA	

Electrical characteristics

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Table 61. HSI48 oscillator characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N _T jitter	Next transition jitter Accumulated jitter on 28 cycles ⁽⁴⁾	-	-	±0.15 ⁽²⁾	-	ns
P _T jitter	Paired transition jitter Accumulated jitter on 56 cycles ⁽⁴⁾	-	-	±0.25 ⁽²⁾	-	ns

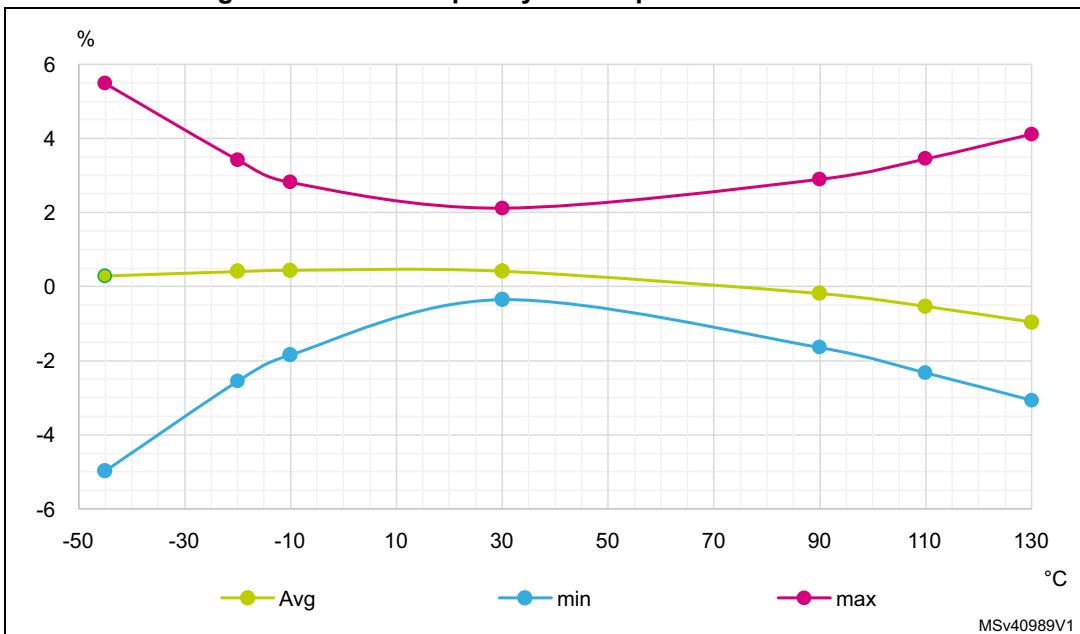
1. V_{DD} = 3 V, T_A = -40 to 125 °C unless otherwise specified.

2. Guaranteed by design.

3. Guaranteed by characterization results.

4. Jitter measurement are performed without clock source activated in parallel.

Figure 26. HSI48 frequency vs. temperature



Electrical characteristics

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Table 61. HSI48 oscillator characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N _T jitter	Next transition jitter Accumulated jitter on 28 cycles ⁽⁴⁾	-	-	±0.15 ⁽²⁾	-	ns
P _T jitter	Paired transition jitter Accumulated jitter on 56 cycles ⁽⁴⁾	-	-	±0.25 ⁽²⁾	-	ns

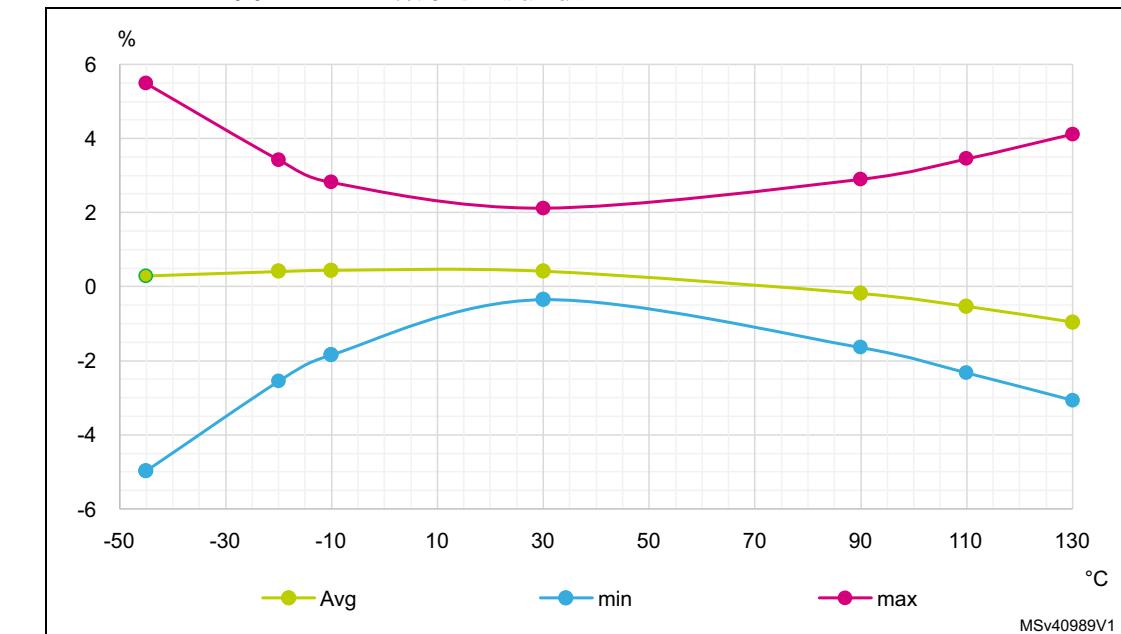
1. V_{DD} = 3 V, T_A = -40 to 125 °C unless otherwise specified.

2. Guaranteed by design.

3. Guaranteed by characterization results.

4. Jitter measurement are performed without clock source activated in parallel.

图 26. HSI48 频率与温度比较



Low-speed internal (LSI) RC oscillator

Table 62. LSI1 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{LSI}	LSI1 frequency	V _{DD} = 3.0 V, T _A = 30 °C	31.04	-	32.96	kHz
		V _{DD} = 1.62 to 3.6 V, T _A = -40 to 125 °C	29.5	-	34	
t _{SU} (LSI1) ⁽²⁾	LSI1 oscillator start-up time	-	-	80	130	μs
t _{STAB} (LSI1) ⁽²⁾	LSI1 oscillator stabilization time	5% of final frequency	-	125	180	
I _{DD} (LSI1) ⁽²⁾	LSI1 oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.

2. Guaranteed by design.

Low-speed internal (LSI) RC oscillator

Table 62. LSI1 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{LSI}	LSI1 frequency	V _{DD} = 3.0 V, T _A = 30 °C	31.04	-	32.96	kHz
		V _{DD} = 1.62 to 3.6 V, T _A = -40 to 125 °C	29.5	-	34	
t _{SU} (LSI1) ⁽²⁾	LSI1 oscillator start-up time	-	-	80	130	μs
t _{STAB} (LSI1) ⁽²⁾	LSI1 oscillator stabilization time	5% of final frequency	-	125	180	
I _{DD} (LSI1) ⁽²⁾	LSI1 oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.

2. Guaranteed by design.

Table 63. LSI2 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI2}	LSI2 frequency	$V_{DD} = 3.0 \text{ V}, T_A = 30^\circ\text{C}$	21.6	-	44.2	kHz
		$V_{DD} = 1.62 \text{ to } 3.6 \text{ V}, T_A = -40 \text{ to } 125^\circ\text{C}$	21.2	-	44.4	
$t_{SU}(LSI2)^{(2)}$	LSI2 oscillator start-up time	-	0.7	-	3.5	ms
$I_{DD}(LSI2)^{(2)}$	LSI2 oscillator power consumption	-	-	500	1180	nA

1. Guaranteed by characterization results.

2. Guaranteed by design.

6.3.12 PLL characteristics

The parameters given in [Table 64](#) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 64. PLL, PLLSAI1 characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock ⁽²⁾	-	2.66	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	2	-	64	MHz
		Voltage scaling Range 2	2	-	16	
$f_{PLL_Q_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	8	-	64	MHz
		Voltage scaling Range 2	8	-	16	
$f_{PLL_R_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	8	-	64	MHz
		Voltage scaling Range 2	8	-	16	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	96	-	344	MHz
		Voltage scaling Range 2	64	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	μs
Jitter	RMS cycle-to-cycle jitter	System clock 64 MHz	-	40	-	ps
	RMS period jitter		-	30	-	
$I_{DD}(PLL)$	PLL power consumption on $V_{DD}^{(1)}$	VCO freq = 96 MHz	-	200	260	μA
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.

2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the two PLLs.

Table 63. LSI2 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI2}	LSI2 frequency	$V_{DD} = 3.0 \text{ V}, T_A = 30^\circ\text{C}$	21.6	-	44.2	kHz
		$V_{DD} = 1.62 \text{ to } 3.6 \text{ V}, T_A = -40 \text{ to } 125^\circ\text{C}$	21.2	-	44.4	
$t_{SU}(LSI2)^{(2)}$	LSI2 oscillator start-up time	-	-	0.7	-	3.5 ms
$I_{DD}(LSI2)^{(2)}$	LSI2 oscillator power consumption	-	-	-	500	1180 nA

1. Guaranteed by characterization results.

2. Guaranteed by design.

6.3.12 PLL characteristics

The parameters given in [Table 64](#) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 64. PLL, PLLSAI1 characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock ⁽²⁾	-	2.66	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	2	-	64	MHz
		Voltage scaling Range 2	2	-	16	
$f_{PLL_Q_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	8	-	64	MHz
		Voltage scaling Range 2	8	-	16	
$f_{PLL_R_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	8	-	64	MHz
		Voltage scaling Range 2	8	-	16	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	96	-	344	MHz
		Voltage scaling Range 2	64	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	μs
Jitter	RMS cycle-to-cycle jitter	System clock 64 MHz	-	40	-	ps
	RMS period jitter		-	30	-	
$I_{DD}(PLL)$	PLL power consumption on $V_{DD}^{(1)}$	VCO freq = 96 MHz	-	200	260	μA
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.

2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the two PLLs.

6.3.13 Flash memory characteristics

Table 65. Flash memory characteristics⁽¹⁾

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.7	90.8	μs
$t_{\text{prog_row}}$	One row (64 double word) programming time	Normal programming	5.2	5.5	ms
		Fast programming	3.8	4.0	
$t_{\text{prog_page}}$	One page (4 Kbytes) programming time	Normal programming	41.8	43.0	
		Fast programming	30.4	31.0	
t_{ERASE}	Page (4 Kbytes) erase time	-	22.0	24.5	
t_{ME}	Mass erase time	-	22.1	25.0	
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	

1. Guaranteed by design.

Table 66. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min ⁽¹⁾	Unit
N_{END}	Endurance	$T_A = -40$ to $+105$ °C	10	kcycles
t_{RET}	Data retention	1 kcycle ⁽²⁾ at $T_A = 85$ °C	30	Years
		1 kcycle ⁽²⁾ at $T_A = 105$ °C	15	
		1 kcycle ⁽²⁾ at $T_A = 125$ °C	7	
		10 kcycles ⁽²⁾ at $T_A = 55$ °C	30	
		10 kcycles ⁽²⁾ at $T_A = 85$ °C	15	
		10 kcycles ⁽²⁾ at $T_A = 105$ °C	10	

1. Guaranteed by characterization results.

2. Cycling performed over the whole temperature range.

6.3.13 Flash memory characteristics

Table 65. Flash memory characteristics⁽¹⁾

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.7	90.8	μs
$t_{\text{prog_row}}$	One row (64 double word) programming time	Normal programming	5.2	5.5	ms
		Fast programming	3.8	4.0	
$t_{\text{prog_page}}$	One page (4 Kbytes) programming time	Normal programming	41.8	43.0	
		Fast programming	30.4	31.0	
t_{ERASE}	Page (4 Kbytes) erase time	-	22.0	24.5	
t_{ME}	Mass erase time	-	22.1	25.0	
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	

1. Guaranteed by design.

Table 66. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min ⁽¹⁾	Unit
N_{END}	Endurance	$T_A = -40$ to $+105$ °C	10	kcycles
t_{RET}	Data retention	1 kcycle ⁽²⁾ at $T_A = 85$ °C	30	Years
		1 kcycle ⁽²⁾ at $T_A = 105$ °C	15	
		1 kcycle ⁽²⁾ at $T_A = 125$ °C	7	
		10 kcycles ⁽²⁾ at $T_A = 55$ °C	30	
		10 kcycles ⁽²⁾ at $T_A = 85$ °C	15	
		10 kcycles ⁽²⁾ at $T_A = 105$ °C	10	

1. Guaranteed by characterization results.

2. Cycling performed over the whole temperature range.

6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operation to be resumed.

The test results are given in [Table 67](#). They are based on the EMS levels and classes defined in AN1709 “EMC design guide for STM8, STM32 and Legacy MCUs”, available on www.st.com.

Table 67. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3 \text{ V}$, $T_A = +25^\circ\text{C}$, $f_{HCLK} = 64 \text{ MHz}$, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3 \text{ V}$, $T_A = +25^\circ\text{C}$, $f_{HCLK} = 64 \text{ MHz}$, conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software.

Good EMC performance is highly dependent on the user application and the software in particular. Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for the application.

Software recommendations

The software flow must include the management of runaway conditions such as:

- corrupted program counter
- unexpected reset
- critical data corruption (e.g. control registers)

6.3.14 电磁兼容性特性

感应性测试在设备特征化过程中以样本为基础进行。

功能性 EMS (电磁感应性)

在设备 (上执行简单应用时, 通过输入/输出端口) 按钮 2 个 LED。该设备受到两个电磁事件的压力, 直到发生故障。故障由 LED 指示:

- **静电放电 (ESD)** (正负) 被应用于所有设备引脚, 直到发生功能性干扰。此测试符合IEC 61000-4-2标准。
- **FTB**: 快速暂态电压冲击 (正负) 通过100 pF 电容被应用于VDD和VSS, 直到发生功能性干扰。此测试符合IEC 61000-4-4标准。

设备重置允许恢复正常运行。

测试结果在表67中给出。它们基于AN1709 “STM8、STM32和遗留 MCUs的EMC 设计指南” 中定义的EMS 级别和类别www.st.com上可用。

Table 67. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3 \text{ V}$, $T_A = +25^\circ\text{C}$, $f_{HCLK} = 64 \text{ MHz}$, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3 \text{ V}$, $T_A = +25^\circ\text{C}$, $f_{HCLK} = 64 \text{ MHz}$, conforming to IEC 61000-4-4	5A

设计强壮的软件以避免噪声问题

EMC 特征化和优化在典型的应用环境中以组件级进行，使用简化的 MCU 软件。

良好的电磁兼容性性能高度依赖于用户应用程序和软件。因此，建议用户在与应用程序所需的电磁兼容性水平相关的情况下，应用电磁兼容性软件优化和预先合格测试。

软件建议

软件流程必须包括管理失控状态，例如：

- 损坏的计数器
- 意外复位
- 关键数据损坏 (例如：控制寄存器)

Electrical characteristics

STM32WB55xx STM32WB35xx

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling two LEDs through the I/O ports). This emission test is compliant with the IEC 61967-2 standard, which specifies the test board and the pin loading.

Table 68. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Peripheral ON SMPS OFF or ON [f _{HSE} / f _{CPUM4} , f _{CPUM0}]	Unit
				32 MHz / 64 MHz, 32 MHz	
S _{EMI}	Peak level	V _{DD} = 3.6 V, T _A = 25 °C, WLCSP100 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	1	dB _μ V
			30 MHz to 130 MHz	4	
			130 MHz to 1 GHz	-1	
			1 GHz to 2 GHz	7	
			EMI level	1.5	
				-	

6.3.15 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 69. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device model)	T _A = +25 °C, conforming to ANSI/ESD STM5.3.1 JS-002		C2a ⁽²⁾ C1 ⁽³⁾	

1. Guaranteed by characterization results.

2. UFQFPN48, VFQPN68 and WLCSP100 packages.

3. UFBGA129 package.

Electrical characteristics

STM32WB55xx STM32WB35xx

预先资质试验

大多数常见的故障，例如意外复位和程序计数器损坏，可以通过手动将 NRST 引脚或振荡器引脚保持在低状态 1 秒来重现。

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

设备发出的电磁场在执行简单应用时被监测，该应用通过输入/输出端口切换两个LED (。这次发射测试符合IEC 61967-2标准，该标准规定了测试板和引脚负载。

Table 68. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Peripheral ON SMPS OFF or ON [f _{HSE} / f _{CPUM4} , f _{CPUM0}]	Unit
				32 MHz / 64 MHz, 32 MHz	
S _{EMI}	Peak level	V _{DD} = 3.6 V, T _A = 25 °C, WLCSP100 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	1	dB _μ V
			30 MHz to 130 MHz	4	
			130 MHz to 1 GHz	-1	
			1 GHz to 2 GHz	7	
			EMI level	1.5	
				-	

6.3.15 电气敏感性特性

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 69. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device model)	T _A = +25 °C, conforming to ANSI/ESD STM5.3.1 JS-002		C2a ⁽²⁾ C1 ⁽³⁾	

1. Guaranteed by characterization results.

2. UFQFPN48, VFQPN68 and WLCSP100 packages.

3. UFBGA129 package.



Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- a supply overvoltage is applied to each power supply pin
- a current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 70. Electrical sensitivity

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105^\circ\text{C}$ conforming to JESD78A	II

6.3.16 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 μA / 0 μA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in [Table 71](#).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 71. I/O current injection susceptibility⁽¹⁾

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins except PB0, PB1	-5	N/A ⁽²⁾	mA
	Injected current on PB0, PB1 pins	-5	0	

1. Guaranteed by characterization results.

2. Injection not possible.

静态锁存

Two complementary static tests are required on six parts to assess the latch-up performance:

- a supply overvoltage is applied to each power supply pin
- a current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 70. Electrical sensitivity

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105^\circ\text{C}$ conforming to JESD78A	II

6.3.16 I/O current injection characteristics

作为一般规则，由于外部电压低于 V_{SS} 或高于 V_{DD} (对于标准的 3.3 能力的 I/O 引脚)，在正常产品运行过程中应避免对 I/O 引脚进行电流注入。但是，为了在异常注入意外发生时提供微控制器韧性的指示，感应性测试会在设备特征化过程中以样本为基础进行。

对I/O电流注入的功能敏感性

在设备上执行简单应用程序时，通过将电流注入浮动输入模式下编程的输入/输出引脚来 stressing 力测试设备。在将电流注入输入/输出引脚时，逐个检查设备是否存在功能故障。

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 μA / 0 μA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in [Table 71](#).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 71. I/O current injection susceptibility⁽¹⁾

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins except PB0, PB1	-5	N/A ⁽²⁾	mA
	Injected current on PB0, PB1 pins	-5	0	

1. Guaranteed by characterization results.

2. Injection not possible.

6.3.17 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 72](#) are derived from tests performed under the conditions summarized in [Table 24: General operating conditions](#). All I/Os are designed as CMOS- and TTL-compliant.

Table 72. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage ⁽¹⁾	1.62 V < V_{DD} < 3.6 V	-	-	$0.3 \times V_{DD}$	V
	I/O input low level voltage ⁽²⁾				$0.39 \times V_{DD} - 0.06$	
V_{IH}	I/O input high level voltage ⁽¹⁾		$0.7 \times V_{DD}$	-	-	
	I/O input high level voltage ⁽²⁾		$0.49 \times V_{DD} + 0.26$	-	-	
V_{hys}	TT_xx, FT_xxx and NRST I/O input hysteresis		-	200	-	mV
I_{lkq}	FT_xx input leakage current	$0 \leq V_{IN} \leq \text{Max}(V_{DDXXX})^{(3)}$	-	-	± 100	nA
		$\text{Max}(V_{DDXXX}) \leq V_{IN} \leq \text{Max}(V_{DDXXX}) + 1 V^{(2)(3)(4)}$	-	-	650	
		$\text{Max}(V_{DDXXX}) + 1 V < V_{IN} \leq 5.5 V^{(2)(3)(4)(5)(6)}$	-	-	200 ⁽⁷⁾	
	FT_lu, FT_u and PC3 IO input leakage current	$0 \leq V_{IN} \leq \text{Max}(V_{DDXXX})^{(3)}$	-	-	± 150	
		$\text{Max}(V_{DDXXX}) \leq V_{IN} \leq \text{Max}(V_{DDXXX}) + 1 V^{(2)(3)}$	-	-	2500	
		$\text{Max}(V_{DDXXX}) + 1 V < V_{IN} \leq 5.5 V^{(1)(3)(4)(8)}$	-	-	250	
	TT_xx input leakage current	$V_{IN} \leq \text{Max}(V_{DDXXX})^{(3)}$	-	-	± 150	
		$\text{Max}(V_{DDXXX}) \leq V_{IN} < 3.6 V^{(3)}$	-	-	2000	
R_{PU}	Weak pull-up equivalent resistor ⁽¹⁾	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor ⁽¹⁾	$V_{IN} = V_{DD}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Tested in production.

2. Guaranteed by design, not tested in production.

3. Represents the pad leakage of the I/O itself. The total product pad leakage is given by $I_{Total_leak_max} = 10 \mu A + \text{number of I/Os where } V_{IN} \text{ is applied on the pad} \times I_{lkq}(\text{Max})$.

4. $\text{Max}(V_{DDXXX})$ is the maximum value among all the I/O supplies.

5. V_{IN} must be lower than $[\text{Max}(V_{DDXXX}) + 3.6 V]$.

6. Refer to [Figure 27: I/O input characteristics](#).

6.3.17 输入/输出 端口特性

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 72](#) are derived from tests performed under the conditions summarized in [Table 24: General operating conditions](#). All I/Os are designed as CMOS- and TTL-compliant.

Table 72. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage ⁽¹⁾	1.62 V < V_{DD} < 3.6 V	-	-	$0.3 \times V_{DD}$	V
	I/O input low level voltage ⁽²⁾				$0.39 \times V_{DD} - 0.06$	
V_{IH}	I/O input high level voltage ⁽¹⁾		$0.7 \times V_{DD}$	-	-	
	I/O input high level voltage ⁽²⁾		$0.49 \times V_{DD} + 0.26$	-	-	
V_{hys}	TT_xx, FT_xxx and NRST I/O input hysteresis		-	200	-	mV
I_{lkq}	FT_xx input leakage current	$0 \leq V_{IN} \leq \text{Max}(V_{DDXXX})^{(3)}$	-	-	± 100	nA
		$\text{Max}(V_{DDXXX}) \leq V_{IN} \leq \text{Max}(V_{DDXXX}) + 1 V^{(2)(3)(4)}$	-	-	650	
		$\text{Max}(V_{DDXXX}) + 1 V < V_{IN} \leq 5.5 V^{(2)(3)(4)(5)(6)}$	-	-	200 ⁽⁷⁾	
	FT_lu, FT_u and PC3 IO input leakage current	$0 \leq V_{IN} \leq \text{Max}(V_{DDXXX})^{(3)}$	-	-	± 150	
		$\text{Max}(V_{DDXXX}) \leq V_{IN} \leq \text{Max}(V_{DDXXX}) + 1 V^{(2)(3)}$	-	-	2500	
		$\text{Max}(V_{DDXXX}) + 1 V < V_{IN} \leq 5.5 V^{(1)(3)(4)(8)}$	-	-	250	
	TT_xx input leakage current	$V_{IN} \leq \text{Max}(V_{DDXXX})^{(3)}$	-	-	± 150	
		$\text{Max}(V_{DDXXX}) \leq V_{IN} < 3.6 V^{(3)}$	-	-	2000	
R_{PU}	Weak pull-up equivalent resistor ⁽¹⁾	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor ⁽¹⁾	$V_{IN} = V_{DD}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Tested in production.

2. Guaranteed by design, not tested in production.

3. Represents the pad leakage of the I/O itself. The total product pad leakage is given by $I_{Total_leak_max} = 10 \mu A + \text{number of I/Os where } V_{IN} \text{ is applied on the pad} \times I_{lkq}(\text{Max})$.

4. $\text{Max}(V_{DDXXX})$ is the maximum value among all the I/O supplies.

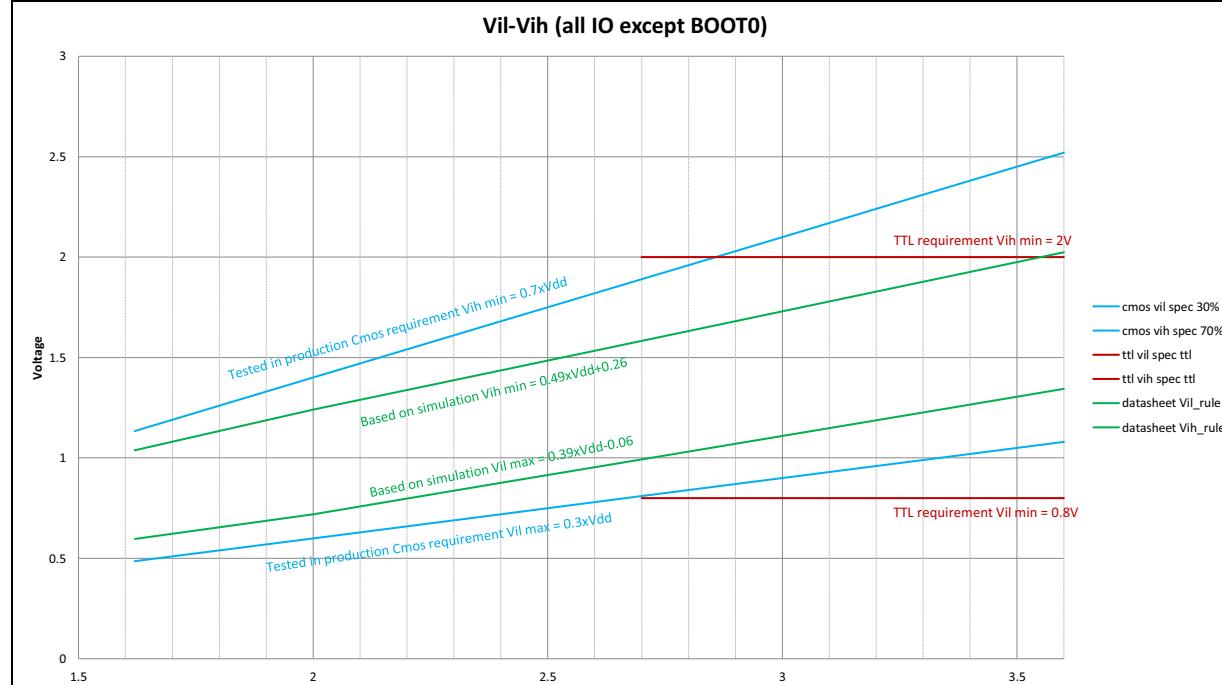
5. V_{IN} must be lower than $[\text{Max}(V_{DDXXX}) + 3.6 V]$.

6. Refer to [Figure 27: I/O input characteristics](#).

7. To sustain a voltage higher than $\text{Min}(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) + 0.3 \text{ V}$, the internal pull-up and pull-down resistors must be disabled. All FT_{xx} IO except FT_{Iu} , FT_{u} and $\text{PC}3$.
8. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS, whose contribution to the series resistance is minimal (~10%).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters, as shown in [Figure 27](#).

Figure 27. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to $\pm 8 \text{ mA}$, and sink or source up to $\pm 20 \text{ mA}$ (with a relaxed V_{OL} / V_{OH}).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#).

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see [Table 20: Voltage characteristics](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} , plus the maximum consumption of the MCU sunk on V_{SS} , cannot exceed the absolute maximum rating ΣI_{VSS} (see [Table 20: Voltage characteristics](#)).

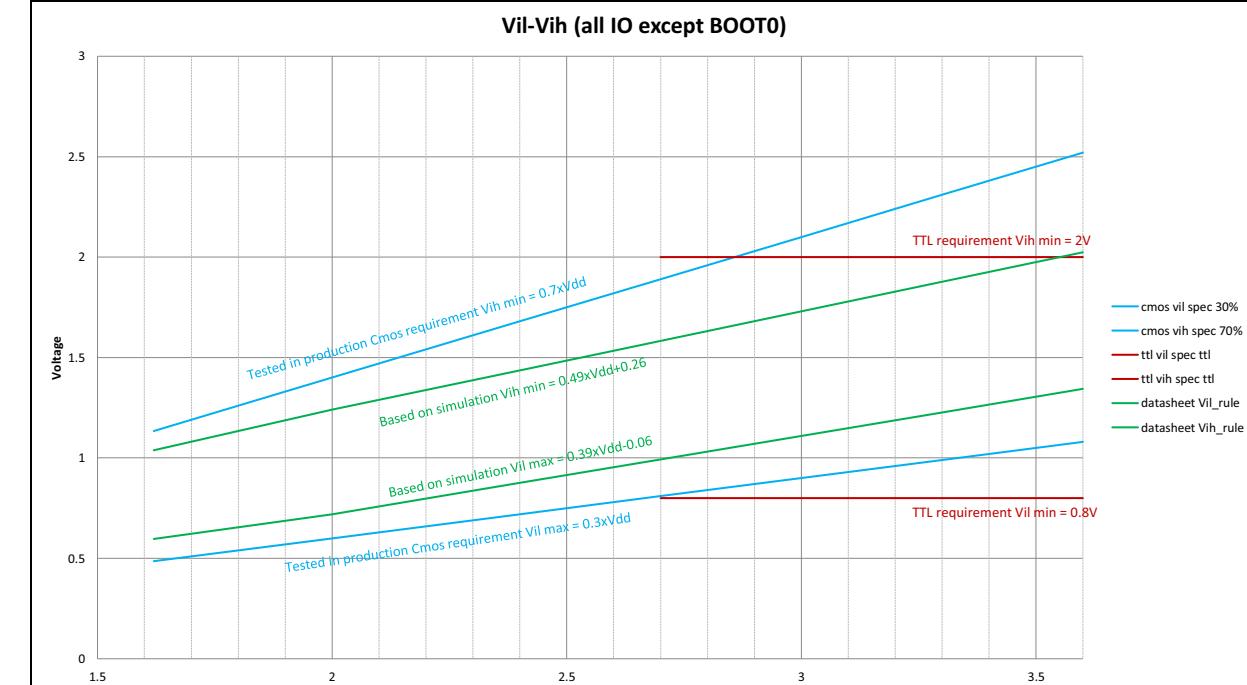
Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#). All I/Os are CMOS- and TTL-compliant (FT or TT unless otherwise specified).

7. To sustain a voltage higher than $\text{Min}(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) + 0.3 \text{ V}$, the internal pull-up and pull-down resistors must be disabled. All FT_{xx} IO except FT_{Iu} , FT_{u} and $\text{PC}3$.
8. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS, whose contribution to the series resistance is minimal (~10%).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters, as shown in [Figure 27](#).

图27. I/O 输入特性



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to $\pm 8 \text{ mA}$, and sink or source up to $\pm 20 \text{ mA}$ (with a relaxed V_{OL} / V_{OH}).

在用户应用程序中，必须限制可以驱动电流的 I/O 引脚数，以符合第6.2节指定的绝对最大额度。

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see [Table 20: Voltage characteristics](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} , plus the maximum consumption of the MCU sunk on V_{SS} , cannot exceed the absolute maximum rating ΣI_{VSS} (see [Table 20: Voltage characteristics](#)).

Output voltage levels

除非另有说明，下表中给出的参数是在环境温度和供电电压条件下进行测试得到的，这些条件总结在表 24：通用运行条件中。所有输入/输出都兼容 CMOS 和 TTL。

Table 73. Output voltage characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(2)}$	Output low level voltage for an I/O pin	CMOS port ⁽³⁾ $ I_{IO} = 8 \text{ mA}$ $V_{DD} \geq 2.7 \text{ V}$	-	0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin		$V_{DD} - 0.4$	-	
$V_{OL}^{(2)}$	Output low level voltage for an I/O pin		-	0.4	
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin	$ I_{IO} = 8 \text{ mA}$ $V_{DD} \geq 2.7 \text{ V}$	2.4	-	V
$V_{OL}^{(2)}$	Output low level voltage for an I/O pin		-	1.3	
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin		$V_{DD} - 1.3$	-	
$V_{OL}^{(2)}$	Output low level voltage for an I/O pin	$ I_{IO} = 4 \text{ mA}$ $V_{DD} \geq 1.62 \text{ V}$	-	0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin		$V_{DD} - 0.45$	-	
$V_{OLFM+}^{(2)}$	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$ I_{IO} = 20 \text{ mA}$ $V_{DD} \geq 2.7 \text{ V}$	-	0.4	
		$ I_{IO} = 10 \text{ mA}$ $V_{DD} \geq 1.62 \text{ V}$	-	0.4	
		$ I_{IO} = 2 \text{ mA}$ $1.62 \text{ V} \geq V_{DD} \geq 1.08 \text{ V}$	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 20: Voltage characteristics](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO} .

2. Guaranteed by design.

3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Table 74](#).

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 74. I/O AC characteristics⁽¹⁾⁽²⁾

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	$C=50 \text{ pF}, 2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	5	MHz
			$C=50 \text{ pF}, 1.62 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$	-	1	
			$C=10 \text{ pF}, 2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	10	
			$C=10 \text{ pF}, 1.62 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$	-	1.5	
	Tr/Tf	Output rise and fall time	$C=50 \text{ pF}, 2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	25	ns
			$C=50 \text{ pF}, 1.62 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$	-	52	
			$C=10 \text{ pF}, 2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	17	
			$C=10 \text{ pF}, 1.62 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$	-	37	

Table 73. Output voltage characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(2)}$	Output low level voltage for an I/O pin	CMOS port ⁽³⁾ $ I_{IO} = 8 \text{ mA}$ $V_{DD} \geq 2.7 \text{ V}$	-	0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin		$V_{DD} - 0.4$	-	
$V_{OL}^{(2)}$	Output low level voltage for an I/O pin		-	0.4	
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin	$ I_{IO} = 8 \text{ mA}$ $V_{DD} \geq 2.7 \text{ V}$	2.4	-	V
$V_{OL}^{(2)}$	Output low level voltage for an I/O pin		-	1.3	
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin		$V_{DD} - 1.3$	-	
$V_{OL}^{(2)}$	Output low level voltage for an I/O pin	$ I_{IO} = 4 \text{ mA}$ $V_{DD} \geq 1.62 \text{ V}$	-	0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin		$V_{DD} - 0.45$	-	
$V_{OLFM+}^{(2)}$	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$ I_{IO} = 20 \text{ mA}$ $V_{DD} \geq 2.7 \text{ V}$	-	0.4	
		$ I_{IO} = 10 \text{ mA}$ $V_{DD} \geq 1.62 \text{ V}$	-	0.4	
		$ I_{IO} = 2 \text{ mA}$ $1.62 \text{ V} \geq V_{DD} \geq 1.08 \text{ V}$	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 20: Voltage characteristics](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO} .

2. Guaranteed by design.

3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Table 74](#).

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 74. I/O AC characteristics⁽¹⁾⁽²⁾

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	$C=50 \text{ pF}, 2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	5	MHz
			$C=50 \text{ pF}, 1.62 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$	-	1	
			$C=10 \text{ pF}, 2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	10	
			$C=10 \text{ pF}, 1.62 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$	-	1.5	
	Tr/Tf	Output rise and fall time	$C=50 \text{ pF}, 2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	25	ns
			$C=50 \text{ pF}, 1.62 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$	-	52	
			$C=10 \text{ pF}, 2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	17	
			$C=10 \text{ pF}, 1.62 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$	-	37	

Table 74. I/O AC characteristics⁽¹⁾⁽²⁾ (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
01	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	25	MHz
			C=50 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	10	
			C=10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	50	
			C=10 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	15	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	9	ns
			C=50 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	16	
			C=10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	4.5	
			C=10 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	9	
10	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	50	MHz
			C=50 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	25	
			C=10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	100 ⁽³⁾	
			C=10 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	37.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	5.8	ns
			C=50 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	11	
			C=10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	2.5	
			C=10 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	5	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	120 ⁽³⁾	MHz
			C=30 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	50	
			C=10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	180 ⁽³⁾	
			C=10 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	75 ⁽³⁾	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	3.3	ns
			C=30 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	6	
			C=10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	1.7	
			C=10 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	3.3	

1. The maximum frequency is defined with $(T_r + T_f) \leq 2/3 T$, and Duty cycle comprised between 45 and 55%.

2. The fall and rise time are defined, respectively, between 90 and 10%, and between 10 and 90% of the output waveform.

3. This value represents the I/O capability but the maximum system frequency is limited to 64 MHz.

Table 74. I/O AC characteristics⁽¹⁾⁽²⁾ (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
01	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	25	MHz
			C=50 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	10	
			C=10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	50	
			C=10 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	15	
10	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	9	ns
			C=50 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	16	
			C=10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	4.5	
			C=10 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	9	
10	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	50	MHz
			C=50 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	25	
			C=10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	100 ⁽³⁾	
			C=10 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	37.5	
11	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	5.8	ns
			C=50 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	11	
			C=10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	2.5	
			C=10 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	5	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	120 ⁽³⁾	MHz
			C=30 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	50	
			C=10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	180 ⁽³⁾	
			C=10 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	75 ⁽³⁾	
11	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	3.3	ns
			C=30 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	6	
			C=10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	1.7	
			C=10 pF, 1.62 V ≤ V _{DD} ≤ 2.7 V	-	3.3	

1. The maximum frequency is defined with $(T_r + T_f) \leq 2/3 T$, and Duty cycle comprised between 45 and 55%.

2. The fall and rise time are defined, respectively, between 90 and 10%, and between 10 and 90% of the output waveform.

3. This value represents the I/O capability but the maximum system frequency is limited to 64 MHz.

6.3.18 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

6.3.18 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

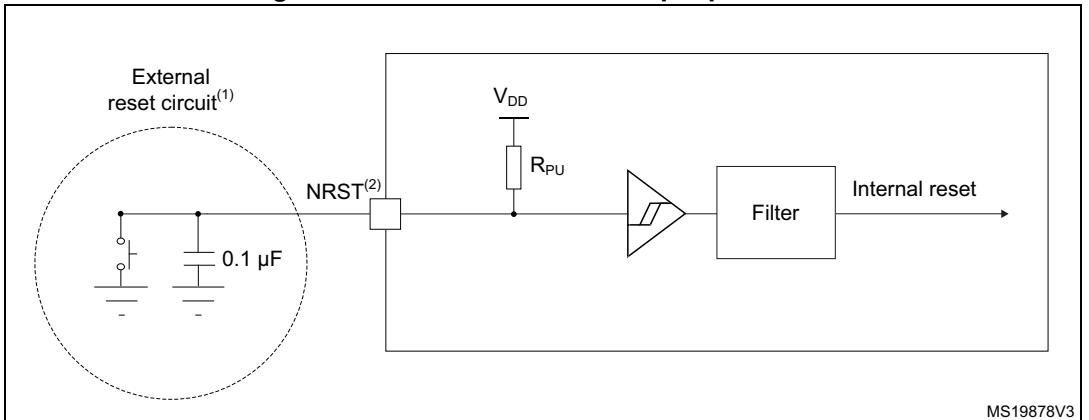
Table 75. NRST pin characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3 \times V_{DD}$	V
$V_{IH(NRST)}$	NRST input high level voltage		$0.7 \times V_{DD}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	$1.71 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	350	-	-	

1. Guaranteed by design.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10%).

Figure 28. Recommended NRST pin protection



- The reset network protects the device against parasitic resets.
- The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 75, otherwise the reset will not be taken into account by the device.
- The external capacitor on NRST must be placed as close as possible to the device.

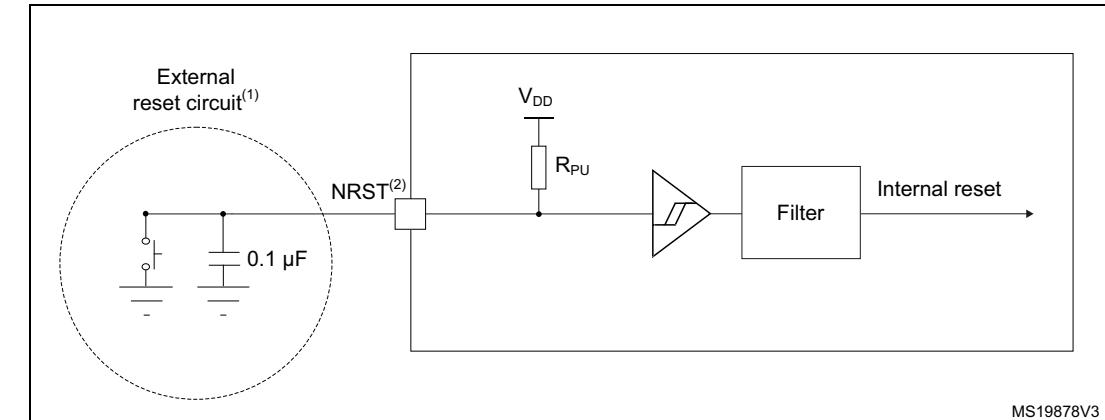
Table 75. NRST pin characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3 \times V_{DD}$	V
$V_{IH(NRST)}$	NRST input high level voltage		$0.7 \times V_{DD}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	$1.71 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	350	-	-	

1. Guaranteed by design.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10%).

图28. 推荐的 NRST 引脚保护



- The reset network protects the device against parasitic resets.
- The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 75, otherwise the reset will not be taken into account by the device.
- The external capacitor on NRST must be placed as close as possible to the device.

6.3.19 Analog switches booster

Table 76. Analog switches booster characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	μs
$I_{DD(BOOST)}$	Booster consumption for $1.62 \text{ V} \leq V_{DD} \leq 2.0 \text{ V}$	-	-	250	μA
	Booster consumption for $2.0 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$	-	-	500	
	Booster consumption for $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	-	900	

1. Guaranteed by design.

6.3.19 模拟开关增强器

表76. 模拟开关增强器特性⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	μs
$I_{DD(BOOST)}$	Booster consumption for $1.62 \text{ V} \leq V_{DD} \leq 2.0 \text{ V}$	-	-	250	μA
	Booster consumption for $2.0 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$	-	-	500	
	Booster consumption for $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	-	900	

1. Guaranteed by design.

6.3.20 Analog-to-Digital converter characteristics

Unless otherwise specified, the parameters given in [Table 77](#) are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in [Table 24: General operating conditions](#).

Note: *It is recommended to perform a calibration after each power-up.*

Table 77. ADC characteristics^{(1) (2) (3)}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2\text{ V}$	2	-	V_{DDA}	V
		$V_{DDA} < 2\text{ V}$		V_{DDA}		V
V_{REF-}	Negative reference voltage	-		V_{SSA}		V
f_{ADC}	ADC clock frequency	Range 1	0.14	-	64	MHz
		Range 2	0.14	-	16	
f_s	Sampling rate for FAST channels	Resolution = 12 bits	-	-	4.26	Msps
		Resolution = 10 bits	-	-	4.92	
		Resolution = 8 bits	-	-	5.81	
		Resolution = 6 bits	-	-	7.11	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	3.36	
		Resolution = 10 bits	-	-	4.00	
		Resolution = 8 bits	-	-	4.57	
		Resolution = 6 bits	-	-	7.11	
f_{TRIG}	External trigger frequency	$f_{ADC} = 64\text{ MHz}$	-	-	4.26	MHz
		Resolution = 12 bits	-	-	15	$1/f_{ADC}$
V_{CMIN}	Input common mode	Differential mode	$(V_{REF+} + V_{REF-})/2 - 0.18$	$(V_{REF+} + V_{REF-})/2$	$(V_{REF+} + V_{REF-})/2 + 0.18$	V
$V_{AIN}^{(4)}$	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-		1		Conversion cycle
t_{CAL}	Calibration time	$f_{ADC} = 64\text{ MHz}$		1.8125		μs
		-		116	$1/f_{ADC}$	

6.3.20 模拟-数字转换器特性

Unless otherwise specified, the parameters given in [Table 77](#) are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in [Table 24: General operating conditions](#).

注意：建议在每次上电后进行校准。

表 77. ADC 特性^{(1) (2) (3)}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2\text{ V}$	2	-	V_{DDA}	V
		$V_{DDA} < 2\text{ V}$		V_{DDA}		V
V_{REF-}	Negative reference voltage	-		V_{SSA}		V
f_{ADC}	ADC clock frequency	Range 1	0.14	-	64	MHz
		Range 2	0.14	-	16	
f_s	Sampling rate for FAST channels	Resolution = 12 bits	-	-	4.26	Msps
		Resolution = 10 bits	-	-	4.92	
		Resolution = 8 bits	-	-	5.81	
		Resolution = 6 bits	-	-	7.11	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	3.36	
		Resolution = 10 bits	-	-	4.00	
		Resolution = 8 bits	-	-	4.57	
		Resolution = 6 bits	-	-	7.11	
f_{TRIG}	External trigger frequency	$f_{ADC} = 64\text{ MHz}$	-	-	4.26	MHz
		Resolution = 12 bits	-	-	15	$1/f_{ADC}$
V_{CMIN}	Input common mode	Differential mode	$(V_{REF+} + V_{REF-})/2 - 0.18$	$(V_{REF+} + V_{REF-})/2$	$(V_{REF+} + V_{REF-})/2 + 0.18$	V
$V_{AIN}^{(4)}$	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-		1		Conversion cycle
t_{CAL}	Calibration time	$f_{ADC} = 64\text{ MHz}$		1.8125		μs
		-		116	$1/f_{ADC}$	

Table 77. ADC characteristics^{(1) (2) (3)} (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	$f_{ADC} = 64$ MHz	0.039	-	10.0	μs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG_STUP}$	ADC voltage regulator start-up time	-	-	-	20	μs
t_{CONV}	Total conversion time (including sampling time)	$f_{ADC} = 64$ MHz Resolution = 12 bits	0.234	-	1.019	μs
		Resolution = 12 bits	$t_s + 12.5$ cycles for successive approximations = 15 to 653			$1/f_{ADC}$
$I_{DDA}(ADC)$	ADC consumption from the V_{DDA} supply	fs = 4.26 Msps	-	730	830	μA
		fs = 1 Msps	-	160	220	
		fs = 10 ksp	-	16	50	
$I_{DDV_S}(ADC)$	ADC consumption from the V_{REF+} single ended mode	fs = 4.26 Msps	-	130	160	μA
		fs = 1 Msps	-	30	40	
		fs = 10 ksp	-	0.6	2	
$I_{DDV_D}(ADC)$	ADC consumption from the V_{REF+} differential mode	fs = 4.26 Msps	-	250	310	μA
		fs = 1 Msps	-	60	70	
		fs = 10 ksp	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enabled when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V.
3. SMPS in bypass mode.
4. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA} , depending on the package.
Refer to [Section 4: Pinouts and pin description](#) for further details.

Table 77. ADC characteristics^{(1) (2) (3)} (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	$f_{ADC} = 64$ MHz	0.039	-	10.0	μs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG_STUP}$	ADC voltage regulator start-up time	-	-	-	20	μs
t_{CONV}	Total conversion time (including sampling time)	$f_{ADC} = 64$ MHz Resolution = 12 bits	0.234	-	1.019	μs
		Resolution = 12 bits	$t_s + 12.5$ cycles for successive approximations = 15 to 653			$1/f_{ADC}$
$I_{DDA}(ADC)$	ADC consumption from the V_{DDA} supply	fs = 4.26 Msps	-	730	830	μA
		fs = 1 Msps	-	160	220	
		fs = 10 ksp	-	16	50	
$I_{DDV_S}(ADC)$	ADC consumption from the V_{REF+} single ended mode	fs = 4.26 Msps	-	130	160	μA
		fs = 1 Msps	-	30	40	
		fs = 10 ksp	-	0.6	2	
$I_{DDV_D}(ADC)$	ADC consumption from the V_{REF+} differential mode	fs = 4.26 Msps	-	250	310	μA
		fs = 1 Msps	-	60	70	
		fs = 10 ksp	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enabled when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V.
3. SMPS in bypass mode.
4. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA} , depending on the package.
Refer to [Section 4: Pinouts and pin description](#) for further details.

Table 78. ADC sampling time⁽¹⁾⁽²⁾

Resolution (bits)	RAIN (kΩ)	Fast channel		Slow channel	
		Minimum sampling time (ns)	Sampling cycles	Minimum sampling time (ns)	Sampling cycles
12	0	33	6.5	57	6.5
	0.05	37	6.5	62	6.5
	0.1	42	6.5	67	6.5
	0.2	51	6.5	76	6.5
	0.5	78	6.5	104	12.5
	1	123	12.5	151	12.5
	5	482	47.5	526	47.5
	10	931	92.5	994	92.5
	20	1830	247.5	1932	247.5
	50	4527	640.5	4744	640.5
	100	9021	640.5	9430	640.5
	0	27	2.5	47	6.5
10	0.05	30	2.5	51	6.5
	0.1	34	6.5	55	6.5
	0.2	41	6.5	62	6.5
	0.5	64	6.5	85	6.5
	1	100	12.5	124	12.5
	5	395	47.5	431	47.5
	10	763	92.5	816	92.5
	20	1500	247.5	1584	247.5
	50	3709	640.5	3891	640.5
	100	7391	640.5	7734	640.5
	0	21	2.5	37	2.5
	0.05	24	2.5	40	6.5
8	0.1	27	2.5	43	6.5
	0.2	32	6.5	49	6.5
	0.5	50	6.5	67	6.5
	1	78	6.5	97	6.5
	5	308	47.5	337	24.5
	10	595	92.5	637	47.5
	20	1169	247.5	1237	92.5
	50	2891	247.5	3037	247.5
	100	5762	640.5	6038	640.5

Table 78. ADC sampling time⁽¹⁾⁽²⁾

Resolution (bits)	RAIN (kΩ)	Fast channel		Slow channel	
		Minimum sampling time (ns)	Sampling cycles	Minimum sampling time (ns)	Sampling cycles
12	0	33	6.5	57	6.5
	0.05	37	6.5	62	6.5
	0.1	42	6.5	67	6.5
	0.2	51	6.5	76	6.5
	0.5	78	6.5	104	12.5
	1	123	12.5	151	12.5
	5	482	47.5	526	47.5
	10	931	92.5	994	92.5
	20	1830	247.5	1932	247.5
	50	4527	640.5	4744	640.5
	100	9021	640.5	9430	640.5
	0	27	2.5	47	6.5
10	0.05	30	2.5	51	6.5
	0.1	34	6.5	55	6.5
	0.2	41	6.5	62	6.5
	0.5	64	6.5	85	6.5
	1	100	12.5	124	12.5
	5	395	47.5	431	47.5
	10	763	92.5	816	92.5
	20	1500	247.5	1584	247.5
	50	3709	640.5	3891	640.5
	100	7391	640.5	7734	640.5
	0	21	2.5	37	2.5
	0.05	24	2.5	40	6.5
8	0.1	27	2.5	43	6.5
	0.2	32	6.5	49	6.5
	0.5	50	6.5	67	6.5
	1	78	6.5	97	6.5
	5	308	47.5	337	24.5
	10	595	92.5	637	47.5
	20	1169	247.5	1237	92.5
	50	2891	247.5	3037	247.5
	100	5762	640.5	6038	640.5



Table 78. ADC sampling time⁽¹⁾⁽²⁾ (continued)

Resolution (bits)	RAIN (kΩ)	Fast channel		Slow channel	
		Minimum sampling time (ns)	Sampling cycles	Minimum sampling time (ns)	Sampling cycles
6	0	15	2.5	26	2.5
	0.05	17	2.5	28	2.5
	0.1	19	2.5	31	2.5
	0.2	23	2.5	35	2.5
	0.5	36	6.5	48	6.5
	1	56	6.5	69	6.5
	5	221	24.5	242	24.5
	10	427	47.5	458	47.5
	20	839	92.5	890	92.5
	50	2074	247.5	2184	247.5
	100	4133	640.5	4342	640.5

1. Guaranteed by design.

2. $V_{DD} = 1.62$ V, $C_{pcb} = 4.7$ pF, 125 °C, booster enabled.Table 78. ADC sampling time⁽¹⁾⁽²⁾ (continued)

Resolution (bits)	RAIN (kΩ)	Fast channel		Slow channel	
		Minimum sampling time (ns)	Sampling cycles	Minimum sampling time (ns)	Sampling cycles
6	0	15	2.5	26	2.5
	0.05	17	2.5	28	2.5
	0.1	19	2.5	31	2.5
	0.2	23	2.5	35	2.5
	0.5	36	6.5	48	6.5
	1	56	6.5	69	6.5
	5	221	24.5	242	24.5
	10	427	47.5	458	47.5
	20	839	92.5	890	92.5
	50	2074	247.5	2184	247.5
	100	4133	640.5	4342	640.5

1. Guaranteed by design.

2. $V_{DD} = 1.62$ V, $C_{pcb} = 4.7$ pF, 125 °C, booster enabled.

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Table 79. ADC accuracy - Limited test conditions 1⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit	
ET	Total unadjusted error	Single ended Differential	Fast channel (max speed)	-	4	5		LSB	
			Slow channel (max speed)	-	4	5			
			Fast channel (max speed)	-	3.5	4.5			
			Slow channel (max speed)	-	3.5	4.5			
			Fast channel (max speed)	-	1	2.5			
	Offset error		Slow channel (max speed)	-	1	2.5			
			Fast channel (max speed)	-	1.5	2.5			
			Slow channel (max speed)	-	1.5	2.5			
			Fast channel (max speed)	-	2.5	4.5			
			Slow channel (max speed)	-	2.5	4.5			
EG	Gain error	Single ended Differential	Fast channel (max speed)	-	2.5	4.5		LSB	
			Slow channel (max speed)	-	2.5	4.5			
			Fast channel (max speed)	-	2.5	3.5			
			Slow channel (max speed)	-	2.5	3.5			
			Fast channel (max speed)	-	1	1.5			
	Differential linearity error		Slow channel (max speed)	-	1	1.5			
			Fast channel (max speed)	-	1	1.2			
			Slow channel (max speed)	-	1	1.2			
			Fast channel (max speed)	-	1.5	2.5			
			Slow channel (max speed)	-	1.5	2.5			
ED	Integral linearity error	Single ended Differential	Fast channel (max speed)	-	1	2		bits	
			Slow channel (max speed)	-	1	2			
			Fast channel (max speed)	-	1.5	2			
			Slow channel (max speed)	-	1.5	2			
			Fast channel (max speed)	10.4	10.5	-			
	ENOB		Slow channel (max speed)	10.4	10.5	-			
			Fast channel (max speed)	10.8	10.9	-			
			Slow channel (max speed)	10.8	10.9	-			
			Fast channel (max speed)	64.4	65	-			
			Slow channel (max speed)	64.4	65	-			
SINAD	Signal-to-noise and distortion ratio	Single ended Differential	Fast channel (max speed)	66.8	67.4	-		dB	
			Slow channel (max speed)	66.8	67.4	-			
			Fast channel (max speed)	65	66	-			
			Slow channel (max speed)	65	66	-			
			Fast channel (max speed)	67	68	-			
	SNR		Slow channel (max speed)	67	68	-			
			Fast channel (max speed)	65	66	-			
			Slow channel (max speed)	65	66	-			
			Fast channel (max speed)	67	68	-			
			Slow channel (max speed)	67	68	-			

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表79. ADC 精度 - 有限测试条件 1⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit	
ET	Total unadjusted error	Single ended Differential	Fast channel (max speed)	-	4	5		LSB	
			Slow channel (max speed)	-	4	5			
			Fast channel (max speed)	-	3.5	4.5			
			Slow channel (max speed)	-	3.5	4.5			
	Offset error		Fast channel (max speed)	-	1	2.5			
			Slow channel (max speed)	-	1	2.5			
			Fast channel (max speed)	-	1.5	2.5			
			Slow channel (max speed)	-	1.5	2.5			
			Fast channel (max speed)	-	2.5	4.5			
EG	Gain error		Slow channel (max speed)	-	2.5	4.5			
			Fast channel (max speed)	-	2.5	3.5			
			Slow channel (max speed)	-	2.5	3.5			
			Fast channel (max speed)	-	1	1.5			
			Slow channel (max speed)	-	1	1.5			
	Differential linearity error		Fast channel (max speed)	-	1	1.2		bits	
			Slow channel (max speed)	-	1	1.2			
			Fast channel (max speed)	-	1.5	2.5			
			Slow channel (max speed)	-	1.5	2.5			
			Fast channel (max speed)	-	1	2			
EL	Integral linearity error	Single ended Differential	Slow channel (max speed)	-	1	2		bits	
			Fast channel (max speed)	10.4	10.5	-			
			Slow channel (max speed)	10.4	10.5	-			
			Fast channel (max speed)	10.8	10.9	-			
			Slow channel (max speed)	10.8	10.9	-			
	ENOB		Fast channel (max speed)	64.4	65	-		dB	
			Slow channel (max speed)	64.4	65	-			
			Fast channel (max speed)	66.8	67.4	-			
			Slow channel (max speed)	66.8	67.4	-			
			Fast channel (max speed)	65	66	-			
SINAD	Signal-to-noise and distortion ratio	Single ended Differential	Slow channel (max speed)	65	66	-		dB	
			Fast channel (max speed)	67	68	-			
			Slow channel (max speed)	67	68	-			
			Fast channel (max speed)	64.4	65	-			
			Slow channel (max speed)	64.4	65	-			
	SNR		Fast channel (max speed)	66.8	67.4	-			
			Slow channel (max speed)	66.8	67.4	-			
			Fast channel (max speed)	65	66	-			
			Slow channel (max speed)	65	66	-			
			Fast channel (max speed)	67	68	-			

Table 79. ADC accuracy - Limited test conditions 1⁽¹⁾⁽²⁾⁽³⁾ (continued)

Symbol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
THD	Total harmonic distortion	Single ended	Fast channel (max speed)	-	-74	-73	dB	
			Slow channel (max speed)	-	-74	-73		
		Differential	Fast channel (max speed)	-	-79	-76		
			Slow channel (max speed)	-	-79	-76		
	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, $V_{DDA} = V_{REF^+} = 3V$, $TA = 25^\circ C$		Fast channel (max speed)	-	-74	-73	dB	
			Slow channel (max speed)	-	-74	-73		
			Fast channel (max speed)	-	-79	-76		
			Slow channel (max speed)	-	-79	-76		

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V. No oversampling.

Table 79. ADC accuracy - Limited test conditions 1⁽¹⁾⁽²⁾⁽³⁾ (continued)

Symbol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
THD	Total harmonic distortion	Single ended	Fast channel (max speed)	-	-74	-73	dB	
			Slow channel (max speed)	-	-74	-73		
		Differential	Fast channel (max speed)	-	-79	-76		
			Slow channel (max speed)	-	-79	-76		
	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, $V_{DDA} = V_{REF^+} = 3V$, $TA = 25^\circ C$		Fast channel (max speed)	-	-74	-73	dB	
			Slow channel (max speed)	-	-74	-73		
			Fast channel (max speed)	-	-79	-76		
			Slow channel (max speed)	-	-79	-76		

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V. No oversampling.

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Table 80. ADC accuracy - Limited test conditions 2⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	Fast channel (max speed)	-	4	6.5		LSB
			Slow channel (max speed)	-	4	6.5		
		Differential	Fast channel (max speed)	-	3.5	5.5		
			Slow channel (max speed)	-	3.5	5.5		
	Offset error	Single ended	Fast channel (max speed)	-	1	4.5		
			Slow channel (max speed)	-	1	5		
		Differential	Fast channel (max speed)	-	1.5	3		
			Slow channel (max speed)	-	1.5	3		
	Gain error	Single ended	Fast channel (max speed)	-	2.5	6		
			Slow channel (max speed)	-	2.5	6		
		Differential	Fast channel (max speed)	-	2.5	3.5		
			Slow channel (max speed)	-	2.5	3.5		
	Differential linearity error	Single ended	Fast channel (max speed)	-	1	1.5		
			Slow channel (max speed)	-	1	1.5		
		Differential	Fast channel (max speed)	-	1	1.2		
			Slow channel (max speed)	-	1	1.2		
	Integral linearity error	Single ended	Fast channel (max speed)	-	1.5	3.5		
			Slow channel (max speed)	-	1.5	3.5		
		Differential	Fast channel (max speed)	-	1	3		
			Slow channel (max speed)	-	1	2.5		
	ENOB	Single ended	Fast channel (max speed)	10	10.5	-		bits
			Slow channel (max speed)	10	10.5	-		
		Differential	Fast channel (max speed)	10.7	10.9	-		
			Slow channel (max speed)	10.7	10.9	-		
	SINAD	Single ended	Fast channel (max speed)	62	65	-		dB
			Slow channel (max speed)	62	65	-		
		Differential	Fast channel (max speed)	66	67.4	-		
			Slow channel (max speed)	66	67.4	-		
	SNR	Single ended	Fast channel (max speed)	64	66	-		
			Slow channel (max speed)	64	66	-		
		Differential	Fast channel (max speed)	66.5	68	-		
			Slow channel (max speed)	66.5	68	-		

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表80. ADC 精度 - 有限测试条件 2⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	Fast channel (max speed)	-	4	6.5		LSB
			Slow channel (max speed)	-	4	6.5		
		Differential	Fast channel (max speed)	-	3.5	5.5		
			Slow channel (max speed)	-	3.5	5.5		
	Offset error	Single ended	Fast channel (max speed)	-	1	4.5		
			Slow channel (max speed)	-	1	5		
		Differential	Fast channel (max speed)	-	1.5	3		
			Slow channel (max speed)	-	1.5	3		
	Gain error	Single ended	Fast channel (max speed)	-	2.5	6		
			Slow channel (max speed)	-	2.5	6		
		Differential	Fast channel (max speed)	-	2.5	3.5		
			Slow channel (max speed)	-	2.5	3.5		
	Differential linearity error	Single ended	Fast channel (max speed)	-	1	1.5		
			Slow channel (max speed)	-	1	1.5		
		Differential	Fast channel (max speed)	-	1	1.2		
			Slow channel (max speed)	-	1	1.2		
	Integral linearity error	Single ended	Fast channel (max speed)	-	1.5	3.5		
			Slow channel (max speed)	-	1.5	3.5		
		Differential	Fast channel (max speed)	-	1	3		
			Slow channel (max speed)	-	1	2.5		
	ENOB	Single ended	Fast channel (max speed)	10	10.5	-		bits
			Slow channel (max speed)	10	10.5	-		
		Differential	Fast channel (max speed)	10.7	10.9	-		
			Slow channel (max speed)	10.7	10.9	-		
	SINAD	Single ended	Fast channel (max speed)	62	65	-		dB
			Slow channel (max speed)	62	65	-		
		Differential	Fast channel (max speed)	66	67.4	-		
			Slow channel (max speed)	66	67.4	-		
	SNR	Single ended	Fast channel (max speed)	64	66	-		
			Slow channel (max speed)	64	66	-		
		Differential	Fast channel (max speed)	66.5	68	-		
			Slow channel (max speed)	66.5	68	-		



Table 80. ADC accuracy - Limited test conditions 2⁽¹⁾⁽²⁾⁽³⁾ (continued)

Symbol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, $V_{DDA} \geq 2\text{ V}$ $TA = 25^\circ\text{C}$	Single ended	Fast channel (max speed)	-	-74	-65	dB
				Slow channel (max speed)	-	-74	-67	
		ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, $V_{DDA} \geq 2\text{ V}$ $TA = 25^\circ\text{C}$	Differential	Fast channel (max speed)	-	-79	-70	
				Slow channel (max speed)	-	-79	-71	

- Guaranteed by design.
- ADC DC accuracy values are measured after internal calibration.
- ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
- The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4\text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4\text{ V}$). It is disable when $V_{DDA} \geq 2.4\text{ V}$. No oversampling.

Table 80. ADC accuracy - Limited test conditions 2⁽¹⁾⁽²⁾⁽³⁾ (continued)

Symbol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, $V_{DDA} \geq 2\text{ V}$ $TA = 25^\circ\text{C}$	Single ended	Fast channel (max speed)	-	-74	-65	dB
				Slow channel (max speed)	-	-74	-67	
		ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, $V_{DDA} \geq 2\text{ V}$ $TA = 25^\circ\text{C}$	Differential	Fast channel (max speed)	-	-79	-70	
				Slow channel (max speed)	-	-79	-71	

- Guaranteed by design.
- ADC DC accuracy values are measured after internal calibration.
- ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
- The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4\text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4\text{ V}$). It is disable when $V_{DDA} \geq 2.4\text{ V}$. No oversampling.

Electrical characteristics

STM32WB55xx STM32WB35xx

Table 81. ADC accuracy - Limited test conditions 3⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions ⁽⁴⁾		Min	Typ	Max	Unit		
ET	Total unadjusted error	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, 1.65 V ≤ V _{DDA} = V _{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	5.5	7.5		
			Slow channel (max speed)	-	4.5	6.5	LSB		
			Differential	Fast channel (max speed)	-	4.5	7.5		
			Slow channel (max speed)	-	4.5	5.5			
			Single ended	Fast channel (max speed)	-	2	5		
	Offset error		Slow channel (max speed)	-	2.5	5			
			Differential	Fast channel (max speed)	-	2	3.5		
			Slow channel (max speed)	-	2.5	3			
			Single ended	Fast channel (max speed)	-	4.5	7		
			Slow channel (max speed)	-	3.5	6			
EG	Gain error		Differential	Fast channel (max speed)	-	3.5	4	LSB	
			Slow channel (max speed)	-	3.5	5			
			Single ended	Fast channel (max speed)	-	1.2	1.5		
			Slow channel (max speed)	-	1.2	1.5			
			Differential	Fast channel (max speed)	-	1	1.2		
	ED		Slow channel (max speed)	-	1	1.2			
			Single ended	Fast channel (max speed)	-	3	3.5		
			Slow channel (max speed)	-	2.5	3.5			
			Differential	Fast channel (max speed)	-	2	2.5		
			Slow channel (max speed)	-	2	2.5			
EL	Integral linearity error		Single ended	Fast channel (max speed)	10	10.4	-	bits	
			Slow channel (max speed)	10	10.4	-			
			Differential	Fast channel (max speed)	10.6	10.7	-		
			Slow channel (max speed)	10.6	10.7	-			
			Single ended	Fast channel (max speed)	62	64	-		
	ENOB		Slow channel (max speed)	62	64	-			
			Differential	Fast channel (max speed)	65	66	-		
			Slow channel (max speed)	65	66	-			
			Single ended	Fast channel (max speed)	63	65	-		
			Slow channel (max speed)	63	65	-			
SINAD	Signal-to-noise and distortion ratio		Differential	Fast channel (max speed)	66	67	-	dB	
			Slow channel (max speed)	66	67	-			
			Single ended	Fast channel (max speed)	65	66	-		
			Slow channel (max speed)	65	66	-			
			Differential	Fast channel (max speed)	66	67	-		
	SNR		Slow channel (max speed)	66	67	-			
			Single ended	Fast channel (max speed)	63	65	-		
			Slow channel (max speed)	63	65	-			
			Differential	Fast channel (max speed)	66	67	-		
			Slow channel (max speed)	66	67	-			

Electrical characteristics

STM32WB55xx STM32WB35xx

表 81. ADC 精度 - 有限测试条件 3⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions ⁽⁴⁾		Min	Typ	Max	Unit	
ET	Total unadjusted error		Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
			Slow channel (max speed)	-	4.5	6.5		
			Differential	Fast channel (max speed)	-	4.5	7.5	
			Slow channel (max speed)	-	4.5	5.5		
			Single ended	Fast channel (max speed)	-	2	5	
	EO		Slow channel (max speed)	-	2.5	5		
			Differential	Fast channel (max speed)	-	2	3.5	
			Slow channel (max speed)	-	2.5	3		
			Single ended	Fast channel (max speed)	-	4.5	7	
			Slow channel (max speed)	-	3.5	6		
EG	Gain error		Differential	Fast channel (max speed)	-	3.5	4	
			Slow channel (max speed)	-	3.5	5		
			Single ended	Fast channel (max speed)	-	1.2	1.5	
			Slow channel (max speed)	-	1.2	1.5		
			Differential	Fast channel (max speed)	-	1	1.2	
	ED		Slow channel (max speed)	-	1	1.2		
			Single ended	Fast channel (max speed)	-	3	3.5	
			Slow channel (max speed)	-	2.5	3.5		
			Differential	Fast channel (max speed)	-	2	2.5	
			Slow channel (max speed)	-	2	2.5		
EL	Integral linearity error		Single ended	Fast channel (max speed)	10	10.4	-	bits
			Slow channel (max speed)	10	10.4	-		
			Differential	Fast channel (max speed)	10.6	10.7	-	
			Slow channel (max speed)	10.6	10.7	-		
			Single ended	Fast channel (max speed)	62	64	-	
	ENOB		Slow channel (max speed)	62	64	-		
			Differential	Fast channel (max speed)	65	66	-	
			Slow channel (max speed)	65	66	-		
			Single ended	Fast channel (max speed)	66	67	-	
			Slow channel (max speed)	66	67	-		
SINAD	Signal-to-noise and distortion ratio		Differential	Fast channel (max speed)	62	64	-	dB
			Slow channel (max speed)	62	64	-		
			Single ended	Fast channel (max speed)	65	66	-	
			Slow channel (max speed)	65	66	-		
			Differential	Fast channel (max speed)	66	67	-	
	SNR		Slow channel (max speed)	66	67	-		
			Single ended	Fast channel (max speed)	63	65	-	
			Slow channel (max speed)	63	65	-		
			Differential	Fast channel (max speed)	66	67	-	
			Slow channel (max speed)	66	67	-		

Table 81. ADC accuracy - Limited test conditions 3⁽¹⁾⁽²⁾⁽³⁾ (continued)

Symbol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, 1.65 V ≤ V _{DDA} = V _{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
	Differential		Fast channel (max speed)	-	-72	-71	dB	
			Slow channel (max speed)	-	-72	-71		

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

表 81. ADC 精度 - 有限测试条件 3⁽¹⁾⁽²⁾⁽³⁾ (继续)

Symbol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, 1.65 V ≤ V _{DDA} = V _{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
	Differential		Fast channel (max speed)	-	-72	-71	dB	
			Slow channel (max speed)	-	-72	-71		

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 82. ADC accuracy - Limited test conditions 4⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	Fast channel (max speed)	-	5	5.4		LSB
			Slow channel (max speed)	-	4	5		
		Differential	Fast channel (max speed)	-	4	5		
			Slow channel (max speed)	-	3.5	4.5		
	Offset error	Single ended	Fast channel (max speed)	-	2	4		
			Slow channel (max speed)	-	2	4		
		Differential	Fast channel (max speed)	-	2	3.5		
			Slow channel (max speed)	-	2	3.5		
	Gain error	Single ended	Fast channel (max speed)	-	4	4.5		
			Slow channel (max speed)	-	4	4.5		
ED	Differential linearity error	Differential	Fast channel (max speed)	-	3	4		
			Slow channel (max speed)	-	3	4		
		Single ended	Fast channel (max speed)	-	1	1.5		
			Slow channel (max speed)	-	1	1.5		
	Integral linearity error	Differential	Fast channel (max speed)	-	1	1.2		
			Slow channel (max speed)	-	1	1.2		
		Single ended	Fast channel (max speed)	-	2.5	3		
			Slow channel (max speed)	-	2.5	3		
		Differential	Fast channel (max speed)	-	2	2.5		
			Slow channel (max speed)	-	2	2.5		
ENOB	Effective number of bits	Single ended	Fast channel (max speed)	10.2	10.5	-	bits	LSB
			Slow channel (max speed)	10.2	10.5	-		
		Differential	Fast channel (max speed)	10.6	10.7	-		
			Slow channel (max speed)	10.6	10.7	-		
	SINAD	Single ended	Fast channel (max speed)	63	65	-	dB	dB
			Slow channel (max speed)	63	65	-		
		Differential	Fast channel (max speed)	65	66	-		
			Slow channel (max speed)	65	66	-		
SNR	Signal-to-noise ratio	Single ended	Fast channel (max speed)	64	65	-	bits	bits
			Slow channel (max speed)	64	65	-		
		Differential	Fast channel (max speed)	66	67	-		
	Signal-to-noise and distortion ratio	Single ended	Fast channel (max speed)	66	67	-		
			Slow channel (max speed)	66	67	-		

表82. ADC 精度 - 有限测试条件 4⁽¹⁾⁽²⁾⁽³⁾

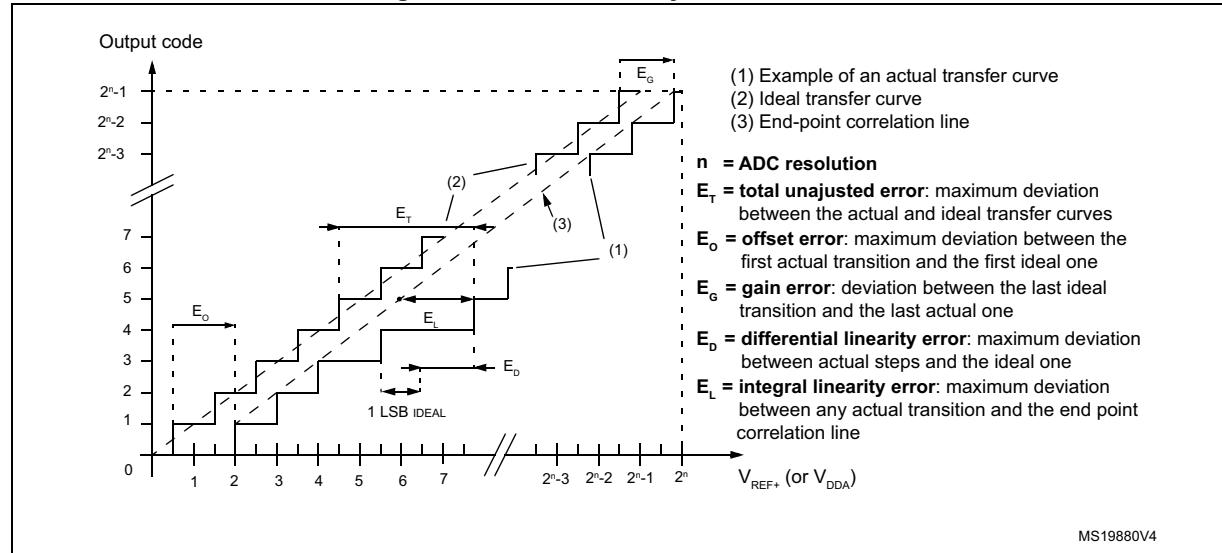
Symbol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit	
ET	Total unadjusted error	Single ended	Fast channel (max speed)	-	5	5.4		LSB	
			Slow channel (max speed)	-	4	5			
		Differential	Fast channel (max speed)	-	4	5			
			Slow channel (max speed)	-	3.5	4.5			
	Offset error	Single ended	Fast channel (max speed)	-	2	4			
			Slow channel (max speed)	-	2	4			
		Differential	Fast channel (max speed)	-	2	3.5			
			Slow channel (max speed)	-	2	3.5			
	Gain error	Single ended	Fast channel (max speed)	-	4	4.5			
			Slow channel (max speed)	-	4	4.5			
ED	Differential linearity error	Differential	Fast channel (max speed)	-	3	4			
			Slow channel (max speed)	-	3	4			
		Single ended	Fast channel (max speed)	-	1	1.5			
			Slow channel (max speed)	-	1	1.5			
		Differential	Fast channel (max speed)	-	1	1.2			
			Slow channel (max speed)	-	1	1.2			
	Integral linearity error	Single ended	Fast channel (max speed)	-	2.5	3			
			Slow channel (max speed)	-	2.5	3			
		Differential	Fast channel (max speed)	-	2	2.5			
			Slow channel (max speed)	-	2	2.5			
EL	Effective number of bits	Single ended	Fast channel (max speed)	10.2	10.5	-	bits	bits	
			Slow channel (max speed)	10.2	10.5	-			
		Differential	Fast channel (max speed)	10.6	10.7	-			
			Slow channel (max speed)	10.6	10.7	-			
	SINAD	Single ended	Fast channel (max speed)	63	65	-	dB	dB	
			Slow channel (max speed)	63	65	-			
		Differential	Fast channel (max speed)	65	66	-			
			Slow channel (max speed)	65	66	-			
SNR	Signal-to-noise ratio	Single ended	Fast channel (max speed)	64	65	-	bits	bits	
			Slow channel (max speed)	64	65	-			
		Differential	Fast channel (max speed)	66	67	-			
	Signal-to-noise and distortion ratio	Single ended	Fast channel (max speed)	66	67	-	dB		
			Slow channel (max speed)	66	67	-			

Table 82. ADC accuracy - Limited test conditions 4⁽¹⁾⁽²⁾⁽³⁾ (continued)

Symbol	Parameter	Conditions ⁽⁴⁾		Min	Typ	Max	Unit
		Single ended	Differential				
THD	Total harmonic distortion	ADC clock frequency ≤ 16 MHz, $1.65 \text{ V} \leq V_{\text{DDA}} = V_{\text{REF+}} \leq 3.6 \text{ V}$, Voltage scaling Range 2	Fast channel (max speed)	-	-71	-69	dB
			Slow channel (max speed)	-	-71	-69	
		Differential	Fast channel (max speed)	-	-73	-72	
			Slow channel (max speed)	-	-73	-72	

- Guaranteed by design.
- ADC DC accuracy values are measured after internal calibration.
- ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins that may potentially inject negative current.
- The I/O analog switch voltage booster is enabled when $V_{\text{DDA}} < 2.4 \text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{\text{DDA}} < 2.4 \text{ V}$). It is disabled when $V_{\text{DDA}} \geq 2.4 \text{ V}$. No oversampling.

Figure 29. ADC accuracy characteristics

Table 82. ADC accuracy - Limited test conditions 4⁽¹⁾⁽²⁾⁽³⁾ (continued)

Symbol	Parameter	Conditions ⁽⁴⁾		Min	Typ	Max	Unit
		Single ended	Differential				
THD	Total harmonic distortion	ADC clock frequency ≤ 16 MHz, $1.65 \text{ V} \leq V_{\text{DDA}} = V_{\text{REF+}} \leq 3.6 \text{ V}$, Voltage scaling Range 2	Fast channel (max speed)	-	-71	-69	dB
			Slow channel (max speed)	-	-71	-69	
		Differential	Fast channel (max speed)	-	-73	-72	
			Slow channel (max speed)	-	-73	-72	

- Guaranteed by design.
- ADC DC accuracy values are measured after internal calibration.
- ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins that may potentially inject negative current.
- The I/O analog switch voltage booster is enabled when $V_{\text{DDA}} < 2.4 \text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{\text{DDA}} < 2.4 \text{ V}$). It is disabled when $V_{\text{DDA}} \geq 2.4 \text{ V}$. No oversampling.

Figure 29. ADC accuracy characteristics

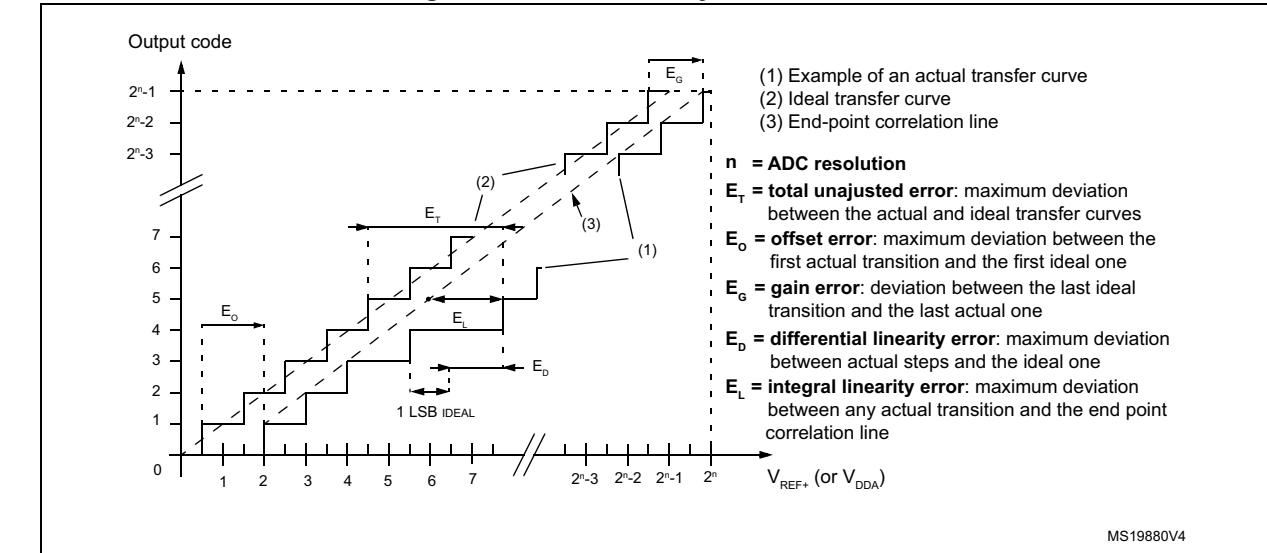
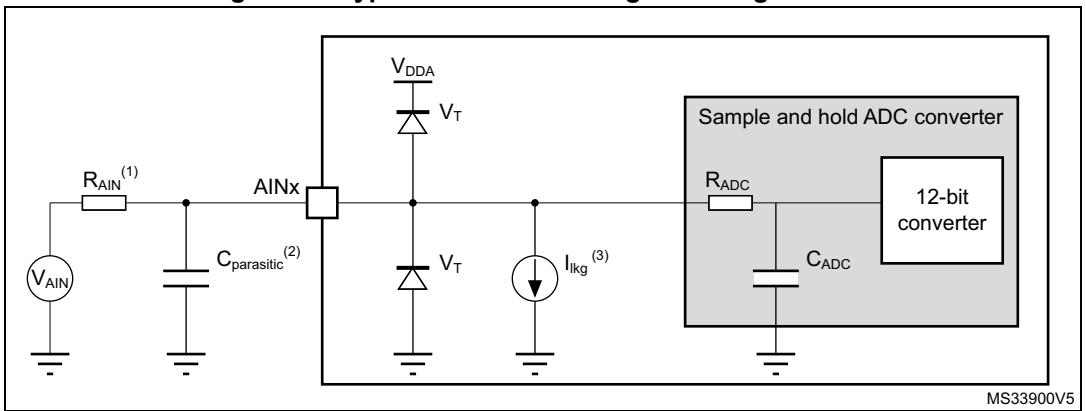


Figure 30. Typical connection diagram using the ADC



- Refer to [Table 77: ADC characteristics](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
- $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to [Table 72: I/O static characteristics](#) for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
- Refer to [Table 72: I/O static characteristics](#) for the values of I_{lkg} .

General PCB design guidelines

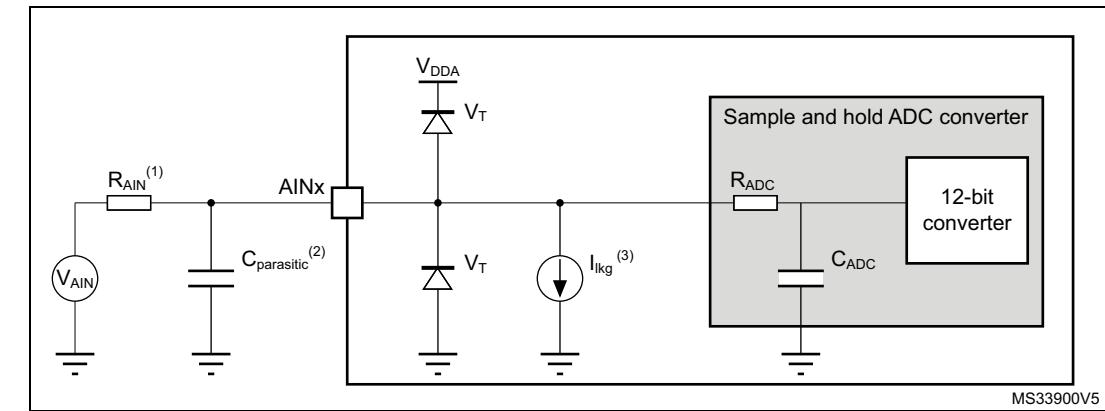
Power supply decoupling has to be performed as shown in [Figure 16: Power supply scheme \(all packages except UFBGA129 and WLCSP100\)](#). The 10 nF capacitor needs to be ceramic (good quality), placed as close as possible to the chip.

6.3.21 Voltage reference buffer characteristics

Table 83. VREFBUF characteristics⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DDA}	Analog supply voltage	Normal mode	$V_{RS} = 0$	2.4	-	3.6	V
			$V_{RS} = 1$	2.8	-	3.6	
	Degraded mode ⁽²⁾	$V_{RS} = 0$	1.65	-	2.4		
		$V_{RS} = 1$	1.65	-	2.8		
V _{REFBUF_OUT}	Voltage reference output	Normal mode	$V_{RS} = 0$	2.046	2.048	2.049	V
			$V_{RS} = 1$	2.498	2.5	2.502	
	Degraded mode ⁽²⁾	$V_{RS} = 0$	$V_{DDA}-150\text{ mV}$	-	V_{DDA}		
		$V_{RS} = 1$	$V_{DDA}-150\text{ mV}$	-	V_{DDA}		
TRIM	Trim step resolution	-	-	-	± 0.05	± 0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	μF
esr	Equivalent series resistor of C_{load}	-	-	-	-	2	Ω
I _{load}	Static load current	-	-	-	-	4	mA

图30. 使用 ADC 的典型连接图



- Refer to [表77: ADC 特性](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} . $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to [表72: I/O静态特性](#) for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
- Refer to [表72: I/O静态特性](#) for the values of I_{lkg} .

General PCB design guidelines

Power supply decoupling has to be performed as shown in [Figure 16: Power supply scheme \(all packages except UFBGA129 and WLCSP100\)](#). The 10 nF capacitor needs to be ceramic (good quality), placed as close as possible to the chip.

6.3.21 Voltage reference buffer characteristics

Table 83. VREFBUF characteristics⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DDA}	Analog supply voltage	Normal mode	$V_{RS} = 0$	2.4	-	3.6	V
			$V_{RS} = 1$	2.8	-	3.6	
	Degraded mode ⁽²⁾	$V_{RS} = 0$	1.65	-	2.4		
		$V_{RS} = 1$	1.65	-	2.8		
V _{REFBUF_OUT}	Voltage reference output	Normal mode	$V_{RS} = 0$	2.046	2.048	2.049	V
			$V_{RS} = 1$	2.498	2.5	2.502	
	Degraded mode ⁽²⁾	$V_{RS} = 0$	$V_{DDA}-150\text{ mV}$	-	V_{DDA}		
		$V_{RS} = 1$	$V_{DDA}-150\text{ mV}$	-	V_{DDA}		
TRIM	Trim step resolution	-	-	-	-	± 0.05	± 0.1
CL	Load capacitor	-	-	0.5	1	1.5	μF
esr	Equivalent series resistor of C_{load}	-	-	-	-	2	Ω
I _{load}	Static load current	-	-	-	-	4	mA

Table 83. VREFBUF characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	$I_{load} = 500 \mu A$	-	200	1000	ppm/V
				-	100	500	
I_{load_reg}	Load regulation	500 μA ≤ I_{load} ≤ 4 mA	Normal mode	-	50	500	ppm/mA
T_{Coef}	Temperature coefficient	-40 °C < T_J < +125 °C		-	-	$T_{coeff_vrefint} + 50$	ppm/ °C
		0 °C < T_J < +50 °C		-	-	$T_{coeff_vrefint} + 50$	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	CL = 0.5 $\mu F^{(3)}$		-	300	350	μs
		CL = 1.1 $\mu F^{(3)}$		-	500	650	
		CL = 1.5 $\mu F^{(3)}$		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase ⁽⁴⁾	-	-	-	8	-	mA
I_{DDA} (VREFBUF)	VREFBUF consumption from V_{DDA}	$I_{load} = 0 \mu A$		-	16	25	μA
		$I_{load} = 500 \mu A$		-	18	30	
		$I_{load} = 4 mA$		-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode the voltage reference buffer cannot maintain accurately the output voltage that will follow (V_{DDA} - drop voltage).
3. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
4. To correctly control the VREFBUF in-rush current during start-up phase and scaling change, the V_{DDA} voltage must be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for $V_{RS} = 0$ and $V_{RS} = 1$.

Table 83. VREFBUF characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	$I_{load} = 500 \mu A$	-	200	1000	ppm/V
				-	100	500	
I_{load_reg}	Load regulation	500 μA ≤ I_{load} ≤ 4 mA	Normal mode	-	50	500	ppm/mA
T_{Coef}	Temperature coefficient	-40 °C < T_J < +125 °C		-	-	$T_{coeff_vrefint} + 50$	ppm/ °C
		0 °C < T_J < +50 °C		-	-	$T_{coeff_vrefint} + 50$	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	CL = 0.5 $\mu F^{(3)}$		-	300	350	μs
		CL = 1.1 $\mu F^{(3)}$		-	500	650	
		CL = 1.5 $\mu F^{(3)}$		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase ⁽⁴⁾	-	-	-	8	-	mA
I_{DDA} (VREFBUF)	VREFBUF consumption from V_{DDA}	$I_{load} = 0 \mu A$		-	16	25	μA
		$I_{load} = 500 \mu A$		-	18	30	
		$I_{load} = 4 mA$		-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode the voltage reference buffer cannot maintain accurately the output voltage that will follow (V_{DDA} - drop voltage).
3. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
4. To correctly control the VREFBUF in-rush current during start-up phase and scaling change, the V_{DDA} voltage must be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for $V_{RS} = 0$ and $V_{RS} = 1$.

6.3.22 Comparator characteristics

Table 84. COMP characteristics⁽¹⁾

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-			1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-			0	-	V_{DDA}	
$V_{BG}^{(2)}$	Scaler input voltage	-			V_{REFINT}			
V_{SC}	Scaler offset voltage	-			-	± 5	± 10	mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)			-	200	300	nA
		BRG_EN=1 (bridge enable)			-	0.8	1	μA
t_{START_SCALER}	Scaler startup time	-			-	100	200	μs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	μs	
			$V_{DDA} < 2.7$ V	-	-	7		
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15		
			$V_{DDA} < 2.7$ V	-	-	25		
		Ultra-low-power mode	-	-	40			
$t_D^{(3)}$	Propagation delay with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns	
			$V_{DDA} < 2.7$ V	-	55	100		
		Medium mode			-	0.55	0.9	
		Ultra-low-power mode			-	4	7	
V_{offset}	Comparator offset error	Full common mode range			-	± 5	± 20	mV
V_{hys}	Comparator hysteresis	No hysteresis			-	0	-	mV
		Low hysteresis			-	8	-	
		Medium hysteresis			-	15	-	
		High hysteresis			-	27	-	
$I_{DDA(COMP)}$	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA	
			With 50 kHz ± 100 mV overdrive square signal	-	1200	-		
		Medium mode	Static	-	5	7		
			With 50 kHz ± 100 mV overdrive square signal	-	6	-		
		High-speed mode	Static	-	70	100		
			With 50 kHz ± 100 mV overdrive square signal	-	75	-		

1. Guaranteed by design, unless otherwise specified.

2. Refer to Table 36: Embedded internal voltage reference.

3. Guaranteed by characterization results.

6.3.22 比较器特性

表 84. COMP 特性⁽¹⁾

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-			1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-			0	-	V_{DDA}	
$V_{BG}^{(2)}$	Scaler input voltage	-			V_{REFINT}			
V_{SC}	Scaler offset voltage	-			-			mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)			-	200	300	nA
		BRG_EN=1 (bridge enable)			-	0.8	1	μA
t_{START_SCALER}	Scaler startup time	-			-	100	200	μs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	μs	
			$V_{DDA} < 2.7$ V	-	-	7		
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15		
			$V_{DDA} < 2.7$ V	-	-	25		
		Ultra-low-power mode	-	-	40			
$t_D^{(3)}$	Propagation delay with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns	
			$V_{DDA} < 2.7$ V	-	55	100		
		Medium mode			-	0.55	0.9	
		Ultra-low-power mode			-	4	7	
V_{offset}	Comparator offset error	Full common mode range			-	± 5	± 20	mV
V_{hys}	Comparator hysteresis	No hysteresis			-	0	-	mV
		Low hysteresis			-	8	-	
		Medium hysteresis			-	15	-	
		High hysteresis			-	27	-	
$I_{DDA(COMP)}$	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA	
			With 50 kHz ± 100 mV overdrive square signal	-	1200	-		
		Medium mode	Static	-	5	7		
			With 50 kHz ± 100 mV overdrive square signal	-	6	-		
		High-speed mode	Static	-	70	100		
			With 50 kHz ± 100 mV overdrive square signal	-	75	-		

1. Guaranteed by design, unless otherwise specified.

2. Refer to Table 36: Embedded internal voltage reference.

3. Guaranteed by characterization results.

6.3.23 Temperature sensor characteristics

Table 85. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{TS} linearity with temperature	-	± 1	± 2	°C
Avg_Slope ⁽²⁾	Average slope	2.3	2.5	2.7	mV / °C
V_{30}	Voltage at 30 °C (± 5 °C) ⁽³⁾	0.742	0.76	0.785	V
$t_{START}^{(TS_BUF)}{(1)}$	Sensor buffer start-up time in continuous mode ⁽⁴⁾	-	8	15	μs
$t_{START}^{(1)}$	Start-up time when entering in continuous mode ⁽⁴⁾	-	70	120	μs
$t_{S_temp}^{(1)}$	ADC sampling time when reading the temperature	5	-	-	μs
$I_{DD(TS)}^{(1)}$	Temperature sensor consumption from V_{DD} , when selected by ADC	-	4.7	7	μA

1. Guaranteed by design.

2. Guaranteed by characterization results.

3. Measured at $V_{DDA} = 3.0$ V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to [Table 11: Temperature sensor calibration values](#).

4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.24 V_{BAT} monitoring characteristics

Table 86. V_{BAT} monitoring characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	3 x 39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er ⁽²⁾	Error on Q	-10	-	10	%
$t_{S_vbat}^{(2)}$	ADC sampling time when reading V_{BAT}	12	-	-	μs

1. $1.55 < V_{BAT} < 3.6$ V.

2. Guaranteed by design.

Table 87. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

6.3.23 温度传感器特性

Table 85. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{TS} linearity with temperature	-	± 1	± 2	°C
Avg_Slope ⁽²⁾	Average slope	2.3	2.5	2.7	mV / °C
V_{30}	Voltage at 30 °C (± 5 °C) ⁽³⁾	0.742	0.76	0.785	V
$t_{START}^{(TS_BUF)}{(1)}$	Sensor buffer start-up time in continuous mode ⁽⁴⁾	-	8	15	μs
$t_{START}^{(1)}$	Start-up time when entering in continuous mode ⁽⁴⁾	-	70	120	μs
$t_{S_temp}^{(1)}$	ADC sampling time when reading the temperature	5	-	-	μs
$I_{DD(TS)}^{(1)}$	Temperature sensor consumption from V_{DD} , when selected by ADC	-	4.7	7	μA

1. Guaranteed by design.

2. Guaranteed by characterization results.

3. Measured at $V_{DDA} = 3.0$ V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to [Table 11: Temperature sensor calibration values](#).

4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.24 V_{BAT} 监控特性

Table 86. V_{BAT} monitoring characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	3 x 39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er ⁽²⁾	Error on Q	-10	-	10	%
$t_{S_vbat}^{(2)}$	ADC sampling time when reading V_{BAT}	12	-	-	μs

1. $1.55 < V_{BAT} < 3.6$ V.

2. Guaranteed by design.

Table 87. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

6.3.25 SMPS step-down converter characteristics

The SMPS step-down converter characteristic are given at 4 MHz clock, with a 20 mA load (unless otherwise specified), using a 10 μ H inductor and a 4.7 μ F capacitor.

6.3.26 LCD controller characteristics

The STM32WB55xx devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the VLCD pin to decouple this converter.

Table 88. LCD controller characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	V	-	-	3.6	
V_{LCD0}	LCD internal reference voltage 0		-	2.62	-	
V_{LCD1}	LCD internal reference voltage 1		-	2.76	-	
V_{LCD2}	LCD internal reference voltage 2		-	2.89	-	
V_{LCD3}	LCD internal reference voltage 3		-	3.04	-	
V_{LCD4}	LCD internal reference voltage 4		-	3.19	-	
V_{LCD5}	LCD internal reference voltage 5		-	3.32	-	
V_{LCD6}	LCD internal reference voltage 6		-	3.46	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.62	-	-	
C_{ext}	V_{LCD} external capacitance	Buffer OFF (BUFEN=0 is LCD_CR register)	0.2	-	2	μ F
		Buffer ON (BUFEN=1 is LCD_CR register)	1	-	2	
$I_{LCD}^{(2)}$	Supply current from V_{DD} at $V_{DD} = 2.2$ V	Buffer OFF (BUFEN=0 is LCD_CR register)	-	3	-	μ A
	Supply current from V_{DD} at $V_{DD} = 3.0$ V	Buffer OFF (BUFEN=0 is LCD_CR register)	-	1.5	-	
I_{VLCD}	Supply current from V_{LCD} ($V_{LCD} = 3$ V)	Buffer OFF (BUFFEN = 0, PON = 0)	-	0.5	-	μ A
		Buffer ON (BUFFEN = 1, 1/2 Bias)	-	0.6	-	
		Buffer ON (BUFFEN = 1, 1/3 Bias)	-	0.8	-	
		Buffer ON (BUFFEN = 1, 1/4 Bias)	-	1	-	
R_{HN}	Total High resistor value for Low drive resistive network	-	5.5	-	$M\Omega$	
R_{LN}	Total Low resistor value for High drive resistive network	-	240	-	$k\Omega$	

6.3.25 SMPS 下降变压器特性

SMPS 下降转换器的特性在 4 MHz 时钟下给出，负载为 20 mA（除非另有说明），使用一个 10 μ H 电感器和一个 4.7 μ F 电容器。

6.3.26 LCD controller characteristics

The STM32WB55xx devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the VLCD pin to decouple this converter.

Table 88. LCD controller characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	V	-	-	3.6	
V_{LCD0}	LCD internal reference voltage 0		-	2.62	-	
V_{LCD1}	LCD internal reference voltage 1		-	2.76	-	
V_{LCD2}	LCD internal reference voltage 2		-	2.89	-	
V_{LCD3}	LCD internal reference voltage 3		-	3.04	-	
V_{LCD4}	LCD internal reference voltage 4		-	3.19	-	
V_{LCD5}	LCD internal reference voltage 5		-	3.32	-	
V_{LCD6}	LCD internal reference voltage 6		-	3.46	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.62	-	-	
C_{ext}	V_{LCD} external capacitance	Buffer OFF (BUFEN=0 is LCD_CR register)	0.2	-	2	μ F
		Buffer ON (BUFEN=1 is LCD_CR register)	1	-	2	
$I_{LCD}^{(2)}$	Supply current from V_{DD} at $V_{DD} = 2.2$ V	Buffer OFF (BUFEN=0 is LCD_CR register)	-	3	-	μ A
	Supply current from V_{DD} at $V_{DD} = 3.0$ V	Buffer OFF (BUFEN=0 is LCD_CR register)	-	1.5	-	
I_{VLCD}	Supply current from V_{LCD} ($V_{LCD} = 3$ V)	Buffer OFF (BUFFEN = 0, PON = 0)	-	0.5	-	μ A
		Buffer ON (BUFFEN = 1, 1/2 Bias)	-	0.6	-	
		Buffer ON (BUFFEN = 1, 1/3 Bias)	-	0.8	-	
		Buffer ON (BUFFEN = 1, 1/4 Bias)	-	1	-	
R_{HN}	Total High resistor value for Low drive resistive network	-	5.5	-	$M\Omega$	
R_{LN}	Total Low resistor value for High drive resistive network	-	240	-	$k\Omega$	

Table 88. LCD controller characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{44}	Segment/Common highest level voltage	V	-	V_{LCD}	-	
V_{34}	Segment/Common 3/4 level voltage		-	$3/4 V_{LCD}$	-	
V_{23}	Segment/Common 2/3 level voltage		-	$2/3 V_{LCD}$	-	
V_{12}	Segment/Common 1/2 level voltage		-	$1/2 V_{LCD}$	-	
V_{13}	Segment/Common 1/3 level voltage		-	$1/3 V_{LCD}$	-	
V_{14}	Segment/Common 1/4 level voltage		-	$1/4 V_{LCD}$	-	
V_0	Segment/Common lowest level voltage		-	0	-	

1. Guaranteed by design.

2. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio = 64, all pixels active, no LCD connected.

6.3.27 Timer characteristics

The parameters given in the following tables are guaranteed by design. Refer to [Section 6.3.17](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 89. TIMx⁽¹⁾ characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 64 \text{ MHz}$	15.625	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 64 \text{ MHz}$	0	40	
Res_{TIM}	Timer resolution	TIM1, TIM16, TIM17	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 64 \text{ MHz}$	0.015625	1024	μs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	65536×65536	$t_{TIMxCLK}$	
		$f_{TIMxCLK} = 64 \text{ MHz}$	-	67.10	s

1. TIMx is used as a general term where x stands for 1, 2, 16 or 17.

Table 88. LCD controller characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{44}	Segment/Common highest level voltage	V	-	V_{LCD}	-	
V_{34}	Segment/Common 3/4 level voltage		-	$3/4 V_{LCD}$	-	
V_{23}	Segment/Common 2/3 level voltage		-	$2/3 V_{LCD}$	-	
V_{12}	Segment/Common 1/2 level voltage		-	$1/2 V_{LCD}$	-	
V_{13}	Segment/Common 1/3 level voltage		-	$1/3 V_{LCD}$	-	
V_{14}	Segment/Common 1/4 level voltage		-	$1/4 V_{LCD}$	-	
V_0	Segment/Common lowest level voltage		-	0	-	

1. Guaranteed by design.

2. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio = 64, all pixels active, no LCD connected.

6.3.27 Timer characteristics

The parameters given in the following tables are guaranteed by design. Refer to [Section 6.3.17](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 89. TIMx⁽¹⁾ characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 64 \text{ MHz}$	15.625	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 64 \text{ MHz}$	0	40	
Res_{TIM}	Timer resolution	TIM1, TIM16, TIM17	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 64 \text{ MHz}$	0.015625	1024	μs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	65536×65536	$t_{TIMxCLK}$	
		$f_{TIMxCLK} = 64 \text{ MHz}$	-	67.10	s

1. TIMx is used as a general term where x stands for 1, 2, 16 or 17.

Electrical characteristics

STM32WB55xx STM32WB35xx

Table 90. IWDG min/max timeout period at 32 kHz (LSI1)⁽¹⁾

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0] = 0x000	Max timeout RL[11:0] = 0xFFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock vs. the LSI clock, hence there is always a full RC period of uncertainty.

6.3.28 Clock recovery system (CRS)

The devices embed a special block for the automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range.

This automatic trimming is based on the external synchronization signal, which can be derived from USB Sart Of Frame (SOF) signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software.

For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

6.3.29 Communication interfaces characteristics

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): bit rate up to 100 kbit/s
- Fast-mode (Fm): bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): bit rate up to 1 Mbit/s.

Table 91. Minimum I²CCLK frequency in all I²C modes

Symbol	Parameter	Condition		Min	Unit
f_{I2CCLK}	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog filter ON, DNF = 0	9	
			Analog filter OFF, DNF = 1	9	
		Fast-mode Plus	Analog filter ON, DNF = 0	19	
			Analog filter OFF, DNF = 1	16	

The I²C timings requirements are guaranteed by design when the I²C peripheral is properly configured (see the reference manual).

Electrical characteristics

STM32WB55xx STM32WB35xx

Table 90. IWDG min/max timeout period at 32 kHz (LSI1)⁽¹⁾

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0] = 0x000	Max timeout RL[11:0] = 0xFFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock vs. the LSI clock, hence there is always a full RC period of uncertainty.

6.3.28 Clock recovery system (CRS)

这些设备内置了一个专门的块，用于对内部 48 MHz 振荡器进行自动校准，以确保在整个设备操作范围内保持最佳精度。

This automatic trimming is based on the external synchronization signal, which can be derived from USB Sart Of Frame (SOF) signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software.

For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

6.3.29 Communication interfaces characteristics

I²C 接口特性

I²C 接口满足 I²C-bus 规范和用户手册第 03 版本的时序要求，用于：

- Standard-mode (Sm): bit rate up to 100 kbit/s
- Fast-mode (Fm): bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): bit rate up to 1 Mbit/s.

Table 91. Minimum I²CCLK frequency in all I²C modes

Symbol	Parameter	Condition		Min	Unit
f_{I2CCLK}	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog filter ON, DNF = 0	9	
			Analog filter OFF, DNF = 1	9	
		Fast-mode Plus	Analog filter ON, DNF = 0	19	
			Analog filter OFF, DNF = 1	16	

The I²C timings requirements are guaranteed by design when the I²C peripheral is properly configured (see the reference manual).



The SDA and SCL I/O requirements are met with the following restriction: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present. The 20 mA output drive requirement in Fast-mode Plus is supported partially.

This limits the maximum load C_{load} supported in Fast-mode Plus, given by these formulas:

- $t_r(SDA/SCL) = 0.8473 \times R_p \times C_{load}$
- $R_p(\min) = [V_{DD} - V_{OL}(\max)] / I_{OL}(\max)$

where R_p is the I2C lines pull-up. Refer to [Section 6.3.17](#) for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter, refer to [Table 92](#) for its characteristics.

Table 92. I2C analog filter characteristics⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50 ⁽²⁾	110 ⁽³⁾	ns

1. Guaranteed by design.

2. Spikes with widths below $t_{AF(\min)}$ are filtered.

3. Spikes with widths above $t_{AF(\max)}$ are not filtered

SPI characteristics

Unless otherwise specified, the parameters given in [Table 93](#) for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in [Table 24: General operating conditions](#).

- Output speed is set to OSPEEDR[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to [Section 6.3.17](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

SDA 和 SCL 的输入/输出要求满足以下限制：SDA 和 SCL 的输入/输出引脚不是开漏的。当配置为开漏时，I/O 引脚和 V_{DD} 之间的 PMOS 被禁用，但仍然存在。快速模式加的 20 mA 输出驱动要求得到了部分支持。

这限制了快速模式加下支持的最大负载电容，由以下公式给出：

- $t_r(SDA/SCL) = 0.8473 \times R_p \times C_{load}$
- $R_p(\min) = [V_{DD} - V_{OL}(\max)] / I_{OL}(\max)$

where R_p is the I2C lines pull-up. Refer to [Section 6.3.17](#) for the I2C I/Os characteristics.

所有 I2C SDA 和 SCL 输入/输出都内置了模拟滤波器，参见 [表 92](#) 其特性。

Table 92. I2C analog filter characteristics⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50 ⁽²⁾	110 ⁽³⁾	ns

1. Guaranteed by design.

2. Spikes with widths below $t_{AF(\min)}$ are filtered.

3. Spikes with widths above $t_{AF(\max)}$ are not filtered

SPI characteristics

Unless otherwise specified, the parameters given in [Table 93](#) for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in [Table 24: General operating conditions](#).

- Output speed is set to OSPEEDR[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to [Section 6.3.17](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 93. SPI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} 1/t _{c(SCK)}	SPI clock frequency	Master mode $1.65 < V_{DD} < 3.6 \text{ V}$ Voltage Range 1	-	-	32	MHz
		Master transmitter mode $1.65 < V_{DD} < 3.6 \text{ V}$ Voltage Range 1			32	
		Slave receiver mode $1.65 < V_{DD} < 3.6 \text{ V}$ Voltage Range 1			32	
		Slave mode transmitter/full duplex $2.7 < V_{DD} < 3.6 \text{ V}$ Voltage Range 1			32 ⁽²⁾	
		Slave mode transmitter/full duplex $1.65 < V_{DD} < 3.6 \text{ V}$ Voltage Range 1			20.5 ⁽²⁾	
		Voltage Range 2			8	
t _{su(NSS)}	NSS setup time	Slave mode, SPI prescaler = 2	4xT _{PCLK}	-	-	-
t _{h(NSS)}	NSS hold time	Slave mode, SPI prescaler = 2	2xT _{PCLK}	-	-	
t _{w(SCKH)} t _{w(SCKL)}	SCK high and low time	Master mode	T _{PCLK} - 1.5	T _{PCLK}	T _{PCLK} + 1	
t _{su(MI)}	Data input setup time	Master mode	1.5	-	-	
t _{su(SI)}		Slave mode	1	-	-	
t _{h(MI)}	Data input hold time	Master mode	5	-	-	
t _{h(SI)}		Slave mode	1	-	-	
t _{a(SO)}	Data output access time	Slave mode	9	-	34	ns
t _{dis(SO)}	Data output disable time		9	-	16	
t _{v(SO)}	Data output valid time	Slave mode $2.7 < V_{DD} < 3.6 \text{ V}$ Voltage Range 1	-	14.5	15.5	
		Slave mode $1.65 < V_{DD} < 3.6 \text{ V}$ Voltage Range 1	-	15.5	24	
		Slave mode $1.65 < V_{DD} < 3.6 \text{ V}$ Voltage Range 2	-	19.5	26	
t _{v(MO)}		Master mode (after enable edge)	-	2.5	3	
t _{h(SO)} t _{h(MO)}	Data output hold time	Slave mode (after enable edge)	8	-	-	ns
		Master mode (after enable edge)	1	-	-	

1. Guaranteed by characterization results.

2. Maximum frequency in Slave transmitter mode is determined by the sum of t_{v(SO)} and t_{su(MI)}, which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having t_{su(MI)} = 0 while Duty(SCK) = 50 %.Table 93. SPI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} 1/t _{c(SCK)}	SPI clock frequency	Master mode $1.65 < V_{DD} < 3.6 \text{ V}$ Voltage Range 1	-	-	32	MHz
		Master transmitter mode $1.65 < V_{DD} < 3.6 \text{ V}$ Voltage Range 1			32	
		Slave receiver mode $1.65 < V_{DD} < 3.6 \text{ V}$ Voltage Range 1			32	
		Slave mode transmitter/full duplex $2.7 < V_{DD} < 3.6 \text{ V}$ Voltage Range 1			32 ⁽²⁾	
		Slave mode transmitter/full duplex $1.65 < V_{DD} < 3.6 \text{ V}$ Voltage Range 1			20.5 ⁽²⁾	
		Voltage Range 2			8	
t _{su(NSS)}	NSS setup time	Slave mode, SPI prescaler = 2	4xT _{PCLK}	-	-	-
t _{h(NSS)}	NSS hold time	Slave mode, SPI prescaler = 2	2xT _{PCLK}	-	-	
t _{w(SCKH)} t _{w(SCKL)}	SCK high and low time	Master mode	T _{PCLK} - 1.5	T _{PCLK}	T _{PCLK} + 1	
t _{su(MI)}	Data input setup time	Master mode	1.5	-	-	
t _{su(SI)}		Slave mode	1	-	-	
t _{h(MI)}	Data input hold time	Master mode	5	-	-	
t _{h(SI)}		Slave mode	1	-	-	
t _{a(SO)}	Data output access time	Slave mode	9	-	34	ns
t _{dis(SO)}	Data output disable time		9	-	16	
t _{v(SO)}	Data output valid time	Slave mode $2.7 < V_{DD} < 3.6 \text{ V}$ Voltage Range 1	-	14.5	15.5	
		Slave mode $1.65 < V_{DD} < 3.6 \text{ V}$ Voltage Range 1	-	15.5	24	
		Slave mode $1.65 < V_{DD} < 3.6 \text{ V}$ Voltage Range 2	-	19.5	26	
t _{v(MO)}		Master mode (after enable edge)	-	2.5	3	
t _{h(SO)} t _{h(MO)}	Data output hold time	Slave mode (after enable edge)	8	-	-	
		Master mode (after enable edge)	1	-	-	

1. Guaranteed by characterization results.

2. Maximum frequency in Slave transmitter mode is determined by the sum of t_{v(SO)} and t_{su(MI)}, which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having t_{su(MI)} = 0 while Duty(SCK) = 50 %.

Figure 31. SPI timing diagram - slave mode and CPHA = 0

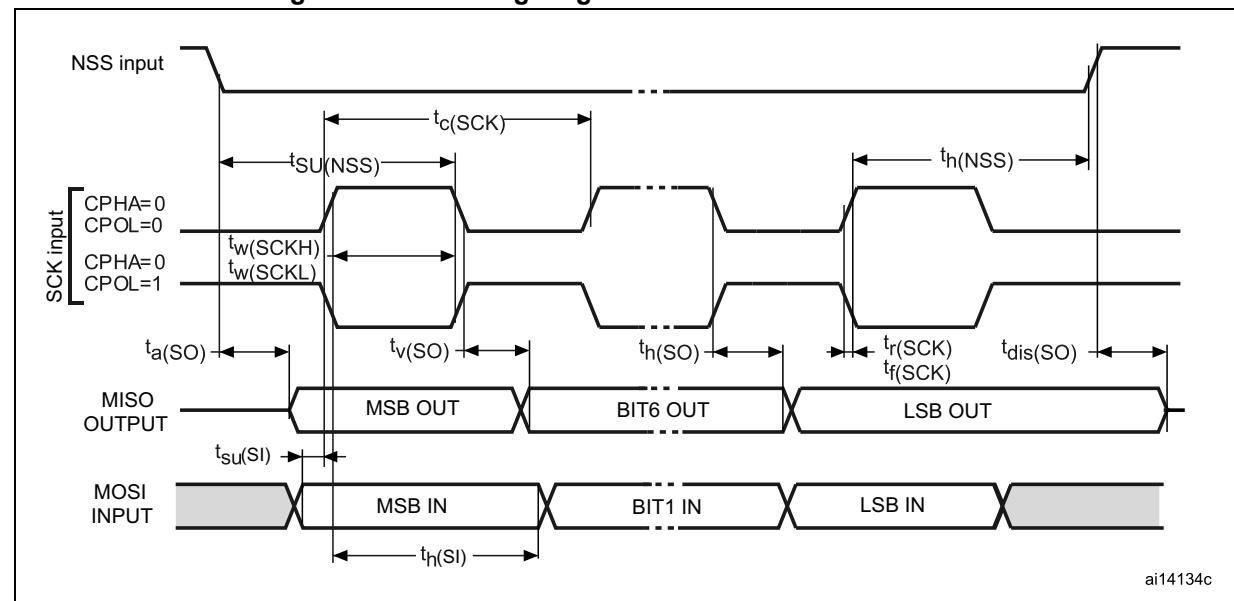
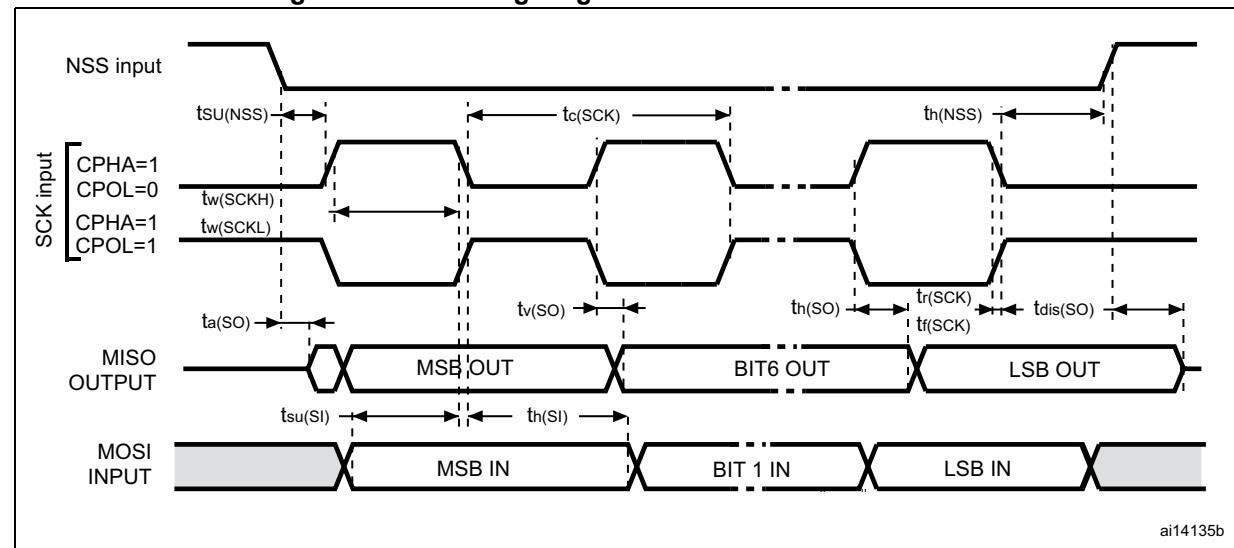


Figure 32. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are set at CMOS levels: $0.3 V_{DD}$ and $0.7 V_{DD}$.

Figure 31. SPI timing diagram - slave mode and CPHA = 0

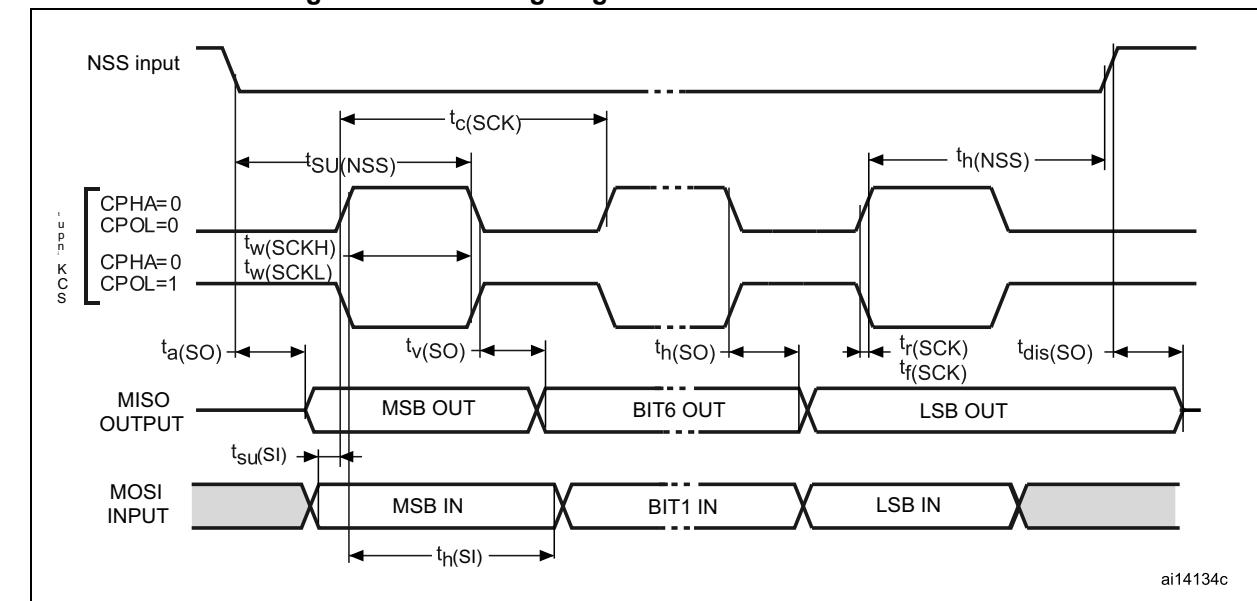
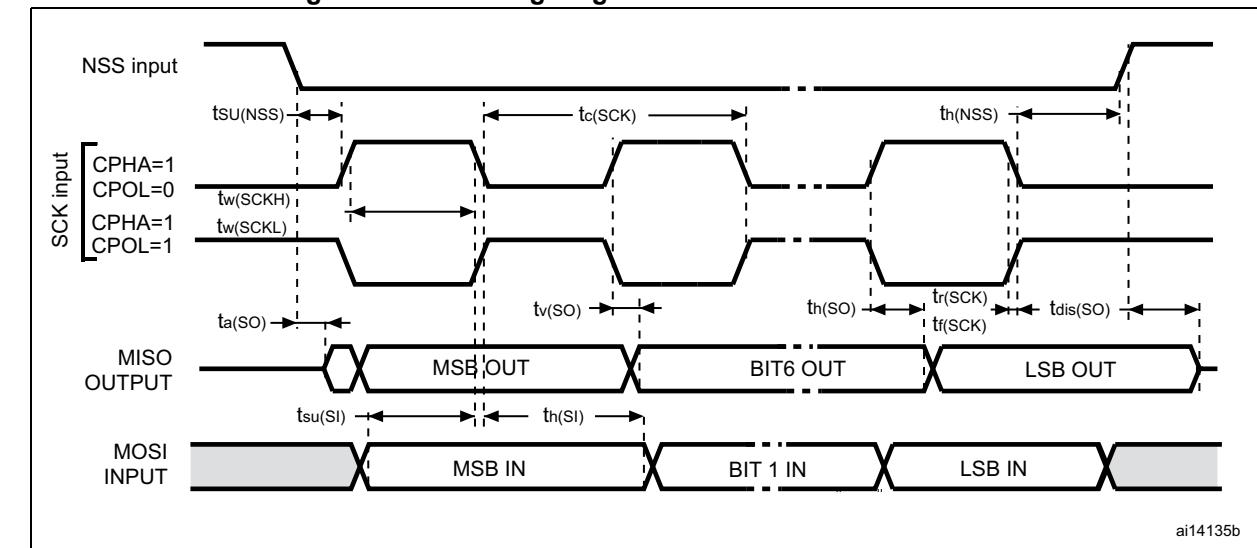


Figure 32. SPI timing diagram - slave mode and CPHA = 1

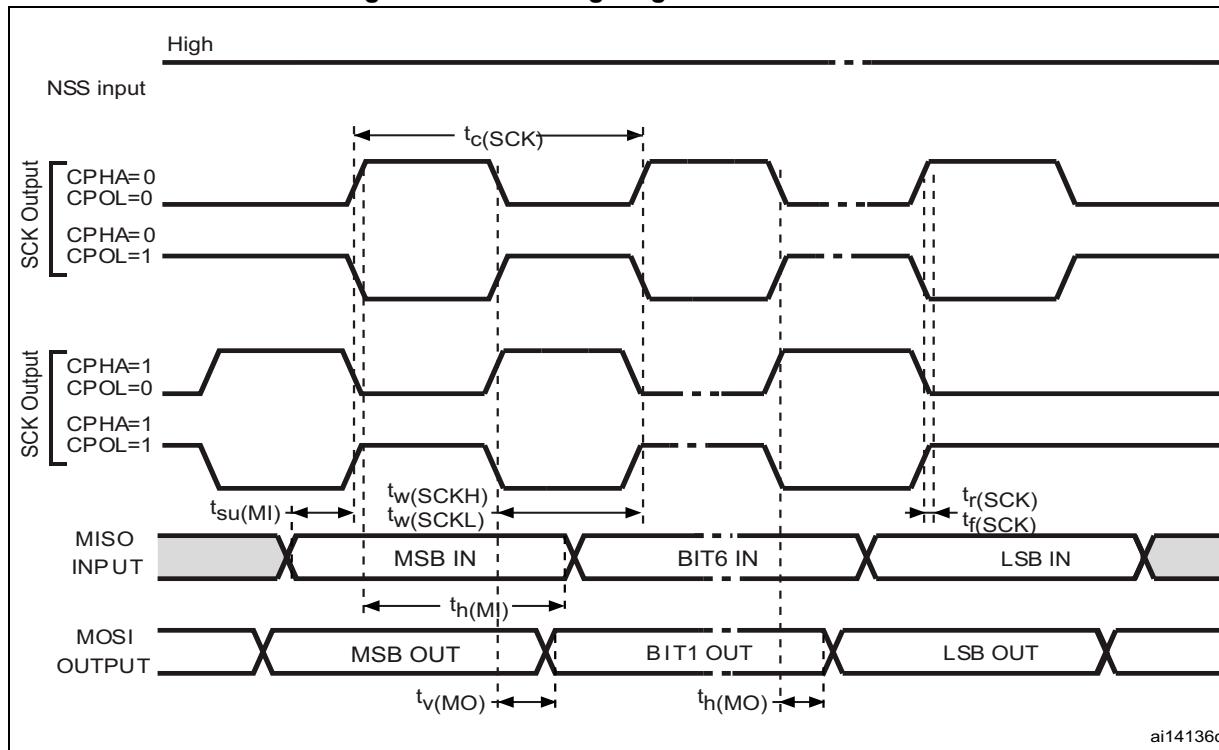


1. Measurement points are set at CMOS levels: $0.3 V_{DD}$ and $0.7 V_{DD}$.

Electrical characteristics

STM32WB55xx STM32WB35xx

Figure 33. SPI timing diagram - master mode

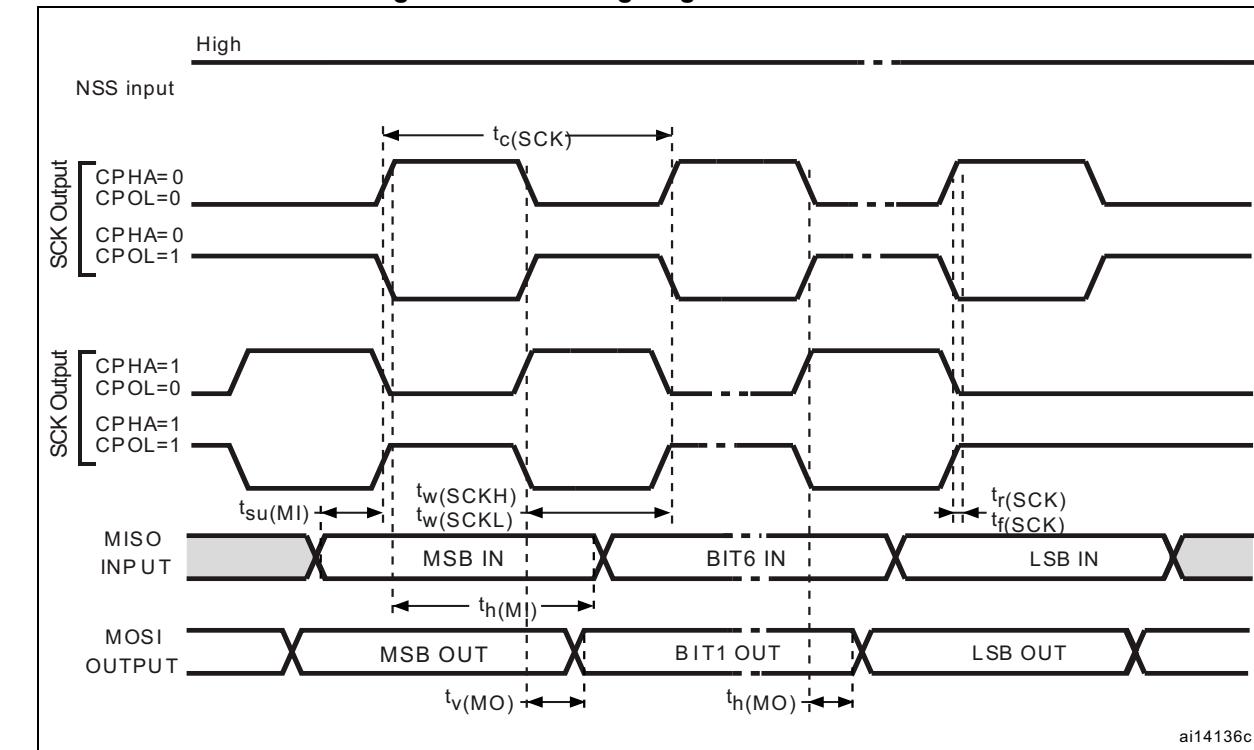


1. Measurement points are set at CMOS levels: $0.3 V_{DD}$ and $0.7 V_{DD}$.

Electrical characteristics

STM32WB55xx STM32WB35xx

Figure 33. SPI timing diagram - master mode



1. Measurement points are set at CMOS levels: $0.3 V_{DD}$ and $0.7 V_{DD}$.

Quad-SPI characteristics

Unless otherwise specified, the parameters given in [Table 94](#) and [Table 95](#) for Quad-SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in [Table 24: General operating conditions](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 15 or 20 pF
- Measurement points are set at CMOS levels: $0.5 \times V_{DD}$

Refer to [Section 6.3.17](#) for more details on the input/output alternate function characteristics.

Table 94. Quad-SPI characteristics in SDR mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F _{CK} 1/t _(CK)	Quad-SPI clock frequency	1.65 < V _{DD} < 3.6 V, C _{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		1.65 < V _{DD} < 3.6 V, C _{LOAD} = 15 pF Voltage Range 1	-	-	48	
		2.7 < V _{DD} < 3.6 V, C _{LOAD} = 15 pF Voltage Range 1	-	-	60	
		1.65 < V _{DD} < 3.6 V C _{LOAD} = 20 pF Voltage Range 2	-	-	16	
t _{w(CKH)}	Quad-SPI clock high and low time	f _{AHBCLK} = 48 MHz, presc=1	t _{(CK)/2 - 0.5}	-	t _{(CK)/2 + 1}	ns
t _{w(CKL)}			t _{(CK)/2 - 1}	-	t _{(CK)/2 + 0.5}	
t _{s(IN)}	Data input setup time	Voltage Range 1	2	-	-	
		Voltage Range 2	3.5	-	-	
t _{h(IN)}	Data input hold time	Voltage Range 1	4.5	-	-	
		Voltage Range 2	6	-	-	
t _{v(OUT)}	Data output valid time	Voltage Range 1	-	1	1.5	
		Voltage Range 2	-	1	1.5	
t _{h(OUT)}	Data output hold time	Voltage Range 1	0	-	-	
		Voltage Range 2	0	-	-	

1. Guaranteed by characterization results.

Quad-SPI characteristics

除非另有说明，否则四线SPI的参数如表94和表95所示，这些参数是在环境温度、AHB频率和VDD供电电压条件下进行的测试中得出的，详见表24：通用运行条件，配置如下：

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 15 or 20 pF
- Measurement points are set at CMOS levels: $0.5 \times V_{DD}$

Refer to [Section 6.3.17](#) for more details on the input/output alternate function characteristics.

Table 94. Quad-SPI characteristics in SDR mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F _{CK} 1/t _(CK)	Quad-SPI clock frequency	1.65 < V _{DD} < 3.6 V, C _{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		1.65 < V _{DD} < 3.6 V, C _{LOAD} = 15 pF Voltage Range 1	-	-	48	
		2.7 < V _{DD} < 3.6 V, C _{LOAD} = 15 pF Voltage Range 1	-	-	60	
		1.65 < V _{DD} < 3.6 V C _{LOAD} = 20 pF Voltage Range 2	-	-	16	
t _{w(CKH)}	Quad-SPI clock high and low time	f _{AHBCLK} = 48 MHz, presc=1	t _{(CK)/2 - 0.5}	-	t _{(CK)/2 + 1}	ns
t _{w(CKL)}			t _{(CK)/2 - 1}	-	t _{(CK)/2 + 0.5}	
t _{s(IN)}	Data input setup time	Voltage Range 1	2	-	-	
		Voltage Range 2	3.5	-	-	
t _{h(IN)}	Data input hold time	Voltage Range 1	4.5	-	-	
		Voltage Range 2	6	-	-	
t _{v(OUT)}	Data output valid time	Voltage Range 1	-	1	1.5	
		Voltage Range 2	-	1	1.5	
t _{h(OUT)}	Data output hold time	Voltage Range 1	0	-	-	
		Voltage Range 2	0	-	-	

1. Guaranteed by characterization results.

Table 95. Quad-SPI characteristics in DDR mode⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad-SPI clock frequency	1.65 < V_{DD} < 3.6 V, $C_{LOAD} = 20 \text{ pF}$ Voltage Range 1		-	-	40	MHz
		2.0 < V_{DD} < 3.6 V, $C_{LOAD} = 20 \text{ pF}$ Voltage Range 1		-	-	50	
		1.65 < V_{DD} < 3.6 V, $C_{LOAD} = 15 \text{ pF}$ Voltage Range 1		-	-	48	
		1.65 < V_{DD} < 3.6 V, $C_{LOAD} = 20 \text{ pF}$ Voltage Range 2		-	-	16	
$t_w(CKH)$	Quad-SPI clock high and low time	$f_{AHBCLK} = 48 \text{ MHz}$, presc=0	$t_{(CKY)/2}$	-	$t_{(CKY)/2 + 1}$		ns
$t_w(CKL)$			$t_{(CKY)/2 - 1}$	-	$t_{(CKY)/2}$		
$t_{sr(IN)}$	Data input setup time on rising edge	Voltage Range 1	2.5	-	-		
		Voltage Range 2	3.5				
$t_{sf(IN)}$	Data input setup time on falling edge	Voltage Range 1	2.5	-	-		
		Voltage Range 2	1.5				
$t_{hr(IN)}$	Data input hold time on rising edge	Voltage Range 1	5.5	-	-		
		Voltage Range 2	6.5				
$t_{hf(IN)}$	Data input hold time on falling edge	Voltage Range 1	5	-	-		
		Voltage Range 2	6				
$t_{vr(OUT)}$	Data output valid time on rising edge	Voltage Range 1	DHHC=0	-	4	5.5	ns
			DHHC=1		$t_{(CKY)/2 + 1}$	$t_{(CKY)/2 + 1.5}$	
		Voltage Range 2			4.5	7	
$t_{vf(OUT)}$	Data output valid time on falling edge	Voltage Range 1	DHHC=0	-	4	6	
			DHHC=1		$t_{(CKY)/2 + 1}$	$t_{(CKY)/2 + 2}$	
		Voltage Range 2			6	7.5	
$t_{hr(OUT)}$	Data output hold time on rising edge	Voltage Range 1	DHHC=0	-	2	-	
			DHHC=1		$t_{(CKY)/2 + 0.5}$	-	
		Voltage Range 2			3.5	-	
$t_{hf(OUT)}$	Data output hold time on falling edge	Voltage Range 1	DHHC=0	-	3	-	
			DHHC=1		$t_{(CKY)/2 + 0.5}$	-	
		Voltage Range 2			5	-	

1. Guaranteed by characterization results.

表 95. 四线串行接口在 DDR 模式下的特性 (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad-SPI clock frequency	1.65 < V_{DD} < 3.6 V, $C_{LOAD} = 20 \text{ pF}$ Voltage Range 1		-	-	40	MHz
		2.0 < V_{DD} < 3.6 V, $C_{LOAD} = 20 \text{ pF}$ Voltage Range 1		-	-	50	
		1.65 < V_{DD} < 3.6 V, $C_{LOAD} = 15 \text{ pF}$ Voltage Range 1		-	-	48	
		1.65 < V_{DD} < 3.6 V, $C_{LOAD} = 20 \text{ pF}$ Voltage Range 2		-	-	16	
$t_w(CKH)$	Quad-SPI clock high and low time	$f_{AHBCLK} = 48 \text{ MHz}$, presc=0	$t_{(CKY)/2}$	-	$t_{(CKY)/2 + 1}$		ns
$t_w(CKL)$			$t_{(CKY)/2 - 1}$	-	$t_{(CKY)/2}$		
$t_{sr(IN)}$	Data input setup time on rising edge	Voltage Range 1	2.5	-	-		
		Voltage Range 2	3.5				
$t_{sf(IN)}$	Data input setup time on falling edge	Voltage Range 1	2.5	-	-		
		Voltage Range 2	1.5				
$t_{hr(IN)}$	Data input hold time on rising edge	Voltage Range 1	5.5	-	-		
		Voltage Range 2	6.5				
$t_{hf(IN)}$	Data input hold time on falling edge	Voltage Range 1	5	-	-		
		Voltage Range 2	6				
$t_{vr(OUT)}$	Data output valid time on rising edge	Voltage Range 1	DHHC=0	-	4	5.5	ns
			DHHC=1		$t_{(CKY)/2 + 1}$	$t_{(CKY)/2 + 1.5}$	
		Voltage Range 2			4.5	7	
$t_{vf(OUT)}$	Data output valid time on falling edge	Voltage Range 1	DHHC=0	-	4	6	
			DHHC=1		$t_{(CKY)/2 + 1}$	$t_{(CKY)/2 + 2}$	
		Voltage Range 2			6	7.5	
$t_{hr(OUT)}$	Data output hold time on rising edge	Voltage Range 1	DHHC=0	-	2	-	
			DHHC=1		$t_{(CKY)/2 + 0.5}$	-	
		Voltage Range 2			3.5	-	
$t_{hf(OUT)}$	Data output hold time on falling edge	Voltage Range 1	DHHC=0	-	3	-	
			DHHC=1		$t_{(CKY)/2 + 0.5}$	-	
		Voltage Range 2			5	-	

1. Guaranteed by characterization results.

Figure 34. Quad-SPI timing diagram - SDR mode

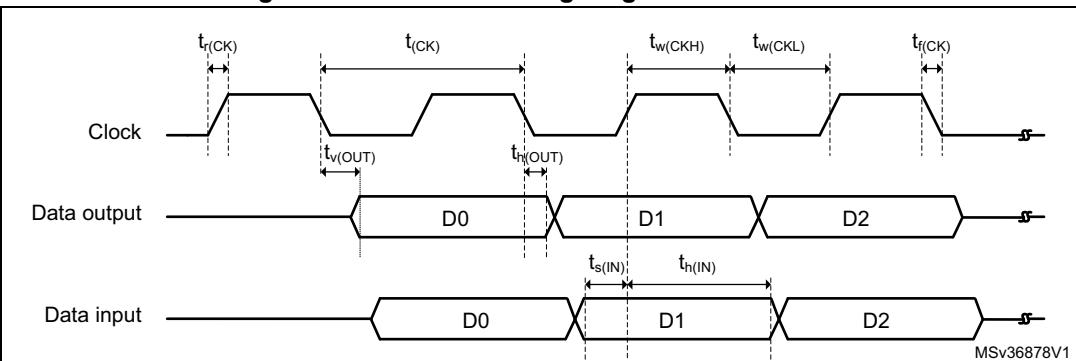
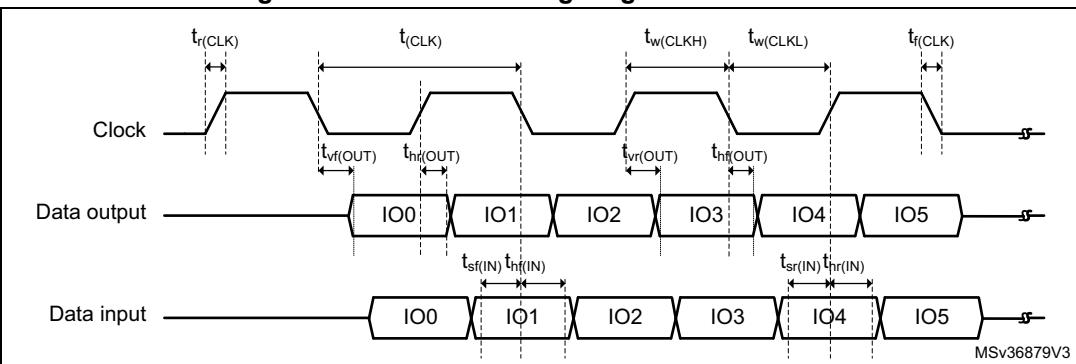


Figure 35. Quad-SPI timing diagram - DDR mode



SAI characteristics

Unless otherwise specified, the parameters given in [Table 96](#) for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 24: General operating conditions](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
 - Capacitive load $C = 30 \text{ pF}$
 - Measurement are performed at CMOS levels: $0.5 \times V_{DD}$
- Refer to [Section 6.3.17](#) for more details on the input/output alternate function characteristics (CK,SD,FS).

图 34. 四线SPI 时序图 - SDR模式

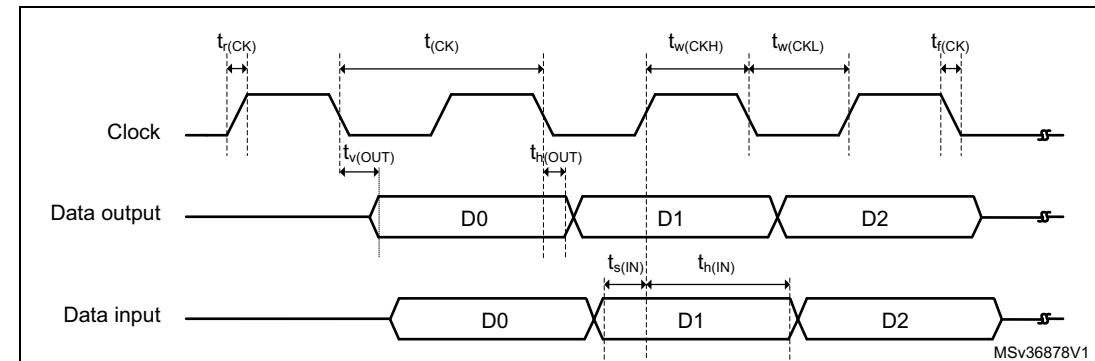
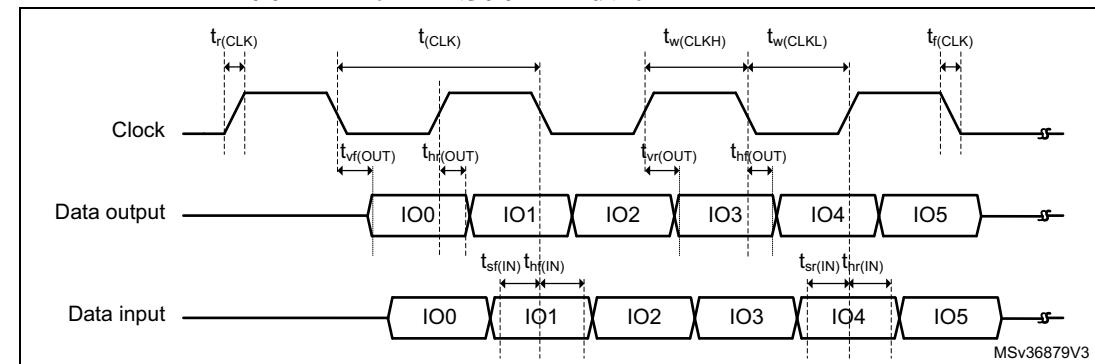


图 35. 四线SPI 时序图 - DDR模式



SAI characteristics

Unless otherwise specified, the parameters given in [Table 96](#) for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} 供电电压条件总结在表 24：通用运行条件中，配置如下：

STM32WB55xx STM32WB35xxSAI 特性输出速度设置为 OSPEEDRy[1:0] = 10 • 电容负载 $C = 30 \text{ pF}$ • 测量在 CMOS 水平上进行：
 $0.5 \times V_{DD}$

请参考第6.3.17节，了解更多关于输入/输出交替函数 特性(CK,SD,FS)的信息。

Table 96. SAI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI main clock output	-	-	50	
f_{CK}	SAI clock frequency ⁽²⁾	Master transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	23.5	MHz
		Master transmitter 1.65 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	16	
		Master receiver Voltage Range 1	-	16	
		Slave transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	26	
		Slave transmitter 1.65 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	20	
		Slave receiver Voltage Range 1	-	32	
		Voltage Range 2	-	8	
$t_{V(FS)}$	FS valid time	Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	21	ns
		Master mode 1.65 V ≤ V_{DD} ≤ 3.6 V	-	30	
$t_h(FS)$	FS hold time	Master mode	10	-	
$t_{su(FS)}$	FS setup time	Slave mode	1.5	-	
$t_h(FS)$	FS hold time	Slave mode	2.5	-	
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD_B_SR)}$		Slave receiver	1.5	-	
$t_h(SD_A_MR)$	Data input hold time	Master receiver	6.5	-	
$t_h(SD_B_SR)$		Slave receiver	2.5	-	
$t_{v(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	19	
		Slave transmitter (after enable edge) 1.65 V ≤ V_{DD} ≤ 3.6 V	-	25	
$t_h(SD_B_ST)$	Data output hold time	Slave transmitter (after enable edge)	10	-	
$t_{v(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	18.5	
		Master transmitter (after enable edge) 1.65 V ≤ V_{DD} ≤ 3.6 V	-	25	
$t_h(SD_A_MT)$	Data output hold time	Master transmitter (after enable edge)	10	-	

1. Guaranteed by characterization results.

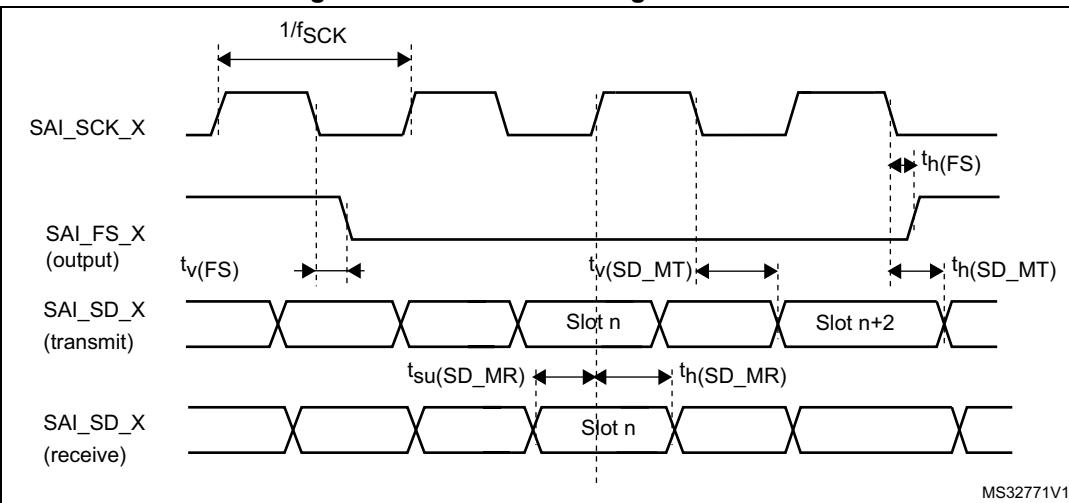
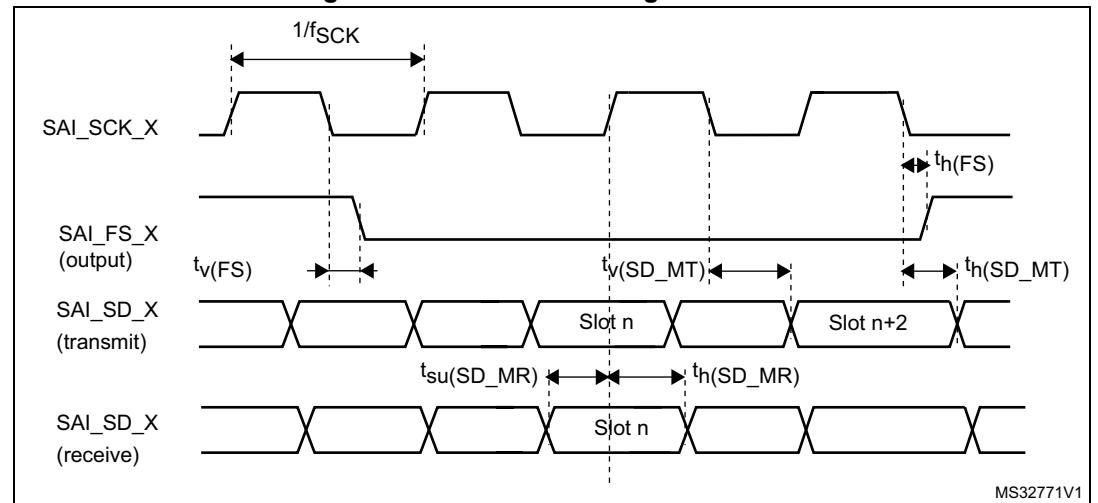
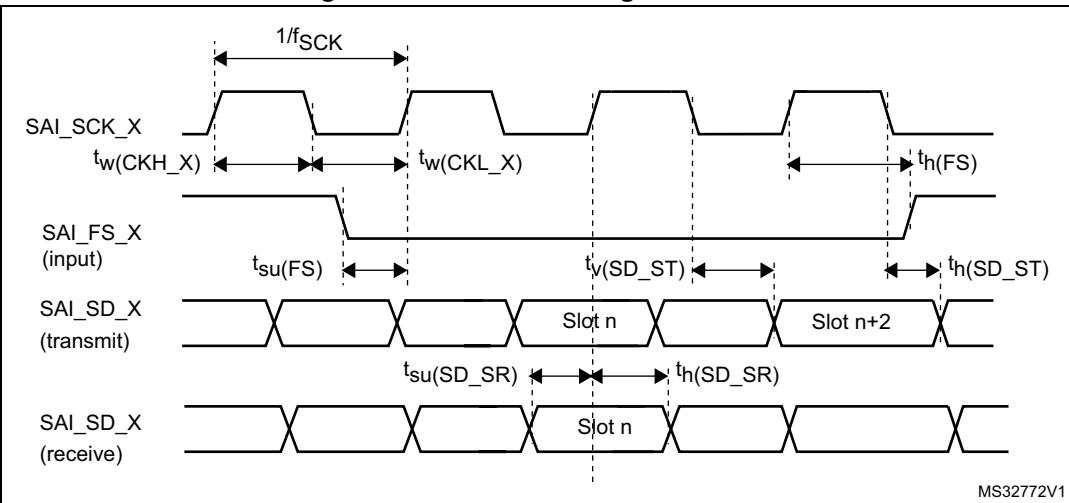
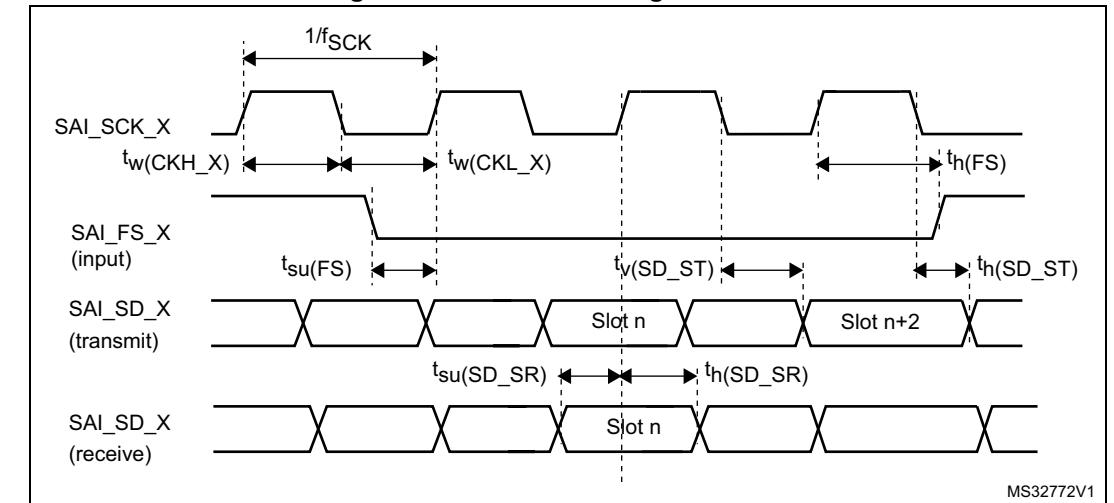
2. APB clock frequency must be at least twice SAI clock frequency.

表96. SAI 特性⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI main clock output	-	-	50	
f_{CK}	SAI clock frequency ⁽²⁾	Master transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	23.5	MHz
		Master transmitter 1.65 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	16	
		Master receiver Voltage Range 1	-	16	
		Slave transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	26	
		Slave transmitter 1.65 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	20	
		Slave receiver Voltage Range 1	-	32	
		Voltage Range 2	-	8	
$t_{V(FS)}$	FS valid time	Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	21	ns
		Master mode 1.65 V ≤ V_{DD} ≤ 3.6 V	-	30	
$t_h(FS)$	FS hold time	Master mode	10	-	
$t_{su(FS)}$	FS setup time	Slave mode	1.5	-	
$t_h(FS)$	FS hold time	Slave mode	2.5	-	
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD_B_SR)}$		Slave receiver	1.5	-	
$t_h(SD_A_MR)$	Data input hold time	Master receiver	6.5	-	
$t_h(SD_B_SR)$		Slave receiver	2.5	-	
$t_{v(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	19	
		Slave transmitter (after enable edge) 1.65 V ≤ V_{DD} ≤ 3.6 V	-	25	
$t_h(SD_B_ST)$	Data output hold time	Slave transmitter (after enable edge)	10	-	
$t_{v(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	18.5	
		Master transmitter (after enable edge) 1.65 V ≤ V_{DD} ≤ 3.6 V	-	25	
$t_h(SD_A_MT)$	Data output hold time	Master transmitter (after enable edge)	10	-	

1. Guaranteed by characterization results.

2. APB clock frequency must be at least twice SAI clock frequency.

Figure 36. SAI master timing waveforms**Figure 36. SAI master timing waveforms****Figure 37. SAI slave timing waveforms****Figure 37. SAI slave timing waveforms**

USB characteristics

The STM32WB55xx and STM32WB35xx USB interface is fully compliant with the USB specification version 2.0, and is USB-IF certified (for Full-speed device operation).

Table 97. USB electrical characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDUSB}	USB transceiver operating voltage	-	3.0 ⁽²⁾	-	3.6	V
$T_{crystal_less}$	USB crystal-less operation temperature	-	-15	-	85	°C
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1400	2300	3200	
$Z_{DRV}^{(3)}$	Output driver impedance ⁽⁴⁾	Driving high and low	28	36	44	

1. $T_A = -40$ to 125 °C unless otherwise specified.

2. The STM32WB55xx and STM32WB35xx USB functionality is ensured down to 2.7 V, but the full USB electrical characteristics are degraded in the 2.7 to 3.0 V voltage range.

3. Guaranteed by design.

4. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

USB 特性

STM32WB55xx 和 STM32WB35xx 的 USB 接口完全符合 USB 规范版本 2.0，且获得了 USB-IF 认证（用于全速设备运行）。

表97. USB电气特性⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDUSB}	USB transceiver operating voltage	-	3.0 ⁽²⁾	-	3.6	V
$T_{crystal_less}$	USB crystal-less operation temperature	-	-15	-	85	°C
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1400	2300	3200	
$Z_{DRV}^{(3)}$	Output driver impedance ⁽⁴⁾	Driving high and low	28	36	44	

1. $T_A = -40$ to 125 °C unless otherwise specified.

2. The STM32WB55xx and STM32WB35xx USB functionality is ensured down to 2.7 V, but the full USB electrical characteristics are degraded in the 2.7 to 3.0 V voltage range.

3. Guaranteed by design.

4. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in [Table 98](#) and [Table 99](#) are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in [Table 24: General operating conditions](#), with the following configuration:

- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Table 98. JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/t_{c(TCK)}$	TCK clock frequency	2.7 < V_{DD} < 3.6 V	-	-	29	MHz
		1.65 < V_{DD} < 3.6 V	-	-	21	
$t_{isu(TMS)}$	TMS input setup time	-	2.5	-	-	ns
$t_{ih(TMS)}$	TMS input hold time	-	2	-	-	
$t_{isu(TDI)}$	TDI input setup time	-	1.5	-	-	
$t_{ih(TDI)}$	TDI input hold time	-	2	-	-	
$t_{ov(TDO)}$	TDO output valid time	2.7 < V_{DD} < 3.6 V	-	13.5	16.5	
		1.65 < V_{DD} < 3.6 V	-	13.5	23	
$t_{oh(TDO)}$	TDO output hold time	-	11	-	-	

JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in [Table 98](#) and [Table 99](#) are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in [Table 24: General operating conditions](#), with the following configuration:

- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

表 98. JTAG 特性

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/t_{c(TCK)}$	TCK clock frequency	2.7 < V_{DD} < 3.6 V	-	-	29	MHz
		1.65 < V_{DD} < 3.6 V	-	-	21	
$t_{isu(TMS)}$	TMS input setup time	-	2.5	-	-	ns
$t_{ih(TMS)}$	TMS input hold time	-	2	-	-	
$t_{isu(TDI)}$	TDI input setup time	-	1.5	-	-	
$t_{ih(TDI)}$	TDI input hold time	-	2	-	-	
$t_{ov(TDO)}$	TDO output valid time	2.7 < V_{DD} < 3.6 V	-	13.5	16.5	
		1.65 < V_{DD} < 3.6 V	-	13.5	23	
$t_{oh(TDO)}$	TDO output hold time	-	11	-	-	

Table 99. SWD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1/t _{c(SWCLK)}	SWCLK clock frequency	2.7 < V _{DD} < 3.6 V	-	-	55	MHz
		1.65 < V _{DD} < 3.6 V	-	-	35	
t _{isU(TMS)}	SWDIO input setup time	-	2.5	-	-	ns
t _{ih(TMS)}	SWDIO input hold time	-	2	-	-	
t _{ov(TDO)}	SWDIO output valid time	2.7 < V _{DD} < 3.6 V	-	16	18	
		1.65 < V _{DD} < 3.6 V	-	16	28	
t _{oh(TDO)}	SWDIO output hold time	-	13	-	-	

Refer to [Section 6.3.17](#) for more details on the input/output alternate function characteristics (CK, SD, WS).

表99. SWD特性

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1/t _{c(SWCLK)}	SWCLK clock frequency	2.7 < V _{DD} < 3.6 V	-	-	55	MHz
		1.65 < V _{DD} < 3.6 V	-	-	35	
t _{isU(TMS)}	SWDIO input setup time	-	2.5	-	-	ns
t _{ih(TMS)}	SWDIO input hold time	-	2	-	-	
t _{ov(TDO)}	SWDIO output valid time	2.7 < V _{DD} < 3.6 V	-	16	18	
		1.65 < V _{DD} < 3.6 V	-	16	28	
t _{oh(TDO)}	SWDIO output hold time	-	13	-	-	

参考 [第6.3.17节](#) 了解更多关于输入/输出替代功能特性的信息(CK, SD, WS).

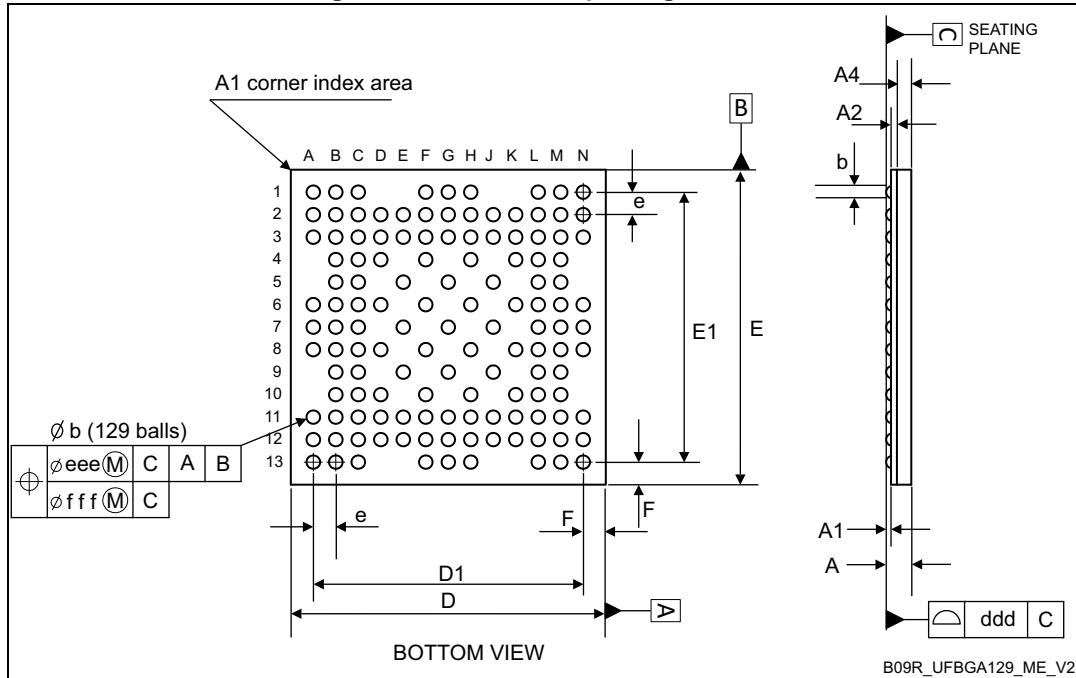
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com.
ECOPACK is an ST trademark.

7.1 UFBGA129 package information

This UFBGA is a 129-ball, 7 x 7 mm, 0.5 mm fine pitch, square ball grid array package.

Figure 38. UFBGA129 package outline



1. Drawing is not to scale.
2. - The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug.
- A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 100. UFBGA129 mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A ⁽²⁾	-	-	0.60	-	-	0.024
A1	-	-	0.11	-	-	0.004
A2	-	0.13	-	-	0.005	-
A4	-	0.32	-	-	0.013	-
b ⁽³⁾	0.24	0.29	0.34	0.009	0.011	0.013

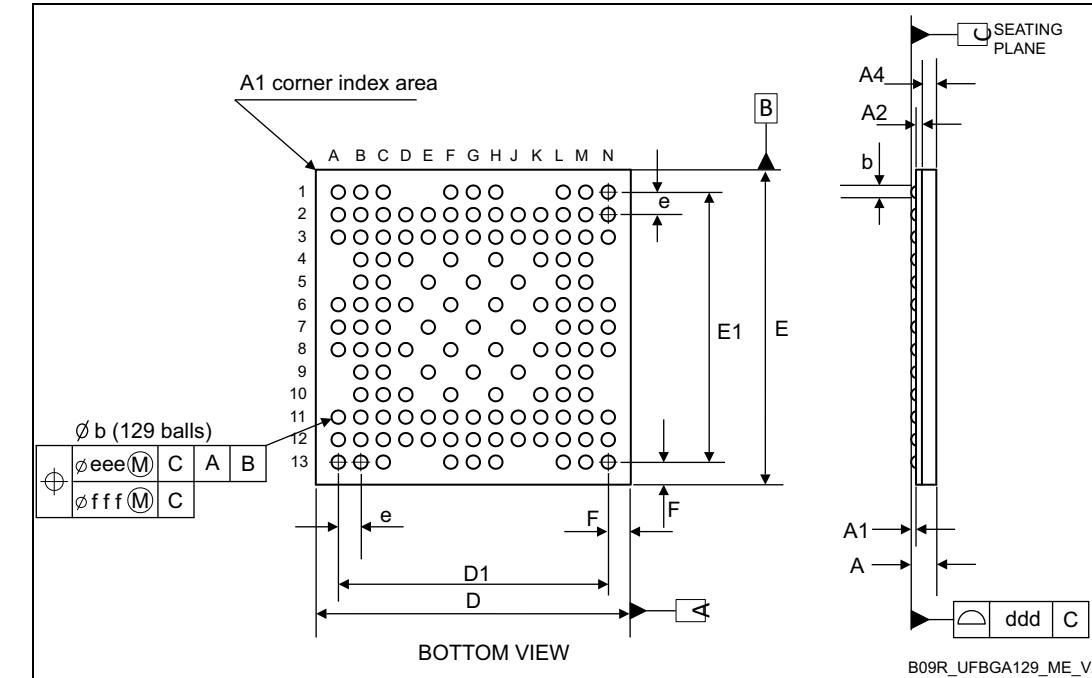
7 包装信息

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com.
ECOPACK is an ST trademark.

7.1 UFBGA129 包装信息

这个 UFBGA 是一个 129 球，7 x 7 毫米，0.5 毫米细距离的方形球阵包装。

图 38. UFBGA129 包装轮廓



1. Drawing is not to scale.
2. - 终端 A1 角必须通过使用角切口，墨水或金属化标记，或包体或集成热 Slug 的其他特征在顶部表面进行识别。- 在包装的底部表面上允许存在用于识别终端 A1 角的区分特征。每个角的确切形状是可选的。

表 100. UFBGA129 机械数据

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A ⁽²⁾	-	-	0.60	-	-	0.024
A1	-	-	0.11	-	-	0.004
A2	-	0.13	-	-	0.005	-
A4	-	0.32	-	-	0.013	-
b ⁽³⁾	0.24	0.29	0.34	0.009	0.011	0.013

Table 100. UFBGA129 mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
D	6.85	7.00	7.15	0.270	0.276	0.281
E	6.85	7.00	7.15	0.270	0.276	0.281
D1	-	6.00	-	-	0.236	-
E1	-	6.00	-	-	0.236	-
e	-	0.50	-	-	0.020	-
F	-	0.50	-	-	0.020	-
ddd	-	-	0.08	-	-	0.003
eee ⁽⁴⁾	-	-	0.15	-	-	0.006
fff ⁽⁵⁾	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to four decimal digits.
2. - UFBGA stands for Ultra Thin Profile Fine Pitch Ball Grid Array.
 - Ultra thin profile: $0.50 < A \leq 0.65\text{mm}$ / Fine pitch: $e < 1.00\text{mm}$ pitch.
 - The total profile height (Dim A) is measured from the seating plane to the top of the component
 - The maximum total package height is calculated by the following methodology:
 $A_{\text{Max}} = A_1 \text{ Typ} + A_2 \text{ Typ} + A_4 \text{ Typ} + \sqrt{(A_1^2 + A_2^2 + A_4^2)}$ tolerance values.
3. The typical balls diameters before mounting is 0.20 mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datum A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datum A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

Figure 39. UFBGA129 recommended footprint

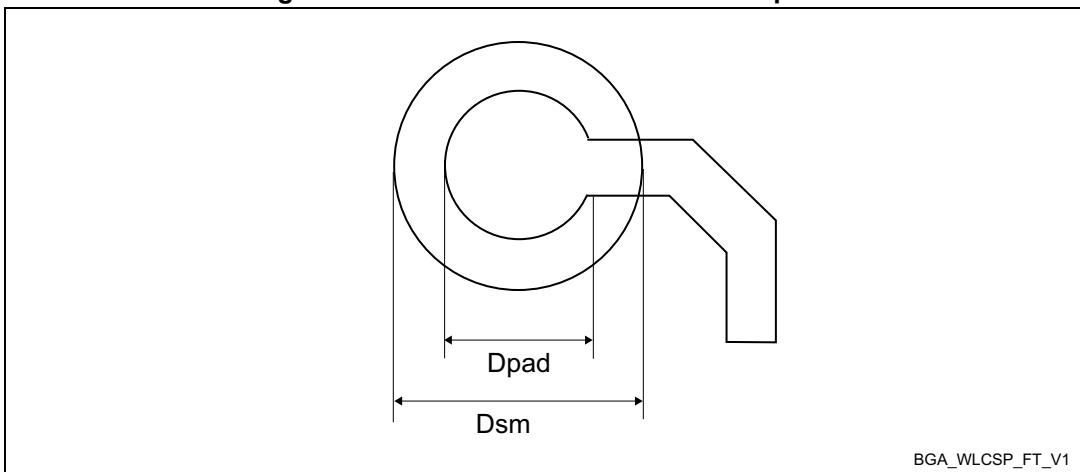


表 100. UFBGA129机械数据 (继续)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
D	6.85	7.00	7.15	0.270	0.276	0.281
E	6.85	7.00	7.15	0.270	0.276	0.281
D1	-	6.00	-	-	0.236	-
E1	-	6.00	-	-	0.236	-
e	-	0.50	-	-	0.020	-
F	-	0.50	-	-	0.020	-
ddd	-	-	0.08	-	-	0.003
eee ⁽⁴⁾	-	-	0.15	-	-	0.006
fff ⁽⁵⁾	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to four decimal digits.
2. - UFBGA 超薄轮廓距球阵。 - 超薄轮廓: $0.50 < A \leq 0.65\text{mm}$ / 细距离: $e < 1.00\text{mm}$ pitch。 - 总轮廓高度 (Dim A) 从座面到组件顶部测量。 - 最大总包装高度通过以下方法计算: $A_{\text{Max}} = A_1 \text{ Typ} + A_2 \text{ Typ} + A_4 \text{ Typ} + \sqrt{(A_1^2 + A_2^2 + A_4^2)}$ 容差值。
3. The typical balls diameters before mounting is 0.20 mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datum A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datum A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

Figure 39. UFBGA129 recommended footprint

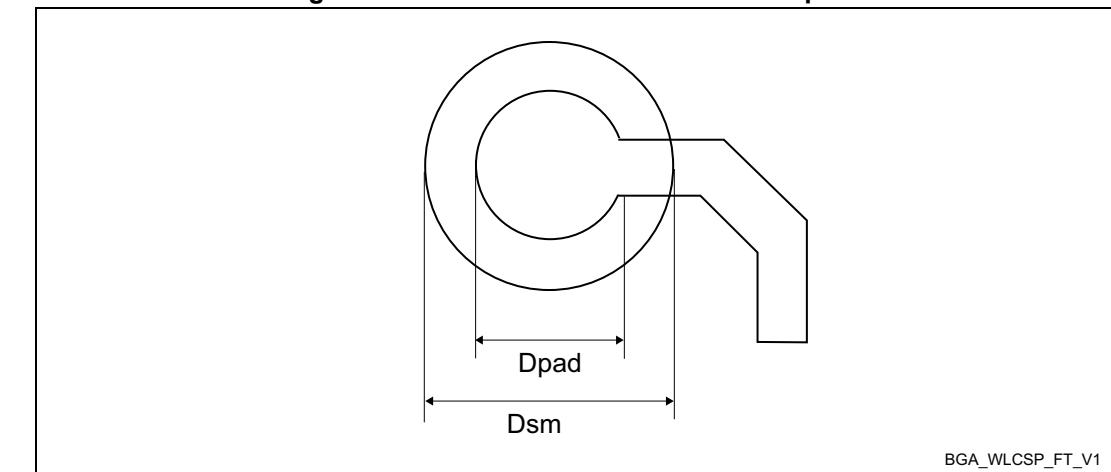


Table 101. UFBGA129 recommended PCB design rules

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0,360 mm
Dsm	0.460 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.360 mm
Stencil thickness	0.100 mm

Device marking for UFBGA129

Figure 40 gives an example of topside marking orientation versus pin 1 identifier location. The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 40. UFBGA129 marking example (package top view)

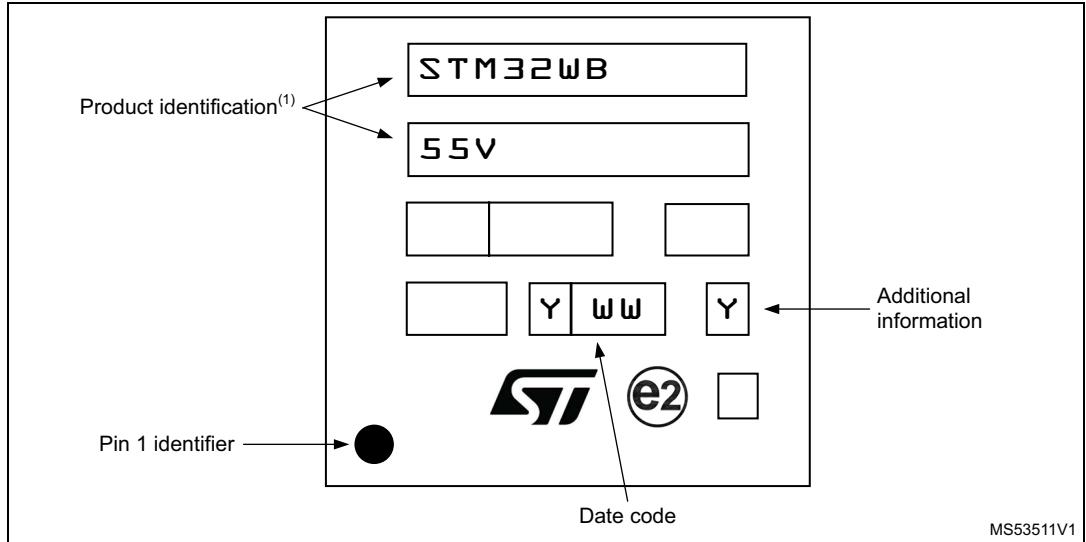


表 101. UFBGA129推荐的PCB设计规则

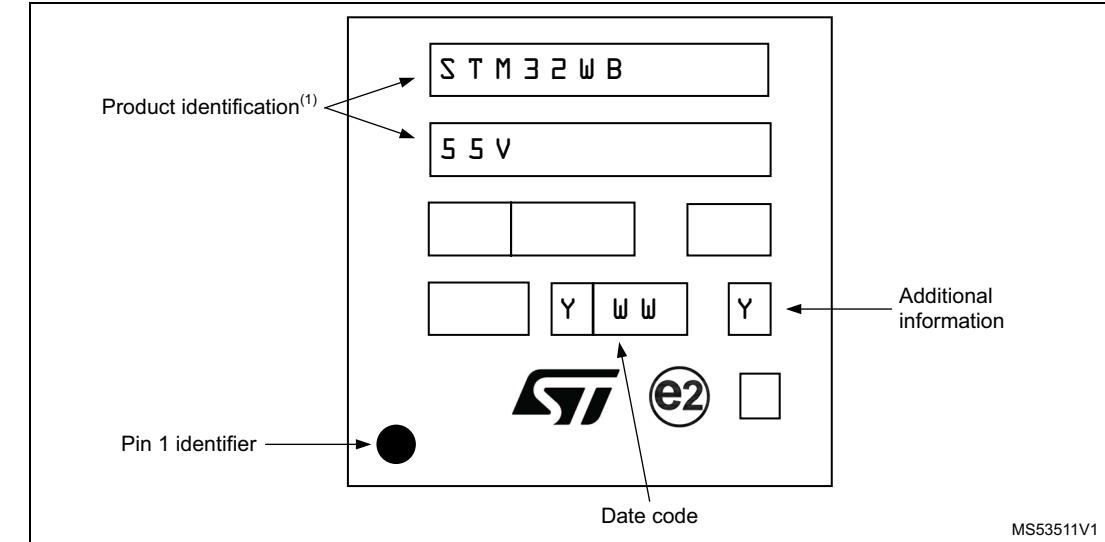
Dimension	Recommended values
Pitch	0.5 mm
Dpad	0,360 mm
Dsm	0.460 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.360 mm
Stencil thickness	0.100 mm

Device marking for UFBGA129

图40展示了正面标记方向与引脚1标识位置的对比。打印标记可能会因供应链而异。

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 40. UFBGA129 marking example (package top view)



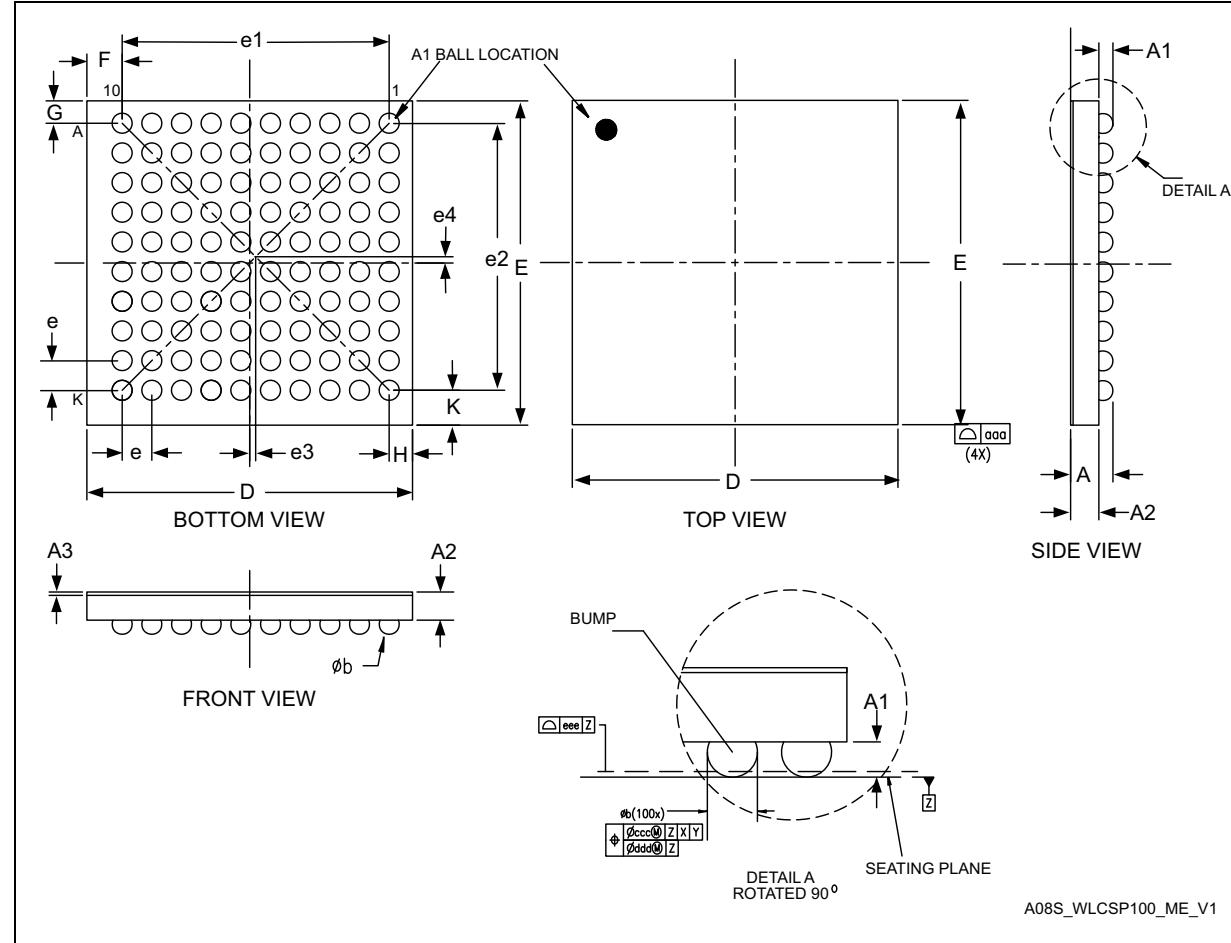
1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

1. 标记为 ES 或 E 或附有工程样本通知信的零件尚未合格，因此不获准在生产中使用。ST 不负责任何由于使用这些零件而导致的后果。在任何情况下，ST 都不负责客户在生产中使用这些工程样本。在决定使用这些工程样本进行资格认证活动之前，必须联系 ST 的质量部门。

7.2 WLCSP100 package information

WLCSP100 is a 100-ball, 4.390 x 4.371 mm, 0.4 mm pitch, wafer level chip scale package.

Figure 41. WLCSP100 outline



7.2 WLCSP100 封装信息

WLCSP100 是一个 100 球，4.390 x 4.371 mm，0.4 mm 布距，晶圆级芯片级封装。

图41. WLCSP100 轮廓

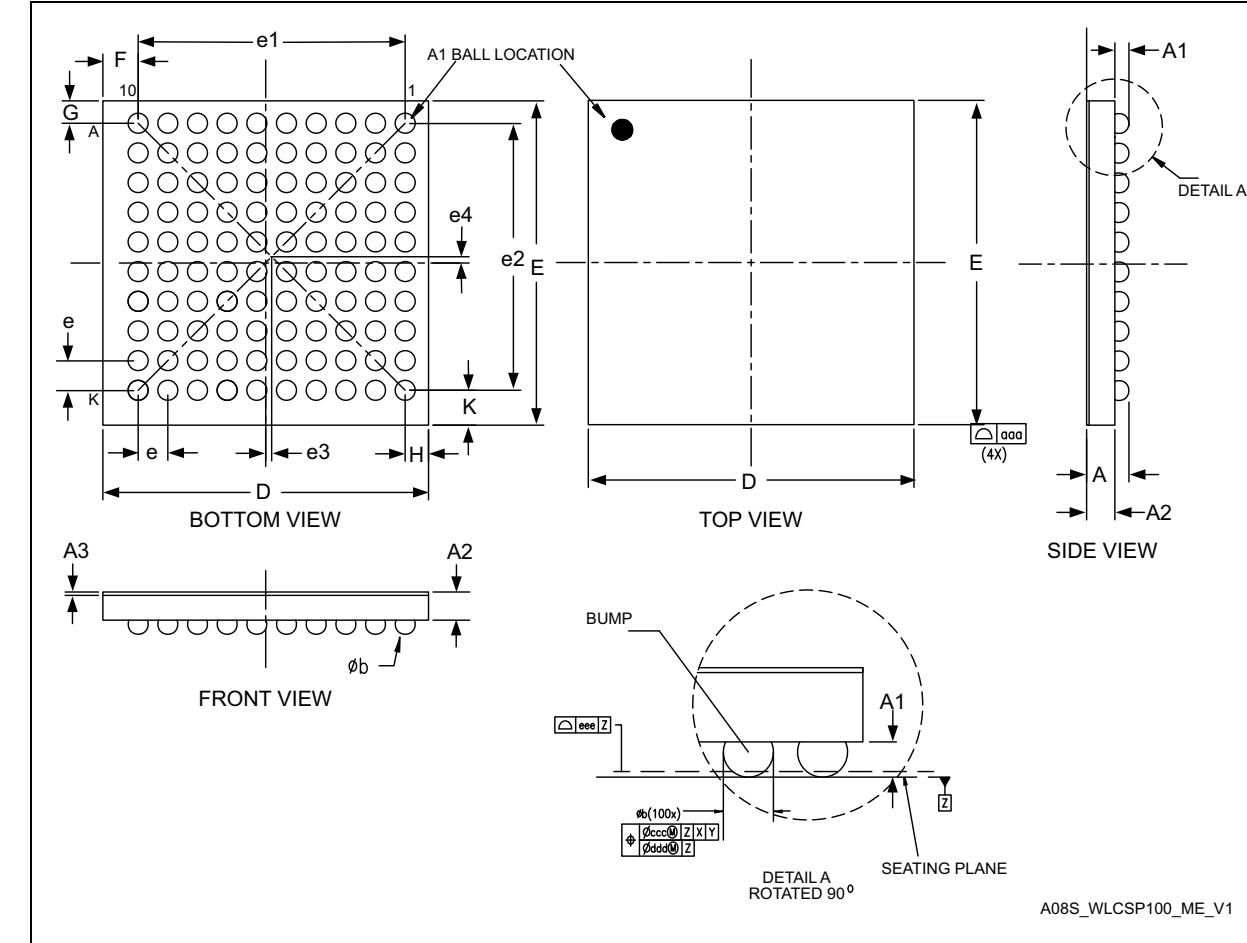


Table 102. WLCSP100 mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3	-	0.025 ⁽²⁾	-	-	0.001	-
b	0.22	0.25	0.28	0.009	0.010	0.0110
D	4.38	4.40	4.42	0.1715	0.1728	0.1742
E	4.36	4.38	4.40	0.1707	0.1721	0.1735
e	-	0.40	-	-	0.0157	-
e1	-	3.60	-	-	0.1417	-
e2	-	3.60	-	-	0.1417	-
e3	-	0.08	-	-	0.0031	-
e4	-	0.08	-	-	0.0033	-
F	-	0.480 ⁽³⁾	-	-	0.0187	-
G	-	0.306 ⁽³⁾	-	-	0.0119	-
H	-	0.32	-	-	0.0124	-
K	-	0.47	-	-	0.0185	-
aaa	-	-	0.10	-	-	0.0039
bbb	-	-	0.10	-	-	0.0039
ccc	-	-	0.10	-	-	0.0039
ddd	-	-	0.05	-	-	0.0020
eee	-	-	0.05	-	-	0.0020

1. Values in inches are converted from mm and rounded to the third decimal place.

2. Nominal dimension rounded to the third decimal place results from process capability.

3. Calculated dimensions are rounded to third decimal place.

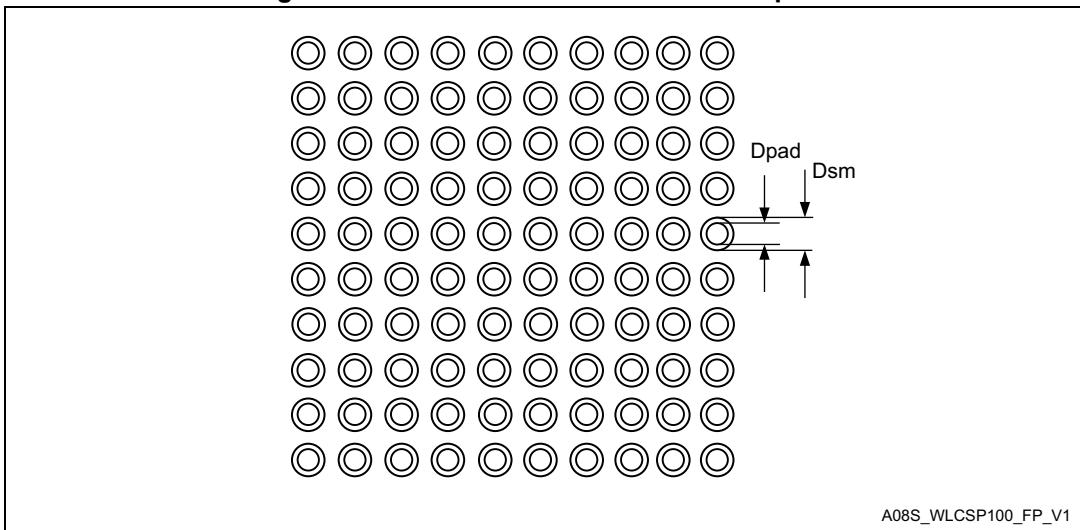
表 102. WLCSP100机械数据

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3	-	0.025 ⁽²⁾	-	-	0.001	-
b	0.22	0.25	0.28	0.009	0.010	0.0110
D	4.38	4.40	4.42	0.1715	0.1728	0.1742
E	4.36	4.38	4.40	0.1707	0.1721	0.1735
e	-	0.40	-	-	0.0157	-
e1	-	3.60	-	-	0.1417	-
e2	-	3.60	-	-	0.1417	-
e3	-	0.08	-	-	0.0031	-
e4	-	0.08	-	-	0.0033	-
F	-	0.480 ⁽³⁾	-	-	0.0187	-
G	-	0.306 ⁽³⁾	-	-	0.0119	-
H	-	0.32	-	-	0.0124	-
K	-	0.47	-	-	0.0185	-
aaa	-	-	0.10	-	-	0.0039
bbb	-	-	0.10	-	-	0.0039
ccc	-	-	0.10	-	-	0.0039
ddd	-	-	0.05	-	-	0.0020
eee	-	-	0.05	-	-	0.0020

1. Values in inches are converted from mm and rounded to the third decimal place.

2. Nominal dimension rounded to the third decimal place results from process capability.

3. Calculated dimensions are rounded to third decimal place.

Figure 42. WLCSP100 recommended footprint

A08S_WLCSP100_FP_V1

- Dimensions are expressed in millimeters.

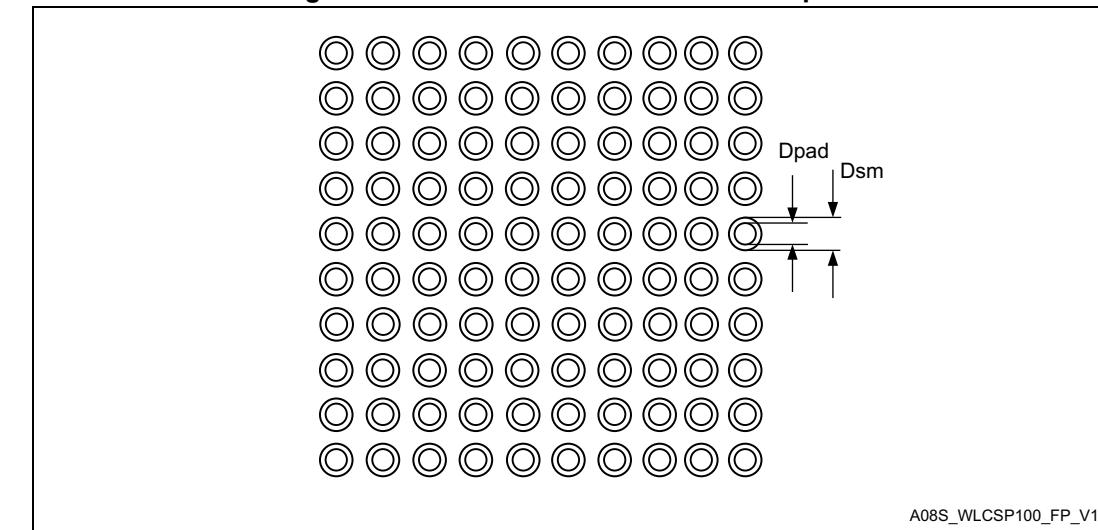
Table 103. WLCSP100 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking for WLCSP100

Figure 43 gives an example of topside marking orientation versus pin 1 identifier location. The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 42. WLCSP100 recommended footprint

A08S_WLCSP100_FP_V1

- 尺寸以毫米为单位表示。

Table 103. WLCSP100 recommended PCB design rules

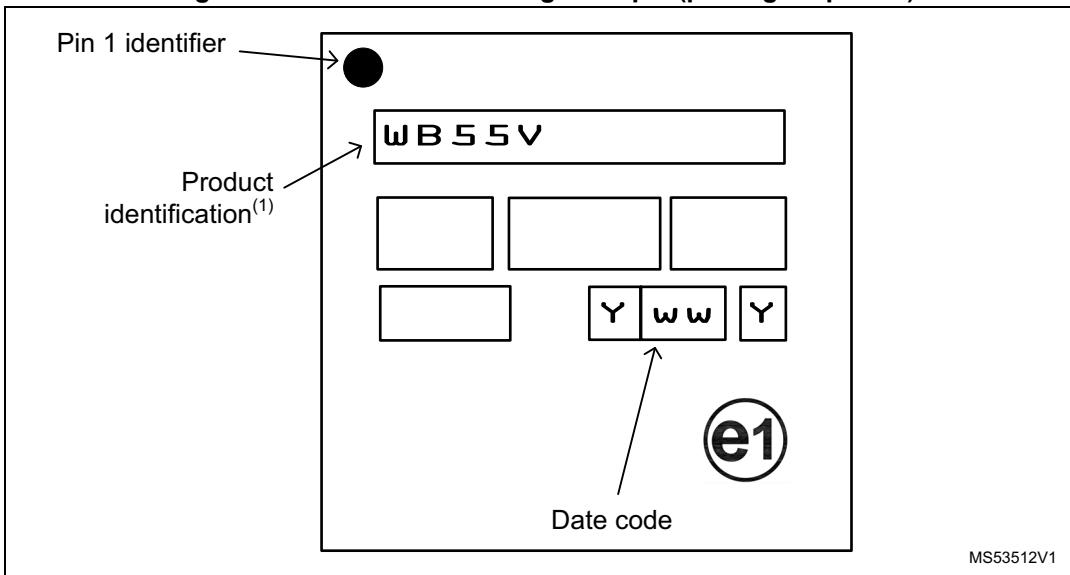
Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

WLCSP100 的设备标记

*图43*展示了正面标记方向与引脚1标识位置的比较。打印标记可能会因为供应链的不同而有所差异。

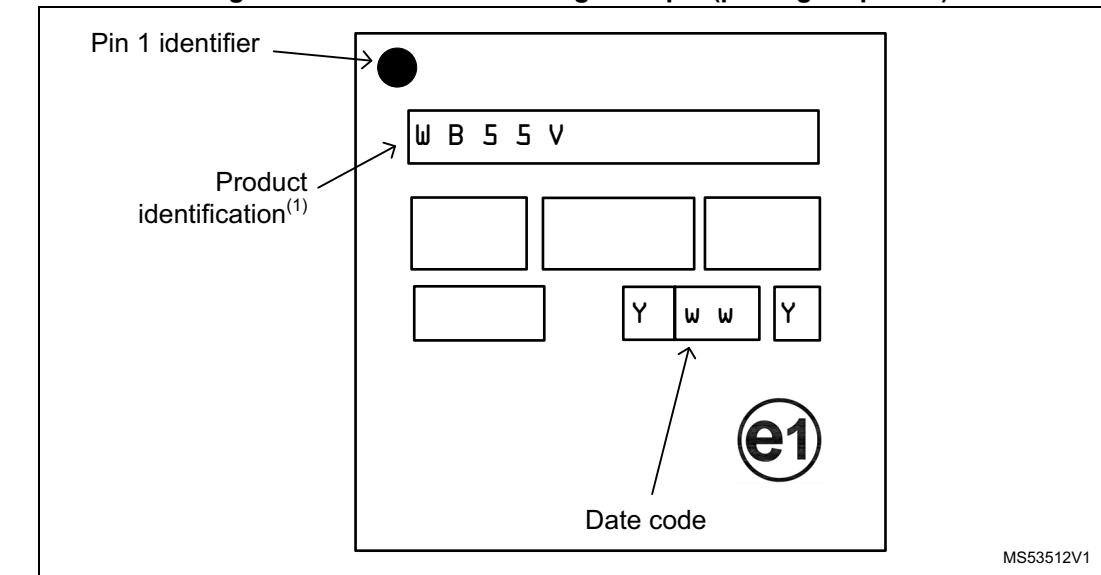
其他可选标记或嵌入/突出标记，用于识别供应链操作中的零件，以下没有显示。

Figure 43. WLCSP100 marking example (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Figure 43. WLCSP100 marking example (package top view)

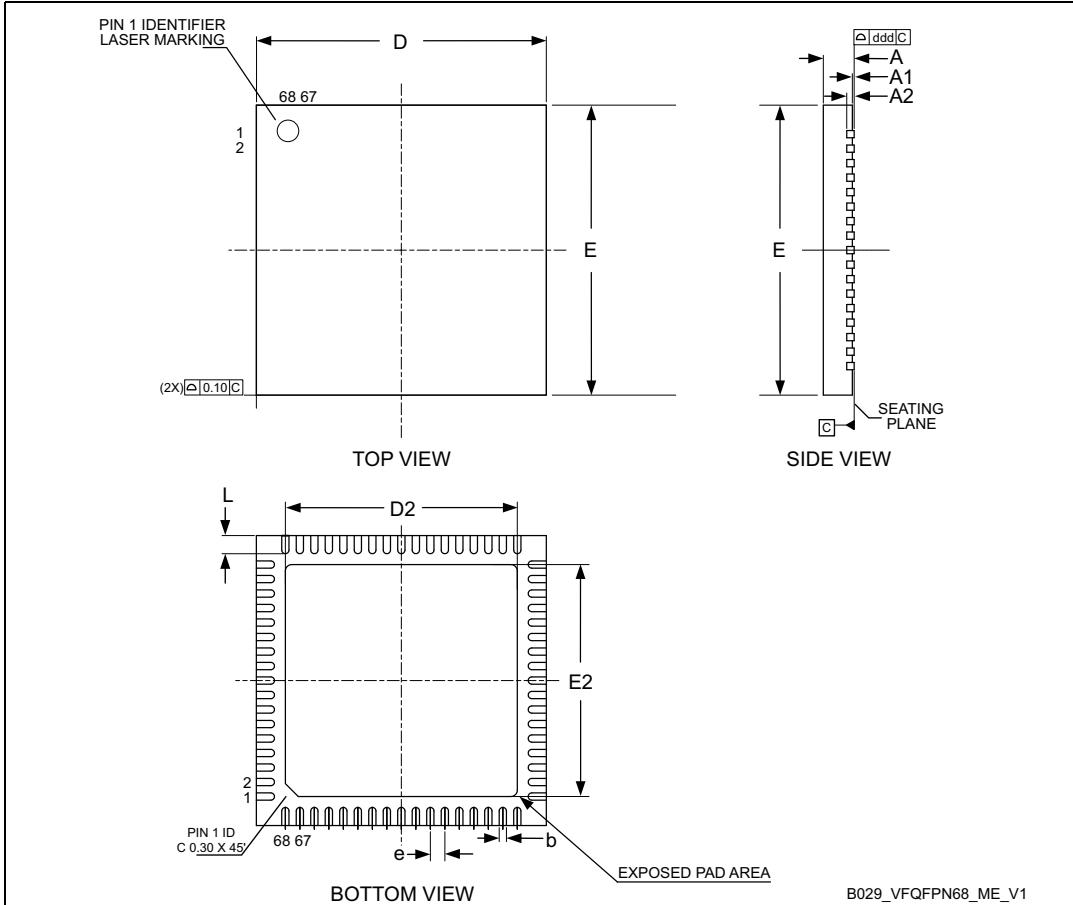


1. 标记为 ES 或 E 或附有工程样本通知信的零件尚未合格，因此不获准在生产中使用。ST 不负责任由于使用这些零件而产生的后果。在任何事件下，ST 都不负责客户在生产中使用这些工程样本。在决定使用这些工程样本进行资格认证活动之前，必须联系 ST 的质量部门。

7.3 VFQFPN68 package information

VFQFPN68 is a 8 x 8 mm, 0.4 mm pitch, very thin fine pitch quad flat package.

Figure 44. VFQFPN68 package outline



B029_VFQFPN68_ME_V1

1. VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Packages No lead. Sawed version. Very thin profile: $0.80 < A \leq 1.00$ mm.
2. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body. Exact shape and size of this feature is optional.

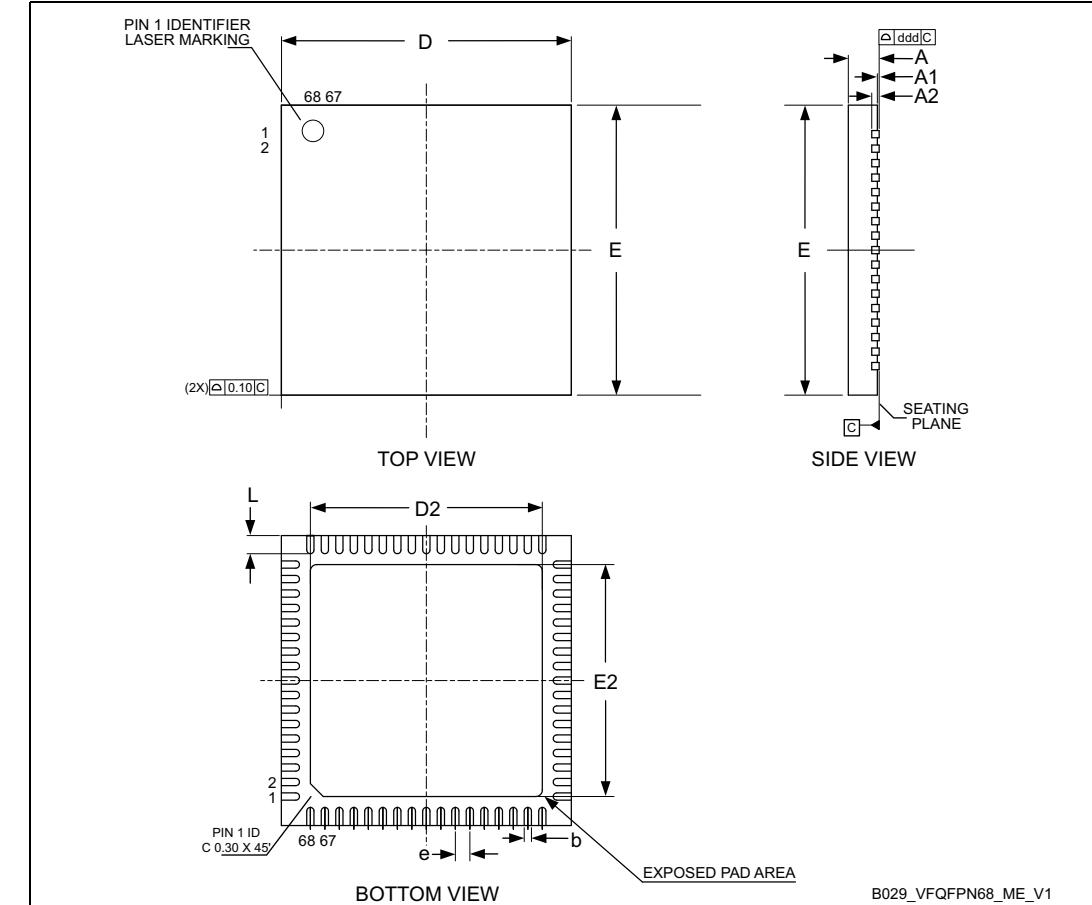
Table 104. VFQFPN68 mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0	0.02	0.05	0	0.0008	0.0020
A3	-	0.20	-	-	0.0008	-
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
D	7.85	8.00	8.15	0.3091	0.3150	0.3209
D2	6.30	6.40	6.50	0.2480	0.2520	0.2559

7.3 VFQFPN68 package information

VFQFPN68 is a 8 x 8 mm, 0.4 mm pitch, very thin fine pitch quad flat package.

Figure 44. VFQFPN68 package outline



1. VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Packages No lead. Sawed version. Very thin profile: $0.80 < A \leq 1.00$ mm.
2. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body. Exact shape and size of this feature is optional.

Table 104. VFQFPN68 mechanical data

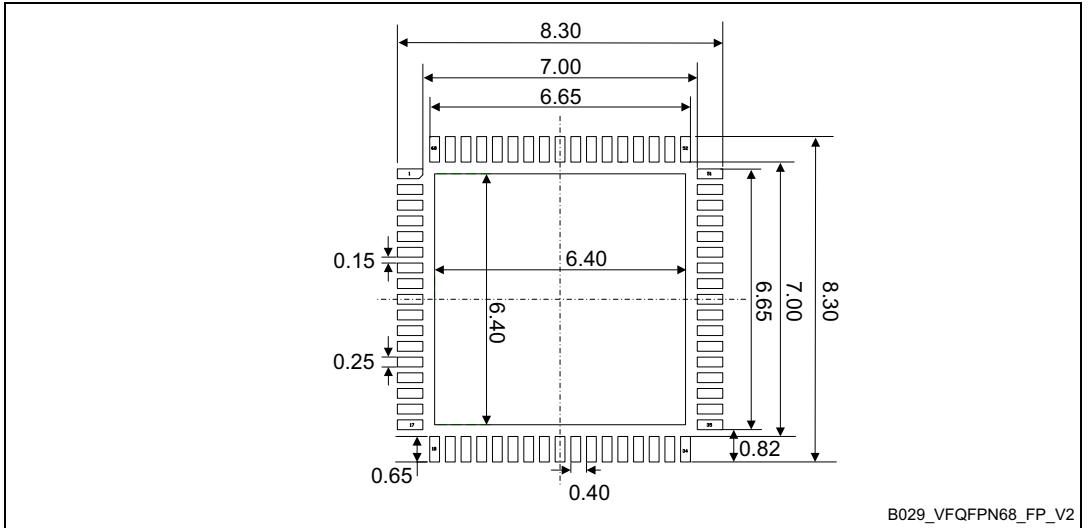
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0	0.02	0.05	0	0.0008	0.0020
A3	-	0.20	-	-	0.0008	-
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
D	7.85	8.00	8.15	0.3091	0.3150	0.3209
D2	6.30	6.40	6.50	0.2480	0.2520	0.2559

Table 104. VFQFPN68 mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E	7.85	8.00	8.15	0.3091	0.3150	0.3209
E2	6.30	6.40	6.50	0.2480	0.2520	0.2559
e	-	0.40	-	-	0.0157	-
L	0.40	0.50	0.60	0.0157	0.0197	0.0236
ddd	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 45. VFQFPN68 recommended footprint



1. Dimensions are expressed in millimeters.

Device marking for VFQFPN68

Figure 45 gives an example of topside marking orientation versus pin 1 identifier location. The printed markings may differ depending on the supply chain.

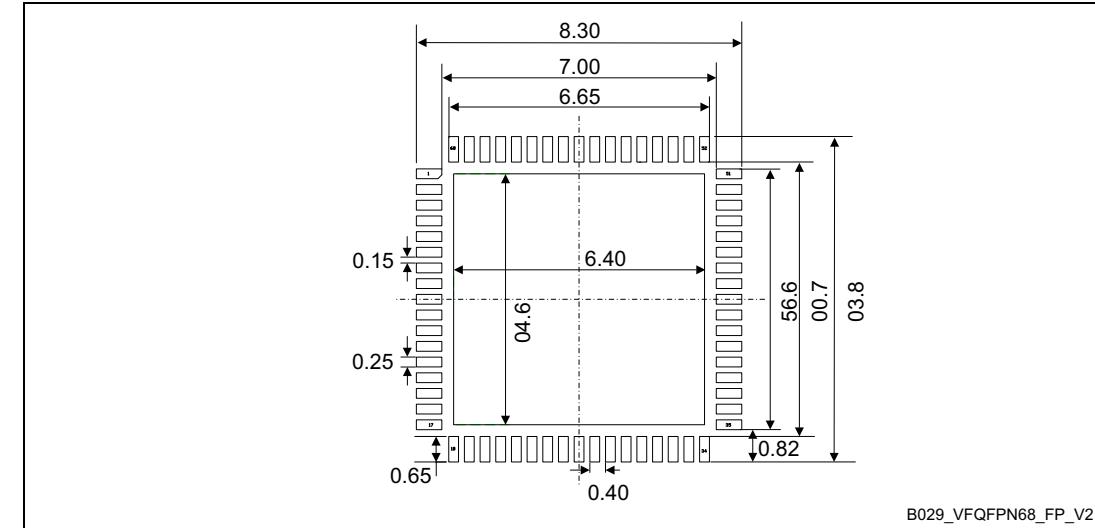
Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Table 104. VFQFPN68 mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E	7.85	8.00	8.15	0.3091	0.3150	0.3209
E2	6.30	6.40	6.50	0.2480	0.2520	0.2559
e	-	0.40	-	-	0.0157	-
L	0.40	0.50	0.60	0.0157	0.0197	0.0236
ddd	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.

图45. VFQFPN68 推荐尺寸



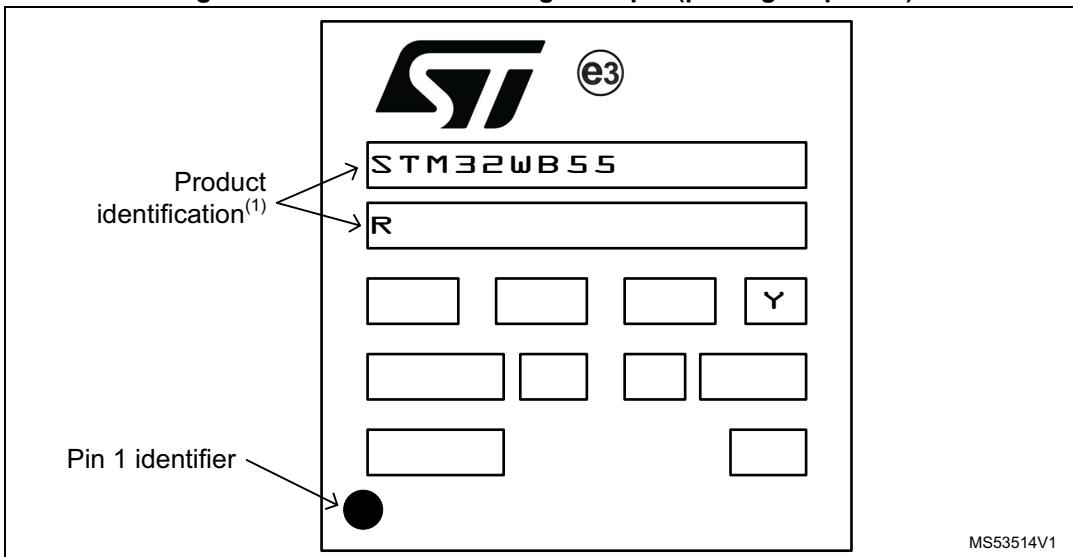
1. Dimensions are expressed in millimeters.

Device marking for VFQFPN68

Figure 45 gives an example of topside marking orientation versus pin 1 identifier location. The printed markings may differ depending on the supply chain.

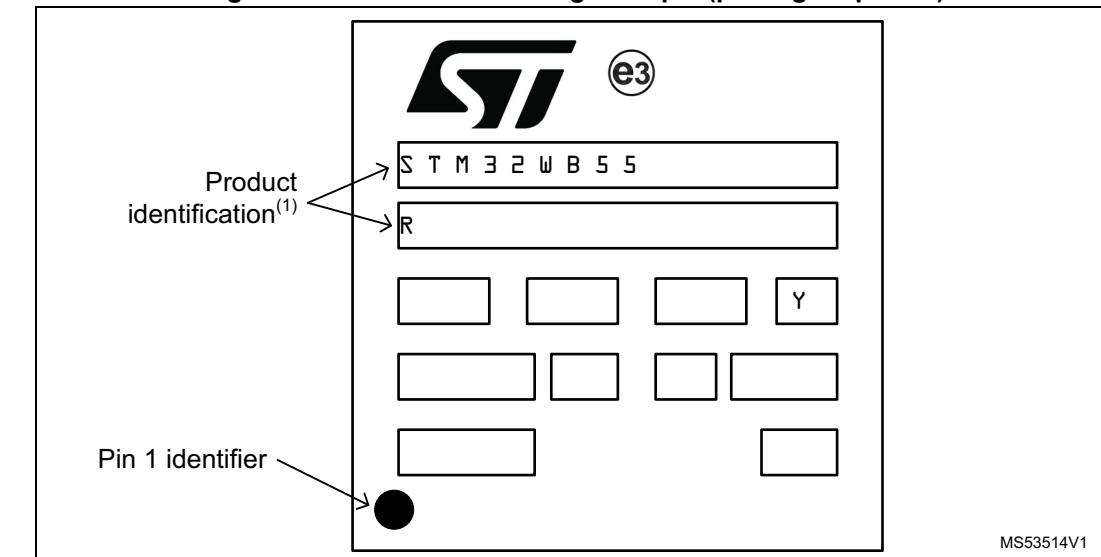
Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 46. VFQFPN68 marking example (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Figure 46. VFQFPN68 marking example (package top view)

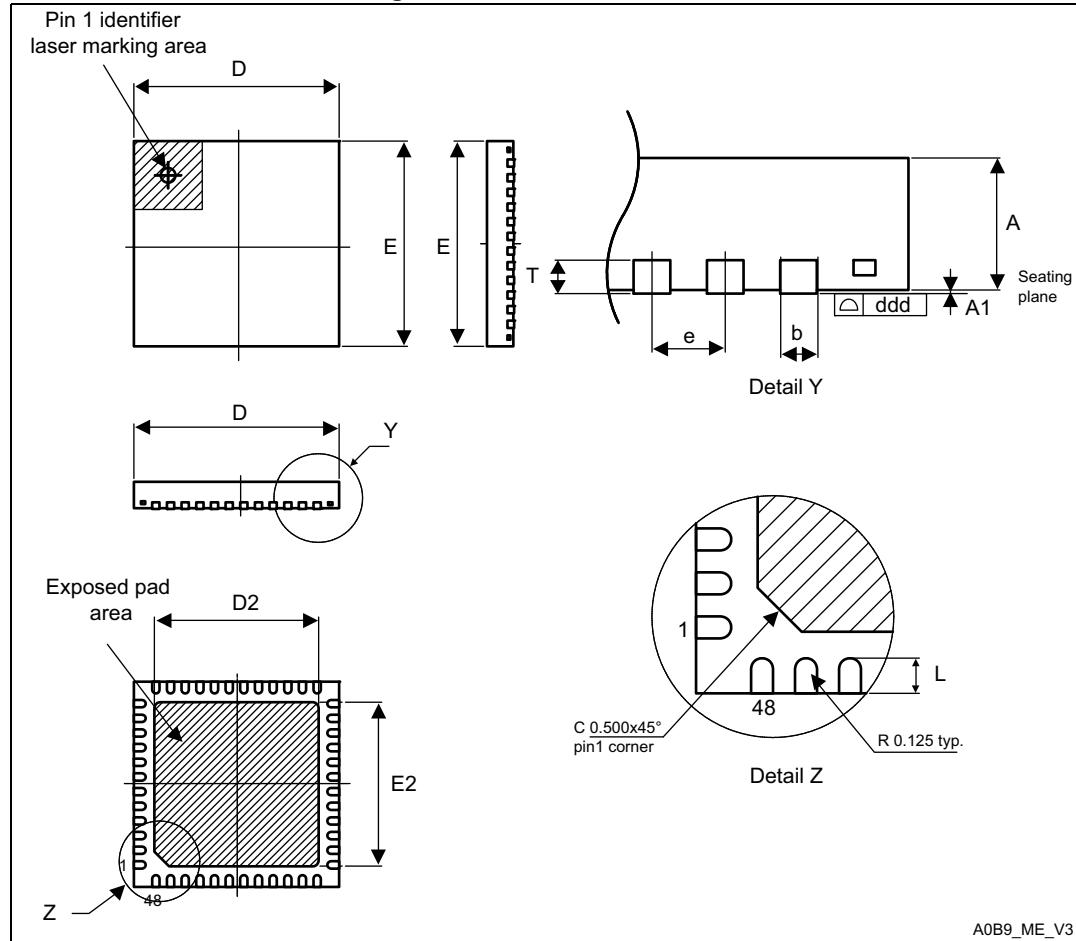


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.4 UFQFPN48 package information

UFQFPN48 is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 47. UFQFPN48 outline

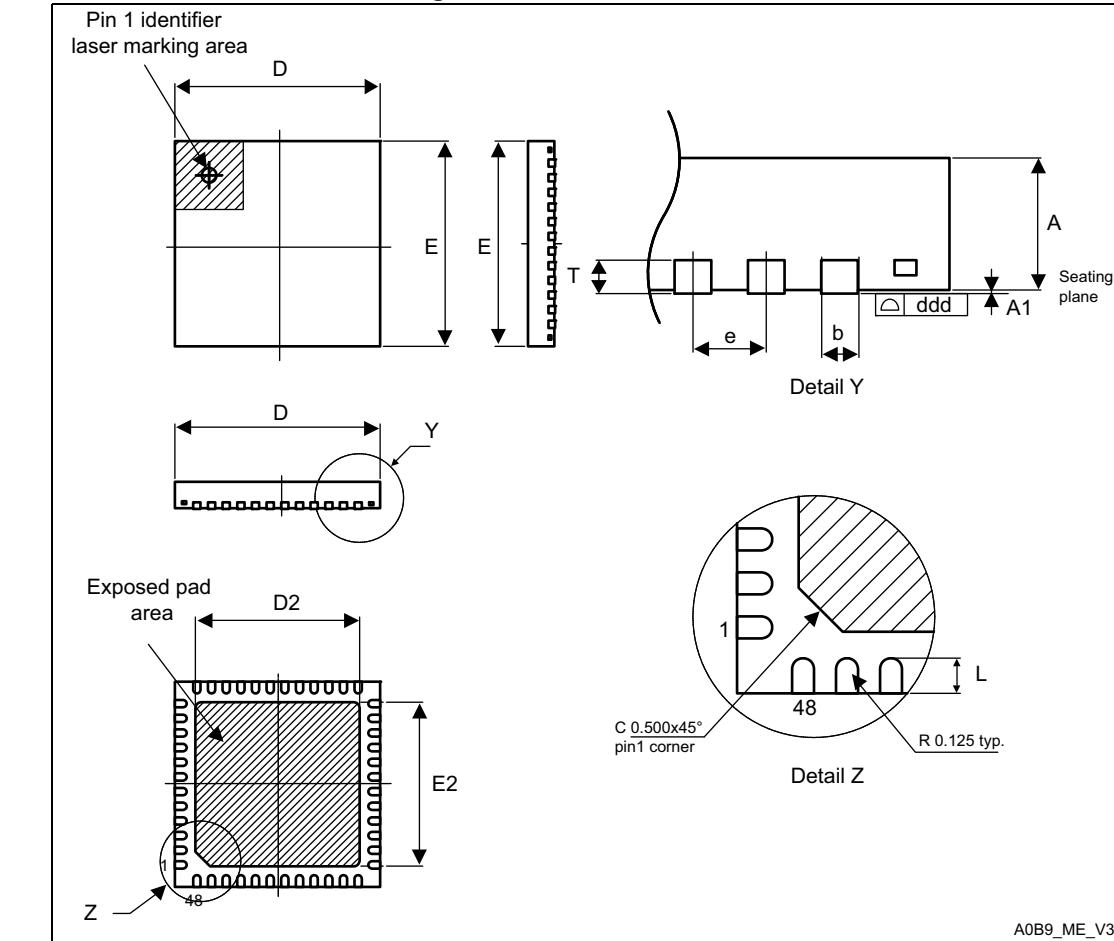


1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package, it must be electrically connected to the PCB ground.

7.4 UFQFPN48 包信息

UFQFPN48 是一个 48 脚、7 x 7 毫米、0.5 毫米距离的超薄细距离平板封装。

Figure 47. UFQFPN48 outline



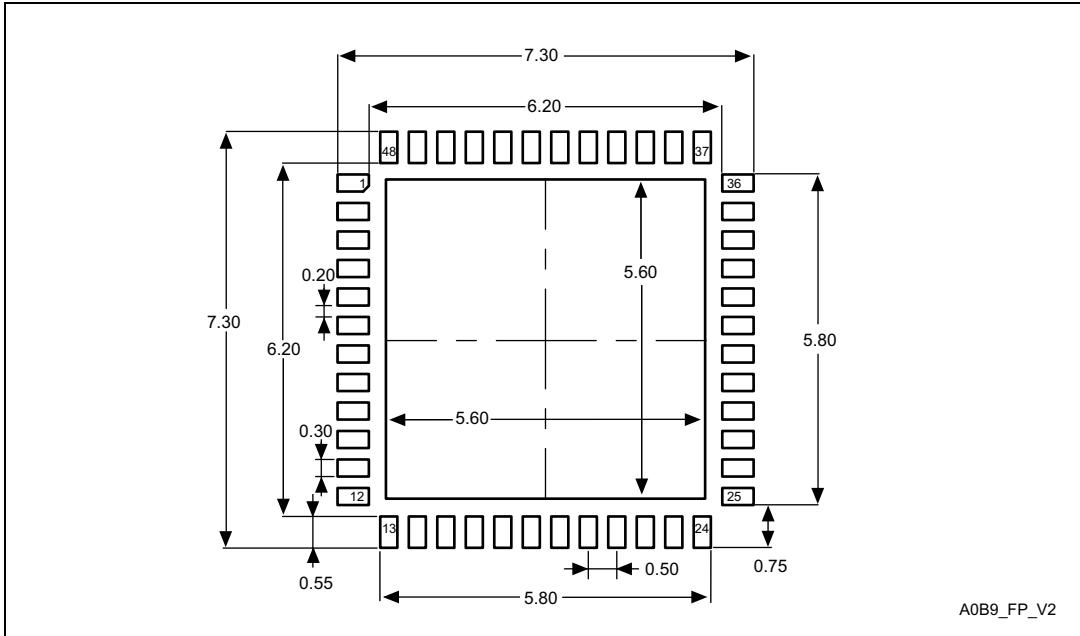
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package, it must be electrically connected to the PCB ground.

Table 105. UFQFPN48 mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 48. UFQFPN48 recommended footprint



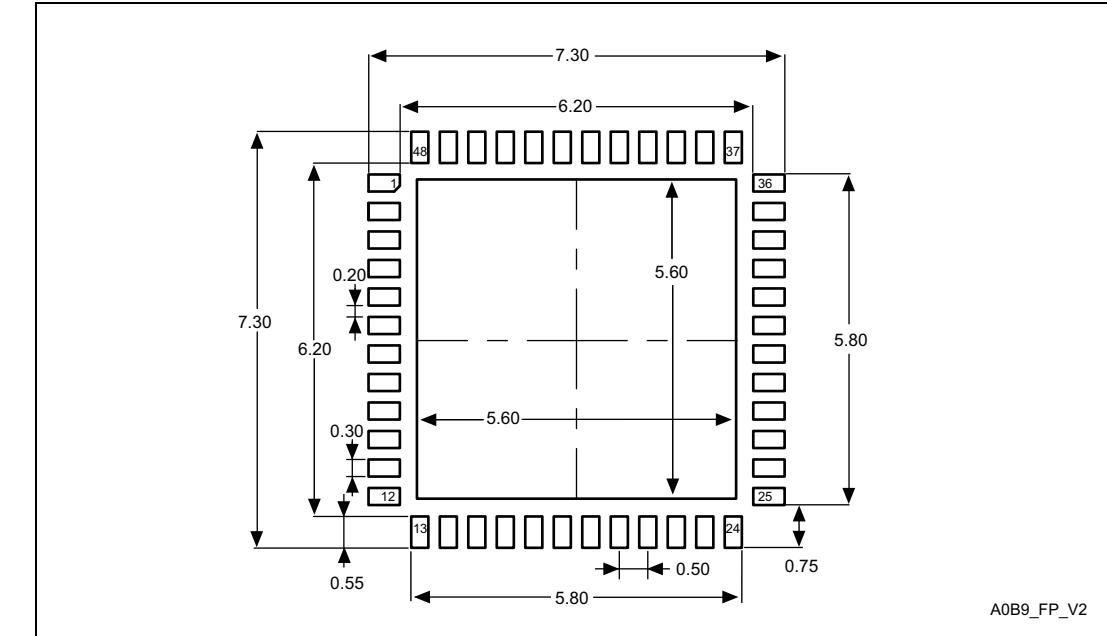
1. Dimensions are expressed in millimeters.

Table 105. UFQFPN48 mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 48. UFQFPN48 recommended footprint

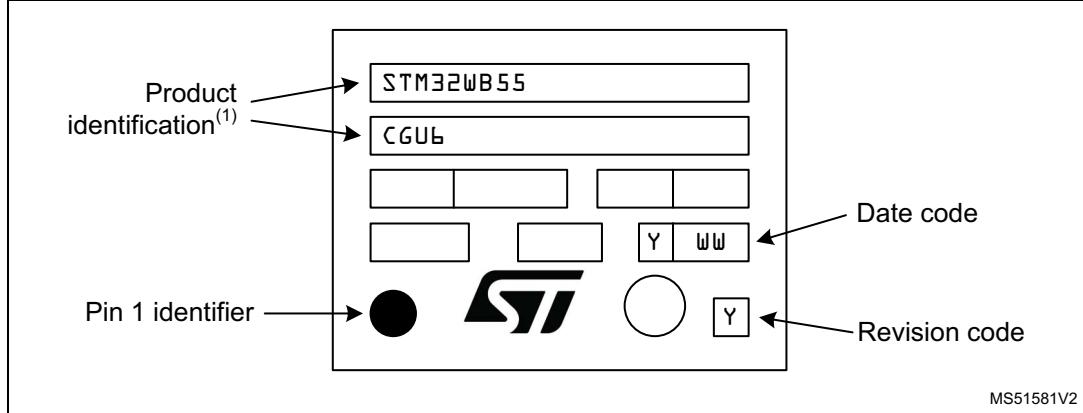


1. Dimensions are expressed in millimeters.

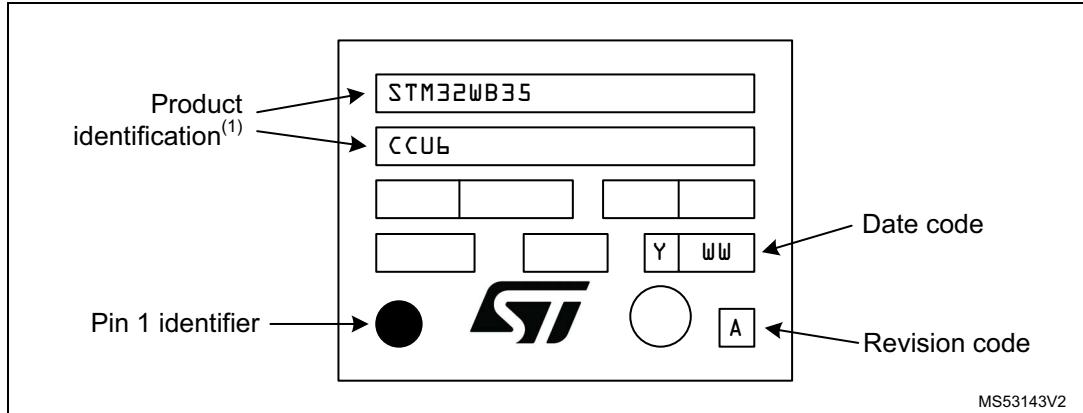
Device marking for UFQFPN48

[Figure 49](#) and [Figure 50](#) give examples of topside marking orientation versus pin 1 identifier location. The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 49. STM32WB55xx UFQFPN48 marking example (package top view)

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

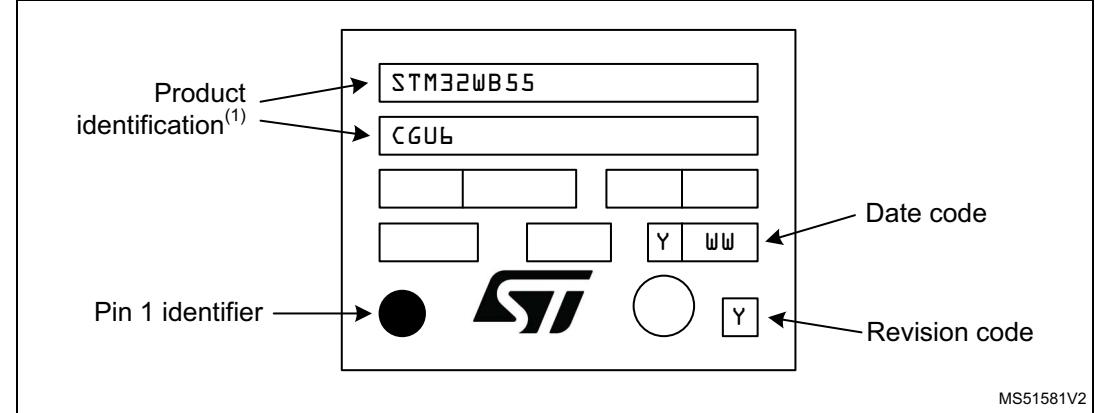
Figure 50. STM32WB35xx UFQFPN48 marking example (package top view)

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

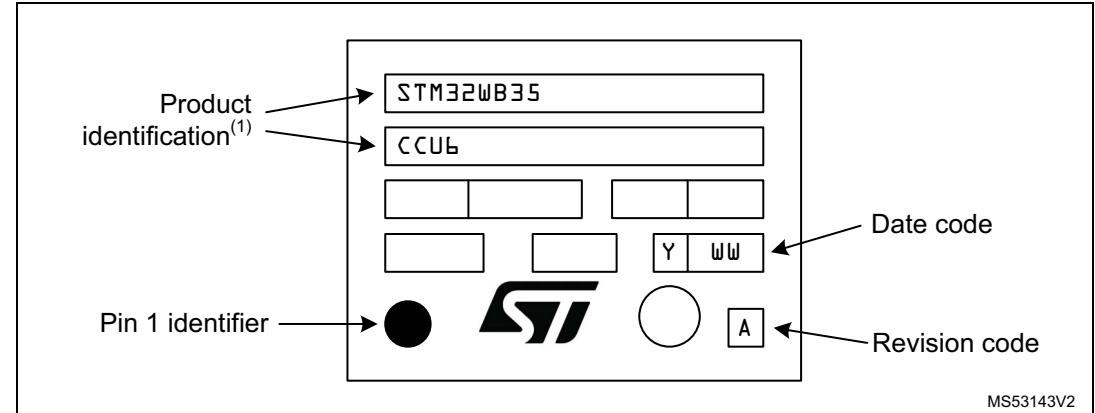
UFQFPN48 的设备标记

[图49](#)和[图50](#)给出正面标记方向与引脚1标识位置的示例。打印标记可能会因供应链而异。

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 49. STM32WB55xx UFQFPN48 marking example (package top view)

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

图50. STM32WB35xx UFQFPN48 标记示例 (包装顶视)

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.5 Thermal characteristics

The maximum chip junction temperature ($T_{J\max}$) must never exceed the values given in [Table 24: General operating conditions](#).

The maximum chip-junction temperature, T_J max, in degrees Celsius, can be calculated using the equation:

$$T_J \max = T_A \max + (P_D \max \times \Theta_{JA})$$

where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C / W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watt. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins:

- $P_{I/O}$ max = $\sum (V_{OL} \times I_{OL}) + \sum ((V_{DD} - V_{OH}) \times I_{OH})$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Note:
When the SMPS is used, a portion of the power consumption is dissipated into the external inductor, therefore reducing the chip power dissipation. This portion depends mainly on the inductor ESR characteristics.

Note:
As the radiated RF power is quite low (< 4 mW), it is not necessary to remove it from the chip power consumption.

Note:
RF characteristics (such as sensitivity, Tx power, consumption) are provided up to 85 °C.

Table 106. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient UFQFPN48 - 7 mm x 7 mm	24.9	°C/W
	Thermal resistance junction-ambient VFQFPN68 - 8 mm x 8 mm	47.0	
	Thermal resistance junction-ambient WLCSP100 - 0.4 mm pitch	35.8	
	Thermal resistance junction-ambient UFBGA129 - 0.5 mm pitch	41.5	
Θ_{JB}	Thermal resistance junction-board UFQFPN48 - 7 mm x 7 mm	13.0	°C/W
	Thermal resistance junction-board VFQFPN68 - 8 mm x 8 mm	36.1	
	Thermal resistance junction-board WLCSP100 - 0.4 mm pitch	N/A	
	Thermal resistance junction-board UFBGA129 - 0.5 mm pitch	16.2	

7.5 Thermal characteristics

最大芯片焊盘温度($T_{J\max}$) 必须不得超过表 24: 通用运行条件。

STM32WB55xx STM32WB35xx最大芯片接合温度, T_J max, 以摄氏度为单位, 可以通过方程进行计算:

$$T_J \max = T_A \max + (P_D \max \times \Theta_{JA})$$

在:

- T_A max 是在 ° 摄氏度下的最大环境温度, • Θ_{JA} 是包装焊盘到环境热阻, 单位为 ° 摄氏度/瓦。• P_D max 是 P_{INT} max 和 $P_{I/O}$ max 的总和。 $(P_D$ max = P_{INT} max + $P_{I/O}$ max),• P_{INT} max 是 IDD 和 VDD 的乘积, 以瓦为单位表示。这是最大芯片内部功率。

$P_{I/O}$ max 表示输出引脚的最大功率散失:

- $P_{I/O}$ max = $\sum (V_{OL} \times I_{OL}) + \sum ((V_{DD} - V_{OH}) \times I_{OH})$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

When the SMPS is used, a portion of the power consumption is dissipated into the external inductor, therefore reducing the chip power dissipation. This portion depends mainly on the inductor ESR characteristics.

Note:
As the radiated RF power is quite low (< 4 mW), it is not necessary to remove it from the chip power consumption.

Note:
无线电特性 (, 例如灵敏度、发射功率、消耗), 在高达 85 ° 摄氏度时提供。

Table 106. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient UFQFPN48 - 7 mm x 7 mm	24.9	°C/W
	Thermal resistance junction-ambient VFQFPN68 - 8 mm x 8 mm	47.0	
	Thermal resistance junction-ambient WLCSP100 - 0.4 mm pitch	35.8	
	Thermal resistance junction-ambient UFBGA129 - 0.5 mm pitch	41.5	
Θ_{JB}	Thermal resistance junction-board UFQFPN48 - 7 mm x 7 mm	13.0	°C/W
	Thermal resistance junction-board VFQFPN68 - 8 mm x 8 mm	36.1	
	Thermal resistance junction-board WLCSP100 - 0.4 mm pitch	N/A	
	Thermal resistance junction-board UFBGA129 - 0.5 mm pitch	16.2	

Table 106. Package thermal characteristics (continued)

Symbol	Parameter	Value	Unit
Θ_{JC}	Thermal resistance junction-case UFQFPN48 - 7 mm x 7 mm	1.3	°C/W
	Thermal resistance junction-case VFQFPN68 - 8 mm x 8 mm	13.7	
	Thermal resistance junction-case WLCSP100 - 0.4 mm pitch	N/A	
	Thermal resistance junction-case UFBGA129 - 0.5 mm pitch	34.9	

7.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Section 8](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the device at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range is best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_A max = 82 °C (measured according to JESD51-2), I_{DD} max = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL} = 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL} = 1.3 V

$$P_{INT} \text{ max} = 50 \text{ mA} \times 3.5 \text{ V} = 175 \text{ mW}$$

$$P_{IO} \text{ max} = 20 \times 8 \text{ mA} \times 0.4 \text{ V} + 8 \times 20 \text{ mA} \times 1.3 \text{ V} = 272 \text{ mW}$$

This gives: P_{INT} max = 175 mW and P_{IO} max = 272 mW

$$P_D \text{ max} = 175 + 272 = 447 \text{ mW}$$

Using the values obtained in [Table 106](#) T_J max is calculated as follows:

- For VFQFPN68, 47 °C / W

$$T_J \text{ max} = 82 \text{ °C} + (47 \text{ °C / W} \times 447 \text{ mW}) = 82 \text{ °C} + 21 \text{ °C} = 103 \text{ °C}$$

This is within the range of the suffix 6 version parts ($-40 < T_J < 105$ °C), see [Section 8](#).

In this case, parts must be ordered at least with the temperature range suffix 6.

Table 106. 包装热特性 (继续)

Symbol	Parameter	Value	Unit
Θ_{JC}	Thermal resistance junction-case UFQFPN48 - 7 mm x 7 mm	1.3	°C/W
	Thermal resistance junction-case VFQFPN68 - 8 mm x 8 mm	13.7	
	Thermal resistance junction-case WLCSP100 - 0.4 mm pitch	N/A	
	Thermal resistance junction-case UFBGA129 - 0.5 mm pitch	34.9	

7.5.1 参考文献

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Section 8](#).

每个温度范围后缀对应于在最大散热时的特定保证的环境温度，以及特定的最大接合温度。

As applications do not commonly use the device at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range is best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_A max = 82 °C (measured according to JESD51-2), I_{DD} max = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL} = 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL} = 1.3 V

$$P_{INT} \text{ max} = 50 \text{ mA} \times 3.5 \text{ V} = 175 \text{ mW}$$

$$P_{IO} \text{ max} = 20 \times 8 \text{ mA} \times 0.4 \text{ V} + 8 \times 20 \text{ mA} \times 1.3 \text{ V} = 272 \text{ mW}$$

This gives: P_{INT} max = 175 mW and P_{IO} max = 272 mW

$$P_D \text{ max} = 175 + 272 = 447 \text{ mW}$$

Using the values obtained in [Table 106](#) T_J max is calculated as follows:

- 对于 VFQFPN68, 47 °C / W

$$\times 447 \text{ 毫瓦}) = 82 \text{ °C} + 21 \text{ °C} = 103 \text{ °C}$$

这在后缀 6 版本部件的范围内($-40 < T_J < 105$ °C), see 第 8 节.

在这种情况下, 零件必须至少以温度范围后缀 6 订购。

Note: With this given P_D max user can find the T_A max allowed for a given device temperature range (order code suffix 7).

$$\text{Suffix 7: } T_A \text{ max} = T_J \text{ max} - (47^\circ\text{C} / W \times 447 \text{ mW}) = 125^\circ\text{C} - 21^\circ\text{C} = 103^\circ\text{C}$$

Example 2: High-temperature application

Using the same rules, it is possible to address applications running at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_A max = 100 °C (measured according to JESD51-2), I_{DD} max = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL} = 0.4 V

$$P_{INT} \text{ max} = 50 \text{ mA} \times 3.5 \text{ V} = 175 \text{ mW}$$

$$P_{IO} \text{ max} = 20 \times 8 \text{ mA} \times 0.4 \text{ V} = 64 \text{ mW}$$

This gives: P_{INTmax} = 175 mW and P_{IO} max = 64 mW

$$P_D \text{ max} = 175 + 64 = 239 \text{ mW}$$

Thus: P_D max = 239 mW

Using the values obtained in [Table 106](#) T_J max is calculated as follows:

- For UFQFPN48, 24.9 °C / W

$$T_J \text{ max} = 100^\circ\text{C} + (24.9^\circ\text{C} / W \times 239 \text{ mW}) = 100^\circ\text{C} + 6^\circ\text{C} = 106^\circ\text{C}$$

This is above the range of the suffix 6 version parts ($-40 < T_J < 105$ °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see [Section 8](#)), unless user reduces the power dissipation to be able to use suffix 6 parts.

Note: With this given 最大功率密度 user can find the T_A max allowed for a given device temperature range (order code suffix 7).

$$\text{Suffix 7: } T_A \text{ max} = T_J \text{ max} - (47^\circ\text{C} / W \times 447 \text{ mW}) = 125^\circ\text{C} - 21^\circ\text{C} = 103^\circ\text{C}$$

Example 2: High-temperature application

Using the same rules, it is possible to address applications running at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

STM32WB55xx STM32WB35xx最大环境温度TA max = 100 °C (按照JESD51-2)测量，最大输入电流IDD max = 50 mA, VDD = 3.5 V, 最多20个输入/输出在输出低电平时同时使用, IOL = 8 mA, VOL = 0.4 V PINT max = 50 mA × 3.5 V = 175 mW PIO max = 20 × 8 mA × 0.4 V = 64 mW 这给出: PINTmax = 175 mW 和 PIO max = 64 mW 最大功率密度PD max = 175 + 64 = 239 mW

Thus: P_D max = 239 mW

Using the values obtained in [Table 106](#) T_J max is calculated as follows:

- For UFQFPN48, 24.9 °C / W

$$T_J \text{ max} = 100^\circ\text{C} + (24.9^\circ\text{C} / W \times 239 \text{ mW}) = 100^\circ\text{C} + 6^\circ\text{C} = 106^\circ\text{C}$$

This is above the range of the suffix 6 version parts ($-40 < T_J < 105$ °C).

在这种情况下, 零件必须至少以温度范围后缀 6 订购。7 (参见第8节, 除非用户降低功率损失, 以便可以使用后缀 6 的零件。

8 Ordering information

Example:

STM32 WB 55 V G V 6 A TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

WB = Wireless Bluetooth®

Device subfamily

55 = Die 5, full set of features

35 = Die 3, full set of features⁽¹⁾**Pin count**

C = 48 pins

R = 68 pins

V = 100 or 129 pins

Flash memory size

C = 256 Kbytes

E = 512 Kbytes

Y⁽²⁾ = 640 Kbytes

G = 1 Mbyte

Package

U = UFQFPN48 7 x 7 mm

V = VFQFPN68 8 x 8 mm

Y = WLCSP100 0.4 mm pitch

Q = UFBGA129 0.5 mm pitch

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)

7 = Industrial temperature range, -40 to 105 °C (125 °C junction)

Identification code

A = Proprietary identification code

blank = Non-proprietary identification code

Packing

TR = tape and reel

xxx = programmed parts

1. STM32WB35xx only available with 48-pin UFQFPN48 package, 256 or 512 Kbytes Flash memory.

2. Only STM32WB55VY, WLCSP100 package, temperature range -40 to 85 °C (105 °C junction).

8 Ordering information

Example:

STM32 WB 55 V G V 6 A TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

WB = Wireless Bluetooth®

Device subfamily

55 = Die 5, full set of features

35 = Die 3, full set of features⁽¹⁾**Pin count**

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Flash memory size

C = 256 Kbytes

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Package

U = UFQFPN48 7 x 7 mm

V = VFQFPN68 8 x 8 mm

Y = WLCSP100 0.4 mm pitch

Q = UFBGA129 0.5 mm pitch

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)

7 = Industrial temperature range, -40 to 105 °C (125 °C junction)

Identification code

A = Proprietary identification code

blank = Non-proprietary identification code

Packing

TR = tape and reel

xxx = programmed parts

1. STM32WB35xx only available with 48-pin UFQFPN48 package, 256 or 512 Kbytes Flash memory.

2. Only STM32WB55VY, WLCSP100 package, temperature range -40 to 85 °C (105 °C junction).

9 Revision history

Table 107. Document revision history

Date	Revision	Changes
25-Jul-2017	1	Initial release.
04-Apr-2018	2	<p>Updated document title, Features, Section 1: Introduction, Section 2: Description, Section 3.1: Architecture, Section 3.3.2: Memory protection unit, Section 3.3.3: Embedded Flash memory, Section 3.4: Security and safety, Section 3.6: RF subsystem, Section 3.6.1: RF front-end block diagram, Section 3.6.2: BLE general description, Section 3.7.1: Power supply distribution, Section 3.7.2: Power supply schemes, Section 3.7.4: Power supply supervisor, Section 3.10: Clocks and startup, Section 3.14: Analog to digital converter (ADC), Section 3.19: True random number generator (RNG), Section 5: Memory mapping, Section 6.3.25: SMPS step-down converter characteristics and Section 7.5.2: Selecting the product temperature range.</p> <p>Updated Table 2: STM32WB55xx devices features and peripheral counts, Table 6: Power supply typical components, Table 7: Features over all modes, Table 8: STM32WB55xx modes overview, Table 13: Timer features, Table 15: Legend/abbreviations used in the pinout table, Table 16: STM32WB55xx pin and ball definitions, Table 17: Alternate functions, Table 23: RF transmitter BLE characteristics, Table 26: RF receiver BLE characteristics (1 Mbps) and added footnote to it, Table 28: RF BLE power consumption for VDD = 3.3 V, Table 31: RF 802.15.4 power consumption for VDD = 3.3 V, Table 37: Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF), VDD= 3.3 V, Table 38: Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1, VDD = 3.3 V, Table 40: Current consumption in Low-power sleep modes, Flash memory in Power down, Table 41: Current consumption in Stop 2 mode, Table 42: Current consumption in Stop 1 mode, Table 43: Current consumption in Stop 0 mode, Table 44: Current consumption in Standby mode, Table 45: Current consumption in Shutdown mode, Table 48: Peripheral current consumption, Table 104: Package thermal characteristics and Table 97: STM32WB55xx ordering information scheme.</p> <p>Added Table 47: Current under Reset condition.</p> <p>Updated Figure 1: STM32WB55xx block diagram, Figure 2: STM32WB55xx RF front-end block diagram, Figure 4: Power distribution, Figure 6: Power supply overview, Figure 7: Clock tree, Figure 8: STM32WB55Cx UFQFPN48 pinout⁽¹⁾⁽²⁾, Figure 9: STM32WB55Rx VFQFPN68 pinout⁽¹⁾⁽²⁾, Figure 10: STM32WB55Vx WLCSP100 ballout⁽¹⁾ and Figure 14: Power supply scheme (all packages except UFBGA129).</p>

9 修订历史

表107. 文档修订历史

Date	Revision	Changes
25-Jul-2017	1	Initial release.
04-Apr-2018	2	<p>Updated document title, Features, Section 1: Introduction, Section 2: Description, Section 3.1: Architecture, Section 3.3.2: Memory protection unit, Section 3.3.3: Embedded Flash memory, Section 3.4: Security and safety, Section 3.6: RF subsystem, Section 3.6.1: RF front-end block diagram, Section 3.6.2: BLE general description, Section 3.7.1: Power supply distribution, Section 3.7.2: Power supply schemes, Section 3.7.4: Power supply supervisor, Section 3.10: Clocks and startup, Section 3.14: Analog to digital converter (ADC), Section 3.19: True random number generator (RNG), Section 5: Memory mapping, Section 6.3.25: SMPS step-down converter characteristics and Section 7.5.2: Selecting the product temperature range.</p> <p>Updated Table 2: STM32WB55xx devices features and peripheral counts, Table 6: Power supply typical components, Table 7: Features over all modes, Table 8: STM32WB55xx modes overview, Table 13: Timer features, Table 15: Legend/abbreviations used in the pinout table, Table 16: STM32WB55xx pin and ball definitions, Table 17: Alternate functions, Table 23: RF transmitter BLE characteristics, Table 26: RF receiver BLE characteristics (1 Mbps) and added footnote to it, Table 28: RF BLE power consumption for VDD = 3.3 V, Table 31: RF 802.15.4 power consumption for VDD = 3.3 V, Table 37: Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF), VDD= 3.3 V, Table 38: Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1, VDD = 3.3 V, Table 40: Current consumption in Low-power sleep modes, Flash memory in Power down, Table 41: Current consumption in Stop 2 mode, Table 42: Current consumption in Stop 1 mode, Table 43: Current consumption in Stop 0 mode, Table 44: Current consumption in Standby mode, Table 45: Current consumption in Shutdown mode, Table 48: Peripheral current consumption, Table 104: Package thermal characteristics and Table 97: STM32WB55xx ordering information scheme.</p> <p>Added Table 47: Current under Reset condition.</p> <p>Updated Figure 1: STM32WB55xx block diagram, Figure 2: STM32WB55xx RF front-end block diagram, Figure 4: Power distribution, Figure 6: Power supply overview, Figure 7: Clock tree, Figure 8: STM32WB55Cx UFQFPN48 pinout⁽¹⁾⁽²⁾, Figure 9: STM32WB55Rx VFQFPN68 pinout⁽¹⁾⁽²⁾, Figure 10: STM32WB55Vx WLCSP100 ballout⁽¹⁾ and Figure 14: Power supply scheme (all packages except UFBGA129).</p>

Table 107. Document revision history (continued)

Date	Revision	Changes
08-Oct-2018	3	<p>Changed document classification to Public.</p> <p>Updated <i>Features</i>, <i>Section 3.6.2: BLE general description</i>, <i>Section 3.7.2: Power supply schemes</i>, <i>Section 3.7.3: Linear voltage regulator</i>, <i>Section 3.10: Clocks and startup</i>, <i>Section 6.3.10: External clock source characteristics</i>, <i>Section 6.3.20: Analog-to-Digital converter characteristics</i>, <i>Section 6.3.29: Communication interfaces characteristics</i>, <i>Section 7.2: WLCSP100 package information</i> and <i>Section 7.5: Thermal characteristics</i>.</p> <p>Replaced V_{DDIOx} with V_{DD} throughout the whole document.</p> <p>Updated <i>Table 5: Typical external components</i>, footnote 2 of <i>Table 7: Features over all modes</i>, <i>Table 8: STM32WB55xx modes overview</i> and its footnote 5, <i>Table 12: Internal voltage reference calibration values</i>, <i>Table 16: STM32WB55xx pin and ball definitions</i> and its footnote 6, <i>Table 17: Alternate functions</i>, <i>Table 20: Thermal characteristics</i>, <i>Table 21: Main performance at VDD = 3.3 V</i>, <i>Table 22: General operating conditions</i>, <i>Table 23: RF transmitter BLE characteristics</i> and its footnote, <i>Table 26: RF receiver BLE characteristics (1 Mbps)</i>, <i>Table 28: RF BLE power consumption for VDD = 3.3 V</i>, <i>Table 29: RF transmitter 802.15.4 characteristics</i> and its footnote 1, <i>Table 30: RF receiver 802.15.4 characteristics</i>, <i>Table 31: RF 802.15.4 power consumption for VDD = 3.3 V</i>, <i>Table 34: Embedded internal voltage reference</i>, <i>Table 35: Current consumption in Run and Low-power run modes</i>, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF), VDD = 3.3 V, <i>Table 36: Current consumption in Run and Low-power run modes</i>, code with data processing running from SRAM1, VDD = 3.3 V, <i>Table 37: Typical current consumption in Run and Low-power run modes, with different codes running from Flash</i>, ART enable (Cache ON Prefetch OFF), VDD = 3.3 V, <i>Table 38: Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1</i>, VDD = 3.3 V, <i>Table 39: Current consumption in Sleep and Low-power sleep modes</i>, Flash memory ON, <i>Table 40: Current consumption in Low-power sleep modes</i>, Flash memory in Power down, <i>Table 41: Current consumption in Stop 2 mode</i>, <i>Table 42: Current consumption in Stop 1 mode</i>, <i>Table 43: Current consumption in Stop 0 mode</i>, <i>Table 44: Current consumption in Standby mode</i>, <i>Table 45: Current consumption in Shutdown mode</i>, <i>Table 46: Current consumption in VBAT mode</i>, <i>Table 47: Current under Reset condition</i>, <i>Table 48: Peripheral current consumption</i>, <i>Table 49: Low-power mode wakeup timings</i>, <i>Table 50: Regulator modes transition times</i>, <i>Table 51: Wakeup time using LPUART</i>, <i>Table 53: HSE clock source requirements</i> and added footnote to it, <i>Table 61: LSI2 oscillator characteristics</i>, <i>Table 63: Flash memory characteristics</i>, <i>Table 65: EMS characteristics</i>, <i>Table 67: ESD absolute maximum ratings</i>, <i>Table 69: I/O current injection susceptibility</i>, <i>Table 70: I/O static characteristics</i> and its footnotes, <i>Table 71: Output voltage characteristics</i>, <i>Table 72: I/O AC characteristics</i> and its footnotes 1 and 2, <i>Table 73: NRST pin characteristics</i>, <i>Table 77: ADC accuracy - Limited test conditions 1</i>, <i>Table 78: ADC accuracy - Limited test conditions 2</i>, <i>Table 79: ADC accuracy - Limited test conditions 3</i>, <i>Table 80: ADC accuracy - Limited test conditions 4</i>, <i>Table 82: COMP characteristics</i>, <i>Table 90: I2C analog filter characteristics</i>, <i>Table 91: SPI characteristics</i>, <i>Table 92: Quad-SPI characteristics in SDR mode</i>, <i>Table 93: Quad-SPI characteristics in DDR mode</i> and <i>Table 94: SAI characteristics</i>.</p>

表107. 文档修订历史 (继续)

Date	Revision	Changes
08-Oct-2018	3	<p>Changed document classification to Public.</p> <p>Updated <i>Features</i>, <i>Section 3.6.2: BLE general description</i>, <i>Section 3.7.2: Power supply schemes</i>, <i>Section 3.7.3: Linear voltage regulator</i>, <i>Section 3.10: Clocks and startup</i>, <i>Section 6.3.10: External clock source characteristics</i>, <i>Section 6.3.20: Analog-to-Digital converter characteristics</i>, <i>Section 6.3.29: Communication interfaces characteristics</i>, <i>Section 7.2: WLCSP100 package information</i> and <i>Section 7.5: Thermal characteristics</i>.</p> <p>Replaced V_{DDIOx} with V_{DD} throughout the whole document.</p> <p>Updated <i>Table 5: Typical external components</i>, footnote 2 of <i>Table 7: Features over all modes</i>, <i>Table 8: STM32WB55xx modes overview</i> and its footnote 5, <i>Table 12: Internal voltage reference calibration values</i>, <i>Table 16: STM32WB55xx pin and ball definitions</i> and its footnote 6, <i>Table 17: Alternate functions</i>, <i>Table 20: Thermal characteristics</i>, <i>Table 21: Main performance at VDD = 3.3 V</i>, <i>Table 22: General operating conditions</i>, <i>Table 23: RF transmitter BLE characteristics</i> and its footnote, <i>Table 26: RF receiver BLE characteristics (1 Mbps)</i>, <i>Table 28: RF BLE power consumption for VDD = 3.3 V</i>, <i>Table 29: RF transmitter 802.15.4 characteristics</i> and its footnote 1, <i>Table 30: RF receiver 802.15.4 characteristics</i>, <i>Table 31: RF 802.15.4 power consumption for VDD = 3.3 V</i>, <i>Table 34: Embedded internal voltage reference</i>, <i>Table 35: Current consumption in Run and Low-power run modes, code with data processing running from Flash</i>, ART enable (Cache ON Prefetch OFF), VDD = 3.3 V, <i>Table 36: Current consumption in Run and Low-power run modes, code with data processing running from SRAM1</i>, VDD = 3.3 V, <i>Table 37: Typical current consumption in Run and Low-power run modes, with different codes running from Flash</i>, ART enable (Cache ON Prefetch OFF), VDD = 3.3 V, <i>Table 38: Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1</i>, VDD = 3.3 V, <i>Table 39: Current consumption in Sleep and Low-power sleep modes</i>, Flash memory ON, <i>Table 40: Current consumption in Low-power sleep modes</i>, Flash memory in Power down, <i>Table 41: Current consumption in Stop 2 mode</i>, <i>Table 42: Current consumption in Stop 1 mode</i>, <i>Table 43: Current consumption in Stop 0 mode</i>, <i>Table 44: Current consumption in Standby mode</i>, <i>Table 45: Current consumption in Shutdown mode</i>, <i>Table 46: Current consumption in VBAT mode</i>, <i>Table 47: Current under Reset condition</i>, <i>Table 48: Peripheral current consumption</i>, <i>Table 49: Low-power mode wakeup timings</i>, <i>Table 50: Regulator modes transition times</i>, <i>Table 51: Wakeup time using LPUART</i>, <i>Table 53: HSE clock source requirements</i> and added footnote to it, <i>Table 61: LSI2 oscillator characteristics</i>, <i>Table 63: Flash memory characteristics</i>, <i>Table 65: EMS characteristics</i>, <i>Table 67: ESD absolute maximum ratings</i>, <i>Table 69: I/O current injection susceptibility</i>, <i>Table 70: I/O static characteristics</i> and its footnotes, <i>Table 71: Output voltage characteristics</i>, <i>Table 72: I/O AC characteristics</i> and its footnotes 1 and 2, <i>Table 73: NRST pin characteristics</i>, <i>Table 77: ADC accuracy - Limited test conditions 1</i>, <i>Table 78: ADC accuracy - Limited test conditions 2</i>, <i>Table 79: ADC accuracy - Limited test conditions 3</i>, <i>Table 80: ADC accuracy - Limited test conditions 4</i>, <i>Table 82: COMP characteristics</i>, <i>Table 90: I2C analog filter characteristics</i>, <i>Table 91: SPI characteristics</i>, <i>Table 92: Quad-SPI characteristics in SDR mode</i>, <i>Table 93: Quad-SPI characteristics in DDR mode</i> and <i>Table 94: SAI characteristics</i>.</p>

Table 107. Document revision history (continued)

Date	Revision	Changes
08-Oct-2018	3 (cont'd)	<p>Updated Figure 2: STM32WB55xx RF front-end block diagram, Figure 14: Power supply scheme (all packages except UFBGA129), Figure 18: Typical energy detection (T = 27°C, VDD = 3.3 V) and Figure 25: I/O input characteristics.</p> <p>Added Figure 5: Power-up/down sequence, Figure 17: Typical link quality indicator code vs. Rx level and Figure 18: Typical energy detection (T = 27°C, VDD = 3.3 V).</p> <p>Added Table 24: RF transmitter BLE characteristics (1 Mbps), Table 25: RF transmitter BLE characteristics (2 Mbps), Table 27: RF receiver BLE characteristics (2 Mbps), Table 52: HSE crystal requirements and Table 89: Minimum I2CCLK frequency in all I2C modes.</p> <p>Added Device marking for UFQFPN48.</p> <p>Removed former Figure 22: I/O AC characteristics definition⁽¹⁾ and Figure 27: SMPS efficiency - VDDSMPS = 3.6 V.</p>
20-Feb-2019	4	<p>Updated document title.</p> <p>Product status moved to Production data.</p> <p>Introduced BGA129 package, hence updated image on cover page, Table 16: STM32WB55xx pin and ball definitions and Section 8: Ordering information, and added Figure 11: STM32WB55Vx UFBGA129 ballout⁽¹⁾ and Section 7.1: UFBGA129 package information.</p> <p>Updated Features, Section 3.3.4: Embedded SRAM, Section 3.17: Touch sensing controller (TSC) and Section 3.24: Low-power universal asynchronous receiver transmitter (LPUART).</p> <p>Added Section 6.3.28: Clock recovery system (CRS).</p> <p>Added Table 76: ADC sampling time.</p> <p>Removed former Table 75: Maximum ADC RAIN and Table 84: SMPS step-down converter characteristics.</p> <p>Updated captions of figures 8, 9 and 10.</p> <p>Updated Figure 43: VFQFPN68 recommended footprint.</p>

表107. 文档修订历史 (continued)

Date	Revision	Changes
08-Oct-2018	3 (cont'd)	<p>Updated Figure 2: STM32WB55xx RF front-end block diagram, Figure 14: Power supply scheme (all packages except UFBGA129), Figure 18: Typical energy detection (T = 27°C, VDD = 3.3 V) and Figure 25: I/O input characteristics.</p> <p>Added Figure 5: Power-up/down sequence, Figure 17: Typical link quality indicator code vs. Rx level and Figure 18: Typical energy detection (T = 27°C, VDD = 3.3 V).</p> <p>Added Table 24: RF transmitter BLE characteristics (1 Mbps), Table 25: RF transmitter BLE characteristics (2 Mbps), Table 27: RF receiver BLE characteristics (2 Mbps), Table 52: HSE crystal requirements and Table 89: Minimum I2CCLK frequency in all I2C modes.</p> <p>Added Device marking for UFQFPN48.</p> <p>Removed former Figure 22: I/O AC characteristics definition⁽¹⁾ and Figure 27: SMPS efficiency - VDDSMPS = 3.6 V.</p>
20-Feb-2019	4	<p>Updated document title.</p> <p>Product status moved to Production data.</p> <p>Introduced BGA129 package, hence updated image on cover page, Table 16: STM32WB55xx pin and ball definitions and Section 8: Ordering information, and added Figure 11: STM32WB55Vx UFBGA129 ballout⁽¹⁾ and Section 7.1: UFBGA129 package information.</p> <p>Updated Features, Section 3.3.4: Embedded SRAM, Section 3.17: Touch sensing controller (TSC) and Section 3.24: Low-power universal asynchronous receiver transmitter (LPUART).</p> <p>Added Section 6.3.28: Clock recovery system (CRS).</p> <p>Added Table 76: ADC sampling time.</p> <p>Removed former Table 75: Maximum ADC RAIN and Table 84: SMPS step-down converter characteristics.</p> <p>Updated captions of figures 8, 9 and 10.</p> <p>Updated Figure 43: VFQFPN68 recommended footprint.</p>

Table 107. Document revision history (continued)

Date	Revision	Changes
20-Feb-2019	4 (cont'd)	Updated Table 2: STM32WB55xx devices features and peripheral counts , Table 8: STM32WB55xx modes overview and its footnotes, Table 21: Main performance at VDD = 3.3 V , Table 22: General operating conditions , Table 23: RF transmitter BLE characteristics , Table 24: RF transmitter BLE characteristics (1 Mbps) , Table 25: RF transmitter BLE characteristics (2 Mbps) , Table 26: RF receiver BLE characteristics (1 Mbps) , Table 27: RF receiver BLE characteristics (2 Mbps) , Table 28: RF BLE power consumption for VDD = 3.3 V , Table 29: RF transmitter 802.15.4 characteristics , Table 31: RF 802.15.4 power consumption for VDD = 3.3 V , Table 35: Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF), VDD = 3.3 V , Table 36: Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, VDD = 3.3 V , Table 37: Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF), VDD= 3.3 V , Table 38: Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1, VDD = 3.3 V , Table 39: Current consumption in Sleep and Low-power sleep modes, Flash memory ON , Table 40: Current consumption in Low-power sleep modes, Flash memory in Power down , Table 41: Current consumption in Stop 2 mode , Table 42: Current consumption in Stop 1 mode , Table 43: Current consumption in Stop 0 mode , Table 44: Current consumption in Standby mode , Table 45: Current consumption in Shutdown mode , Table 46: Current consumption in VBAT mode , Table 47: Current under Reset condition , Table 48: Peripheral current consumption and its footnotes , Table 49: Low-power mode wakeup timings , Table 50: Regulator modes transition times and its footnote 1 , Table 65: EMS characteristics , Table 66: EMI characteristics , Table 67: ESD absolute maximum ratings , Table 69: I/O current injection susceptibility , Table 75: ADC characteristics , Table 77: ADC accuracy - Limited test conditions 1 , Table 78: ADC accuracy - Limited test conditions 2 , Table 79: ADC accuracy - Limited test conditions 3 , Table 80: ADC accuracy - Limited test conditions 4 and Table 104: Package thermal characteristics .
04-Oct-2019	5	Updated Features, Section 2: Description , Section 6.1.6: Power supply scheme , Section 6.2: Absolute maximum ratings and Section 7.2: WLCSP100 package information . Updated Table 6: Power supply typical components , Table 7: Features over all modes , Table 11: Temperature sensor calibration values , Table 16: STM32WB55xx pin and ball definitions , Table 17: Alternate functions , Table 21: Main performance at VDD = 3.3 V , Table 26: RF receiver BLE characteristics (1 Mbps) , Table 34: Embedded internal voltage reference , Table 62: PLL, PLLSAI1 characteristics and Table 67: ESD absolute maximum ratings . Updated Figure 6: Power supply overview and Figure 33: Quad-SPI timing diagram - DDR mode . Added Figure 15: Power supply scheme (UFBGA129 package) and Figure 21: Low-speed external clock source AC timing diagram . Added Table 56: Low-speed external user clock characteristics – Bypass mode .

表107. 文档修订历史 (继续)

Date	Revision	Changes
20-Feb-2019	4 (cont'd)	Updated Table 2: STM32WB55xx devices features and peripheral counts , Table 8: STM32WB55xx modes overview and its footnotes, Table 21: Main performance at VDD = 3.3 V , Table 22: General operating conditions , Table 23: RF transmitter BLE characteristics , Table 24: RF transmitter BLE characteristics (1 Mbps) , Table 25: RF transmitter BLE characteristics (2 Mbps) , Table 26: RF receiver BLE characteristics (1 Mbps) , Table 27: RF receiver BLE characteristics (2 Mbps) , Table 28: RF BLE power consumption for VDD = 3.3 V , Table 29: RF transmitter 802.15.4 characteristics , Table 31: RF 802.15.4 power consumption for VDD = 3.3 V , Table 35: Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF), VDD = 3.3 V , Table 36: Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, VDD = 3.3 V , Table 37: Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF), VDD= 3.3 V , Table 38: Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1, VDD = 3.3 V , Table 39: Current consumption in Sleep and Low-power sleep modes, Flash memory ON , Table 40: Current consumption in Low-power sleep modes, Flash memory in Power down , Table 41: Current consumption in Stop 2 mode , Table 42: Current consumption in Stop 1 mode , Table 43: Current consumption in Stop 0 mode , Table 44: Current consumption in Standby mode , Table 45: Current consumption in Shutdown mode , Table 46: Current consumption in VBAT mode , Table 47: Current under Reset condition , Table 48: Peripheral current consumption and its footnotes , Table 49: Low-power mode wakeup timings , Table 50: Regulator modes transition times and its footnote 1 , Table 65: EMS characteristics , Table 66: EMI characteristics , Table 67: ESD absolute maximum ratings , Table 69: I/O current injection susceptibility , Table 75: ADC characteristics , Table 77: ADC accuracy - Limited test conditions 1 , Table 78: ADC accuracy - Limited test conditions 2 , Table 79: ADC accuracy - Limited test conditions 3 , Table 80: ADC accuracy - Limited test conditions 4 and Table 104: Package thermal characteristics .
04-Oct-2019	5	Updated Features, Section 2: Description , Section 6.1.6: Power supply scheme , Section 6.2: Absolute maximum ratings and Section 7.2: WLCSP100 package information . Updated Table 6: Power supply typical components , Table 7: Features over all modes , Table 11: Temperature sensor calibration values , Table 16: STM32WB55xx pin and ball definitions , Table 17: Alternate functions , Table 21: Main performance at VDD = 3.3 V , Table 26: RF receiver BLE characteristics (1 Mbps) , Table 34: Embedded internal voltage reference , Table 62: PLL, PLLSAI1 characteristics and Table 67: ESD absolute maximum ratings . Updated Figure 6: Power supply overview and Figure 33: Quad-SPI timing diagram - DDR mode . Added Figure 15: Power supply scheme (UFBGA129 package) and Figure 21: Low-speed external clock source AC timing diagram . Added Table 56: Low-speed external user clock characteristics – Bypass mode .

Table 107. Document revision history (continued)

Date	Revision	Changes
19-Feb-2020	6	<p>Updated Features, Section 2: Description, I/O system current consumption, Section 3.17: Touch sensing controller (TSC), Section 7.1: UFBGA129 package information, Section 7.2: WLCSP100 package information, Section 7.3: VFQFPN68 package information, Section 7.4: UFQFPN48 package information, Section 7.5: Thermal characteristics and Section 8: Ordering information.</p> <p>Added JTAG/SWD interface characteristics, Device marking for UFBGA129, Device marking for WLCSP100 and Device marking for VFQFPN68.</p> <p>Updated Table 2: STM32WB55xx devices features and peripheral counts, Table 7: Features over all modes, Table 16: STM32WB55xx pin and ball definitions, Table 17: Alternate functions, Table 18: Voltage characteristics, Table 22: General operating conditions, Table 26: RF receiver BLE characteristics (1 Mbps), Table 27: RF receiver BLE characteristics (2 Mbps), Table 30: RF receiver 802.15.4 characteristics, Table 47: Current under Reset condition, Table 61: LSI2 oscillator characteristics and Table 104: Package thermal characteristics.</p> <p>Added footnote 5 to Table 15: Legend/abbreviations used in the pinout table.</p> <p>Updated Figure 2: STM32WB55xx RF front-end block diagram, Figure 6: Power supply overview, Figure 7: Clock tree, Figure 11: STM32WB55Vx UFBGA129 ballout⁽¹⁾, Figure 14: Power supply scheme (all packages except UFBGA129), Figure 36: UFBGA129 package outline and Figure 47: UFQFPN48 marking example (package top view).</p>
10-Apr-2020	7	<p>Updated Section 3.6.5: Typical RF application schematic and Section 6.3.10: External clock source characteristics.</p> <p>Updated Table 16: STM32WB55xx pin and ball definitions and Table 54: HSE crystal requirements.</p> <p>Updated Figure 11: STM32WB55Vx UFBGA129 ballout⁽¹⁾ and Figure 14: Power supply scheme (all packages except UFBGA129).</p> <p>Minor text edits across the whole document.</p>
17-Jun-2020	8	<p>Introduced STM32WB55VY.</p> <p>Updated Section 3.3.4: Embedded SRAM, Section 3.4: Security and safety, Section 3.14: Analog to digital converter (ADC), Section 6.3.10: External clock source characteristics and Section 8: Ordering information.</p> <p>Updated Table 1: Device summary, Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts, Table 26: RF transmitter BLE characteristics (1 Mbps), Table 27: RF transmitter BLE characteristics (2 Mbps), Table 65: Flash memory characteristics and Table 77: ADC characteristics.</p> <p>Updated Figure 10: STM32WB55Cx and STM32WB35Cx UFQFPN48 pinout⁽¹⁾⁽²⁾, Figure 11: STM32WB55Rx VFQFPN68 pinout⁽¹⁾⁽²⁾ and Figure 17: Power supply scheme (UFBGA129 and WLCSP100 packages).</p> <p>Updated footnote 5 of Table 15: Legend/abbreviations used in the pinout table and footnote 8 of Table 16: STM32WB55xx pin and ball definitions.</p> <p>Added footnote 3 to Table 16, footnote 2 to Figure 16, footnote 1 to Table 86 and footnotes to tables 23, 30 and 33.</p> <p>Added Table 55: HSE clock source requirements.</p>

表 107. 文档修订历史 (继续)

Date	Revision	Changes
19-Feb-2020	6	<p>Updated Features, Section 2: Description, I/O system current consumption, Section 3.17: Touch sensing controller (TSC), Section 7.1: UFBGA129 package information, Section 7.2: WLCSP100 package information, Section 7.3: VFQFPN68 package information, Section 7.4: UFQFPN48 package information, Section 7.5: Thermal characteristics and Section 8: Ordering information.</p> <p>Added JTAG/SWD interface characteristics, Device marking for UFBGA129, Device marking for WLCSP100 and Device marking for VFQFPN68.</p> <p>Updated Table 2: STM32WB55xx devices features and peripheral counts, Table 7: Features over all modes, Table 16: STM32WB55xx pin and ball definitions, Table 17: Alternate functions, Table 18: Voltage characteristics, Table 22: General operating conditions, Table 26: RF receiver BLE characteristics (1 Mbps), Table 27: RF receiver BLE characteristics (2 Mbps), Table 30: RF receiver 802.15.4 characteristics, Table 47: Current under Reset condition, Table 61: LSI2 oscillator characteristics and Table 104: Package thermal characteristics.</p> <p>Added footnote 5 to Table 15: Legend/abbreviations used in the pinout table.</p> <p>Updated Figure 2: STM32WB55xx RF front-end block diagram, Figure 6: Power supply overview, Figure 7: Clock tree, Figure 11: STM32WB55Vx UFBGA129 ballout⁽¹⁾, Figure 14: Power supply scheme (all packages except UFBGA129), Figure 36: UFBGA129 package outline and Figure 47: UFQFPN48 marking example (package top view).</p>
10-Apr-2020	7	<p>Updated Section 3.6.5: Typical RF application schematic and Section 6.3.10: External clock source characteristics.</p> <p>Updated Table 16: STM32WB55xx pin and ball definitions and Table 54: HSE crystal requirements.</p> <p>Updated Figure 11: STM32WB55Vx UFBGA129 ballout⁽¹⁾ and Figure 14: Power supply scheme (all packages except UFBGA129).</p> <p>Minor text edits across the whole document.</p>
17-Jun-2020	8	<p>Introduced STM32WB55VY.</p> <p>Updated Section 3.3.4: Embedded SRAM, Section 3.4: Security and safety, Section 3.14: Analog to digital converter (ADC), Section 6.3.10: External clock source characteristics and Section 8: Ordering information.</p> <p>Updated Table 1: Device summary, Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts, Table 26: RF transmitter BLE characteristics (1 Mbps), Table 27: RF transmitter BLE characteristics (2 Mbps), Table 65: Flash memory characteristics and Table 77: ADC characteristics.</p> <p>Updated Figure 10: STM32WB55Cx and STM32WB35Cx UFQFPN48 pinout⁽¹⁾⁽²⁾, Figure 11: STM32WB55Rx VFQFPN68 pinout⁽¹⁾⁽²⁾ and Figure 17: Power supply scheme (UFBGA129 and WLCSP100 packages).</p> <p>Updated footnote 5 of Table 15: Legend/abbreviations used in the pinout table and footnote 8 of Table 16: STM32WB55xx pin and ball definitions.</p> <p>Added footnote 3 to Table 16, footnote 2 to Figure 16, footnote 1 to Table 86 and footnotes to tables 23, 30 and 33.</p> <p>Added Table 55: HSE clock source requirements.</p>

Table 107. Document revision history (continued)

Date	Revision	Changes
02-Jul-2020	9	<p>Added STM32WB35xx devices.</p> <p>Updated Section 2: Description, Section 3.3.4: Embedded SRAM and Section 8: Ordering information.</p> <p>Updated Table 1: Device summary, Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts, Table 7: Features over all modes and Table 106: Package thermal characteristics.</p> <p>Added Table 17: STM32WB35xx pin and ball definitions and Table 19: Alternate functions (STM32WB35xx).</p> <p>Added Figure 2: STM32WB35xx block diagram, Figure 8: STM32WB35xx - Power supply overview and Figure 50: STM32WB35xx UFQFPN48 marking example (package top view),</p> <p>Updated Figure 1: STM32WB55xx block diagram, Figure 4: External components for the RF part, Figure 16: Power supply scheme (all packages except UFBGA129 and WLCSP100), Figure 17: Power supply scheme (UFBGA129 and WLCSP100 packages) and added footnote to Figure 9: Clock tree.</p> <p>Added footnote 1 to Table 8: STM32WB55xx and STM32WB35xx modes overview.</p>
23-Nov-2020	10	<p>Updated Features, Section 3.15: Voltage reference buffer (VREFBUF) and Section 3.28.2: Embedded Trace Macrocell™.</p> <p>Updated Table 9: STM32WB55xx and STM32WB35xx CPU1 peripherals interconnect matrix, Table 17: STM32WB35xx pin and ball definitions, Table 26: RF transmitter BLE characteristics (1 Mbps), Table 27: RF transmitter BLE characteristics (2 Mbps), Table 31: RF transmitter 802.15.4 characteristics, Table 50: Peripheral current consumption, Table 54: HSE crystal requirements, Table 55: HSE clock source requirements, footnote 2 of Table 57: Low-speed external user clock characteristics and Table 86: V_{BAT} monitoring characteristics.</p> <p>Added footnote 2 to Table 24, footnote 2 to Table 26 and footnote 2 to Table 27.</p> <p>Updated Figure 9: Clock tree and Figure 13: STM32WB55Vx UFBGA129 bailout⁽¹⁾.</p> <p>Minor text edits across the whole document.</p>
07-Apr-2021	11	<p>Updated document title, Features, Section 1: Introduction, Section 2: Description, Section 3.3.4: Embedded SRAM, Section 3.6: RF subsystem, Section 3.6.2: BLE general description and Section 6.1.2: Typical values, Section 6.3.10: External clock source characteristics.</p> <p>Updated Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts, Table 16: STM32WB55xx pin and ball definitions, Table 17: STM32WB35xx pin and ball definitions, Table 18: Alternate functions (STM32WB55xx), Table 19: Alternate functions (STM32WB35xx), Table 23: Main performance at VDD = 3.3 V, Table 50: Peripheral current consumption, Table 53: Wakeup time using USART/LPUART and Table 55: HSE clock source requirements.</p> <p>Updated Figure 3: STM32WB55xx and STM32WB35xx RF front-end block diagram, Figure 9: Clock tree, Figure 16: Power supply scheme (all packages except UFBGA129 and WLCSP100), Figure 17: Power supply scheme (UFBGA129 and WLCSP100 packages) and Figure 29: ADC accuracy characteristics.</p> <p>Removed former footnote 3 from Table 83: VREFBUF characteristics.</p>

Table 107. Document revision history (continued)

Date	Revision	Changes
02-Jul-2020	9	<p>Added STM32WB35xx devices.</p> <p>Updated Section 2: Description, Section 3.3.4: Embedded SRAM and Section 8: Ordering information.</p> <p>Updated Table 1: Device summary, Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts, Table 7: Features over all modes and Table 106: Package thermal characteristics.</p> <p>Added Table 17: STM32WB35xx pin and ball definitions and Table 19: Alternate functions (STM32WB35xx).</p> <p>Added Figure 2: STM32WB35xx block diagram, Figure 8: STM32WB35xx - Power supply overview and Figure 50: STM32WB35xx UFQFPN48 marking example (package top view),</p> <p>Updated Figure 1: STM32WB55xx block diagram, Figure 4: External components for the RF part, Figure 16: Power supply scheme (all packages except UFBGA129 and WLCSP100), Figure 17: Power supply scheme (UFBGA129 and WLCSP100 packages) and added footnote to Figure 9: Clock tree.</p> <p>Added footnote 1 to Table 8: STM32WB55xx and STM32WB35xx modes overview.</p>
23-Nov-2020	10	<p>Updated Features, Section 3.15: Voltage reference buffer (VREFBUF) and Section 3.28.2: Embedded Trace Macrocell™.</p> <p>Updated Table 9: STM32WB55xx and STM32WB35xx CPU1 peripherals interconnect matrix, Table 17: STM32WB35xx pin and ball definitions, Table 26: RF transmitter BLE characteristics (1 Mbps), Table 27: RF transmitter BLE characteristics (2 Mbps), Table 31: RF transmitter 802.15.4 characteristics, Table 50: Peripheral current consumption, Table 54: HSE crystal requirements, Table 55: HSE clock source requirements, footnote 2 of Table 57: Low-speed external user clock characteristics and Table 86: V_{BAT} monitoring characteristics.</p> <p>Added footnote 2 to Table 24, footnote 2 to Table 26 and footnote 2 to Table 27.</p> <p>Updated Figure 9: Clock tree and Figure 13: STM32WB55Vx UFBGA129 bailout⁽¹⁾.</p> <p>Minor text edits across the whole document.</p>
07-Apr-2021	11	<p>Updated document title, Features, Section 1: Introduction, Section 2: Description, Section 3.3.4: Embedded SRAM, Section 3.6: RF subsystem, Section 3.6.2: BLE general description and Section 6.1.2: Typical values, Section 6.3.10: External clock source characteristics.</p> <p>Updated Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts, Table 16: STM32WB55xx pin and ball definitions, Table 17: STM32WB35xx pin and ball definitions, Table 18: Alternate functions (STM32WB55xx), Table 19: Alternate functions (STM32WB35xx), Table 23: Main performance at VDD = 3.3 V, Table 50: Peripheral current consumption, Table 53: Wakeup time using USART/LPUART and Table 55: HSE clock source requirements.</p> <p>Updated Figure 3: STM32WB55xx and STM32WB35xx RF front-end block diagram, Figure 9: Clock tree, Figure 16: Power supply scheme (all packages except UFBGA129 and WLCSP100), Figure 17: Power supply scheme (UFBGA129 and WLCSP100 packages) and Figure 29: ADC accuracy characteristics.</p> <p>Removed former footnote 3 from Table 83: VREFBUF characteristics.</p>



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