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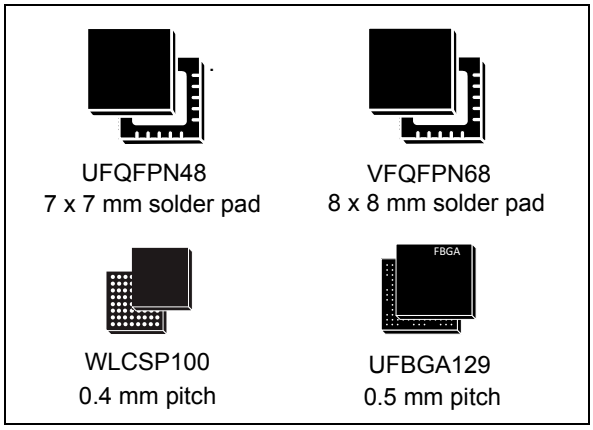
STM32WB55xx
STM32WB35xx

Multiprotocol wireless 32 4-bit MCU
® 5 2 802 15 4
Arm®-based Cortex®-M4 FPU, Bluetooth® 5.2 and 802.15.4 radio solution

数据手册 - 生产 数据

功能

- Include ST state-of-the-art patented technology
- 射频
  – 2.4 GHz– RF收发器支持蓝牙® 5.2规范，IEEE 802.15.4-2011 PHY和MAC，支持Thread和 Zigbee® 3.0– RX灵敏度：-96 dBm (蓝牙® 低功耗于1 Mbps), -100 dBm (802.15.4)– 可编程输出功率高达+6 dBm，步长1 dB– 集成平衡变压器以减少BOM– 支持2Mbps– 专门的Arm® 32-bit Cortex® M 0+ CPU用于实时射频层– 准确的RSSI用于启用功率控制– 适用于需要遵守射频规定的系统，例如ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15和ARIB STD-T66– 支持外部放大器– 可用集成被动设备(IPD)伴随芯片，用于优化匹配解决方案(MLPF-WB-01E3或MLPF-WB-02E3)超低功耗平台– 1.71到3.6 V电源– – 40 °C到85 / 105 °C温度范围– 13 nA关闭模式– 600 nA待机模式 + RTC + 32 KB RAM– 2.1 µA停止模式 + RTC + 256 KB RAM– 主动模式MCU: < 53 µA / MHz当RF和SMPS开启– 射频：接收4.5mA/传输0dBm 5.2mA
-



- 核心：Arm® 32-位 Cortex®-M4 CPU配 FPU，适应性实时加速器 (ART 加速器) 允许从闪存执行 0 等待状态，频率可达 64 MHz，MPU，80 DMIPS 和 DSP 指令
- Performance benchmark
  – 1.25 DMIPS/兆赫 (Drystone 2.1)– 219.48 CoreMark® (3.43 CoreMark/兆赫于 64 MHz)
- 能量基准– 303 ULPMark™ CP 分数
- 供电和复位管理
  – 高效集成 SMPS 降压转换器配备智能绕过模式– 超安全，低功耗 BOR (电压下降复位) 具有五个可选择的阈值– 超低功耗 POR/PDR– 可编程电压检测器 (PVD)– VBAT 模式配备 RTC 和 备份寄存器
- 时钟源
  – 32 兆赫 晶体 振荡器，集成 校准 电容器 (射频 和 CPU 时钟)– 32 kHz 晶体 振荡器 用于 RTC (LSE)– 内部 低功耗 32 kHz (±5%) RC (LSI1)– 内部 低功耗 32 kHz (稳定性±500 ppm) RC (LSI2)

– Internal multispeed 100 kHz to 48 MHz 振荡器, auto-trimmed by LSE (better than±0.25% 精度)– High speed internal 16 MHz factory trimmed RC (±1%)– 2x PLL for system clock, USB, SAI and ADC

- 内存

– Up to 1 MB 闪存内存 with sector protection (PCROP) against R/W operations, enabling radio stack and application– Up to 256 KB SRAM, including 64 KB with hardware parity check– 20x32-bit backup register– Boot loader supporting USART, SPI, I2C and USB interfaces– OTA (over the air) 蓝牙® 低功耗和 802.15.4 update– Quad SPI memory interface with XIP– 1 Kbyte (128 double words) OTP• Rich analog peripherals (down to 1.62 V)– 12-bit ADC 4.26 兆赫, up to 16-bit with hardware oversampling, 200 µA/Msps– 2 x ultra-low-power comparator– Accurate 2.5 V or 2.048 V reference voltage buffered output• System peripherals– Inter processor communication controller (IPCC) for communication with Bluetooth®低功耗和 802.15.4– HW semaphores for resources sharing between CPUs– 2x DMA controllers (7 x channels each)supporting ADC, SPI, I2C, USART, QSPI, SAI, AES, timers– 1x USART (ISO 7816, IrDA, SPI Master, Modbus and Smartcard mode)– 1x LPUART (low power)
– 2x SPI 32 Mbit/s– 2x I2C (SMBus/PMBus)
– 1x SAI (dual channel high quality audio)
– 1x USB 2.0 FS 设备，无晶体，BCD 和 LPM– Touch sensing controller, up to 18 sensors– LCD 8x40 with step-up converter– 1x 16-bit, four channels advanced timer– 2x 16-bit, two channels timer– 1x 32-bit, four channels timer– 2 x 16-bit ultra-low-power timer– 1x independent Systick– 1x independent watchdog– 1x window watchdog

- Security and ID
  - Secure firmware installation (SFI) for Bluetooth® Low Energy and 802.15.4 SW stack
  - 3x hardware encryption AES maximum 256-bit for the application, the Bluetooth® Low Energy and IEEE802.15.4
  - Customer key storage / key manager services
  - HW public key authority (PKA)
  - Cryptographic algorithms: RSA, Diffie-Helman, ECC over GF(p)
  - True random number generator (RNG)
  - Sector protection against R/W operation (PCROP)
  - CRC calculation unit
  - Die information: 96-bit unique ID
  - IEEE 64-bit unique ID. Possibility to derive 802.15.4 64-bit and Bluetooth® Low Energy 48-bit EUI
- Up to 72 fast I/Os, 70 of them 5 V-tolerant
- Development support
  - Serial wire debug (SWD), JTAG for the application processor
  - Application cross trigger with input / output
  - Embedded Trace Macrocell™ for application
- All packages are ECOPACK2 compliant

Table 1. Device summary

Reference	Part numbers
STM32WB55xx	STM32WB55CC, STM32WB55CE, STM32WB55CG, STM32WB55RC, STM32WB55RE, STM32WB55RG, STM32WB55VC, STM32WB55VE, STM32WB55VG, STM32WB55VY
STM32WB35xx	STM32WB35CC, STM32WB35CE

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1 Introduction

本文档提供了STM32WB55xx和STM32WB35xx微控制器的订购信息和机械设备特性，基于Arm® 核心(a).

此文档必须与参考手册同时阅读 (RM0434), 可以从 STMicroelectronics 网站获得 *www.st.com*.

有关设备 errata 信息，与数据手册和参考手册相比，请参考 STM32WB55xx 和 STM32WB35xx errata 表格 (ES0394), 可以从 STMicroelectronics 网站获得 *www.st.com*.

有关 Cortex-M4 和 Cortex-M0+ 核心的信息，请分别参考 Cortex-M4 技术参考手册和 Cortex-M0+ 技术参考手册，两者都可在 www.arm.com 网站上获得。

有关 802.15.4 的信息，请参考 IEEE 网站 (www.ieee.org).
有关 蓝牙 的信息，请参考 www.bluetooth.com。

a. Arm is a reArm Limited 的注册商标 (或其子公司) 在 th e US and/or elsewhere.

2 描述

STM32WB55xx 和 STM32WB35xx 多协议无线电超低功耗设备集成了一款强大且超低功耗的射频，符合 Bluetooth® 低功耗 SIG 规范 5.2 和 IEEE 802.15.4-2011。它们包含一个专用的 Arm® Cortex®-M0+ 用于执行所有实时低层操作。

这些设备设计用于极低功耗，基于高性能的 Arm® Cortex®-M4 32 RISC 核心，在频率最高可达 64 MHz 的情况下运行。此核心包含一个 Floating point 单元 (FPU) 单精度，支持所有 Arm® 单精度数据处理指令和数据类型。它还实现了完整的 DSP 指令集和内存保护单元 (MPU) ，以提高应用程序安全性。

增强的跨处理器通信由 IPCC 提供，具有六个双向通道。HSEM 提供硬件信号量，用于在两个处理器之间共享公共资源。

这些设备嵌入了高速内存 (最高可达 1 M字节的闪存内存用 STM32WB55xx，最高可达 512 K字节用 STM32WB35xx，最高可达 256 K字节的 SRAM 用 STM32WB55xx，96 K字节用 STM32WB35xx)，四线SPI闪存接口(可在所有封装中使用) ，以及广泛的增强输入/输出和外围设备。

内存和外围设备之间的直接数据传输，以及内存与内存之间的数据传输，由 DMAMUX 外围设备提供的完全灵活的通道映射支持，共有十四个 DMA 通道。

STM32WB55xx STM32WB35xx设备具有多种嵌入式闪存内存和SRAM的机制：读取保护、写入保护和专有代码读取保护。内存的一些部分可以为Cortex® -M0+ 独占访问进行保护。

两个 AES 加密引擎，PKA 和 随机数生成器，使得底层 MAC 和顶层密码学能够更有效地工作。客户密钥存储功能可用于保持密钥的安全。

这些设备提供一个快速的 12 位 ADC 和两个与高精度参考电压生成器相关联的超低功耗比较器。

这些设备集成了一个低功耗RTC、一个高级16位定时器、一个通用32位计数器、两个通用16位计数器和两个16位低功耗计时器。

此外，STM32WB55xx (不在UFQFPN48封装)上，可提供高达18个电容式传感器通道。STM32WB55xx还集成了一个内置的LCD驱动器，分辨率为8x40或4x44，具有内部升压转换器。

STM32WB55xx 和 STM32WB35xx 也具有标准和高级的通信接口，即一种 USART (ISO 7816, IrDA, Modbus 和 Smartcard mode), 一种低功耗 UART (LPUART), 两个 I2Cs (SMBus/PMBus), 两个 SPIs (一个用于 STM32WB35xx) 最高 32 MHz, 一种串行音频接口 (SAI) 带有两个通道和三个 PDMs, 一种 USB 2.0 FS 设备带有集成的无晶体振荡器，支持 BCD 和 LPM，以及一种 Quad-SPI 带有执行在地方 (XIP) 能力。

STM32WB55xx 和 STM32WB35xx 在 -40 到 +105 °C (+125 °C 节点)和 -40 到 +85 °C (+105 °C 节点)温度范围内运行，电源为 1.71V到3.6V电源。一套全面的电源省电模式使得可以设计低功耗应用。

设备包括模拟输入的独立电源，用于ADC。

The STM32WB55xx and STM32WB35xx integrate a high efficiency SMPS 下降转换器 with automatic bypass mode capability when the VDD falls below VBORx (=1 2 3 x , , 4) (2 0) , voltage level default is . V . It includes independent power supplies for analog input for ADC and comparators, as well as a 3.3伏 dedicated supply input for USB.

一个专门为 VBAT 设计的供电系统允许设备备份 LSE 2.768 kHz 振荡器、RTC 和备份寄存器，从而使 STM32WB55xx 和 STM32WB35xx 即使主 VDD 不可用也能通过 CR2032 相似的电池、Supercap 或小型可充电电池提供这些功能。

STM32WB55xx 提供四种封装，引至至129引。 STM STM STM3535xx 提供一种封装，48 个引脚。 e

表 2. STM32WB55xx 和 STM32WB35xx 设备功能和外围设备计数

Feature		STM32WB55Cx			STM32WB55Rx			STM32WB55Vx				STM32WB35Cx	
Memory density (bytes)	Flash	256 K	512 K	1 M	256 K	512 K	1 M	256 K	512 K	1 M	640 K	256 K	512 K
	SRAM	128 K	256 K	256 K	128 K	256 K	256 K	128 K	256 K	256 K		96 K	
	SRAM1	64 K	192 K		64 K	192 K		64 K	192 K			32 KB	
	SRAM2	64 K											
BLE		5.2 (2 Mbps)											
802.15.4		Yes											
Timers	Advanced	1 (16 bits)											
	General purpose	2 (16 bits) + 1 (32 bits)											
	Low power	2 (16 bits)											
	SysTick	1											
Communication interfaces	SPI	1			2							1	
	I2C	2											
	USART(1)	1											
	LPUART	1											
	SAI	2 channels											
	USB FS	Yes											
	QSPI	1											
RTC		1											
Tamper pin		1			3							1	
Wakeup pin		2			5							2	
LCD, COMxSEG		Yes, 4x13			Yes, 4x28			Yes, 8x40 or 4x44				No	
GPIOs		30			49			72				30	
Capacitive sensing		No			6			18				No	
12-bit ADC Number of channels		13 channels (incl. 3 internal)			19 channels (incl. 3 internal)							13 channels (incl. 3 internal)	
Internal V_{ref}		Yes											

表 2. STM32WB55xx 和 STM32WB35xx 设备功能和外围设备计数 (继续)

Feature		STM32WB55Cx	STM32WB55Rx	STM32WB55Vx		STM32WB35Cx
Analog comparator		2				
Max CPU frequency		64 MHz				
Operating temperature	Ambient	-40 to +85 and -40 to +105 °C			-40 to +85 °C	-40 to +85 and -40 to +105 °C
	Junction	-40 to +105 and -40 to +125 °C			-40 to +105 °C	-40 to +105 and -40 to +125 °C
Operating voltage		1.71 to 3.6 V				
Package		UFQFPN48 7 mm x 7 mm 0.5 mm pitch, solder pad	VFQFPN68 8 mm x 8 mm 0.4 mm pitch, solder pad	WLCSP100 0.4 mm pitch		UFQFPN48 7 mm x 7 mm 0.5 mm pitch, solder pad
				UFBGA129 0.5 mm pitch	-	

1. USART peripheral can be used as SPI.

图1. STM32WB55xx 块图

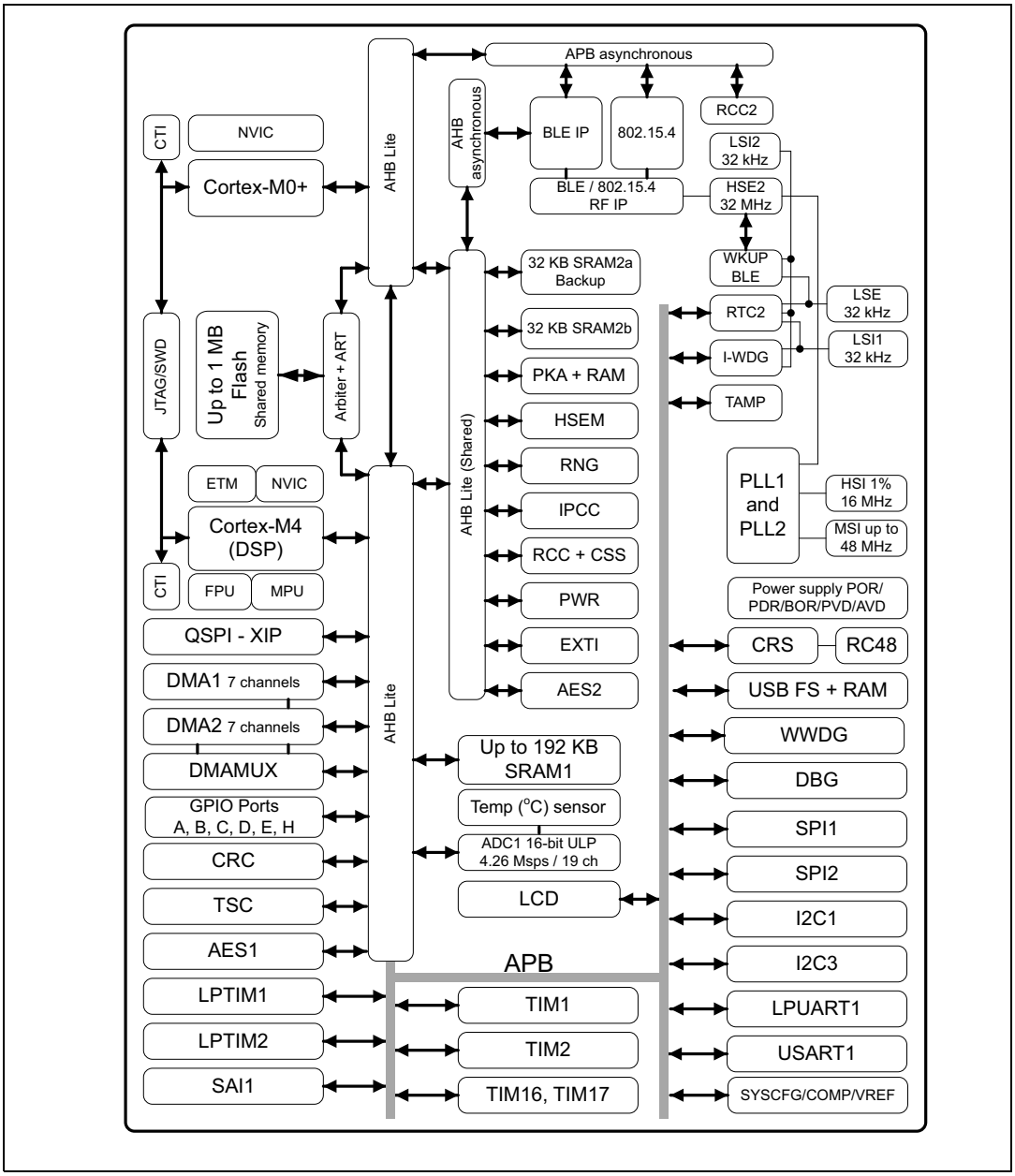
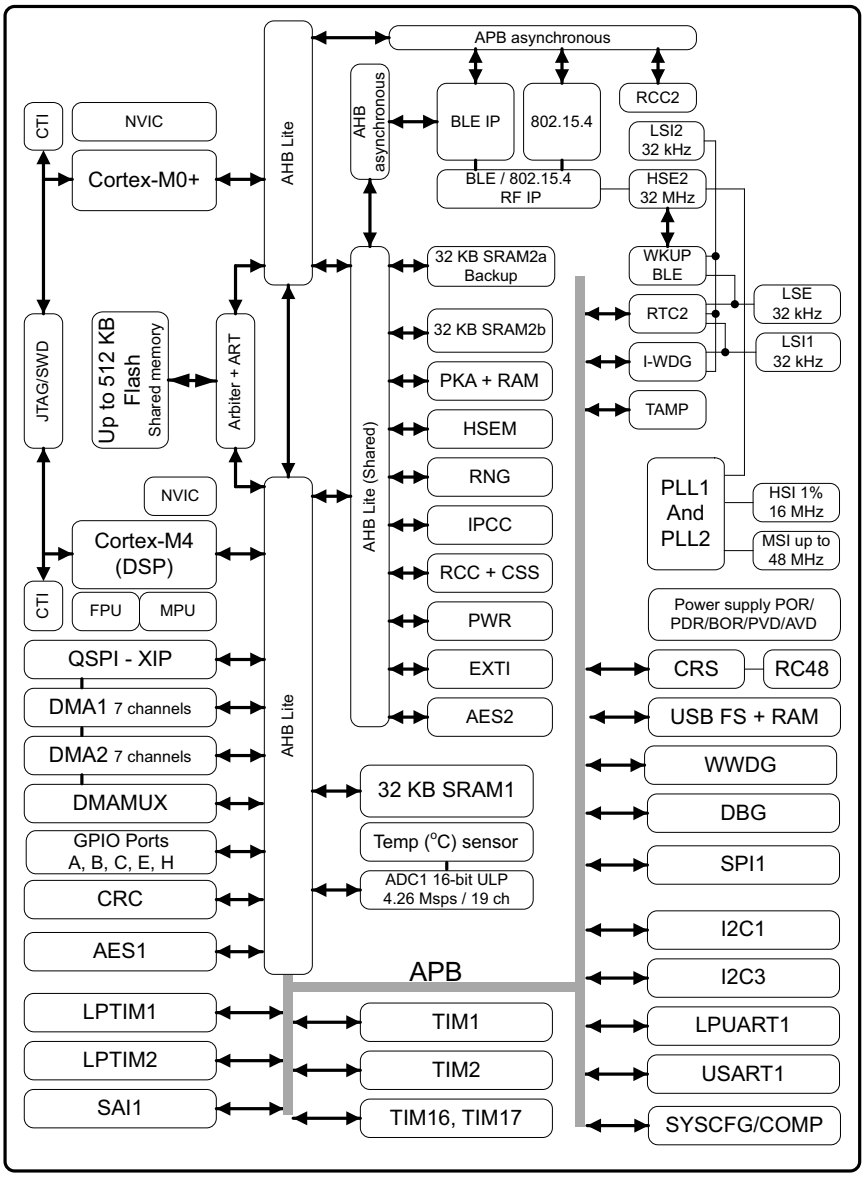


图2. STM32WB35xx 块图



3 功能概述

3.1 架构

STM32WB55xx和STM32WB35xx多协议无线设备集成了一个蓝牙和802.15.4无线电子子系统，通过Arm® Cortex®-M4 CPU (称为CPU1) 的通用微控制器子系统进行接口，主机应用程序运行在此处。

无线电子子系统由一个无线电模拟前端、蓝牙和802.15.4数字MAC块组成，以及一个专有Arm® Cortex®-M0+ 微控制器 (称为CPU2)，还包含专有外设。无线电子子系统执行所有蓝牙和802.15.4低层堆叠，减少了与CPU1的交互，仅限于高电平交换。

一些函数在无线电子子系统CPU (CPU2) 和主机CPU(CPU1)之间共享：

- 闪存内存• SRAM1、SRAM2a和SRAM2b (SRAM2a可以在待机模式下保留)
- 安全外设 (随机数生成器、AES1、PKA)• 时钟RCC• 电源控制 (PWR)

无线电子子系统与Cortex-M4 CPU之间的通信和外围设备共享通过专用的内部处理器通信控制器IPCC和信号量机制HSEM实现。

3.2 Arm® Cortex®-M4 核心配备浮点单元

STM32WB55xx STM32WB35xxArm® Cortex®-M4 core with FPU 是嵌入式系统的处理器。它被开发用于提供一个成本较低的平台，以满足 MCU 实现的需求，具有减少的引脚数量和低功耗，同时提供出色的计算性能和高级中断响应。

The Arm® Cortex®-M4 with FPU 32位精简指令集处理器 features exceptional code-efficiency, delivering the high-performance expected from an Arm® core in the memory size usually associated with 8- and 16-bit devices.

该处理器支持一组 DSP 指令，使得信号处理和复杂算法执行更加高效。

其单精度浮点单元可以通过使用金属语言开发工具来加速软件开发，同时避免饱和。

具有嵌入式 Arm® Cortex®-M4 核心，STM32WB55xx 和 STM32WB35xx 兼容所有 Arm® Cortex®-M4 工具和软件。 th

图1和图2分别显示 STM32WB55xx 和 STM32WB35xx 设备的通用块图。

3.3 内存

3.3.1 适应实时内存加速器 (ART 加速器)

ART 加速器是一种为 STM32 业标 Arm® Cortex®-M4 处理器优化的内存加速器。它平衡了 Arm® Cortex®-M4 对闪存技术的固有性能优势，后者通常需要处理器在更高频率下等待闪存。

为了在 64 MHz 下释放接近 80 DMIPS 的性能，该加速器实现了指令预取队列和分支缓存，从而提高了从 64 位闪存中执行程序的速度。基于 CoreMark 基准测试，由 ART 加速器实现的性能相当于在 CPU 频率最高为 64 MHz 时从闪存中进行 0 等待状态程序执行。

3.3.2 内存保护单元

内存保护单元 (MPU) 用于管理 CPU1 对内存的访问，以防止一个任务意外损坏其他任何活动任务使用的内存或资源。此内存区域组织成多达八个受保护区域，这些区域可以分割成八个子区域。受保护区域的大小介于 32 字节和可寻址的整个 4 GB 内存之间。

MPU尤其适用于一些需要保护关键或认证代码免受其他任务不当行为影响的应用场景。它通常由实时操作系统 (real-time operating system) 管理。如果一个程序访问了 MPU 禁止的内存位置，RTOS 将检测到并采取行动。在 RTOS 环境中，内核可以根据要执行的进程动态更新 MPU 区域设置。

MPU 是可选的，并且可以为那些不需要它的应用程序绕过。

3.3.3 嵌入式闪存内存

STM32WB55xx 和 STM32WB35xx 设备分别提供高达 1 Mbyte 和 512 Kbytes 的嵌入式闪存内存，用于存储程序和数据，以及一些客户密钥。

通过选项字节可以配置灵活的保护措施：

- 读取保护 (RDP) 用于保护整个内存。有三个水平可用：
  – 级别 0: 无读取保护– 级别 1: 内存读取保护: 如果调试功能连接，或在 SRAM 中启动，或选择引导加载程序，则无法从或向闪存内存进行读取– 级别 2: 芯片读取保护: 调试功能 (Cortex®-M4 和 Cortex®-M0+JTAG 和 串行线缆), 在 SRAM 中启动和引导加载程序选择被禁用 (JTAG 熔丝). 此选择是不可逆的。

表 3. 访问状态与读取保护级别和执行模式

Area	Protection level	User execution			Debug, boot from SRAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No(1)	No(1)	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(2)	No	No	N/A(2)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2a SRAM2b	1	Yes	Yes	Yes(2)	No	No	No(2)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. The option byte can be modified by the RF subsystem.
2. Erased when RDP changes from Level 1 to Level 0.

- 写入保护 (WRP): 受保护区域对擦除和编程进行了保护。可以选择两个区域，具有 4-K 字节粒度。• 专有代码读取保护 (PCROP): 可以保护闪存内存的两部分免受第三方的读取和写入。受保护区域是只执行的：它只能由 STM32 CPU 作为指令代码访问，而所有其他访问 (DMA, 调试和 CPU 数据读取、写入和擦除) 都被严格禁止。可以选择两个区域，具有 2-K字节粒度。一个额外的选项位 (PCROP_RDP) 允许选择 PCROP 区域是否在 RDP 保护从别 1 更改为 级别 0 时被擦除。

闪存内存的一部分用于 RF 子系统 CPU2，并且不能被主机 CPU1 访问。

T整个非易失性内存嵌入了错误纠正代码 (ECC) 功能，支持：
- 单错误检测和修复• 双错误检测• ECC 失败的地址可

以在 ECC 寄存器中读取

嵌入式闪存内存在 CPU1 和 CPU2 之间以时间共享基础共享。专门的硬件机制允许这两个 CPU 执行写/擦除操作。

3.3.4 嵌入式 SRAM

STM32WB55xx 设备配备了高达 256 K 字节的嵌入式 SRAM，分成三个块：

- **SRAM1**: 最多 192 Kbytes 映射到地址 0x2000 0000• **SRAM2a**: 32 Kbytes 于地址 0x2003 0000，也镜像在 0x1000 0000，具有硬件奇偶校验 (此 SRAM 可以在待机模式下保留)• **SRAM2b**: 32 Kbytes 于地址 0x2003 8000 (与 SRAM2a 连续) 并镜像在 0x1000 8000，具有硬件奇偶校验

STM32WB35xx 设备配备了 96 Kbytes 的嵌入式 SRAM，分为三个块：

- **SRAM1**: 32 Kbytes 映射到地址 0x2000 0000• **SRAM2a**: 32 Kbytes 于地址 0x2003 0000也也镜像在 0x1000 0000，具有硬件奇偶校验 (此 SRAM 可以在待机模式下保留)• **SRAM2b**: 32 Kbytes 于地址 0x2003 8000 (与 SRAM2a 连续) 并镜像在 0x1000 8000，具有硬件奇偶校验

SRAM2a 和 SRAM2b 可以被写保护，粒度为 1-Kbyte。SRAM2a 和 SRAM2b 的一部分用于 RF子系统，并且不能被主机 CPU1 访问。

内存可以以 0 等待状态在所有 CPU1 和 CPU2 时钟速度下进行读/写访问。

3.4 安全性和安全性

STM32WB55xx 和 STM32WB35xx 包含了 BLE 和 IEEE 802.15.4 以及主机应用程序的许多安全块。 r

它包括：

- BLE 和 802.15.4 密钥的客户存储• 仅限无线电子子系统访问的安全闪存内存分区
- 仅能由 RF子系统 访问的安全 SRAM 分区• 真正的随机数生成器 (RNG)• 高级加密标准硬件加速器 (AES-128 位和 AES-256 位，支持链式模式 ECB, CBC, CTR, GCM, GMAC, CCM)• 私加速 (PKA) 包括:– 最大模大小为3136位的模运算，包括幂运算
– 椭圆曲线在素域上的标数乘法，ECDSA 签名，ECDSA 验证，最大模大小为 521 位

- 循环冗余校验计算单元 (CRC)

为了确保无论主机应用程序如何，RF子系统 CPU2 执行的所有代码都是安全的，已经实施了一种特定机制。对于 AES1，客户密钥可以由 CPU2 管理，并由 CPU1 用于加密/解密数据。

3.5 启动模式和固件更新

At startup, BOOT0引脚 and BOOT1 选项位 are used to select one of three boot options:

- 从用户Flash启动 • 从系

统内存启动 • 从嵌入式

SRAM启动

设备总是在 CPU1 核心上启动。 内置引导加载程序代码使其能够从各种外围设备启动：

- USB
- UART
- I2C
- SPI

安全固件更新 (特别是从系统启动并通过空中提供的蓝牙和 802.15.4) 。

3.6 无线电子子系统

STM32WB55xx 和 STM32WB35xx 集成了一个超低功耗的多协议射频 Bluetooth® Low Energy (BLE) 和 802.15.4 网络处理器，符合 Bluetooth® 规范 5.2 和 IEEE® 802.15.4-2011。BLE 功能包括 1 Mbps 和 2 Mbps 的传输速率，支持同时扮演 BLE 传感器和中心设备的多个角色，集成了椭圆曲线 Diffie-Hellman (ECDH) 密钥协商协议，从而确保安全连接。

蓝牙堆栈和802.15.4 低层次层运行在嵌入式 Arm® Cortex®-M0+ core(CPU2)上。堆栈存储在嵌入式闪存内存中，该内存也与 Arm® Cortex®-M4 (CPU1) 应用共享，从而实现现场堆栈更新。

3.6.1 RF 前端块图

RF 前端基于 Tx 中载波的直接调制，并在 Rx 模式下使用低中间频率架构。

感谢 RF 接口上的内部变压器，电路直接通过天线(单端连接接口，阻抗接近 50 Ω)。内部变压器的自然带通行为简化了旨在进行谐波滤波和外带干扰拒绝的外部电路。

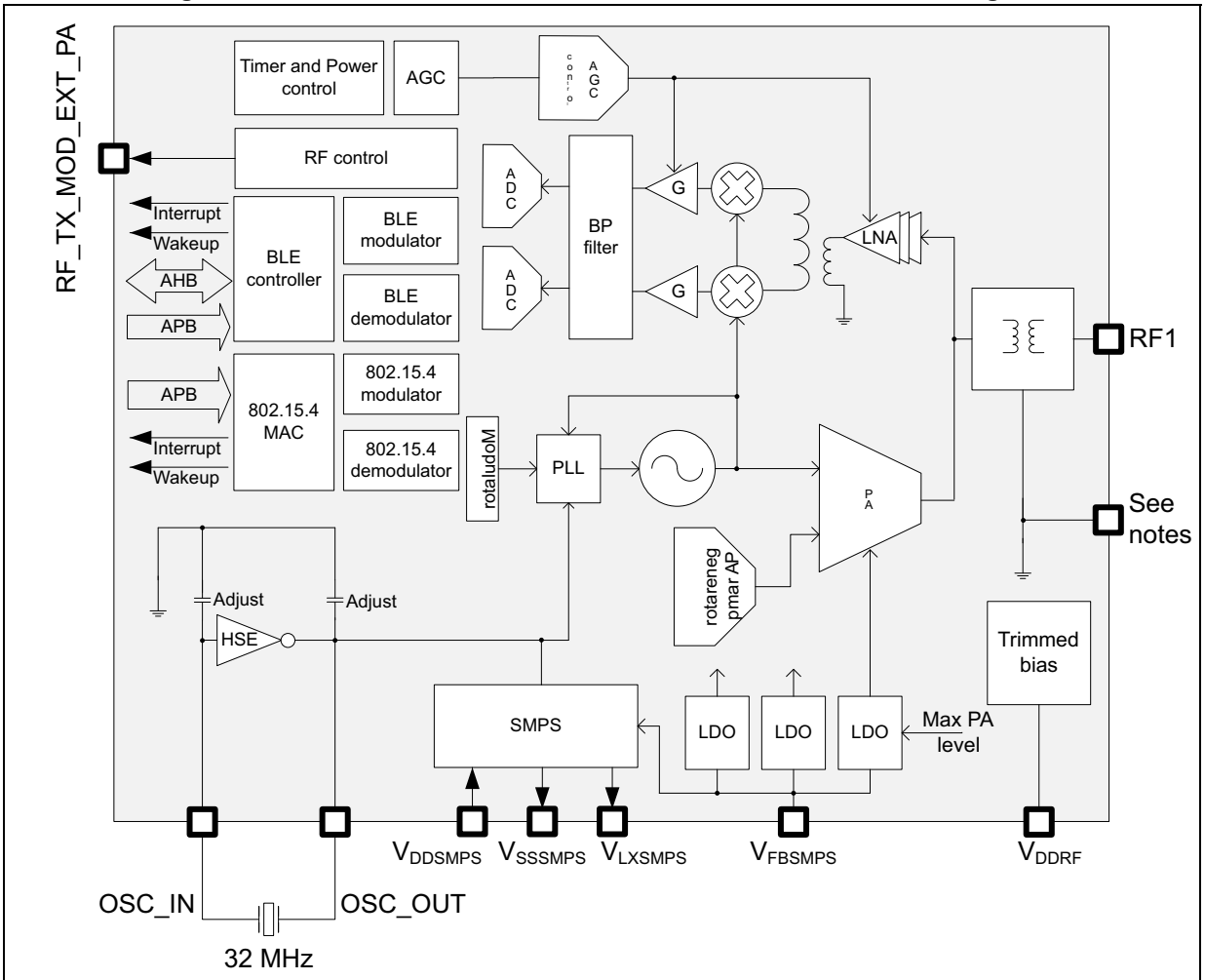
在发送模式下，最大输出功率可以通过功率放大器的可编程 LDO 电压由用户可选择。线性化、平滑的模拟控制提供清洁的功率上升。

在接收模式下，电路可以用于标准的高性能或降低的功耗 (用户可编程)。自动增益控制 (AGC) 可以减少 RF 和 IF 位置的链路增益，以实现优化的干扰拒绝。感于使用复杂滤波和高度准确的 I/Q 架构，可以实现高灵敏度和优秀的线性。

物料清单减少是由于高度的集成。无线电频率来源是从外部 32 MHz 晶体振荡器合成的，不需要任何外部

通过用户可编程集成电容器的双重网络，实现了调节电容网络。

Figure 3. STM32STM32WB55xx 和 STM32WB35xx 无线电前端块图 lock diagram



注意：- UFQFPN48 和 VFQFPN68：V_{SS} 通过暴露的铜箔，和 V_{SSRF} 引脚必须连接到地平面 - WLCSP100 和 UFBGA129：V_{SSRF} 引脚必须连接到地平面

3.6.2 BLE 通用描述

BLE块是一个主从处理器，遵循蓝牙规范5.2标准 (2 Mbps)。

它集成了一个2.44 GHz RF收发器和一个强大的 Cortex®-M0+ 核心，上面运行着完整的 Bluetooth Low Energy 协议的电源优化栈，提供主/从角色支持

STM32WB55xx STM32WB35xx3.6.2 BLE 通用描述•
GAP：中心、外围设备、观察者或广播角色• ATT/GATT：
客户端和服务器• SM：隐私、身份验证和授权•
L2CAP• 链路层：AES-128 加密和解密

此外，根据蓝牙规范 5.2，BLE块提供：
• 同时支持多个角色• 主从机和多个角色同时存在• LE 数据包长度扩展 (使得在应用水平上能够达到 800 kbps)• LE 隐私 1.2• LE 安全连接• 灵活的互联网连接选项• 高数据速率 (2 Mbps)

该设备允许应用程序满足由使用标准硬币电池而产生的紧密峰值电流要求。当使用高效集成 SMPS 降压转换器时，无线电前端消耗 (Itmax) 仅为最高输出功率 (+6 dBm) 下的 8.1 mA。

子系统的电源效率已优化：在同时运行射频和应用核心时使用 SMPS，Cortex®-M4 核心消耗在活动模式下达到 53 µA / MHz。

超低功耗休眠模式和不同工作模式之间的非常短的过渡时间导致实际工作条件下的非常低的平均电流消耗，从而延长电池寿命。

BLE块集成了一个完整的带通 balun，因此减少了对外部组件的需求。

Cortex®-M4应用程序处理器 (CPU1) 运行应用程序与运 BLE堆栈在专用 Cortex®-M0+ (CPU2) 上运行之间的连接通过一个标准化的 API 进行，使用一个专用的 IPCC。

3.6.3 802.15.4 通用描述

The STM32WB55xx and STM32WB35xx embed a dedicated 802.15.4 硬件MAC:
• 支持 802.15.4 2011年发布• 高级 MAC 帧过滤；硬件防火墙：基于源/目的地地址、帧版本、安全性启用、帧类型的可编程过滤器• 256-字节 接收FIFO；最大 8 帧容量，额外帧信息 (时序、平均RSSI、LQI)• 128-字节 发送FIFO 保留– 内容不丢失，CPU2控制下可以进行重传• 自动帧确认，可编程延迟• 高级信道访问特性– 完整 CSMA-CA 支持– 超帧计时器– 定位信号支持 (需要 LSE)– 灵活的发送控制与可编程延迟• 具有保留功能的配置寄存器，可降低至待机模式以进行软件/自动恢复• 独立嗅探器，基于计时器或CPU2请求唤醒• 自动帧发送/接收/睡眠周期，特定事件触发 CPU2 中断

3.6.4 RF pin description

RF块包含专用引脚，列在 表4.

表4. 无线电引脚列表

Name	Type	Description
RF1	I/O	RF Input/output, must be connected to the antenna through a low-pass matching network
OSC_OUT		32 MHz main oscillator, also used as HSE source
OSC_IN		
RF_TX_ MOD_EXT_PA		External PA transmit control
VDDRF	V_{DD}	Dedicated supply, must be connected to V_{DD}
VSSRF(1)	V_{SS}	To be connected to GND

1. On packages with exposed pad, this pad must be connected to GND plane for correct RF operation.

3.6.5 典型射频应用原理图

图式图在 图4和表4中列出的外部组件表4仅用于参考。有关更多详细信息，请参见 “参考设计” 提供在单独文档中。

图4. 无线电部分的外部组件

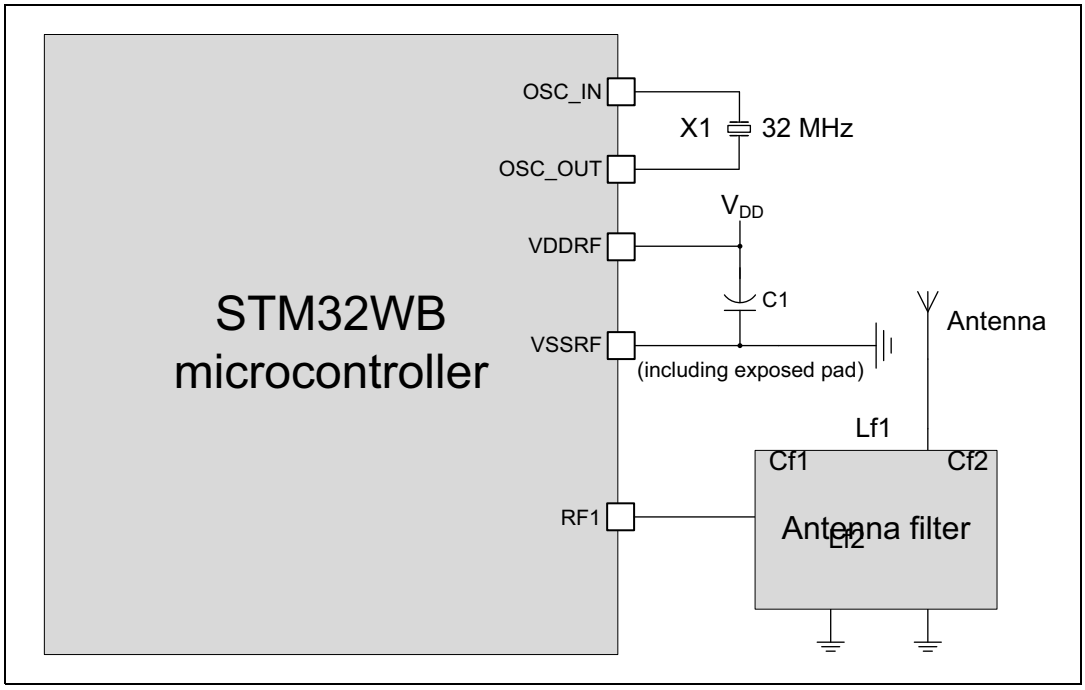


表 5. 典型外部组件

Component	Description	Value
C1	Decoupling capacitance for RF	100 nF // 100 pF
X1	32 MHz crystal(1)	32 MHz
Antenna filter	Antenna filter and matching network	Refer to AN5165, on *www.st.com*
Antenna	2.4 GHz band antenna	-

1. e.g. NDK reference: NX2016SA 32 MHz EXS00A-CS06654.

Note: *For more details refer to AN5165 "使用 STM32WB 微控制器开发无线电硬件" available on www.st.com.*

3.7 Power supply management

3.7.1 电源分布

The device integrate an SMPS 下降转换器 to improve low功耗能 when the VDD 电压 is high enough. This converter has an intelligent mode that automatically enters in bypass mode when the VDD 电压 falls below a specific BORx

x ,, or voltage.

(= 1 2 3 4)
默认情况下，复位时，SMPS 位于绕过模式。

该设备可以通过将其输出连接到 VDD 来无需 SMPS 进行操作。这种情况适用于电压低或功率消耗不关键的应用场景。

图5. 电源分布

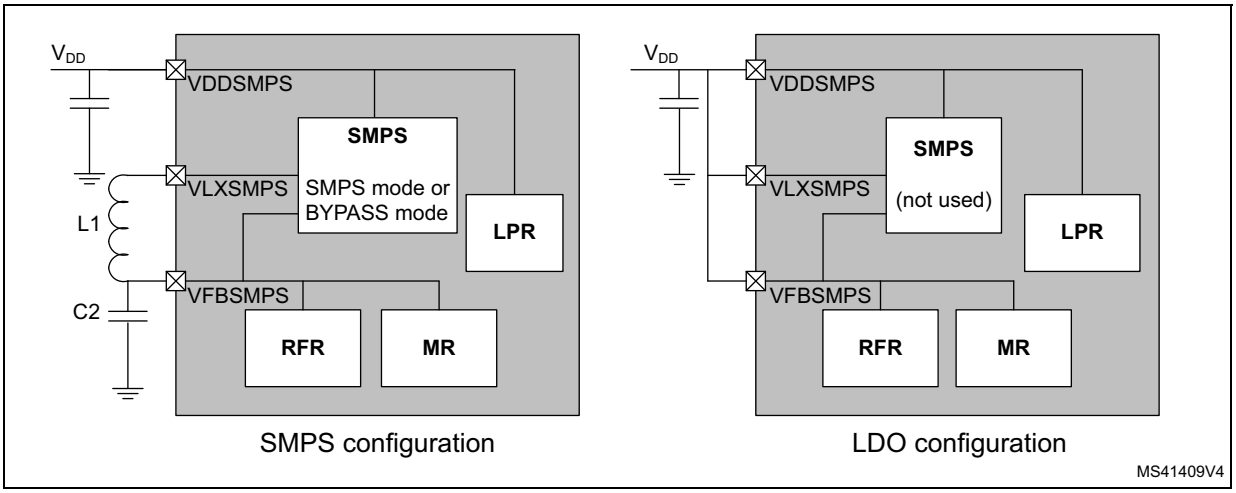


表6. 电源典型组件

Component	Description		Value
C2	SMPS output capacitor(1)		4.7 µF
L1(2)	SMPS inductance	For 8 MHz(3)	2.2 µH
		For 4 MHz(4)	10 µH

1. e.g. GRM155R60J475KE19.
2. An extra 10 nH inductor in series with L1 is needed to improve the receiver performance, e.g Murata LQG15WZ10NJ02D
3. e.g. Wurth 74479774222.
4. e.g. Murata LQM21FN100M70L.

SMPS 可以在任何时候由应用软件开启或设置为绕过模式，例如当需要非常准确的 ADC 测量时。

3.7.2 电源方案

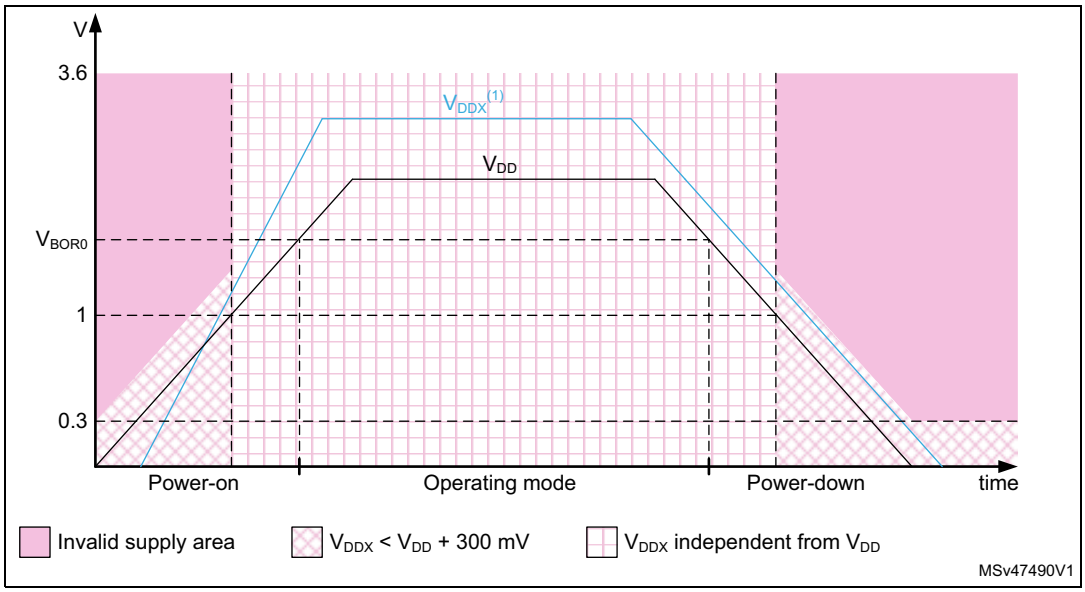
设备有不同的电压供应(看图7和图8) 可以在以下电压范围内运行:

- VDD = 1.71 到 3.6 V：外部 I/Os 的电源，包括 (VDDIO)、内部调节器和系统功能，例如 RF、SMPS、复位、电源管理和内部时钟。它通过 VDD 引脚提供。VDDRF 和 VDDSMPS 必须始终连接到 VDD 引脚。
- VDDA = 1.62 (ADC/COMPs) 到 3.6 V：外部模拟电源用于 ADC、比较器和电压参考缓冲器。VDDA 电压水平可以独立于 VDD 电压。如果未使用 VDDA，则必须连接到 VDD。
- VDDUSB = 3.0 到 3.6 V：外部独立电源用于 USB 收发器。如果未使用 VDDUSB，则必须连接到 VDD。
- VLCD = 2.5 到 3.6 V：LCD 控制器可以通过 VLCD 引脚外部供电，也可以从嵌入式升压转换器生成的内部电压供电。该转换器可以生成高达 3.6 V 的 VLCD 电压，前提是 VDD 电压高于 2.0 V。请注意，LCD 只在 STM32WB55xx 设备上可用。

在上电/下电过程中，必须遵守以下电源顺序要求：

- 当 VDD 低于 1V 时，其他电源 (VDDA, VDDUSB, VLCD) 必须保持在 VDD + 300 mV 以下。
- 当 VDD 高于 1V 时，所有电源都是独立的。

图6. 上电/下电序列

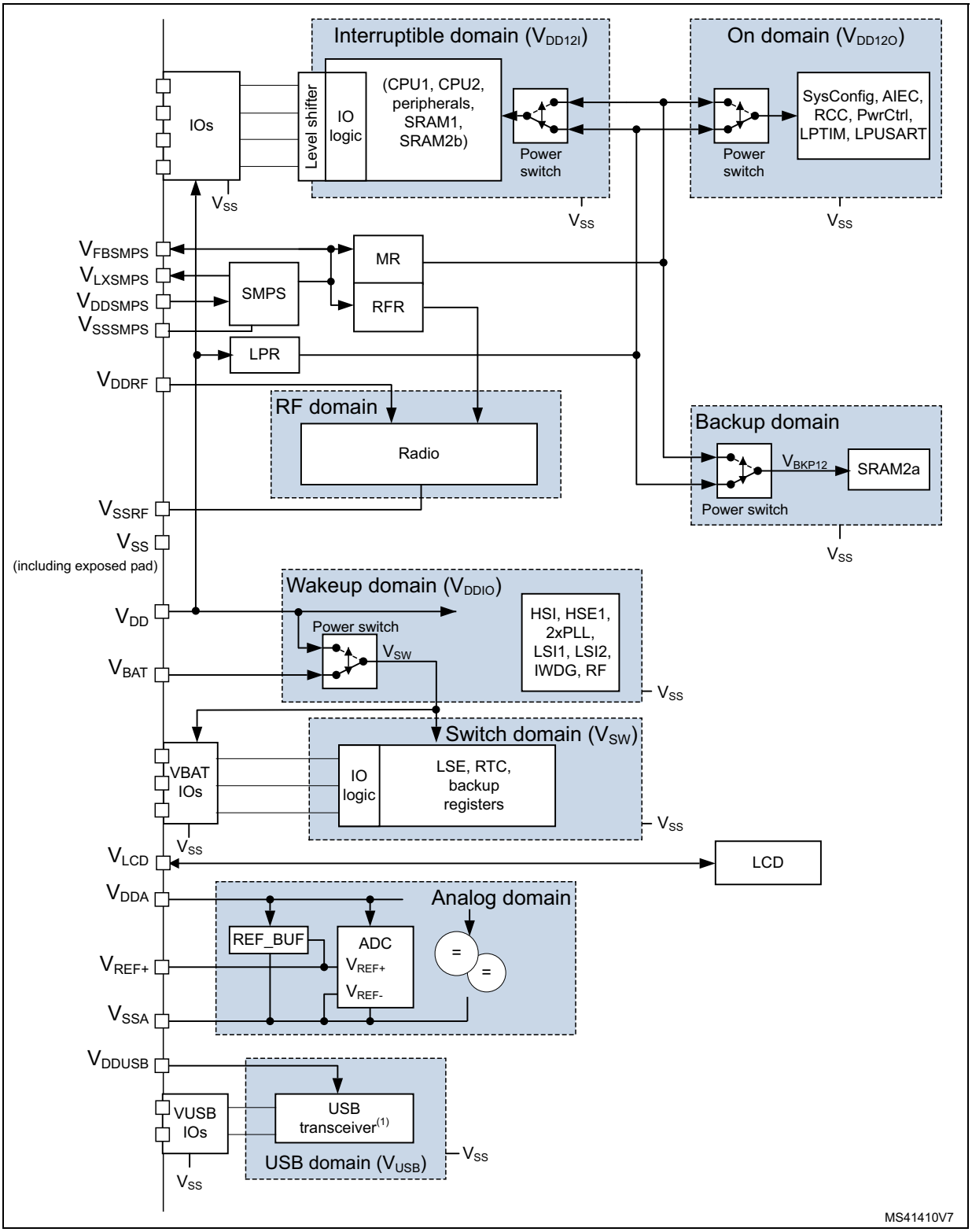


1. VDDX 指的是 VDDA, VDDUSB 和 VLCD 中的任何一个电源。

在断电阶段，VDD 可能暂时低于其他电源，只要为 MCU 提供的能量低于 1 mJ。这允许外部耦合电容器以不同的时间常数在断电瞬变阶段放电。

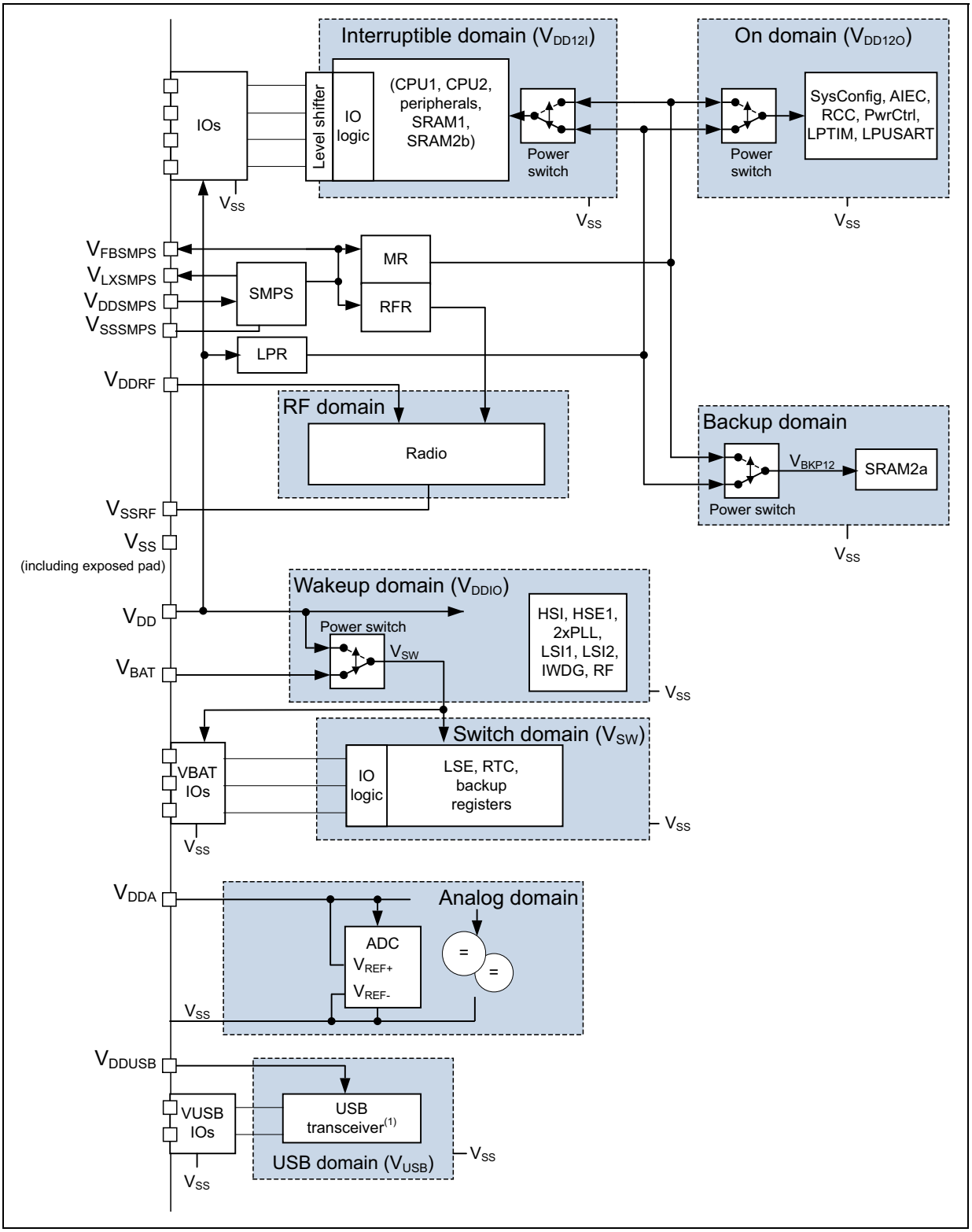
Note: *VDD, VDDRF* 和 *VDDSMPS* 必须连接在一起，以便它们可以跟随相同的电压序列。

图7. STM32WB55xx - 电源概述



1. USB收发器由 VDDUSB 供电，当选择 USB替代功能 (PA11 和 PA12) 时，与 USB 相关的 GPIOs 由 VDDUSB 供电。当不选择 USB替代功能时，与 USB 相关的 GPIOs 作为标准 GPIOs 供电。

图8. STM32WB35xx - 电源概述



1. USB收发器由 VDDUSB 供电，当选择 USB替代功能 (PA11 和 PA12) 时，与 USB 关联的 GPIOs 由 VDDUSB 供电。当未选择 USB替代功能时，与 USB 关联的 GPIOs 以标准 GPIOs 的方式供电。

3.7.3 线性电压调节器

三个嵌入式线性电压调节器为大部分数字和无线电电路提供动力，包括主调节器 (MR)、低功耗调节器 (LPR) 和 无线电调节器 (RFR)。

- 主调节器在运行模式和休眠模式以及停止0模式中使用。• 低功耗调节器在低功耗运行、低功耗休眠、停止1和停止2模式中使用。它也用于为保持状态下的保留的SRAM2a提供电源。• 无线电调节器用于为无线电模拟部分提供电源，其活动由无线电子子系统自动管理。

所有调节器在待机模式和关闭模式下进入关闭状态：调节器输出处于高阻抗状态，内核电路断电，导致零消耗。

超低功耗STM32WB55xx和STM32WB35xx支持动态电压缩放，以优化运行模式下的功率消耗。主调节器供应逻辑的电压可以根据系统的最大操作频率进行调整。(VCORE)

有两个电压和频率范围：

- 范围1，CPU运行到64 MHz• 范围2，最大CPU频率为16 MHz (注意HSE可以在此模式下启用). 所有外设时钟也被限制为16 MHz。

VCORE 也可以由低功耗调节器供电，主调节器已关闭。系统则处于 低功耗运行模式。在这种情况下，CPU以最高 2 兆赫的速度运行，且带有独立时钟的外围设备可以由 HSI16 (在此模式下供电。RF 子系统不可用)。

3.7.4 电源监控器

在所有模式除了关闭之外，都激活了集成的超低功耗电压下降复位 (BOR) ，确保上电和断电期间的正确操作。当监控的供电电压 VDD 低于指定阈值时，设备将保持复位模式，无需外部复位电路。

BOR 级别的最低水平为上电时的 1.71 V，其他更高的阈值可以通过选项字节进行选择。该设备具有内置的可编程电压检测器 (PVD) ，它监控 VDD 电源并将其与 VPVD 阈值进行比较。当 VDD 低于 VPVD 阈值或 VDD 高于 VPVD 阈值时，可以生成中断。中断服务例程随后可以生成警告消息并/或将 MCU 置于安全状态。PVD 由软件启用。

此外，设备内置了一个外围电压监测器 (PVM) ，它将独立的供电电压 VDDA 与固定的阈值进行比较，以确保外围设备处于其功能性供电范围内。

任何 BOR 级别也可以用来在 VDD 电压低于给定的电压水平时自动将 SMPS 下降转换器切换到绕过模式。运行模式可通过寄存器位选择，BOR 级别可通过选项字节选择。

3.7.5 低功耗模式

这些超低功耗设备支持多种低功耗模式，以实现低功耗、短启动时间、可用外围设备和可用唤醒源之间的最佳折衷。

默认情况下，微控制器在系统或电源复位后处于运行模式，范围1。用户可以选择以下描述的低功耗模式中的一个：

- **睡眠模式**

  在睡眠模式下，只有 CPU1 停止。所有外围设备，包括无线电子子系统，继续运行并可以在中断/事件发生时唤醒 CPU。

- **低功耗运行**

  此模式通过低功耗调节器供应 VCORE 来实现，以最小化调节器运行电流。代码可以从 SRAM 或闪存内存执行，并且 CPU1 频率限制为 2 兆赫。具有独立时钟的外围设备可以由 HSI16 起动。无线电子子系统在此模式下不可用，并且必须关闭。

- **低功耗休眠**

  此模式从低功耗运行模式进入。只有 CPU1 时钟停止。当唤醒由事件或中断触发时，系统恢复到 低功耗运行模式。无线电子子系统在此模式下不可用，并且必须关闭。

- **停止模式 0、停止模式 1 和停止模式 2**

  停止模式可以实现最低的功率消耗，同时保留所有 SRAM 和寄存器的内容。LSE (或 LSI) 仍在运行。

  RTC 可以在停止模式下保持活动状态，包括带有 RTC 的停止模式和不带有 RTC 的停止模式。
  一些具有唤醒能力的外围设备可以在停止模式下启用HSI16 RC，以检测它们的唤醒条件。

  三种模式可用：停止模式 0、停止模式 1 和停止模式 2。在停止 2 模式中，大部分 VCORE 领域被置于更低的泄漏模式。

  停止 1 提供了最多的活动外围设备和唤醒源，唤醒时间更短，但消耗量高于停止 2。在停止 0 模式下，主调节器保持打开状态，允许非常快的唤醒时间，但消耗量较高。

  在这些模式下，无线电子子系统可以在所有停止模式下等待 incoming来的事件。
  退出 Stop 0, Stop1 或 Stop2 模式后，系统时钟可以是 MSI 最高到 48 兆赫或 HSI16（如果 RF 子系统已禁用）。如果使用 RF 子系统或 SMPS，则退出必须设置为仅 HSI16。如果使用，则 SMPS 将自动重新启动。

- **待机模式**

  待机模式用于在 BOR 下实现最低的功率消耗。内部调节器被关闭，以便 VCORE 领域也被关闭。

  RTC 可以在 RTC) 的情况下保持活跃 (待机模式。
  电压下降复位 (BOR) 在待机模式下始终保持活跃。
  每个 I/O 在待机模式下的状态可以通过软件进行选择：带有内部上拉、内部下拉或浮动的 I/O。

  进入待机模式后，SRAM1、SRAM2b和寄存器内容将丢失，除了备份域中的寄存器和待机电路。可选地，可以在待机模式下保留SRAM2a，由低功耗调节器(提供，在32 KB SRAM2a 保留模式)下工作。

  设备在发生外部复位 (NRST 引脚)、IWDG 复位、WKUP 引脚事件 (可配置的上升或下降油v4}，或 RTC 事件 (报警、周期性唤醒、时间戳、篡改) 时从待机模式退出。如果 LSE (在 LSE 上的 CSS 或从无线电系统唤醒)检测到故障，则也会退出待机模式。

唤醒后的系统时钟为 16 MHz，来自 HSI16。如果使用，则 SMPS 会自动重新启动。

在此模式下，RF 可以被使用。

- **关闭**

  关闭模式允许实现最低的功率消耗。内部调节器被关闭，以便VCORE 领域也被关闭。

  RTC 在 (关闭模式, RTC, 关闭模式无 RTC) 下可以保持活动状态。

  电压下降复位在关闭模式下不可用。在此模式下无法进行电压监控，因此切换到备份域不受支持。SRAM1、SRAM2a、SRAM2b 和寄存器内容会丢失，除了在 VCCORE 的寄存器之外。

  备份域。

  设备在外部复位 (NRST 引脚) 或 WKUP 引脚时退出关闭模式。
  事件 (可配置的上升或下降沿)，或者发生 RTC 事件 (报警，周期性唤醒，时间戳，篡改).
  唤醒后的系统时钟为 4 MHz，来自 MSI.
  在这种模式下，RF 不再工作。

当 RF 子系统活动时，它会根据其需求更改电源状态 (运行，停止，待机模式)。这个操作对于 CPU1 主机应用程序是透明的，并且由一个专门的硬件状态机管理。在任何给定的时间，实际达到的有效电源状态是 CPU1 和 RF 子系统所需要的较高的那个。

表7总结了所有可用模式下的外围功能。唤醒能力详细说明在灰色单元格中。

表7. 所有模式的功能(1)

Peripheral(2)	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1		Stop 2		Standby		Shutdown		VBAT
						-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU1	Y		-	Y	-	-	-	-	-	-	-	-	-	-
CPU2	Y		-	Y	-	-	-	-	-	-	-	-	-	-
Radio system (BLE, 802.15.4)	Y	Y(3)	Y	-	-	Y	Y	Y	Y	Y(4)	Y(4)			
Flash memory	Y (5)		Y	O(6)	O(6)	R	-	R	-	R	-	R	-	R
SRAM1	Y		Y(7)	Y	Y(7)	R	-	R	-	-	-	-	-	-
SRAM2a	Y		Y(7)	Y	Y(7)	R	-	R	-	R(8)	-	-	-	-
SRAM2b	Y		Y(7)	Y	Y(7)	R	-	R	-	-	-	-	-	-
Quad-SPI	O		O	O	O	-	-	-	-	-	-	-	-	-
Backup registers	Y		Y	Y	Y	R	-	R	-	R	-	R	-	R
Brown-out reset (BOR)	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-

表7. 所有模式的功能(1) (继续)

Peripheral(2)	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1		Stop 2		Standby		Shutdown		VBAT
						-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Programmable voltage detector (PVD)	O		O	O	O	O	O	O	O	-	-	-	-	-
Peripheral voltage monitor PVMx (x=1, 3)	O		O	O	O	O	O	O	O	-	-	-	-	-
SMPS	O		O	O	O	O(9)	-	-	-	-	-	-	-	-
DMAx (x = 1, 2)	O		O	O	O	-	-	-	-	-	-	-	-	-
High speed internal (HSI16)	O		O	O	O	O(10)	-	O(10)	-	-	-	-	-	-
Oscillator HSI48	O		O	-	-	-	-	-	-	-	-	-	-	-
High speed external (HSE)(11)	O		O	O	O	-	-	-	-	-	-	-	-	-
Low speed internal (LSI1 or LSI2)	O		O	O	O	O	-	O	-	O	-	-	-	-
Low speed external (LSE)	O		O	O	O	O	-	O	-	O	-	O	-	O
Multi-speed internal (MSI)(12)	48	24	O	48	O	-	-	-	-	-	-	-	-	-
PLLx VCO maximum frequency	344	128	O	-	-	-	-	-	-	-	-	-	-	-
Clock security system (CSS)	O		O	O	O	O	O(13)	O	O(13)	-	-	-	-	-
Clock security system on LSE	O		O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto wakeup	O		O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC tamper pins	3		3	3	3	3	O	3	O	3	O	3	O	3
LCD	O		O	O	O	O	O	O	O	-	-	-	-	-
USB FS	O	-	O	-	-	-	O	-	-	-	-	-	-	-
USART1	O		O	O	O	O(14)	O(14)	-	-	-	-	-	-	-
Low-power UART (LPUART1)	O		O	O	O	O(14)	O(14)	O(14)	O(14)	-	-	-	-	-
I2C1	O		O	O	O	O(15)	O(15)	-	-	-	-	-	-	-
I2C3	O		O	O	O	O(15)	O(15)	O(15)	O(15)	-	-	-	-	-
SPIx (x=1, 2)	O		O	O	O	-	-	-	-	-	-	-	-	-
SAI1	O		O	O	O	-	-	-	-	-	-	-	-	-

表7. 所有模式的功能(1) (继续)

Peripheral(2)	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1		Stop 2		Standby		Shutdown		VBAT
						-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
ADC1	O		O	O	O	-	-	-	-	-	-	-	-	-
VREFBUF	O		O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x=1, 2)	O		O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O		O	O	O	-	-	-	-	-	-	-	-	-
Timers TIMx (x=1, 2, 16, 17)	O		O	O	O	-	-	-	-	-	-	-	-	-
Low-power Timer 1 (LPTIM1)	O		O	O	O	O	O	O	O	-	-	-	-	-
Low-power Timer 2 (LPTIM2)	O		O	O	O	O	O	-	-	-	-	-	-	-
Independent watchdog (IWDG)	O		O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O		O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O		O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O		O	O	O	-	-	-	-	-	-	-	-	-
True random number generator (RNG)	O	-	O	-	-	-	-	-	-	-	-	-	-	-
AES2 hardware accelerator	O		O	O	O	-	-	-	-	-	-	-	-	-
CRC calculation unit	O		O	O	O	-	-	-	-	-	-	-	-	-
IPCC	O		-	O	-	-	-	-	-	-	-	-	-	-
HSEM	O		-	O	-	-	-	-	-	-	-	-	-	-
PKA	O		O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O		O	O	O	O	O	O	O	(16)	5 pins	(17)	5 pins	-

1. Legend: Y = Yes (Enabled), O = Optional (Disabled by default, can be enabled by software), R = Data retained, - = Not available.
2. Available peripherals depend upon package, STM32WB35xx features one SPI, no LCD, no TSC and two wakeup pins. See *Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts* for more details.
3. Bluetooth® Low Energy not possible in this mode.
4. Standby with SRAM2a retention mode only.
5. Flash memory programming only possible in Range 1 voltage, not in Range 2 and not in Low Power mode.
6. The Flash memory can be configured in Power-down mode. By default, it is not in Power-down mode.
7. The SRAM clock can be gated on or off.

8. 当 PWR_CR3 寄存器的 RRS 位被设置时，SRAM2a 内容将被保存。 9. 只有 Stop 0 模式。在低功率运行时，SMPS 将自动切换到绕过或开路模式。 10. 一些具有从 Stop 模式唤醒功能的外围设备可以请求启用 HSI16。在这种情况下，外围设备会唤醒 HSI16，只为供求它的外围设备提供电力。当外围设备不再需要 HSI16 时，HSI16 将自动关闭。 11. 根据执行 RF 操作 (Tx 或 Rx) 的需求，HSE 可以被 RF 子系统使用。 12. MSI 最大频率。 13. 如果 RF 将被使用且 HSE 失败。 14. 在 Stop 模式下，UART 和 LPUART 接收是有效的，并在开始、地址匹配或接收帧事件时生成唤醒中断。 15. 在 Stop 模式下，I2C 地址检测是有效的，并在地址匹配时生成唤醒中断。 16. I/Os 可以在待机模式下配置为内部上拉、下拉或浮动。 17. I/Os 可以在关闭模式下配置为内部上拉、下拉或浮动，但退出关闭模式后配置将丢失。

Table 8. STM32WB55xx and STM32WB35xx modes overview

Mode	Regulator	CPU1	Flash	SRAM	Clocks	DMA and peripherals[1]	Wakeup source	Consumption[2]	Wakeup time
Run	Range 1	Yes	ON[3][4]	ON	Any	All	N/A	107 µA/MHz	N/A
	Range 2					All except RNG and USB-FS		100 µA/MHz	
LPRun	LPR	Yes	ON[3]	ON	Any except PLL	All except RF, RNG and USB-FS	N/A	103 µA/MHz	15.33 µs
Sleep	Range 1	No	ON[3]	ON[5]	Any	All	Any interrupt or event	41 µA/MHz	9 cycles
	Range 2					All except RNG and USB-FS		46 µA/MHz	
LPSleep	LPR	No	ON[3]	ON[5]	Any except PLL	All except RF, RNG and USB-FS	Any interrupt or event	45 µA/MHz	9 cycles
Stop 0	Range 1	No	OFF	ON	LSE, LSI, HSE[6], HSI16[7]	RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1[8] LPUART1[8] I2Cx (x=1, 3)[9] LPTIMx (x=1, 2), SMPS All other peripherals are frozen.	Reset pin, all I/Os, RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 LPUART1 I2Cx (x=1, 3) LPTIMx (x=1, 2) USB	100 µA	1.7 µs
	Range 2								
Stop 1	LPR	No	OFF	ON	LSE, LSI, HSE[6], HSI16[7]	RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1[8] LPUART1[8] I2Cx (x=1, 3)[9] LPTIMx (x=1, 2) All other peripherals are frozen.	Reset pin, all I/Os RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 LPUART1 I2Cx (x=1, 3) LPTIMx (x=1, 2) USB	9.2 µA w/o RTC 9.6 µA w RTC	4.7 µs

Table 8. STM32WB55xx and STM32WB35xx modes overview (continued)

Mode	Regulator	CPU1	Flash	SRAM	Clocks	DMA and peripherals(1)	Wakeup source	Consumption(2)	Wakeup time
Stop 2	LPR	No	OFF	ON	LSE, LSI	RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) LPUART1(8) I2C3(9) LPTIM1 All other peripherals are frozen.	Reset pin, all I/Os RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) LPUART1 I2C3 LPTIM1	1.85 µA w/o RTC 2.1 µA w RTC	5.71 µs
Standby	LPR	No	OFF	SRAM2a ON(10)	LSE, LSI	RF, BOR, RTC, IWDG All other peripherals are powered off. I/O configuration can be floating, pull-up or pull-down	RF, Reset pin 5 I/Os (WKUPx)(11) BOR, RTC, IWDG	0.32 µA w/o RTC 0.60 µA w RTC	51 µs
	OFF			OFF				0.11 µA w/o RTC 0.390 µA w RTC	
Shutdown	OFF	No	OFF	OFF	LSE	RTC All other peripherals are powered off. I/O configuration can be floating, pull-up or pull-down(12)	5 I/Os (WKUPx)(11), RTC	0.028 µA w/o RTC 0.315 µA w/ RTC	-

1. Available peripherals depend upon package, STM32WB35xx features one SPI, no LCD, no TSC and two wakeup pins. See *Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts* for more details.
2. Typical current at V_{DD} = 1.8 V, 25 °C. for STOPx, SHUTDOWN and Standby, else V_{DD} = 3.3 V, 25 °C.
3. The Flash memory controller can be placed in power-down mode if the RF subsystem is not in use and all the program is run from the SRAM.
4. Flash memory programming is only possible in Range 2 voltage.
5. The SRAM1 and SRAM2 clocks can be gated off independently.
6. HSE (32 MHz) automatically used when RF activity is needed by the RF subsystem.
7. HSI16 (16 MHz) automatically used by some peripherals.
8. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, Address match or Received frame event.
9. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
10. SRAM1 and SRAM2b are OFF.
11. I/Os with wakeup from Standby/Shutdown capability: PA0, PC13, PC12, PA2, PC5.
12. I/Os can be configured with internal pull-up, pull-down or floating but the configuration is lost immediately when exiting the Shutdown mode.

3.7.6 复位模式

为了改善复位时的消耗，复位期间和复位后的I/O状态是 “模拟状态” (I/O施密特触发器被禁用)。此外，当复位源是内部时，内部复位上拉会被关闭。

3.8 VBAT 操作

VBAT引脚允许从外部电池、外部超级电容或在没有外部电池和外部超级电容时从VDD供电设备VBAT领域(RTC, LSE 和 备份寄存器)。在VBAT 模式下，可用三个防篡改检测引脚。

VBAT 操作会在VDD不存在时自动激活。

内置了一个内部VBAT电池充电电路，当VDD存在时可以激活。

注意: 当微控制器仅从*VBAT*供电时，外部中断和*RTC*警报/事件不会退出*VBAT* 操作。

3.9 互连矩阵

多个外围设备之间有直接的硬件连接。这允许外围设备之间进行自主通信，从而节省CPU1 资源，并且随着减少电源消耗。此外，这些硬件连接导致了快速且可预测的延迟。

根据外围设备，这些互连可以在运行、睡眠模式、低功耗运行和睡眠模式、停止模式 0、停止模式 1 和停止模式 2 模式下运行。

表9. STM32WB55xx 和 STM32WB35xx CPU1 外围设备互连矩阵

Source	Destination	Action	Run	Sleep	Low-power run	Low-power	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADC1	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-
COMPx	TIM1 TIM2	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	Y(1)
ADC1	TIM1	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-

表9. STM32WB55xx 和 STM32WB35xx CPU1 外围设备互连矩阵 (继续)

Source	Destination	Action	Run	Sleep	Low-power run	Low-power	Stop 0 / Stop 1	Stop 2
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y(1)
All clock sources (internal and external)	TIM2 TIM16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-	-
CSS CPU (hard fault) SRAM (parity error) Flash memory (ECC error) COMPx PVD	TIM1 TIM16,17	Timer break	Y	Y	Y	Y	-	-
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y(1)
	ADC1	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 only.

3.10 时钟和启动

STM32WB55xx 和 STM32WB35xx 设备集成了多个时钟源：

• LSE: 32.768 kHz 外部晶体振荡器，用于提供准确的 RTC 和与其他嵌入式 RC 振荡器进行校准• LSI1: 32 kHz 上片低消耗 RC 振荡器• LSI2: 几乎 32 kHz，上片高稳定性 RC 振荡器，由 RF 子系统使用• HSE: 高质量 32 MHz 外部晶体振荡器，具有调节功能，RF 子系统需要• HSI16: 16 MHz 高精度上片 RC 振荡器• MSI: 100 kHz 到 48 MHz 多速上片低功耗 RC 振荡器，可以使用 LSE 信号进行调节• HSI48: 48 MHz 上片 RC 振荡器，用于无晶体 USB 目的

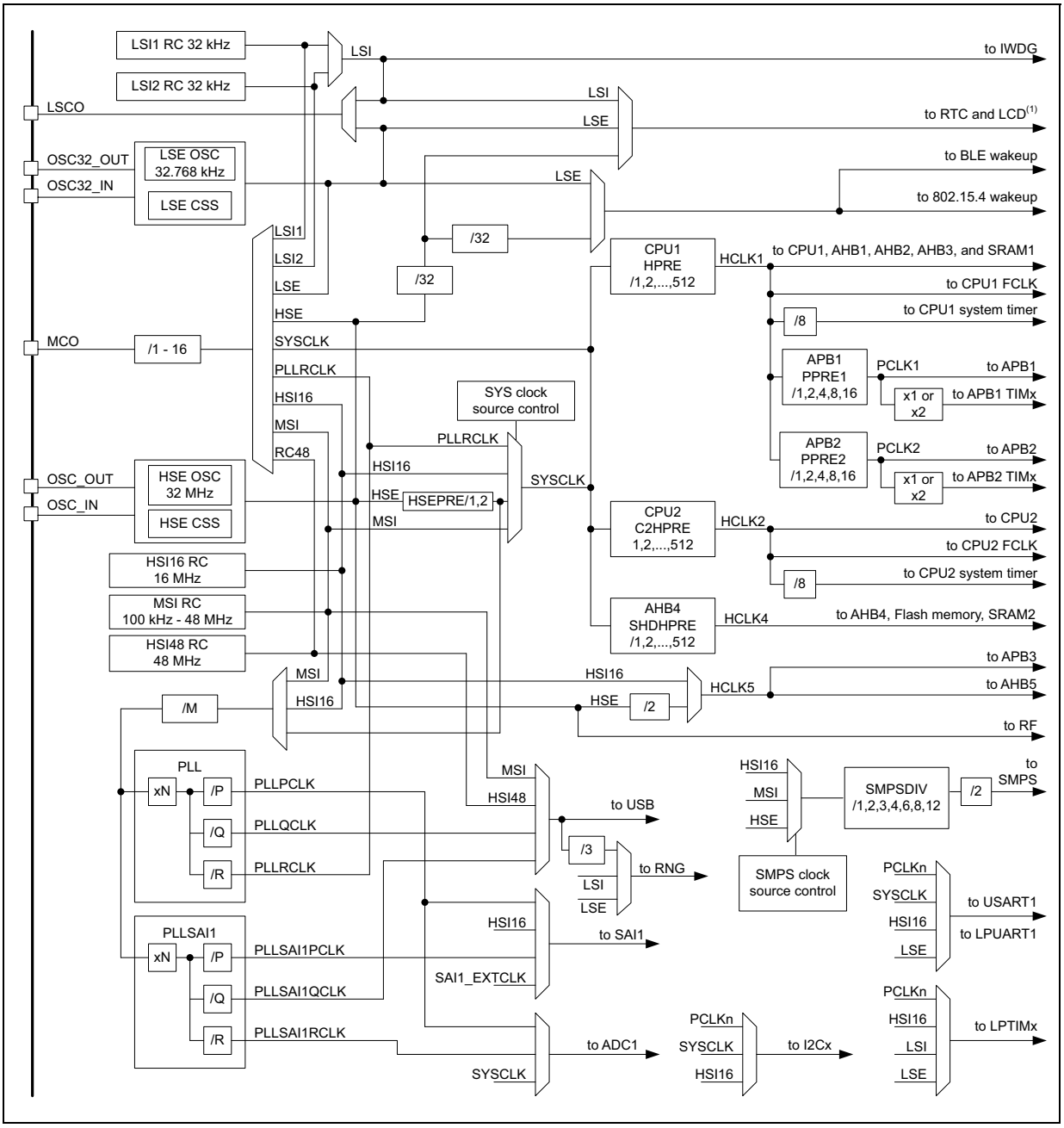
时钟控制器 (查看 图表 9) 将来自不同振荡器的时钟分发给核心和外围设备，包括 RF 子系统。它还管理时钟屏蔽以实现低功耗模式，并确保时钟的健壮性。它具有以下功能：

• **时钟预分频器:** 为了在速度和电流消耗之间取得最佳折衷，可以通过可编程预分频器调整发送送到 CPU 和外围设备的时钟频率• **安全时钟切换:** 可以在运行模式下通过配置寄存器动态安全地更改时钟源• **时钟管理:** 为了降低功率消耗，时钟控制器可以停止向核心、单独的外围设备或内存发送时钟• **系统时钟源:** 可以使用四种不同的时钟源驱动主时钟 SYSCLK:– 16 兆赫高速内置 RC 振荡器 (HSI16), 可以通过软件调节，能够为 PLL – 多速内置 RC 振荡器 (MSI), 可以通过软件调节，能够生成 12 种频率，从 100 kHz 到 48 MHz。当系统中可用一个 32.768 kHz 时钟源 (LSE) 时，MSI 频率可以通过硬件自动调节，以实现超过 ±0.25% 的精度。MSI 能够为 PLL – 系统 PLL，可以由 HSE, HSI16 或 MSI 饲料，最大频率为 64 MHz• **辅助时钟源:** 两个超低功耗时钟源，可以用于驱动 LCD 控制器和实时时钟：– 32.768 kHz 低速外部晶体 (LSE), 支持四种驱动模式。LSE 还可以配置为绕过模式以使用外部时钟– 32 kHz 低速内置 RC (LSI), 也用于驱动独立看门狗。LSI 时钟的精度为 ±5%。LSI 源可以是 LSI1 或 LSI2 上片振荡器• **外围设备时钟源:** 多个外围设备 (RNG, SAI, USARTs, I2C, LPTimers, ADC) 都具有独立的时钟，无论系统时钟如何。两个 PLL，每

STM32WB55xx STM32WB35xx具有三个独立输出，提供最高灵活性，可以为 ADC、RNG和SAI生成独立时钟。启动时钟：在复位后，微控制器默认以内部 4 MHz 时钟（MSI）重新启动。预分频比率和时钟源可以在代码执行开始后由应用程序更改。时钟安全系统：这一功能可以通过软件启用。如果发生 HSE 时钟故障，主时钟会自动切换到 HSI16，并且如果启用，则会生成软件中断。还可以检测 LSE 故障并生成中断。时钟输出能力：它将内部时钟之一输出给应用程序进行外部使用。低频时钟（LSIx, LSE）可用于 Stop 1 低功耗模式。LSCO：低速时钟输出：它在所有低功耗模式下输出 LSI 或 LSE，直至待机模式。

几个预分频器允许用户配置 AHB 频率、高速 APB(APB2) 和低速 APB (APB1) 域。AHB 和 APB 域的最大频率为 64 MHz。

图9. 时钟树



1. LCD 在 M32WB35xx 设备上不可用。

3.11 通用输入/输出 (GPIOs)

Each of the GPIO pins can be configured by software as output (推挽 or 开漏), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2总线.

输入/输出的alternate function configuration可以被锁定，如果需要，按照特定的序列进行，以避免在输入/输出寄存器中发生spurious writing。

3.12 直接内存访问控制器 (DMA) (DMA)

该设备集成了两个DMAs。参考 *表 10*以获取功能实现。

Direct memory access (DMA) 是用于在外围设备和内存之间以及在内存之间提供高速数据传输的。数据可以快速由 DMA 移动，而无需任何 CPU 行为。这将 CPU 资源保持自由，以便进行其他操作。

两个 DMA 控制器共有十四个通道，一个完整的交叉矩阵允许任何外围设备映射到可用的 DMA 通道上。每个 DMA 都有一个仲裁器来处理 DMA 请求之间的优先级。

The DMA supports:

• fourteen 配置的通道 (requests)• A full cross matrix between peripherals and all the DMA channels exist. There is also a HW trigger possibility through the DMAMUX.• Priorities between requests from DMA channels are software programmable (four levels consisting in very high, high, medium and low) or hardware in case of equality(request 1 has priority over request 2, etc.).• Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.• Support for circular buffer management.• Three event flags (DMA half transfer, DMA transfer complete and DMA transfer error)logically OR-ed together in a single interrupt request for each channel.• Memory-to-memory transfer.• Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers.• Access to Flash memory, SRAM, APB and AHB peripherals as source and destination.• Programmable number of data to be transferred: up to 65536.

表 10. DMA 实现

DMA features	DMA1	DMA2
Number of regular channels	7	7

A DMAMUX 块使得可以将任何外围设备源路由到任何 DMA 通道。

3.13 中断和事件

3.13.1 嵌套向量中断控制器 (NVIC)

这些设备嵌入了一个能够管理 16 优先级级别的嵌套向量中断控制器，能够处理高达 63 个可屏蔽中断通道加上 Cortex®-M4 的 16 中断线，其中包含 FPU。

NVIC 的优势如下：

• 紧密耦合的 NVIC 给出低延迟的中断处理• 中断入口向量表地址直接传递给核心• 允许早期处理中断• 处理晚到达的更高优先级中断

• 支持尾随链接• 自动保存处理器状态• 在中断退出时恢复中断入口，无指令开销

NVIC 硬件块提供了灵活的中断管理功能，具有最小的中断延迟。

3.13.2 扩展中断和事件控制器 (EXTI)

STM32WB55xx STM32WB35xx扩展中断和事件控制器 (EXTI) 通过可配置的直接事件输入来管理唤醒。它向电源控制提供 唤醒请求，并向 CPUx NVIC 生成中断请求，同时向 CPUx 事件输入生成事件。

可以配置的事件/中断来自能够生成脉冲的外围设备，使得可以选择事件/中断触发边缘和/或软件触发。

直接来自具有自身清除机制的外围设备的事件/中断。

3.14 模拟-数字转换器 (ADC)

该设备集成了具有以下功能的逐级逼近模拟到数字转换器：

• 12-bit原生分辨率，带有内置校准• 最高16位分辨率，256超采样比例• 4.26 Msps最大转换速率，全分辨率– 采样时间低至39 ns– 低分辨率下的转换速率增加 (最高6位分辨率为7.11 Msps)• 最高十六个外部通道和三个内部通道：内部参考电压，温度传感器• 单端和差分模式输入• 低功耗设计– 在低转换速率下可进行低电流运行(消耗随速度线性降低)– 双时钟域架构：ADC速度与CPU频率无关• 非常灵活的数字接口– 单脉冲或连续/不连续序列器基于扫描模式：两组模拟信号转换可以编程来区分背景和高优先级实时转换– ADC支持多个触发输入用于与片上计数器和外部信号同步– 结果存储在三个数据寄存器或使用DMA控制器支持的SRAM中

– 数据预处理：左右对齐和每通道偏移补偿– 内置过采样单元用于增强的信号噪声比– 通道可编程采样时间– 三个模拟看门狗用于自动电压监控，生成中断和为选择的计时器设置触发– 硬件助手准备注入通道的上下文以允许快速上下文切换

3.14.1 温度传感器

温度传感器 (TS) 生成一个与温度线性变化的电压 VTS。

温度传感器内部连接到 ADC1_IN17 输入通道，用于将传感器输出电压转换为数字值。

为了提高温度传感器测量的精度，每个设备都由 ST 个工厂校准。温度传感器工厂校准数据是

存储在系统内存区域中，以只读模式访问。

表11. 温度传感器校准值

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.14.2 内部电压参考 (VREFINT) (VREFINT)

内部电压参考 (VREFINT) (VREFINT) 为 ADC 和 比较器 提供一个稳定的 (带隙) 电压输出。VREFINT 内部连接到 ADC1_IN0 输入通道。VREFINT 的精确电压由 ST 在生产测试期间为每个部件 individually量并存储在系统内存区域中。它以只读模式访问。

表 12. 内部电压参考校准值

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.6 V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.15 电压参考缓冲器 (VREFBUF)

STM32WB55xx 设备集成了一个电压参考缓冲器，可以作为 ADC 的电压参考使用，并且通过 VREF+ 接口也可以作为外部组件的电压参考。内部电压参考缓冲器支持两个电压：

- 2.048
V• 2.5 V

STM32WB55xx STM32WB35xx3.16 Comparators (COMP)当内部电压参考缓冲器关闭时，可以通过 VREF+ pin 提供外部电压参考。VREF+ pin 与 UFQFPN48 封装上的 VDDA 进行双接触，因此内部电压参考缓冲器不可用于专门的引脚，但用户仍然可以使用 VDDA 值。

3.16 比较器 (比较器)

STM32WB55xx 和 STM32WB35xx 设备集成了两个全范围比较器，具有可编程参考电压 (内部或外部)、滞回路和速度 (低功耗的低速) ，并且可以选择输出极性。

The reference voltage can be one of the following:

- 外部I/O• 内部参考电压或分数 (1/4, 1/2, 3/4).

所有比较器都可以从停止模式中唤醒，生成中断并为定时器产生中断，并且还可以组合成一个窗口比较器。

3.17 触摸感应控制器 (TSC)

触摸感应控制器提供了一种简单的解决方案，用于向任何应用程序添加电容式感应功能。电容式感应技术能够检测手指靠近受绝缘体（如玻璃或塑料）保护的电极附近的存在。手指引入的电容变化 (或任何导电对象)通过基于表面电荷传输获取原则的经过验证的实现进行测量。

触摸感应控制器由 STMTouch 触摸感应固件库 (免费使用) 完全支持，并在最终应用程序中启用可靠的触摸感应功能。

触摸传感器控制器的主要功能如下：

- 成熟而稳定的表面电荷传输获取原则
- 支持高达18个电容式传感器通道
- 最多可以并行获取六个电容式传感器通道，提供非常好的响应时间
- 扩频功能，以在嘈杂环境中提高系统稳定性
- 完全硬件管理电荷转移采集序列
- 可编程电荷转移频率
- 可编程采样电容器I/O引脚
- 可编程通道I/O引脚
- 可编程最大计数值，避免在通道故障时进行长时间采集
- 专用的采集结束和最大计数错误标志带中断能力
- 一个采样电容器可用于高达三个电容式传感器通道，以减少系统组件
- 兼容近距离、触摸按键、线性和旋转触摸传感器实现
- 设计用于与 STMTouch 触摸感应固件库一起运行

注意：电容式传感器通道的数量取决于封装 *(* 不可用于 *QFPN48)* 并受到 *I/O* 可用性的限制。

3.18 液晶显示控制器 (LCD)

STM32WB55xx 设备集成了具有以下特性的 LCD 控制器：

• 高度灵活的帧率控制。• 支持静态、1/2、1/3、1/4和1/8占空比。• 支持静态、1/2、1/3和1/4偏置。• 双缓冲存储允许应用程序件随时更新LCD_RAM 寄存器中的数据，而无需影响显示的数据完整性。– LCD 数据 RAM 最大为 16 x 32 位寄存器，包含像素信息。(active/inactive)• 软件可选择的 LCD 输出电压。(对比度。) 从 VLCDmin 到 VLCDmax。• 无需外部模拟组件：– 内置了升压转换器来生成内部 VLCD 电压，高于 VDD。(最高到 3.6 V 如果 VDD > 2.0 V。)– 软件可选择外部和内部 VLCD 电压来源。在使用外部来源时，内部升压电路将被禁用以降低功耗。– 内置了阻性网络来生成中间 VLCD 电压。– 阻性网络的结构可以通过软件进行配置以适应 LCD 面板所需的电容充电，从而降低功耗。– 集成的电压输出缓冲器用于提高 LCD 驱动能力。• 对比度可以使用两种不同的方法调整：– 当使用内部升压转换器时，软件可以调整 VLCD 在 VLCDmin 和 VLCDmax 之间。– 可编程死时间。(最高到八个相反转换周期。) 帧之间。• 完全支持低功耗模式：LCD 控制器可以处于睡眠模式、 低功耗运行、低功耗休眠和停止模式，或者可以完全禁用以降低功耗。• 内置了相反转换以降低功耗和 EMI。(电磁干扰。).• 帧开始中断用于在更新 LCD 数据 RAM 时同步软件。• 闪烁功能：– 1, 2, 3, 4, 8 或所有像素都可以编程在可配置的频率下闪烁。– 软件可调整的闪烁频率可以实现约 0.5 Hz、1 Hz、2 Hz 或 4 Hz。

用于 LCD 段和公共引脚应配置为 GPIO 替代功能，未使用的段和公共引脚可以用于通用输入/输出或其他外设替代功能。

Note: 当 *LCD* 依赖内部升压转换器时，*VLCD* 引脚应连接到 *VSS*，并附上一个电容器。其典型值是 *1 µF*。

3.19 真随机数生成器 (RNG)

这些设备集成了一个真正的 RNG，它通过集成的模拟电路生成 32 位随机数。

3.20 定时器和看门狗

STM32WB55xx 和 STM32WB35xx 包含一个高级 16 位定时器，一个通用 32 位定时器，两个 16 位基本定时器，两个 低功耗计数器，两个 看门狗定时器和一个 SysTick 定时器。表 13比较了高级控制、通用和基本定时器的功能。

表 13. 定时器功能

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1	16-bits	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General purpose	TIM2	32-bits	Up, down, Up/down			4	No
General purpose	TIM16	16-bits	Up			2	1
General purpose	TIM17	16-bits	Up			2	1
Low power	LPTIM1 LPTIM2	16-bits	Up			1	1

3.20.1 高级控制定时器 (TIM1)

高级控制定时器可以看作是在六个通道上复用的三相 PWM。它们具有可编程插入死时间的互补 PWM 输出。它们也可以看作是完整的通用计时器。四个独立通道可以用于：

- 输入捕获• 输出比较• PWM 生成 (边缘或中心对齐模式) 具全范围调制能力 (0 到 100%)• 单脉冲模式输出

在调试模式下，高级控制定时器计数器可以被冻结，PWM 输出可以被禁用以关闭由这些输出驱动的任何电源开关。

许多功能与通用 TIMx 定时器共享(描述第 3.20 节2) 使用相同的架构，因此高级控制定时器可以通过定时器链接功能与 TIMx 定时器协同工作进行进行同步或事件链。

3.20.2 通用定时器 (TIM2, TIM16, TIM17)

STM32WB55xx 和 STM32WB35xx 中嵌入了多达三个可以同步的通用定时器(参见 表 13以查看差异). 每个通用定时器都可以用于生成 PWM 输出，或者作为简单的时间基准。

- TIM2– 完整功能的通用计时器

– 具有四个独立通道，用于输入捕获/输出比较、PWM或单脉冲模式输出。可以一起工作，或者通过定时器链接功能与其他通用计时器进行同步或事件链。– 计数器可以在调试模式下冻结。– 独立的DMA请求生成，支持四象限编码器。

- TIM16和TIM17
  – 通用计时器具有中等级特性:– 16-bit 自动重新加载递增计数器和 16位预分频器.– 1 通道和 1 个补充通道.– 所有通道都可以用于输入捕获/输出比较、PWM 或 脉冲模式输出.– 定时器可以通过定时器链接功能一起工作，以实现同步或事件链。定时器具有独立的 DMA 请求生成.– 计数器可以在调试模式下冻结。

3.20.3 低功耗计时器 (LPTIM1 和 LPTIM2)

这些设备集成了两个 低功耗计时器，如果它们由 LSE、LSIx 或外部时钟驱动，则在停止模式下运行独时时。它们能够从停止模式唤醒系统。

LPTIM1 在停止模式 0、停止模式 1 和停止模式 2 下有效。

LPTIM2 在停止模式 0 和停止模式 1 下有效。

低功耗计时器支持以下功能：

- 16-bit up counter with 16位自动重载寄存器• 16-bit compare register• 可配置输出：脉冲，PWM• 连续/单脉冲模式• 可选的软件/硬件输入触发• 可选的时钟源– 内部时钟源：LSE，LSI1或LSI2，HSI16或APB 时钟– 通过LPTIM输入的外部时钟源 (即使没有内部时钟源运行也能工作，由脉冲计数器应用使用)• 可编程数字杂散滤波器• 编码器模式 (仅适用于LPTIM1)

3.20.4 独立看门狗 (IWDG)

独立看门狗基于一个12位下计数器和8位预分频器。它从独立的32 kHz内部RC LSI(运行) 供电，并且因为它独立于主时钟运行，所以可以在停止和待机模式下运行。它可以作为看门狗来复位设备，当出现问题时，或者作为应用程序超时管理的自由运行定时器。它可以通过选项字节进行硬件或软件配置。计数器可以在调试模式下冻结。

3.20.5 系统窗口看门狗 (系统窗口看门狗)

窗口看门狗基于一个可以设置为自由运行的7位下计数器。它可以用作看门狗来在发生问题时复位设备。它从主时钟获取时钟信号。它具有早期警告中断功能，计数器可以在调试模式下冻结。

3.20.6 SysTick 定时器

这个计数器专门用于实时操作系统，但也可以作为标准下降计数器使用。它具有：

- a 24位下计数器• 自动重载功能• a 当计数器达到 0 时的可屏蔽的系统中断生成• a 可编程的时钟源.

3.21 实时时钟 (RTC) 和 备份寄存器

STM32WB55xx STM32WB35xx3.21 实时钟 (RTC) 和备份寄存器RTC 是一个独立的 BCD 计时器/计数器，支持以下功能：

STM32WB55xx STM32WB35xx3.21 实时钟 (RTC) 和备份寄存器包含亚秒、秒、分钟、小时 (12 或 24 格式)，星期、日期、月份、年份，以 BCD (（二进制编码的十进制）) 格式存储。• 对于 28 29 (（闰年）)、30 和 31 天的月份进行自动校正。• 两个可编程的报警。• 从 1 到 32767 RTC 时钟脉冲的即时校正。这可以用来将其与主时钟同步。• 参考时钟检测：一个更精确的秒源时钟 (50 或 60 Hz) 可以用来提高日历的精度。• 具有 0.95 ppm 分辨率的数字校准电路，用于补偿氧化铝晶体的不准确性。• 三个可编程滤波器的防篡改检测引脚。• 时间戳功能，可以用来保存日历内容。此功能可以由 timestamp 引脚上的事件、篡改事件或切换到 VBAT 模式触发。• 17-bit 自动加载唤醒计数器 (WUT) 用于具有可编程分辨率和周期的周期性事件。

RTC 和 20 个备份寄存器通过一个开关供电，该开关从 VDD 供电 (（存在) ）或 VBAT 引脚供电。

备份寄存器是 32 位寄存器，用于在没有 VDD 电源时存储 80 字节的用户应用数据。它们不会被系统复位或电源复位复，也不会在设备从 待机模式 或 关闭模式 中唤醒时重置。

RTC 时钟源可以是：

- 一 2.768 kHz 外部晶体 (LSE)• 一个外部共振器或挤器 (LSE)• 其中一个内部低功率 RC 振荡器 (LSI1 或 LSI2，典型频率 32 kHz)• 高速外部时钟 (HSE) 除以 32。

RTC 在 VBAT 模式下以及在 LSE 调制时的所有低功耗模式下都是可用的。当由 LSIs 调制时，RTC 在 VBAT 模式下不可用，但在所有低功耗模式下均可用，除了关闭模式。

所有 RTC 事件 (报警、唤醒计数器、时间戳或篡改) 都可以生成中断并从低功耗模式唤醒设备。

3.22 互联互通电路接口 (I2C)

这些设备集成了两个 I2C。参考 *表14*以获取功能实现。

I2C总线接口处理微控制器与串行I2C总线之间的通信。它控制所有I2C总线特定的序列化、协议、仲裁和时序。

The I2C peripheral supports:

STM32WB55xx STM32WB35xx3.22 Inter-integrated circuit interface (I2C) specification and user manual rev. 5 compatibility:从机和主机模式，多主机能力标准模式 SM，比特率高达 100 kbit/s快速模式 Fm，比特率高达 400 kbit/s快速模式加 Fm，比特率高达 1 Mbit/s且具有 20 mA 输出驱动的输入/输出

s

STM32WB55xx STM32WB35xx3.22 Inter-integrated circuit interface (I2C)– 7-bit 和 10-bit 地址模式，多个 7-bit 从机地址 – 可编程设置和保持时间 – 可选的时钟拉长 • 系统管理总线 (SMBus) 规范 rev 2.0 兼容性： – 硬件 PEC (数据包错误检测) 与 ACK 控制一起的生成和验证 – 地址分辨协议 (ARP) 支持 – SMBus 警告 • 电源管理协议 (PMBus ™) 规范 rev 1.1 兼容性 • 独立时钟：选择独立时钟源，使 I2C 通信速度可以独立于 PCLK 重编程。参考 图9：时钟树。 • 在地址匹配时从停止模式唤醒 • 可编程模拟和数字噪声过滤器 • 1字节缓冲区具有 DMA 能力

表14. I2C 实现

I2C features(1)	I2C1	I2C3
Standard-mode (up to 100 kbit/s)	X	X
Fast-mode (up to 400 kbit/s)	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X
Programmable analog and digital noise filters	X	X
SMBus/PMBus hardware support	X	X

表14. I2C 实现 (继续)

I2C features(1)	I2C1	I2C3
Independent clock	X	X
Wakeup from Stop 0 / Stop 1 mode on address match	X	X
Wakeup from Stop 2 mode on address match	-	X

1. X: supported

3.23 通用同步/异步接收-发送器 (USART)

设备集成了一个通用同步接收发送器。

此接口提供异步通信，IrDA SIR ENDEC 支持，多处理器通信模式，单线半双工通信模式，并具有 LIN 主从机功能。它提供 CTS 和 RTS 信号的硬件管理，并启用 RS485 驱动器。

USART 能够以高达 4 Mbit/s 的速度进行通信，并提供符合 ISO 7816 的智能卡模式和 SPI 相似通信能力。

USART 支持 (SPI 模式)的同步操作，并可作为 SPI 主机使用。

USART 具有与 CPU 时钟独立的时钟域，允许在使用高达 200 kbaud 的波特率时从停止模式唤醒 MCU。停止模式的唤醒事件是可编程的，并且可以是：

- 起始位检测• 任何接收数据帧
- 一个特定的编程数据帧。

USART 接口可以由 DMA 控制器提供服务。

3.24 低功耗异步接收发送器(LPUART)

该设备集成了一个低功耗UART，支持最小功率消耗的异步串行通信。LPUART 支持半双工单线通信和调制解调器操作(CTS/RTS)，允许多处理器通信。

LPUART 的时钟域与 CPU 时钟独立，并且可以通过波特率高达 220 kbaud 来唤醒系统从停止模式中恢复。停止模式的唤醒事件是可编程的，并且可以是：

- 起始位检测• 任何接收数据帧
- 一个特定的编程数据帧。

只需要一个 32.768 kHz 时钟(LSE) 才能进行高达 9600 波特率的 LPUART 通信。因此，即使在停止模式下，LPUART 也可以等待入站帧，同时具有

极低的能量消耗。更高速度的时钟可以用于实现更高的波特率。

LPUART接口可以由DMA 控制器提供服务。

3.25 串行外围接口 (SPI1, SPI2)

两个 SPI 接口支持主模式下的最高 32 Mbit/s 和从模式下的最高 24 Mbit/s，半双工、全双工和单工模式。3位预分频器提供 8 个主模式频率，帧大小可配置为 4 位到 16 位。SPI 接口支持 NSS脉冲模式、TI模式和硬件CRC计算。

SPI 接口可以由 DMA 控制器服务。

3.26 串行音频接口 (SAI1)

设备集成了一个支持全双工音频操作的双通道SAI外围设备。SAI总线接口处理微控制器与串行音频协议之间的通信。

SAI 外围设备支持：

- 一个独立的音频子块，可以是发射器或接收器，具有相应的FIFO• 8-字集成FIFOs
- 同步或异步模式• 主或从配置• 在音频子块配置为主模式时，时钟生成器可用于目标独立的音频频率采样• 数据大小可配置：8-, 10-, 16-, 20-, 24-, 32-bit• 具有大量可配置性和灵活性的外围设备，允许将其作为示例目标以下音频协议：I2S, LSB或MSB对齐, PCM/DSP, TDM, AC’97 以及 SPDIF 输出 • 最多可用 16 个插槽，具有可配置的大小，并且可以选择哪些在音频帧中激活• 每帧的比特数可能可配置• 帧同步有效水平可配置 (偏移, 比特长度, 水平)• 插槽中的首个有效比特位置可配置• LSB先或MSB先用于数据传输• 静音模式• 立体声/单声道音频帧能力• 通信时钟扫描边缘可配置 (SCK)• 如果启用则存在的错误标志与相关的中断– 溢出和未溢出检测– 从机模式下的预期帧同步信号检测– 从机模式下的延迟帧同步信号检测– Codec不准备好处理AC’97 接收模式

• 启用时的中断源：– 错误– FIFO请求• DMA接口使用两个专用通道访问SAI音频子块的专用集成FIFO。

PDM (脉冲密度调制) 块允许用户管理多达三对数字麦克风(，使用两个不同的时钟)。该块通过可编程延迟线进行右侧和左侧麦克风 解交错和时间对齐，以便正确地为SAI提供输入。

3.27 四线SPI 内存接口 (四线式 SPI 内存接口)

Quad-SPI 是一种专门用于单个、双重或四线 SPI 闪存内存的通信接口。它可以在以下三种模式中运行：

• 间接模式：所有操作都使用 QUADSPI 寄存器进行• 状态轮询模式：外部内存状态寄存器定期读取，并且可以生成中断

内存映射模式：外部 闪存内存被映射，并且系统看到它就像是一个内部内存。此模式可以用于 Execute In Place (XIP)

Quad-SPI 接口支持：

• 三种功能模式：间接、状态轮询和内存映射• SDR 和 DDR 支持• 完全可编程的指令，用于间接和内存映射模式• 完全可编程的帧格式，用于间接和内存映射模式• 每个以下五个阶段都可以独立配置 (使能、长度、单/双/四线通信)– 指令阶段– 地址阶段– 交替字节阶段– 哨兵周期阶段– 数据阶段• 集成 FIFO 用于接收和传输• 8, 16, 和 32 位数据访问被允许• DMA 频道用于间接模式操作• 可编程的屏蔽，用于外部闪存内存标志管理 • 超时管理 • 基于 FIFO 阈值、超时、状态匹配、操作完成和访问错误的中断生成

3.28 开发支持

3.28.1 串行线 JTAG 调试端口 (SWJ-DP)

Arm® 串行线 JTAG 调试端口是嵌入式的，它是一个结合了 JTAG 和 串行调试 的端口，可以连接连接连接行调调或或或 或探到目标。

调试使用两个引脚而不是 JTAG 需要的五个引脚进行。然后，JTAG 引脚可以作为具有替代功能的 GPIOs 被重用：JTAG TMS 和 TCK 引脚分别与 SWDIO 和 SWCLK 共享，而在 TMS 引脚上的特定序列用于在 JTAG-DP 和 SW-DP 之间切换。

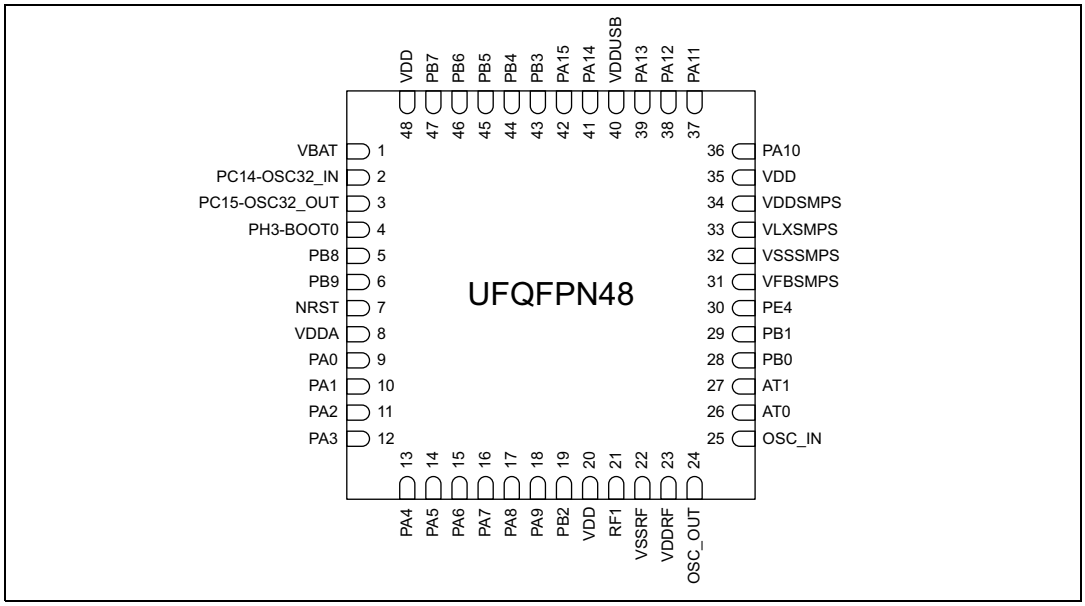
3.28.2 Embedded Trace Macrocell™

Arm嵌入式跟踪宏单元提供了对CPU核心内部指令和数据流的更高可见性，通过从STM32WB55xx通过少量ETM引脚以非常高的速率流动压缩数据到外部硬件跟踪分析器。实时指令和数据流可以被记录并格式化用于显示在运行调试软件的主机计算机上。TPA硬件由常见的开发工具供应商提供。

嵌入式跟踪宏单元与第三方调试软件工具一起工作。

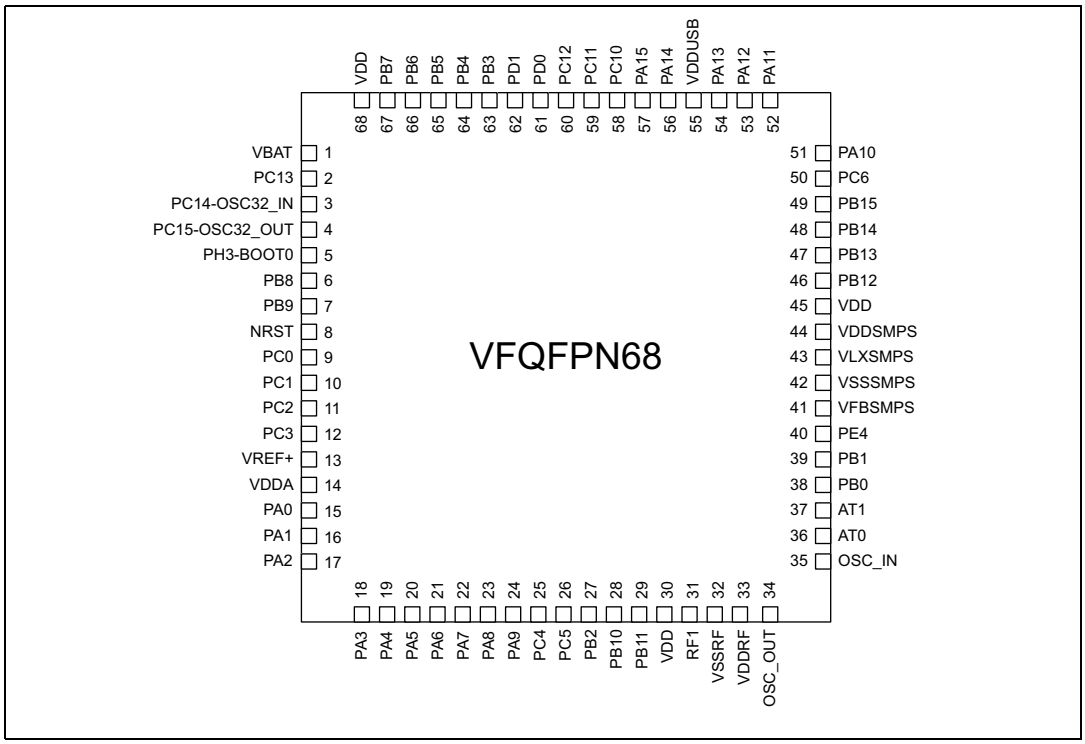
4 引脚布局和引脚描述

图10. STM32WB55Cx 和 STM32WB35Cx UFQFPN48 引脚排列(1)(2)



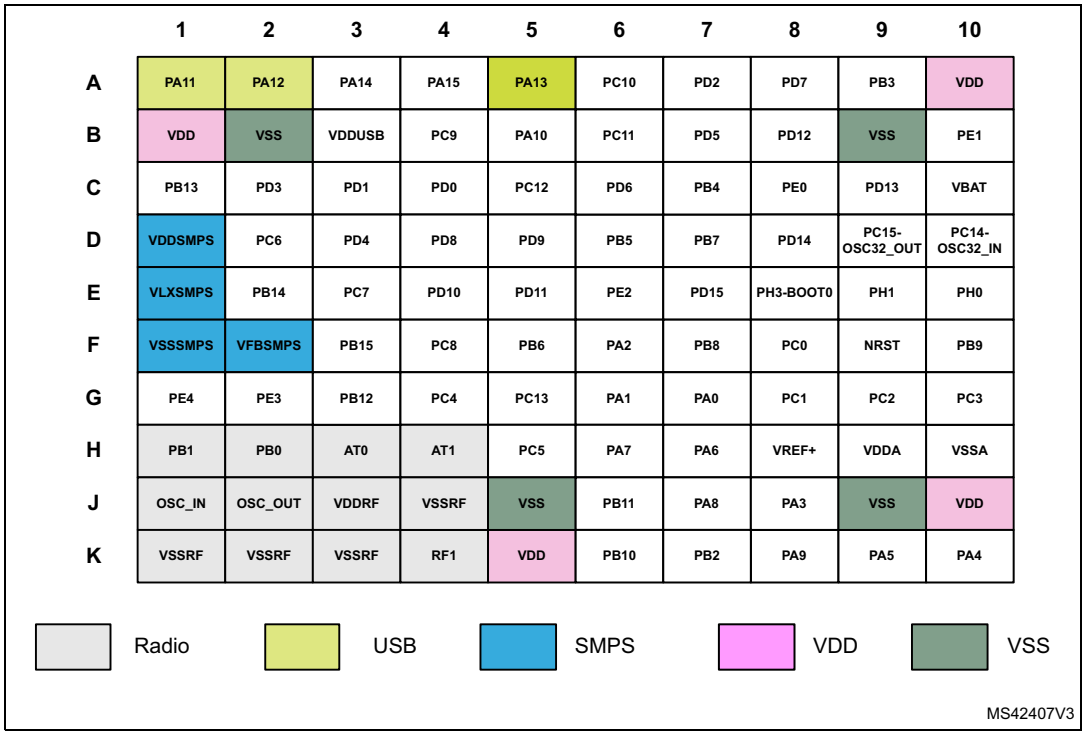
1. 上图显示封装顶视。2. 暴露的铜箔必须连接到地平面。

图11. STM32WB55Rx VFQFPN68 引脚排列(1)(2)



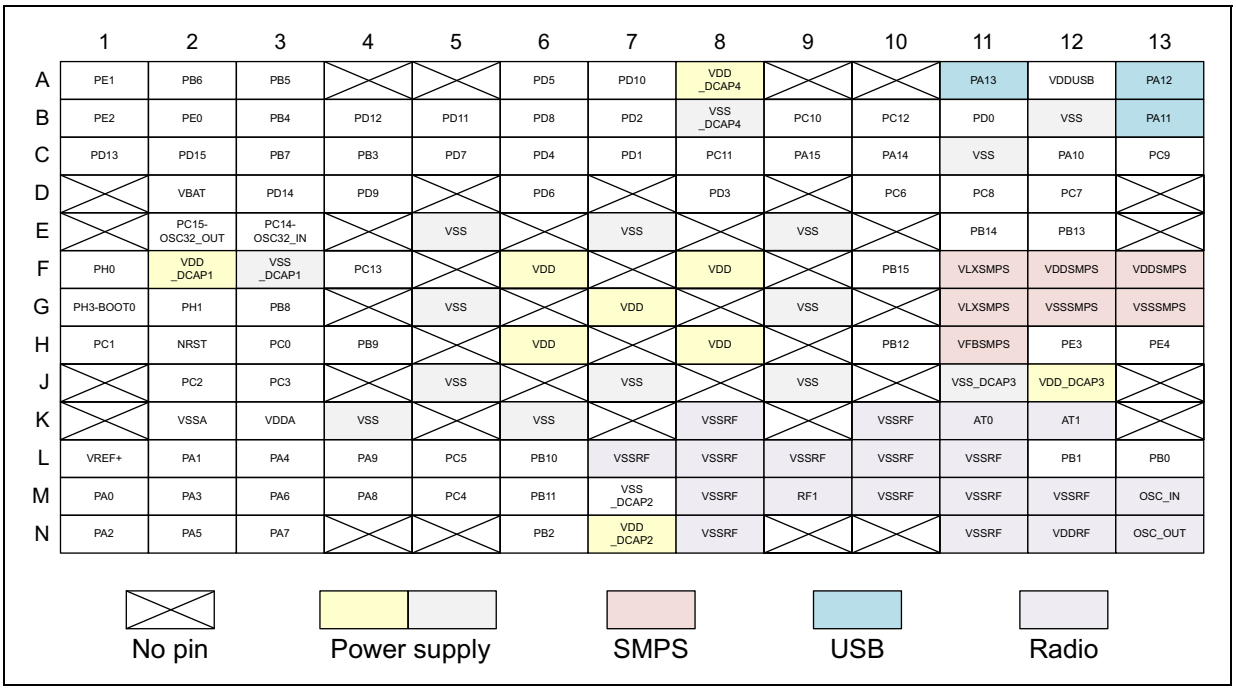
1. 上图显示封装顶视。2. 暴露的铜箔必须连接到地平面。

图12. STM32WB55Vx WLCSP100 球阵排列(1)



1. 上图显示的是封装顶视。

图13. STM32WB55Vx UFBGA129 球阵排列(1)



1. 上述图示封装顶视。

表15. 在引脚表中使用的图例/缩写

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		RF	RF I/O
		RST	Bidirectional reset pin with weak pull-up resistor
		Option for TT or FT I/Os	
		_f (1)	I/O, Fm+ capable
		_l (2)	I/O, with LCD function supplied by V_{LCD}
		_u(3)	I/O, with USB function supplied by V_{DDUSB}
		_a(4) (5)	I/O, with Analog switch function supplied by V_{DDA}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 16* are: FT_f, FT_fa, FT_fl, FT_fla.
2. The related I/O structures in *Table 16* are: FT_l, FT_fl, FT_lu.
3. The related I/O structures in *Table 16* are: FT_u, FT_lu.
4. The related I/O structures in *Table 16* are: FT_a, FT_la, FT_fa, FT_fla, TT_a, TT_la.
5. Analog switch for the TSC function is supplied by V_{DD}.

表16. STM32WB55xx 引脚和球定义

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
-	-	C8	B2	PE0	I/O	FT_l	-	TIM1_ETR, TSC_G7_IO3, LCD_SEG36, TIM16_CH1, CM4_EVENTOUT	-
-	-	B10	A1	PE1	I/O	FT_l	-	TSC_G7_IO2, LCD_SEG37, TIM17_CH1, CM4_EVENTOUT	-
-	-	E6	B1	PE2	I/O	FT_l	-	TRACECK, SAI1_PDM_CK1, TSC_G7_IO1, LCD_SEG38, SAI1_MCLK_A, CM4_EVENTOUT	-
-	-	C9	C1	PD13	I/O	FT_l	-	TSC_G6_IO4, LCD_SEG33, LPTIM2_OUT, CM4_EVENTOUT	-
-	-	D8	D3	PD14	I/O	FT_l	-	TIM1_CH1, LCD_SEG34, CM4_EVENTOUT	-
-	-	E7	C2	PD15	I/O	FT_l	-	TIM1_CH2, LCD_SEG35, CM4_EVENTOUT	-
1	1	C10	D2	VBAT	S	-	-	-	-
-	2	G5	F4	PC13	I/O	FT	(1) (2)	CM4_EVENTOUT	RTC_TAMP1/RTC_TS/ RTC_OUT/WKUP2
2	3	D10	E3	PC14-OSC32_IN	I/O	FT	(1) (2)	CM4_EVENTOUT	OSC32_IN
3	4	D9	E2	PC15-OSC32_OUT	I/O	FT	(1) (2)	CM4_EVENTOUT	OSC32_OUT
-	-	-	E5	VSS	S	-	-	-	-
-	-	-	F6	VDD	S	-	-	-	-
-	-	E10	F1	PH0	I/O	FT	-	CM4_EVENTOUT	-
-	-	E9	G2	PH1	I/O	FT	-	CM4_EVENTOUT	-
4	5	E8	G1	PH3-BOOT0	I/O	FT	-	CM4_EVENTOUT, LSCO(3)	-
5	6	F7	G3	PB8	I/O	FT_fl	-	TIM1_CH2N, SAI1_PDM_CK1, I2C1_SCL, QUADSPI_BK1_IO1, LCD_SEG16, SAI1_MCLK_A, TIM16_CH1, CM4_EVENTOUT	-

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
6	7	F10	H4	PB9	I/O	FT_fla	-	TIM1_CH3N, SAI1_PDM_DI2, I2C1_SDA, SPI2_NSS, IR_OUT, TSC_G7_IO4, QUADSPI_BK1_IO0, LCD_COM3, SAI1_FS_A, TIM17_CH1, CM4_EVENTOUT	-
7	8	F9	H2	NRST	I/O	RST	-	-	-
-	9	F8	H3	PC0	I/O	FT_fla	-	LPTIM1_IN1, I2C3_SCL, LPUART1_RX, LCD_SEG18, LPTIM2_IN1, CM4_EVENTOUT	ADC1_IN1
-	10	G8	H1	PC1	I/O	FT_fla	-	LPTIM1_OUT, SPI2_MOSI, I2C3_SDA, LPUART1_TX, LCD_SEG19, CM4_EVENTOUT	ADC1_IN2
-	11	G9	J2	PC2	I/O	FT_la	-	LPTIM1_IN2, SPI2_MISO, LCD_SEG20, CM4_EVENTOUT	ADC1_IN3
-	-	-	E7	VSS	S	-	-	-	-
-	-	-	H6	VDD	S	-	-	-	-
-	12	G10	J3	PC3	I/O	FT_a	-	LPTIM1_ETR, SAI1_PDM_DI1, SPI2_MOSI, LCD_VLCD, SAI1_SD_A, LPTIM2_ETR, CM4_EVENTOUT	ADC1_IN4
-	-	H10	K2	VSSA	S	-	-	-	-
-	13	H8	L1	VREF+	S	-	-	-	VREFBUF_OUT
8	14	H9	K3	VDDA	S	-	(4)	-	-
-	-	J9	E9	VSS	S	-	-	-	-
-	-	J10	F8	VDD	S	-	-	-	-
9	15	G7	M1	PA0	I/O	FT_a	-	TIM2_CH1, COMP1_OUT, SAI1_EXTCLK, TIM2_ETR, CM4_EVENTOUT	COMP1_INM, ADC1_IN5, RTC_TAMP2/WKUP1
10	16	G6	L2	PA1	I/O	FT_la	-	TIM2_CH2, I2C1_SMBA, SPI1_SCK, LCD_SEG0, CM4_EVENTOUT	COMP1_INP, ADC1_IN6

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
11	17	F6	N1	PA2	I/O	FT_la	-	LSCO(3), TIM2_CH3, LPUART1_TX, QUADSPI_BK1_NCS, LCD_SEG1, COMP2_OUT, CM4_EVENTOUT	COMP2_INM, ADC1_IN7, WKUP4
12	18	J8	M2	PA3	I/O	FT_la	-	TIM2_CH4, SAI1_PDM_CK1, LPUART1_RX, QUADSPI_CLK, LCD_SEG2, SAI1_MCLK_A, CM4_EVENTOUT	COMP2_INP, ADC1_IN8
13	19	K10	L3	PA4	I/O	FT_a	-	SPI1_NSS, SAI1_FS_B, LPTIM2_OUT, LCD_SEG5, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN9
14	20	K9	N2	PA5	I/O	FT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, LPTIM2_ETR, SAI1_SD_B, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN10
15	21	H7	M3	PA6	I/O	FT_la	-	TIM1_BKIN, SPI1_MISO, LPUART1_CTS, QUADSPI_BK1_IO3, LCD_SEG3, TIM16_CH1, CM4_EVENTOUT	ADC1_IN11
16	22	H6	N3	PA7	I/O	FT_fla	-	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, LCD_SEG4, COMP2_OUT, TIM17_CH1, CM4_EVENTOUT	ADC1_IN12
17	23	J7	M4	PA8	I/O	FT_la	-	MCO, TIM1_CH1, SAI1_PDM_CK2, USART1_CK, LCD_COM0, SAI1_SCK_A, LPTIM2_OUT, CM4_EVENTOUT	ADC1_IN15
18	24	K8	L4	PA9	I/O	FT_fla	-	TIM1_CH2, SAI1_PDM_DI2, I2C1_SCL, SPI2_SCK, USART1_TX, LCD_COM1, SAI1_FS_A, CM4_EVENTOUT	COMP1_INM, ADC1_IN16
-	25	G4	M5	PC4	I/O	FT_la	-	LCD_SEG22, CM4_EVENTOUT	COMP1_INM, ADC1_IN13
-	-	-	F3	VSS_DCAP1	S	-	-	-	-
-	-	-	G7	VDD	S	-	-	-	-

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
-	26	H5	L5	PC5	I/O	FT_la	-	SAI1_PDM_DI3, LCD_SEG23, CM4_EVENTOUT	COMP1_INP, ADC1_IN14, WKUP5
19	27	K7	N6	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, SPI1_NSS, LCD_VLCD, SAI1_EXTCLK, CM4_EVENTOUT	COMP1_INP
-	28	K6	L6	PB10	I/O	FT_fl	-	TIM2_CH3, I2C3_SCL, SPI2_SCK, LPUART1_RX, TSC_SYNC, QUADSPI_CLK, LCD_SEG10, COMP1_OUT, SAI1_SCK_A, CM4_EVENTOUT	-
-	29	J6	M6	PB11	I/O	FT_fl	-	TIM2_CH4, I2C3_SDA, LPUART1_TX, QUADSPI_BK1_NCS, LCD_SEG11, COMP2_OUT, CM4_EVENTOUT	-
-	-	-	G5	VSS	S	-	-	-	-
-	-	-	G9	VSS	S	-	-	-	-
20	30	K5	H8	VDD	S	-	-	-	-
-	-	-	N8	VSSRF	S	-	-	-	-
-	-	J4	L7	VSSRF	S	-	-	-	-
-	-	-	L8	VSSRF	S	-	-	-	-
-	-	-	M8	VSSRF	S	-	-	-	-
21	31	K4	M9	RF1	I/O	RF	(5)	-	-
22	32	K3	M10	VSSRF	S	-	-	-	-
-	-	K2	M11	VSSRF	S	-	-	-	-
-	-	-	K8	VSSRF	S	-	-	-	-
-	-	-	L9	VSSRF	S	-	-	-	-
-	-	-	L10	VSSRF	S	-	-	-	-
-	-	-	N11	VSSRF	S	-	-	-	-
23	33	J3	N12	VDDRF	S	-	-	-	-
-	-	K1	K10	VSSRF	S	-	-	-	-
-	-	-	M12	VSSRF	S	-	-	-	-
24	34	J2	N13	OSC_OUT	O	RF	(6)	-	-

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
25	35	J1	M13	OSC_IN	I	RF	(6)	-	-
-	-	-	L11	VSSRF	S	-	-	-	-
26	36	H3	K11	AT0	O	RF	(7)	-	-
27	37	H4	K12	AT1	O	RF	(7)	-	-
28	38	H2	L13	PB0	I/O	TT	(8)	COMP1_OUT, CM4_EVENTOUT, RF_TX_MOD_EXT_PA	-
29	39	H1	L12	PB1	I/O	TT	(8)	LPUART1_RTS_DE, LPTIM2_IN1, CM4_EVENTOUT	-
-	-	J5	-	VSS	S	-	-	-	-
-	-	-	M7	VSS_DCAP2	S	-	-	-	-
-	-	G2	H12	PE3	I/O	FT	-	CM4_EVENTOUT	-
30	40	G1	H13	PE4	I/O	FT	-	CM4_EVENTOUT	-
31	41	F2	H11	VFBSMPS	S	-	-	-	-
-	-	-	G13	VSSSMPS	S	-	-	-	-
32	42	F1	G12	VSSSMPS	S	-	-	-	-
33	43	E1	F11	VLXSMPS	S	-	-	-	-
-	-	-	G11	VLXSMPS	S	-	-	-	-
34	44	D1	F12	VDDSMPS	S	-	-	-	-
-	-	-	F13	VDDSMPS	S	-	-	-	-
-	-	-	K4	VSS	S	-	-	-	-
35	45	B1	-	VDD	S	-	-	-	-
-	46	G3	H10	PB12	I/O	FT_l	-	TIM1_BKIN, I2C3_SMBA, SPI2_NSS, LPUART1_RTS, TSC_G1_IO1, LCD_SEG12, SAI1_FS_A, CM4_EVENTOUT	-
-	47	C1	E12	PB13	I/O	FT_fl	-	TIM1_CH1N, I2C3_SCL, SPI2_SCK, LPUART1_CTS, TSC_G1_IO2, LCD_SEG13, SAI1_SCK_A, CM4_EVENTOUT	-

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
-	48	E2	E11	PB14	I/O	FT_fl	-	TIM1_CH2N, I2C3_SDA, SPI2_MISO, TSC_G1_IO3, LCD_SEG14, SAI1_MCLK_A, CM4_EVENTOUT	-
-	49	F3	F10	PB15	I/O	FT_l	-	RTC_REFIN, TIM1_CH3N, SPI2_MOSI, TSC_G1_IO4, LCD_SEG15, SAI1_SD_A, CM4_EVENTOUT	-
-	50	D2	D10	PC6	I/O	FT_l	-	TSC_G4_IO1, LCD_SEG24, CM4_EVENTOUT	-
-	-	E3	D12	PC7	I/O	FT_l	-	TSC_G4_IO2, LCD_SEG25, CM4_EVENTOUT	-
-	-	F4	D11	PC8	I/O	FT_l	-	TSC_G4_IO3, LCD_SEG26, CM4_EVENTOUT	-
-	-	B4	C13	PC9	I/O	FT_l	-	TIM1_BKIN, TSC_G4_IO4, USB_NOE, LCD_SEG27, SAI1_SCK_B, CM4_EVENTOUT	-
-	-	-	K6	VSS	S	-	-	-	-
-	-	B2	-	VSS	S	-	-	-	-
36	51	B5	C12	PA10	I/O	FT_fl	-	TIM1_CH3, SAI1_PDM_DI1, I2C1_SDA, USART1_RX, USB_CRS_SYNC, LCD_COM2, SAI1_SD_A, TIM17_BKIN, CM4_EVENTOUT	-
37	52	A1	B13	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS, USB_DM, CM4_EVENTOUT	-
38	53	A2	A13	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, LPUART1_RX, USART1_RTS_DE, USB_DP, CM4_EVENTOUT	-
39	54	A5	A11	PA13 (JTMS_SWDIO)	I/O	FT_u	(9)	JTMS-SWDIO, IR_OUT, USB_NOE, SAI1_SD_B, CM4_EVENTOUT	-
40	55	B3	A12	VDDUSB	S	-	-	-	-
-	-	-	C11	VSS	S	-	-	-	-

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
41	56	A3	C10	PA14 (JTCK_SWCLK)	I/O	FT_l	(9)	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, LCD_SEG5, SAI1_FS_B, CM4_EVENTOUT	-
42	57	A4	C9	PA15 (JTDI)	I/O	FT_l	(9)	JTDI, TIM2_CH1, TIM2_ETR, SPI1_NSS, TSC_G3_IO1, LCD_SEG17, CM4_EVENTOUT, MCO	-
-	-	-	J11	VSS_DCAP3	S	-	-	-	-
-	58	A6	B9	PC10	I/O	FT_l	-	TRACED1, TSC_G3_IO2, LCD_COM4/LCD_SEG28/ LCD_SEG40, CM4_EVENTOUT	-
-	59	B6	C8	PC11	I/O	FT_l	-	TSC_G3_IO3, LCD_COM5/LCD_SEG29/ LCD_SEG41, CM4_EVENTOUT	-
-	60	C5	B10	PC12	I/O	FT_l	-	LSCO(3), TRACED3, TSC_G3_IO4, LCD_COM6/LCD_SEG30/ LCD_SEG42, CM4_EVENTOUT	RTC_TAMP3/WKUP3
-	61	C4	B11	PD0	I/O	FT	-	SPI2_NSS, CM4_EVENTOUT	-
-	62	C3	C7	PD1	I/O	FT	-	SPI2_SCK, CM4_EVENTOUT	-
-	-	A7	B7	PD2	I/O	FT_l	-	TRACED2, TSC_SYNC, LCD_COM7/LCD_SEG31/LCD_SEG43, CM4_EVENTOUT	-
-	-	C2	D8	PD3	I/O	FT	-	SPI2_SCK, SPI2_MISO, QUADSPI_BK1_NCS, CM4_EVENTOUT	-
-	-	D3	C6	PD4	I/O	FT	-	SPI2_MOSI, TSC_G5_IO1, QUADSPI_BK1_IO0, CM4_EVENTOUT	-
-	-	B7	A6	PD5	I/O	FT	-	TSC_G5_IO2, QUADSPI_BK1_IO1, SAI1_MCLK_B, CM4_EVENTOUT	-

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
-	-	C6	D6	PD6	I/O	FT	-	SAI1_PDM_DI1, TSC_G5_IO3, QUADSPI_BK1_IO2, SAI1_SD_A, CM4_EVENTOUT	-
-	-	A8	C5	PD7	I/O	FT_l	-	TSC_G5_IO4, QUADSPI_BK1_IO3, LCD_SEG39, CM4_EVENTOUT	-
-	-	B9	B12	VSS	S	-	-	-	-
-	-	D4	B6	PD8	I/O	FT_l	-	TIM1_BKIN2, LCD_SEG28, CM4_EVENTOUT	-
-	-	D5	D4	PD9	I/O	FT_l	-	TRACED0, LCD_SEG29, CM4_EVENTOUT	-
-	-	E4	A7	PD10	I/O	FT_l	-	TRIG_INOUT, TSC_G6_IO1, LCD_SEG30, CM4_EVENTOUT	-
-	-	E5	B5	PD11	I/O	FT_l	-	TSC_G6_IO2, LCD_SEG31, LPTIM2_ETR, CM4_EVENTOUT	-
-	-	B8	B4	PD12	I/O	FT_l	-	TSC_G6_IO3, LCD_SEG32, LPTIM2_IN1, CM4_EVENTOUT	-
43	63	A9	C4	PB3 (JTDO)	I/O	FT_la	(9)	JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, USART1_RTS_DE, LCD_SEG7, SAI1_SCK_B, CM4_EVENTOUT	COMP2_INM
44	64	C7	B3	PB4 (NJTRST)	I/O	FT_fla	(9)	NJTRST, I2C3_SDA, SPI1_MISO, USART1_CTS, TSC_G2_IO1, LCD_SEG8, SAI1_MCLK_B, TIM17_BKIN, CM4_EVENTOUT	COMP2_INP
45	65	D6	A3	PB5	I/O	FT_l	-	LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, USART1_CK, LPUART1_TX, TSC_G2_IO2, LCD_SEG9, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, CM4_EVENTOUT	-

表16. STM32WB55xx 引脚和球定义 (继续)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
46	66	F5	A2	PB6	I/O	FT_fla	-	LPTIM1_ETR, I2C1_SCL, USART1_TX, TSC_G2_IO3, LCD_SEG6, SAI1_FS_B, TIM16_CH1N, MCO, CM4_EVENTOUT	COMP2_INP
47	67	D7	C3	PB7	I/O	FT_fla	-	LPTIM1_IN2, TIM1_BKIN, I2C1_SDA, USART1_RX, TSC_G2_IO4, LCD_SEG21, TIM17_CH1N, CM4_EVENTOUT	COMP2_INM, PVD_IN
-	-	-	J5	VSS	S	-	-	-	-
-	-	-	J7	VSS	S	-	-	-	-
-	-	-	J9	VSS	S	-	-	-	-
-	-	-	B8	VSS_DCAP4	S	-	-	-	-
48	68	A10	-	VDD	S	-	-	-	-
-	-	-	A8	VDD_DCAP4	S	-	-	-	-
-	-	-	F2	VDD_DCAP1	S	-	-	-	-
-	-	-	J12	VDD_DCAP3	S	-	-	-	-
-	-	-	N7	VDD_DCAP2	S	-	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch. As this switch only sinks a limited amount of current (3 mA), the use of the PC13, PC14 and PC15 GPIOs in output mode is limited:
   - the speed must not exceed 2 MHz with a maximum load of 30 pF
   - these GPIOs must not be used as current sources (e.g. to drive a LED).

2. 在备份域上电后，PC13、PC14 和 PC15 作为 GPIOs 运行。它们的功能取决于未被系统复位重置的 RTC 寄存器的内容。有关如何管理这些 GPIOs 的详细信息，请参阅参考手册 RM0434 中的备份域和 RTC 寄存器描述，可在 *www.st.com*.

3. LSCO 上的时钟在运行和停止模式下可用，而在 PA2 上则在待机和关闭模式下可用。

4. 在 UFQFPN48 上，VDDA 与 VREF+ 连接。

5. 无线电引脚，使用标准 PCB 布局。

6. 32 MHz振荡器引脚, use the nominal PCB layout according to reference design (see AN5165).

7. Reserved, must be kept unconnected.

8. High frequency (above 32 kHz) may impact the RF性能. Set output speed GPIOB_OSPEEDRy[1:0] to 00 (y = 0 and1) during RF operation.

9. After reset these pins are configured as JTAG/SW调试替代功能, and the internal pull-up on PA15, PA13 and PB4 pins and the internal pull-down on PA14 pin are activated.

表17. STM32WB35xx 引脚和球定义

Pin		Pin type	I/O structures	Notes	Alternate functions	Additional functions
Number	Name (function after reset)					
1	VBAT	S	-	-	-	-
2	PC14-OSC32_IN	I/O	FT	(1) (2)	CM4_EVENTOUT	OSC32_IN
3	PC15-OSC32_OUT	I/O	FT	(1) (2)	CM4_EVENTOUT	OSC32_OUT
4	PH3-BOOT0	I/O	FT	-	CM4_EVENTOUT, LSCO(3)	-
5	PB8	I/O	FT_f	-	TIM1_CH2N, SAI1_PDM_CK1, I2C1_SCL, QUADSPI_BK1_IO1, SAI1_MCLK_A, TIM16_CH1, CM4_EVENTOUT	-
6	PB9	I/O	FT_f	-	TIM1_CH3N, SAI1_PDM_DI2, I2C1_SDA, IR_OUT, QUADSPI_BK1_IO0, SAI1_FS_A, TIM17_CH1, CM4_EVENTOUT	-
7	NRST	I/O	RST	-	-	-
8	VDDA	S	-	-	-	-
9	PA0	I/O	FT_a	-	TIM2_CH1, COMP1_OUT, SAI1_EXTCLK, TIM2_ETR, CM4_EVENTOUT	COMP1_INM, ADC1_IN5, RTC_TAMP2/WKUP1
10	PA1	I/O	FT_a	-	TIM2_CH2, I2C1_SMBA, SPI1_SCK, CM4_EVENTOUT	COMP1_INP, ADC1_IN6
11	PA2	I/O	FT_a	-	LSCO(3), TIM2_CH3, LPUART1_TX, QUADSPI_BK1_NCS, COMP2_OUT, CM4_EVENTOUT	COMP2_INM, ADC1_IN7, WKUP4
12	PA3	I/O	FT_a	-	TIM2_CH4, SAI1_PDM_CK1, LPUART1_RX, QUADSPI_CLK, SAI1_MCLK_A, CM4_EVENTOUT	COMP2_INP, ADC1_IN8
13	PA4	I/O	FT_a	-	SPI1_NSS, SAI1_FS_B, LPTIM2_OUT, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN9
14	PA5	I/O	FT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, LPTIM2_ETR, SAI1_SD_B, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN10
15	PA6	I/O	FT_a	-	TIM1_BKIN, SPI1_MISO, LPUART1_CTS, QUADSPI_BK1_IO3, TIM16_CH1, CM4_EVENTOUT	ADC1_IN11
16	PA7	I/O	FT_fa	-	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, COMP2_OUT, TIM17_CH1, CM4_EVENTOUT	ADC1_IN12
17	PA8	I/O	FT_a	-	MCO, TIM1_CH1, SAI1_PDM_CK2, USART1_CK, SAI1_SCK_A, LPTIM2_OUT, CM4_EVENTOUT	ADC1_IN15

表17. STM32WB35xx 引脚和球定义 (继续)

Pin		Pin type	I/O structures	Notes	Alternate functions	Additional functions
Number	Name (function after reset)					
18	PA9	I/O	FT_fa	-	TIM1_CH2, SAI1_PDM_DI2, I2C1_SCL, USART1_TX, SAI1_FS_A, CM4_EVENTOUT	COMP1_INM, ADC1_IN16
19	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, SPI1_NSS, SAI1_EXTCLK, CM4_EVENTOUT	COMP1_INP
20	VDD	S	-	-	-	-
21	RF1	I/O	RF	(4)	-	-
22	VSSRF	S	-	-	-	-
23	VDDRF	S	-	-	-	-
24	OSC_OUT	O	RF	(5)	-	-
25	OSC_IN	I	RF	(5)	-	-
26	AT0	O	RF	(6)	-	-
27	AT1	O	RF	(6)	-	-
28	PB0	I/O	TT	(7)	COMP1_OUT, CM4_EVENTOUT, RF_TX_MOD_EXT_PA	-
29	PB1	I/O	TT	(7)	LPUART1_RTS_DE, LPTIM2_IN1, CM4_EVENTOUT	-
30	PE4	I/O	FT	-	CM4_EVENTOUT	-
31	VFBSMPS	S	-	-	-	-
32	VSSSMPS	S	-	-	-	-
33	VLXSMPS	S	-	-	-	-
34	VDDSMPS	S	-	-	-	-
35	VDD	S	-	-	-	-
36	PA10	I/O	FT_f	-	TIM1_CH3, SAI1_PDM_DI1, I2C1_SDA, USART1_RX, USB_CRS_SYNC, SAI1_SD_A, TIM17_BKIN, CM4_EVENTOUT	-
37	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS, USB_DM, CM4_EVENTOUT	-
38	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, LPUART1_RX, USART1_RTS_DE, USB_DP, CM4_EVENTOUT	-
39	PA13 (JTMS-SWDIO)	I/O	FT	(8)	JTMS-SWDIO, IR_OUT, USB_NOE, SAI1_SD_B, CM4_EVENTOUT	-
40	VDDUSB	S	-	-	-	-

表17. STM32WB35xx 引脚和球定义 (继续)

Pin		Pin type	I/O structures	Notes	Alternate functions	Additional functions
Number	Name (function after reset)					
41	PA14 (JTCK-SWCLK)	I/O	FT	(8)	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, SAI1_FS_B, CM4_EVENTOUT	-
42	PA15 (JTDI)	I/O	FT	(8)	JTDI, TIM2_CH1, TIM2_ETR, SPI1_NSS, CM4_EVENTOUT, MCO	-
43	PB3 (JTDO)	I/O	FT_a	-	JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, USART1_RTS_DE, SAI1_SCK_B, CM4_EVENTOUT	COMP2_INM
44	PB4 (NJTRST)	I/O	FT_fa	(8)	NJTRST, I2C3_SDA, SPI1_MISO, USART1_CTS, SAI1_MCLK_B, TIM17_BKIN, CM4_EVENTOUT	COMP2_INP
45	PB5	I/O	FT_a	-	LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, USART1_CK, LPUART1_TX, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, CM4_EVENTOUT	-
46	PB6	I/O	FT_fa	-	LPTIM1_ETR, I2C1_SCL, USART1_TX, SAI1_FS_B, TIM16_CH1N, MCO, CM4_EVENTOUT	COMP2_INP
47	PB7	I/O	FT_fa	-	LPTIM1_IN2, TIM1_BKIN, I2C1_SDA, USART1_RX, TIM17_CH1N, CM4_EVENTOUT	COMP2_INM, PVD_IN
48	VDD	S	-	-	-	-

1. PC14 and PC15 are supplied through the power switch. As this switch only sinks a limited amount of current (3 mA), the use of the PC14 and PC15 GPIOs in output mode is limited:
   - the speed must not exceed 2 MHz with a maximum load of 30 pF
   - these GPIOs must not be used as current sources (e.g. to drive a LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers that are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the reference manual RM0434, available on *www.st.com*.

3. LSCO 上的时钟在运行和停止模式下可用，而在 PA2 上则在待机和关闭模式下可用。

4. RF引脚，使用标准 PCB 布局。

5. 32 MHz振荡器引脚，使用参考设计 (看 AN5165) 中的典型 PCB 布局。

6. 保留，必须保持未连接。

7. 高频 (超过 32 kHz) 可能会影响 RF 性能。在 RF 操作期间，将输出速度 GPIOB_OSPEEDRy[1:0] 设置为 00 (y = 0 和 1) 。

8. 复位后，这些引脚配置为 JTAG/SW 调试替代功能，并且 PA15、PA13 和 PB4 引脚上的内部上拉以及 PA14 引脚上的内部下拉被激活。

Table 18. Alternate functions (STM32WB55xx)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
A	PA0	-	TIM2_ CH1	-	-	-	-	-	-	-	-	-	-	COMP1_ OUT	SAI1_ EXTCLK	TIM2_ ETR	CM4_ EVENTOUT
	PA1	-	TIM2_ CH2	-	-	I2C1_ SMBA	SPI1_ SCK	-	-		-	-	LCD_SEG0	-	-	-	CM4_ EVENTOUT
	PA2	LSCO	TIM2_ CH3	-	-	-	-	-	-	LPUART1 _TX	-	QUADSPI_ BK1_NCS	LCD_SEG1	COMP2_ OUT	-	-	CM4_ EVENTOUT
	PA3	-	TIM2_ CH4	-	SAI1_ PDM_CK1	-	-	-	-	LPUART1 _RX	-	QUADSPI_ CLK	LCD_SEG2	-	SAI1 _MCLK_A	-	CM4_ EVENTOUT
	PA4	-	-	-	-		SPI1_ NSS	-	-	-	-	-	LCD_SEG5	-	SAI1 _FS_B	LPTIM2_ OUT	CM4_ EVENTOUT
	PA5	-	TIM2_ CH1	TIM2_ ETR	-		SPI1_ SCK	-	-	-	-	-	-	-	SAI1 _SD_B	LPTIM2_ ETR	CM4_ EVENTOUT
	PA6	-	TIM1_ BKIN	-	-		SPI1_ MISO	-	-	LPUART1 _CTS	-	QUADSPI_ BK1_IO3	LCD_SEG3	TIM1_ BKIN	-	TIM16 _CH1	CM4_ EVENTOUT
	PA7	-	TIM1_ CH1N	-	-	I2C3_ SCL	SPI1_ MOSI	-	-	-	-	QUADSPI_ BK1_IO2	LCD_SEG4	COMP2_ OUT	-	TIM17 _CH1	CM4_ EVENTOUT
	PA8	MCO	TIM1_ CH1	-	SAI1_ PDM_CK2	-	-	-	USART1_ CK	-	-		LCD_COM0	-	SAI1 _SCK_A	LPTIM2_ OUT	CM4_ EVENTOUT
	PA9	-	TIM1_ CH2	-	SAI1_ PDM_DI2	I2C1_ SCL	SPI2_ SCK	-	USART1_ TX	-	-		LCD_COM1	-	SAI1 _FS_A	-	CM4_ EVENTOUT
	PA10	-	TIM1_ CH3	-	SAI1_ PDM_DI1	I2C1_ SDA		-	USART1_ RX	-	-	USB_CRS _SYNC	LCD_COM2	-	SAI1 _SD_A	TIM17 _BKIN	CM4_ EVENTOUT
	PA11	-	TIM1_ CH4	TIM1_ BKIN2	-	-	SPI1_ MISO	-	USART1_ CTS	-	-	USB_DM	-	TIM1_ BKIN2	-	-	CM4_ EVENTOUT
	PA12	-	TIM1_ ETR	-	-	-	SPI1_ MOSI	-	USART1_ RTS_DE	LPUART1 _RX	-	USB_DP	-	-	-	-	CM4_ EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	IR_OUT	-	USB_NOE	-	-	SAI1 _SD_B	-	CM4_ EVENTOUT
	PA14	JTCK-SWCLK	LPTIM1_ OUT	-	-	I2C1_ SMBA	-	-	-	-	-	-	LCD_SEG5	-	SAI1 _FS_B	-	CM4_ EVENTOUT
	PA15	JTDI	TIM2_ CH1	TIM2_ ETR	-		SPI1_ NSS	MCO	-	-		-	LCD_SEG17	-	-	-	CM4_ EVENTOUT

Table 18. Alternate functions (STM32WB55xx) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
B	PB0	-	-	-	-	-	-	RF_TX_ MOD_ EXT_PA	-		-	-	-	COMP1_ OUT	-	-	CM4_ EVENTOUT
	PB1	-	-	-	-	-	-	-	-	LPUART1 _RTS_DE	-	-	-	-	-	LPTIM2_ IN1	CM4_ EVENTOUT
	PB2	RTC_ OUT	LPTIM1_ OUT	-	-	I2C3_ SMBA	SPI1_ NSS	-	-	-	-	-	LCD_VLCD	-	SAI1_ EXTCLK	-	CM4_ EVENTOUT
	PB3	JTDO-TRACE SWO	TIM2_ CH2	-	-	-	SPI1_ SCK	-	USART1_ RTS_DE	-	-	-	LCD_SEG7	-	SAI1_ SCK_B	-	CM4_ EVENTOUT
	PB4	NJTRST	-	-	-	I2C3_ SDA	SPI1_ MISO	-	USART1_ CTS	-	TSC_G2 _IO1	-	LCD_SEG8	-	SAI1_ MCLK_B	TIM17_ BKIN	CM4_ EVENTOUT
	PB5	-	LPTIM1_ IN1	-	-	I2C1_ SMBA	SPI1_ MOSI	-	USART1_ CK	LPUART1 _TX	TSC_G2 _IO2	-	LCD_SEG9	COMP2_ OUT	SAI1_ SD_B	TIM16_ BKIN	CM4_ EVENTOUT
	PB6	MCO	LPTIM1_ ETR	-	-	I2C1_ SCL	-	-	USART1_ TX	-	TSC_G2 _IO3	-	LCD_SEG6	-	SAI1_ FS_B	TIM16_ CH1N	CM4_ EVENTOUT
	PB7	-	LPTIM1_ IN2	-	TIM1_ BKIN	I2C1_ SDA	-	-	USART1_ RX	-	TSC_G2 _IO4	-	LCD_SEG21	-	-	TIM17_ CH1N	CM4_ EVENTOUT
	PB8	-	TIM1_ CH2N	-	SAI1_ PDM_CK1	I2C1_ SCL	-	-	-	-	-	QUADSPI_ BK1_IO1	LCD_SEG16	-	SAI1_ MCLK_A	TIM16_ CH1	CM4_ EVENTOUT
	PB9	-	TIM1_ CH3N	-	SAI1_ PDM_DI2	I2C1_ SDA	SPI2_ NSS	-	-	IR_OUT	TSC_G7 _IO4	QUADSPI_ BK1_IO0	LCD_COM3	-	SAI1_ FS_A	TIM17_ CH1	CM4_ EVENTOUT
	PB10	-	TIM2_ CH3	-	-	I2C3_ SCL	SPI2_SC K	-	-	LPUART1 _RX	TSC _SYNC	QUADSPI_ CLK	LCD_SEG10	COMP1_ OUT	SAI1_ SCK_A	-	CM4_ EVENTOUT
	PB11	-	TIM2_ CH4	-	-	I2C3_ SDA	-	-	-	LPUART1 _TX	-	QUADSPI_ BK1_NCS	LCD_SEG11	COMP2_ OUT	-	-	CM4_ EVENTOUT
	PB12	-	TIM1_ BKIN	-	TIM1_ BKIN	I2C3_ SMBA	SPI2_ NSS	-	-	LPUART1 _RTS	TSC_G1 _IO1	-	LCD_SEG12	-	SAI1_ FS_A	-	CM4_ EVENTOUT
	PB13	-	TIM1_ CH1N	-	-	I2C3_ SCL	SPI2_ SCK	-	-	LPUART1 _CTS	TSC_G1 _IO2	-	LCD_SEG13	-	SAI1_ SCK_A	-	CM4_ EVENTOUT
	PB14	-	TIM1_ CH2N	-	-	I2C3_ SDA	SPI2_ MISO	-	-	-	TSC_G1 _IO3	-	LCD_SEG14	-	SAI1_ MCLK_A	-	CM4_ EVENTOUT
	PB15	RTC_ REFIN	TIM1_ CH3N	-	-	-	SPI2_ MOSI	-	-	-	TSC_G1 _IO4	-	LCD_SEG15	-	SAI1_ SD_A	-	CM4_ EVENTOUT

Table 18. Alternate functions (STM32WB55xx) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
C	PC0	-	LPTIM1_ IN1	-	-	I2C3 _SCL	-	-	-	LPUART1 _RX	-	-	LCD_SEG18	-	-	LPTIM2_ IN1	CM4_ EVENTOUT
	PC1	-	LPTIM1_ OUT	-	SPI2_ MOSI	I2C3 _SDA		-	-	LPUART1 _TX	-	-	LCD_SEG19	-	-	-	CM4_ EVENTOUT
	PC2	-	LPTIM1_ IN2	-	-	-	SPI2_ MISO	-	-	-	-	-	LCD_SEG20	-	-	-	CM4_ EVENTOUT
	PC3	-	LPTIM1_ ETR	-	SAI1_ PDM_DI1	-	SPI2_ MOSI	-	-	-	-	-	LCD_VLCD	-	SAI1 _SD_A	LPTIM2_ ETR	CM4_ EVENTOUT
	PC4	-	-	-	-	-	-	-	-	-	-	-	LCD_SEG22	-	-	-	CM4_ EVENTOUT
	PC5	-	-	-	SAI1_ PDM_DI3	-	-	-	-	-	-	-	LCD_SEG23	-	-	-	CM4_ EVENTOUT
	PC6	-	-	-	-	-	-	-	-	-	TSC_G4 _IO1	-	LCD_SEG24	-	-	-	CM4_ EVENTOUT
	PC7	-	-	-	-	-	-	-	-	-	TSC_G4 _IO2	-	LCD_SEG25	-	-	-	CM4_ EVENTOUT
	PC8	-	-	-	-	-	-	-	-	-	TSC_G4 _IO3	-	LCD_SEG26	-	-	-	CM4_ EVENTOUT
	PC9	-	-	-	TIM1 _BKIN	-	-	-	-	-	TSC_G4 _IO4	USB_NOE	LCD_SEG27	-	SAI1 _SCK_B	-	CM4_ EVENTOUT
	PC10	TRACE D1	-	-	-	-	-	-	-	-	TSC_G3 _IO2	-	LCD_COM4 LCD_SEG28 LCD_SEG40	-	-	-	CM4_ EVENTOUT
	PC11	-	-	-	-	-	-	-	-	-	TSC_G3 _IO3	-	LCD_COM5 LCD_SEG29 LCD_SEG41	-	-	-	CM4_ EVENTOUT
	PC12	TRACE D3	-	-	-	-	-	LSCO	-	-	TSC_G3 _IO4	-	LCD_COM6 LCD_SEG30 LCD_SEG42	-	-	-	CM4_ EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT

Table 18. Alternate functions (STM32WB55xx) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
D	PD0	-	-	-	-	-	SPI2_ NSS	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PD1	-	-	-	-	-	SPI2_ SCK	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PD2	TRACE D2	-	-	-	-	-	-	-	-	TSC_ SYNC	-	LCD_COM7 LCD_SEG31 LCD_SEG43	-	-	-	CM4_ EVENTOUT
	PD3	-	-	-	SPI2_SCK	-	SPI2_ MISO	-	-	-	-	QUADSPI_ BK1_NCS	-	-	-	-	CM4_ EVENTOUT
	PD4	-	-	-	-	-	SPI2_ MOSI	-	-	-	TSC_ G5_IO1	QUADSPI_ BK1_IO0	-	-	-	-	CM4_ EVENTOUT
	PD5	-	-	-	-	-	-	-	-	-	TSC_ G5_IO2	QUADSPI_ BK1_IO1	-	-	SAI1_ MCLK_B	-	CM4_ EVENTOUT
	PD6	-	-	-	SAI1_ PDM_DI1	-	-	-	-	-	TSC_ G5_IO3	QUADSPI_ BK1_IO2	-	-	SAI1_ SD_A	-	CM4_ EVENTOUT
	PD7	-	-	-	-	-	-	-	-	-	TSC_ G5_IO4	QUADSPI_ BK1_IO3	LCD_SEG39	-	-	-	CM4_ EVENTOUT
	PD8	-	-	TIM1 _BKIN2	-	-	-	-	-	-	-	-	LCD_SEG28	-	-	-	CM4_ EVENTOUT
	PD9	TRACE D0	-	-	-	-	-	-	-	-	-	-	LCD_SEG29	-	-	-	CM4_ EVENTOUT
	PD10	TRIG _INOUT	-	-	-	-	-	-	-	-	TSC_ G6_IO1	-	LCD_SEG30	-	-	-	CM4_ EVENTOUT
	PD11	-	-	-	-	-	-	-	-	-	TSC_ G6_IO2	-	LCD_SEG31	-	-	LPTIM2_ ETR	CM4_ EVENTOUT
	PD12	-	-	-	-	-	-	-	-	-	TSC_ G6_IO3	-	LCD_SEG32	-	-	LPTIM2_ IN1	CM4_ EVENTOUT
	PD13	-	-	-	-	-	-	-	-	-	TSC_ G6_IO4	-	LCD_SEG33	-	-	LPTIM2_ OUT	CM4_ EVENTOUT
	PD14	-	TIM1_ CH1	-	-	-	-	-	-	-	-	-	LCD_SEG34	-	-	-	CM4_ EVENTOUT
	PD15	-	TIM1_ CH2	-	-	-	-	-	-	-	-	-	LCD_SEG35	-	-	-	CM4_ EVENTOUT

Table 18. Alternate functions (STM32WB55xx) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
E	PE0	-	TIM1_ ETR	-	-	-	-	-	-	-	TSC_ G7_IO3	-	LCD_SEG36	-	-	TIM16_ CH1	CM4_ EVENTOUT
	PE1	-	-	-	-	-	-	-	-	-	TSC_ G7_IO2	-	LCD_SEG37	-	-	TIM17_ CH1	CM4_ EVENTOUT
	PE2	TRACECK	-	-	SAI1_ PDM_CK1	-	-	-	-	-	TSC_ G7_IO1	-	LCD_SEG38	-	SAI1_ MCLK_A	-	CM4_ EVENTOUT
	PE3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PE4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PH3	LSCO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT

Table 19. Alternate functions (STM32WB35xx)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF10	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SAI1/ TIM1	I2C1/ I2C3	SPI1	RF	USART1	LPUART1	USB/ QUADSPI	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
A	PA0	-	TIM2_ CH1	-	-	-	-	-	-	-	-	COMP1_ OUT	SAI1_ EXTCLK	TIM2_ ETR	CM4_ EVENTOUT
	PA1	-	TIM2_ CH2	-	-	I2C1_ SMBA	SPI1_ SCK	-	-		-	-	-	-	CM4_ EVENTOUT
	PA2	LSCO	TIM2_ CH3	-	-	-	-	-	-	LPUART1 _TX	QUADSPI_ BK1_NCS	COMP2_ OUT	-	-	CM4_ EVENTOUT
	PA3	-	TIM2_ CH4	-	SAI1_ PDM_CK1	-	-	-	-	LPUART1 _RX	QUADSPI_ CLK	-	SAI1 _MCLK_A	-	CM4_ EVENTOUT
	PA4	-	-	-	-		SPI1_ NSS	-	-	-	-	-	SAI1 _FS_B	LPTIM2_ OUT	CM4_ EVENTOUT
	PA5	-	TIM2_ CH1	TIM2_ ETR	-		SPI1_ SCK	-	-	-	-	-	SAI1 _SD_B	LPTIM2_ ETR	CM4_ EVENTOUT
	PA6	-	TIM1_ BKIN	-	-		SPI1_ MISO	-	-	LPUART1 _CTS	QUADSPI_ BK1_IO3	TIM1_ BKIN	-	TIM16 _CH1	CM4_ EVENTOUT
	PA7	-	TIM1_ CH1N	-	-	I2C3_ SCL	SPI1_ MOSI	-	-	-	QUADSPI_ BK1_IO2	COMP2_ OUT	-	TIM17 _CH1	CM4_ EVENTOUT
	PA8	MCO	TIM1_ CH1	-	SAI1_ PDM_CK2	-	-	-	USART1_ CK	-		-	SAI1 _SCK_A	LPTIM2_ OUT	CM4_ EVENTOUT
	PA9	-	TIM1_ CH2	-	SAI1_ PDM_DI2	I2C1_ SCL	-	-	USART1_ TX	-		-	SAI1 _FS_A	-	CM4_ EVENTOUT
	PA10	-	TIM1_ CH3	-	SAI1_ PDM_DI1	I2C1_ SDA	-	-	USART1_ RX	-	USB_CRS _SYNC	-	SAI1 _SD_A	TIM17 _BKIN	CM4_ EVENTOUT
	PA11	-	TIM1_ CH4	TIM1_ BKIN2	-	-	SPI1_ MISO	-	USART1_ CTS	-	USB_DM	TIM1_ BKIN2	-	-	CM4_ EVENTOUT
	PA12	-	TIM1_ ETR	-	-	-	SPI1_ MOSI	-	USART1_ RTS_DE	LPUART1 _RX	USB_DP	-	-	-	CM4_ EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	IR_OUT	USB_NOE	-	SAI1 _SD_B	-	CM4_ EVENTOUT
	PA14	JTCK-SWCLK	LPTIM1_ OUT	-	-	I2C1_ SMBA	-	-	-	-	-	-	SAI1 _FS_B	-	CM4_ EVENTOUT
	PA15	JTDI	TIM2_ CH1	TIM2_ ETR	-		SPI1_ NSS	MCO	-	-	-	-	-	-	CM4_ EVENTOUT

Table 19. Alternate functions (STM32WB35xx) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF10	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SAI1/ TIM1	I2C1/ I2C3	SPI1	RF	USART1	LPUART1	USB/ QUADSPI	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
B	PB0	-	-	-	-	-	-	RF_TX_ MOD_EXT_PA	-		-	COMP1_ OUT	-	-	CM4_ EVENTOUT
	PB1	-	-	-	-	-	-	-	-	LPUART1 _RTS_DE	-	-	-	LPTIM2_ IN1	CM4_ EVENTOUT
	PB2	RTC_ OUT	LPTIM1_ OUT	-	-	I2C3_ SMBA	SPI1_ NSS	-	-	-	-	-	SAI1_ EXTCLK	-	CM4_ EVENTOUT
	PB3	JTDO-TRACE SWO	TIM2_ CH2	-	-	-	SPI1_ SCK	-	USART1_ RTS_DE	-	-	-	SAI1_ SCK_B	-	CM4_ EVENTOUT
	PB4	NJTRST	-	-	-	I2C3_ SDA	SPI1_ MISO	-	USART1_ CTS	-	-	-	SAI1_ MCLK_B	TIM17_ BKIN	CM4_ EVENTOUT
	PB5	-	LPTIM1_ IN1	-	-	I2C1_ SMBA	SPI1_ MOSI	-	USART1_ CK	LPUART1 _TX	-	COMP2_ OUT	SAI1_ SD_B	TIM16_ BKIN	CM4_ EVENTOUT
	PB6	MCO	LPTIM1_ ETR	-	-	I2C1_ SCL	-	-	USART1_ TX	-	-	-	SAI1_ FS_B	TIM16_ CH1N	CM4_ EVENTOUT
	PB7	-	LPTIM1_ IN2	-	TIM1_ BKIN	I2C1_ SDA	-	-	USART1_ RX	-	-	-	-	TIM17_ CH1N	CM4_ EVENTOUT
	PB8	-	TIM1_ CH2N	-	SAI1_ PDM_CK1	I2C1_ SCL	-	-	-	-	QUADSPI_ BK1_IO1	-	SAI1_ MCLK_A	TIM16_ CH1	CM4_ EVENTOUT
	PB9	-	TIM1_ CH3N	-	SAI1_ PDM_DI2	I2C1_ SDA	-	-	-	IR_OUT	QUADSPI_ BK1_IO0	-	SAI1_ FS_A	TIM17_ CH1	CM4_ EVENTOUT
C	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
E	PE4	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
H	PH3	LSCO	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT

5 内存映射

STM32WB55xx 和 STM32WB35xx 设备具有一个单一的物理地址空间，可以由应用程序处理器和无线电子子系统访问。

一部分闪存内存和SRAM2a和SRAM2b内存被使为安全的，仅可由CPU2访问，受到执行、读取和写入从CPU1和DMA的保护。

在共享资源的情况下，软件应该实现仲裁机制以避免访问冲突。这发生在外围设备复位和时钟控制器(RCC)、电源控制(PWC)、扩展中断和事件控制器和闪存接口上，可以使用内置的信号量块(HSEM)进行实现。

默认情况下，无线电子子系统和CPU2以安全模式运行。这意味着闪存和SRAM2内存的一部分只能被无线电子子系统和CPU2访问。在这种情况下，主处理器(CPU1) 无法访问这些资源。

详细的内存映射和外围设备映射可以在参考手册 RM0434 中找到。

6 电气特性

6.1 参数条件

除非另有说明，所有电压均参考 VSS.

6.1.1 最小和最大值

除非另有说明，最小和最大值在最差的环境温度、供电电压和频率条件下通过生产中的测试来保证，测试范围内100%的设备，环境温度为 TA = 25 °C 和 TA = TAmax (由选择的温度范围)给出。

基于特性化结果、设计模拟和/或技术特性的数据在表脚注中标明，且不在生产中进行测试。基于特性化，最小和最大值指的是样本测试，并表示平均值加减三倍的标准差 (mean ±3σ).

6.1.2 典型值

除非另有说明，典型数据基于 VDD = VDDA = VDDRF = 3 V 和 TA = 25 °C。这些数据只作为设计指南提供，并未进行测试。

典型 ADC 精度值通过对标准扩散批次中的样本批次进行特征化来确定，覆盖全温度范围，其中 95% 的设备的错误小于或等于 (平均 ± 2σ). 值。

6.1.3 典型曲线

除非另有说明，所有典型曲线只作为设计指南提供，并未进行测试。

6.1.4 载流器电容器

用于引脚参数测量的加载条件如 图*14*所示。

6.1.5 引脚输入电压

输入电压测量在设备的一个引脚上被描述为图*15*.

图14. 引脚加载条件

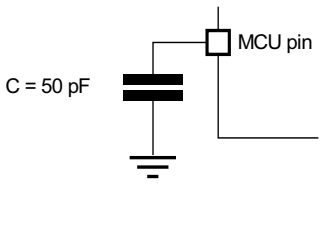
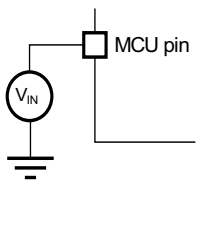
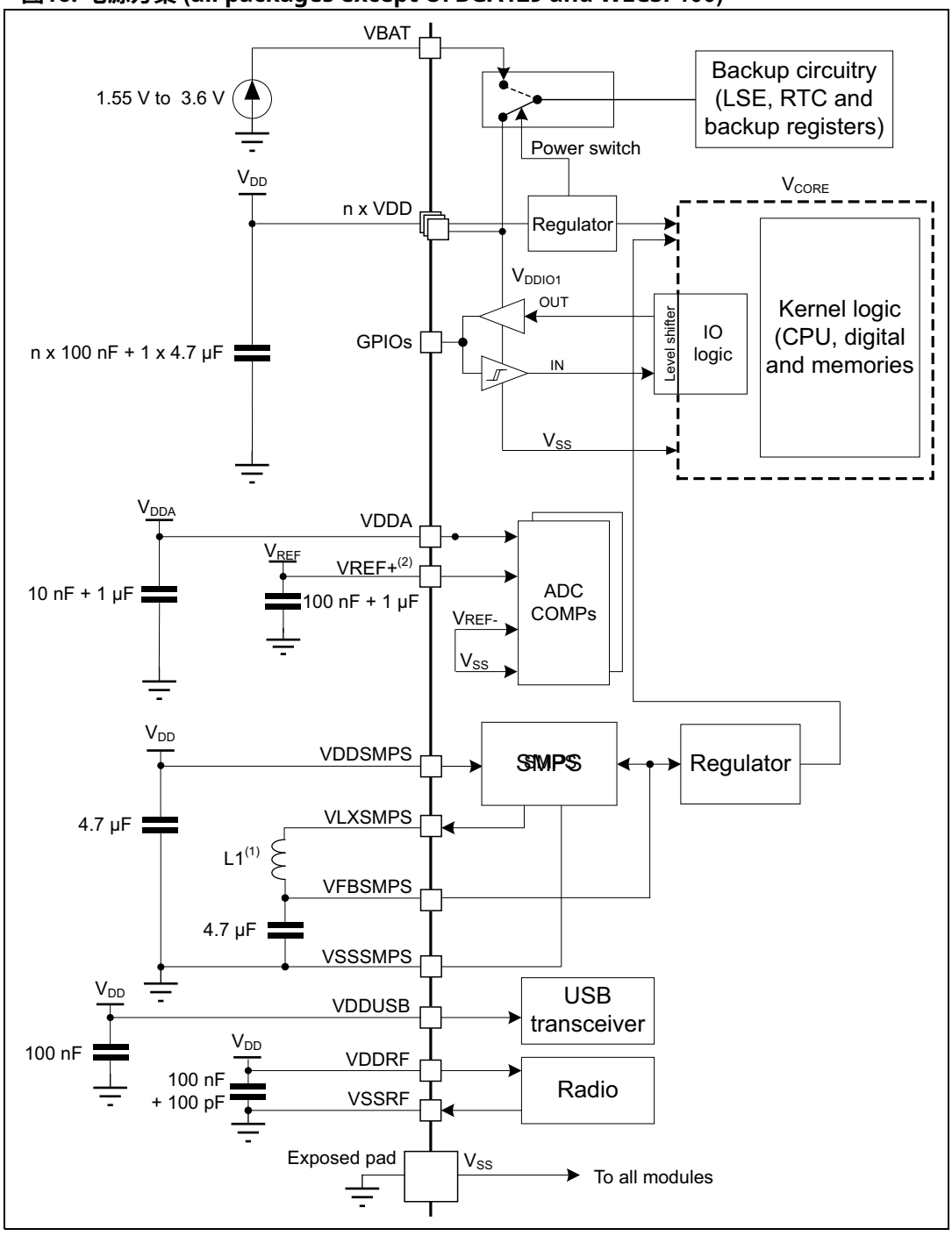


Figure 15. Pin input voltage



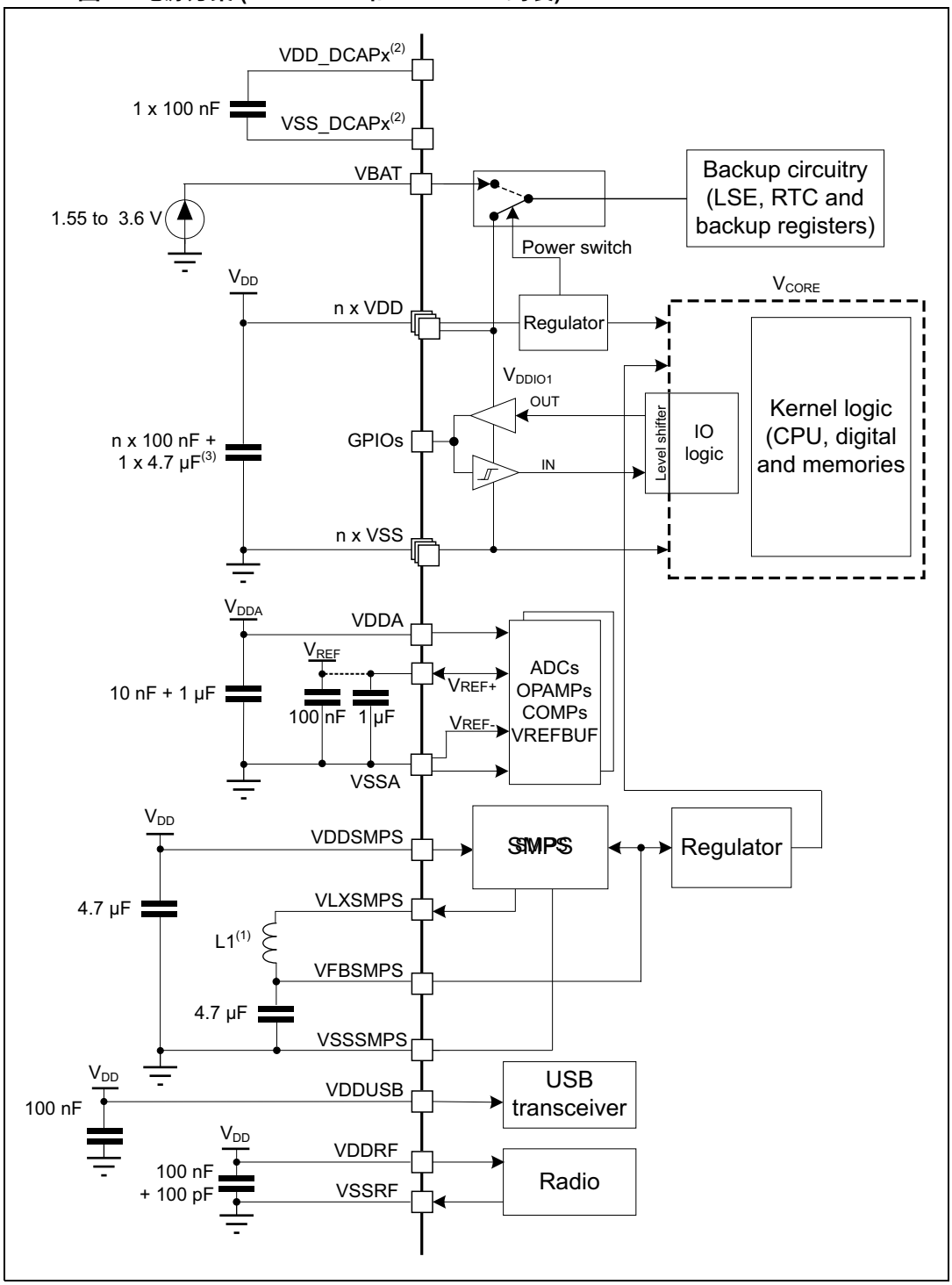
6.1.6 电源方案

图16. 电源方案 (all packages except UFBGA129 and WLCSP100)



1. L1的值取决于频率，如表格中所示。表6. 2. VREF+ 连接不可用于UFQFPN48封装。

图17. 电源方案 (UFBGA129和WLCSP100封装)

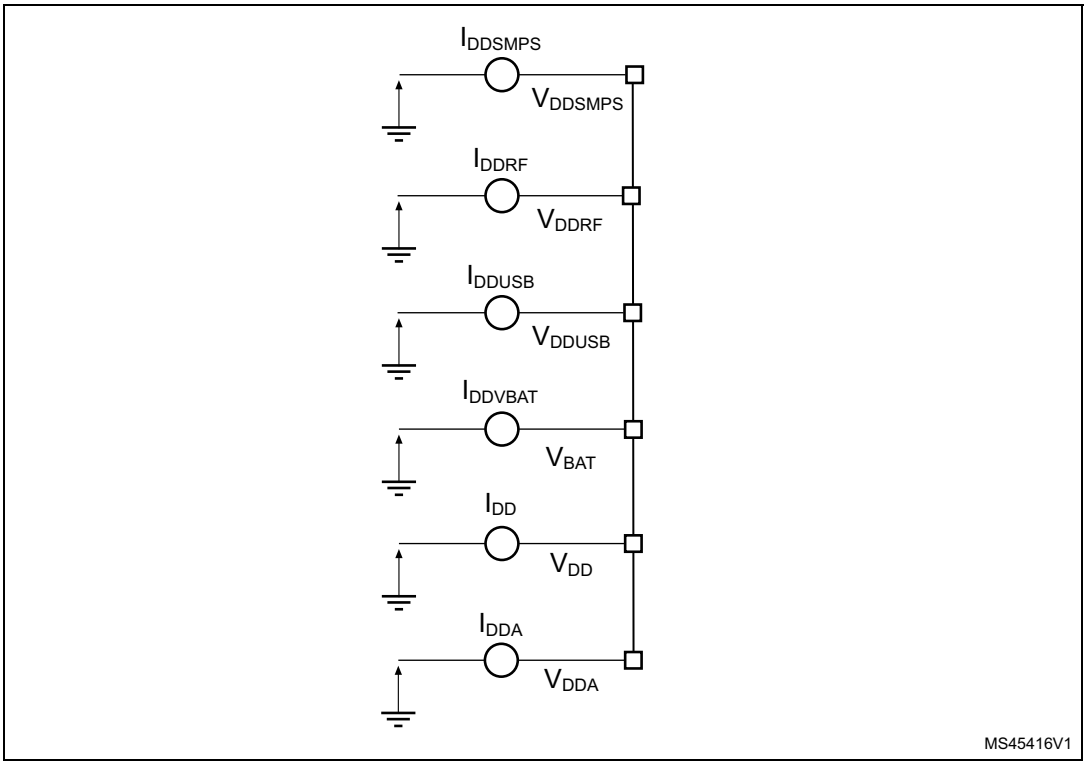


1. The value of L1 depends upon the frequency, as indicated in *Table 6*.
2. For UFBGA129 package VDD_DCAPx and VSS_DCAPx balls are connected to V_{DD} and V_{SS} internally, to simplify the 2-layer board layout and especially the ground plane below the BGA. V_{DD} power supply can be made with a single connection to the center of the BGA on the board bottom layer. The decoupling 100 nF capacitors are connected without cutting the board ground plane.
3. n x 100 nF only for WLCSP package.

注意: Each power supply pair (V_{DD} / V_{SS}, V_{DDA} / V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown in 图16. These capacitors must be placed as close aspossible to (or below) t he appropriate pins on the underside of the PCB to ensure the goodfunctionality of the device.

6.1.7 电流消耗测量

Figure 18. Current consumption measurement scheme



6.2 绝对最大额定值

超出表20、表21和表22中列出的绝对最大额定值的应力可能会对设备造成永久性损坏。这些是应力额定值，设备在这些条件下的功能运行不在此范围内。长期暴露在最大额定值条件下可能会影响设备的可靠性。

Device mission profile (应用条件) 符合 JEDEC JESD47 认证标准，扩展任务配置文件可按需提供。

表20. 电压特性(1)

Symbol	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}, V_{DDRF}, V_{DDSMPS}, V_{BAT}, V_{REF+})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS}-0.3	min (V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}, V_{DDRF}, V_{DDSMPS}) + 4.0(3)(4)	
	Input voltage on TT_xx pins		4.0	
	Input voltage on any other pin		4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins(5)	-	50	
V_{REF+} - V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA}	-	0.4	V

1. All main power (V_{DD}, V_{DDRF}, V_{DDA}, V_{DDUSB}, V_{LCD}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 21* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

表21. 电流特性

Symbol	Ratings	Max	Unit
$\sum I_{VDD}$	Total current into sum of all V_{DD} power lines (source)(1)	130	mA
$\sum I_{VSS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	130	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	100	
	Total output current sourced by sum of all I/Os and control pins(2)	100	
$I_{INJ(PIN)}$(3)	Injected current on FT_xxx, TT_xx, RST and B pins, except PB0 and PB1	–5 / +0(4)	
	Injected current on PB0 and PB1	-5/0	
$\sum\lvert I_{INJ(PIN)}\rvert$	Total injected current (sum of all I/Os and control pins)(5)	25	

1. All main power (V_{DD}, V_{DDRF}, V_{DDA}, V_{DDUSB}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count packages.
3. Positive injection (when V_{IN} > V_{DD}) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by V_{IN} < V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 20: Voltage characteristics* for the maximum allowed input voltage values.

5. W当多个输入被提交到一个电流注入中，最大 ∑|IINJ(PIN)| 是负载电流 (瞬时值)的绝对总和。 e
inj

表22. 热特性

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	130	

6.3 工作条件

6.3.1 主要性能总结

表 23. 主要性能在 VDD = 3.3 V

Parameter			Test conditions	Typ	Unit
I_{CORE}	Core current consumption		VBAT (V_{BAT} = 1.8 V, V_{DD} = 0 V)	0.002	µA
			Shutdown (V_{DD} = 1.8 V)	0.013	
			Standby (V_{DD} = 1.8 V, 32 Kbytes RAM retention)	0.320	
			Stop2	1.85	
			Sleep (16 MHz)	740	
			LP run (2 MHz)	320	
			Run (64 MHz)	5000	
			Radio RX(1)	4500	
			Radio TX 0 dBm output power(1)	5200	
I_{PERI}	Peripheral current consumption	BLE	Advertising with Stop 2(2) (Tx = 0 dBm; Period 1.28 s; 31 bytes, 3 channels)	13	
			Advertising with Stop 2(2) (Tx = 0 dBm, 6 bytes; period 10.24 s, 3 channels)	4	
		LP timers	-	6	
		I2C3	-	7.1	
		LPUART	-	7.7	
		RTC	-	2.5	

1. Power consumption including RF subsystem and digital processing.
2. Power consumption integrated over 100 s, including Cortex-M4, RF subsystem, digital processing and Cortex-M0+.

6.3.2 通用运行条件

表24. 通用工作条件

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	64	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	64	
f_{PCLK2}	Internal APB2 clock frequency	-	0	64	
V_{DD}	Standard operating voltage	-	1.71(1)(2)	3.6	V
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	
		VREFBUF used	2.4		
		ADC, COMP, VREFBUF not used	0		
V_{BAT}	Backup operating voltage	-	1.55	3.6	

表24. 通用工作条件 (继续)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{FBSMPS}	SMPS Feedback voltage	-	1.4	3.6	V
V_{DDRF}	Minimum RF voltage	-	1.71	3.6	
V_{DDUSB}	USB supply voltage	USB used	3.0	3.6	
		USB not used	0	3.6	
V_{IN}	I/O input voltage	TT_xx I/O	–0.3	V_{DD} + 0.3	
		All I/O except TT_xx	–0.3	min (min (V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) + 3.6 V, 5.5 V)(3)(4)	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(5)	UFQFPN48	-	803	mW
		VFQFPN68	-	425	
		WLCSP100	-	558	
		UFBGA129	-	481	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(6)		105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	–40	105	
		Low-power dissipation(6)		125	
T_J	Junction temperature range	Suffix 6 version	–40	105	
		Suffix 7 version		125	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. 当 VDDmin 低于 1.95 V 时，SMPS 的运行模式必须通过启用 BORH 配置来强制进入绕过模式，或者 SMPS 不应该被启用。
3. 这个公式只能应用于与 IO 结构相关的电源，IO 结构由引脚定义表描述。

   最大 I/O 输入电压是 VDD, VDDA, VDDUSB, VLCD 的最小值，不超过 6 V 和 5.5 V。
4. 对于电压高于最小 (V 的操作 $_{DD}$, V_{DDA}, V_{DDUSB} , V_{LCD}) + 0.3 V，内部上拉下拉电阻必须禁用。
5. 如果 T_A较低，更高的 P_D值被允许，只要 T_J不超过 T_J最大 (参见 第 7.5 节： *Therma* *l* 特性).

在低功耗散状态下，T可以扩展到这个范围，只要J不超过Jmax。见节7.5。
热特性).

6.3.3 RF BLE 特性

RF 特性在 1 Mbps 下给出，除非另有说明。

表25. RF 发射器 BLE 特性

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_{op}	Frequency operating range	-	2402	-	2480	MHz
F_{xtal}	Crystal frequency	-	-	32	-	
ΔF	Delta frequency	-	-	250	-	kHz

表25. RF 发射器 BLE 特性 (继续)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Rgfsk	On Air data rate	-	-	1	2	Mbps
PLLres	RF channel spacing	-	-	2	-	MHz

表26. RF 发射器 BLE 特性 (1 Mbps)(1)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
P_{rf}	Maximum output power		SMPS Bypass or ON (V_{FBSMPS} = 1.7 V and V_{DD} > 1.95 V)(2)	-	6.0	-	dBm
			SMPS Bypass (V_{DD} > 1.71 V) or ON (V_{FBSMPS} = 1.4 V and V_{DD} > 1.95 V), Code 29(2)	-	3.7	-	
	0 dBm output power		-	-	0	-	
	Minimum output power		-	-	-20	-	
P_{band}	Output power variation over the band		Tx = 0 dBm - Typical	-0.5	-	0.4	dB
BW6dB	6 dB signal bandwidth		Tx = maximum output power	-	670	-	kHz
IBSE	In band spurious emission	2 MHz	Bluetooth® Low Energy: -20 dBm	-	-50	-	dBm
		≥ 3 MHz	Bluetooth® Low Energy: -30 dBm	-	-53	-	
f_d	Frequency drift		Bluetooth® Low Energy: ±50 kHz	-50	-	+50	kHz
maxdr	Maximum drift rate		Bluetooth® Low Energy: ±20 kHz / 50 µs	-20	-	+20	kHz/ 50 µs
fo	Frequency offset		Bluetooth® Low Energy: ±150 kHz	-150	-	+150	kHz
Δf1	Frequency deviation average		Bluetooth® Low Energy: between 225 and 275 kHz	225	-	275	
Δfa	Frequency deviation Δf2 (average) / Δf1 (average)		Bluetooth® Low Energy:> 0.80	0.80	-	-	-
OBSE(3)	Out of band spurious emission	< 1 GHz	-	-	-61	-	dBm
		≥ 1 GHz	-	-	-46	-	

1. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.
2. V_{FBSMPS} and V_{DD} must be set to different voltage levels, depending upon the desired TX signal (see AN5246 *Usage of SMPS on STM32WB Series microcontrollers*, available on www.st.com).
3. Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

表27. RF 发射器 BLE 特性 (2 Mbps)(1)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
P_{rf}	Maximum output power		SMPS Bypass or ON (V_{FBSMPS} = 1.7 V and V_{DD} > 1.95 V)(2)	-	6.0	-	dBm
			SMPS Bypass or ON (V_{FBSMPS} = 1.4 V and V_{DD} > 1.71 V), Code 29(2)	-	3.7	-	
	0 dBm output power		-	-	0	-	
	Minimum output power		-	-	-20	-	
P_{band}	Output power variation over the band		Tx = 0 dBm - Typical	-0.5	-	0.4	dB
BW6dB	6 dB signal bandwidth		Tx = maximum output power	-	670	-	kHz
IBSE	In band spurious emission	4 MHz	Bluetooth® Low Energy: -20 dBm	-	-56	-	dBm
		5 MHz	Bluetooth® Low Energy: -20 dBm	-	-57	-	
		≥ 6 MHz	Bluetooth® Low Energy: -30 dBm		-58		
f_d	Frequency drift		Bluetooth® Low Energy: ±50 kHz	-50	-	50	kHz
maxdr	Maximum drift rate		Bluetooth® Low Energy: ±20 kHz / 50 µs	-20	-	20	kHz/ 50 µs
fo	Frequency offset		Bluetooth® Low Energy: ±150 kHz	-150	-	150	kHz
Δf1	Frequency deviation average		Bluetooth® Low Energy: between 450 and 550 kHz	450	-	550	
Δfa	Frequency deviation Δf2 (average) / Δf1 (average)		Bluetooth® Low Energy:> 0.80	0.80	-	-	-
OBSE(3)	Out of band spurious emission	< 1 GHz	-	-	-61	-	dBm
		≥ 1 GHz	-	-	-46	-	

1. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.
2. V_{FBSMPS} and V_{DD} must be set to different voltage levels, depending upon the desired TX signal (see AN5246 *Usage of SMPS on STM32WB Series microcontrollers*, available on *www.st.com*).
3. Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

表28. 无线电接收器 蓝牙特性 (1 Mbps)

Symbol	Parameter	Test conditions	Typ	Unit
Prx_max	Maximum input signal	PER <30.8% Bluetooth® Low Energy: min -10 dBm	0	dBm
Psens(1)	High sensitivity mode (SMPS Bypass)	PER <30.8% Bluetooth® Low Energy: max -70 dBm	-96	
	High sensitivity mode (SMPS ON)		-95.5	
$Rssi_{maxrange}$	RSSI maximum value	-	-7	
$Rssi_{minrange}$	RSSI minimum value	-	-94	
$Rssi_{accu}$	RSSI accuracy	-	2	dB
C/Ico	Co-channel rejection	Bluetooth® Low Energy: 21 dB	8	
C/I	Adjacent channel interference	Adj ≥ 5 MHz Bluetooth® Low Energy: -27 dB	-53	
		Adj ≤ -5 MHz Bluetooth® Low Energy: -27 dB	-53	
		Adj = 4 MHz Bluetooth® Low Energy: -27 dB	-48	
		Adj = -4 MHz Bluetooth® Low Energy: -15 dB	-33	
		Adj = 3 MHz Bluetooth® Low Energy: -27 dB	-46	
		Adj = 2 MHz Bluetooth® Low Energy: -17 dB	-39	
		Adj = -2 MHz Bluetooth® Low Energy: -15 dB	-35	
		Adj = 1 MHz Bluetooth® Low Energy: 15 dB	-2	
		Adj = -1 MHz Bluetooth® Low Energy: 15 dB	2	
C/Image	Image rejection (F_{image} = -3 MHz)	Bluetooth® Low Energy: -9 dB	-29	
P_IMD	Intermodulation	|f2-f1| = 3 MHz Bluetooth® Low Energy: -50 dBm	-34	dBm
		|f2-f1| = 4 MHz Bluetooth® Low Energy: -50 dBm	-30	
		|f2-f1| = 5 MHz Bluetooth® Low Energy: -50 dBm	-32	

Table 28. RF receiver 蓝牙特性 (1 Mbps) (continued)

Symbol	Parameter	Test conditions	Typ	Unit
P_OBB	Out of band blocking	30 to 2000 MHz Bluetooth® Low Energy: -30 dBm	-3	dBm
		2003 to 2399 MHz Bluetooth® Low Energy: -35 dBm	-5	
		2484 to 2997 MHz Bluetooth® Low Energy: -35 dBm	-2	
		3 to 12.75 GHz Bluetooth® Low Energy: -30 dBm	7	

1. With ideal TX.

Table 29. RF receiver 蓝牙特性 (2 Mbps)

Symbol	Parameter	Test conditions	Typ	Unit
Prx_max	Maximum input signal	PER <30.8% Bluetooth® Low Energy: min -10 dBm	0	dBm
Psens(1)	High sensitivity mode (SMPS Bypass)	PER <30.8% Bluetooth® Low Energy: max -70 dBm	-93	
	High sensitivity mode (SMPS ON)		-92.5	
$Rssi_{maxrange}$	RSSI maximum value	-	-7	
$Rssi_{minrange}$	RSSI minimum value	-	-94	
$Rssi_{accu}$	RSSI accuracy	-	2	dB
C/Ico	Co-channel rejection	Bluetooth® Low Energy spec: 21 dB	9	
C/I	Adjacent channel interference	Adj ≥ 8MHz Bluetooth® Low Energy: -27 dB	-53	
		Adj ≤ -8 MHz Bluetooth® Low Energy: -27 dB	-50	
		Adj = 6 MHz Bluetooth® Low Energy: -27 dB	-49	
		Adj = -6 MHz Bluetooth® Low Energy: -15 dB	-46	
		Adj = 4 MHz Bluetooth® Low Energy: -17 dB	-42	
		Adj = 2 MHz Bluetooth® Low Energy:15 dB	-3	
		Adj = -2 MHz Bluetooth® Low Energy:15 dB	-3	
C/Image	Image rejection (F_{image} = -4 MHz)	Bluetooth® Low Energy: -9 dB	-26	

表29. 射频接收器 蓝牙特性 (2 Mbps) (continued)

Symbol	Parameter	Test conditions	Typ	Unit
P_IMD	Intermodulation	|f2-f1| = 6 MHz Bluetooth® Low Energy: -50 dBm	-29	dBm
		|f2-f1| = 8 MHz Bluetooth® Low Energy: -50 dBm	-30	
		|f2-f1| = 10 MHz Bluetooth® Low Energy: -50 dBm	-29	
P_OBB	Out of band blocking	30 to 2000 MHz Bluetooth® Low Energy: -30 dBm	-3	
		2003 to 2399 MHz Bluetooth® Low Energy: -35 dBm	-9	
		2484 to 2997 MHz Bluetooth® Low Energy: -35 dBm	-3	
		3 to 12.75 GHz Bluetooth® Low Energy: -30 dBm	4	

1. With ideal TX.

表30. VDD = 3.3 V(1) 蓝牙 RF 功率消耗

Symbol	Parameter	Typ	Unit
I_{txmax}	TX maximum output power consumption (SMPS Bypass)	12.7	mA
	TX maximum output power consumption (SMPS On, V_{FBSMPS} = 1.7 V)	7.8	
I_{tx0dbm}	TX 0 dBm output power consumption (SMPS Bypass)	8.8	
	TX 0 dBm output power consumption (SMPS On, V_{FBSMPS} = 1.4 V)	5.2	
I_{rxlo}	Rx consumption (SMPS Bypass)	7.9	
	Rx consumption (SMPS On, V_{FBSMPS} = 1.4 V)	4.5	

1. Power consumption including RF subsystem and digital processing.

6.3.4 RF 802.15.4 特性

表31. RF 发射器 802.15.4 特性 istics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{op}	Frequency operating range	-	2405	-	2480	MHz
F_{xtal}	Crystal frequency	-	-	32	-	
ΔF	Delta frequency	-	-	5	-	
Roqpsk	On air data rate	-	-	250	-	kbps
PLLres	RF channel spacing	-	-	5	-	MHz

表31. RF 发射器 802.15.4 特性 (继续)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Prf	Maximum output power(1)	SMPS Bypass or ON (V_{FBSMPS} = 1.7 V and V_{DD} > 1.95 V)	-	5.7	-	dBm
		SMPS Bypass (V_{DD} > 1.71 V) or ON (V_{FBSMPS} = 1.4 V and V_{DD} > 1.95 V)	-	3.7	-	
	0 dBm output power	-	-	0	-	
	Minimum output power	-	-	-20	-	
Pband	Output power variation over the band	Tx = 0 dBm - Typical	-0.5	-	0.4	dB
EVMrms	EVM rms	Pmax	-	8	-	%
Txpd	Transmit power density	|f - fc| > 3.5 MHz	-	-35	-	dB

1. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

表32. RF 接收器 802.15.4 特性

Symbol	Parameter	Conditions	Typ	Unit
Prx_max	Maximum input signal	Min: -20 dBm and PER < 1%	-10	dBm
Rsens	Sensitivity (SMPS Bypass)	Max: -85 dBm and PER < 1%	-100	
	Sensitivity (SMPS ON)		-98	
C/adj	Adjacent channel rejection	-	35	dB
C/alt	Alternate channel rejection	-	46	

图19. 典型链路质量指标代码与接收级别比较

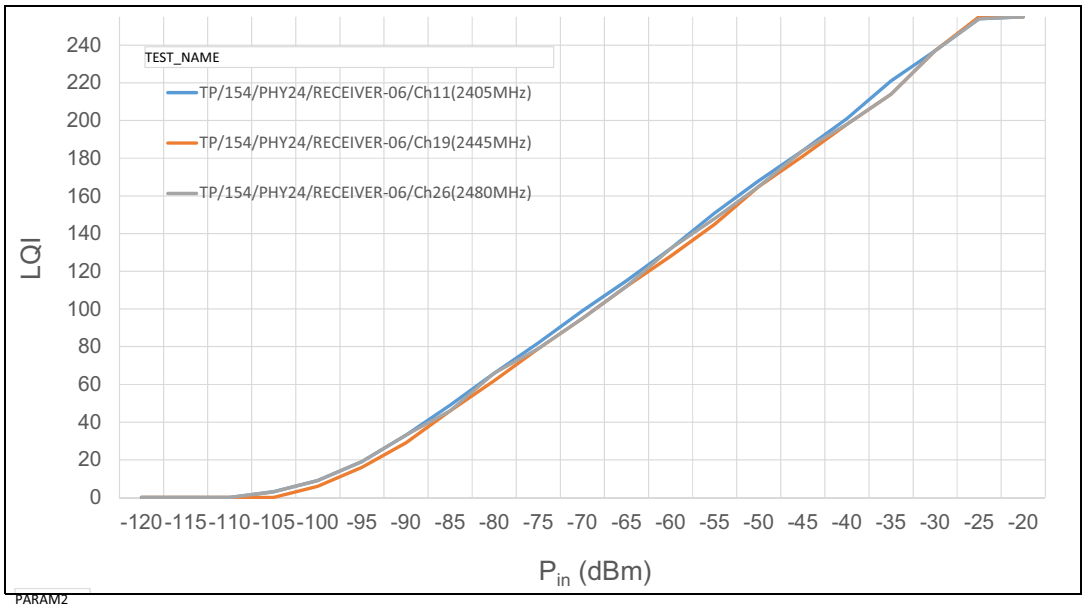


图20. 典型能量检测 (T = 27°C, VDD = 3.3 V)

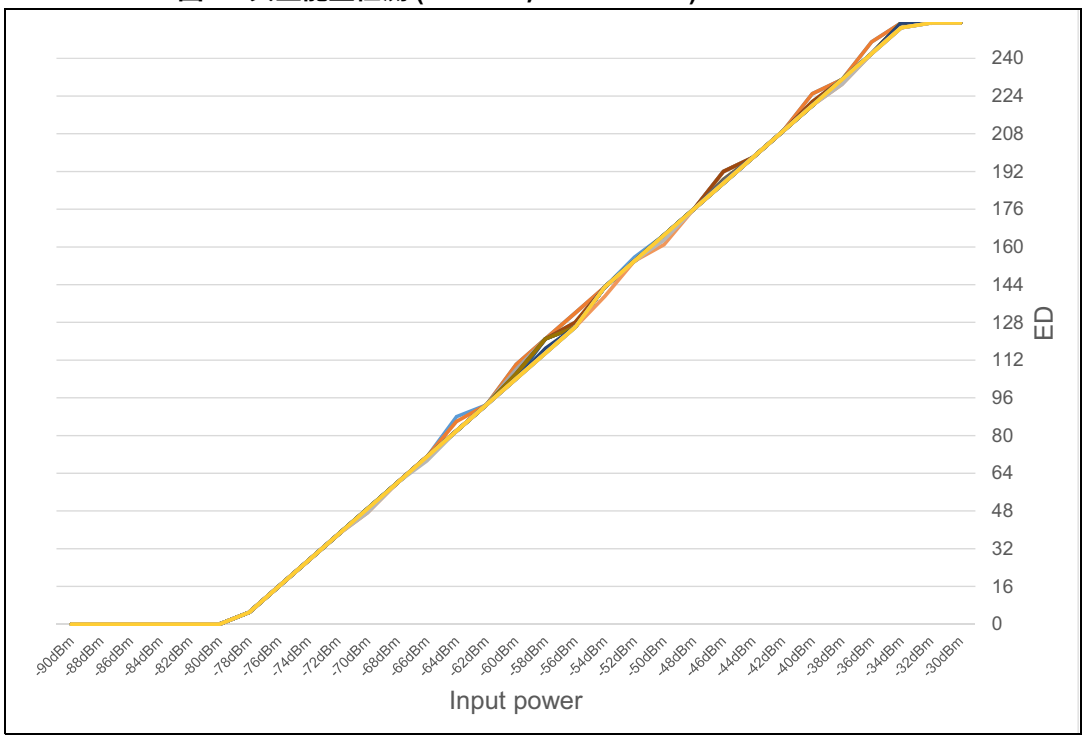


表33. RF 802.15.4 功率消耗 для VDD = 3.3 V(1)

Symbol	Parameter	Typ	Unit
I_{txmax}	TX maximum output power consumption (SMPS Bypass)	11.7	mA
	TX maximum output power consumption (SMPS On, V_{FBSMPS} = 1.7 V)	6.5	
I_{tx0dbm}	TX 0 dBm output power consumption (SMPS Bypass)	9.1	
	TX 0 dBm output power consumption (SMPS On, V_{FBSMPS} = 1.4 V)	4.5	
I_{rxlo}	Rx consumption (SMPS Bypass)	9.2	
	Rx consumption (SMPS On)	4.5	

1. Power consumption including RF subsystem and digital processing.

6.3.5 上电/下电工作条件

The parameters given in 表 *34* are derived from tests performed under the ambienttemperature condition summarized in 表 *24*.

Table 34. 上电/下电工作条件

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	-	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	-	0	∞	
	V_{DDUSB} fall time rate		10	∞	
t_{VDDRF}	V_{DDRF} rise time rate	-	-	∞	
	V_{DDRF} fall time rate		-	∞	

6.3.6 嵌入式复位和电源控制块特性

给定的参数在表 *35*中，是在表 *24*：通用运行条件中总结的环境温度条件下进行的测试中获得的。

Table 35. 嵌入式复位和电源控制块特性

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$t_{RSTTEMPO}$[2]	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}[2]	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.70	V
		Falling edge	1.60	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.10	2.14	
		Falling edge	1.96	2.00	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.10	2.15	2.19	
		Falling edge	2.00	2.05	2.10	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	
		Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	
		Falling edge	2.31	2.36	2.41	

表 35. 嵌入式复位和电源控制块特性 (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	
I_{DD} (BOR_PVD)[2]	BOR[3] (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	µA
V_{PVM1}	V_{DDUSB} peripheral voltage monitoring	-	1.18	1.22	1.26	V
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	
		Falling edge	1.6	1.64	1.68	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM1}	PVM1 hysteresis	-	-	10	-	
I_{DD} (PVM1)[2]	PVM1 consumption from V_{DD}	-	-	0.2	-	µA
I_{DD} (PVM3)[2]	PVM3 consumption from V_{DD}	-	-	2	-	

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

6.3.7 内置电压参考

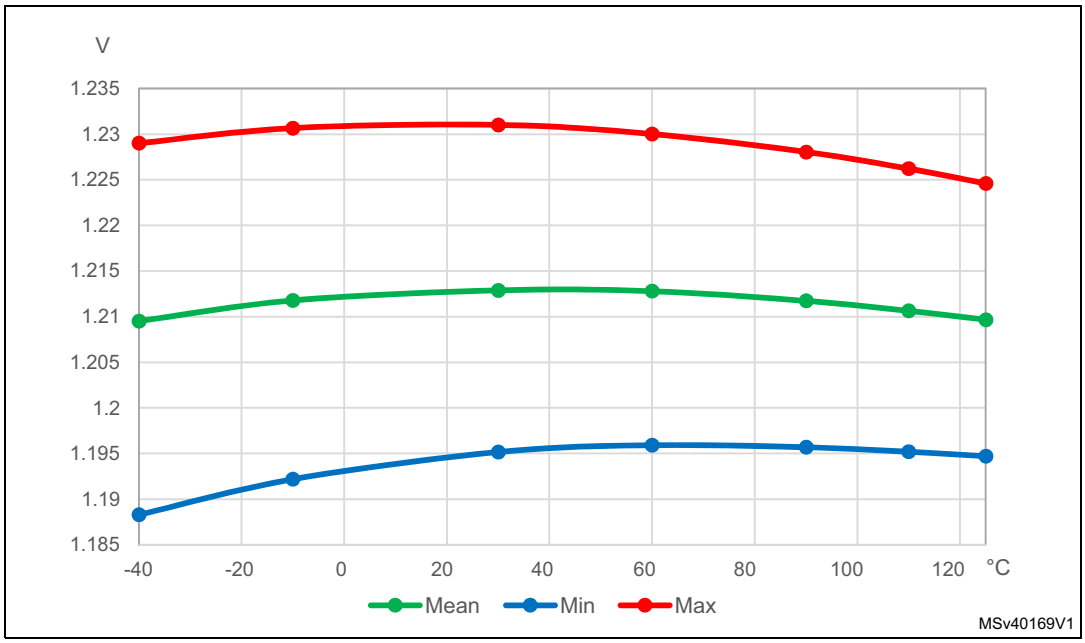
给定的参数在表 *36*是基于在表 *24*：通用运行条件总结的环境温度和供电电压条件下进行的测试得出的。

表 36. 嵌入式内部电压参考

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +125 °C	1.182	1.212	1.232	V
$t_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enabled	-	-	8	12(2)	
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
T_{Coeff}	Temperature coefficient	–40 °C < T_A < +125 °C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25 °C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

图 21. VREFINT 与温度比较



6.3.8 电源电流特性

电流消耗是一个函数，取决于多个参数和因素，例如工作电压、环境温度、I/O引脚负荷、设备软件配置、工作频率、I/O引脚切换速率、程序在内存中的位置和执行的二进制代码。

电流消耗是按照 图*18*：电流消耗测量方案所述进行测量的。

典型和最大电流消耗

MCU 会在以下条件下运行：

- 所有 I/O 引脚处于模拟输入模式
- 除非明确提及，否则所有外围设备都被禁用
- Flash 内存访问时间根据 fHCLK 频率调整为最小的等待状态数 (参考表格“CPU 时钟对应的等待状态数 (HCLK) 频率”可在参考手册中找到).
- 当外围设备启用时 fPCLK = fHCLK
- 为 Flash 内存和共享外围设备 fPCLK = fHCLK = fHCLKS

参数来自 表*37*到 表*48*，这些参数是在环境温度和供电电压条件下进行的测试得出的，详见 表*24*：通用运行条件。

Table 37. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF), V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ				Max(1)			Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HCLK} = f_{HSE}$ = 32 MHz f_{HSI16} + PLL ON above 32 MHz All peripherals disabled	Range 2	16 MHz	1.90	1.90	2.00	2.20	2.40	2.52	2.96	mA
				2 MHz	0.960	0.985	1.10	1.25	1.25	1.57	2.05	
			Range 1	64 MHz	8.15	8.25	8.40	8.60	9.30	9.60	10.02	
				32 MHz	4.20	4.25	4.40	4.65	4.25	4.63	5.17	
				16 MHz	2.25	2.30	2.40	2.65	2.65	2.91	3.52	
			SMPS Range 1	64 MHz	5.00	5.00	5.10	5.20	-	-	-	
				32 MHz	3.15	3.15	3.25	3.35	-	-	-	
				16 MHz	2.30	2.30	2.35	2.45	-	-	-	
I_{DD}(LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled		2 MHz	0.335	0.360	0.470	0.670	0.480	0.910	1.47	
				1 MHz	0.170	0.210	0.325	0.520	0.270	0.730	1.31	
				400 kHz	0.0815	0.120	0.230	0.425	0.140	0.590	1.18	
				100 kHz	0.0415	0.076	0.190	0.385	0.070	0.550	1.14	

1. Guaranteed by characterization results unless otherwise specified.

Table 38. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ				Max(1)			Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HCLK} = f_{HSE}$ = 32 MHz f_{HSI16} + PLL ON above 32 MHz All peripherals disabled	Range 2	16 MHz	2.00	2.05	2.15	2.30	2.57	3.04	3.64	mA
				2 MHz	0.970	1.00	1.10	1.25	1.62	1.90	2.55	
			Range 1	64 MHz	8.80	8.90	9.00	9.20	10.50	10.80	11.30	
				32 MHz	4.50	4.55	4.70	4.90	4.63	4.89	5.62	
				16 MHz	2.40	2.40	2.55	2.70	2.50	2.70	3.21	
			SMPS Range 1	64 MHz	5.25	5.30	5.35	5.45	-	-	-	
				32 MHz	3.25	3.25	3.35	3.45	-	-	-	
				16 MHz	2.35	2.35	2.40	2.45	-	-	-	
I_{DD}(LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled		2 MHz	0.265	0.285	0.385	0.550	0.440	0.940	1.620	
				1 MHz	0.135	0.170	0.270	0.430	0.290	0.760	1.480	
				400 kHz	0.066	0.097	0.195	0.360	0.200	0.670	1.380	
				100 kHz	0.031	0.0625	0.160	0.325	0.170	0.470	1.330	

1. Guaranteed by characterization results, unless otherwise specified.

表39. 在运行和低功耗运行模式下的典型电流消耗，不同代码从闪存运行，ART启用 (缓存开启预取关闭), VDD= 3.3 V

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, f_{HSI16} + PLL ON above 32 MHz All peripherals disable	Range 2 f_{HCLK} = 16 MHz	Reduced code(1)	1.90	mA	119	µA/MHz
				Coremark	1.85		116	
				Dhrystone 2.1	1.85		116	
				Fibonacci	1.75		109	
				While(1)	1.60		100	
			Range 1 f_{HCLK} = 64 MHz	Reduced code(1)	8.15	mA	127	µA/MHz
				Coremark	8.00		125	
				Dhrystone 2.1	8.10		127	
				Fibonacci	7.60		119	
				While(1)	6.85		107	
			Range 1, SMPS On f_{HCLK} = 64 MHz	Reduced code(1)	5.00	mA	78	µA/MHz
				Coremark	4.95		77	
				Dhrystone 2.1	4.95		77	
				Fibonacci	4.75		74	
				While(1)	4.40		69	
			Range 1, SMPS On f_{HCLK} = 64 MHz, When RF Tx level = 0 dBm(2)	Reduced code(1)	4.07	mA	64	µA/MHz
				Coremark	3.99		62	
				Dhrystone 2.1	4.04		63	
				Fibonacci	3.79		59	
				While(1)	3.42		53	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2 MHz All peripherals disable		Reduced code(1)	320	µA	160	µA/MHz
				Coremark	350		175	
				Dhrystone 2.1	350		175	
				Fibonacci	390		195	
				While(1)	225		113	

1. Reduced code used for characterization results provided in *Table 37* and *Table 38*.
2. Value computed. MCU consumption when RF TX and SMPS are ON.

表40. 典型电流消耗在运行和低功运行模式下，不同代码从SRAM1运行，VDD = 3.3 V

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, f_{HSI16} + PLL ON above 32 MHz All peripherals disable	Range 2 f_{HCLK} = 16 MHz	Reduced code(1)	2.00	mA	125	µA/MHz
				Coremark	1.75		109	
				Dhrystone 2.1	1.95		122	
				Fibonacci	1.85		116	
				While(1)	1.85		116	
			Range 1 f_{HCLK} = 64 MHz	Reduced code(1)	8.80	mA	138	µA/MHz
				Coremark	7.50		117	
				Dhrystone 2.1	8.60		134	
				Fibonacci	7.90		123	
				While(1)	8.00		125	
			Range 1, SMPS On f_{HCLK} = 64 MHz	Reduced code(1)	5.25	mA	82	µA/MHz
				Coremark	4.65		73	
				Dhrystone 2.1	5.15		80	
				Fibonacci	4.85		76	
				While(1)	4.90		77	
			Range 1, SMPS On f_{HCLK} = 64 MHz, When RF Tx level = 0 dBm(2)	Reduced code(1)	4.39	mA	69	µA/MHz
				Coremark	3.74		58	
				Dhrystone 2.1	4.29		67	
				Fibonacci	3.94		62	
				While(1)	3.99		62	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2 MHz All peripherals disable		Reduced code(1)	255	µA	128	µA/MHz
				Coremark	205		103	
				Dhrystone 2.1	250		125	
				Fibonacci	230		115	
				While(1)	220		110	

1. Reduced code used for characterization results provided in *Table 37* and *Table 38*.
2. Value computed. MCU consumption when RF TX and SMPS are ON.

Table 41. Current consumption in Sleep and Low-power sleep modes Flash memory ON

Symbol	Parameter	Conditions			TYP				MAX(1)			Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DD}(Sleep)	Supply current in sleep mode,	f_{HCLK} = f_{HSI16} up to 16 MHz included, f_{HCLK} = f_{HSE} up to 32 MHz f_{HSI16} + PLL ON above 32 MHz All peripherals disabled	Range 2	16 MHz	0.740	0.765	0.865	1.05	0.840	1.210	1.810	mA
			Range 1	64 MHz	2.65	2.70	2.80	3.00	3.00	3.33	3.91	
				32 MHz	1.40	1.45	1.60	1.80	1.55	1.86	2.49	
				16 MHz	0.845	0.875	0.990	1.20	0.970	1.40	2.02	
			SMPS Range 1	64 MHz	2.60	2.60	2.65	2.75	-	-	-	
				32 MHz	1.90	1.95	2.00	2.10	-	-	-	
				16 MHz	1.70	1.70	1.75	1.80	-	-	-	
I_{DD}(LPSleep)	Supply current in low-power sleep mode	f_{HCLK} = f_{MSI} All peripherals disabled		2 MHz	0.090	0.125	0.235	0.430	0.130	0.600	1.19	
				1 MHz	0.058	0.093	0.205	0.400	0.090	0.570	1.16	
				400 kHz	0.044	0.0725	0.185	0.380	0.070	0.540	1.11	
				100 kHz	0.0315	0.0635	0.0175	0.370	0.055	0.530	1.13	

1. Guaranteed by characterization results, unless otherwise specified.

Table 42. Current consumption in Low-power sleep modes, Flash memory in Power down

Symbol	Parameter	Conditions		TYP				MAX(1)			Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DD} (LPSleep)	Supply current in low-power sleep mode	f_{HCLK} = f_{MSI} All peripherals disabled	2 MHz	94.0	115	200	335	135	610	1201	µA
			1 MHz	56.5	86.0	170	305	94.2	560	1171	
			400 kHz	40.5	66.5	150	285	68.0	540	1129	
			100 kHz	27.5	57.5	140	275	54.6	539	1131	

1. Guaranteed by characterization results, unless otherwise specified.

Table 43. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	LCD disabled BLE disabled	1.8 V	1.00	1.85	3.15	5.95	21.5	50.0	1.58	4.12	56.9	132.7	µA
			2.4 V	1.10	1.85	3.20	6.00	22.0	51.0	-	-	-	-	
			3.0 V	1.10	1.85	3.25	6.10	22.0	52.0	1.60	4.17	57.9	135.6	
			3.6 V	1.15	1.95	3.35	6.25	23.0	53.0	1.69	4.40	58.6	135.7	
		LCD enabled(2) and clocked by LSI BLE disabled	1.8 V	1.20	2.00	3.35	6.10	22.0	50.5	1.76	4.30	57.1	133.3	
			2.4 V	1.20	2.00	3.40	6.20	22.0	51.0	-	-	-	-	
			3.0 V	1.25	2.10	3.45	6.30	22.5	52.0	1.85	4.41	58.1	135.8	
			3.6 V	1.30	2.15	3.60	6.55	23.0	53.5	1.97	4.66	59.4	136.6	
I_{DD} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled, BLE disabled	RTC clocked by LSI, LCD disabled	1.8 V	1.30	2.10	3.45	6.25	22.0	50.5	1.91	4.50	57.2	133.0	
			2.4 V	1.45	2.25	3.55	6.40	22.5	51.5	-	-	-	-	
			3.0 V	1.50	2.30	3.70	6.55	22.5	52.5	2.11	4.64	58.3	136.1	
			3.6 V	1.75	2.50	3.95	6.85	23.5	53.5	2.26	5.12	59.7	136.9	
		RTC clocked by LSI, LCD enabled(2)	1.8 V	1.35	2.20	3.55	6.30	22.0	50.5	1.99	4.57	57.4	133.8	
			2.4 V	1.50	2.35	3.65	6.50	22.5	51.5	-	-	-	-	
			3.0 V	1.70	2.45	3.85	6.65	23.0	52.5	2.17	4.87	58.4	136.3	
			3.6 V	1.80	2.60	4.05	6.95	23.5	54.0	2.41	5.11	59.9	137.1	
		RTC clocked by LSE quartz(3) in low drive mode	1.8 V	1.35	2.20	3.50	6.25	22.0	50.5	1.91	4.29	57.1	133.5	
			2.4 V	1.45	2.25	3.65	6.40	22.5	51.5	-	-	-	-	
			3.0 V	1.55	2.45	3.80	6.65	23.0	52.5	2.01	4.31	58.0	135.9	
			3.6 V	1.70	2.55	4.05	6.95	23.5	54.0	2.16	4.40	81.6	137.0	

Table 43. Current consumption in Stop 2 mode (continued)

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (wakeup from Stop 2)	Supply current during wakeup from Stop 2 mode bypass mode	Wakeup clock is HSI16, voltage Range 2. See(4).	3.0 V	-	389	-	-	-	-	-	-	-	-	µA
		Wakeup clock is MSI = 32 MHz, voltage Range 1. See(4).	3.0 V	-	320	-	-	-	-	-	-	-	-	
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See(4).	3.0 V	-	528	-	-	-	-	-	-	-	-	

1. Guaranteed based on test during characterization, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash memory. Average value given for a typical wakeup time as specified in *Table 51: Low-power mode wakeup timings*.

Table 44. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Stop 1)	Supply current in Stop 1 mode, RTC disabled	BLE disabled LCD disabled	1.8 V	5.05	9.20	15.5	28.0	96.0	210	7.00	28.4	343.7	738.6	µA
			2.4 V	5.10	9.25	15.5	28.5	96.5	215	-	-	-	-	
			3.0 V	5.15	9.30	15.5	28.5	97.0	215	7.07	28.5	346.8	746.0	
			3.6 V	5.25	9.45	16.0	29.0	97.5	215	7.30	28.8	351.0	749.4	
		BLE disabled LCD enabled(2), clocked by LSI	1.8 V	5.05	9.30	15.5	28.5	96.0	210	7.10	28.7	344.4	739.0	
			2.4 V	5.10	9.35	16.0	28.5	96.5	215	-	-	-	-	
			3.0 V	5.20	9.65	16.0	28.5	97.0	215	7.26	29.6	345.0	747.0	
			3.6 V	5.55	9.85	16.0	29.0	98.5	215	7.62	29.8	349.0	750.8	
I_{DD} (Stop 1 with RTC)	Supply current in Stop 1 mode, RTC enabled, BLE disabled	RTC clocked by LSI LCD disabled	1.8 V	5.30	9.35	16.0	28.5	96.5	215	7.30	29.5	343.7	739.2	
			2.4 V	5.40	9.45	16.0	28.5	97.0	215	-	-	-	-	
			3.0 V	5.70	9.55	16.5	29.0	98.5	220	7.69	29.7	347.2	746.1	
			3.6 V	5.85	10.0	16.5	29.5	96.5	215	8.08	29.8	349.9	751.1	
		RTC clocked by LSI LCD enabled(2)	1.8 V	5.25	9.60	16.0	28.5	96.5	215	7.10	29.0	344.3	739.9	
			2.4 V	5.30	9.75	16.0	29.0	97.0	215	-	-	-	-	
			3.0 V	5.85	9.80	16.5	29.0	97.5	215	7.53	29.8	347.4	746.2	
			3.6 V	5.90	10.5	16.5	29.0	98.5	220	8.18	29.9	350.6	751.8	
		RTC clocked by LSE quartz(3) in Low drive mode	1.8 V	5.35	9.55	16.0	28.5	96.5	215	6.00	28.7	343.9	738.7	
			2.4 V	5.40	9.70	16.0	29.0	96.5	215	-	-	-	-	
			3.0 V	5.75	9.70	16.0	29.0	97.5	215	7.40	28.9	346.6	743.8	
			3.6 V	5.90	10.0	16.5	29.5	99.0	220	7.58	29.2	349.0	749.9	

Table 44. Current consumption in Stop 1 mode (continued)

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (wakeup from Stop1)	Supply current during wakeup from Stop 1 bypass mode	Wakeup clock HSI16, voltage Range 2. See (4).	3.0 V	-	129	-	-	-	-	-	-	-	-	µA
		Wakeup clock MSI = 32 MHz, voltage Range 1. See (4).	3.0 V	-	124	-	-	-	-	-	-	-	-	
		Wakeup clock MSI = 4 MHz, voltage Range 2. See (4).	3.0 V	-	207	-	-	-	-	-	-	-	-	

1. Guaranteed based on test during characterization, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 51: Low-power mode wakeup timings*.

Table 45. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Stop 0)	Supply current in Stop 0 mode, RTC disabled, BLE disabled, LCD disabled	--	1.8 V	95.5	100	110	120	195	315	110.0	114.2	458.1	874.8	µA
			2.4 V	97.5	105	110	125	195	315	-	-	-	-	
			3.0 V	98.5	105	110	125	195	320	117.3	134.3	461.8	880.0	
			3.6 V	100	105	115	125	200	320	165.0	135.7	494.0	884.1	
	Supply current during wakeup from Stop 0 Bypass mode	Wakeup clock HSI16, voltage Range 2. See (2).	3.0 V	-	331	-	-	-	-	-	-	-	-	
		Wakeup clock is MSI = 32 MHz, voltage Range 1. See (2).	3.0 V	-	349	-	-	-	-	-	-	-	-	
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See (2).	3.0 V	-	196	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Wakeup with code execution from Flash memory. Average value given for a typical wakeup time as specified in *Table 51: Low-power mode wakeup timings*.

Table 46. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Standby)	Supply current in Standby mode (backup registers and SRAM2a retained), RTC disabled	BLE disabled No independent watchdog	1.8 V	0.270	0.320	0.515	0.920	3.45	8.20	0.300	0.828	7.850	19.300	µA
			2.4 V	0.270	0.350	0.540	0.955	3.50	8.80	-	-	-	-	
			3.0 V	0.270	0.370	0.575	1.00	3.85	9.50	0.380	0.945	8.505	21.200	
			3.6 V	0.300	0.410	0.645	1.15	4.20	10.50	0.400	1.040	8.980	22.400	
		BLE disabled With independent watchdog	1.8 V	0.265	0.525	0.710	1.10	3.90	8.40	0.520	1.095	8.041	19.500	
			2.4 V	0.280	0.595	0.790	1.20	4.00	9.05	-	-	-	-	
			3.0 V	0.290	0.670	0.855	1.35	4.15	9.80	0.730	1.253	8.774	21.400	
			3.6 V	0.295	0.770	0.990	1.50	4.60	11.00	0.851	1.356	9.360	22.840	
I_{DD} (Standby with RTC)	Supply current in Standby mode (backup registers and SRAM2a retained), RTC enabled BLE disabled	RTC clocked by LSI, no independent watchdog	1.8 V	0.500	0.600	0.780	1.20	3.70	8.45	0.680	1.165	8.143	19.660	
			2.4 V	0.630	0.705	0.910	1.30	3.80	9.10	-	-	-	-	
			3.0 V	0.725	0.825	1.050	1.50	3.95	9.90	0.930	1.463	8.977	21.440	
			3.6 V	0.860	0.970	1.200	1.70	4.25	11.00	1.050	1.628	9.634	23.080	
		RTC clocked by LSI, with independent watchdog	1.8 V	0.565	0.655	0.830	1.25	3.75	8.55	0.734	1.196	8.187	19.710	
			2.4 V	0.635	0.790	0.975	1.40	4.10	9.20	-	-	-	-	
			3.0 V	0.725	0.915	1.100	1.55	4.50	10.00	1.028	1.573	9.072	21.810	
			3.6 V	0.870	1.050	1.300	1.80	4.90	11.00	1.144	1.723	9.730	23.200	
		RTC clocked by LSE quartz (2) in low drive mode	1.8 V	0.525	0.625	0.840	1.25	3.75	8.60	0.600	1.061	8.029	19.610	
			2.4 V	0.665	0.755	0.960	1.35	4.05	9.25	-	-	-	-	
			3.0 V	0.775	0.880	1.100	1.55	4.40	10.00	0.600	1.100	8.719	21.570	
			3.6 V	0.935	1.050	1.300	1.80	5.00	11.00	0.750	1.171	9.460	23.030	

Table 46. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (SRAM2a)(3)	Supply current to be subtracted in Standby mode when SRAM2a is not retained	-	1.8 V	0.160	0.210	0.380	0.660	2.30	5.15	-	-	-	-	µA
			2.4 V	0.165	0.245	0.375	0.650	2.15	5.20	-	-	-	-	
			3.0 V	0.155	0.250	0.385	0.630	2.25	5.20	-	-	-	-	
			3.6 V	0.155	0.235	0.375	0.670	2.20	5.20	-	-	-	-	
I_{DD} (wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is HSI16. See (4). SMPS OFF	3.0 V	-	1.73	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. The supply current in Standby with SRAM2a mode is: I_{DD}(Standby) + I_{DD}(SRAM2a). The supply current in Standby with RTC with SRAM2a mode is: I_{DD}(Standby + RTC) + I_{DD}(SRAM2a).
4. Wakeup with code execution from Flash memory. Average value given for a typical wakeup time as specified in *Table 51*.

Table 47. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	1.8 V	0.039	0.013	0.030	0.100	0.635	1.950	-	-	2.099	6.200	µA
			2.4 V	0.059	0.014	0.055	0.120	0.785	2.350	-	-	-	-	
			3.0 V	0.064	0.037	0.070	0.180	1.000	2.900	-	0.185	2.670	7.490	
			3.6 V	0.071	0.093	0.140	0.280	1.300	3.700	-	0.247	3.120	8.450	
I_{DD} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE quartz (2) in low drive mode	1.8 V	0.320	0.315	0.355	0.420	0.985	2.300	-	0.572	2.702	6.180	
			2.4 V	0.425	0.405	0.460	0.540	1.200	2.800	-	-	-	-	
			3.0 V	0.535	0.535	0.595	0.700	1.500	3.450	-	0.664	2.990	7.800	
			3.6 V	0.695	0.720	0.790	0.940	2.000	4.350	-	0.790	3.730	9.140	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 48. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP						MAX(1)						Unit
		-	V_{BAT}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	
I_{DD}(VBAT)	Backup domain supply current	RTC disabled	1.8 V	1.00	2.00	4.00	10.0	52.0	145	-	-	-	-	-	-	nA
			2.4 V	1.00	2.00	5.00	12.0	60.0	165	-	-	-	-	-	-	
			3.0 V	2.00	4.00	7.00	16.0	75.0	225	-	-	-	-	-	-	
			3.6 V	7.00	15.0	23.0	42.0	170	450	-	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz(2)	1.8 V	295	305	315	325	380	480	-	-	-	-	-	-	
			2.4 V	385	395	400	415	475	595	-	-	-	-	-	-	
			3.0 V	495	505	515	530	600	765	-	-	-	-	-	-	
			3.6 V	630	645	660	685	830	1150	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 49. Current under Reset condition

Symbol	Conditions	TYP						MAX(1)						Unit
		0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	
$I_{DD(RST)}$	1.8 V	-	410	-	-	-	-	-	-	-	-	-	-	µA
	2.4 V	-	-	-	-	-	-	-	-	-	-	-	-	
	3.0 V	-	550	-	-	-	-	-	750	-	-	-	-	
	3.6 V	-	750	-	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

I/O系统电流消耗

I/O系统电流消耗有两个组成部分：静态和动态。

I/O静态电流消耗

所有用作带上拉的输入的 I/O 都会在引脚被外部保持低电压时产生电流消耗。这个电流消耗的值可以简单地通过使用 表72：I/O静态特性 中给出的上拉/下拉电阻值来计算。

对于输出引脚，任何外部下拉或外部负载也必须考虑，以估算电流消耗。

额外的I/O电流消耗是由于I/Os配置为输入时，外部应用了中间电压水平所致。这种电流消耗是由于使用输入施密特触发器电路来区分输入值而引起的。除非应用程序需要这种特定配置，否则可以通过将这些I/Os配置为模拟模式来避免这种供电电流消耗。这尤其适用于ADC输入引脚，它们应该配置为模拟输入。

注意: 任何浮动输入引脚都可以定定到中间电压水平，或者由于外部电磁噪声而意外切换。为了避免与浮动引脚相关的电流消耗，它们必须要是配置为模拟模式，或者被内部强制设置为确定的数字值。这可以通过使用上拉/下拉电阻或将引脚配置为输出模式来实现。

I/O动态电流消耗

除了之前测量的内部外围电流消耗之外(参见表*50*：外设电流消耗，应用使用的输入/输出也贡献于电流消耗。当一个输入/输出引脚切换时，它会从输入/输出供电电压中获取电流来为输入/输出引脚电路和电容负荷充电/放电。(内部或外部) 连接到引脚上：

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

- ISW是由切换输入/输出用于充电/放电电容负荷所吸收的电流• VDD是输入/输出供电电压• fSW是输入/输出切换频率• C是输入/输出引脚看到的总电容：C = CIO+ CEXT• CIO是输入/输出引脚电容• CEXT是PCB板电容加上任何连接的外部设备引脚电容。

测试引脚配置为推挽输出模式，并由软件以固定频率切换。

片上外设电流消耗

片上外设电流消耗如下所示:表50. MCU放置在以下条件下:

- 所有 I/O 引脚都在模拟模式下• 给定值是通过测量电流消耗的差异计算得出的：– 当外围设备被时时时钟时– 当外围设备被关闭时时钟时• 环境工作温度和供电电压条件总结在表20: 电压特性• 外围设备数字部分的功率消耗给在表50。外围设备模拟部分的功率消耗(适用时) 在数据手册中相关章节中指示。

表50. 外设电流消耗

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB1	Bus matrix(1)	2.40	2.00	1.80	μA/MHz
	TSC	1.25	1.05	1.05	
	CRC	0.465	0.375	0.380	
	DMA1	1.90	1.55	1.80	
	DMA2	2.00	1.65	1.80	
	DMAMUX	4.15	3.40	4.45	
	All AHB1 peripherals	12.0	10.0	11.5	
AHB2(2)	AES1	4.00	3.30	3.90	
	ADC1 independent clock domain	2.55	2.10	2.10	
	ADC1 clock domain	2.25	1.90	1.90	
	All AHB2 peripherals	7.45	6.20	6.60	
AHB3	QSPI	7.60	6.25	7.10	
AHB Shared	TRNG independent clock domain	3.80	N/A	N/A	
	TRNG clock domain	2.00	N/A	N/A	
	SRAM2	1.70	1.35	1.35	
	FLASH	8.35	6.90	8.45	
	AES2	6.95	5.75	7.00	
	PKA	4.40	3.65	4.25	
	All AHB shared peripherals	17.5	14.5	16.0	

表50. 外设电流消耗 (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB1	RTCA	1.10	0.88	1.25	μA/MHz
	CRS	0.24	0.20	0.20	
	USB FS independent clock domain	3.20	N/A	N/A	
	USB FS clock domain	2.05	N/A	N/A	
	I2C1 independent clock domain	2.50	4.40	4.40	
	I2C1 clock domain	4.80	4.00	5.50	
	I2C3 independent clock domain	2.10	3.50	3.55	
	I2C3 clock domain	3.70	3.10	3.55	
	LCD	1.35	1.10	2.10	
	SPI2	1.65	1.40	2.25	
	LPTIM1 independent clock domain	2.10	3.40	3.00	
	LPTIM1 clock domain	3.60	3.00	3.80	
	TIM2	5.65	4.70	4.90	
	LPUART1 independent clock domain	2.70	4.15	3.85	
	LPUART1 clock domain	4.45	3.70	5.25	
	LPTIM2 clock domain	3.95	3.25	4.50	
	LPTIM2 independent clock domain	2.20	3.70	3.80	
	WWDG	0.335	0.285	0.965	
	All APB1 peripherals	27.0	22.5	25.5	
APB2	AHB to APB2(3)	1.10	0.885	1.35	
	TIM1	8.20	6.80	7.25	
	TIM17	2.85	2.40	2.40	
	TIM16	2.75	2.30	2.55	
	USART1 independent clock domain	4.40	7.80	7.00	
	USART1 clock domain	8.80	7.30	7.75	
	SPI1	1.75	1.45	1.45	
	SAI1 independent clock domain	2.50	1.50	3.50	
	SAI1 clock domain	2.40	N/A	N/A	
	All APB2 on	28.0	23.0	25.5	
ALL		97.5	80.5	90.0	

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. GPIOs consumption during read and write accesses.
3. The AHB to APB2 bridge is automatically active when at least one peripheral is ON on the APB2.

6.3.9 唤醒时间从低功耗模式和电压缩放 过渡时间

给出的唤醒时间在表*51*是事件和第一个用户指令执行之间的延迟。

设备在 WFE (Wait For Event) 指令后进入低功模式。

Table 51. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		9	10	No. of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with memory in power-down during low-power sleep mode (FPDS = 1 in PWR_CR1) and with clock MSI = 2 MHz		9	10	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash memory	Range 1	Wakeup clock MSI = 32 MHz	2.38	2.96	µs
			Wakeup clock HSI16 = 16 MHz	1.69	2.00	
		Range 2	Wakeup clock HSI16 = 16 MHz	1.70	2.01	
			Wakeup clock MSI = 4 MHz	7.43	8.59	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 32 MHz	2.63	3.00	
			Wakeup clock HSI16 = 16 MHz	1.80	2.00	
		Range 2	Wakeup clock HSI16 = 16 MHz	1.82	2.02	
			Wakeup clock MSI = 4 MHz	7.58	8.70	
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in Flash memory SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	4.67	5.56	
			Wakeup clock HSI16 = 16 MHz	5.09	6.03	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.08	6.00	
			Wakeup clock MSI = 4 MHz	8.36	9.28	
	Wake up time from Stop 1 mode to Run in SRAM1 SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	4.88	5.55	
			Wakeup clock HSI16 = 16 MHz	5.29	5.95	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.28	5.96	
			Wakeup clock MSI = 4 MHz	8.49	9.30	
	Wake up time from Stop 1 mode to Low-power run mode in Flash memory	Regulator in Low-power mode (LPR = 1 in PWR_CR1)	Wakeup clock MSI = 4 MHz	7.96	9.59	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			8.00	9.47	

表51. 低功率模式唤醒时序(1) (继续)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash memory SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	5.27	6.07	µs
			Wakeup clock HSI16 = 16 MHz	5.71	6.52	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.72	6.52	
			Wakeup clock MSI = 4 MHz	9.10	9.93	
	Wake up time from Stop 2 mode to Run mode in SRAM1 SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	5.20	5.94	
			Wakeup clock HSI16 = 16 MHz	5.64	6.42	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.64	6.43	
			Wakeup clock MSI = 4 MHz	9.05	9.85	
t_{WUSTBY}	Wakeup time from Standby mode to Run mode SMPS Bypassed	Range 1	Wakeup clock HSI16 = 16 MHz	51.0	58.1	µs

1. Guaranteed by characterization results (V_{DD} = 3 V, .T = 25 °C).

表52. 调节器模式过渡时间(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low-power run mode to Run mode(2)	Code run with MSI 2 MHz	15.33	16.30	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3)	Code run with HSI16	21.4	28.9	

1. Guaranteed by characterization results (V_{DD} = 3 V, T = 25 °C).
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

表53. 使用 USART/LPUART(1) 唤醒时间

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wakeup time needed to calculate the maximum USART/LPUART baud rate allowing to wakeup from Stop modes when USART/LPUART clock source is HSI16	Stop mode 0	-	1.7	µs
		Stop mode 1/2	-	8.5	

1. Guaranteed by design.

6.3.10 外部时钟源特性

高速外部用户时钟从外部来源生成

高速外部(HSE) 时钟通过一个32 MHz晶体振荡器、正弦波或方波供电。

设备包含内部可编程电容，可以用来调节晶体频率，以补偿PCB 寄生值。

特性在 *表54* 和 *表55* 是在推荐的工作条件下测量的，除非另有说明。典型值参考 TA = 25 °C 和 VDD = 3.0 V。

表54. HSE 晶体要求(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{NOM}	Oscillator frequency	-	-	32	-	MHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance.	-	-	(2)	ppm
C_L	Load capacitance	-	6	-	8	pF
ESR	Equivalent series resistance	-	-	-	100	Ω

1. 32 MHz XTAL is specified for two specific references: NX2016SA and NX1612SA.
2. Refer to the standard specification: 50 ppm for BLE, 40 ppm for 802.15.4 and when both BLE and 802.15.4 are used.

表55. HSE 时钟源要求(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	-	32	-	MHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature and aging.	-	-	(2)	ppm
V_{HSE}	Clock input voltage limits	Sine or square wave, AC-coupled(3)	0.4	-	1.6	V_{PP}
DuCy(HSE)	Duty cycle	-	45	50	55	%
t_r, t_f	Rise and fall times	10% - 90% square wave	-	-	15 * V_{PP}	ns
$\varphi_{n(HSE)}$	Phase noise for 32 MHz	Offset = 10 kHz	-	-	-127	dBc/Hz
		Offset = 100 kHz	-	-	-135	
		Offset = 1 MHz	-	-	-138	

1. Guaranteed by design.
2. Refer to the standard specification: 50 ppm for BLE, 40 ppm for 802.15.4 and when both BLE and 802.15.4 are used.
3. Only AC coupled is supported (capacitor 470 pF to 100 nF).

表 56. HSE 振荡器特性

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SUA(HSE)}$	Startup time for 80% amplitude stabilization	V_{DDRF} stabilized, XOTUNE=000000, -40 to +125 °C range	-	1000	-	µs
$t_{SUR(HSE)}$	Startup time for XOREADY signal		-	250	-	
$I_{DDRF(HSE)}$	HSE current consumption	HSEGMC=000, XOTUNE=000000	-	50	-	µA
$XOT_{g(HSE)}$	XOTUNE granularity	Capacitor bank	-	1	5	ppm
$XOT_{fp(HSE)}$	XOTUNE frequency pulling		±20	±40	-	
$XOT_{nb(HSE)}$	XOTUNE number of tuning bits		-	6	-	bit
$XOT_{st(HSE)}$	XOTUNE setting time		-	-	0.1	ms

Note: For information about oscillator trimming refer to AN5165 "使用 STM32WB 微控制器开发无线电硬件", available from www.st.com.

低速外部用户时钟从外部来源生成

低速外部(LSE) 时钟可以使用 32.768 kHz 晶体共振振荡器供电。本节中提供的信息基于在 <style>表 57 中指定的典型外部组件上进行的设计模拟结果。在应用中，共振器和负载电容必须尽可能靠近振荡器引脚放置，以最小化输出失真和启动稳定时间。

请参考晶体共振器制造商了解更多关于共振器特性(频率、封装、精度).

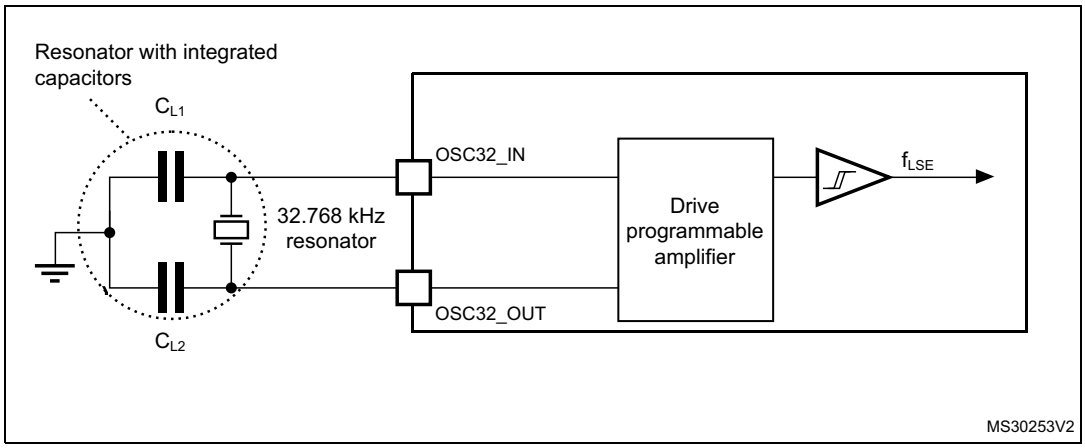
表 57. 低速外部用户时钟特性(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$G_{mcritmax}$	Maximum critical crystal g_m	LSEDRV[1:0] = 00 Low drive capability	-	-	0.50	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.70	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.70	
$t_{SU(LSE)}$(2)	Startup time	V_{DD} stabilized	-	2	-	s

1. 设计保证. 2. tSU(LSE) 是从启用时刻(由软件) 测量到稳定的32 kHz振荡所需的启动时间。此值是为标准晶体测量的，它会根据晶体制造商而显著变化。

Note: *For information on selecting the crystal refer to application note AN2867 “STM8S, STM8A和STM32微控制器的振荡器设计指南” available from www.st.com.*

图22. 使用 32.768 kHz 晶体振荡器的典型应用



Note: 在 *OSC32_IN* 和 *OSC32_OUT* 之间不需要外部阻容器，并是禁止添加。

在绕过模式下，LSE 振荡器会被关闭，输入引脚变为标准的 GPIO。

The external clock signal has to respect the I/O characteristics detailed in 第*6.3.17*节.The recommend clock input waveform is shown in 图*23*.

图23. 低速外部时钟源交流时序图

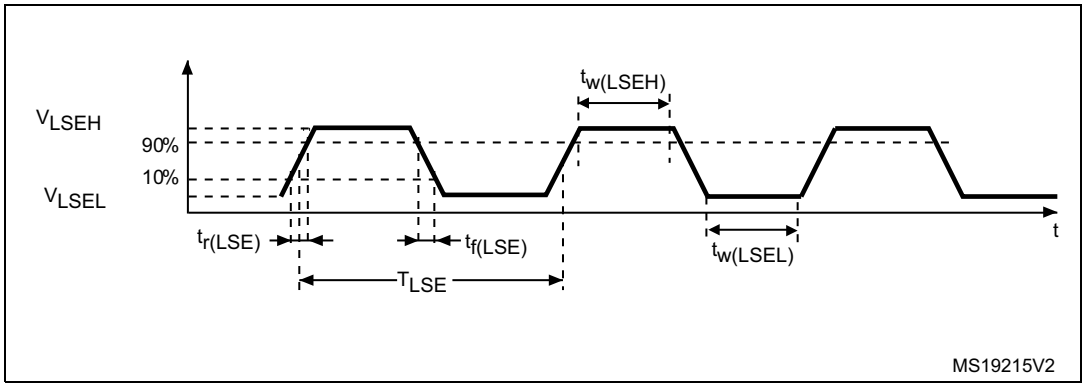


表 58. 低速外部用户时钟特性(1) – 绕过模式

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	21.2	32.768	44.4	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDx}	-	V_{DDx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns
f_{tolLSE}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling	-500	-	+500	ppm

1. Guaranteed by design.

6.3.11 内部时钟源特性

给定的参数在表 *59*中，是在环境温度和供电电压条件下进行测试得出的，这些条件总结在表 *24*：通用运行条件。提供的曲线是特征化结果，而非在生产中进行的测试。

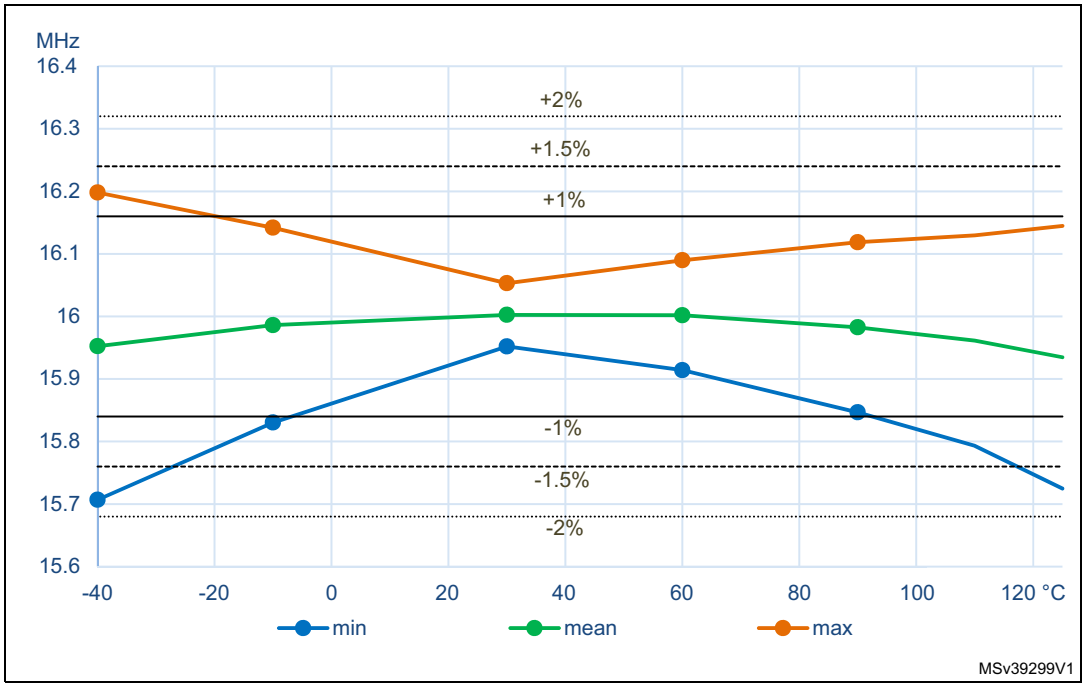
高速内部 (HSI16) RC 振荡器

表 59. HSI16 振荡器特性(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16)(2)	Duty Cycle	-	45	-	55	
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	
		T_A= -40 to 125 °C	-2	-	1.5	
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	
t_{su}(HSI16)(2)	HSI16 oscillator start-up time	-	-	0.8	1.2	µs
t_{stab}(HSI16)(2)	HSI16 oscillator stabilization time	-	-	3	5	
I_{DD}(HSI16)(2)	HSI16 oscillator power consumption	-	-	155	190	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

图24. HSI16 频率与温度比较



内部多速度RC振荡器

Table 60. MSI 振荡器特性(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD}=3 V and T_A=30 °C	MSI mode	Range 0	98.7	100	101.3	kHz
			Range 1	197.4	200	202.6	
			Range 2	394.8	400	405.2	
			Range 3	789.6	800	810.4	
			Range 4	0.987	1	1.013	MHz
			Range 5	1.974	2	2.026	
			Range 6	3.948	4	4.052	
			Range 7	7.896	8	8.104	
			Range 8	15.79	16	16.21	
			Range 9	23.69	24	24.31	
			Range 10	31.58	32	32.42	
			Range 11	47.38	48	48.62	
		PLL mode XTAL= 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	MHz
			Range 5	-	1.999	-	
			Range 6	-	3.998	-	
			Range 7	-	7.995	-	
			Range 8	-	15.991	-	
			Range 9	-	23.986	-	
			Range 10	-	32.014	-	
			Range 11	-	48.005	-	
Δ_{TEMP}(MSI)(2)	MSI oscillator frequency drift over temperature	MSI mode	T_A= -0 to 85 °C	-3.5	-	3	%
			T_A= -40 to 125 °C	-8	-	6	

表 60. MSI 振荡器特性(1) (继续)

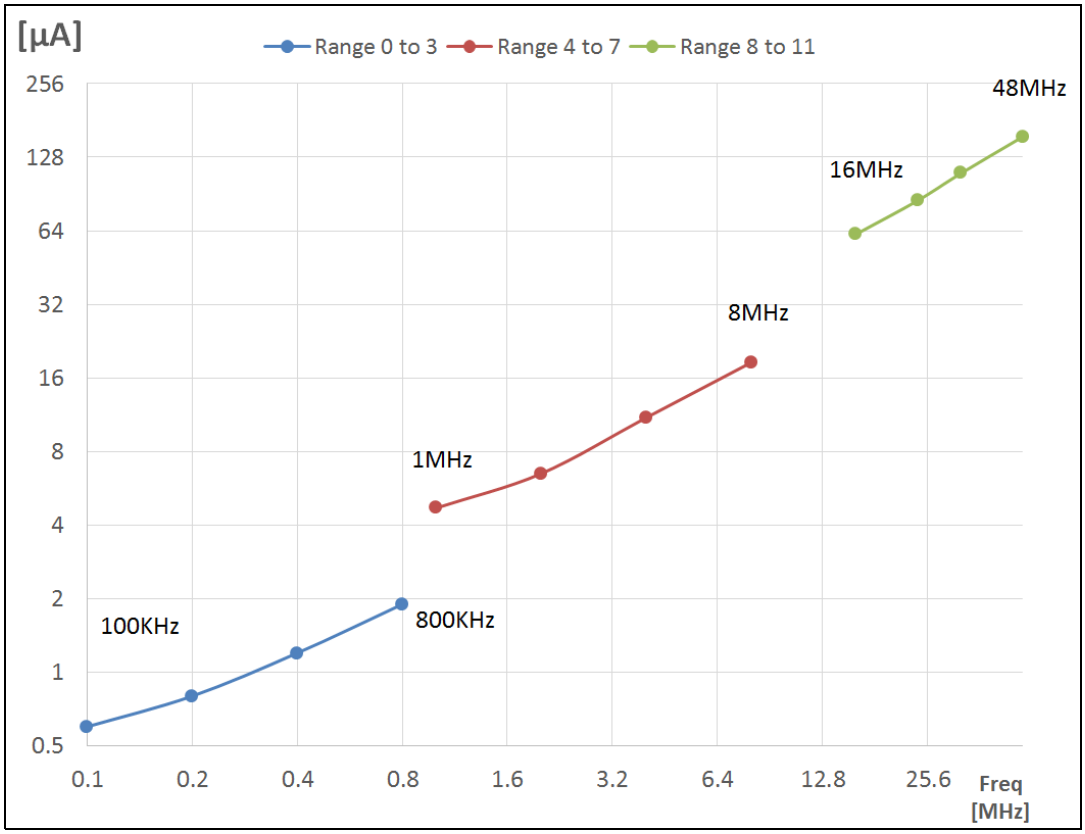
Symbol	Parameter	Conditions			Min	Typ	Max	Unit
Δ_{VDD}(MSI)(2)	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	V_{DD} = 1.62 to 3.6 V	-1.2	-	0.5	%
				V_{DD} = 2.4 to 3.6 V	-0.5	-		
			Range 4 to 7	V_{DD} = 1.62 to 3.6 V	-2.5	-	0.7	
				V_{DD} = 2.4 to 3.6 V	-0.8	-		
			Range 8 to 11	V_{DD} = 1.62 to 3.6 V	-5	-	1	
				V_{DD} = 2.4 to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}$ (MSI)(2)(6)	Frequency variation in sampling mode(3)	MSI mode	T_A= -40 to 85 °C		-	1	2	
			T_A= -40 to 125 °C		-	2	4	
P_USB Jitter(MSI)(6)	Period jitter for USB clock(4)	PLL mode Range 11	For next transition	-	-	-	3.458	ns
			For paired transition	-	-	-	3.916	
MT_USB Jitter(MSI)(6)	Medium term jitter for USB clock(5)	PLL mode Range 11	For next transition	-	-	-	2	
			For paired transition	-	-	-	1	
CC jitter(MSI)(6)	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI)(6)	RMS period jitter	PLL mode Range 11		-	-	50	-	
t_{SU}(MSI)(6)	MSI oscillator start-up time	Range 0		-	-	10	20	µs
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
t_{STAB}(MSI)(6)	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	

表 60. MSI 振荡器特性(1) (继续)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$I_{DD}(MSI)^{(6)}$	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1	µA
			Range 1	-	-	0.8	1.2	
			Range 2	-	-	1.2	1.7	
			Range 3	-	-	1.9	2.5	
			Range 4	-	-	4.7	6	
			Range 5	-	-	6.5	9	
			Range 6	-	-	11	15	
			Range 7	-	-	18.5	25	
			Range 8	-	-	62	80	
			Range 9	-	-	85	110	
			Range 10	-	-	110	130	
			Range 11	-	-	155	190	

1. 设计保证。2. 这是一个个体部件在初始频率被测量后的偏差。3. 采样模式意味着温度传感器关闭的低功耗运行/低功耗休眠模式。4. 48 MHz 的 MSI 的平均周期与 28 转数内的真实 48 MHz 时钟进行比较。它包括频率容忍度 + 4848 MHz 上的 MSI 累积抖动。5. 只有 28 转数内的 48 MHz 上的 MSI 累积抖动被提取。 为下一个过渡：MSI 在兆赫上的 2 28 48 1000 连续 28 帧的最小和最大抖动，用于超过转数的捕获。为配对过渡：MSI 在 48 MHz 上的 56 转数内的 2 个连续帧的最小和最大抖动，用于 1000 次捕获超过 56 转数。6. 设计保证。

图25. 典型电流消耗与 MSI 频率比较



高速内部 48 兆赫 HSI48 RC 振荡器

表61. HSI48 振荡器特性(1)

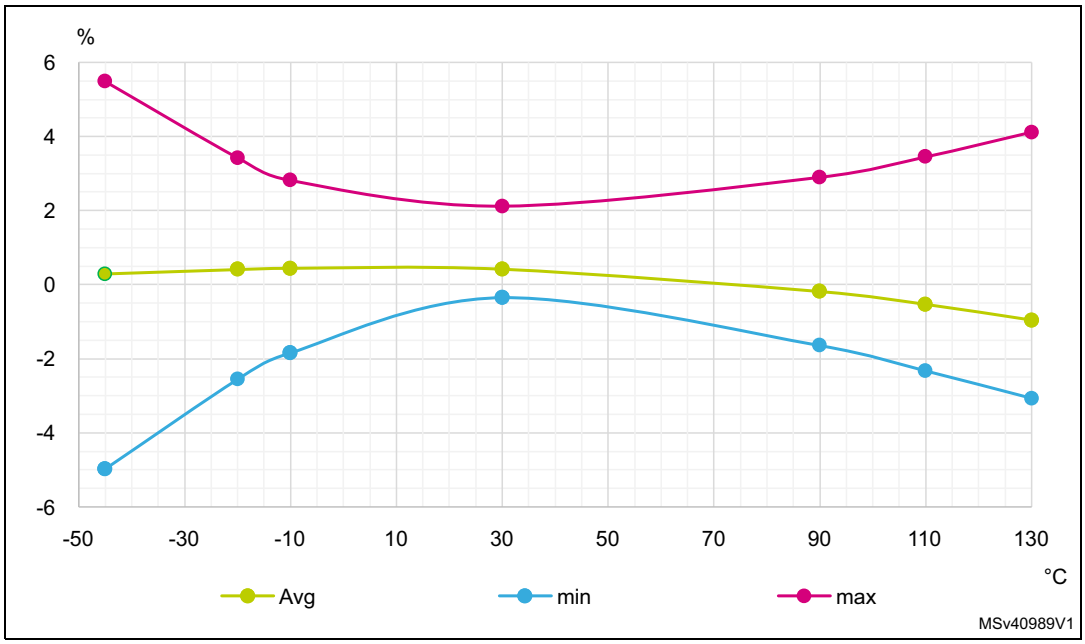
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 frequency	V_{DD} = 3.0 V, T_A = 30 °C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11(2)	0.18(2)	%
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3(3)	±3.5(3)	-	
DuCy(HSI48)	Duty cycle	-	45(2)	-	55(2)	
ACC_{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V, T_A = –15 to 85 °C	-	-	±3(3)	
		V_{DD} = 1.65 V to 3.6 V, T_A = –40 to 125 °C	-	-	±4.5(3)	
D_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(3)	0.05(3)	
		V_{DD} = 1.65 V to 3.6 V	-	0.05(3)	0.1(3)	
t_{su}(HSI48)	HSI48 oscillator start-up time	-	-	2.5(2)	6(2)	µs
I_{DD}(HSI48)	HSI48 oscillator power consumption	-	-	340(2)	380(2)	µA

表61. HSI48 振荡器特性(1) (继续)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(4)	-	-	±0.15(2)	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(4)	-	-	±0.25(2)	-	

1. V_{DD} = 3 V, T_A = –40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

图 26. HSI48 频率与温度比较



低速内部 (LSI) RC 振荡器

表62. LSI1 振荡器特性(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI1 frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.62 to 3.6 V, T_A = -40 to 125 °C	29.5	-	34	
$t_{SU}(LSI1)$(2)	LSI1 oscillator start-up time	-	-	80	130	µs
$t_{STAB}(LSI1)$(2)	LSI1 oscillator stabilization time	5% of final frequency	-	125	180	
$I_{DD}(LSI1)$(2)	LSI1 oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

表63. LSI2 振荡器特性(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI2}	LSI2 frequency	V_{DD} = 3.0 V, T_A = 30 °C	21.6	-	44.2	kHz
		V_{DD} = 1.62 to 3.6 V, T_A = -40 to 125 °C	21.2	-	44.4	
$t_{SU}(LSI2)^{(2)}$	LSI2 oscillator start-up time	-	0.7	-	3.5	ms
$I_{DD}(LSI2)^{(2)}$	LSI2 oscillator power consumption	-	-	500	1180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

6.3.12 PLL 特性

The parameters given in 表64 are derived from tests performed under temperature andVDD supply voltage conditions summarized in 表24：通用运行条件.

表64. PLL, PLLSAI1 特性(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	2.66	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	2	-	64	MHz
		Voltage scaling Range 2	2	-	16	
$f_{PLL\_Q\_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	8	-	64	
		Voltage scaling Range 2	8	-	16	
$f_{PLL\_R\_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	8	-	64	
		Voltage scaling Range 2	8	-	16	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	96	-	344	
		Voltage scaling Range 2	64	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 64 MHz	-	40	-	ps
	RMS period jitter		-	30	-	
$I_{DD}(PLL)$	PLL power consumption on V_{DD}(1)	VCO freq = 96 MHz	-	200	260	µA
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the two PLLs.

6.3.13 Flash memory characteristics

表65. 闪存存储特性(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.7	90.8	µs
t_{prog_row}	One row (64 double word) programming time	Normal programming	5.2	5.5	ms
		Fast programming	3.8	4.0	
t_{prog_page}	One page (4 Kbytes) programming time	Normal programming	41.8	43.0	
		Fast programming	30.4	31.0	
t_{ERASE}	Page (4 Kbytes) erase time	-	22.0	24.5	
t_{ME}	Mass erase time	-	22.1	25.0	
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	

1. Guaranteed by design.

表66. 闪存耐用性和数据保留

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		1 kcycle(2) at T_A = 125 °C	7	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

6.3.14 EMC 特性

感应性测试在设备特征化过程中以样本为基础进行。

功能性 EMS (电磁感应性)

在设备上执行一个简单的应用 (通过 I/O 端口控制 2 个 LED). 设备受到两种电磁事件的压力，直到发生故障。 故障通过以下 LED 表示：

- **静电放电(ESD)** (正负) 被应用于所有设备引脚，直到发生功能干扰。此测试符合IEC 61000-4-2标准。• **FTB**: 快速暂态电压冲击(正负) 通过100 pF 电容应用于VDD和VSS，直到发生功能干扰。此测试符合IEC 61000-4-4标准。

设备重置允许恢复正常运行。

测试结果显示在 *表67*. 它们基于 AN{style}STM8, STM32 和 遗留 MCUs 的 EMC 设计指南”, 可以在 *www.st.com*.

表67. EMS 特性

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 64 MHz, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 64 MHz, conforming to IEC 61000-4-4	5A

设计强壮的软件以避免噪声问题

EMC 特征化和优化在典型应用环境和简化的 MCU 软件下进行组件级执行。

良好的 EMC 性能高度依赖于用户应用程序和软件。因此，建议用户根据应用程序所需的 EMC 级别应 EMC 软件优化和预先合格测试。

软件建议

软件流程必须包括以下失控状态的管理：

- 损坏的计数器• 意外复位• 关键数据损坏 (例如. 控制寄存器)

预先资质试验

大多数常见的故障，例如意外复位和程序计数器损坏，可以通过手动将 NRST 引脚或振荡器引脚保持在低状态 1 秒来重现。

为了完成这些试验，ESD应力可以直接应用于设备，覆盖规格值的范围。当检测到意外行为时，软件可以加固以防止发生无法恢复的错误 (见应用说明 AN1015).

电磁干扰 (EMI)

在执行简单应用程序时，监控设备发射的电磁场 (通过 I/O 端口切换两个 LED). 这种发射测试符合 IEC 61967-2 标准，该标准指定了测试板和引脚负载。

表 68. EMI 特性

Symbol	Parameter	Conditions	Monitored frequency band	Peripheral ON SMPS OFF or ON [f_{HSE} / f_{CPUM4}, f_{CPUM0}]	Unit
				32 MHz / 64 MHz, 32 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, WLCSP100 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	1	dBµV
			30 MHz to 130 MHz	4	
			130 MHz to 1 GHz	-1	
			1 GHz to 2 GHz	7	
			EMI level	1.5	-

6.3.15 电气敏感性特性

基于三种不同的测试 (ESD, LU) 使用特定的测量方法，对设备进行应力以确定其在电气敏感性方面的性能。

静电放电 (ESD)

静电放电 (a正后跟随一个负脉冲) 分别在每个样本的引脚上应用，按照每个引脚组合进行。样本大小取决于设备中供电引脚的数量 (3 零件 × (n+1) 供电引脚)。此测试符合 ANSI/JEDEC 标准。

表 69. ESD 绝对最大额定值

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1 JS-002	C2a(2)	500(2)	
			C1(3)	250(3)	

1. Guaranteed by characterization results.
2. UFQFPN48, VFQPN68 and WLCSP100 packages.
3. UFBGA129 package.

静态锁存

需要在六个零件上进行两个互补的静态测试来评估锁存性能：

- a供过压被应用于每个电源引脚• a电流注入被应用于每个输入、输出和可配置的I/O引脚。

这些测试符合EIA/JESD 78A集成电路上锁标准。

表 70. 电气敏感性

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II

6.3.16 I/O 电流注入特性

作为一般规则，由于外部电压低于VSS或高于VDD (对于标准的3.3伏兼容的I/O引脚) 应该避免在正常产品运行中发生电流注入。然而，为了给出微控制器在异常注入意外发生时的韧性指示，感应性测试在设备特征化过程中以样本方式进行。

对I/O电流注入的功能敏感性

在设备上执行简单应用程序时，通过向编程为浮动输入模式的I/O引脚注入电流来 stressing力设备。在将电流注入到I/O引脚时，一个一个地进行，设备会被检查是否存在功能故障。

故障由超出范围的参数表示：ADC错误高于某个限制 (高于 5 LSB TUE)，或者超出相邻引脚诱导漏电流的常规限制 (超出{-v4}A / 0 µA 范围) ，或者其他功能故障 (例如复位发生或振荡器频率偏差).

特性化结果在 *表 71*.

负向诱导漏电流是由负向注入引起的，正向诱导漏电流是由正向注入引起的。

表 71. I/O 电流注入易受性(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins except PB0, PB1	-5	N/A(2)	mA
	Injected current on PB0, PB1 pins	-5	0	

1. Guaranteed by characterization results.
2. Injection not possible.

6.3.17 I/O 端口特性

通用输入输出特性

除非另有说明，参数如 表 72所示，是在 表 24：通用运行条件总结的条件下进行测试得到的。所有输入/输出都设计为兼容 CMOS 和 TTL。

表 72. I/O 静态特性

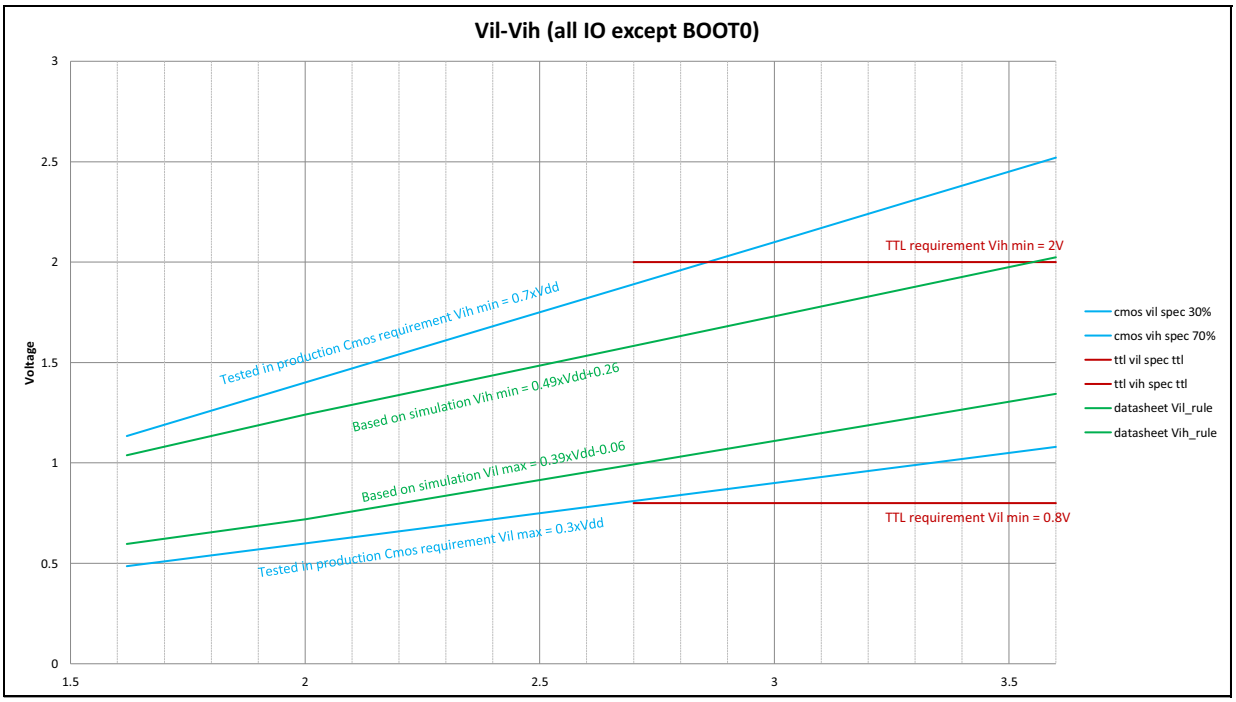
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage(1)	1.62 V < V_{DD} < 3.6 V	-	-	0.3 x V_{DD}	V
	I/O input low level voltage(2)				0.39 x V_{DD} - 0.06	
V_{IH}	I/O input high level voltage(1)		0.7 x V_{DD}	-	-	
	I/O input high level voltage(2)		0.49 x V_{DD} + 0.26	-	-	
V_{hys}	TT_xx, FT_xxx and NRST I/O input hysteresis		-	200	-	mV
I_{lkg}	FT_xx input leakage current	0 ≤ V_{IN} ≤ Max(V_{DDXXX})(3)	-	-	±100	nA
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX}) +1 V(2)(3)(4)	-	-	650	
		Max(V_{DDXXX}) +1 V < V_{IN} ≤ 5.5 V(2)(3)(4)(5)(6)	-	-	200(7)	
	FT_lu, FT_u and PC3 IO input leakage current	0 ≤ V_{IN} ≤ Max(V_{DDXXX})(3)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX}) +1 V(2)(3)	-	-	2500	
		Max(V_{DDXXX}) +1 V < V_{IN} ≤ 5.5 V(1)(3)(4)(8)	-	-	250	
	TT_xx input leakage current	V_{IN} ≤ Max(V_{DDXXX})(3)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} < 3.6 V(3)	-	-	2000	
R_{PU}	Weak pull-up equivalent resistor(1)	V_{IN} = V_{SS}	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(1)	V_{IN} = V_{DD}	25	40	55	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Tested in production.
2. Guaranteed by design, not tested in production.
3. Represents the pad leakage of the I/O itself. The total product pad leakage is given by $I_{Total\_Ileak\_max}$ = 10 µA + number of I/Os where V_{IN} is applied on the pad x $I_{lkg(Max)}$.
4. Max(V_{DDXXX}) is the maximum value among all the I/O supplies.
5. V_{IN} must be lower than [Max(V_{DDXXX}) + 3.6 V].
6. Refer to *Figure 27: I/O input characteristics*.

7. 为了维持高于 Min(VDD, VDDA, VDDUSB, VLCD) + 0.3 V 的电压，内部上拉下拉电阻必须被禁用。所有 FT_xx IO 除了 t FT_lu, FT_u 和 PC3。8. 上拉下拉电阻是与一个可切换的 PMOS/NMOS 并联设计的，其对串联电阻的贡献最小 (~10%)。

All I/Os are CMOS- and TTL-compliant (no software configuration required). Theircharacteristics cover more than the strict CMOS-technology or TTL parameters, as shownin 图*27* .

图27. I/O 输入特性



输出驱动电流

GPIOs (通用输入/输出) 可以吸收或提供高达 ±8 mA 的电流，并且在放松的 VOL / VOH) 下，可以吸收或提供高达 ± 20 mA 的电流。

在用户应用程序中，能够驱动电流的 I/O 引脚数量必须受到 <style><style='3'>第6.2节. 中指定的绝对最大值的限制。

- 所有 I/O 引脚在 VDD 上提供的电流之和，加上 MCU 在 VDD, 上提供的最大消耗，不能超过绝对最大值 ΣIVDD (参见 表 *20:* 电压特性).• 所有 I/O 引脚在 VSS 上吸收的电流之和，加上 MCU 在 VSS 上吸收的最大消耗，不能超过绝对最大值 ΣIVSS (参见 表 *20:* 电压特性).

输出电压级别

除非另有说明，下面表格中给出的参数是在 <style><style='3'>表 24: 通用运行条件. 中总结的环境温度和供电电压条件下进行的测试中得出的。所有 I/O 引脚都兼容 CMOS 和 TTL (FT 或 TT 除非另有说明).

表 73. 输出电压特性(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage for an I/O pin	CMOS port(3) $\|I_{IO}\|$ = 8 mA $V_{DD} \geq 2.7$ V	-	0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DD} - 0.4	-	
V_{OL}(2)	Output low level voltage for an I/O pin	TTL port(3) $\|I_{IO}\|$ = 8 mA $V_{DD} \geq 2.7$ V	-	0.4	
V_{OH}(2)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(2)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DD} \geq 2.7$ V	-	1.3	
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DD} - 1.3	-	
V_{OL}(2)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA $V_{DD} \geq 1.62$ V	-	0.4	
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DD} - 0.45	-	
V_{OLFM+}(2)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with “f” option)	$\|I_{IO}\|$ = 20 mA $V_{DD} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\|$ = 10 mA $V_{DD} \geq 1.62$ V	-	0.4	
		$\|I_{IO}\|$ = 2 mA 1.62 V ≥ V_{DD} ≥ 1.08 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 20: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings Σ I_{IO}.
2. Guaranteed by design.
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

输入/输出交流特性

The definition and values of input/output AC characteristics are given in 表 *74*.

除非另有说明，否则给定的参数是在环境温度和供电电压条件下进行测试得出的，这些条件总结在 表 *24*：通用运行条件.

表 74. I/O 交流特性(1)(2)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5	MHz
			C=50 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	1	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	10	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	1.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	25	ns
			C=50 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	52	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	17	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ ≤2.7 V	-	37	

表 74. I/O 交流特性(1)(2) (继续)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
01	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	25	MHz
			C=50 pF, 1.62 V ≤ V_{DD} ≤ ≤2.7 V	-	10	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	50	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	15	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	9	ns
			C=50 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	16	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4.5	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	9	
10	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	50	MHz
			C=50 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	25	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	100(3)	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	37.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.8	ns
			C=50 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	11	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.5	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	5	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	120(3)	MHz
			C=30 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	50	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	180(3)	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	75(3)	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.3	ns
			C=30 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	6	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.7	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	3.3	

1. The maximum frequency is defined with (T_r+ T_f) ≤ 2/3 T, and Duty cycle comprised between 45 and 55%.
2. The fall and rise time are defined, respectively, between 90 and 10%, and between 10 and 90% of the output waveform.
3. This value represents the I/O capability but the maximum system frequency is limited to 64 MHz.

6.3.18 NRST 引脚特性

NRST 引脚输入驱动器使用 CMOS 技术。它连接到一个永久的 上拉电阻 RPU。

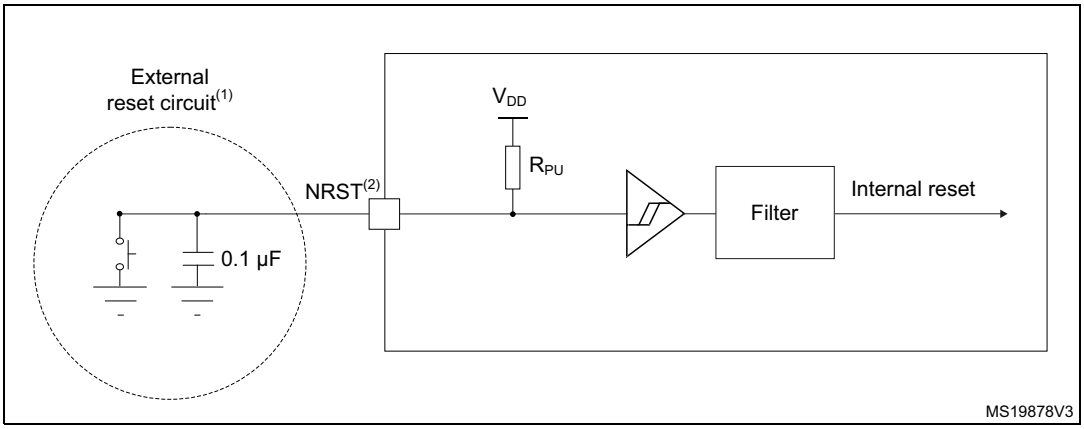
除非另有说明，下面表格中的参数是在环境温度和供电电压条件下进行测试得出的，这些条件总结在表 *24*：通用运行条件.

表75. NRST 引脚特性(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.7 x V_{DD}	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10%).

图28. 推荐的 NRST 引脚保护



1. 复位网络保护设备免受寄生复位的影响。2. 用户必须确保 NRST 引脚上的水平可以低于 $V_{IL(NRST)}$ 最大水平，如 表75所示，否则设备将不会考虑复位。3. 在 NRST 上的外部电容器必须尽可能靠近设备。

6.3.19 模拟开关增强器

表76. 模拟开关增强器特性(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	-	-	250	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

1. Guaranteed by design.

6.3.20 模拟-数字转换器特性

除非另有说明，否则在表 77 中给出的参数是在环境温度、PCLK 频率和 VDDA 供电电压条件下进行的测试中提取的初步值，这些条件总结在表 24：通用运行条件中。

注意：建议在每次上电后进行校准。

表 77. ADC 特性(1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	V_{DDA} ≥ 2 V	2	-	V_{DDA}	V
		V_{DDA} < 2 V	V_{DDA}			V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
f_{ADC}	ADC clock frequency	Range 1	0.14	-	64	MHz
		Range 2	0.14	-	16	
f_s	Sampling rate for FAST channels	Resolution = 12 bits	-	-	4.26	Msps
		Resolution = 10 bits	-	-	4.92	
		Resolution = 8 bits	-	-	5.81	
		Resolution = 6 bits	-	-	7.11	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	3.36	
		Resolution = 10 bits	-	-	4.00	
		Resolution = 8 bits	-	-	4.57	
		Resolution = 6 bits	-	-	7.11	
f_{TRIG}	External trigger frequency	f_{ADC} = 64 MHz Resolution = 12 bits	-	-	4.26	MHz
		Resolution = 12 bits	-	-	15	$1/f_{ADC}$
V_{CMIN}	Input common mode	Differential mode	(V_{REF+}+ V_{REF-}) / 2 - 0.18	(V_{REF+}+ V_{REF-}) / 2	(V_{REF+}+ V_{REF-}) / 2 + 0.18	V
V_{AIN} (4)	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			Conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 64 MHz	1.8125			µs
		-	116			$1 / f_{ADC}$

表 77. ADC 特性(1) (2) (3) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 64 MHz	0.039	-	10.0	µs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 64 MHz Resolution = 12 bits	0.234	-	1.019	µs
		Resolution = 12 bits	t_s + 12.5 cycles for successive approximations = 15 to 653			$1/f_{ADC}$
I_{DDA}(ADC)	ADC consumption from the V_{DDA} supply	fs = 4.26 Msps	-	730	830	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 4.26 Msps	-	130	160	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 4.26 Msps	-	250	310	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. SMPS in bypass mode.
4. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pinouts and pin description* for further details.

表78. ADC 抽样时间(1)(2)

Resolution (bits)	RAIN (kΩ)	Fast channel		Slow channel	
		Minimum sampling time (ns)	Sampling cycles	Minimum sampling time (ns)	Sampling cycles
12	0	33	6.5	57	6.5
	0.05	37	6.5	62	6.5
	0.1	42	6.5	67	6.5
	0.2	51	6.5	76	6.5
	0.5	78	6.5	104	12.5
	1	123	12.5	151	12.5
	5	482	47.5	526	47.5
	10	931	92.5	994	92.5
	20	1830	247.5	1932	247.5
	50	4527	640.5	4744	640.5
	100	9021	640.5	9430	640.5
10	0	27	2.5	47	6.5
	0.05	30	2.5	51	6.5
	0.1	34	6.5	55	6.5
	0.2	41	6.5	62	6.5
	0.5	64	6.5	85	6.5
	1	100	12.5	124	12.5
	5	395	47.5	431	47.5
	10	763	92.5	816	92.5
	20	1500	247.5	1584	247.5
	50	3709	640.5	3891	640.5
	100	7391	640.5	7734	640.5
8	0	21	2.5	37	2.5
	0.05	24	2.5	40	6.5
	0.1	27	2.5	43	6.5
	0.2	32	6.5	49	6.5
	0.5	50	6.5	67	6.5
	1	78	6.5	97	6.5
	5	308	47.5	337	24.5
	10	595	92.5	637	47.5
	20	1169	247.5	1237	92.5
	50	2891	247.5	3037	247.5
	100	5762	640.5	6038	640.5

表78. ADC 抽样时间[1][2] (继续)

Resolution (bits)	RAIN (kΩ)	Fast channel		Slow channel	
		Minimum sampling time (ns)	Sampling cycles	Minimum sampling time (ns)	Sampling cycles
6	0	15	2.5	26	2.5
	0.05	17	2.5	28	2.5
	0.1	19	2.5	31	2.5
	0.2	23	2.5	35	2.5
	0.5	36	6.5	48	6.5
	1	56	6.5	69	6.5
	5	221	24.5	242	24.5
	10	427	47.5	458	47.5
	20	839	92.5	890	92.5
	50	2074	247.5	2184	247.5
	100	4133	640.5	4342	640.5

1. Guaranteed by design.
2. V_{DD} = 1.62 V, C_{pcb} = 4.7 pF, 125 °C, booster enabled.

表79. ADC 精度 - 有限测试条件 1(1)(2)(3)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, $V_{DDA} = V_{REF+} = 3$ V, TA = 25 °C	Single ended	Fast channel (max speed)	-	4	5	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	3.5	4.5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	2.5	
				Slow channel (max speed)	-	1	2.5	
			Differential	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.5	-	bits
				Slow channel (max speed)	10.4	10.5	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65	-	dB
				Slow channel (max speed)	64.4	65	-	
			Differential	Fast channel (max speed)	66.8	67.4	-	
				Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
			Differential	Fast channel (max speed)	67	68	-	
				Slow channel (max speed)	67	68	-	

表79. ADC 精度 - 有限测试条件 1[1][2][3] (继续)

Symbol	Parameter	Conditions[4]			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, $V_{DDA} = V_{REF+} = 3$ V, TA = 25 °C	Single ended	Fast channel (max speed)	-	-74	-73	dB
				Slow channel (max speed)	-	-74	-73	
			Differential	Fast channel (max speed)	-	-79	-76	
				Slow channel (max speed)	-	-79	-76	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

表80. ADC 精度 - 有限测试条件 2(1)(2)(3)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, V_{DDA} ≥ 2 V TA = 25 °C	Single ended	Fast channel (max speed)	-	4	6.5	LSB
				Slow channel (max speed)	-	4	6.5	
			Differential	Fast channel (max speed)	-	3.5	5.5	
				Slow channel (max speed)	-	3.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	4.5	
				Slow channel (max speed)	-	1	5	
			Differential	Fast channel (max speed)	-	1.5	3	
				Slow channel (max speed)	-	1.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	6	
				Slow channel (max speed)	-	2.5	6	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	3.5	
				Slow channel (max speed)	-	1.5	3.5	
			Differential	Fast channel (max speed)	-	1	3	
				Slow channel (max speed)	-	1	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.5	-	bits
				Slow channel (max speed)	10	10.5	-	
			Differential	Fast channel (max speed)	10.7	10.9	-	
				Slow channel (max speed)	10.7	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	65	-	dB
				Slow channel (max speed)	62	65	-	
			Differential	Fast channel (max speed)	66	67.4	-	
				Slow channel (max speed)	66	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	66	-	
				Slow channel (max speed)	64	66	-	
			Differential	Fast channel (max speed)	66.5	68	-	
				Slow channel (max speed)	66.5	68	-	

表80. ADC 精度 - 有限测试条件 2[1][2][3] (继续)

Symbol	Parameter	Conditions[4]			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, V_{DDA} ≥ 2 V TA = 25 °C	Single ended	Fast channel (max speed)	-	-74	-65	dB
				Slow channel (max speed)	-	-74	-67	
			Differential	Fast channel (max speed)	-	-79	-70	
				Slow channel (max speed)	-	-79	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

表 81. ADC 精度 - 有限测试条件 3[1][2][3]

Symbol	Parameter	Conditions[4]			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
				Slow channel (max speed)	-	4.5	6.5	
			Differential	Fast channel (max speed)	-	4.5	7.5	
				Slow channel (max speed)	-	4.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	5	
				Slow channel (max speed)	-	2.5	5	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.5	7	
				Slow channel (max speed)	-	3.5	6	
			Differential	Fast channel (max speed)	-	3.5	4	
				Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.2	1.5	
				Slow channel (max speed)	-	1.2	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	3	3.5	
				Slow channel (max speed)	-	2.5	3.5	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.4	-	bits
				Slow channel (max speed)	10	10.4	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	64	-	dB
				Slow channel (max speed)	62	64	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	65	-	
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

表 81. ADC 精度 - 有限测试条件 3[(1)(2)(3)] (继续)

Symbol	Parameter	Conditions[(4)]			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
			Differential	Fast channel (max speed)	-	-72	-71	
				Slow channel (max speed)	-	-72	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

表82. ADC 精度 - 有限测试条件 4(1)(2)(3)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 16 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	5	5.4	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	4	5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	4	
				Slow channel (max speed)	-	2	4	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2	3.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	4	4.5	
				Slow channel (max speed)	-	4	4.5	
			Differential	Fast channel (max speed)	-	3	4	
				Slow channel (max speed)	-	3	4	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	2.5	3	
				Slow channel (max speed)	-	2.5	3	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.2	10.5	-	bits
				Slow channel (max speed)	10.2	10.5	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	63	65	-	dB
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	65	-	
				Slow channel (max speed)	64	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

表82. ADC 精度 - 有限测试条件 4(1)(2)(3) (继续)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 16 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	-71	-69	dB
				Slow channel (max speed)	-	-71	-69	
			Differential	Fast channel (max speed)	-	-73	-72	
				Slow channel (max speed)	-	-73	-72	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins that may potentially inject negative current.
4. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disabled when V_{DDA} ≥ 2.4 V. No oversampling.

Figure 29. ADC accuracy characteristics

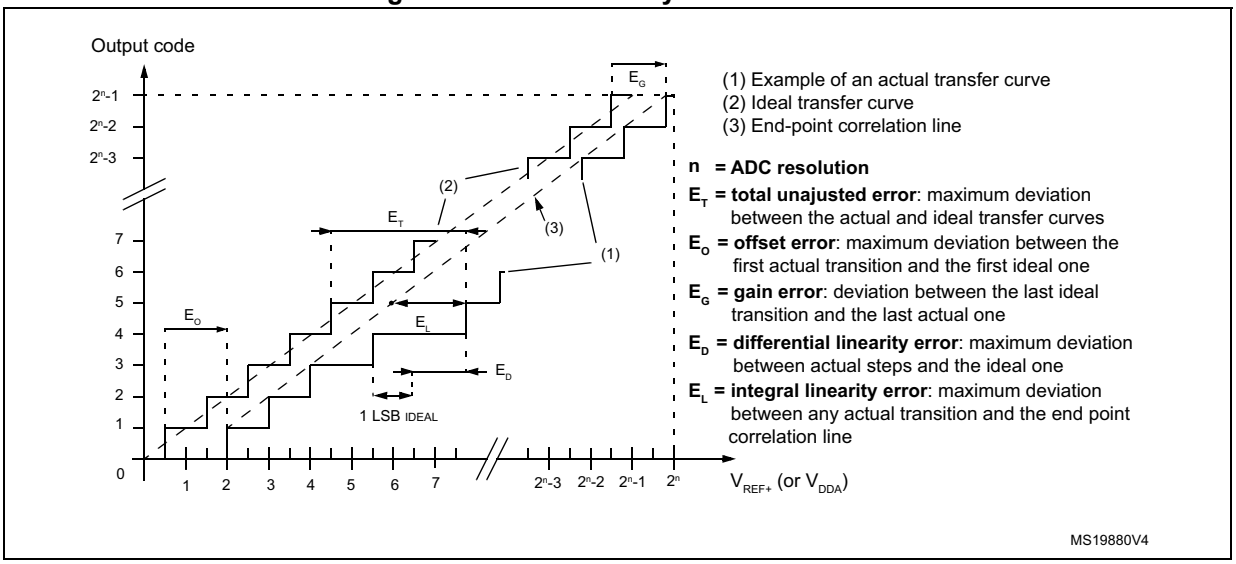
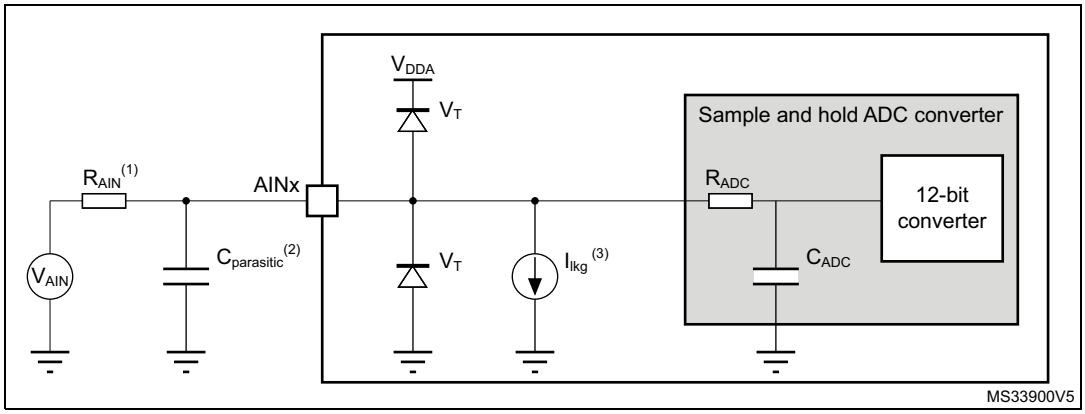


图30. 使用 ADC 的典型连接图



1. Refer to 表77：*ADC* 特性 for the values of RAIN, RADC and CADC.2. Cparasitic represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to 表72：*I/O*静态特性 for the value of the pad capacitance). A high Cparasitic value will downgrade conversion accuracy. To remedy this, fADC should be reduced.3. Refer to 表72：*I/O*静态特性 for the values of Ilkg.

通用 PCB 设计指南

电源隔离需要按照所示进行图*16: 电源方案(所有封装除外 UFBGA129 和 WLCSP100)*. 10 nF 电容需要是陶瓷的 (高质量), 尽可能靠近芯片.

6.3.21 电压参考缓冲器特性

表 83. VREFBUF 特性(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	V_{RS} = 0	2.4	-	3.6	V
			V_{RS} = 1	2.8	-	3.6	
		Degraded mode(2)	V_{RS} = 0	1.65	-	2.4	
			V_{RS} = 1	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode	V_{RS} = 0	2.046	2.048	2.049	
			V_{RS} = 1	2.498	2.5	2.502	
		Degraded mode(2)	V_{RS} = 0	V_{DDA}-150 mV	-	V_{DDA}	
			V_{RS} = 1	V_{DDA}-150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	µF
esr	Equivalent series resistor of C_{load}	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA

表 83. VREFBUF 特性(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	1000	ppm/V
			I_{load} = 4 mA	-	100	500	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	-	50	500	ppm/mA
T_{Coeff}	Temperature coefficient	-40 °C < T_J < +125 °C		-	-	$T_{coeff\_vrefint}$ + 50	ppm/ °C
		0 °C < T_J < +50 °C		-	-	$T_{coeff\_vrefint}$ + 50	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	CL = 0.5 µF(3)		-	300	350	µs
		CL = 1.1 µF(3)		-	500	650	
		CL = 1.5 µF(3)		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase (4)	-	-	-	8	-	mA
I_{DDA} (VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA		-	16	25	µA
		I_{load} = 500 µA		-	18	30	
		I_{load} = 4 mA		-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode the voltage reference buffer cannot maintain accurately the output voltage that will follow (V_{DDA} - drop voltage).
3. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
4. To correctly control the VREFBUF in-rush current during start-up phase and scaling change, the V_{DDA} voltage must be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

6.3.22 比较器特性

表 84. COMP 特性(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	V
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			V
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	40	
t_D(3)	Propagation delay with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	55	100	
		Medium mode		-	0.55	0.9	µs
		Ultra-low-power mode		-	4	7	
V_{offset}	Comparator offset error	Full common mode range		-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 36: Embedded internal voltage reference*.
3. Guaranteed by characterization results.

6.3.23 温度传感器特性

表85. TS特性

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(2)	Average slope	2.3	2.5	2.7	mV / °C
V_{30}	Voltage at 30 °C (±5 °C)(3)	0.742	0.76	0.785	V
t_{START} (TS_BUF)(1)	Sensor buffer start-up time in continuous mode(4)	-	8	15	µs
t_{START}(1)	Start-up time when entering in continuous mode(4)	-	70	120	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	5	-	-	µs
I_{DD}(TS)(1)	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 11: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.24 VBAT 监控特性

表86. VBAT 监控特性(1)

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	3 x 39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er(2)	Error on Q	-10	-	10	%
t_{S_vbat}(2)	ADC sampling time when reading V_{BAT}	12	-	-	µs

1. 1.55 < V_{BAT} < 3.6 V.
2. Guaranteed by design.

表87. VBAT 充电特性

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

6.3.25 SMPS 下降变压器特性

The SMPS 下降变压器 characteristic are given at 4 MHz clock, with a 20 mA load(unless otherwise specified), using a 10 µH inductor and a 4.7 µF capacitor.

6.3.26 LCD 控制器特性

STM32WB55xx 设备内置了一个升压转换器，以提供一个独立于 VDD 电压的恒定 LCD 参考电压。外部电容器 Cext 必须连接到 VLCD 引脚以解耦此转换器。

表格88. LCD 控制器特性(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage		-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0		-	2.62	-	
V_{LCD1}	LCD internal reference voltage 1		-	2.76	-	
V_{LCD2}	LCD internal reference voltage 2		-	2.89	-	
V_{LCD3}	LCD internal reference voltage 3		-	3.04	-	
V_{LCD4}	LCD internal reference voltage 4		-	3.19	-	
V_{LCD5}	LCD internal reference voltage 5		-	3.32	-	
V_{LCD6}	LCD internal reference voltage 6		-	3.46	-	
V_{LCD7}	LCD internal reference voltage 7		-	3.62	-	
C_{ext}	V_{LCD} external capacitance	Buffer OFF (BUFEN=0 is LCD_CR register)	0.2	-	2	µF
		Buffer ON (BUFEN=1 is LCD_CR register)	1	-	2	
I_{LCD}(2)	Supply current from V_{DD} at V_{DD} = 2.2 V	Buffer OFF (BUFEN=0 is LCD_CR register)	-	3	-	µA
	Supply current from V_{DD} at V_{DD} = 3.0 V	Buffer OFF (BUFEN=0 is LCD_CR register)	-	1.5	-	
I_{VLCD}	Supply current from V_{LCD} (V_{LCD} = 3 V)	Buffer OFF (BUFFEN = 0, PON = 0)	-	0.5	-	µA
		Buffer ON (BUFFEN = 1, 1/2 Bias)	-	0.6	-	
		Buffer ON (BUFFEN = 1, 1/3 Bias)	-	0.8	-	
		Buffer ON (BUFFEN = 1, 1/4 Bias)	-	1	-	
R_{HN}	Total High resistor value for Low drive resistive network		-	5.5	-	MΩ
R_{LN}	Total Low resistor value for High drive resistive network		-	240	-	kΩ

表格88. LCD 控制器特性(1) (继续)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{44}	Segment/Common highest level voltage		-	V_{LCD}	-	V
V_{34}	Segment/Common 3/4 level voltage		-	3/4 V_{LCD}	-	
V_{23}	Segment/Common 2/3 level voltage		-	2/3 V_{LCD}	-	
V_{12}	Segment/Common 1/2 level voltage		-	1/2 V_{LCD}	-	
V_{13}	Segment/Common 1/3 level voltage		-	1/3 V_{LCD}	-	
V_{14}	Segment/Common 1/4 level voltage		-	1/4 V_{LCD}	-	
V_0	Segment/Common lowest level voltage		-	0	-	

1. Guaranteed by design.
2. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio = 64, all pixels active, no LCD connected.

6.3.27 定时器特性

The parameters given in the following tables are guaranteed by design. Refer to第*6.3.17*节 for details on the input/output alternate function characteristics (outputcompare, input capture, external clock, PWM output).

表格89. TIMx(1) 特性

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	15.625	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 64 MHz	0	40	
Res_{TIM}	Timer resolution	TIM1, TIM16, TIM17	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	0.015625	1024	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	-	67.10	s

1. TIMx, is used as a general term where x stands for 1, 2, 16 or 17.

表 90. IWDG 最小/最大超时周期于 32 kHz (LSI 1)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0] = 0x000	Max timeout RL[11:0] = 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock vs. the LSI clock, hence there is always a full RC period of uncertainty.

6.3.28 时钟恢复系统 (CRS)

设备内置了一个专门的块，用于自动校准内部 48 MHz 振荡器，以确保在整个设备操作范围内获得最佳精度。

这种自动校准基于外部同步信号，该信号可以从 USB 开始帧 (SOF) 信号化、LSE 振荡器、外部信号 CRS_SYNC 引脚或由用户软件生成。

为了在启动时更快地锁定，也可以将自动校准与手动校准操作结合起来。

6.3.29 通信接口特性

I2C 接口特性

I2C 接口满足 I2C-bus 规范和用户手册第 03 版本的时序要求：

- 标准模式 (Sm): 位率可达 100 kbit/s• 快速模式 (Fm): 位率可达 400 kbit/s• 快速模式加 (Fm+): 位率可达 1 Mbit/s.

表 91. 所有 I2C 模式的最小 I2CCLK 频率

Symbol	Parameter	Condition		Min	Unit
$f_{(I2CCLK)}$	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog filter ON, DNF = 0	9	
			Analog filter OFF, DNF = 1	9	
		Fast-mode Plus	Analog filter ON, DNF = 0	19	
			Analog filter OFF, DNF = 1	16	

I2C 时序要求在 I2C 外设正确配置 (设计保证).

SDA 和 SCL 的输入/输出要求满足以下限制：SDA 和 SCL 的输入/输出引脚不是开漏的。当配置为开漏时，I/O 引脚和 VDD 之间的 PMOS 被禁用，但仍然存在。快速模式加的 20 mA 输出驱动要求得到了部分支持。

这限制了快速模式加下支持的最大负载电容，由以下公式给出：

- tr(SDA/SCL) = 0.8473 x Rp x 负载电容• Rp(min) = [VDD - VOL(max)] / 输出低电平电流(max)

where R_p是 I2C 线路上拉。参考 第6.3.17节的 I2C 输入/输出特性。

所有 I2C SDA 和 SCL 输入/输出都内置了模拟滤波器，参考 表92的特性。

表 92. I2C 模拟滤波器特性(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	110(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI 特性

除非另有说明，否则在 表93中给出的 SPI 参数是在环境温度下进行的测试中得到的，f_{PCLKx} 频率和供电电压条件总结在 表24：通用运行条件。

- 输出速度设置为 OSPEEDRy[1:0] = 11• 电容负载 C = 30 皮法
- 测量点在 CMOS 水平：0.5 x VDD

参考 第6.3.17节以获取有关输入/输出替代功能特性的更多信息(NSS, SCK, MOSI, MISO SPI).

表93. SPI 特性(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 1.65 < V_{DD} < 3.6 V Voltage Range 1	-	-	32	MHz
		Master transmitter mode 1.65 < V_{DD} < 3.6 V Voltage Range 1			32	
		Slave receiver mode 1.65 < V_{DD} < 3.6 V Voltage Range 1			32	
		Slave mode transmitter/full duplex 2.7 < V_{DD} < 3.6 V Voltage Range 1			32(2)	
		Slave mode transmitter/full duplex 1.65 < V_{DD} < 3.6 V Voltage Range 1			20.5(2)	
		Voltage Range 2			8	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	4xT_{PCLK}	-	-	-
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	2xT_{PCLK}	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{PCLK} - 1.5	T_{PCLK}	T_{PCLK} + 1	
$t_{su(MI)}$	Data input setup time	Master mode	1.5	-	-	ns
$t_{su(SI)}$		Slave mode	1	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	-	34	
$t_{dis(SO)}$	Data output disable time		9	-	16	
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 < V_{DD} < 3.6 V Voltage Range 1	-	14.5	15.5	ns
		Slave mode 1.65 < V_{DD} < 3.6 V Voltage Range 1	-	15.5	24	
		Slave mode 1.65 < V_{DD} < 3.6 V Voltage Range 2	-	19.5	26	
$t_{v(MO)}$		Master mode (after enable edge)	-	2.5	3	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	8	-	-	
$t_{h(MO)}$		Master mode (after enable edge)	1	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$, which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.

图31. SPI时序图 - 从机模式和CPHA = 0

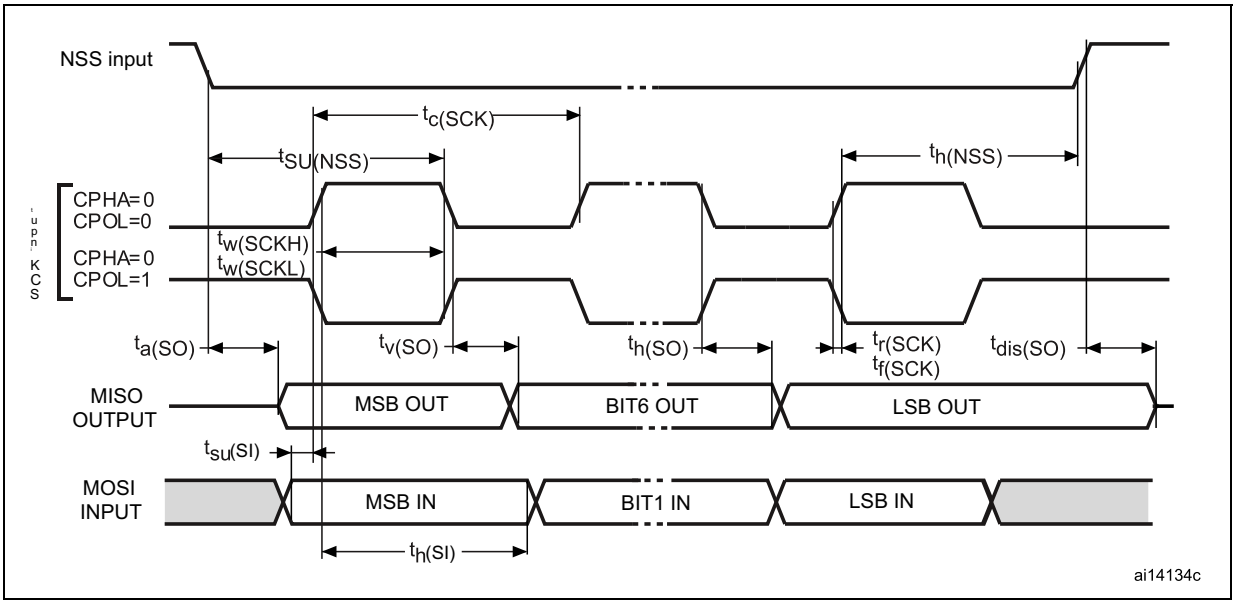
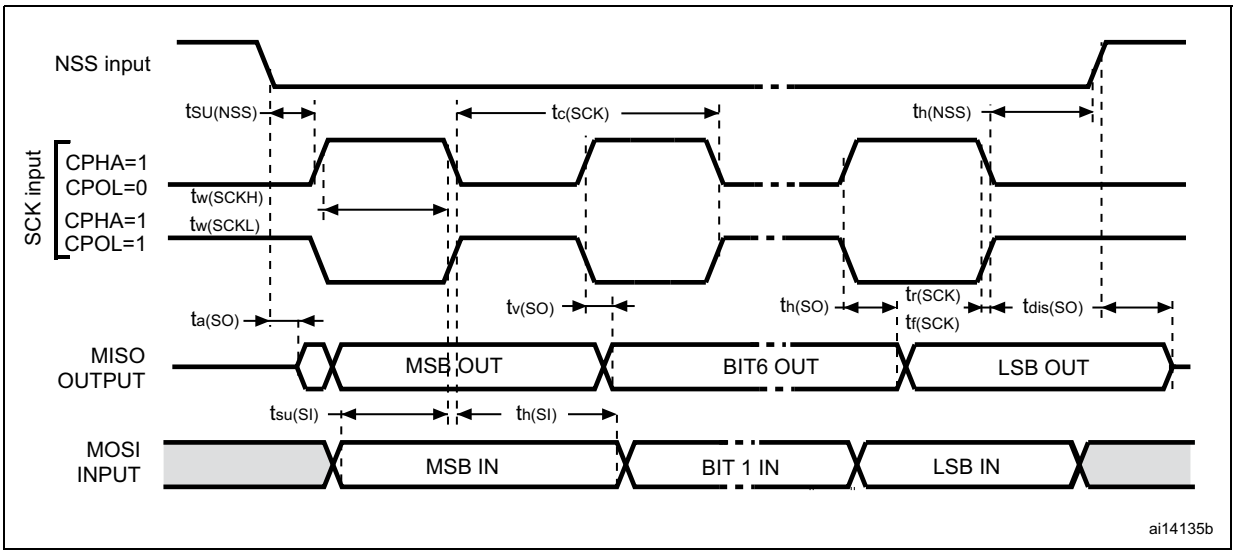
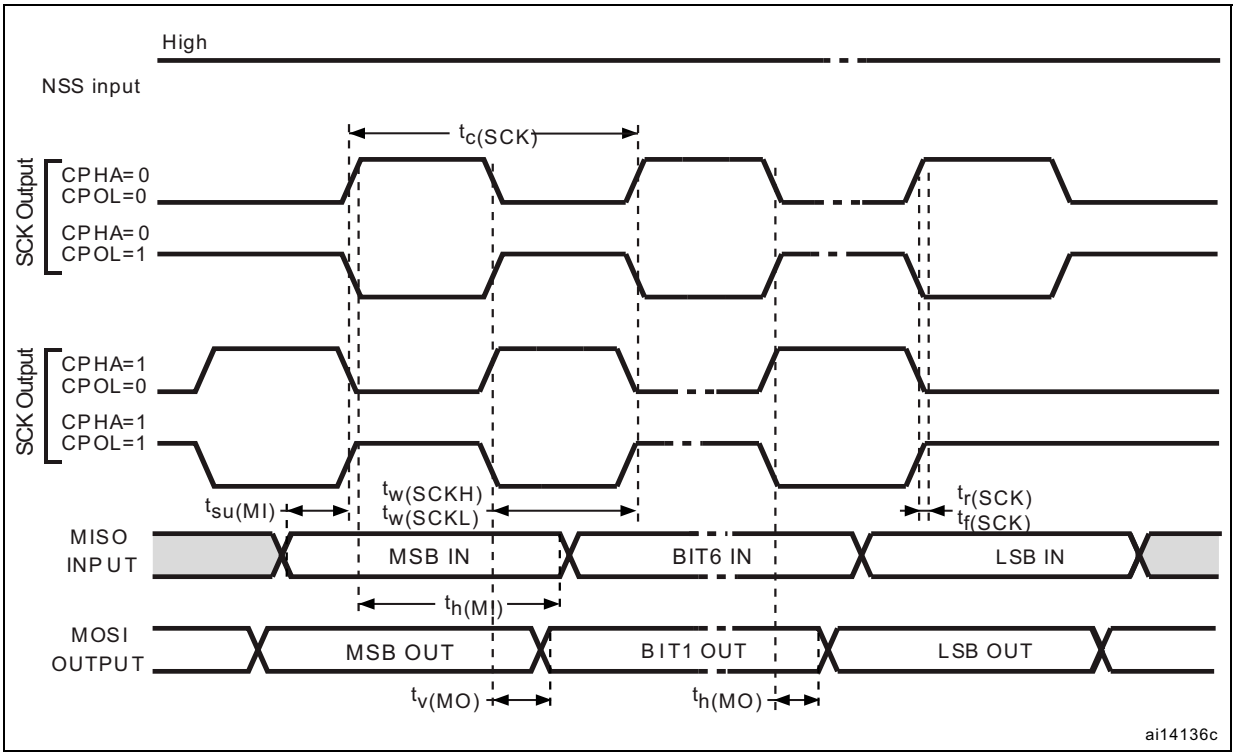


图32. SPI时序图 - 从机模式和CPHA = 1



1. 测量点设置在 CMOS 水平：0.3 VDD 和 0.7 VDD。

图33. SPI时序图 - 主模式



1. Measurement points are set at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

四线串行接口特性

Unless otherwise specified, the parameters given in 表94和 表95for 四线SPI是接口从在环境温度下进行的测试中获得的，频率为 {v3} AHB，供电电压条件总结在 表24：通用运行条件，配置如下：

- 输出速度设置为 OSPEEDRy[1:0] = 11• 电容负载 C = 15 或 20 皮法• 测量点设置在 CMOS 水平：0.5 x VDD

参考 第6.3.17节了解有关输入/输出替代功能特性的更多信息。

表94. 四线串行接口特性在 SDR模式下(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad-SPI clock frequency	1.65 < V_{DD}< 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		1.65 < V_{DD}< 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	48	
		2.7 < V_{DD}< 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	60	
		1.65 < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2	-	-	16	
$t_{w(CKH)}$	Quad-SPI clock high and low time	f_{AHBCLK}= 48 MHz, presc=1	$t_{(CK)}/2$ - 0.5	-	$t_{(CK)}/2$ + 1	ns
$t_{w(CKL)}$			$t_{(CK)}/2$ - 1	-	$t_{(CK)}/2$ + 0.5	
$t_{s(IN)}$	Data input setup time	Voltage Range 1	2	-	-	
		Voltage Range 2	3.5	-	-	
$t_{h(IN)}$	Data input hold time	Voltage Range 1	4.5	-	-	
		Voltage Range 2	6	-	-	
$t_{v(OUT)}$	Data output valid time	Voltage Range 1	-	1	1.5	
		Voltage Range 2	-	1	1.5	
$t_{h(OUT)}$	Data output hold time	Voltage Range 1	0	-	-	
		Voltage Range 2	0	-	-	

1. Guaranteed by characterization results.

表95. 四线串行接口特性在 DDR 模式下的特性(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad-SPI clock frequency	1.65 < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1		-	-	40	MHz
		2.0 < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1		-	-	50	
		1.65 < V_{DD} < 3.6 V, C_{LOAD} = 15 pF Voltage Range 1		-	-	48	
		1.65 < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2		-	-	16	
$t_{w(CKH)}$	Quad-SPI clock high and low time	f_{AHBCLK} = 48 MHz, presc=0		$t_{(CK)}/2$	-	$t_{(CK)}/2 + 1$	ns
$t_{w(CKL)}$				$t_{(CK)}/2 - 1$	-	$t_{(CK)}/2$	
$t_{sr(IN)}$	Data input setup time on rising edge	Voltage Range 1		2.5	-	-	
		Voltage Range 2		3.5			
$t_{sf(IN)}$	Data input setup time on falling edge	Voltage Range 1		2.5	-	-	
		Voltage Range 2		1.5			
$t_{hr(IN)}$	Data input hold time on rising edge	Voltage Range 1		5.5	-	-	
		Voltage Range 2		6.5			
$t_{hf(IN)}$	Data input hold time on falling edge	Voltage Range 1		5	-	-	
		Voltage Range 2		6			
$t_{vr(OUT)}$	Data output valid time on rising edge	Voltage Range 1	DHHC=0	-	4	5.5	
			DHHC=1		$t_{(CK)}/2 + 1$	$t_{(CK)}/2 + 1.5$	
		Voltage Range 2			4.5	7	
$t_{vf(OUT)}$	Data output valid time on falling edge	Voltage Range 1	DHHC=0	-	4	6	
			DHHC=1		$t_{(CK)}/2 + 1$	$t_{(CK)}/2 + 2$	
		Voltage Range 2			6	7.5	
$t_{hr(OUT)}$	Data output hold time on rising edge	Voltage Range 1	DHHC=0	2	-	-	
			DHHC=1	$t_{(CK)}/2 + 0.5$	-	-	
		Voltage Range 2		3.5	-	-	
$t_{hf(OUT)}$	Data output hold time on falling edge	Voltage Range 1	DHHC=0	3	-	-	
			DHHC=1	$t_{(CK)}/2 + 0.5$	-	-	
		Voltage Range 2		5	-	-	

1. Guaranteed by characterization results.

Figure 34. 四线SPI 时序图 - 单数据传输率

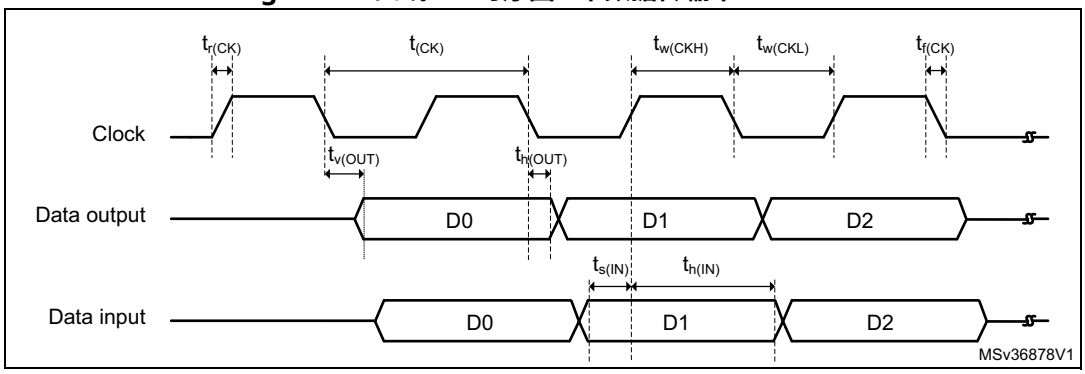
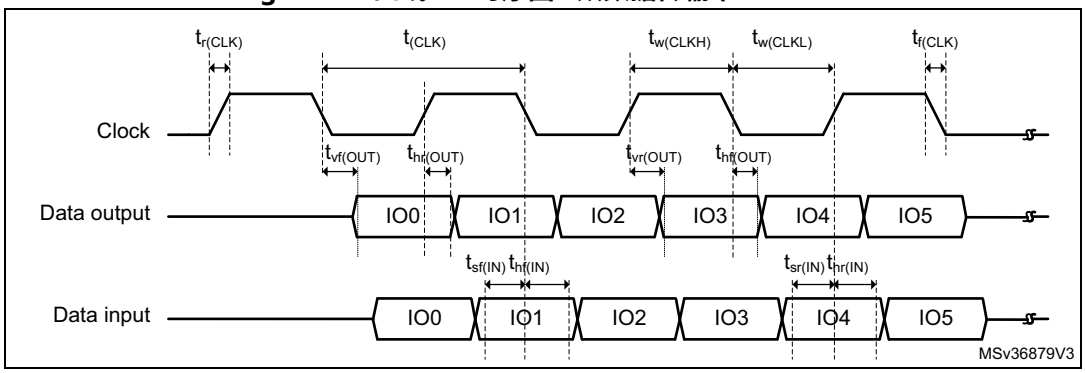


Figure 35. 四线SPI 时序图 - 双数据传输率



SAI 特性

除非另有说明，否则在 表96 中给出的参数是在环境温度、fPCLKx 频率和 VDD 下进行测试得到的，用于 SAI。

供电电压条件总结在 *表24：通用运行条件* 中，配置如下：

- 输出速度设置为 OSPEEDRy[1:0] = 10• 电容负载 C = 30 皮法
- 测量在 CMOS 水平上进行：0.5 x VDD。

请参考 *第6.3.17节* 了解更多关于输入/输出替代功能 特性 (CK,SD,FS)的信息。

表96. SAI 特性(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(2)	Master transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	23.5	
		Master transmitter 1.65 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	16	
		Master receiver Voltage Range 1	-	16	
		Slave transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	26	
		Slave transmitter 1.65 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	20	
		Slave receiver Voltage Range 1	-	32	
		Voltage Range 2	-	8	
$t_{v(FS)}$	FS valid time	Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	21	ns
		Master mode 1.65 V ≤ V_{DD} ≤ 3.6 V	-	30	
$t_{h(FS)}$	FS hold time	Master mode	10	-	
$t_{su(FS)}$	FS setup time	Slave mode	1.5	-	
$t_{h(FS)}$	FS hold time	Slave mode	2.5	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	1.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	6.5	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	19	
		Slave transmitter (after enable edge) 1.65 V ≤ V_{DD} ≤ 3.6 V	-	25	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	-	
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	18.5	
		Master transmitter (after enable edge) 1.65 V ≤ V_{DD} ≤ 3.6 V	-	25	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	10	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.

图36. SAI 主机定时波形

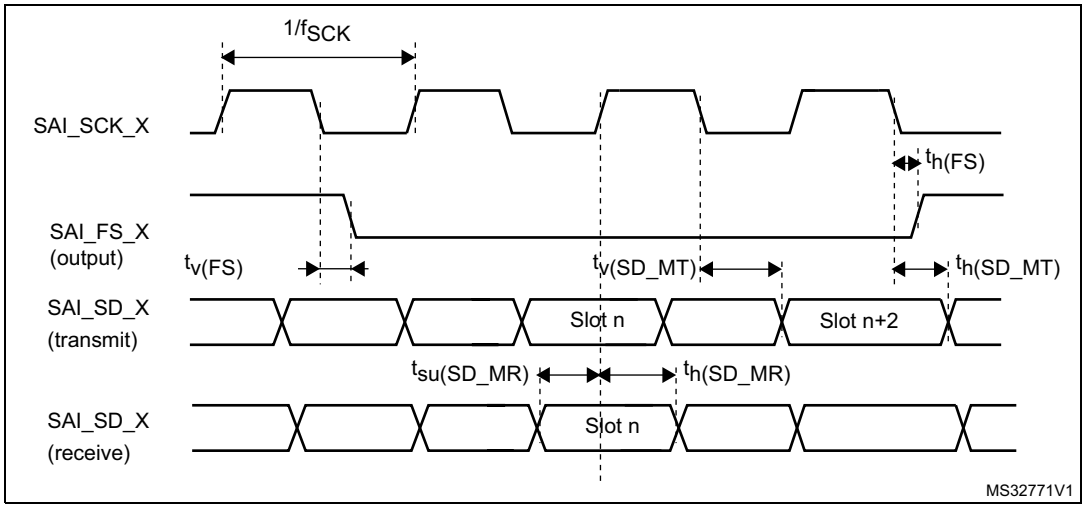
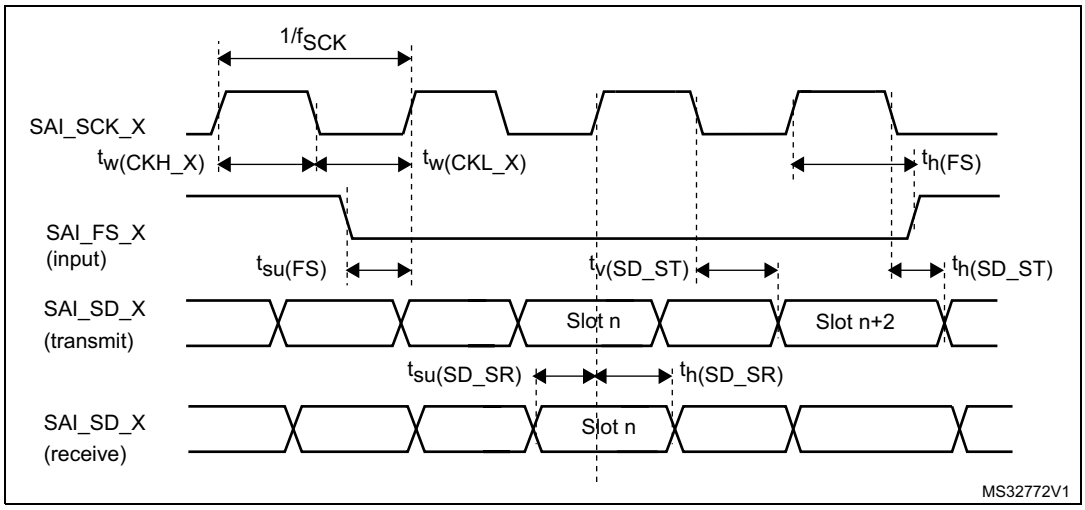


图37. SAI 从机定时波形



USB 特性

STM32WB55xx 和 STM32WB35xx USB 接口完全符合 USB 规范版本 2.0，且是 USB-IF 认证 (用于 Full-speed 设备操作).

表 97. USB 电气特性(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDUSB}	USB transceiver operating voltage	-	3.0(2)	-	3.6	V
$T_{crystal\_less}$	USB crystal-less operation temperature	-	-15	-	85	°C
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1400	2300	3200	
Z_{DRV}(3)	Output driver impedance(4)	Driving high and low	28	36	44	

1. T_A = -40 to 125 °C unless otherwise specified.
2. The STM32WB55xx and STM32WB35xx USB functionality is ensured down to 2.7 V, but the full USB electrical characteristics are degraded in the 2.7 to 3.0 V voltage range.
3. Guaranteed by design.
4. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

JTAG/SWD 接口特性

除非另有说明，参数在 表 98 和 表 99 中给出，这些参数是在环境温度、f_{PCLKx} 频率和供电电压条件下进行的测试得到的，这些条件总结在 表 24：通用运行条件 中，配置如下：

- 电容负载 C = 30 pF
- 测量点在 CMOS 水平：0.5 x VDD 上进行

表 98. JTAG 特性

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/t_{c(TCK)}$	TCK clock frequency	2.7 < V_{DD} < 3.6 V	-	-	29	MHz
		1.65 < V_{DD} < 3.6 V	-	-	21	
$t_{isu(TMS)}$	TMS input setup time	-	2.5	-	-	ns
$t_{ih(TMS)}$	TMS input hold time	-	2	-	-	
$t_{isu(TDI)}$	TDI input setup time	-	1.5	-	-	
$t_{ih(TDI)}$	TDI input hold time	-	2	-	-	
$t_{ov(TDO)}$	TDO output valid time	2.7 < V_{DD} < 3.6 V	-	13.5	16.5	
		1.65 < V_{DD} < 3.6 V	-	13.5	23	
$t_{oh(TDO)}$	TDO output hold time	-	11	-	-	

表99. SWD特性

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/t_{c(SWCLK)}$	SWCLK clock frequency	$2.7 < V_{DD} < 3.6$ V	-	-	55	MHz
		$1.65 < V_{DD} < 3.6$ V	-	-	35	
$t_{isu(TMS)}$	SWDIO input setup time	-	2.5	-	-	ns
$t_{ih(TMS)}$	SWDIO input hold time	-	2	-	-	
$t_{ov(TDO)}$	SWDIO output valid time	$2.7 < V_{DD} < 3.6$ V	-	16	18	
		$1.65 < V_{DD} < 3.6$ V	-	16	28	
$t_{oh(TDO)}$	SWDIO output hold time	-	13	-	-	

Refer to 第*6.3.17*节 for more details on the input/output alternate function characteristics(CK, SD, WS).

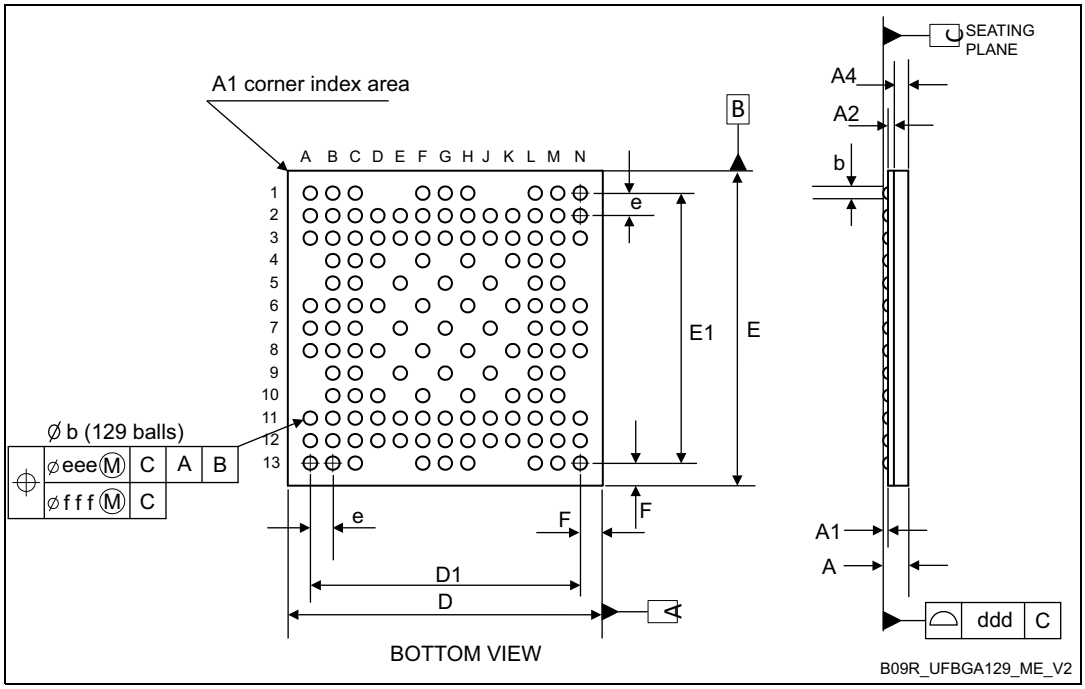
7 包装信息

为了满足环境要求，ST 提供了不同等级的 ECOPACK 封装设备，这取决于它们的环境合规程度。ECOPACK 规范、等级定义和产品状态可在以下位置找到：www.st.com。
ECOPACK 是 ST 商标。

7.1 UFBGA129 包装信息

这个 UFBGA 是一个 129 球, 7 x 7 毫米, 0.5 毫米细距离, 正方形球阵列封装.

图 38. UFBGA129 包装轮廓



1. Drawing is not to scale.
2. - 终端 A1 角必须通过使用角缺口， 墨水或金属标记, 或者包体或集成散热块的其他特征来在顶部表面上识别. - 在包装的底部表面上允许有一个区分特征来识别终端 A1 角. 每个角的精确形状是可选的.

表 100. UFBGA129机械数据

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A(2)	-	-	0.60	-	-	0.024
A1	-	-	0.11	-	-	0.004
A2	-	0.13	-	-	0.005	-
A4	-	0.32	-	-	0.013	-
b(3)	0.24	0.29	0.34	0.009	0.011	0.013

表100. UFBGA129机械数据(继续)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	6.85	7.00	7.15	0.270	0.276	0.281
E	6.85	7.00	7.15	0.270	0.276	0.281
D1	-	6.00	-	-	0.236	-
E1	-	6.00	-	-	0.236	-
e	-	0.50	-	-	0.020	-
F	-	0.50	-	-	0.020	-
ddd	-	-	0.08	-	-	0.003
eee[4]	-	-	0.15	-	-	0.006
fff[5]	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to four decimal digits.

2. - UFBGA 代表超薄轮廓细距离球阵。 - 超薄轮廓: 0.50 < A ≤ 0.65mm / 细距离: e < 1.00mm pitch。
- 总轮廓高度 (Dim A) 从座面到组件顶部测量。 - 最大总包装高度按照以下方法计算： A Max = A1 Typ + A2 Typ + A4 Typ + √ (A1²+A2²+A4² 容差值)。

3. 典型安装前的球直径为 0.20 mm。

4. 控制球模式相对于基准A和B的位置的位置公差。 每个球都有一个与基准C垂直且位于相对于基准A和B的真实位置的圆柱形公差区域eee。每个球的与基准C垂直的轴必须位于此公差区域内。

5. 控制球在矩阵中相对于彼此的位置的位置公差。 每个球都有一个与基准C垂直且位于由e定义的真实位置的圆柱形公差区域fff。每个球的与基准C垂直的轴必须位于此公差区域内。数组中每个公差区域fff都完全位于上述各自的公差区域eee内。每个球的轴必须同时位于这两个公差区域内。

图39. UFBGA129 推荐尺寸

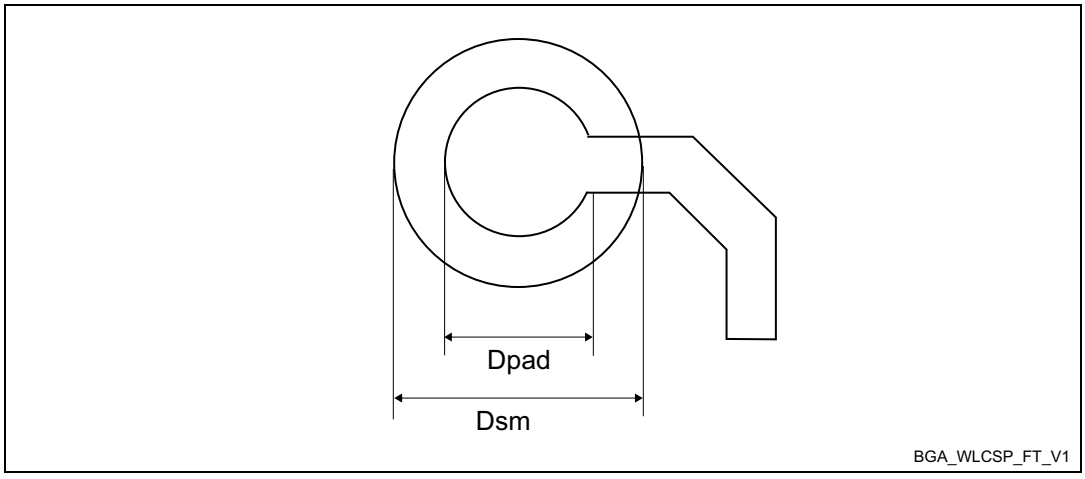


表101. UFBGA129 推荐的PCB设计规则

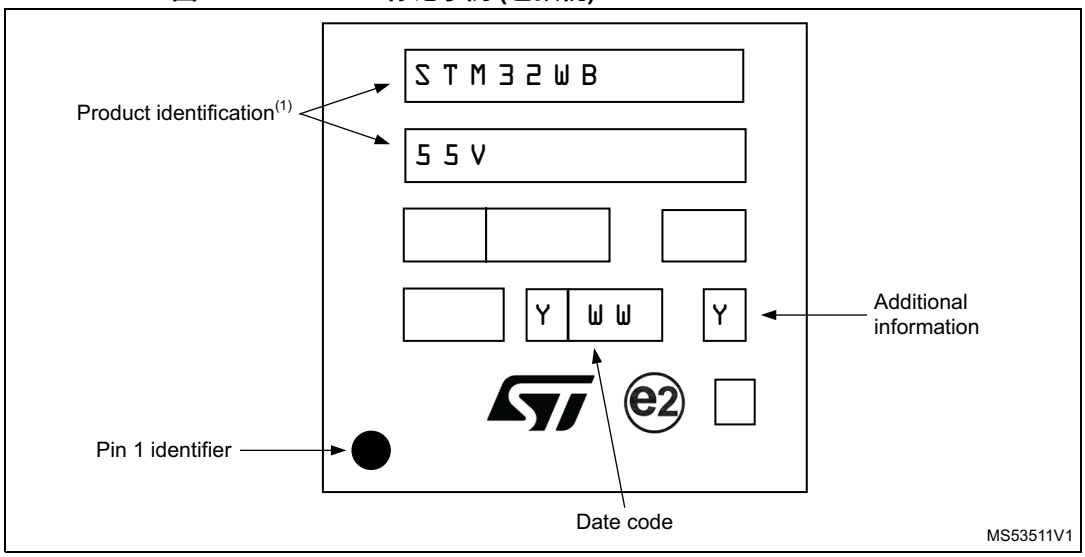
Dimension	Recommended values
Pitch	0.5 mm
Dpad	0,360 mm
Dsm	0.460 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.360 mm
Stencil thickness	0.100 mm

UFBGA129的设备标记

图*40*给出了正面标记方向与引脚1标识位置的比较。打印标记可能会因为供应链而有所不同。

其他可选标记或嵌入/突出标记，用于识别供应链操作中的零件，以下没有显示。

图40. UFBGA129 标记示例 (包顶视)



1. 标记为 ES 或 E 或附有工程样本通知信的零件尚未合格，因此不批准用于生产。ST 不对由此使用导致的后果负责。在任何情况下，ST 都不会因客户在生产中使用这些工程样本而负责。ST's 质量部门在做出任何决定之前必须被联系以运行合格活动。

7.2 WLCSP100 封装信息

WLCSP100 是一个 100颗, 4.390 x 4.371 毫米, 0.4 毫米间距, 晶圆级芯片尺度封装。

图41. WLCSP100 轮廓

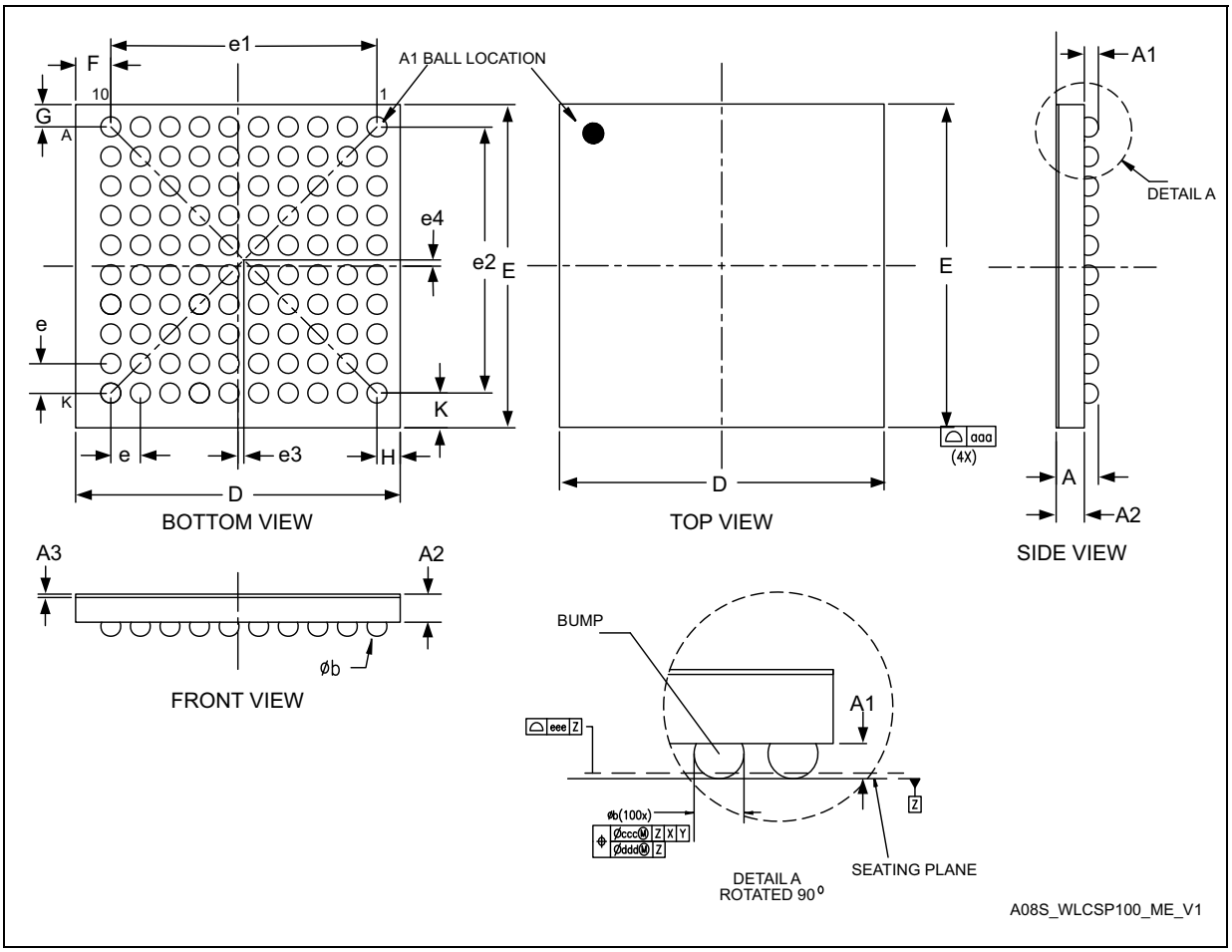
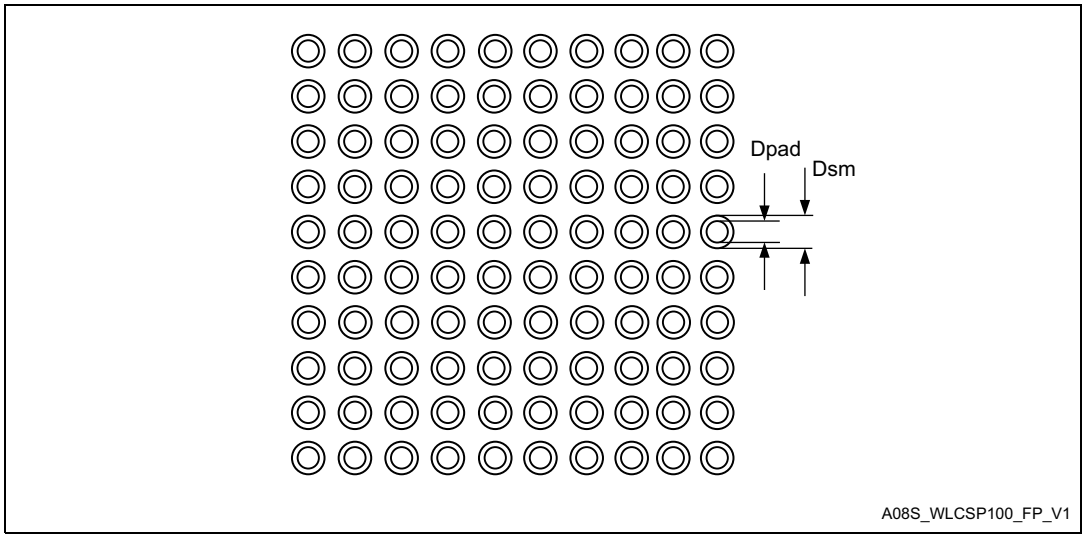


表102. WLCSP100机械数据

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3	-	0.025[2]	-	-	0.001	-
b	0.22	0.25	0.28	0.009	0.010	0.0110
D	4.38	4.40	4.42	0.1715	0.1728	0.1742
E	4.36	4.38	4.40	0.1707	0.1721	0.1735
e	-	0.40	-	-	0.0157	-
e1	-	3.60	-	-	0.1417	-
e2	-	3.60	-	-	0.1417	-
e3	-	0.08	-	-	0.0031	-
e4	-	0.08	-	-	0.0033	-
F	-	0.480[3]	-	-	0.0187	-
G	-	0.306[3]	-	-	0.0119	-
H	-	0.32	-	-	0.0124	-
K	-	0.47	-	-	0.0185	-
aaa	-	-	0.10	-	-	0.0039
bbb	-	-	0.10	-	-	0.0039
ccc	-	-	0.10	-	-	0.0039
ddd	-	-	0.05	-	-	0.0020
eee	-	-	0.05	-	-	0.0020

1. Values in inches are converted from mm and rounded to the third decimal place.
2. Nominal dimension rounded to the third decimal place results from process capability.
3. Calculated dimensions are rounded to third decimal place.

图42. WLCSP100 推荐尺寸



1. 尺寸以毫米为单位。

表103. WLCSP100推荐的PCB设计规则

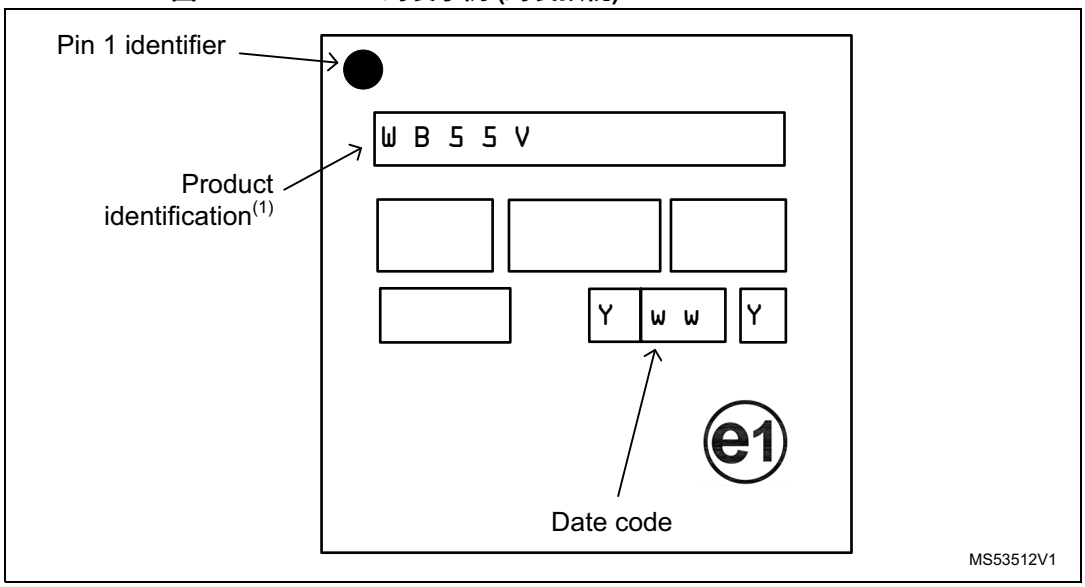
Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

WLCSP100设备标记

图*43*给出了正面标记方向与引脚1标识位置的比较。打印标记可能会因为供应链而有所不同。

其他可选标记或嵌入/突出标记，用于在供应链操作中识别零件，未在下面指示。

图43. WLCSP100 封装示例 (封装顶视)

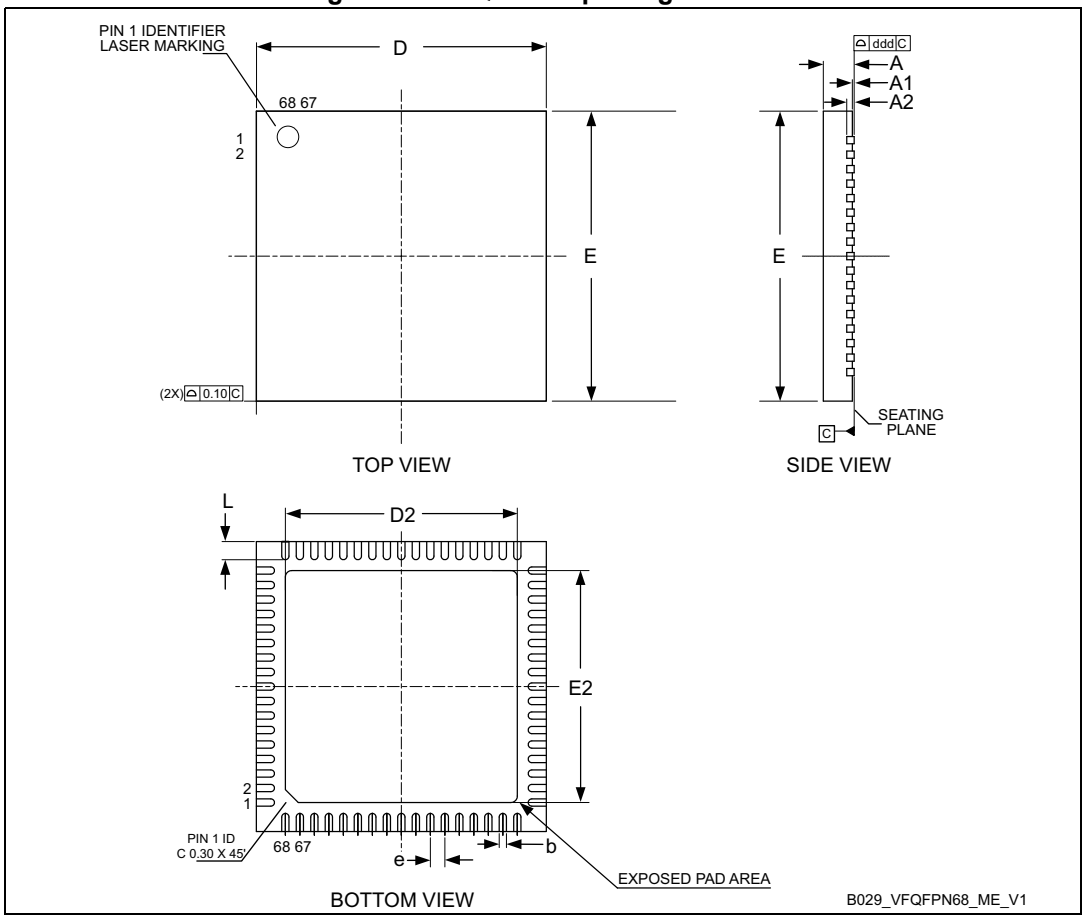


1. 标记为 ES 或 E 或附有工程样本通知信的零件尚未合格，因此不批准用于生产。ST 不负责任何使用这些零件导致的后果。在任何事件中，ST 都不负责客户在生产中使用这些工程样本。在决定使用这些工程样本运行合格活动之前，必须联系 ST 的质量部门。

7.3 VFQFPN68 包信息

VFQFPN68 是一个 8 x 8 毫米, 0.4 毫米间距, 非常薄的细距离四面包封装。

Figure 44. VFQFPN68 package outline



1. VFQFPN for 热性能增强的非常薄的细距离四面包封装无铅。锯割版本。非常薄的轮廓：0.80 < A ≤ 1.00 mm. 2. 引脚 #1 标识必须存在于包体通过凹陷标记或其他特征在顶部表面上标识。此特征的确切形状和大小是可选的。

表104. VFQFPN68机械数据

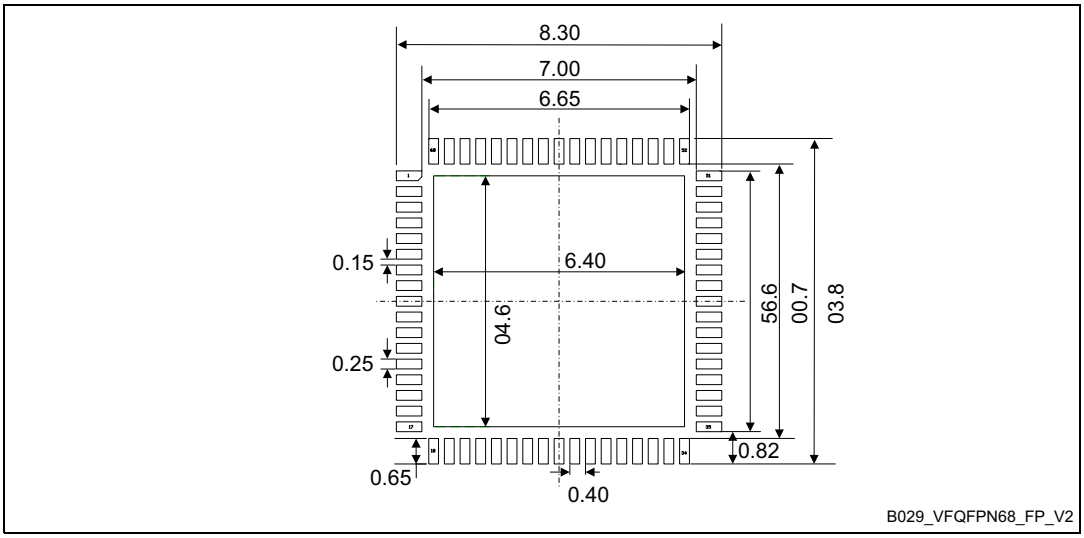
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0	0.02	0.05	0	0.0008	0.0020
A3	-	0.20	-	-	0.0008	-
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
D	7.85	8.00	8.15	0.3091	0.3150	0.3209
D2	6.30	6.40	6.50	0.2480	0.2520	0.2559

表104. VFQFPN68机械数据 (继续)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E	7.85	8.00	8.15	0.3091	0.3150	0.3209
E2	6.30	6.40	6.50	0.2480	0.2520	0.2559
e	-	0.40	-	-	0.0157	-
L	0.40	0.50	0.60	0.0157	0.0197	0.0236
ddd	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.

图45. VFQFPN68 推荐尺寸



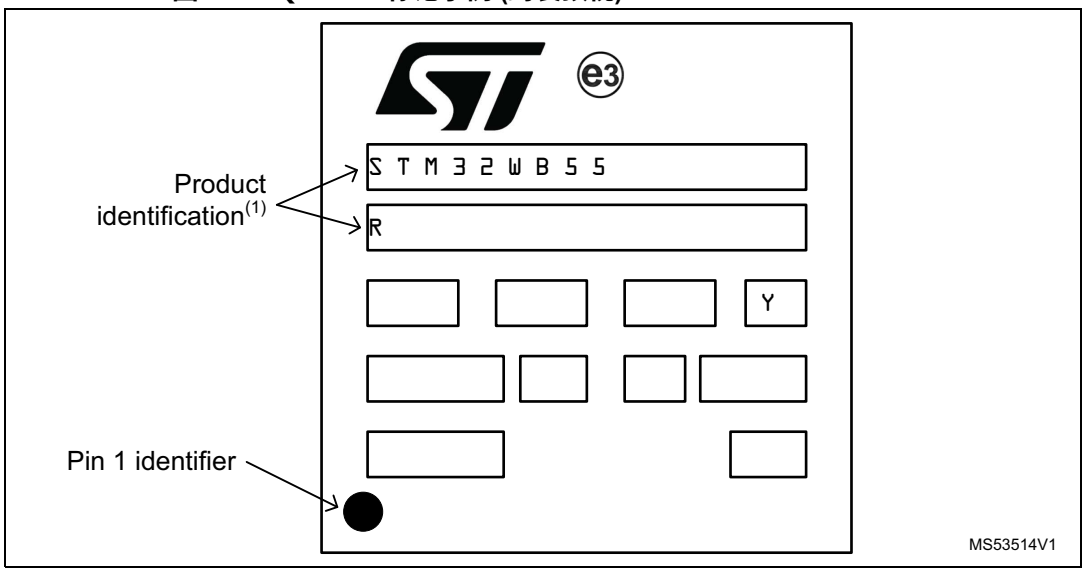
1. 尺寸以毫米为单位。

VFQFPN68设备标记

图*45*给出了正面标记方向与引脚1标识位置的例子。打印标记可能会因供应链而异。 .

其他可选标记或嵌入/突出标记，用于识别供应链操作中的零件，未在下面显示。

图46. VFQFPN68 标记示例 (封装顶视)

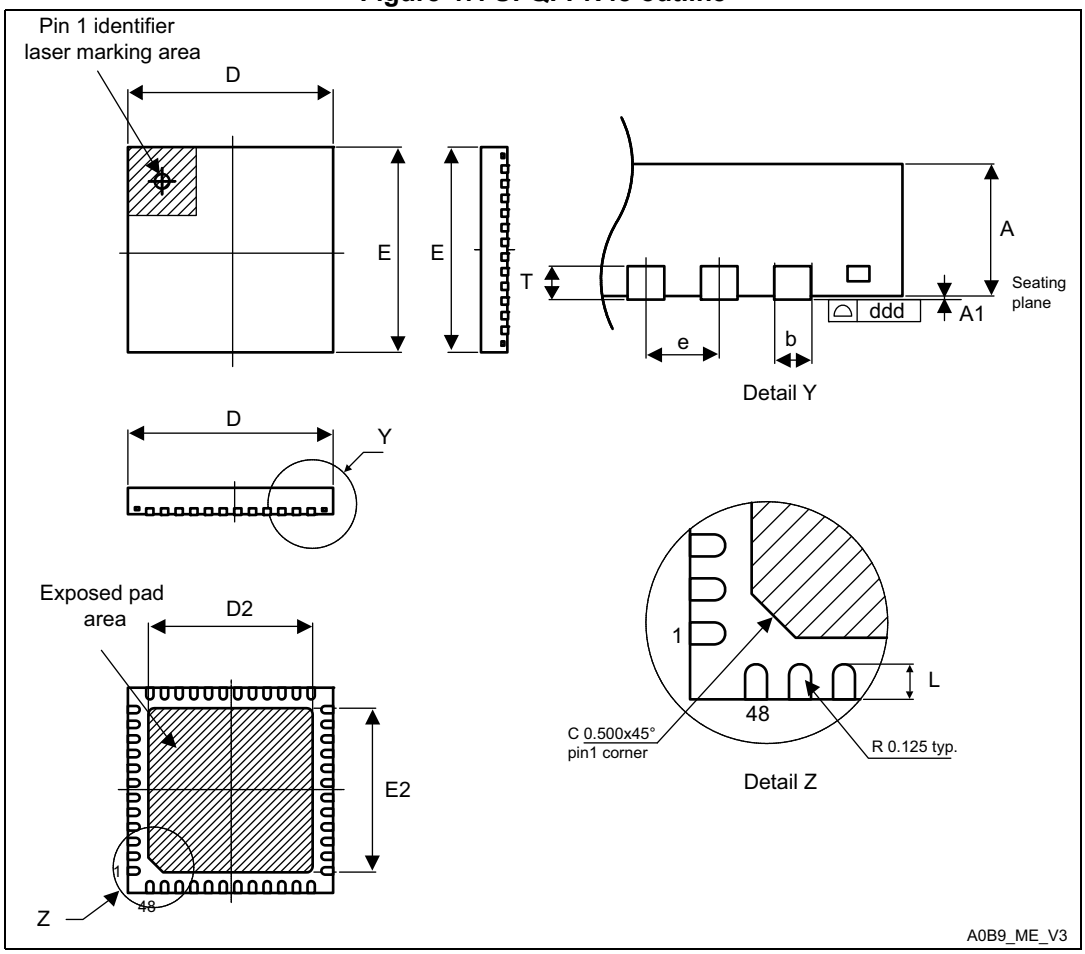


1. 标记为 ES 或 E 的零件，或附有工程样本通知信的零件，尚未合格，因此不批准用于生产。ST不负责因使用这些零件而导致的任何后果。在任何事件中，ST都不负责客户在生产中使用这些工程样本。ST's 质量部门必须在做出使用这些工程样本的决定之前进行联系，以运行合格活动。

7.4 UFQFPN48 包信息

UFQFPN48 是一个 48 脚，7 x 7 毫米，0.5 毫米距离，超薄细距离平板封装。

Figure 47. UFQFPN48 outline



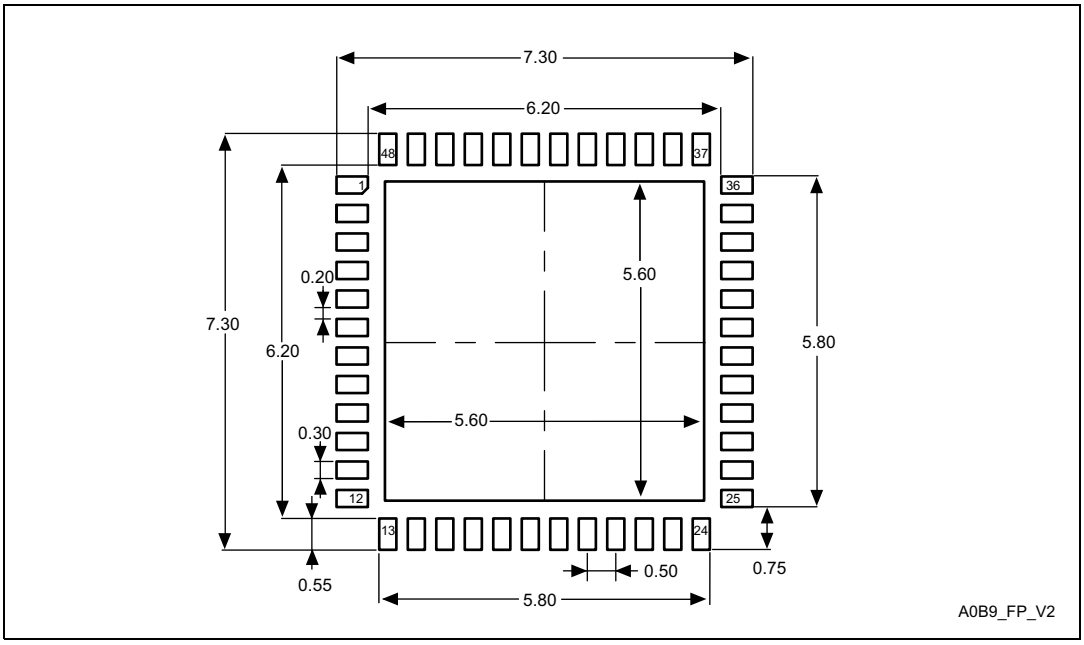
1. 图纸不按比例。 2. 所有脚/铜箔也应连接到 PCB 上焊接，以改善脚/铜箔焊接寿命。 3. UFQFPN 封装的下面有一个暴露的晶圆底部，它必须电气上连接到 PCB 地。

表 105. UFQFPN48机械数据

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.

图48. UFQFPN48 推荐尺寸



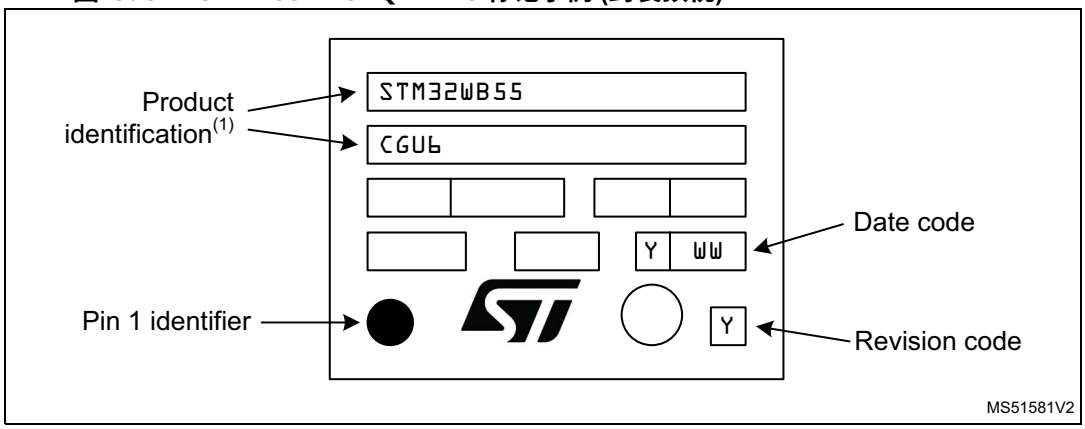
1. 尺寸以毫米为单位。

UFQFPN48 的设备标记

图*49* and 图*50*给出正面标记方向与引脚1标识位置的例子。打印标记可能会因为供应链而有所不同。

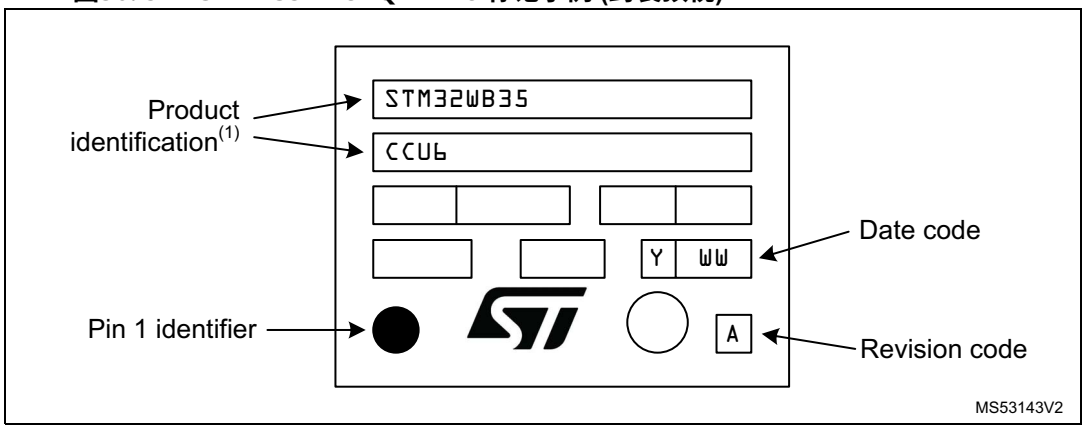
其他可选标记或嵌入/突出标记，用于在供应链操作中识别零件，以下未示示。

图49. STM32WB55xx UFQFPN48 标记示例 (封装顶视)



1. 标记为 “ES”, “E” 或附有工程样本通知信的零件尚未合格，因此尚未准备好用于生产，从而产生的任何后果将不会由 ST 费用承担。在任何事件下，ST 不负责客户在生产中使用这些工程样本。在做出是否使用这些工程样本进行合格活动的决定之前，必须联系 ST Quality。

图50. STM32WB35xx UFQFPN48 标记示例 (封装顶视)



1. 标记为 “ES”, “E” 或附有工程样本通知信的零件尚未合格，因此尚未准备好用于生产，从而产生的任何后果将不会由 ST 费用承担。在任何事件下，ST 不负责客户在生产中使用这些工程样本。在做出是否使用这些工程样本进行合格活动的决定之前，必须联系 ST Quality。

7.5 热特性

The maximum chip junction temperature (TJmax) must never exceed the values given in 表 24：通用运行条件.

最大芯片接合温度，TJ max，以摄氏度为单位，可以通过以下方程计算：

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

where:

- TA max 是最大环境温度，以 °C 为单位，• Θ_{JA} 是包装焊盘到环境热阻，以 °C / W 为单位，• PD max 是 PINT max 和 PI/O max 的和 (PD max = PINT max + PI/O max),• PINT max 是 IDD 和 VDD 的乘积，以 瓦 为单位。这是最大芯片内部功率。

PI/O max 表示输出引脚的最大功率散失：

- $P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH})$

考虑应用中 I/Os 在低电平和高电平下的实际 VOL / IOL 和 VOH / IOH。

Note: 当使用 *SMPS* 时，一部分功率消耗被散热到外部电感器中，因此降低了芯片功率散热。这个部分主要依赖于电感器 *ESR* 特性。

注意: 由于辐射无线电功率非常低 *(< 4 mW)*，因此不需要从中移除它。
芯片功率消耗。

注意: *RF* 特性 *(*例如灵敏度，*Tx* 功率，消耗*)* 都提供到 *85 °C*。

表 106. 包装热特性

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFQFPN48 - 7 mm x 7 mm	24.9	°C/W
	Thermal resistance junction-ambient VFQFPN68 - 8 mm x 8 mm	47.0	
	Thermal resistance junction-ambient WLCSP100 - 0.4 mm pitch	35.8	
	Thermal resistance junction-ambient UFBGA129 - 0.5 mm pitch	41.5	
Θ_{JB}	**Thermal resistance junction-board** UFQFPN48 - 7 mm x 7 mm	13.0	°C/W
	Thermal resistance junction-board VFQFPN68 - 8 mm x 8 mm	36.1	
	Thermal resistance junction-board WLCSP100 - 0.4 mm pitch	N/A	
	Thermal resistance junction-board UFBGA129 - 0.5 mm pitch	16.2	

表 106. 包装热特性 (继续)

Symbol	Parameter	Value	Unit
Θ_{JC}	**Thermal resistance junction-case** UFQFPN48 - 7 mm x 7 mm	1.3	°C/W
	Thermal resistance junction-case VFQFPN68 - 8 mm x 8 mm	13.7	
	Thermal resistance junction-case WLCSP100 - 0.4 mm pitch	N/A	
	Thermal resistance junction-case UFBGA129 - 0.5 mm pitch	34.9	

7.5.1 参考文献

JESD51-2 集成电路热测试方法环境条件 - 自然对流 (平静空气)。可在 www.jedec.org 获取。

7.5.2 选择产品温度范围

When ordering the microcontroller, the temperature range is specified in the orderinginformation scheme shown in 第 *8* 节.

每个温度范围后缀对应于特定的在大散热时的保证环境温度，以及特定的最大接合温度。

由于应用通常不会使用设备在最大散热时，因此计算精确的功率消耗和接合温度是有用的，以确定哪个温度范围最适合应用。

以下示例展示了如何为给定的应用计算所需的温度范围。

示例 1: 高性能应用

假设以下应用条件：

最大环境温度TA max = 82 °C (根据JESD51-2)测量，IDD max = 50 mA，VDD = 3.5 V，同时使用最大20个输入/输出在低电平输出，IOL = 8 mA，VOL = 0.4 V，以及同时使用最大8个输入/输出在低电平输出，IOL = 20 mA，VOL= 1.3 V PINT max = 50 mA × 3.5 V = 175 mW PIO max = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW 这给出了：PINT max = 175 mW 和 PIO max = 272 mW PD max = 175 + 272 = 447 mW

使用 表*106* 中获得的值，可以按照以下方式计算TJ max：

– 对于 VFQFPN68， 47 °C / W TJ max = 82 °C + (47 °C / W × 447 毫瓦) = 82 °C + 21 °C = 103 °C

这在后缀 6 版本部件的范围内(–40 < TJ < 105 °C), see 第 *8* 节.

在这种情况下，零件必须至少以温度范围后缀 6 订购。

Note: With this given 最大功率密度 user can find the TA max allowed for a given device temperature range (order code suffix 7).

后缀 7: TA max = TJ max - (47 ° °C / W × 447 毫瓦) = 125 ° °C - 21 ° °C = 103 ° °C

例 2: 高温应用

使用相同的规则，可以处理在高环境温度下运行的应用程序，只要接合温度TJ在指定范围内，并且散热量较低。

假设以下应用条件：

最大环境温度TA max = 100 °C (根据JESD51-2)测量，IDD max = 50 mA，VDD = 3.5 V，最多20个输入/输出同时在低电平输出，IOL = 8 mA，VOL= 0.4 V PINT max = 50 mA × 3.5 V = 175 mW PIO max = 20 × 8 mA × 0.4 V = 64 mW。这给出了PINTmax = 175 mW和PIO max = 64 mW，PD max = 175 + 64 = 239 mW

因此: PD max = 239 mW

使用表106中获得的值表 *106* TJ max 的计算方法如下:

– For UFQFPN48, 24.9 °C / W

T_J max = 100 °C + (24.9 °C / W × 239 mW) = 100 °C + 6 °C = 106 °C

这超出了后缀 6 版本部件 (–40 < TJ < 105 °C) 的温度范围。

在这种情况下，零件必须至少以温度范围后缀 7 (参见章 *8*), 用户减少功率损失才能使用后缀 6 零件。

8 订购信息

Example: STM32 WB 55 V G V 6 A TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

WB = Wireless Bluetooth®

Device subfamily

55 = Die 5, full set of features

35 = Die 3, full set of features(1)

Pin count

C = 48 pins

R = 68 pins

V = 100 or 129 pins

Flash memory size

C = 256 Kbytes

E = 512 Kbytes

Y(2) = 640 Kbytes

G = 1 Mbyte

Package

U = UFQFPN48 7 x 7 mm

V = VFQFPN68 8 x 8 mm

Y = WLCSP100 0.4 mm pitch

Q = UFBGA129 0.5 mm pitch

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)

7 = Industrial temperature range, -40 to 105 °C (125 °C junction)

Identification code

A = Proprietary identification code

blank = Non-proprietary identification code

Packing

TR = tape and reel

xxx = programmed parts

1. STM32WB35xx only available with 48-pin UFQFPN48 package, 256 or 512 Kbytes Flash memory.
2. Only STM32WB55VY, WLCSP100 package, temperature range -40 to 85 °C (105 °C junction).

9 修订历史

表107. 文档修订历史

Date	Revision	Changes
25-Jul-2017	1	Initial release.
04-Apr-2018	2	Updated document title, *Features*, *Section 1: Introduction*, *Section 2: Description*, *Section 3.1: Architecture*, *Section 3.3.2: Memory protection unit*, *Section 3.3.3: Embedded Flash memory*, *Section 3.4: Security and safety*, *Section 3.6: RF subsystem*, *Section 3.6.1: RF front-end block diagram*, *Section 3.6.2: BLE general description*, *Section 3.7.1: Power supply distribution*, *Section 3.7.2: Power supply schemes*, *Section 3.7.4: Power supply supervisor*, *Section 3.10: Clocks and startup*, *Section 3.14: Analog to digital converter (ADC)*, *Section 3.19: True random number generator (RNG)*, *Section 5: Memory mapping*, *Section 6.3.25: SMPS step-down converter characteristics* and *Section 7.5.2: Selecting the product temperature range*. Updated *Table 2: STM32WB55xx devices features and peripheral counts*, *Table 6: Power supply typical components*, *Table 7: Features over all modes*, *Table 8: STM32WB55xx modes overview*, *Table 13: Timer features*, *Table 15: Legend/abbreviations used in the pinout table*, *Table 16: STM32WB55xx pin and ball definitions*, *Table 17: Alternate functions*, *Table 23: RF transmitter BLE characteristics*, *Table 26: RF receiver BLE characteristics (1 Mbps)* and added footnote to it, *Table 28: RF BLE power consumption for VDD = 3.3 V*, *Table 31: RF 802.15.4 power consumption for VDD = 3.3 V*, *Table 37: Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF), VDD= 3.3 V*, *Table 38: Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1, VDD = 3.3 V*, *Table 40: Current consumption in Low-power sleep modes, Flash memory in Power down*, *Table 41: Current consumption in Stop 2 mode*, *Table 42: Current consumption in Stop 1 mode*, *Table 43: Current consumption in Stop 0 mode*, *Table 44: Current consumption in Standby mode*, *Table 45: Current consumption in Shutdown mode*, *Table 48: Peripheral current consumption*, *Table 104: Package thermal characteristics* and *Table 97: STM32WB55xx ordering information scheme*. Added *Table 47: Current under Reset condition*. Updated *Figure 1: STM32WB55xx block diagram*, *Figure 2: STM32WB55xx RF front-end block diagram*, *Figure 4: Power distribution*, *Figure 6: Power supply overview*, *Figure 7: Clock tree*, *Figure 8: STM32WB55Cx UFQFPN48 pinout*(1)(2), *Figure 9: STM32WB55Rx VFQFPN68 pinout*(1)(2), *Figure 10: STM32WB55Vx WLCSP100 ballout*(1) and *Figure 14: Power supply scheme (all packages except UFBGA129)*.

表107. 文档修订历史 (继续)

Date	Revision	Changes
08-Oct-2018	3	Changed document classification to Public. Updated *Features*, *Section 3.6.2: BLE general description*, *Section 3.7.2: Power supply schemes*, *Section 3.7.3: Linear voltage regulator*, *Section 3.10: Clocks and startup*, *Section 6.3.10: External clock source characteristics*, *Section 6.3.20: Analog-to-Digital converter characteristics*, *Section 6.3.29: Communication interfaces characteristics*, *Section 7.2: WLCSP100 package information* and *Section 7.5: Thermal characteristics*. Replaced V_{DDIOx} with V_{DD} throughout the whole document. Updated *Table 5: Typical external components*, footnote *2* of *Table 7: Features over all modes*, *Table 8: STM32WB55xx modes overview* and its footnote *5*, *Table 12: Internal voltage reference calibration values*, *Table 16: STM32WB55xx pin and ball definitions* and its footnote *6*, *Table 17: Alternate functions*, *Table 20: Thermal characteristics*, *Table 21: Main performance at VDD = 3.3 V*, *Table 21: Main performance at VDD = 3.3 V*, *Table 22: General operating conditions*, *Table 23: RF transmitter BLE characteristics* and its footnote, *Table 26: RF receiver BLE characteristics (1 Mbps)*, *Table 28: RF BLE power consumption for VDD = 3.3 V*, *Table 29: RF transmitter 802.15.4 characteristics* and its footnote *1*, *Table 30: RF receiver 802.15.4 characteristics*, *Table 31: RF 802.15.4 power consumption for VDD = 3.3 V*, *Table 34: Embedded internal voltage reference*, *Table 35: Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF), VDD = 3.3 V*, *Table 36: Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, VDD = 3.3 V*, *Table 37: Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF), VDD= 3.3 V*, *Table 38: Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1, VDD = 3.3 V*, *Table 39: Current consumption in Sleep and Low-power sleep modes, Flash memory ON*, *Table 40: Current consumption in Low-power sleep modes, Flash memory in Power down*, *Table 41: Current consumption in Stop 2 mode*, *Table 42: Current consumption in Stop 1 mode*, *Table 43: Current consumption in Stop 0 mode*, *Table 44: Current consumption in Standby mode*, *Table 45: Current consumption in Shutdown mode*, *Table 46: Current consumption in VBAT mode*, *Table 47: Current under Reset condition*, *Table 48: Peripheral current consumption*, *Table 49: Low-power mode wakeup timings*, *Table 50: Regulator modes transition times*, *Table 51: Wakeup time using LPUART*, *Table 53: HSE clock source requirements* and added footnote to it, *Table 61: LSI2 oscillator characteristics*, *Table 63: Flash memory characteristics*, *Table 65: EMS characteristics*, *Table 67: ESD absolute maximum ratings*, *Table 69: I/O current injection susceptibility*, *Table 70: I/O static characteristics* and its footnotes, *Table 71: Output voltage characteristics*, *Table 72: I/O AC characteristics* and its footnotes *1* and *2*, *Table 73: NRST pin characteristics*, *Table 77: ADC accuracy - Limited test conditions 1*, *Table 78: ADC accuracy - Limited test conditions 2*, *Table 79: ADC accuracy - Limited test conditions 3*, *Table 80: ADC accuracy - Limited test conditions 4*, *Table 82: COMP characteristics*, *Table 90: I2C analog filter characteristics*, *Table 91: SPI characteristics*, *Table 92: Quad-SPI characteristics in SDR mode*, *Table 93: Quad-SPI characteristics in DDR mode* and *Table 94: SAI characteristics*.

表107. 文档修订历史 (continued)

Date	Revision	Changes
08-Oct-2018	3 (cont'd)	Updated *Figure 2: STM32WB55xx RF front-end block diagram*, *Figure 14: Power supply scheme (all packages except UFBGA129)*, *Figure 18: Typical energy detection (T = 27°C, VDD = 3.3 V)* and *Figure 25: I/O input characteristics*. Added *Figure 5: Power-up/down sequence*, *Figure 17: Typical link quality indicator code vs. Rx level* and *Figure 18: Typical energy detection (T = 27°C, VDD = 3.3 V)*. Added *Table 24: RF transmitter BLE characteristics (1 Mbps)*, *Table 25: RF transmitter BLE characteristics (2 Mbps)*, *Table 27: RF receiver BLE characteristics (2 Mbps)*, *Table 52: HSE crystal requirements* and *Table 89: Minimum I2CCLK frequency in all I2C modes*. Added *Device marking for UFQFPN48*. Removed former *Figure 22: I/O AC characteristics definition*(1) and *Figure 27: SMPS efficiency - VDDSMPS = 3.6 V*.
20-Feb-2019	4	Updated document title. Product status moved to Production data. Introduced BGA129 package, hence updated image on cover page, *Table 16: STM32WB55xx pin and ball definitions* and *Section 8: Ordering information*, and added *Figure 11: STM32WB55Vx UFBGA129 ballout*(1) and *Section 7.1: UFBGA129 package information*. Updated *Features*, *Section 3.3.4: Embedded SRAM*, *Section 3.17: Touch sensing controller (TSC)* and *Section 3.24: Low-power universal asynchronous receiver transmitter (LPUART)*. Added *Section 6.3.28: Clock recovery system (CRS)*. Added *Table 76: ADC sampling time*. Removed former *Table 75: Maximum ADC RAIN* and *Table 84: SMPS step-down converter characteristics*. Updated captions of figures *8*, *9* and *10*. Updated *Figure 43: VFQFPN68 recommended footprint*.

表107. 文档修订历史 (继续)

Date	Revision	Changes
20-Feb-2019	4 (cont'd)	Updated *Table 2: STM32WB55xx devices features and peripheral counts*, *Table 8: STM32WB55xx modes overview* and its footnotes, *Table 21: Main performance at VDD = 3.3 V*, *Table 22: General operating conditions*, *Table 23: RF transmitter BLE characteristics*, *Table 24: RF transmitter BLE characteristics (1 Mbps)*, *Table 25: RF transmitter BLE characteristics (2 Mbps)*, *Table 26: RF receiver BLE characteristics (1 Mbps)*, *Table 27: RF receiver BLE characteristics (2 Mbps)*, *Table 28: RF BLE power consumption for VDD = 3.3 V*, *Table 29: RF transmitter 802.15.4 characteristics*, *Table 31: RF 802.15.4 power consumption for VDD = 3.3 V*, *Table 35: Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF), VDD = 3.3 V*, *Table 36: Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, VDD = 3.3 V*, *Table 37: Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF), VDD= 3.3 V*, *Table 38: Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1, VDD = 3.3 V*, *Table 39: Current consumption in Sleep and Low-power sleep modes, Flash memory ON*, *Table 40: Current consumption in Low-power sleep modes, Flash memory in Power down*, *Table 41: Current consumption in Stop 2 mode*, *Table 42: Current consumption in Stop 1 mode*, *Table 43: Current consumption in Stop 0 mode*, *Table 44: Current consumption in Standby mode*, *Table 45: Current consumption in Shutdown mode*, *Table 46: Current consumption in VBAT mode*, *Table 47: Current under Reset condition*, *Table 48: Peripheral current consumption* and its footnotes, *Table 49: Low-power mode wakeup timings*, *Table 50: Regulator modes transition times* and its footnote *1*, *Table 65: EMS characteristics*, *Table 66: EMI characteristics*, *Table 67: ESD absolute maximum ratings*, *Table 69: I/O current injection susceptibility*, *Table 75: ADC characteristics*, *Table 77: ADC accuracy - Limited test conditions 1*, *Table 78: ADC accuracy - Limited test conditions 2*, *Table 79: ADC accuracy - Limited test conditions 3*, *Table 80: ADC accuracy - Limited test conditions 4* and *Table 104: Package thermal characteristics*.
04-Oct-2019	5	Updated *Features*, *Section 2: Description*, *Section 6.1.6: Power supply scheme*, *Section 6.2: Absolute maximum ratings* and *Section 7.2: WLCSP100 package information*. Updated *Table 6: Power supply typical components*, *Table 7: Features over all modes*, *Table 11: Temperature sensor calibration values*, *Table 16: STM32WB55xx pin and ball definitions*, *Table 17: Alternate functions*, *Table 21: Main performance at VDD = 3.3 V*, *Table 26: RF receiver BLE characteristics (1 Mbps)*, *Table 34: Embedded internal voltage reference*, *Table 62: PLL, PLLSAI1 characteristics* and *Table 67: ESD absolute maximum ratings*. Updated *Figure 6: Power supply overview* and *Figure 33: Quad-SPI timing diagram - DDR mode*. Added *Figure 15: Power supply scheme (UFBGA129 package)* and *Figure 21: Low-speed external clock source AC timing diagram*. Added *Table 56: Low-speed external user clock characteristics – Bypass mode*.

表107. 文档修订历史 (继续)

Date	Revision	Changes
19-Feb-2020	6	Updated *Features*, *Section 2: Description*, *I/O system current consumption*, *Section 3.17: Touch sensing controller (TSC)*, *Section 7.1: UFBGA129 package information*, *Section 7.2: WLCSP100 package information*, *Section 7.3: VFQFPN68 package information*, *Section 7.4: UFQFPN48 package information*, *Section 7.5: Thermal characteristics* and *Section 8: Ordering information*. Added *JTAG/SWD interface characteristics*, *Device marking for UFBGA129*, *Device marking for WLCSP100* and *Device marking for VFQFPN68*. Updated *Table 2: STM32WB55xx devices features and peripheral counts*, *Table 7: Features over all modes*, *Table 16: STM32WB55xx pin and ball definitions*, *Table 17: Alternate functions*, *Table 18: Voltage characteristics*, *Table 22: General operating conditions*, *Table 26: RF receiver BLE characteristics (1 Mbps)*, *Table 27: RF receiver BLE characteristics (2 Mbps)*, *Table 30: RF receiver 802.15.4 characteristics*, *Table 47: Current under Reset condition*, *Table 61: LSI2 oscillator characteristics* and *Table 104: Package thermal characteristics*. Added footnote *5* to *Table 15: Legend/abbreviations used in the pinout table*. Updated *Figure 2: STM32WB55xx RF front-end block diagram*, *Figure 6: Power supply overview*, *Figure 7: Clock tree*, *Figure 11: STM32WB55Vx UFBGA129 ballout(1)*, *Figure 14: Power supply scheme (all packages except UFBGA129)*, *Figure 36: UFBGA129 package outline* and *Figure 47: UFQFPN48 marking example (package top view)*.
10-Apr-2020	7	Updated *Section 3.6.5: Typical RF application schematic* and *Section 6.3.10: External clock source characteristics*. Updated *Table 16: STM32WB55xx pin and ball definitions* and *Table 54: HSE crystal requirements*. Updated *Figure 11: STM32WB55Vx UFBGA129 ballout(1)* and *Figure 14: Power supply scheme (all packages except UFBGA129)*. Minor text edits across the whole document.
17-Jun-2020	8	Introduced STM32WB55VY. Updated *Section 3.3.4: Embedded SRAM*, *Section 3.4: Security and safety*, *Section 3.14: Analog to digital converter (ADC)*, *Section 6.3.10: External clock source characteristics* and *Section 8: Ordering information*. Updated *Table 1: Device summary*, *Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts*, *Table 26: RF transmitter BLE characteristics (1 Mbps)*, *Table 27: RF transmitter BLE characteristics (2 Mbps)*, *Table 65: Flash memory characteristics* and *Table 77: ADC characteristics*. Updated *Figure 10: STM32WB55Cx and STM32WB35Cx UFQFPN48 pinout(1)(2)*, *Figure 11: STM32WB55Rx VFQFPN68 pinout(1)(2)* and *Figure 17: Power supply scheme (UFBGA129 and WLCSP100 packages)*. Updated footnote *5* of *Table 15: Legend/abbreviations used in the pinout table* and footnote *8* of *Table 16: STM32WB55xx pin and ball definitions*. Added footnote *3* to *Table 16*, footnote *2* to *Figure 16*, footnote *1* to *Table 86* and footnotes to tables *23*, *30* and *33*. Added *Table 55: HSE clock source requirements*.

表107. 文档修订历史 (继续)

Date	Revision	Changes
02-Jul-2020	9	Added STM32WB35xx devices. Updated *Section 2: Description*, *Section 3.3.4: Embedded SRAM* and *Section 8: Ordering information*. Updated *Table 1: Device summary*, *Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts*, *Table 7: Features over all modes* and *Table 106: Package thermal characteristics*. Added *Table 17: STM32WB35xx pin and ball definitions* and *Table 19: Alternate functions (STM32WB35xx)*. Added *Figure 2: STM32WB35xx block diagram*, *Figure 8: STM32WB35xx - Power supply overview* and *Figure 50: STM32WB35xx UFQFPN48 marking example (package top view)*, Updated *Figure 1: STM32WB55xx block diagram*, *Figure 4: External components for the RF part*, *Figure 16: Power supply scheme (all packages except UFBGA129 and WLCSP100)*, *Figure 17: Power supply scheme (UFBGA129 and WLCSP100 packages)* and added footnote to *Figure 9: Clock tree*. Added footnote *1* to *Table 8: STM32WB55xx and STM32WB35xx modes overview*.
23-Nov-2020	10	Updated *Features*, *Section 3.15: Voltage reference buffer (VREFBUF)* and *Section 3.28.2: Embedded Trace Macrocell™*. Updated *Table 9: STM32WB55xx and STM32WB35xx CPU1 peripherals interconnect matrix*, *Table 17: STM32WB35xx pin and ball definitions*, *Table 26: RF transmitter BLE characteristics (1 Mbps)*, *Table 27: RF transmitter BLE characteristics (2 Mbps)*, *Table 31: RF transmitter 802.15.4 characteristics*, *Table 50: Peripheral current consumption*, *Table 54: HSE crystal requirements*, *Table 55: HSE clock source requirements*, footnote *2* of *Table 57: Low-speed external user clock characteristics* and *Table 86: V_{BAT} monitoring characteristics*. Added footnote *2* to *Table 24*, footnote *2* to *Table 26* and footnote *2* to *Table 27*. Updated *Figure 9: Clock tree* and *Figure 13: STM32WB55Vx UFBGA129 ballout*[(1)]. Minor text edits across the whole document.
07-Apr-2021	11	Updated document title, *Features*, *Section 1: Introduction*, *Section 2: Description*, *Section 3.3.4: Embedded SRAM*, *Section 3.6: RF subsystem*, *Section 3.6.2: BLE general description* and *Section 6.1.2: Typical values*, *Section 6.3.10: External clock source characteristics*. Updated *Table 2: STM32WB55xx and STM32WB35xx devices features and peripheral counts*, *Table 16: STM32WB55xx pin and ball definitions*, *Table 17: STM32WB35xx pin and ball definitions*, *Table 18: Alternate functions (STM32WB55xx)*, *Table 19: Alternate functions (STM32WB35xx)*, *Table 23: Main performance at VDD = 3.3 V*, *Table 50: Peripheral current consumption*, *Table 53: Wakeup time using USART/LPUART* and *Table 55: HSE clock source requirements*. Updated *Figure 3: STM32WB55xx and STM32WB35xx RF front-end block diagram*, *Figure 9: Clock tree*, *Figure 16: Power supply scheme (all packages except UFBGA129 and WLCSP100)*, *Figure 17: Power supply scheme (UFBGA129 and WLCSP100 packages)* and *Figure 29: ADC accuracy characteristics*. Removed former footnote *3* from *Table 83: VREFBUF characteristics*.

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