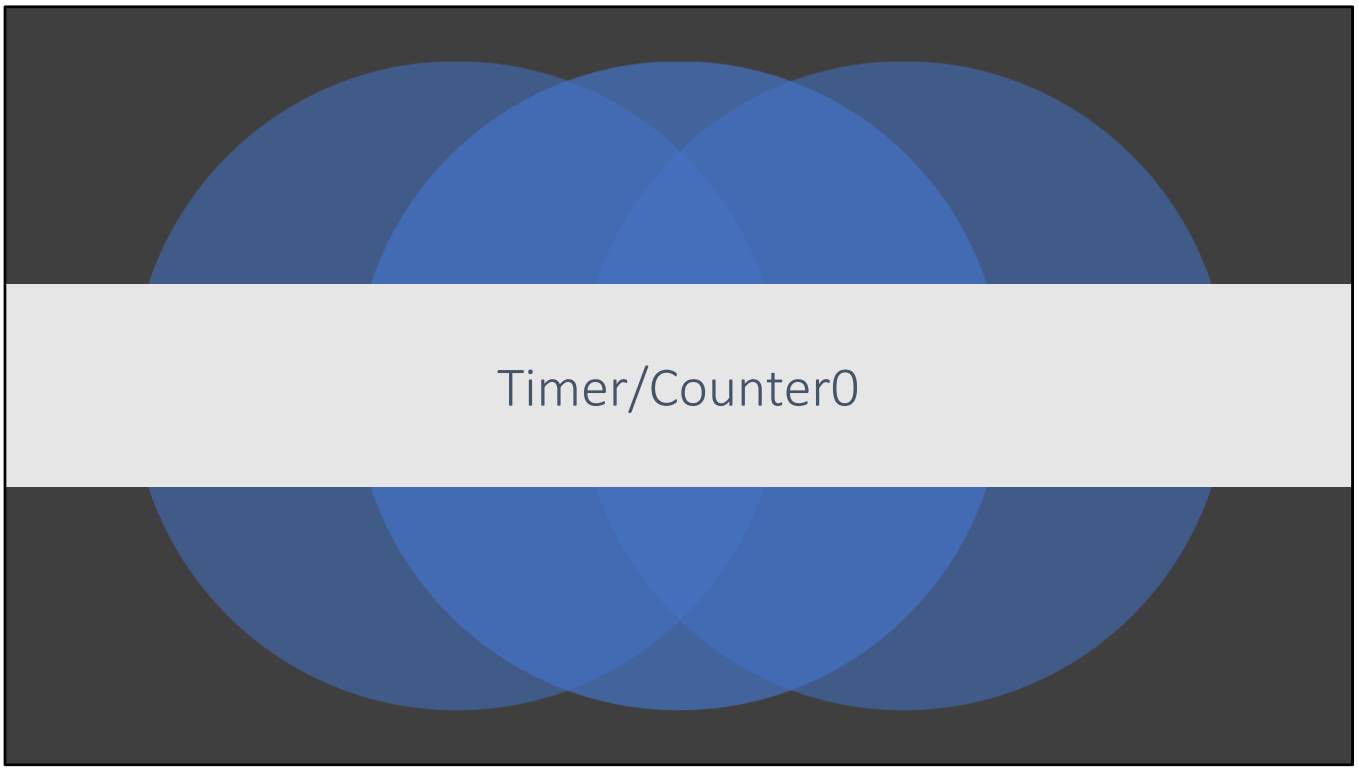
AT90CAN128
ATmega128
Timer-ek

Borsos Döníz


Timer/Counter0

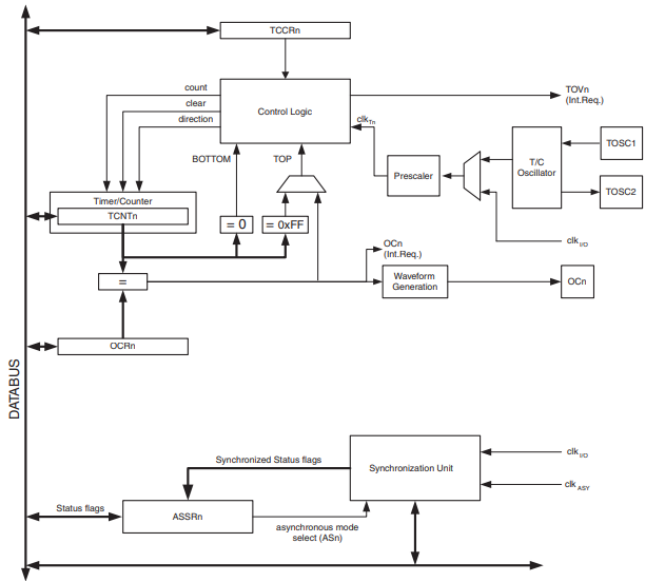
Timer0

- ATmega128 adatlap
  - 92. oldaltól
- AT90CAN adatlap
  - 99. oldaltól

Jellemzők

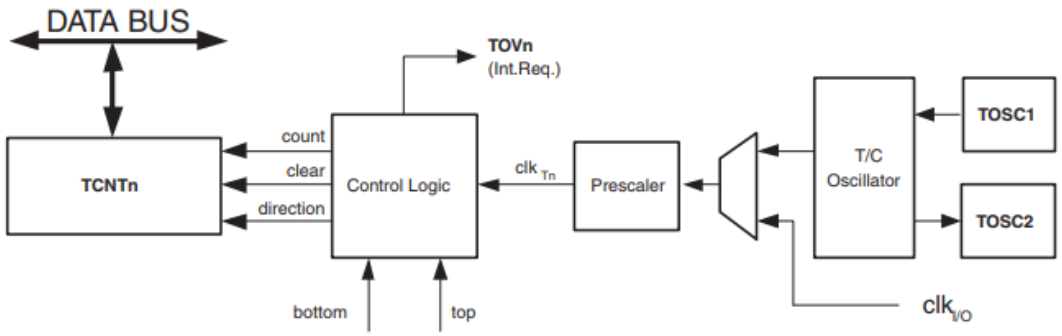
- 8 bit
- Single Channel Counter
- Clear Timer on Compare Match (Auto Reload)
- Glitch-free, Phase Correct Pulse Width Modulator (PWM)
- Frequency Generator
- 10-bit Clock Prescaler
- Overflow and Compare Match Interrupt Sources (TOV0 and OCF0)
- Allows Clocking from External 32kHz Watch Crystal Independent of the I/O Clock (ATmega128)
- External Event Counter (AT90CAN128)

Figure 34. 8-bit Timer/Counter Block Diagram



ATmega128 adatlap 92. oldal
TCCR0: Timer/Counter0 Control Register
TOV0: Timer/Counter Overflow Flag
T/C oscillator: Timer/Counter
TOSC: Timer/Counter Oscillator pins
TCNT: Timer/Counter Register
OCn: Output Compare pin
OCRn: Output Compare Register
ASSR: Asynchronous Status Register

Számláló egység



ATmega128 adatlap 93. oldal

Count: inkrement, dekrement
Direction: ezt választja ki
Clear: TCNT nullázása
Top: max. érték
Bottom: min. érték - 0

Table 56. Clock Select Bit Description

CS02	CS01	CS00	Description
0	0	0	No clock source (Timer/Counter stopped)
0	0	1	clk_{T0S}/(No prescaling)
0	1	0	clk_{T0S}/8 (From prescaler)
0	1	1	clk_{T0S}/32 (From prescaler)
1	0	0	clk_{T0S}/64 (From prescaler)
1	0	1	clk_{T0S}/128 (From prescaler)
1	1	0	clk_{T0S}/256 (From prescaler)
1	1	1	clk_{T0S}/1024 (From prescaler)

ATmega128

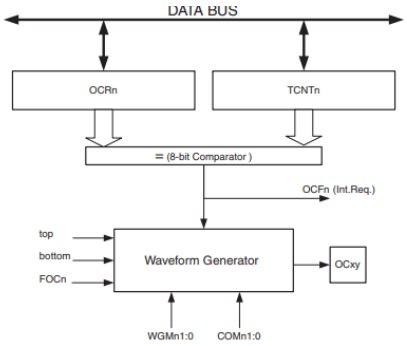
AT90CAN128

CS02	CS01	CS00	Description
0	0	0	No clock source (Timer/Counter stopped)
0	0	1	$clk_{I/O}$/(No prescaling)
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
1	0	0	$clk_{I/O}$/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

ATmega128 adatlap 105. oldal
AT90CAN128 adatlap 111. oldal

Output Compare Unit

- 8bites komparátor
  - Folyamatos összehasonlítás (TCNT0, OCR0)
  - Ha TCNT0=OCR0, akkor OCF0 flag a következő órajelciklusban 1 lesz
  - Megszakítás engedélyesés esetén (OCIE0) - törlődik



ATmega128 94-95. oldal

Normál mód

- Legegyszerűbb működési mód
- Mindig felfele számlál (increment)
- Nem törlődik a számláló
- Túlcsordul, ha eléri a TOP értéket (8bit – 0xFF)
- Újraindul a BOTTOM értékről (0x00)
- A TOV0 flag akkor lesz 1, amikor a TCNT0 nullává válik

ATmega128 adatlap 97. oldal

Table 52. Waveform Generation Mode Bit Description

Mode	WGM01[1] (CTC0)	WGM00[1] (PWM0)	Timer/Counter Mode of Operation	TOP	Update of OCR0 at	TOV0 Flag Set on
0	0	0	Normal	0xFF	Immediate	MAX
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	1	0	CTC	OCR0	Immediate	MAX
3	1	1	Fast PWM	0xFF	BOTTOM	MAX

ATmega128 adatlap 104. oldal

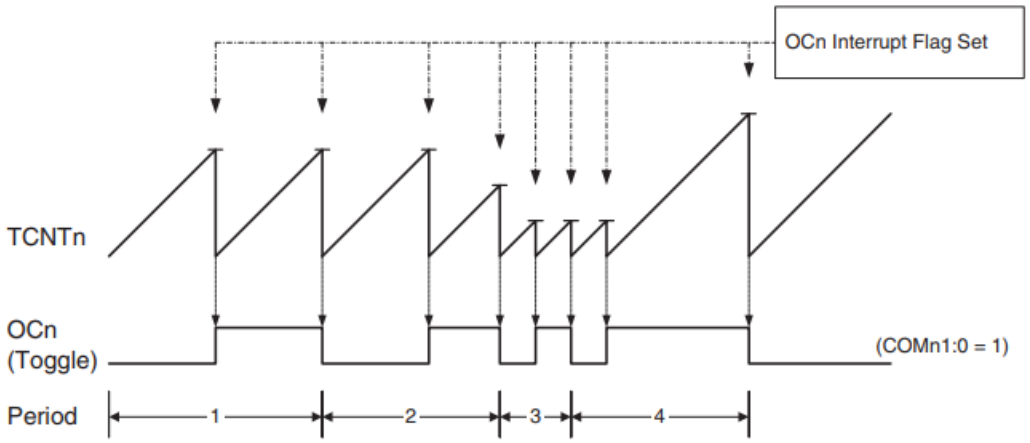
CTC mód: Clear Timer on Compare

- A számláló felbontásának kezelésére szolgál
- Ha a TCNT0 eléri az OCR0 értékét, akkor a számláló nullára vált
- OCR0 a számláló legmagasabb értéke
- Megszakítás generálódik, ha a számláló eléri a TOP értéket

$$f_{OCn} = \frac{f_{clk\_I/O}}{2 \cdot N \cdot (1 + OCRn)}$$

$N = 1, 8, 32, 64, 128, 256, \text{or } 1024$

ATmega128 adatlap 97. oldal



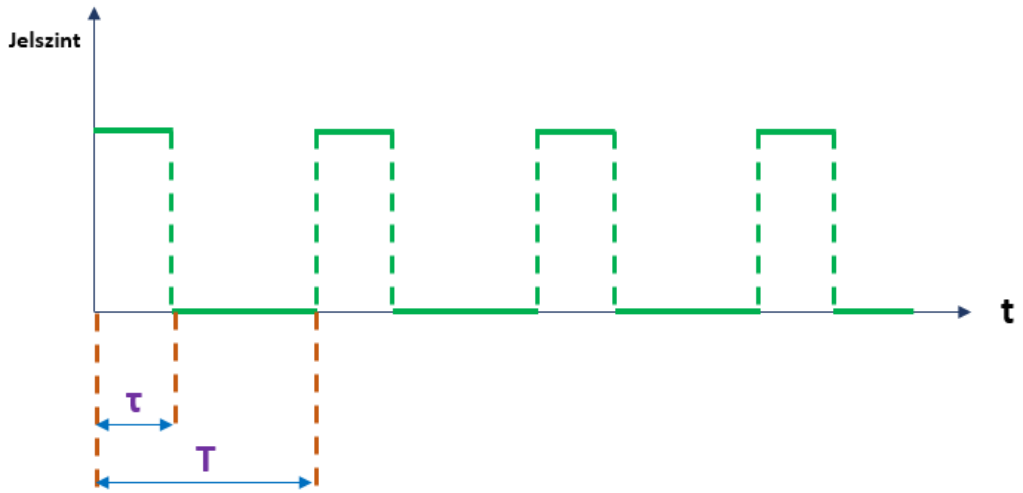
ATmega128 adatlap 97. oldal

Table 52. Waveform Generation Mode Bit Description

Mode	WGM01[1] (CTC0)	WGM00[1] (PWM0)	Timer/Counter Mode of Operation	TOP	Update of OCR0 at	TOV0 Flag Set on
0	0	0	Normal	0xFF	Immediate	MAX
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	1	0	CTC	OCR0	Immediate	MAX
3	1	1	Fast PWM	0xFF	BOTTOM	MAX

ATmega128 adatlap 104. oldal

PWM



Fast PWM mód

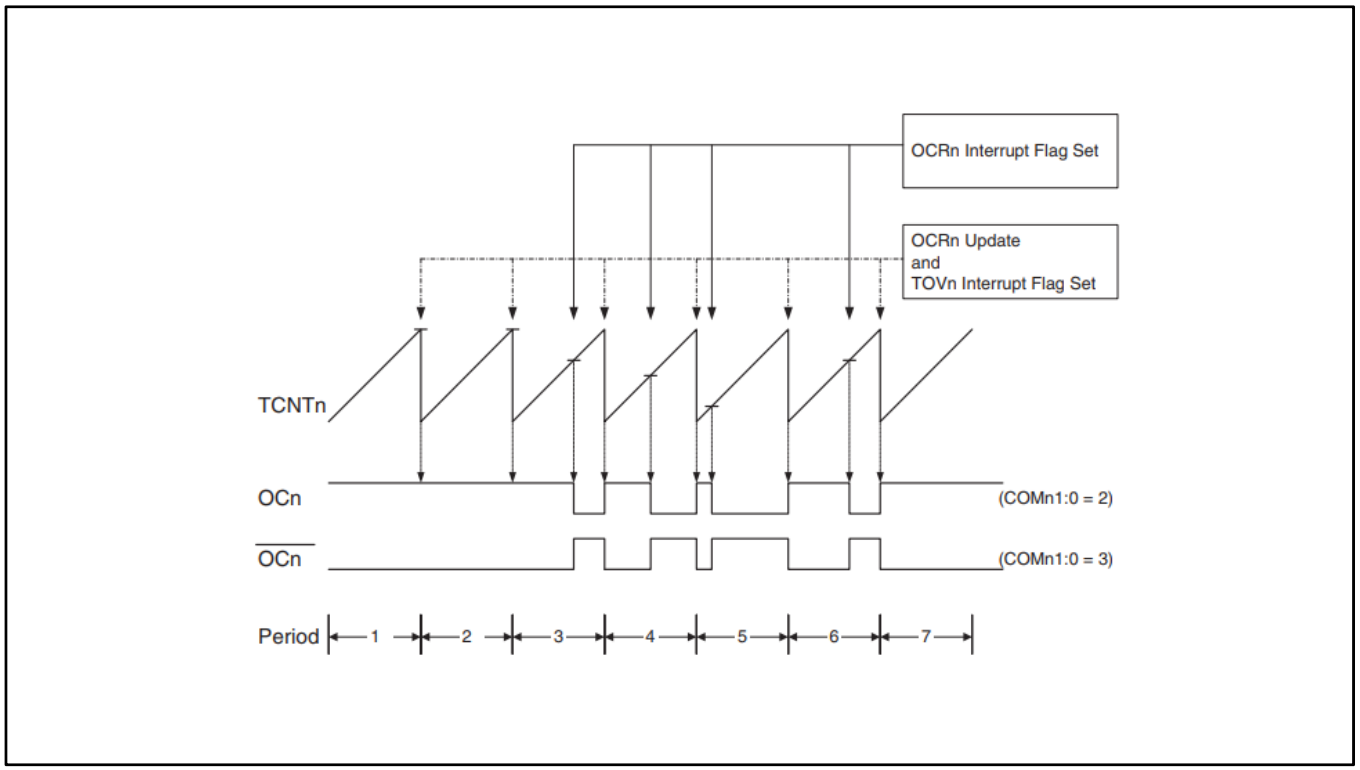
- Egymeredekségű működés
- Számláló a BOTTOM értéktől a MAX értékig számol, majd újraindul
- Kétszeres frekvencia a Phase Correct PWM módhoz képest
- Invertáló és nem invertáló mód

$$f_{OCnPWM} = \frac{f_{clk\_I/O}}{N \cdot 256}$$

Table 52. Waveform Generation Mode Bit Description

Mode	WGM01[1] (CTC0)	WGM00[1] (PWM0)	Timer/Counter Mode of Operation	TOP	Update of OCR0 at	TOV0 Flag Set on
0	0	0	Normal	0xFF	Immediate	MAX
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	1	0	CTC	OCR0	Immediate	MAX
3	1	1	Fast PWM	0xFF	BOTTOM	MAX

ATmega128 adatlap 104. oldal



ATmega128 adatlap 99. oldal

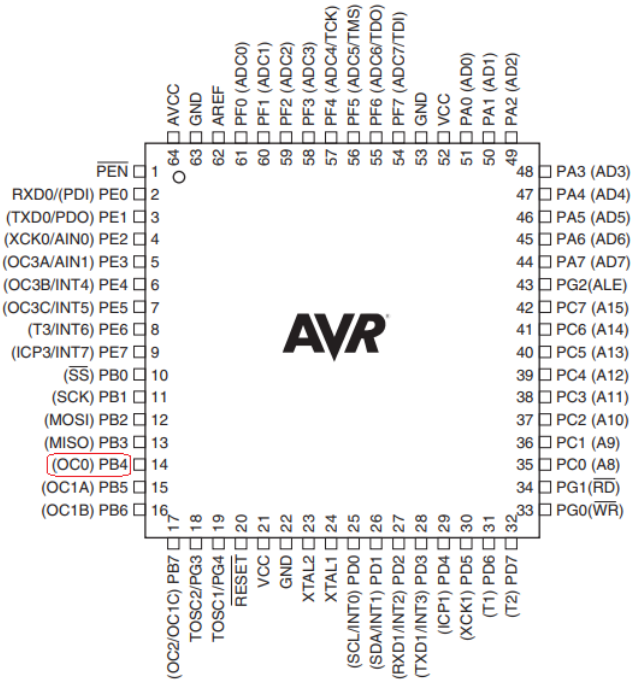


Table 54. Compare Output Mode, Fast PWM Mode[1]

COM01	COM00	Description
0	0	Normal port operation, OC0 disconnected.
0	1	Reserved
1	0	Clear OC0 on compare match, set OC0 at BOTTOM, (non-inverting mode)
1	1	Set OC0 on compare match, clear OC0 at BOTTOM, (inverting mode)

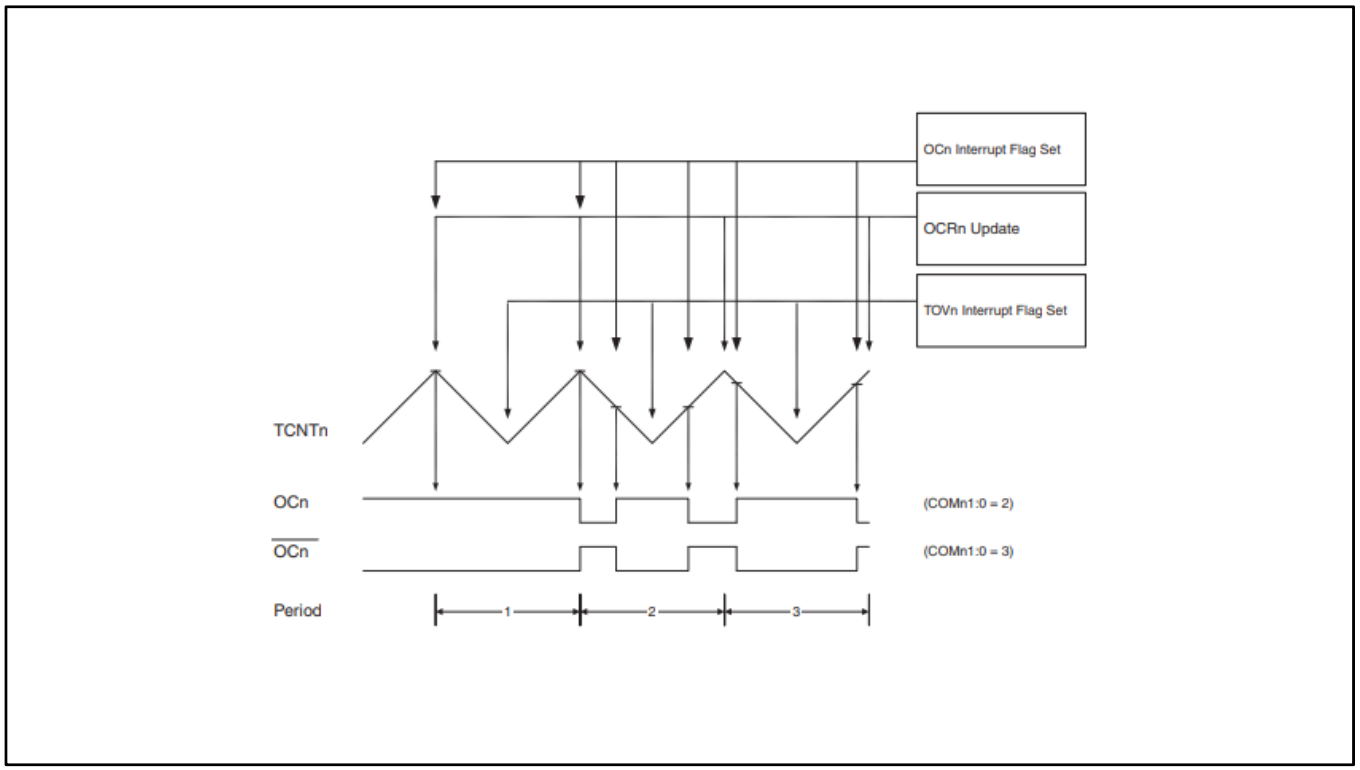
ATmega128 adatlap 2. oldal, 104. oldal

Phase Correct PWM mód

- Kettős meredekségű működés
- A számláló a BOTTOM értéktől számol a MAX értékig, majd vissza a BOTTOM-ig
- Invertáló és nem invertáló mód

$$f_{OCnPCPWM} = \frac{f_{clk\_I/O}}{N \cdot 510}$$

ATmega128 adatlap 100. oldal



ATmega128 adatlap 100. oldal

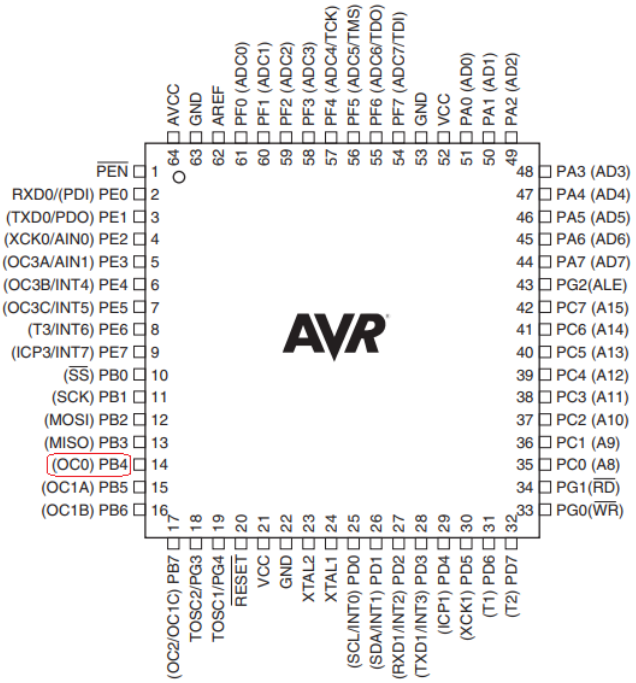


Table 55. Compare Output Mode, Phase Correct PWM Mode[1]

COM01	COM00	Description
0	0	Normal port operation, OC0 disconnected.
0	1	Reserved
1	0	Clear OC0 on compare match when up-counting. Set OC0 on compare match when downcounting.
1	1	Set OC0 on compare match when up-counting. Clear OC0 on compare match when downcounting.

ATmega128 adatlap 2. oldal, 104. oldal

Megszakítások

- OCIE0: Timer/Counter0 Output Compare Match Interrupt
- TOIE0: Timer/Counter0 Overflow Interrupt

Regiszterek

Timer/Counter Control Register – TCCR0

Bit	7	6	5	4	3	2	1	0	
	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	TCCR0
Read/Write	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Timer/Counter Register – TCNT0

Bit	7	6	5	4	3	2	1	0	
	TCNT0[7:0]								TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Output Compare Register – OCR0

Bit	7	6	5	4	3	2	1	0	
	OCR0[7:0]								OCR0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Timer/Counter Interrupt Mask Register – TIMSK

Bit	7	6	5	4	3	2	1	0	
	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0	TIMSK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Timer/Counter Interrupt Flag Register – TIFR

Bit	7	6	5	4	3	2	1	0	
	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0	TIFR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	


TIMER/Counter 1/3

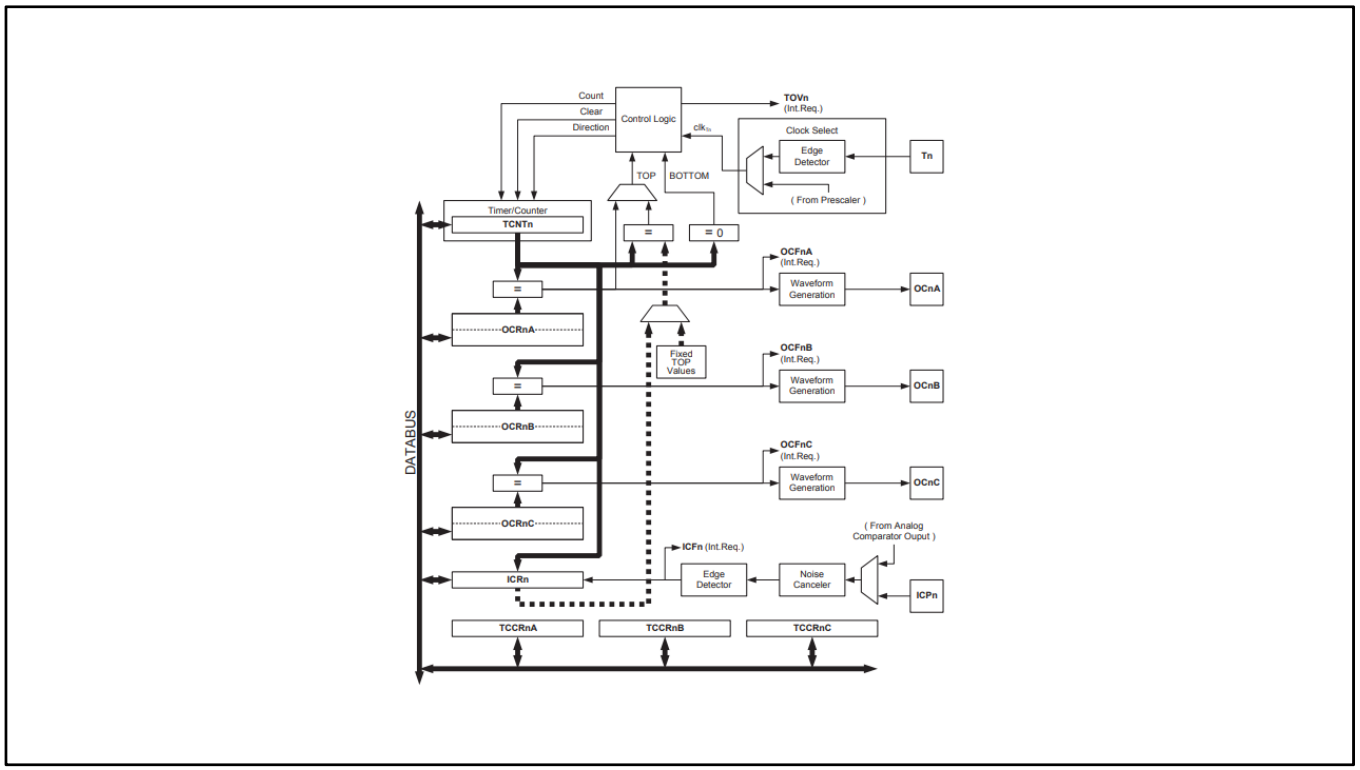
Timer1/3

- ATmega128
  - Adatlap 111. oldal
- AT90CAN128
  - Adatlap 113. oldal

16bites Timer/Counter jellemzők

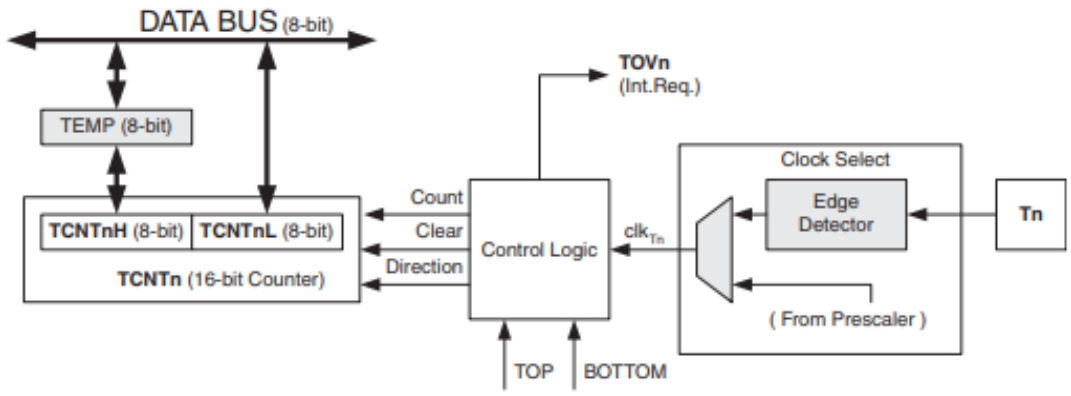
- True 16-bit Design (i.e.,Allows 16-bit PWM)
- Three Independent Output Compare Units
- Double Buffered Output Compare Registers
- One Input Capture Unit
- Input Capture Noise Canceler
- Clear Timer on Compare Match (Auto Reload)
- Glitch-free, Phase Correct Pulse width Modulator (PWM)
- Variable PWM Period
- Frequency Generator
- External Event Counter
- Ten Independent Interrupt Sources (TOV1, OCF1A, OCF1B, OCF1C, ICF1, TOV3, OCF3A, OCF3B, OCF3C, and ICF3)

ATmega128 adatlap 111. oldal



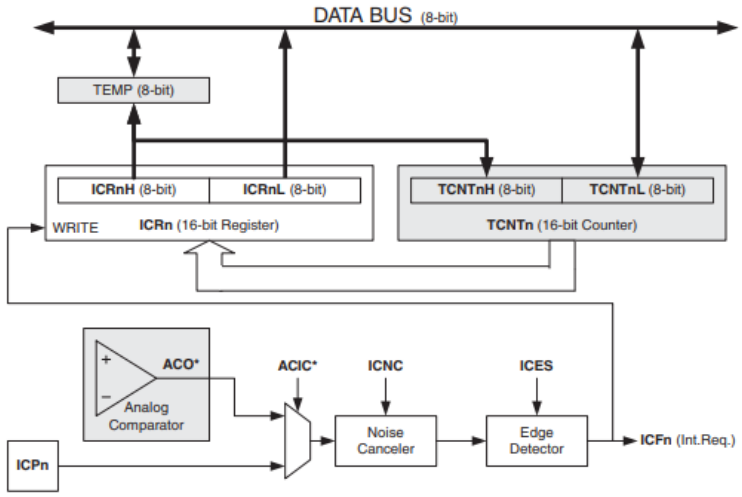
ATmega128 adatlap 114. oldal

Számláló egység

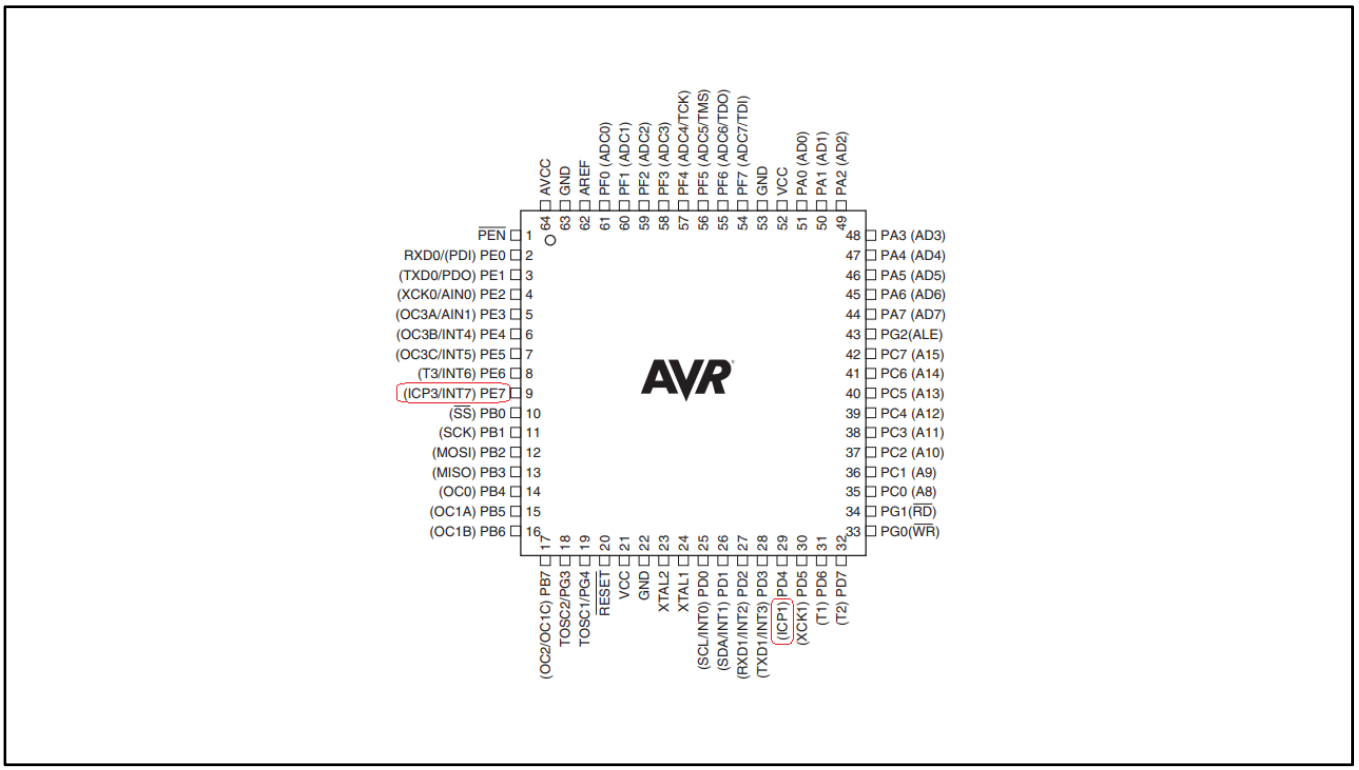


ATmega128 adatlap 117. oldal

Input Capture Unit

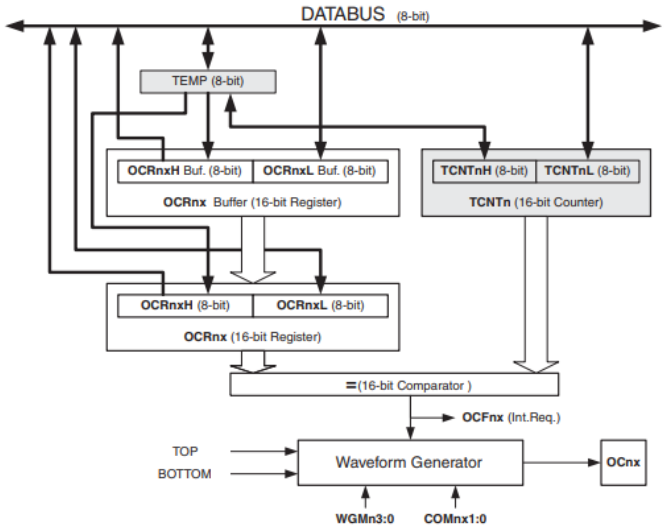


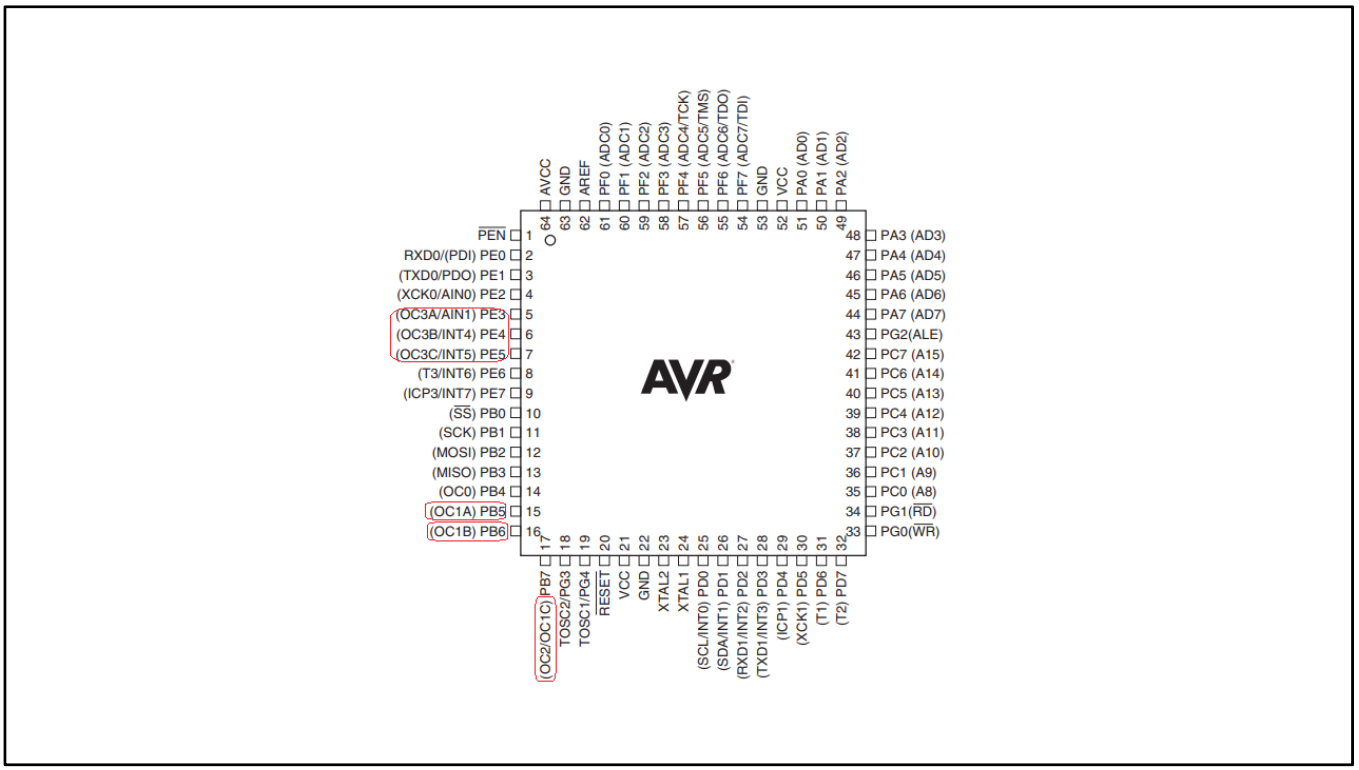
Atmega128 adatlap 118. oldal
ACO: Analog Comparator Output (ACO)
Csak a Timer1-nél az ACO
Külső események az ICPn-en Input Capture Pin (alternatív funkció)
Szintváltáskor – él detektálása
ICRn-be kerül a számláló aktuális értéke
Zajszűrő: egyszerű digitális szűrő


AVCC 64
GND 63
AREF 62
PF0 (ADC0) 61
PF1 (ADC1) 60
PF2 (ADC2) 59
PF3 (ADC3) 58
PF4 (ADC4/TCK) 57
PF5 (ADC5/TMS) 56
PF6 (ADC6/TDO) 55
PF7 (ADC7/TDI) 54
GND 53
VCC 52
PA0 (AD0) 51
PA1 (AD1) 50
PA2 (AD2) 49
PEN 1
RXD0/(PDI) PE0 2
(TXD0/PDO) PE1 3
(XCK0/AIN0) PE2 4
(OC3A/AIN1) PE3 5
(OC3B/INT4) PE4 6
(OC3C/INT5) PE5 7
(T3/INT6) PE6 8
(ICP3/INT7) PE7 9
(SS) PB0 10
(SCK) PB1 11
(MOSI) PB2 12
(MISO) PB3 13
(OC0) PB4 14
(OC1A) PB5 15
(OC1B) PB6 16
48 PA3 (AD3)
47 PA4 (AD4)
46 PA5 (AD5)
45 PA6 (AD6)
44 PA7 (AD7)
43 PG2(ALE)
42 PC7 (A15)
41 PC6 (A14)
40 PC5 (A13)
39 PC4 (A12)
38 PC3 (A11)
37 PC2 (A10)
36 PC1 (A9)
35 PC0 (A8)
34 PG1(RD)
33 PG0(WR)
(OC2/OC1C) PB7 17
TOSC2/PG3 18
TOSC1/PG4 19
RESET 20
VCC 21
GND 22
XTAL2 23
XTAL1 24
(SCL/INT0) PD0 25
(SDA/INT1) PD1 26
(RXD1/INT2) PD2 27
(TXD1/INT3) PD3 28
(ICP1) PD4 29
(XCK1) PD5 30
(T1) PD6 31
(T2) PD7 32

2. oldal

Output Compare Unit




AVCC 64
GND 63
AREF 62
PF0 (ADC0) 61
PF1 (ADC1) 60
PF2 (ADC2) 59
PF3 (ADC3) 58
PF4 (ADC4/TCK) 57
PF5 (ADC5/TMS) 56
PF6 (ADC6/TDO) 55
PF7 (ADC7/TDI) 54
GND 53
VCC 52
PA0 (AD0) 51
PA1 (AD1) 50
PA2 (AD2) 49
PEN 1
RXD0/(PDI) PE0 2
(TXD0/PDO) PE1 3
(XCK0/AIN0) PE2 4
(OC3A/AIN1) PE3 5
(OC3B/INT4) PE4 6
(OC3C/INT5) PE5 7
(T3/INT6) PE6 8
(ICP3/INT7) PE7 9
(SS) PB0 10
(SCK) PB1 11
(MOSI) PB2 12
(MISO) PB3 13
(OC0) PB4 14
(OC1A) PB5 15
(OC1B) PB6 16
48 PA3 (AD3)
47 PA4 (AD4)
46 PA5 (AD5)
45 PA6 (AD6)
44 PA7 (AD7)
43 PG2(ALE)
42 PC7 (A15)
41 PC6 (A14)
40 PC5 (A13)
39 PC4 (A12)
38 PC3 (A11)
37 PC2 (A10)
36 PC1 (A9)
35 PC0 (A8)
34 PG1(RD)
33 PG0(WR)
17 (OC2/OC1C) PB7
18 TOSC2/PG3
19 TOSC1/PG4
20 RESET
21 VCC
22 GND
23 XTAL2
24 XTAL1
25 (SCL/INT0) PD0
26 (SDA/INT1) PD1
27 (RXD1/INT2) PD2
28 (TXD1/INT3) PD3
29 (ICP1) PD4
30 (XCK1) PD5
31 (T1) PD6
32 (T2) PD7

2. oldal

Működési módok

- Normál
- CTC
  - OCRnA
  - ICRn
- Fast PWM és Phase Correct PWM mód
  - OCRnA
  - ICRn
  - 8, 9 ,10 bit
- Phase and Frequency Correct PWM mód

Phase and Frequency Correct PWM mód

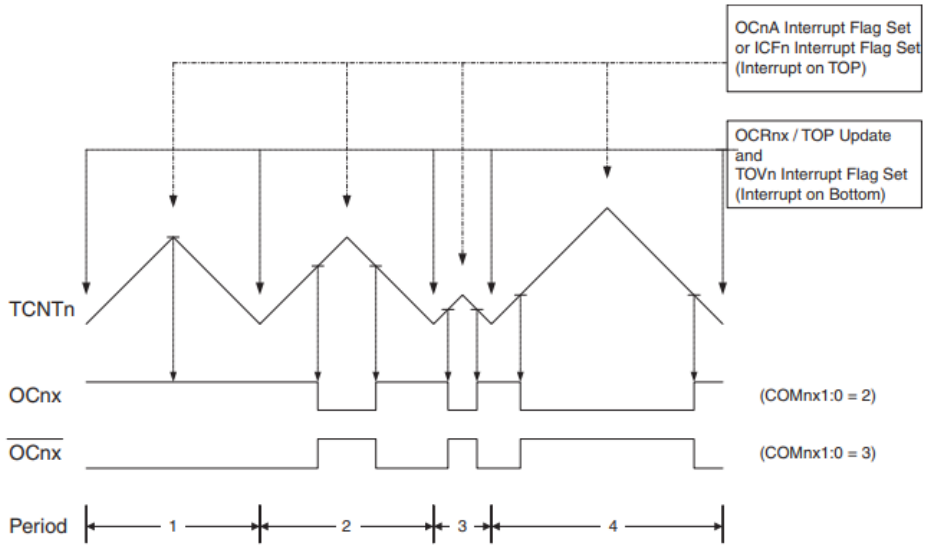
- Nagy felbontás
- Kettős meredekség
- Max érték
  - OCRnA
  - ICRn

$$f_{OCnxPFCPWM} = \frac{f_{clk\_I/O}}{2 \cdot N \cdot TOP}$$

1, 8, 64, 256, or 1024

ATmega128 adatlap 128. oldal

Figure 54. Phase and Frequency Correct PWM Mode, Timing Diagram



ATmega128 adatlap 129. oldal

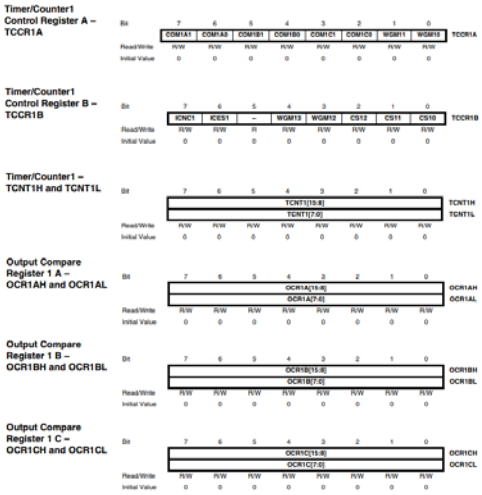
Mode	WGMn3	WGMn2 (CTCn)	WGMn1 (PWMn1)	WGMn0 (PWMn0)	Timer/Counter Mode of Operation[1]	TOP	Update of OCRnx at	TOVn Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCRnA	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	BOTTOM	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	BOTTOM	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICRn	BOTTOM	BOTTOM
9	1	0	0	1	PWM, Phase and Frequency Correct	OCRnA	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICRn	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCRnA	TOP	BOTTOM
12	1	1	0	0	CTC	ICRn	Immediate	MAX
13	1	1	0	1	(Reserved)	–	–	–
14	1	1	1	0	Fast PWM	ICRn	BOTTOM	TOP
15	1	1	1	1	Fast PWM	OCRnA	BOTTOM	TOP

ATmega128 adatlap 124. oldal

Megszakítások

- Timer1 [TIMSK]
  - TICIE1 (IC)
  - OCIE1A (OCA)
  - OCIE1B (OCB)
  - TOIE1 (OVF)
- Timer3 [ETIMSK]
  - TICIE3
  - OCIE3A
  - OCIE3B
  - TOIE3
  - OCIE3C
  - OCIE1C

Regiszterek



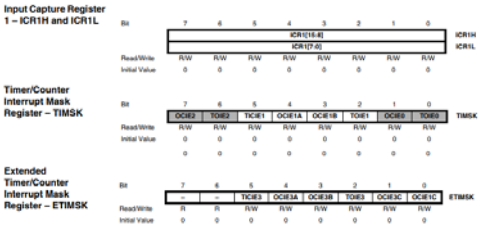


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Table 58. Compare Output Mode, non-PWM

COMnA1/COMnB1/ COMnC1	COMnA0/COMnB0/ COMnC0	Description
0	0	Normal port operation, OCnA/OCnB/OCnC disconnected.
0	1	Toggle OCnA/OCnB/OCnC on compare match.
1	0	Clear OCnA/OCnB/OCnC on compare match (set output to low level).
1	1	Set OCnA/OCnB/OCnC on compare match (set output to high level).

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Table 59. Compare Output Mode, Fast PWM

COMnA1/COMnB1/ COMnC1	COMnA0/COMnB0/ COMnC0	Description
0	0	Normal port operation, OCnA/OCnB/OCnC disconnected.
0	1	WGMn3:0 = 15: Toggle OCnA on Compare Match, OCnB/OCnC disconnected (normal port operation). For all other WGMn settings, normal port operation, OCnA/OCnB/OCnC disconnected.
1	0	Clear OCnA/OCnB/OCnC on compare match, set OCnA/OCnB/OCnC at BOTTOM, (non-inverting mode)
1	1	Set OCnA/OCnB/OCnC on compare match, clear OCnA/OCnB/OCnC at BOTTOM, (inverting mode)

Table 60. Compare Output Mode, Phase Correct and Phase and Frequency Correct PWM

COMnA1/COMnB1/ COMnC1	COMnA0/COMnB0/ COMnC0	Description
0	0	Normal port operation, OCnA/OCnB/OCnC disconnected.
0	1	WGMn3:0 = 9 or 11: Toggle OCnA on Compare Match, OCnB/OCnC disconnected (normal port operation). For all other WGMn settings, normal port operation, OCnA/OCnB/OCnC disconnected.
1	0	Clear OCnA/OCnB/OCnC on compare match when up-counting. Set OCnA/OCnB/OCnC on compare match when downcounting.
1	1	Set OCnA/OCnB/OCnC on compare match when up-counting. Clear OCnA/OCnB/OCnC on compare match when downcounting.