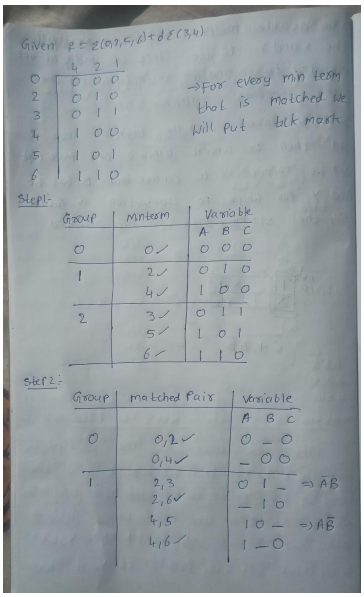
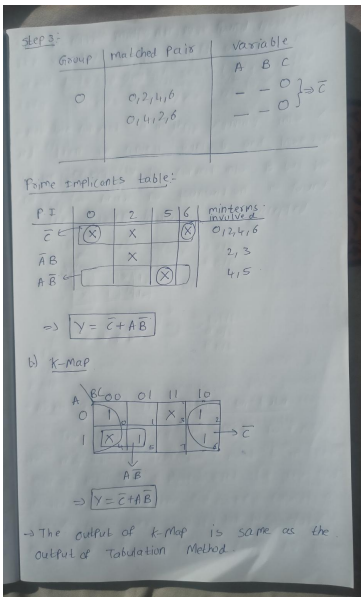
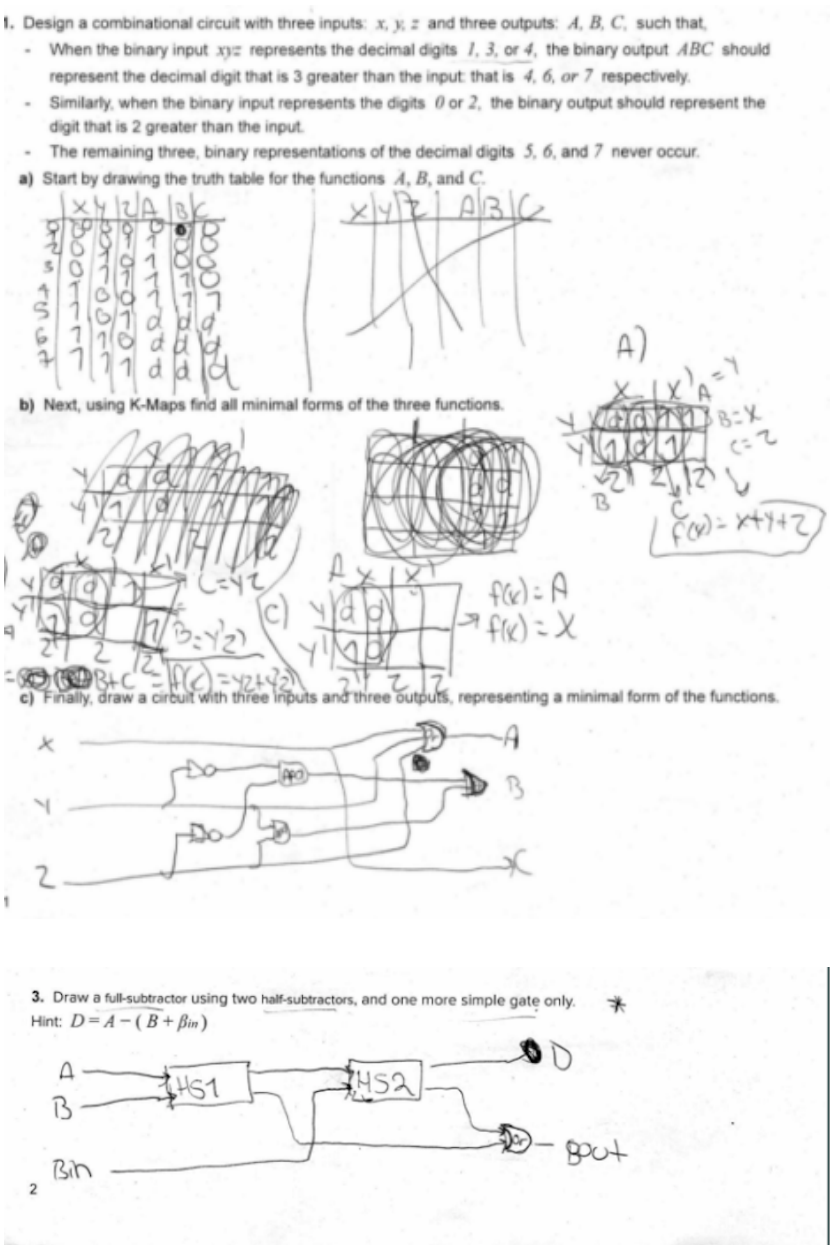
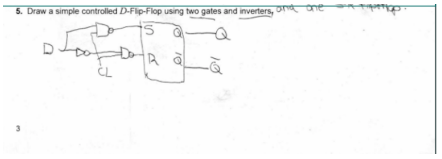
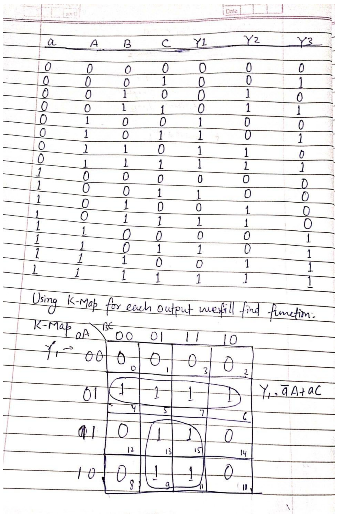

Given F = Σ(0,2,3,4,5,6) + dΣ(3,4)
→For every min term that is matched we will put tick mark
Step1:-
Group
Minterm
Variable
A B C
Step2:-
Group
matched Pair
Variable
A B C
⇒ $\bar{A}B$
⇒ $A\bar{B}$


Step 3:-
Group
Matched Pair
Variable
A B C
⇒ $\bar{C}$
Prime Implicants table:-
PI
minterms involved
$\bar{C}$
$\bar{A}B$
$A\bar{B}$
⇒ $Y = \bar{C} + A\bar{B}$
b) K-Map
⇒ $Y = \bar{C} + A\bar{B}$
→ The output of k-map is same as the output of Tabulation Method.


1. Design a combinational circuit with three inputs: x, y, z and three outputs: A, B, C, such that,
- When the binary input xyz represents the decimal digits 1, 3, or 4, the binary output ABC should represent the decimal digit that is 3 greater than the input: that is 4, 6, or 7 respectively.
- Similarly, when the binary input represents the digits 0 or 2, the binary output should represent the digit that is 2 greater than the input.
- The remaining three, binary representations of the decimal digits 5, 6, and 7 never occur.
a) Start by drawing the truth table for the functions A, B, and C.
b) Next, using K-Maps find all minimal forms of the three functions.
A)
B=X
C=Z
f(x) = X+Y+Z
c) Finally, draw a circuit with three inputs and three outputs, representing a minimal form of the functions.
f(x) = A
f(x) = X
X
Y
Z
A
B
C
1

3. Draw a full-subtractor using two half-subtractors, and one more simple gate only.
Hint: $D = A - (B + \beta_{in})$
A
B
Bin
HS1
HS2
D
Bout
2


5. Draw a simple controlled D-Flip-Flop using two gates and inverters.
D
CL
S
R
Q
$\bar{Q}$
3



a	A	B	C	Y1	Y2	Y3
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	1	0	0
0	1	0	1	1	0	1
0	1	1	0	1	1	0
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	1	1	0
1	1	0	0	0	0	1
1	1	0	1	1	0	1
1	1	1	0	0	1	1
1	1	1	1	1	1	1

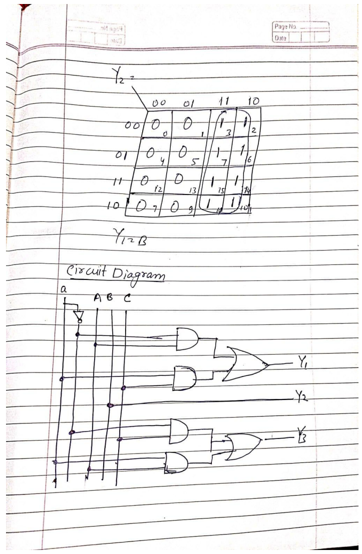
Using K-Map for each output we will find function.

K-Map

$Y_1 \to$

aA \ BC	00	01	11	10
00	0 (0)	0 (1)	0 (3)	0 (2)
01	1 (4)	1 (5)	1 (7)	1 (6)
11	0 (12)	1 (13)	1 (15)	0 (14)
10	0 (8)	1 (9)	1 (11)	0 (10)

$Y_1 = \bar{a}A + aC$

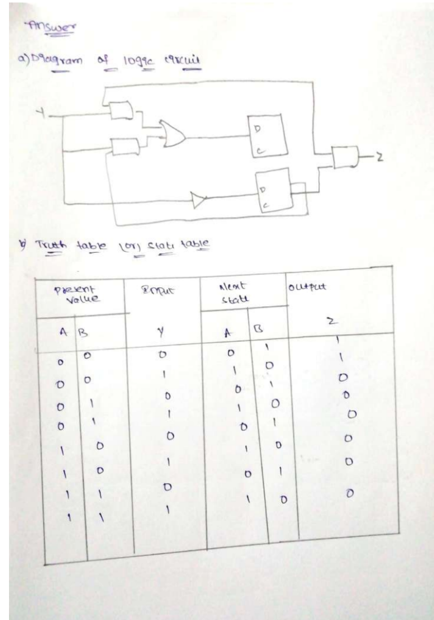


$Y_2 =$

	00	01	11	10
00	0 (0)	0 (1)	1 (3)	1 (2)
01	0 (4)	0 (5)	1 (7)	1 (6)
11	0 (12)	0 (13)	1 (15)	1 (14)
10	0 (7)	0 (9)	1 (11)	1 (10)

$Y_1 = B$

Circuit Diagram



Answer

a) Diagram of logic circuit

b) Truth table (or) State table

Present Value		Input	Next State		Output
A	B	Y	A	B	Z
0	0	0	0	1	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	0	1	0
1	1	1	1	0	0