Direct Digital Synthesis

This design is a waveform generator with Sine, Cosine and Square outputs that employs Direct Digital Synthesis techniques.

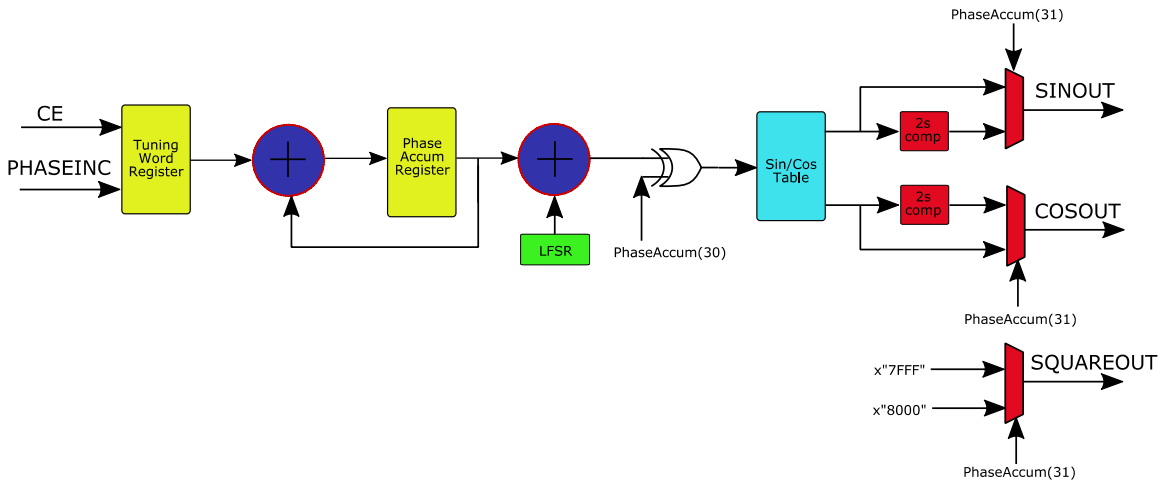


Figure 1: DDS block diagram

Ports

The DDS is clocked from a single clock domain (CLK input) and reset by the RST input.

Port Name	Direction	Description
CLK	in	AXI clock. All operations and interfaces are synchronous to this clock.
RST	in	Active high or low asynchronous reset. Internally synchronized to CLK. Polarity can be chosen by RESET_POLARITY generic.
CE	in	A new Phase Accumulator increment value will be loaded to the internal register at every rising clock edge where CE is high.
PHASEINC[31:0]	in	Phase Accumulator increment value, often known in DDS terms as the tuning word.
SINOUT[15:0]	out	Sine wave output (connect to DAC). Output format is 2s complement, full range is 32767 to -32767.
COSOUT[15:0]	out	Sine wave output (connect to DAC). Output format is 2s complement, full range is 32767 to -32767.
SQUAREOUT	out	Square Wave output (connect to DAC). Output format is 2s complement, full range is 32767 to -32767.

Options

The DDS system can be configured by using the VHDL generics in the dds_v1_0.vhd file:

Generic Name	Type	Description
RESET_POLARITY	bit	'1' – external reset is active high '0' – external reset is active low.
SINE_TABLE	integer	Only valid values are 16 or 12. Sets the number of address bits used for the internal sine lookup table. 16 = sine table will be the equivalent of 2^{16} entries. 12 = sine table will be the equivalent of 2^{12} entries.

Effect of reset on output ports

When the reset input is active, the output ports will take the following values:

Port Name	Value during reset
SINOUT[15:0]	0x0000
COSOUT[15:0]	0x7FFF
SQUAREOUT	0x8000

The reset input should be kept active for a minimum of two clock cycles to guarantee a correct reset of the DDS core.

Output frequency

The output frequency (FOUT) is dependent on the Phase Increment value (PHASEINC), the frequency of the main clock (CLK) and the size of the phase accumulator (32bits):

$$Fout = \frac{Fclk.PHASEINC}{2^{32}}$$

The maximum frequency that can be generated is FCLK/2 and the minimum (known as the DDS resolution is FCLK/2^{32}.

For example, if the input clock (CLK) is 200MHz, the frequency resolution is 0.0456Hz.

Sine/Cosine Lookup table

To save memory resources, the sine/cosine lookup table is implemented as a dual-port ROM which contains a quarter-wave (0 -> π/2) rather than a full wave (0 -> 2π).

The effective number of entries in the table is decided by the SINE_TABLE generic which has two possible values; 12 or 16. When SINE_TABLE = 12, there are effectively 4096 (2^{12}) entries in the table, when it is set to 16 there are 65536 entries (2^{16}).

The quadrant selection is done by the upper two bits of the phase accumulator output. When phaseAccum(31:30) = 00, the DDS generates the first quadrant (0 -> π/2). Whenever phaseAccum(30) = 1, we invert the addresses to the look-up table so that we can generate either the second or fourth quadrants. When phaseAccum(31) = 1, we generate the two's complement value of the sine/cosine table output to obtain the third and fourth quadrants.

Dithering

Phase dithering is a technique to reduce undesired spectral components in the DDS output, often known as "spurs", and so improves the Spurious Free Dynamic Range (SFDR).

Dithering is achieved by adding a pseudo-random value which is generated by a Linear Feedback Shift Register (LFSR) to the fractional bits of the phase accumulator output.

When SINE_TABLE = 12, there are 20 fractional bits and the pseudo-random value will be generated by a 20bit maximal length LFSR.

When SINE_TABLE = 16, there are 16 fractional bits and the pseudo-random value will be generated by a 16bit maximal length LFSR.

Resources Used

Estimation of used resources obtained with Vivado 2016.4, all options at default values.

- Target device is Kintex UltraScale KU040, -1 speed grade
- Target clock speed is 100MHz

Configuration	LUT	FF	DSP48	BRAM36k	I/O	Clock Buffer
All outputs connected 16bit sine table USE_DSP48 set to no	113	152	0	8	83 (1)	1 (2)
All outputs connected 12bit sine table USE_DSP48 set to no	98	152	0	0.5	83 (1)	1 (2)
All outputs connected 16bit sine table USE_DSP48 set to yes	81	88	1	8	83 (1)	1 (2)

(1) Normally some core I/O ports will be internal to the FPGA.
(2) Normally shared between other blocks in the system.

Maximum clock frequency

The DDS core was implemented in standalone mode (i.e. without other logic) to obtain an estimate of maximum clock frequency.

Configuration	FREQ (MHz)
All outputs connected 16bit sine table	400

Estimation of maximum clock speed obtained with Vivado 2016.4, all options at default values.

- Target device is Kintex UltraScale KU040, -1 speed grade
- USE_DSP48 for phaseAccum attribute set to “no”.

Timing restrictions

The external reset input (RST) is considered to be asynchronous and is synchronized internally to the clock (CLK). To guarantee that it will recognized, it must be asserted for at least two clock periods.

The synchronized internal reset will not be released until at least four clock periods after the external reset input (RST) has been deasserted. If the CE input port is asserted before the internal reset has been released it will be ignored and the tuning word register will not be loaded.

The latency from a load of a new tuning word to a new output frequency is five clocks:

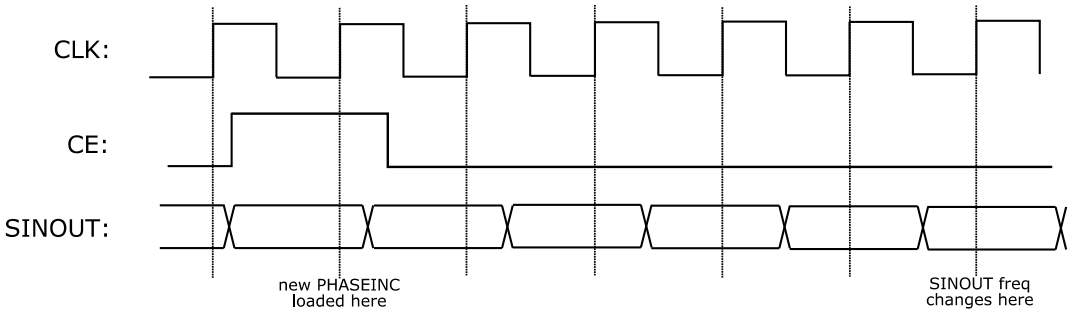


Figure 2: DDS latency

Xilinx-specific implementation details

The sine/cosine look-up tables can be implemented as either BlockRAM or distributed RAM. The look-up table RTL sources files (dpROM_12.vhd and dpROM_16.vhd) both contain the Xilinx-specific attributes to choose the implementation.

```
-- Vivado specific attributes to force use of BlockRAM
 attribute rom_style : string;
 attribute rom_style of rom : signal is "block";
```

The user can comment these attributes if it is preferred to leave the choice of implementation to the Vivado tool. Note that implementing the sine/cosine look-up table as distributed RAM is only recommended when SINE_TABLE = 12.

The 32bit phase accumulator in the dds.vhd source file is implemented in logic by default, but users can choose to move this to a DSP48 with the appropriate attribute:

```
    -- xilinx specific attribute to implement phase accumulator in DSP48
    attribute use_dsp48 : string;
    attribute use_dsp48 of phaseAccum : signal is "yes";
    attribute use_dsp48 of ditherWord : signal is "no";
```

Files and directories

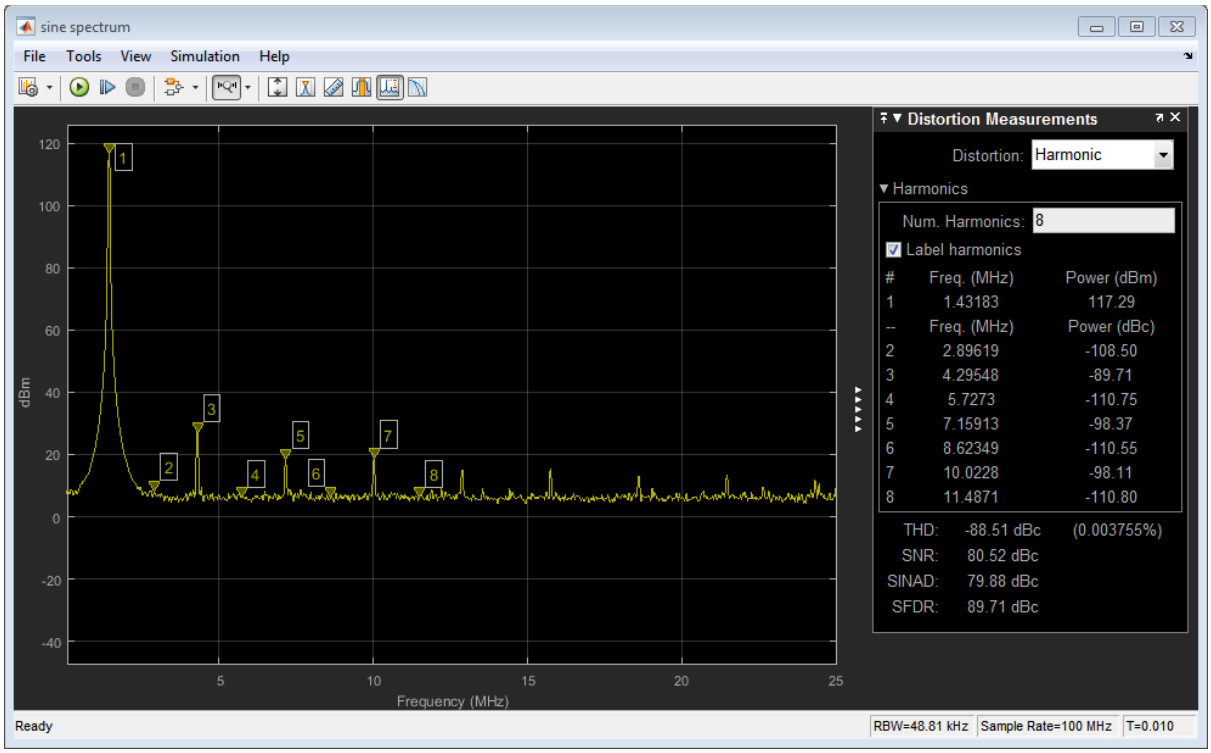
The complete zipped archive contains the following folders:

cst	*example XDC file*
src	*VHDL source files*
sim	*VHDL testbench*
doc	*This User Guide*

This User guide is relevant to the ver1_0 RTL source files.

Spectrum Analysis with System Generator

Fclk = 100MHz, Fout = 1.43183MHz, SINE_TABLE = 16



Fclk = 100MHz, Fout = 1.43183MHz, SINE_TABLE = 12