

18NTO308T Smart Sensor Systems

UNIT V

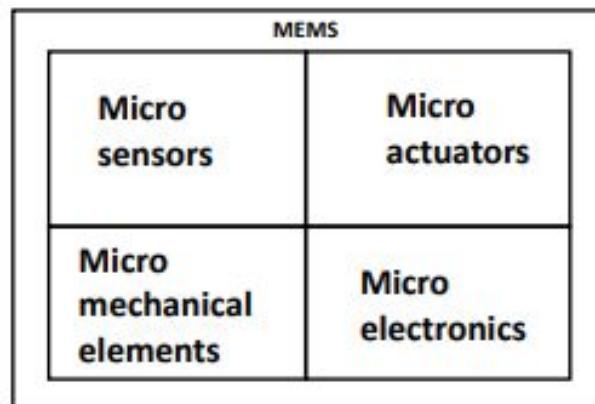
Lecture -1

Fundamentals of MEMS/ fabrication;
Frequently Used Microfabrication Processes

MEMS

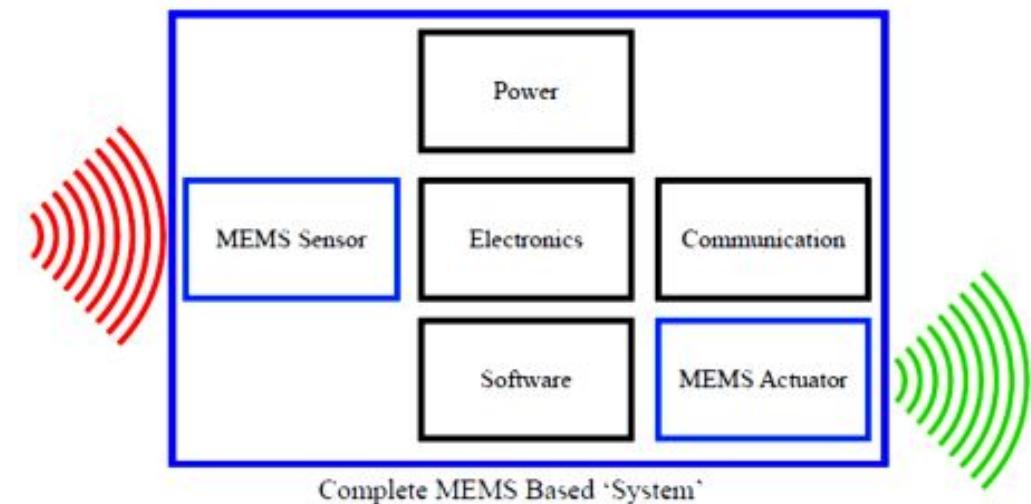
(MicroElectroMechanicalSystems)

- Micron sized electronic devices with signal processing circuits integrated together typically on a ‘Silicon’ substrate to perform a task.
- MEMS is an integration of Micro sensors, micro actuators, micro mechanical elements and micro electronics on a single silicon platform
- Microelectromechanical systems are also referred to as:
 - Micromachines (Japan)
 - Micro System Technology (MST) (Europe)
 - Microsystems
 - Micro Sensors and Actuators
 - Micro Transducers
- Features:
 - Micro electronics
 - Multiplicity
 - Miniaturization

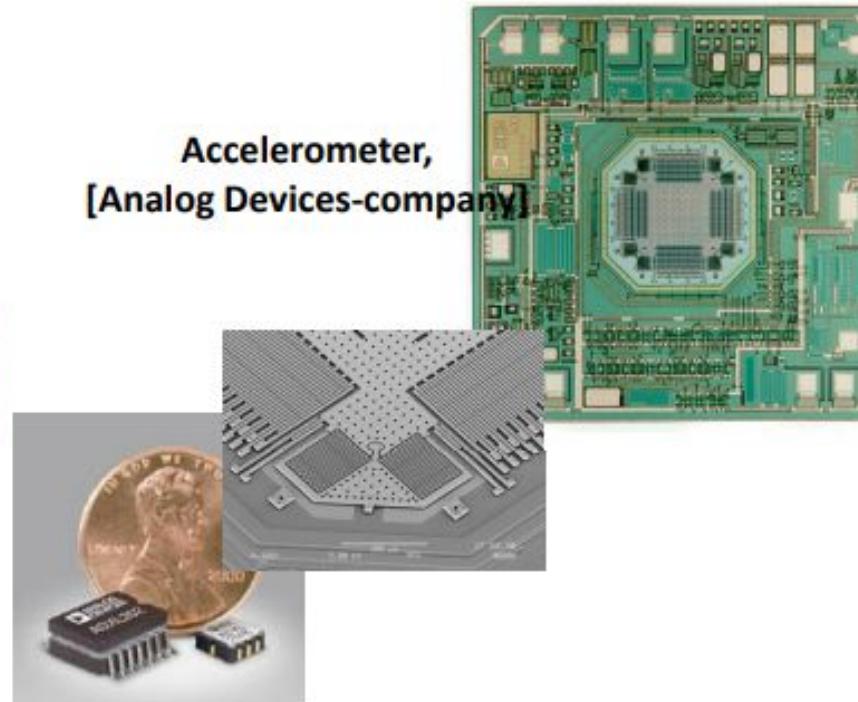


What are MEMS?

The term MEMS generally refers to the micro-scale 'components' or micro-scale 'devices' within a system. Not the entire system itself. In this sense, the name MEMS is somewhat misleading. In order to create a completely functioning 'System' that makes use of MEMS, the system will require various other sub-systems, such as: power, microelectronics, communication and software.



**Accelerometer,
[Analog Devices-company]**



History

- 1st Transistor was designed by “William Shockley, John Bardeen and Walter Brattain” on 1947 in Bell telephone lab, for which they got Nobel Prize on 1956

The first point contact transistor
William Shockley, John Bardeen, and Walter Brattain
Bell Laboratories, Murray Hill, New Jersey (1947)



- In 1953, Silicon substrate surface oxidation was demonstrated, which had opened a window for “Monolithic Transistors”
- 1958 – Integrated circuit (**Jack Kilby**)
- Gordon Moore (co-founder of Intel) predicted in 1965 that the transistor density of semiconductor chips would double roughly every 18 months.

History of MEMS Technology

- 1959 - "There's Plenty of Room at the Bottom" - Famous talk by Richard P. Feynman
- 1967 - Invention of surface micromachining (Nathanson, Resonant Gate Transistor)
- 1970 - Micromachined silicon pressure sensor demonstrated (Petersen)
- 1970 - First silicon accelerometer demonstrated (Kulite)
- 1977 - First capacitive pressure sensor (Stanford)
- 1984 - First polysilicon MEMS device (Howe, Muller)
- 1988 - Rotary electrostatic side drive motors (Fan, Tai, Muller)
- 1989 - Lateral comb drive (Tang, Nguyen, Howe)
- 1991 - Polysilicon hinges developed (Pister, Judy, Burgett, Fearing)
- 1992 - Multi User MEMS Process (MUMPs) is introduced by MCNC, (now MEMSCAP)
- 1993 - First surface micromachined accelerometer (ADXL50) sold, (Analog Devices)
- 1998 - Demonstration of DMD (Digital Mirror Device), (Texas Instruments)

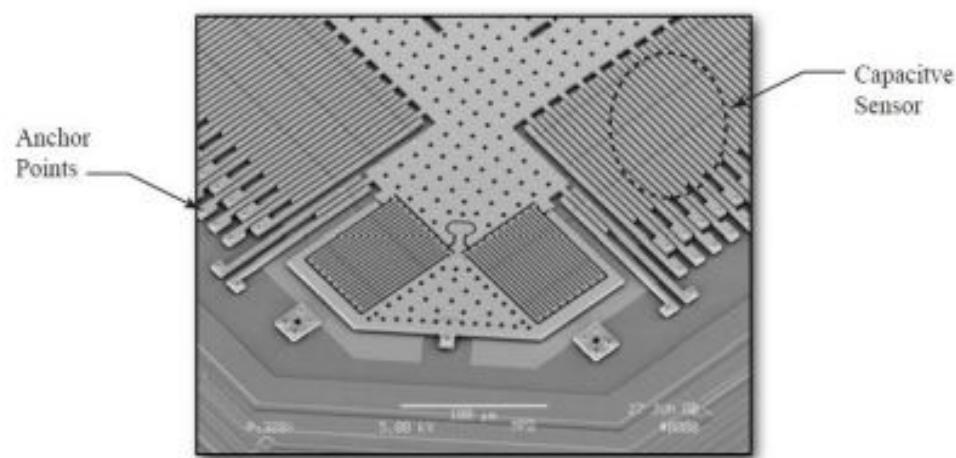
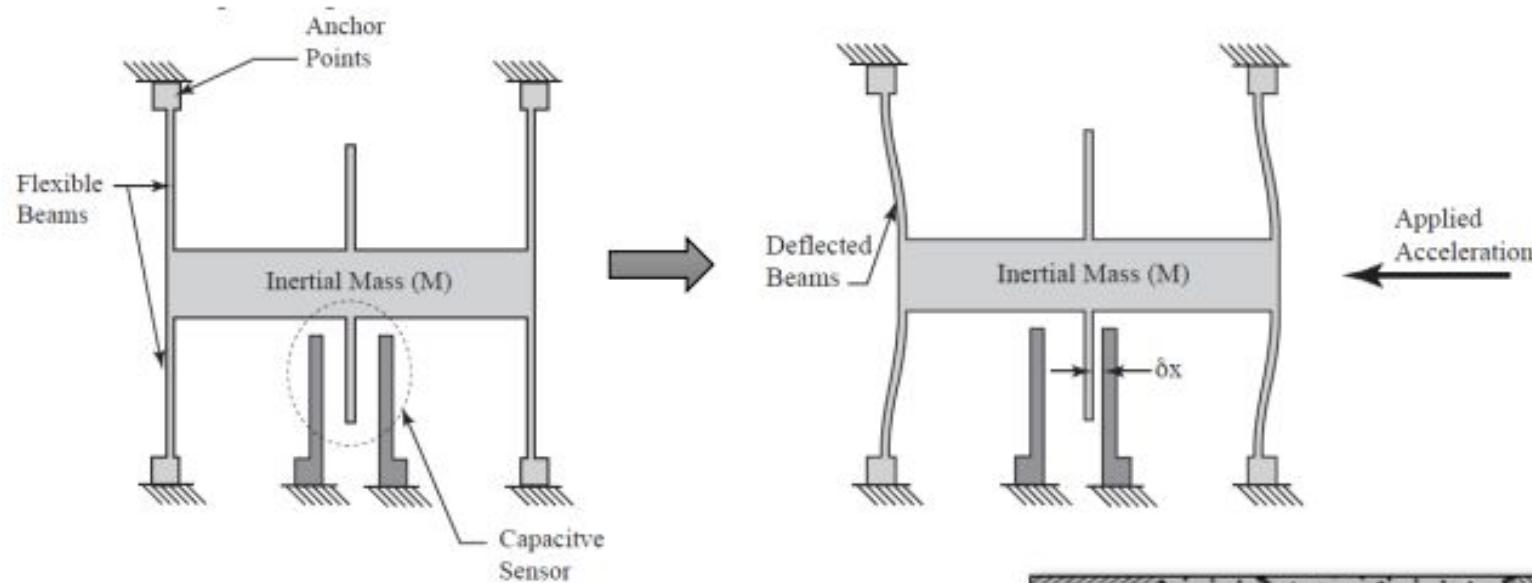
Need for MEMS

- For some applications, scaling devices down to the microscale may allow for some unique advantages. Physical size is only one of many considerations.
- For micro-scale sensors:
 - Higher Sensitivity
 - Better Linearity
 - Better Responsivity
 - Dynamic Range
 - Cost Reduction from Batch Fabrication
- For micro-scale actuators:
 - Dynamic Response Speed
 - Lower Power Consumption
 - Footprint
 - Cost Reduction from Batch Fabrication

How are MEMS made?

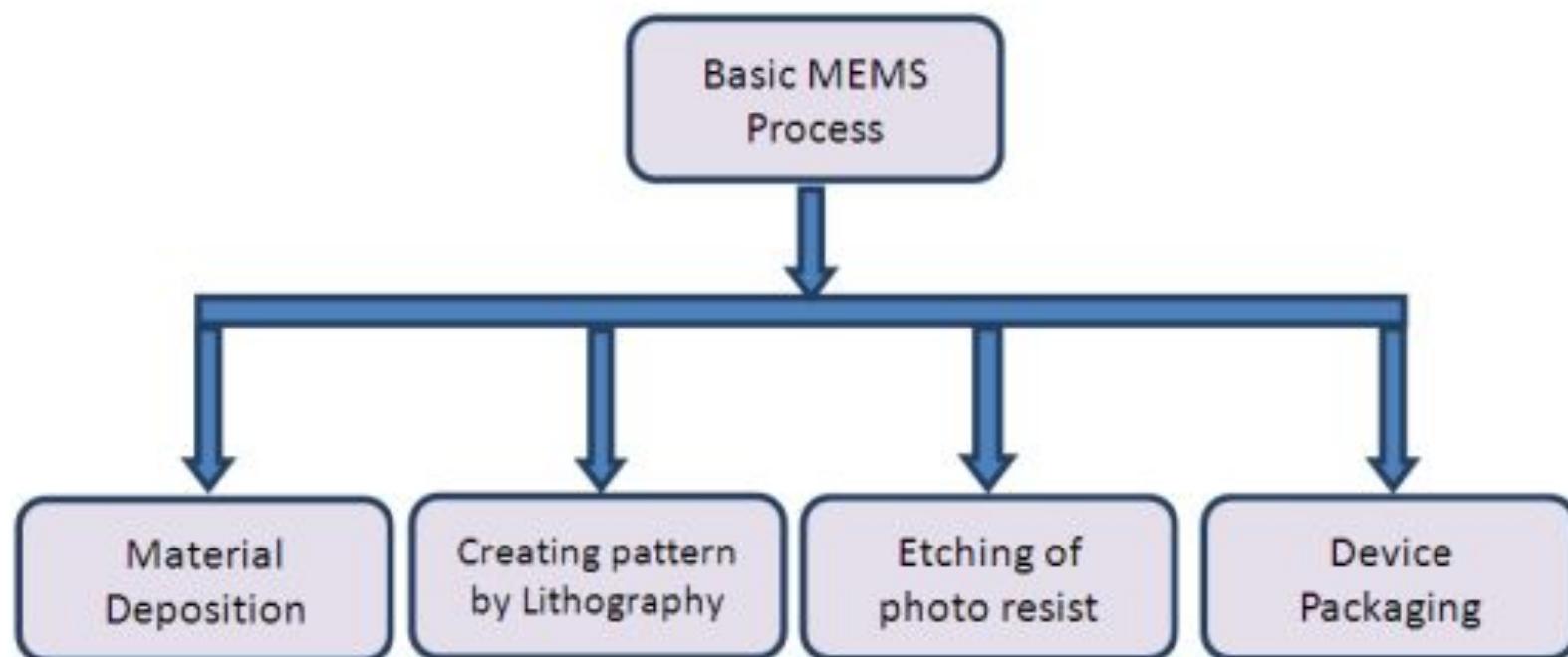
- MEMS are fabricated with a unique set of technologies collectively referred to as 'microfabrication' or 'micromachining'.
Due to their small size, standard machine tools cannot be used to machine MEMS features.
- These methods are quite different from macro-scale techniques.
- Micromachining technology is closely related to IC (integrated circuit) fabrication, with some notable differences.
- There are two main areas of micromachining:
 - Surface Micromachining, which is based on the successive deposition and etching of thin films of material such as silicon nitride, polysilicon, silicon oxide and gold.
 - Bulk Micromachining, which is based on the etching and bonding of thick sheets of material such as silicon oxides and crystalline silicon.

MEMS Working (Accelerometer Principle of Operation)



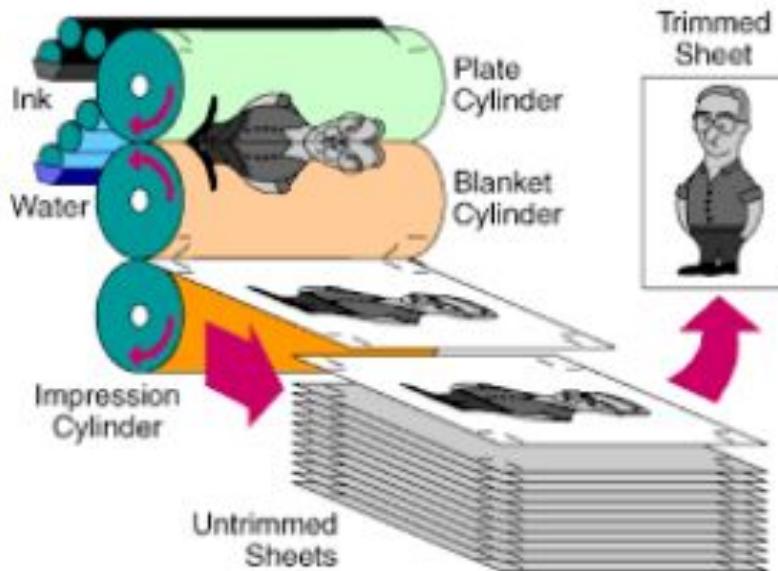
2-Axis Accelerometer, [Analog Devices]

Fundamentals of MEMS fabrication: Introduction and description of basic processes

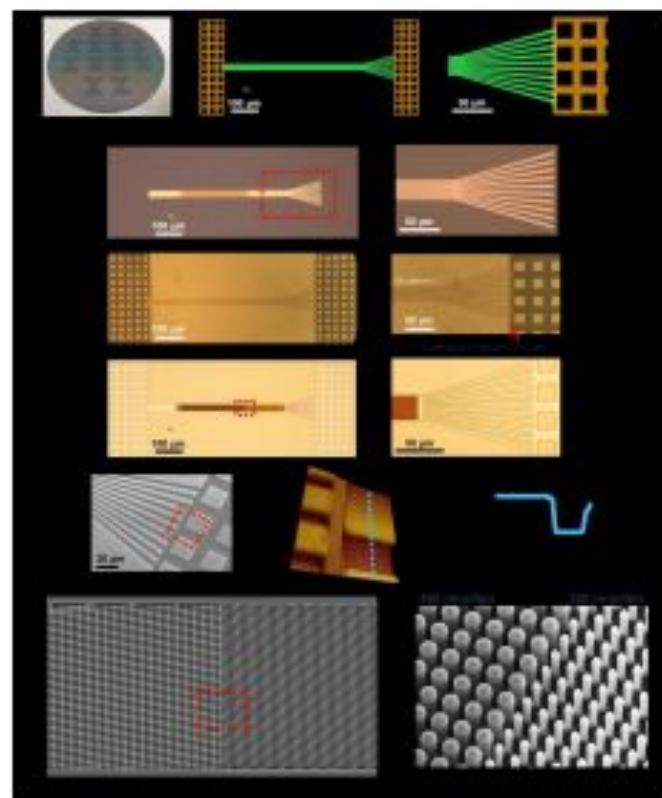


Lithography Process

- Lithography = Photoengraving
- Lithography in the MEMS context is typically the transfer of a pattern to a photosensitive material by selective exposure to a radiation source such as light.



Offset Lithography



Mixed lithography process for the fabrication of nanopillar (NP) array channels.

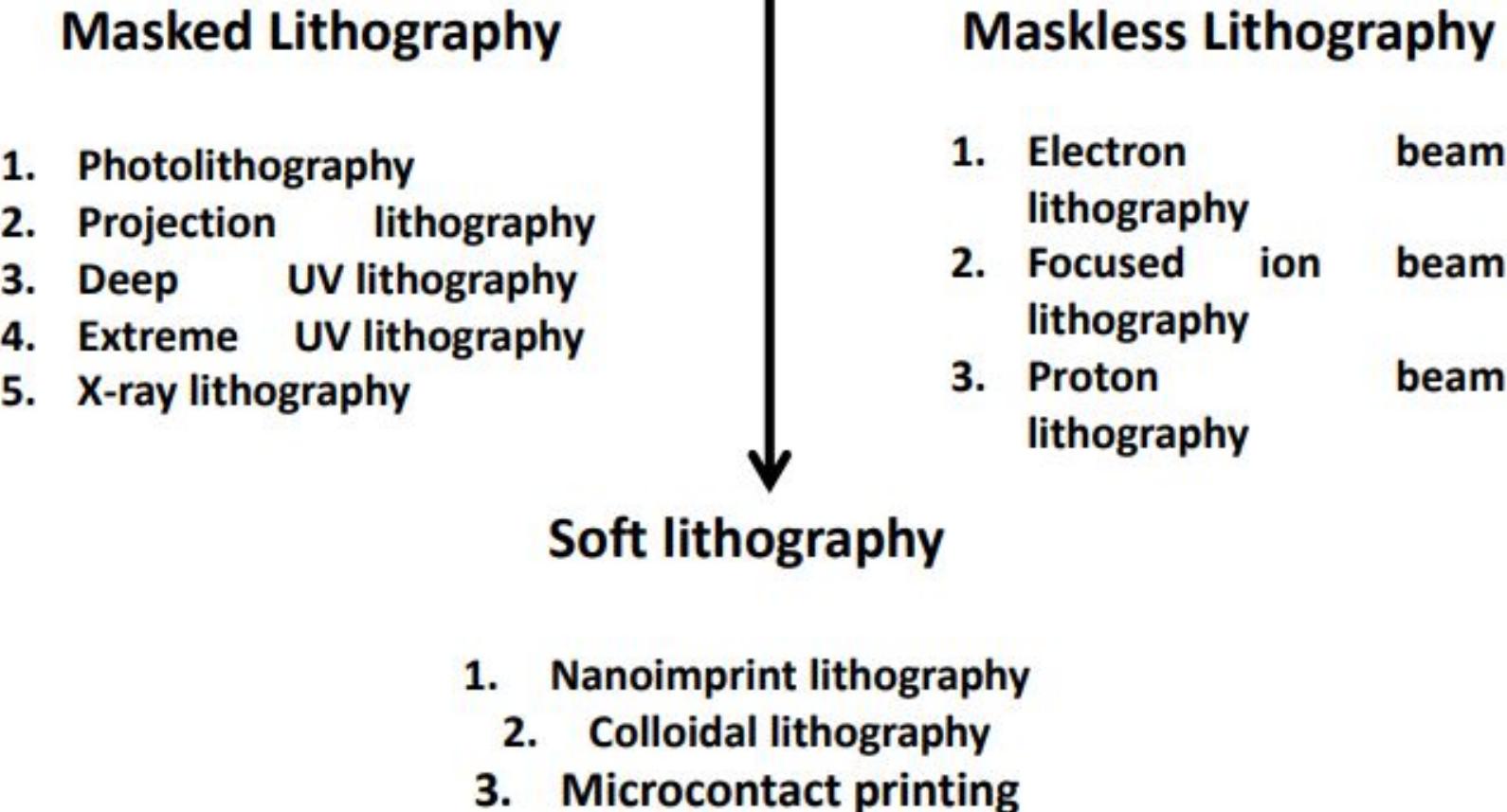
Types of lithography :

1. Optical or Photolithography
(Visible, UV, EUV)
2. Soft lithography
3. Electron beam lithography.
4. Ion beam lithography.
5. Ion track lithography.
6. X-ray lithography.
7. Nanoimprint lithography.
(Diblock copolymer, Alumina membrane, Nanochannel glass)
8. Scanning Probe lithography
(voltage pulse, CVD, Local electrodeposition, Dip-pen)

Basic techniques of lithography :

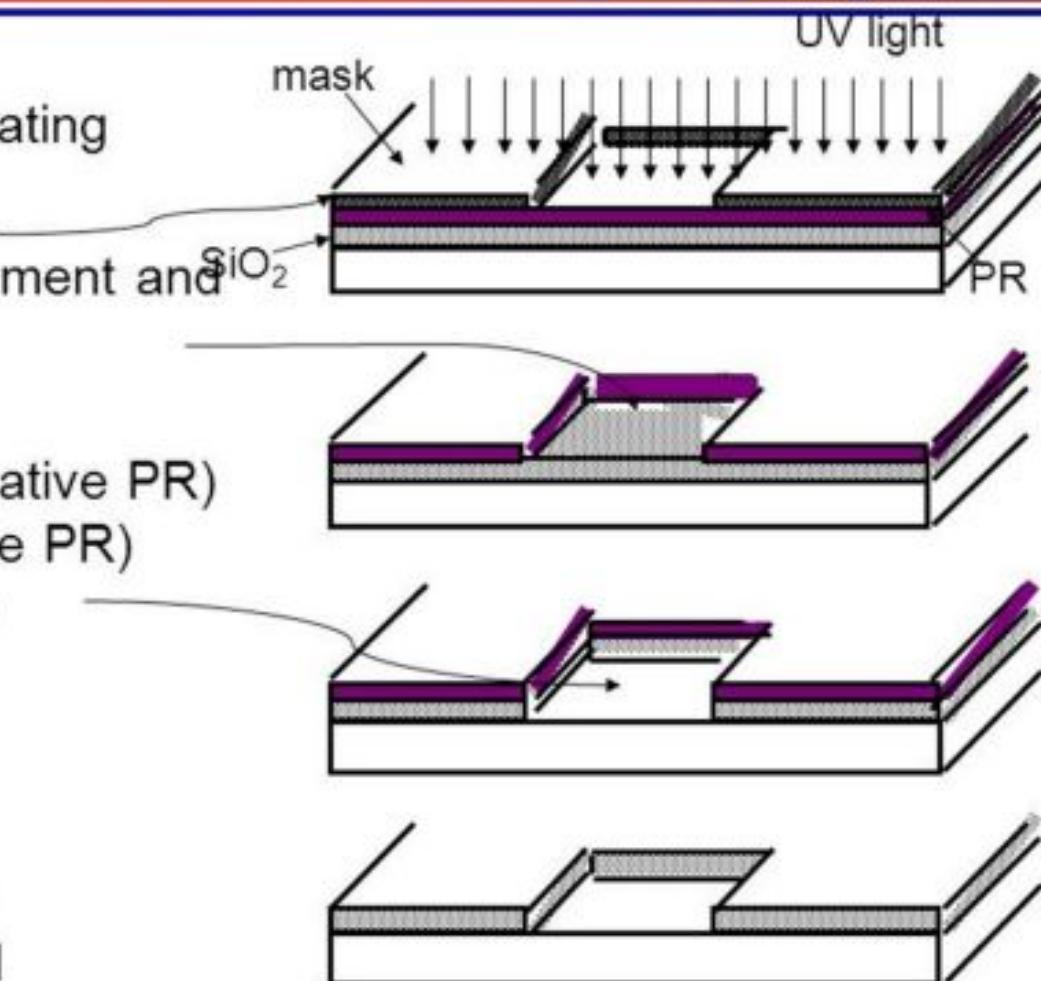
Substrate → Deposition of film → Pattern the film → Etching

Lithography



Patterning - Photolithography

1. Oxidation
2. Photoresist (PR) coating
3. Stepper exposure
4. Photoresist development and SiO_2 bake
5. Acid etching
 - Unexposed (negative PR)
 - Exposed (positive PR)
6. Spin, rinse, and dry
7. Processing step
 - Ion implantation
 - Plasma etching
 - Metal deposition
8. Photoresist removal



Important steps in lithography process

Process steps

- Surface cleaning
- Barrier layer formation (Oxidation), optional
- Spin coating with photoresist
- Soft baking
- Mask alignment and Exposure
- Development
- Hard baking
- Post process cleaning
- Etch back or liftoff

- Surface cleaning

Typical contaminants that must be removed prior to photoresist coating:
dust from scribing or cleaving (minimized by laser scribing) atmospheric dust
(minimized by good clean room practice) abrasive particles (from lapping or
CMP)
lint from wipers (minimized by using lint-free wipers)
photoresist residue from previous photolithography (minimized by performing
Oxygen plasma ashing)
Bacteria (minimized by good DI water system)

Films from other sources

Solvent residue

H₂O residue

Photoresist or developer residue

Oil

Silicone



Oxidation (Barrier layer formation)

Oxidation may be defined as the chemical process in which a substance gains oxygen or loses electrons and hydrogen. When one of the reactants is oxygen, then **oxidation** is the gain of oxygen.

Oxidation of silicon

It occurs immediately to form amorphous **silicon** dioxide film (called native oxide, usually 2-3 nm thick) by exposing a **silicon** surface to oxygen in atmospheric environment.

Thermal Oxidation

In microfabrication, thermal oxidation is a way to produce a thin layer of oxide (usually silicon dioxide) on the surface of a wafer. The technique forces an oxidizing agent to diffuse into the wafer at high temperature and react with it.

Thermal Oxidation of silicon

Thermal oxidation of silicon is usually performed at a temperature between 800 and 1200⁰C, resulting in oxide layer. It may use either water vapor or molecular oxygen as the oxidant. There are two types wet oxidation and dry oxidation.

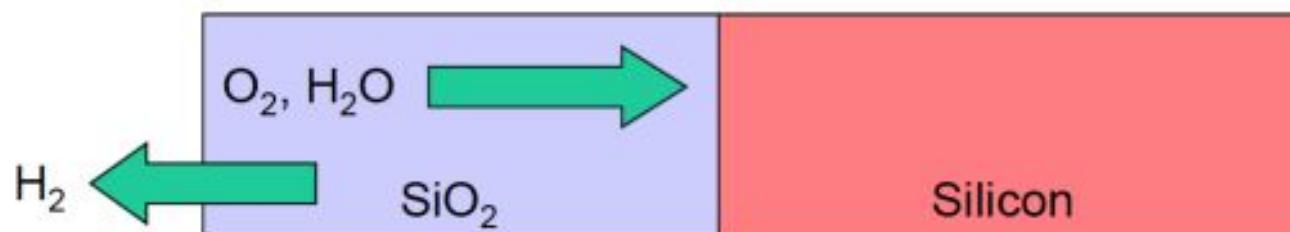
Why thermal Oxidation of silicon

Silicon Dioxide (SiO_2)

- The single thermodynamically stable oxide of silicon.
- Essential to the fabrication of MOS devices.
 - Creates extremely high electronic quality gate oxides.
- Essential to the patterning of silicon for high temperature processing.
 - Photoresist cannot handle temperatures much above 150°C.
 - Patterned SiO_2 can be used for masking diffusions, etches, and other processes up to temperatures of >1400°C.
- *The extreme purity and perfection of the Si/SiO_2 interface is the ultimate reason why silicon has been the #1 semiconductor for microelectronics.*
 - And is likely to remain so...

Oxidation of Silicon

- Carried out at temperatures of 900 – 1200°C.
- Dry oxidation: N_2 carrier gas + O_2
 - O_2 must diffuse through the growing SiO_2 layer.
- Wet oxidation: N_2 carrier gas + O_2 + H_2O (sat. vapor)
 - H_2O must diffuse through the growing SiO_2 layer.
 - Diffusion of H_2O is much faster than O_2 ; wet oxides grow faster.
 - H_2 must diffuse back out; usually very rapid and not a limiter.
- SiO_2 grows from the SiO_2/Si interface:
 - Oldest SiO_2 remains on the surface.
 - Youngest SiO_2 finishes at the SiO_2/Si interface.



Photoresist

It is a soft material used in the micro/nano fabrication process for pattern transfer, which changes its chemical properties upon exposure to different radiations like light, x-ray, ion, electron and proton beams

Chemical composition

Photoresists are composed of adhesive agents, sensitizers and solvents.

Binders (~20%)

As a binder Novolac is used, which is a synthetic resin to control the thermal characteristics of the resist.

Sensitizer (~10%)

Sensitizers define the photosensitivity of the resist. Sensitizers are composed of molecules which affect the solubility of the resist if it is exposed to energetic radiation. Thus the lithography has to take place in areas with ambient light which has a low energy.

Solvents (~70%)

Solvents define the viscosity of the resist. By annealing, the solvent is vaporized and the resist is stabilized.

Two types of photoresist

There are two types of photoresist, positive tone and negative tone resist, which are used in different applications.

Positive tone resist

In positive tone resist, the exposed areas become soluble in the developer solutions because the molecular bonding in the resist material will break upon radiation exposure (e.g. PMMA, ZEP520, AZ)

Negative tone resist

In negative tone resist the exposed areas become insoluble in the developer solution because the polymer chains will crosslink in the resist materials upon radiation exposure. (e.g. HSQ, SU8)

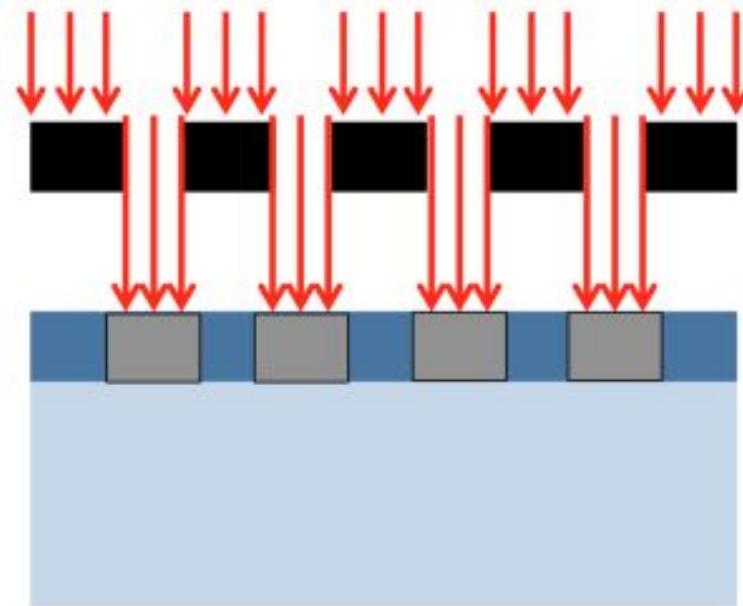
Characteristics of positive resists:

- excellent resolution
 - stable against
 - developers
 - can be developed in aqueous developers
 - bad resistance in etching
- or

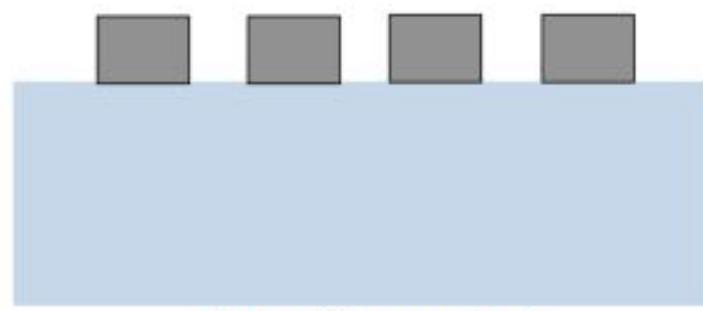
Characteristics of negative resists:

- high sensitiveness
- fair adhesion
- excellent resistance against etch or implantation processes
- cheaper than positive resists
- lower resolution
- organic developers are

Two types of photoresist



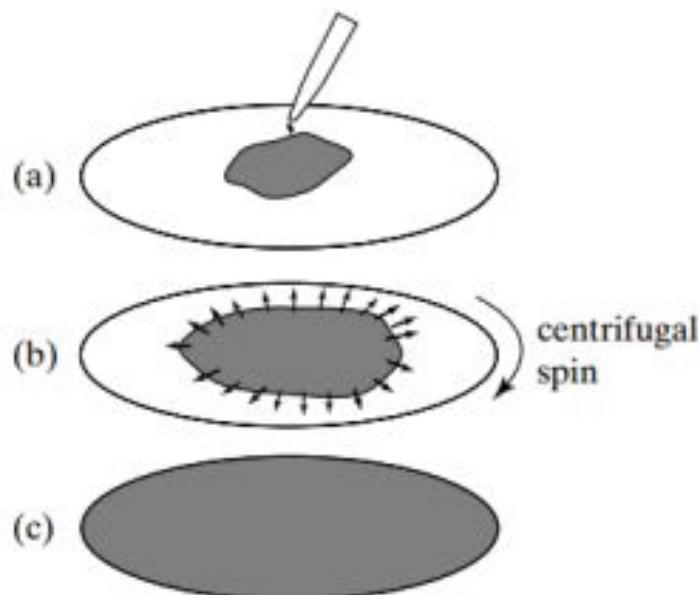
Positive resist



Negative resist

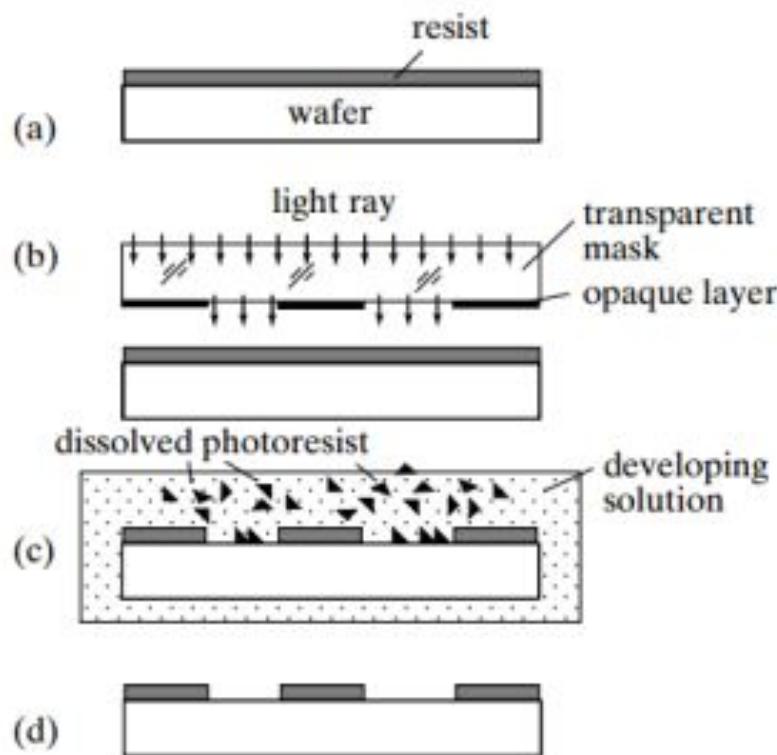
photoresist spin coating

Photoresist is applied to the wafer surface by spin coating, or spinning. In this operation, the substrate is placed on a vacuum chuck which holds the wafer in place. Next, a quantity of resist is dispensed from a nozzle while the chuck is rotated at a slow speed. Finally, the speed is ramped up to several thousand rpm which causes all but a thin layer of resist (generally about 1 to 2 μm thick) to be thrown off. By carefully controlling the rotation rate and the resist viscosity, uniform layers with reproducible thickness can be obtained.



The wafers are then placed in an exposure tool and aligned so that the patterns projected onto the substrate during the exposure step are registered properly with previously defined patterns. If this is the first mask, the patterns are aligned to the wafer flat.

The resist is exposed to light from an intense source as it passes through the clear areas of the mask or reticle. The light and dark patterns on the mask are thus transferred to the resist. The effect of the light is to change the solubility of the resist in a solution called the developer. Resists that increase in solubility upon exposure to light are called positive resists and are nearly universally used. (8) Because dark areas on the mask correspond to areas of resist which remain after development, the "polarity" of the mask pattern is duplicated in the positive resist.



The exposed wafer is then developed by either spraying or dipping the substrate in an appropriate solvent. Most positive resists are developed in proprietary alkaline solutions (e.g., dilute NaOH or KOH). The exposure process increases the solubility of the resist by a factor of about one thousand, so unexposed areas are largely untouched while the exposed portions are quickly washed away. However, since the solubility of unexposed resist is finite, careful control of the development process is essential in controlling the pattern dimensions.

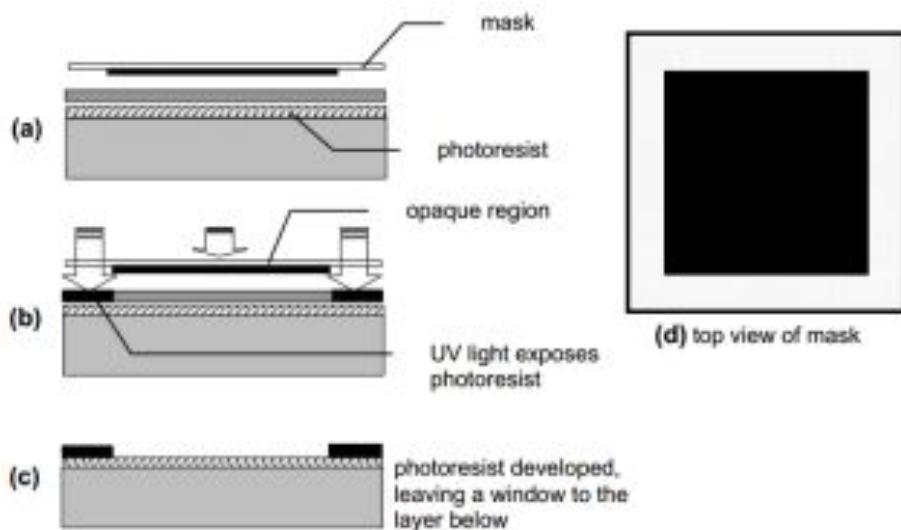
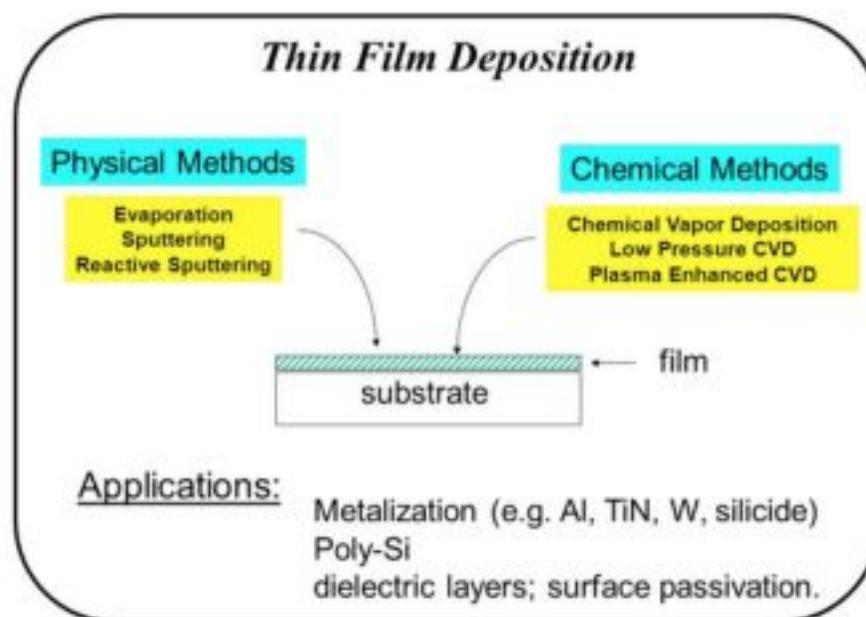


Fig. 3.1. Steps in a simple photolithographic process

Creating and transferring patterns—Photolithography

Deposition

It is an additive process by which a thin layer (usually sub micrometer or few micrometer thick) of metallic or dielectric or organic material is coated on the substrate surface



Thin film

Thin film: thickness typically <1000nm.

Special properties of thin films: different from bulk materials, it may be –

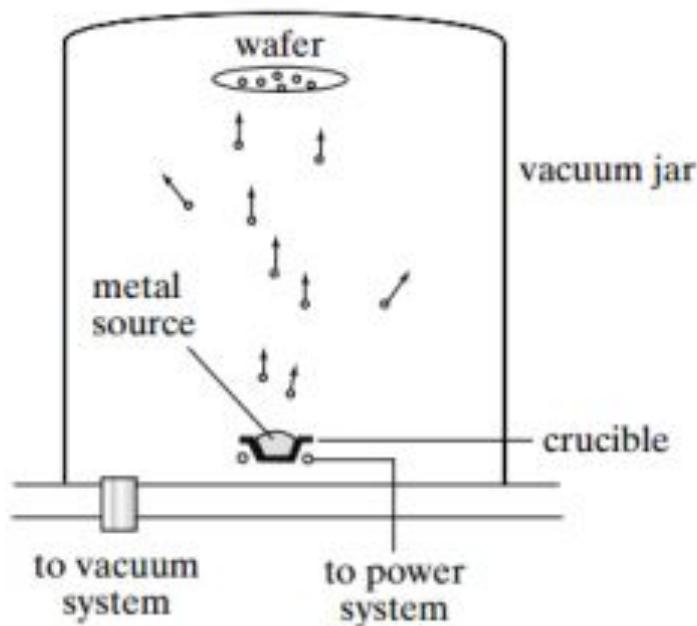
- Not fully dense
- Under stress
- Different defect structures from bulk
- Quasi - two dimensional (very thin films)
- Strongly influenced by surface and interface effects

Typical steps in making thin films:

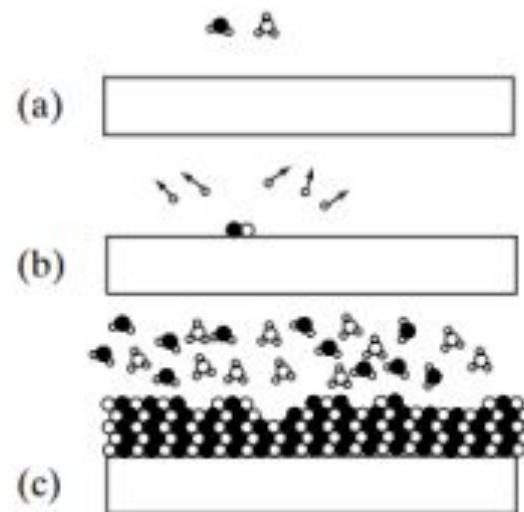
1. Emission of particles from source (heat, high voltage . . .)
2. Transport of particles to substrate
3. Condensation of particles on substrate

Lithography, thin film deposition and its etching are the three most important processes for micro-nano fabrication.

Thin Film Deposition



A schematic diagram of the metal evaporation equipment.



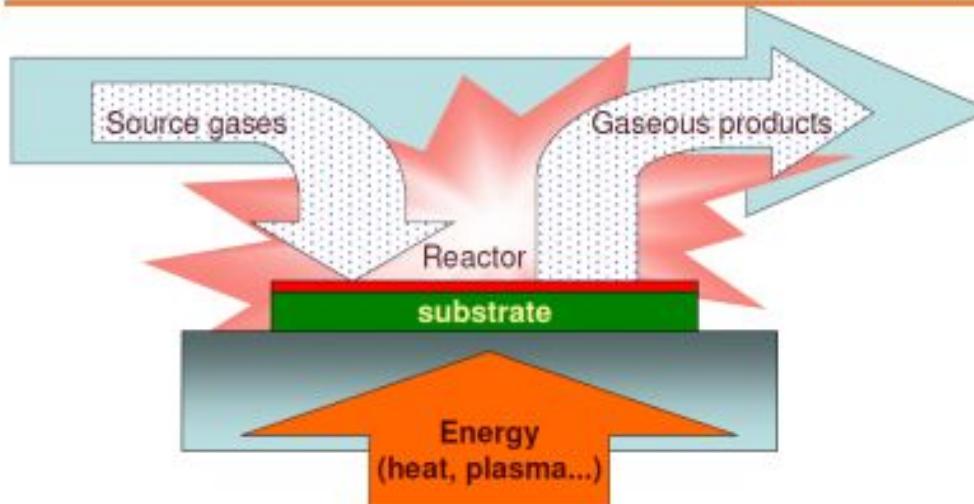
A process of chemical reactive deposition
(e.g., chemical vapor deposition)

Evaporation and sputtering are largely physical deposition processes. In both types of processes the material to be deposited starts out as a solid and is transported to the substrate surface where a film is slowly built up. In evaporation, the transport takes place by thermally converting the solid into a vapor. In sputtering, atoms or molecules of the desired material are removed (from the "target") by energetic ions created in a glow discharge.

The configuration of an evaporation system is shown in Figure. The system consists of a large bell jar evacuated to a low base pressure, generally less than 10^{-7} torr. (The lower the base pressure, the fewer the impurities incorporated into the growing film.) The substrates are placed near the top of the vacuum chamber, with the side receiving the film face down. The material to be deposited is converted into a vapor, which condenses onto the substrates. Because the base pressure in the system is low, the mean free path of the evaporated atoms is high. This means that collisions between source atoms and background gas molecules are rare; thus there is little scattering of the vapor as it travels from the crucible to the wafers.

The result is that evaporated films are not particularly conformal. The cloud of atoms striking the substrate can be shadowed by features on the surface of the substrate. To prevent this, the substrates are mounted on a planetary system which rotates them about their own axis and rotates the hemispherical planetary assembly about its own axis. Also, since the source emits vapor over a well-defined solid angle, the substrates must be placed at a considerable distance from the source to obtain reasonable wafer-to-wafer uniformity.

Chemical Vapor Deposition (CVD)



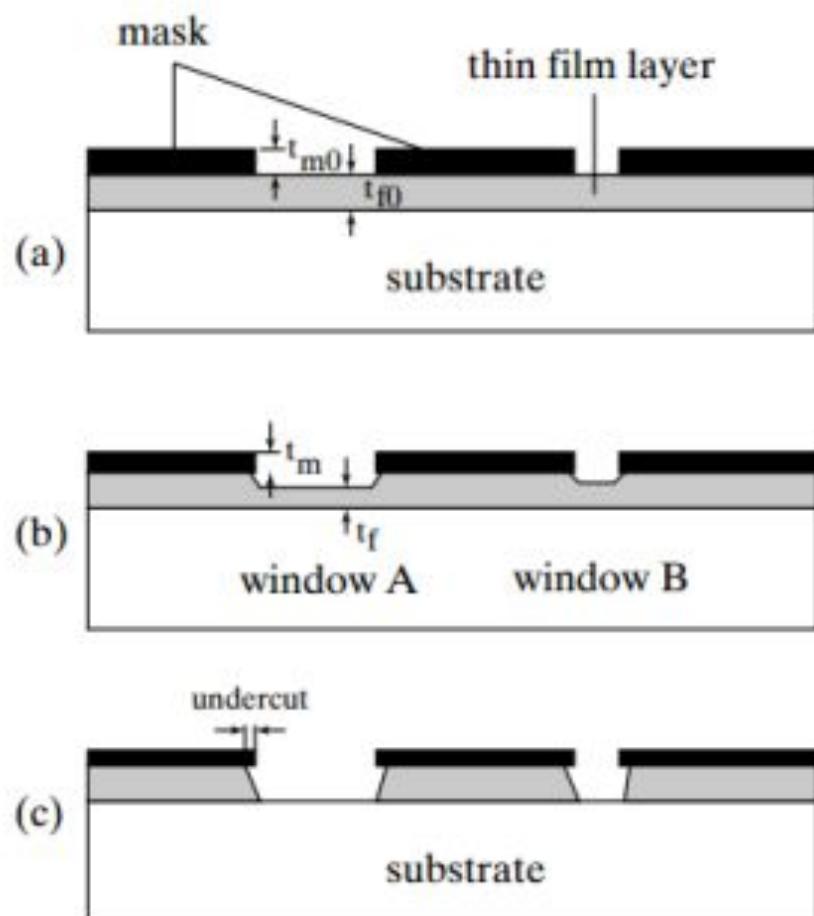
CVD : deposit film through chemical reaction and surface adsorption.

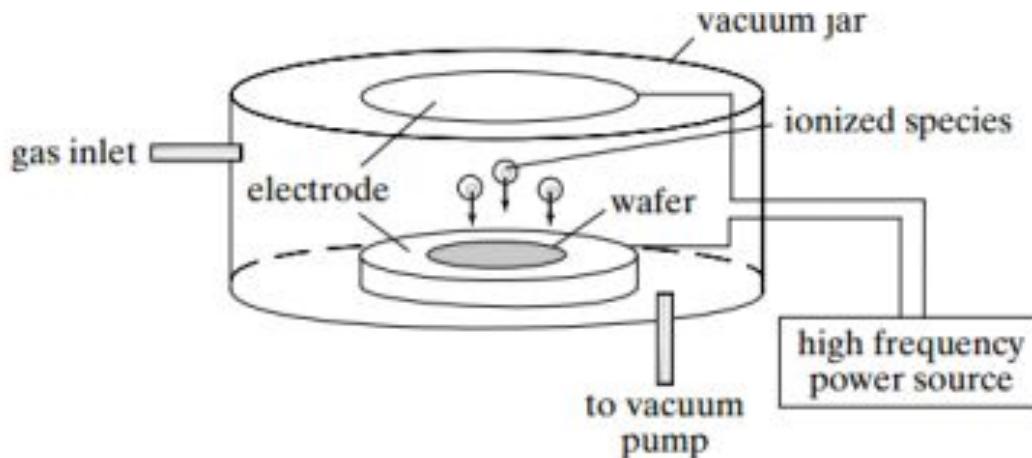
CVD steps:

- Introduce reactive gases to the chamber.
- Activate gases (decomposition) by heat or plasma.
- Gas adsorption by substrate surface .
- Reaction take place on substrate surface, film formed.
- Transport of volatile byproducts away from substrate.
- Exhaust waste.

Wet Etching

Removing materials by wet chemical reaction is common. It is used for removing metal, di-electrics, semiconductors, polymers, and functional materials. The selectivity of etching against masking materials, substrates and the target material is a crucial issue for MEMS process design. Important performance characteristics include etch rate, temperature, and uniformity.



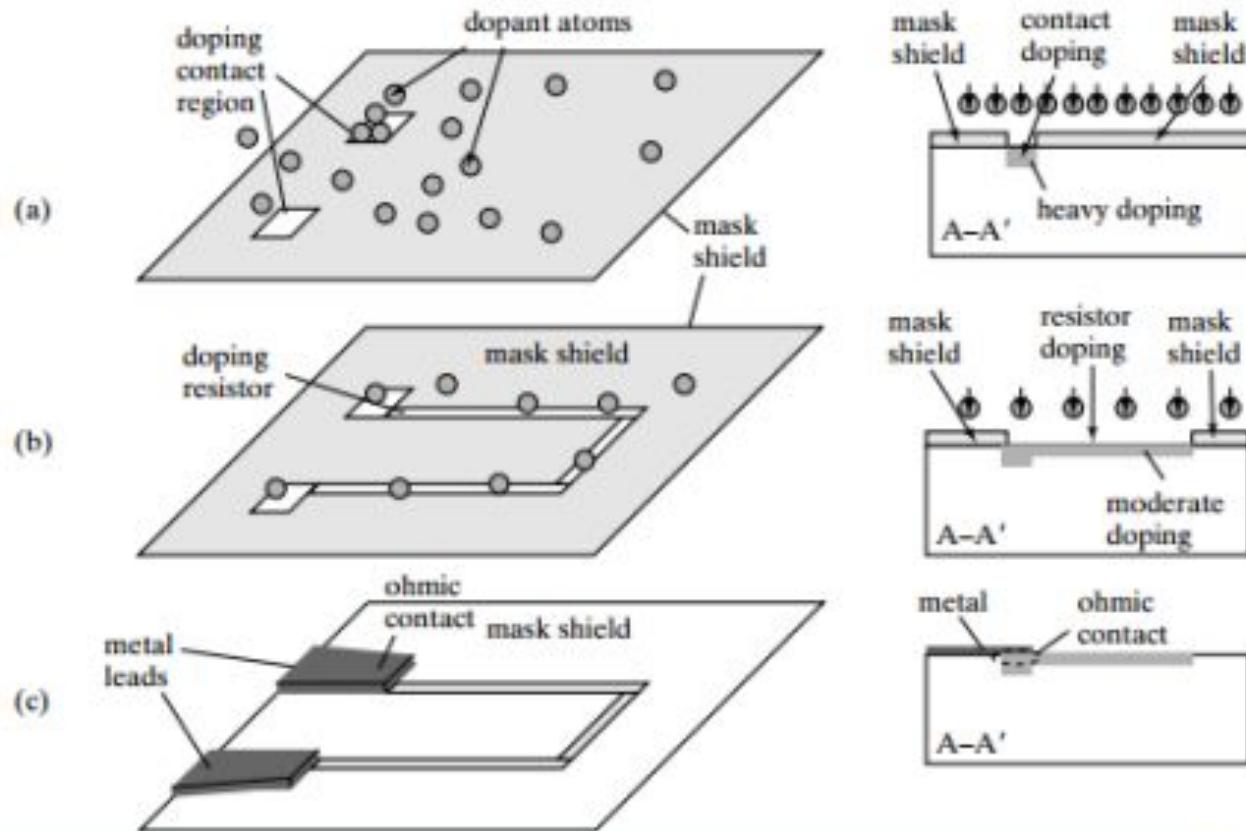
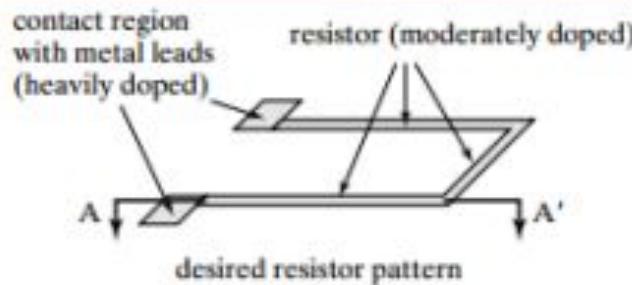


Plasma Etching and Reactive Ion Etching

Plasma etching is a very prominent method of removing materials from a wafer surface. Since the process does not involve wet chemicals, it is often referred to as dry etching. The etching is carried out in a specialized process equipment called the plasma etcher. A chamber with two opposing electrodes is filled with a chemically active gas species. The process pressure is typically rather low. Inside the plasma etcher, gas species are broken up by the electric field, creating active gaseous radicals that are electrically charged. The radicals may react with the wafer chemically. Meanwhile, the charged radicals may be accelerated in the electrical field to high speed and interact with materials on the wafer physically (bombardment, sputtering). Both physical and chemical processes may be present at the same time. In general, physical etching is more directional and anisotropic, whereas chemical etching is isotropic and material selective.

Doping

Doping is the process of planting dopant atoms into the host semiconductor lattice in order to change the electrical characteristics of the host material. The initial source dopants can be placed on the surface of the wafer or precisely injected into the silicon lattice using the ion implantation method.

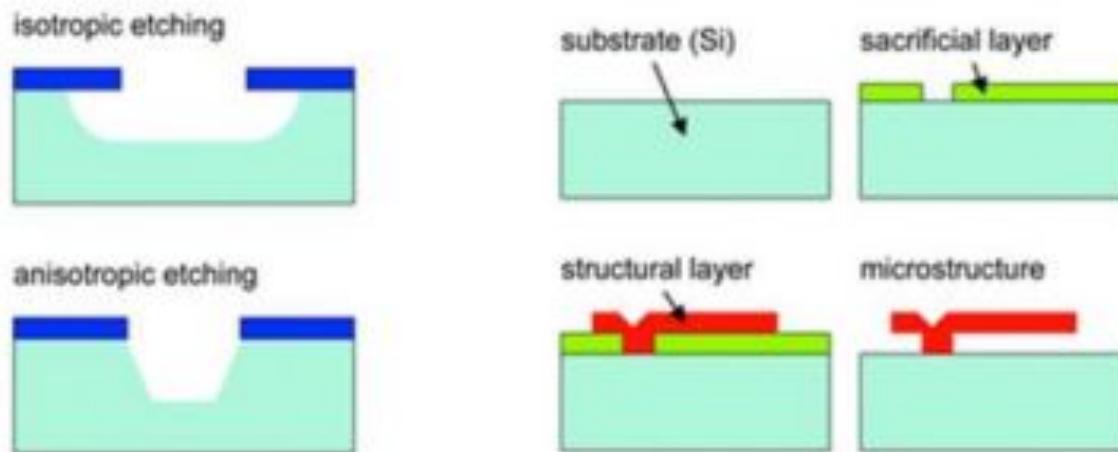


MEMS fabrication technologies: bulk micromachining

Silicon micromachining

Most MEMS fabrication techniques can be classified as

- *in the substrate, bulk micromachining, or*
- *above the substrate, surface micromachining.*



Bulk micromachining is a fabrication technique to selectively remove substrate to create MEMS devices

Surface micromachining is a fabrication technique for depositing various films on top of the substrate (substrate as a construction base material) and selectively remove parts of deposited films to create MEMS devices

Bulk micromachining processes

The process of bulk micromachining refers to creating structures by re-moving material from the substrate. This can occur in many ways. The most prevalent method is to chemically eat away the material in a process called chemical etching, or simply etching. Solutions containing the re-quired components to achieve the desired chemical reaction(s) are appro-priately called etchants. Historically most etchants have been in liquid form, and the process has therefore also been called wet chemical etching.

This also distinguishes the process from those in which the reactive com-ponents are contained in a gas or plasma, which is called dry etching.

The overall goal in bulk micromachining is to remove material from the substrate itself. The amount of material removed per unit time during etch-ing is called the etch rate. It is usually measured in dimensions of length (signifying the depth into the substrate) per unit time. In general, higher etch rates are desirable. This allows for batch fabrication to proceed more quickly.

4.2.1 Wet chemical etching

As an example of wet etching, consider Fig. 4.1, which shows a two step process used to etch a pit into a (100) silicon wafer. In the first step a silicon dioxide layer is etched through a window of a photoresist mask. The resist layer is then stripped, leaving a window through the oxide layer to the silicon substrate below. The oxide layer now forms a mask for etching the substrate. (This is often referred to as a hard mask.) Using a different etchant, the exposed portion of the silicon wafer is etched next, forming the desired pit in the substrate.

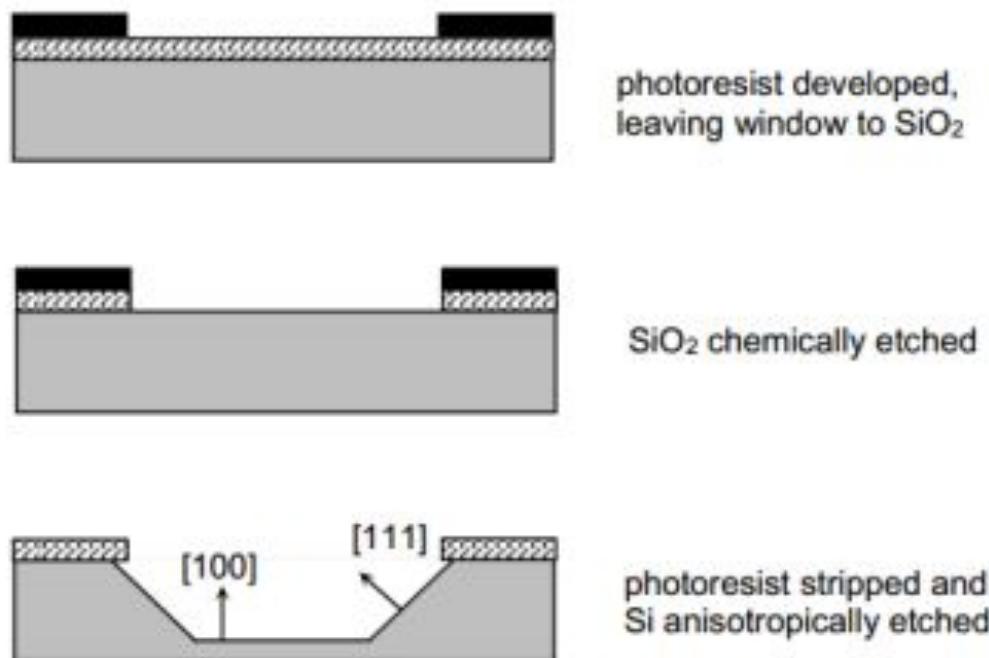
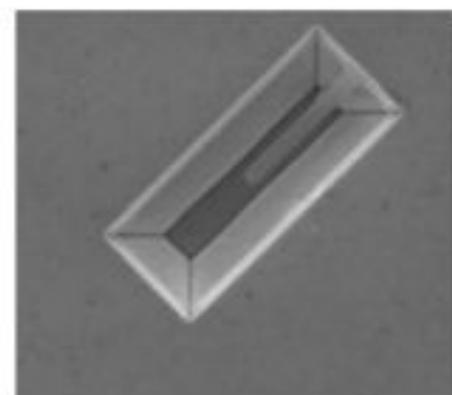


Fig. 4.1. Two step wet etching process to produce a pit in a (100) silicon wafer

It is important to realize that the etchants used in the above described process react with everything with which they come into contact, at least to a small degree. For the process to work, however, the etchants must react very slowly with some materials, while reacting very quickly with others. For example, we would like the etchant used to etch the oxide layer to react very quickly with the oxide itself, but very slowly with the photoresist layer as well as with the silicon substrate below. In this way we can ensure that the resulting pattern in the oxide layer closely resembles the photoresist pattern, and that the reaction stops when the substrate is reached. Likewise, the etchant used for creating the pit in the substrate should react quickly with the silicon, but very slowly with the oxide.

The relative etch rate of an etchant solution with one material compared to another is called **selectivity**. In essence we are playing games with selectivity in order to bring about the desired structures.

You may have noticed in Fig. 4.1 that the resulting window in the oxide layer does not resemble the photoresist mask perfectly. Specifically, the opening in the oxide is slightly wider than that of the photoresist. This is because the chemical reaction has proceeded in the horizontal direction to some degree as well as in the thickness direction of the oxide layer. This phenomenon is called **undercutting**.



You may also have noticed in two preceding figures that the silicon wafer pits have slanted sidewalls. This is because the etchant used not only is selective towards the silicon material, but to certain crystallographic directions as well. When an etching process proceeds at different rates in different directions, it is called an **anisotropic etch**. For the etchant and crystalline orientation of the wafer shown here, the resulting shape of the pit resembles an inverted pyramid with sidewalls corresponding to the {111} planes. When the etching process proceeds at the same rate in all directions, we have an **isotropic etch**. The resulting shape resembles the rounded pit shown in Fig. 4.3.

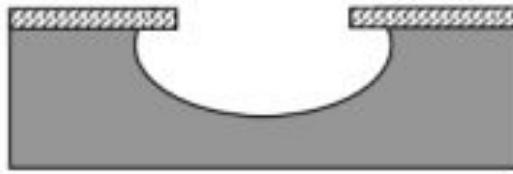


Fig. 4.3. Side view of an isotropically etched pit

Table 4.1 gives the etch rates of various commonly used etchants with respect to silicon and silicon dioxide. Etch rates for various materials are available from numerous sources including handbooks and online resources. They can differ significantly based on differences in conditions, such as concentration and temperature. From Table 4.1 we see that the first two etchants listed are highly selective towards SiO_2 over Si, whereas the last three are selective towards Si. Furthermore, basic etchants tend to etch silicon anisotropically, whereas acidic etchants are isotropic. Since most photoresists are soluble in basic solutions, it is therefore usually necessary to form a silicon dioxide hard mask to etch silicon anisotropically.

Table 4.1. Applications and properties of different etchants (Data taken from Madou)

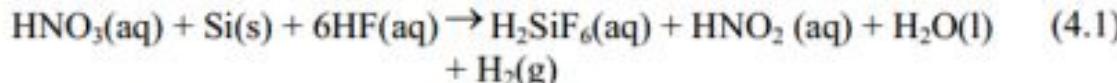
Etchant	Application	Etch Rate (s)	Notes
48% HF	SiO ₂	20-2000 nm/min 0.3 Å/min for Si	Isotropic
Buffered oxide etch (BOE) (28 mL HF/113 g NH ₄ F/170 mL H ₂ O)	SiO ₂	100-500 nm/min (25°C)	Isotropic
Poly etch HF/HNO ₃ /H ₂ O ₂ 8/75/17 (v/v/v)	Si	5 µm/min (25°C)	Isotropic
KOH (44 g/100 mL)	Si	1.4 µm/min (80°C) 28 Å/min SiO ₂	Anisotropic IC incompatible
Tetramethylammonium hydroxide (TMAH) (22 wt%)	Si	10 µm/min (90°C) SiO ₂ virtually unreac- tive	Anisotropic IC incompatible

In wet chemical etching, an etchant solution is brought into contact with the surface to be etched. The reactive component in the etchant solution first finds its way to the surface. Next, one or more chemical reactions take place involving the surface material and the etchant. Last, the products of the reaction(s) move away from the surface, and new etchant moves in to take the place of the products. This process continues until actively stopped in some way.

Isotropic etching

In isotropic wet etching the etch rate is the same in all directions. Isotropic etchants are typically acidic with the reactions carried out at room temperature. The isotropy is due to the fast chemical kinetics (fast reactions) of the etchant/material combination. Hence, isotropic etching tends to be diffusion limited. Isotropic etchants also have the fastest etch rates, on the order of microns to tens of microns per minute.

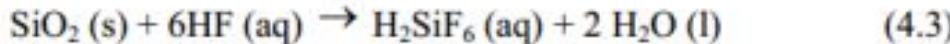
One of the most prevalent isotropic etchants used with silicon is *HNA* ($\text{HF}/\text{HNO}_3/\text{HC}_2\text{H}_3\text{O}_2$) also called *poly etch* for its frequent use with polycrystalline silicon¹. The overall reaction is given by



The etching process actually occurs in several steps. In the first step, nitric acid oxidizes the silicon.



In the second step, the newly formed silicon dioxide is etched by the hydrofluoric acid.



In the isotropic etching of glass or silicon dioxide, the oxidation step is not required. Hence, there is no need for nitric acid, and a buffered oxide etch (BOE) consisting of aqueous HF and NH_4F can be used. The reaction proceeds directly from the second step of Eq. (4.3).

In isotropic etching the amount of undercutting of a mask will be on the order of the depth to which the layer is etched. For example, the opening at the top of an oxide layer created using a photoresist mask with initial dimensions of $200\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$ will have dimensions of $210\text{ }\mu\text{m} \times 210\text{ }\mu\text{m}$ after etching to a depth of $10\text{ }\mu\text{m}$.

Anisotropic etching

Unlike isotropic etching, anisotropic etching occurs at different rates in different directions, specifically along different crystalline planes. The etchants are typically alkaline instead of acidic, and the reactions are carried out at slightly elevated temperatures, usually between 70°C and 90°C. Also unlike isotropic etching, the process is reaction limited, resulting in slower etch rates on the order of 1 μm/min. The anisotropy itself is due to different crystal planes etching at different rates.

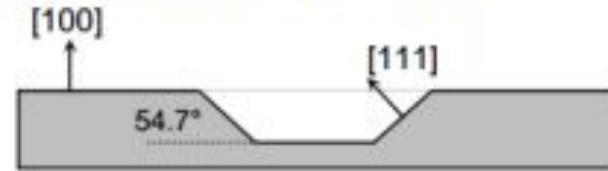
In the anisotropic etching of silicon, silicon dioxide is formed first. Then, the oxide is reacted with a strong base, producing $\text{Si}(\text{OH})_4$ (aq) or more likely, $\text{H}_2\text{SiO}_4^{2-}$ (aq). The {111} planes etch the slowest, and the {100} planes etch the fastest. In fact, the etch rate for the {100} planes is 100 times greater than that for {111} planes when using KOH as the etchant!

Common anisotropic etchants of silicon and their properties are summarized in Table 4.2

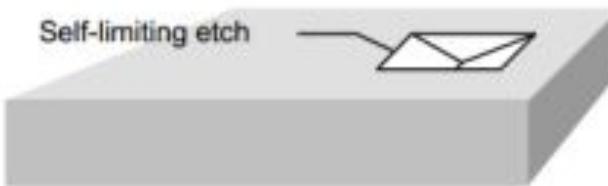
Table 4.2. Selected anisotropic etchants of silicon.

Etchant	Temperature	Si etch rate (μm/min)	{111}/{100} selectivity	SiO_2 etch rate (nm/min)
KOH (40-50 wt%)	70°-90°C	0.5-3	100:1	10
EDP (750ml Ethyl- enediamine 120g Py- rochatechol, 100 ml water)	115°C	0.75	35:1	0.2
TMAH (Tetra- thylammonium hy-	90°C	0.5-1.5	50:1	0.1

MEMS designers use anisotropic etching techniques in order to create the uniquely shaped trenches often seen in MEMS devices. The most common of these is the inverted pyramid shape seen in the anisotropic etching of (100) silicon, the sidewalls of which make angles of 54.7° with the plane of the wafer. (Fig. 4.5.) If the window through the hard mask is made small enough, the etch will continue only until the intersection of the {111} planes is reached. The crystalline structure serves as its own etch stop in this case. However, this technique only works when the {111} planes form concave corners. Even the slightest deformity on a convex corner of the intersection of {111} planes will expose much faster etching planes, which leads to massive undercutting of the hard mask. Sometimes this is most undesirable and the designer must make use of cleverly designed sets of masks for “corner compensation”. However, this undercutting is often planned right into the process, as is the case in creating suspended structures over etched pits. (Fig. 4.6.)



(a)



(b)

Fig. 4.5. Anisotropic etching of (100) silicon. (a) Anisotropic etching exposes {111} planes, creating sidewalls at 54.7° angles. (b) Intersection of various {111} planes creating a self-limited etch.

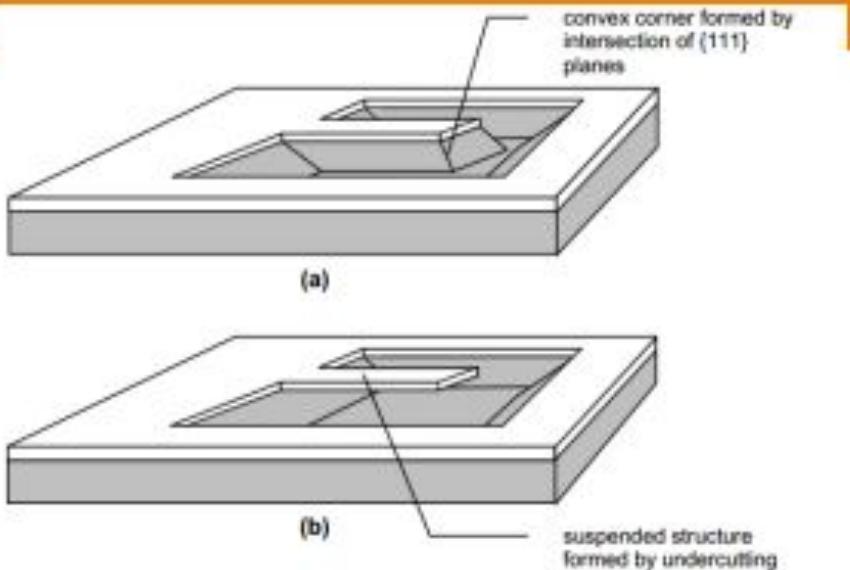


Fig. 4.6. Purposely exposing convex corners formed by {111} planes (a) can be used to undercut hard masks, thereby creating suspended structures (b).

For (110) silicon anisotropic etching results in an opening in the plane of the wafer that resembles a lopsided hexagon. The sidewalls make different angles with the horizontal than in (100) silicon. (Fig. 4.7.) Four of

these sidewalls are vertical, a feature that otherwise usually requires more expensive and involved techniques compared to wet chemical etching. The bottom of the etched pit is initially a {110} plane, and therefore flat. For long etch times, however, the two slanted {111} planes intersect each other, creating a self-limiting etch. This self-limiting etch is pronounced for mask openings with small aspect ratios, but not large ones. Hence, anisotropic etching of (110) silicon is often used to create long narrow trenches like those used in active liquid cooling of microelectronic components. As with (100) silicon, undercutting of hard masks is sometimes used — to create suspended structures.

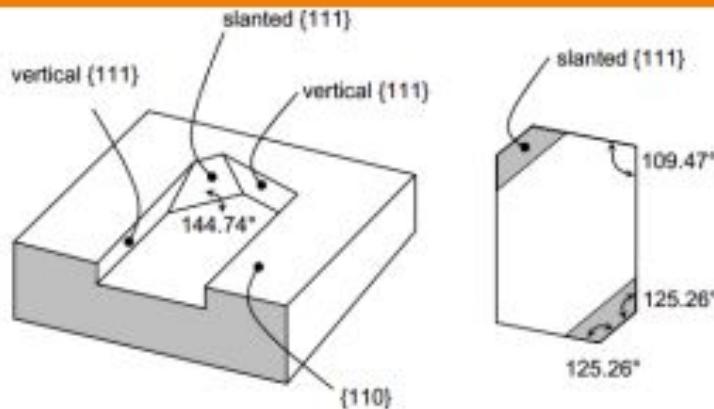


Fig. 4.7. Anisotropic etching of (110) silicon exposes various {111} planes, producing four vertical sidewalls and two slanted sidewalls.

For (111) silicon, the surface plane of the substrate is the one that etches the slowest. Since no other planes are exposed, a bare (111) wafer placed in an anisotropic etchant simply etches very, very slowly with no result other than the wafer becoming thinner. If a “starter hole” is pre-etched in the surface using some other technique, however, other planes will be exposed. Anisotropic etching can now proceed. This is most often used to create pits or trenches underneath a hard mask on the surface. (Fig. 4.8 (a).) When the sidewalls of the pre-etched shape are protected, deep trenches well below the surface can be formed. (Fig. 4.8 (b).) This technique is sometimes used to create microfluidic channels.

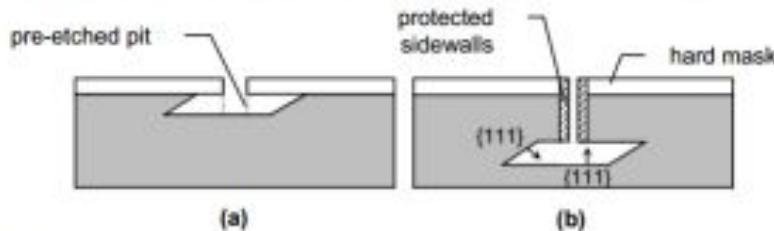


Fig. 4.8. Anisotropic etching of (111) silicon: (a) A pit must be pre-etched before anisotropic etching can proceed. (b) Protecting the sidewalls of the pre-etched shape can be used to produce deep trenches.

Etch stop

Getting the chemical reaction that makes up an etching process to stop can pose a difficult problem within microfabrication. One technique is to time the etch, simply pulling a wafer out of the wet etching solution when the desired depth has been reached. Variability of etch rates, however, makes this technique less than precise. The resolution for thickness is generally on the orders of microns. That is to say, if you attempt to leave a membrane in a silicon wafer less than 10 μm thick using this technique, it could result in a membrane 0 μm thick!

In an *insulator etch stop* the etching process stops when the etchant reaches an insulating layer. In the case of a silicon wafer, the insulator is usually an oxide layer grown on one side of the wafer. Due to the selectivity of the etchant, the etching essentially ceases upon reaching the silicon dioxide. In the case of an insulator etch stop, the insulator makes up part of the structure of the MEMS.

Other etch stop techniques involve varying etchant composition and temperature. Much more precise, however, is to make use of a wafer that has been previously doped at a certain depth. This can allow for a very precise control over etch depth, which has in large part led to microfabrication becoming a high yield process.

Anisotropic etchants do no attack heavily doped Si layers (often designated p^+), and severe drops in etch rate result when the p-type layer is reached. As boron is most frequently used to create p-type silicon, this process is often called a *boron etch stop*. According to the anisotropic etching model of Siedel *et al.* the p-type layer is electron deficient, and there are no electrons available to react with water at the surface. (According to this model, the reduction of water is the rate-limiting step in the etching process.) One disadvantage of a boron etch stop is that the high

level of p-type doping, on the order of $5 \times 10^{18}/\text{cm}^3$, is not compatible with CMOS standards for integrated circuit fabrication.

One technique that is compatible with CMOS standards is called *electrochemical etch stop*. In this particular etch stop an n-type layer is grown on a p-type Si substrate, creating a p-n junction. The required level of doping is very light compared to the boron etch stop method. During etching, an electric potential is applied across the p-n junction creating a reverse-bias diode. The diode keeps current from flowing across the junction, and etching of the p-type substrate can occur readily. As soon as the etching reaches the n-type layer, however, the diode vanishes and current starts flowing. The newly freed electrons oxidize the Si at the surface, forming SiO_2 . Since silicon dioxide etches very slowly in an alkaline medium, the etching stops almost immediately.

4.2.2 Dry etching

In contrast to wet etching, which employs etchants in aqueous solution form, **dry etching** delivers the chemically reactive species to the etching surface in gaseous form, or within an ionized gas, called a *plasma*. In dry etching the gas or plasma bombards the etching surface, producing a sputtering-like effect. Hence, dry etching actually consists of a combination of physical and chemical etching mechanisms. This bombardment also gives the etching process a directional component, and dry etching techniques have become the standard for creating near vertical sidewalls with large aspect ratios.

An example of an etchant used in dry etching is xenon diflouride (XeF_2). XeF_2 is a highly selective etchant that can etch silicon or polysilicon without etching metals, silicon dioxide, or many other structural layers. This selectivity makes XeF_2 vapor a valuable etchant for the release step in surface micromachining processes in which polysilicon is the sacrificial layer.

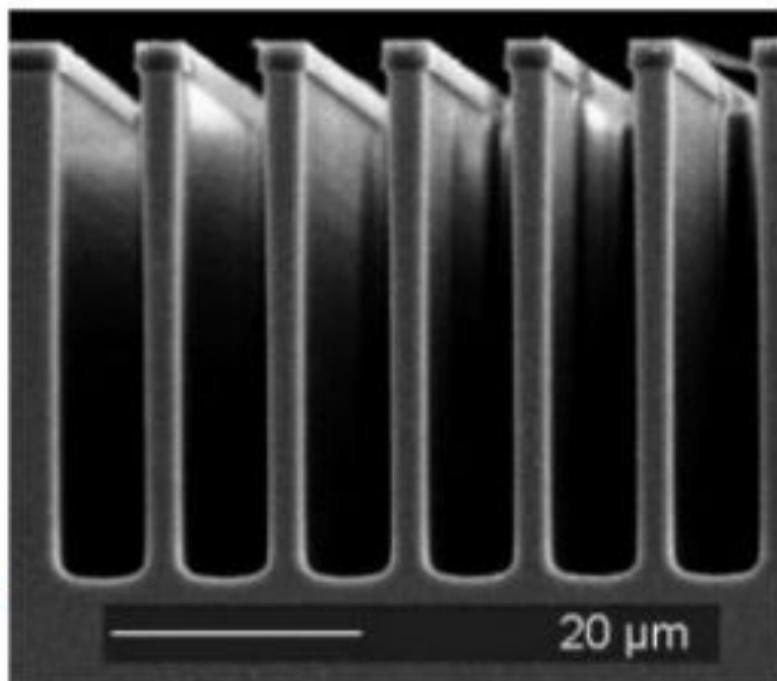
Dry etching

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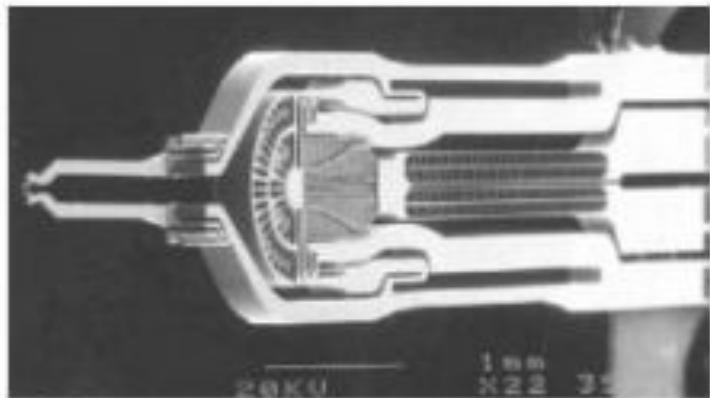
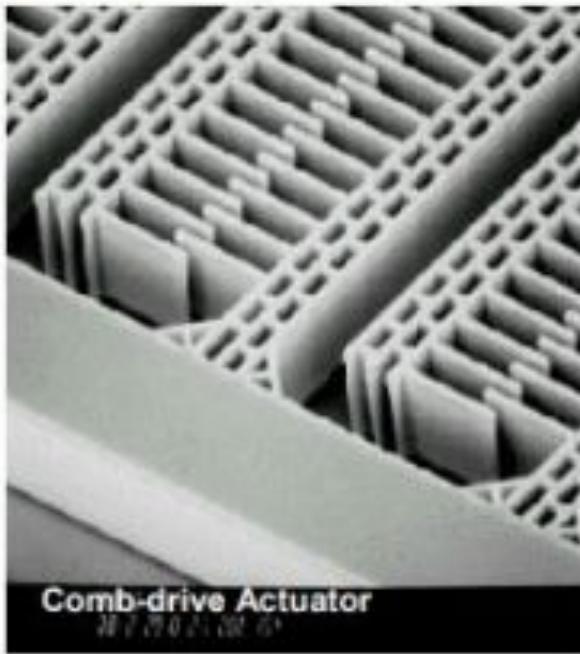
Reactive ion etching (RIE)

In the limit of low pressures, plasma etching can take on much higher degrees of directionality, especially when the ions are directed normal to the surface. This process has become known as reactive ion etching, or RIE.

RIE is capable of creating features with high aspect ratios and nearly vertical sidewalls of high surface quality

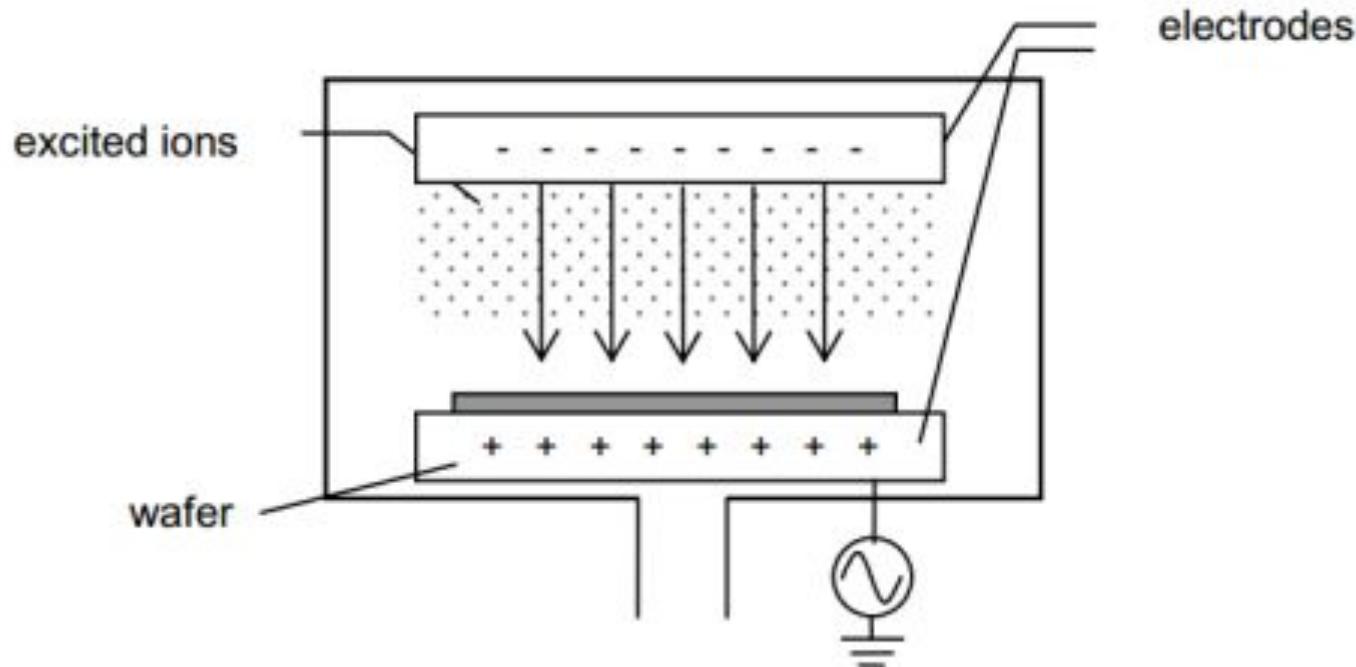


DRIE Examples



Keller, MEMS Precision
Instruments

RIE is typically done by bombarding wafers with heavy ions such as Ar ions in the presence of an energetic plasma. Since the ions are directed toward horizontal surfaces, they typically do not hit the sidewalls during etching. It is by this mechanism that vertical walls are produced.



A schematic of an RIE chamber. Electrodes produce an RF electric field that excites ions and directs them toward the surface of the wafers

Plasma etching

In **plasma etching**, the chemically reactive gas is ignited by an RF (radio frequency) electric field, usually in the range of 10-15 MHz. The reactive chemical species is contained within a plasma inside a vacuum chamber where the surface to be etched also resides. The plasma provides the necessary energy for, or “excites” the reactive gas in order to etch the wafer.

One variant of plasma etching called **plasma ashing** is commonly used to remove photoresist from wafers after completing photolithography steps. In this process an oxygen plasma converts the polymer that makes up the photoresist into carbon dioxide and water vapor, which are then removed by the vacuum pump of the ashing system.

Backside processing

Many MEMS devices are fabricated using both sides of the substrate. A good example is a bulk micromachined MEMS pressure sensor. (Fig. 4.19.) In this device a thin diaphragm is created by etching through the bottom of the wafer. Etching through the bottom of the wafer in this way is an example of **backside processing**. Piezoresistive sensing elements and metal interconnects are also needed for the device, but these are processed from the top.

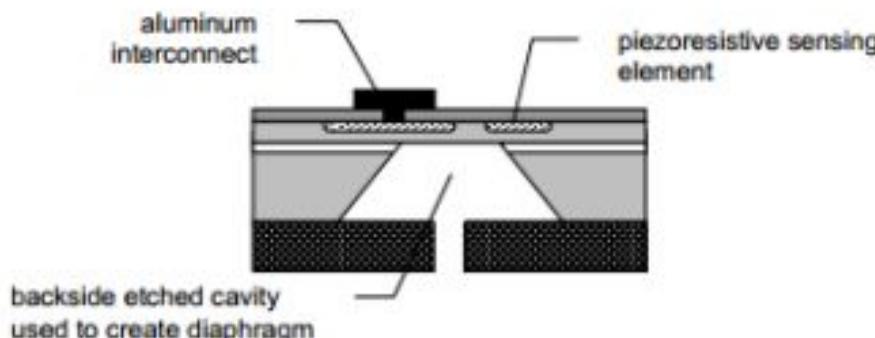
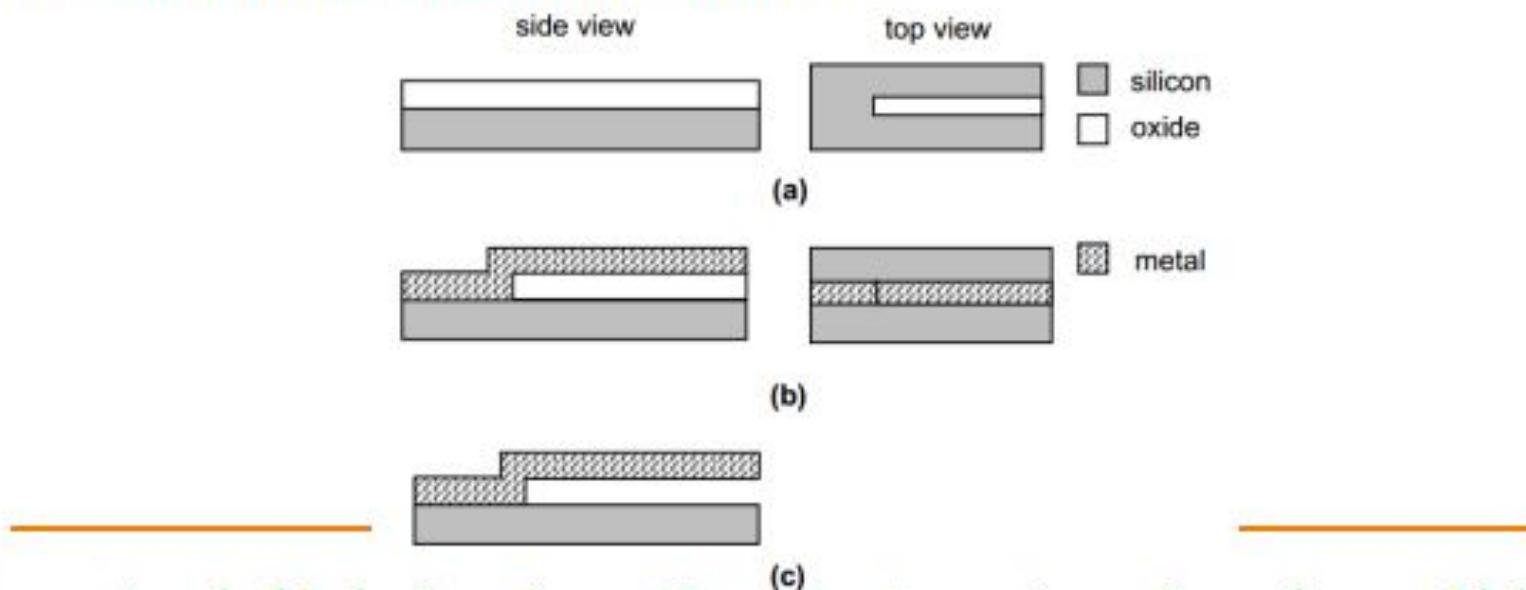


Fig. 4.19. Bulk micromachined pressure sensors are examples of devices requiring backside processing.

Surface micromachining

Surface micromachining (SMM) is a process that uses thin-film deposition, patterning via photolithography, and chemical etching to build mechanical structures on top of a substrate, typically a silicon wafer. It is a layered fabrication process in which some layers form structural elements and others are etched away.

The layers are referred to as structural layers and sacrificial layers, respectively, and form the building blocks of the process. The typical process of SMM is first to deposit a layer, then pattern it, and finally chemically etch away unwanted material. This set of steps can be repeated several times in order to create complicated structures, often with moving parts.



Process steps in fabrication of a cantilever structure using surface micromachining

High-aspect-ratio (LIGA and LIGA-Like) technology

- LIGA is a German acronym that stands for Lithographie, Galvanoformung and Abformung.
- When translated it means lithography, electroplating and molding.

- Two main types of LIGA Technology: X-ray LIGA and Extreme Ultraviolet (EUV) LIGA.
- X-ray LIGA can fabricate with great precision high aspect ratio microstructures.
- EUV LIGA can fabricate lower quality microstructures.

- LIGA is a hybrid fabrication technique
- The LIGA Process
 - Lithography
 - ✖ Electron beam lithography
 - ✖ Focused ion beam lithography
 - ✖ Optical and exciter laser lithography
 - ✖ Deep X-ray lithography using synchrotron radiation
 - Electroplating
 - ✖ metalized layer (seed layer)
 - Molding
 - ✖ Machining process to remove overplated metal region

3.3.3 High-Aspect-Ratio (**LIGA** and **LIGA-Like**) Technology

There is a critical need to develop the fabrication technologies allowing one to fabricate high-aspect-ratio microstructures and microdevices. The **LIGA** process, which denotes Lithography–Galvanoforming–Molding (in German **Lithografie–Galvanik–Abformung**), is capable of producing three-dimensional microstructures of a few centimeters high with the aspect ratio (depth versus lateral dimension) of more than 100. This ratio can be achieved only through bulk micromachining using wet *anisotropic* etching.

The **LIGA** technology is based on the x-ray lithography which guarantees shorter wavelength (from few to ten Å which lead to negligible diffraction effects) and larger depth of focus compared with optical lithography. The ability to fabricate microstructures and microdevices in the centimeter range is particularly important in the actuators applications since the specifications are imposed on the rated force and torque developed by the microdevices. Due to the limited force and torque densities, the designer faces the need to increase the actuator dimensions. The **LIGA** and **LIGA-like** processes are based on deep x-ray lithography and electroplating of metal and alloy structures, allowing one to achieve structural heights in the centimeter range [32-35]. This type of processing expands the material base significantly and allows the fabrication of new high-performance electromechanical microtransducers.

Figure 3.3.7 illustrates the basic sequential processes (steps) in LIGA technology. Here, the x-ray lithography is used to produce patterns in very thick layers of photoresist. The x-rays from a synchrotron source are shone through a special mask onto a thick photoresist layer (sensitive to x-rays) which covers a conductive substrate (step 1). This photoresist is then developed (step 2). The pattern formed is electroplated with metal (step 3). The metal structures produced can be the final product, however, it is common to produce a metal mould (step 4). This mould can then be filled with a suitable media (e.g., metal, alloy, polymer, etc.) as shown in step 5. The final structure is released (step 6).

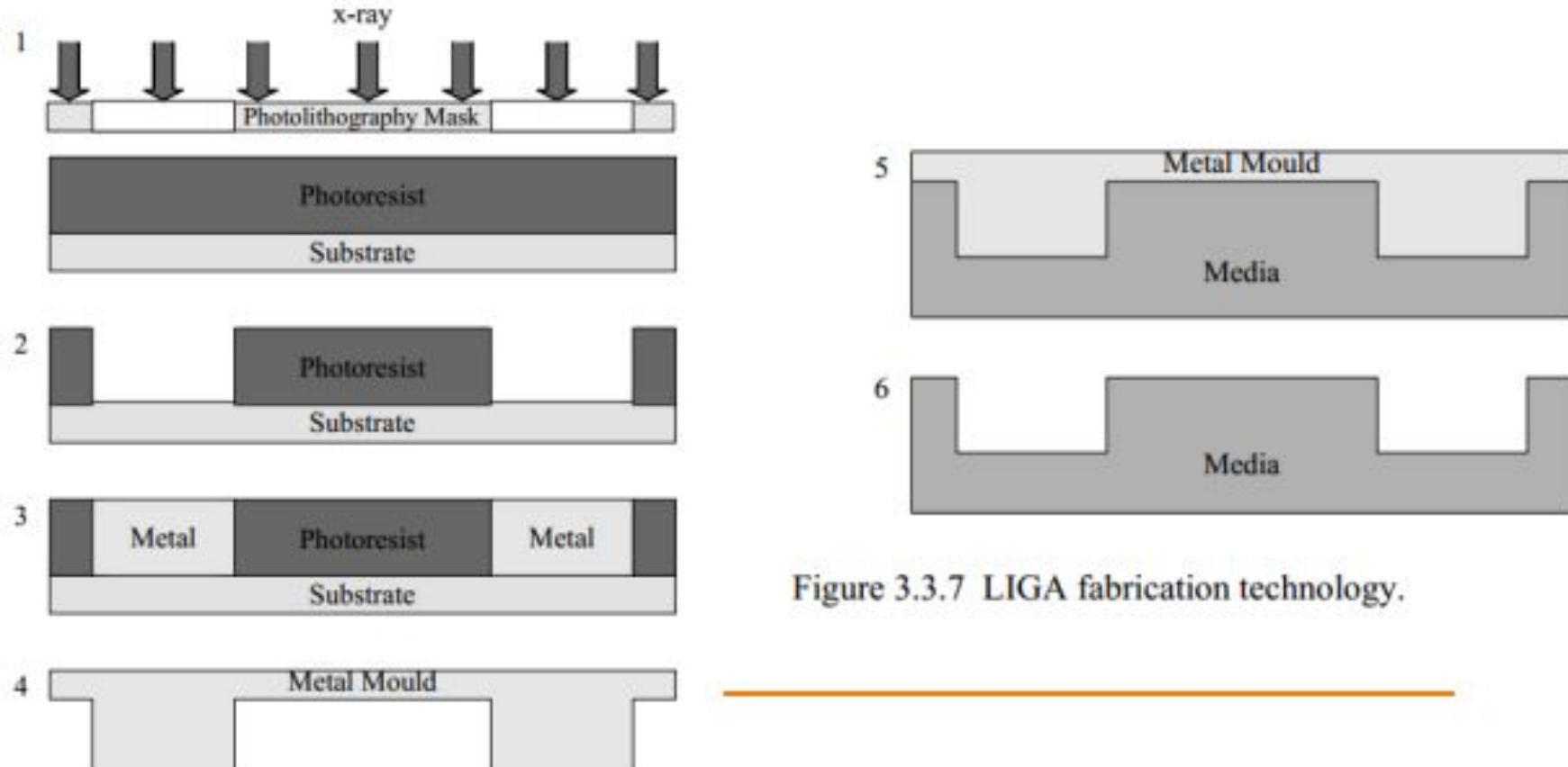


Figure 3.3.7 LIGA fabrication technology.

A critical part of the high-aspect-ratio processes is plating to form the metallic electromechanical microstructures in the mold. Using plating, metal is deposited from ions in a solution following the shape of the plating mold. This is the additive process, and the thickness of the plated metal can be large since the plating rate can be high. A variety of metals (Al, Au, Cu, Fe, Ni, and W) and alloys (NiCo, NiFe, and NiSi) can be deposited or codeposited. It is important that roughness (smoothness) of the reflective metal surfaces with the desired shape can be achieved even for optical applications. Electroplating (well-known from chemistry and covered in Chapter 8) and electroless plating (reduction of the metal ions occurs by the chemical reaction between a reducing agent and metal ion on a properly activated substrate) are the commonly used plating processes. The metal seed layer can be deposited and removed from the substrate or sacrificial layer. The plating rate and the grain size are controlled by the current density, temperature, duty cycle, etc. (see Chapter 8).

18NTO308T Smart Sensor Systems

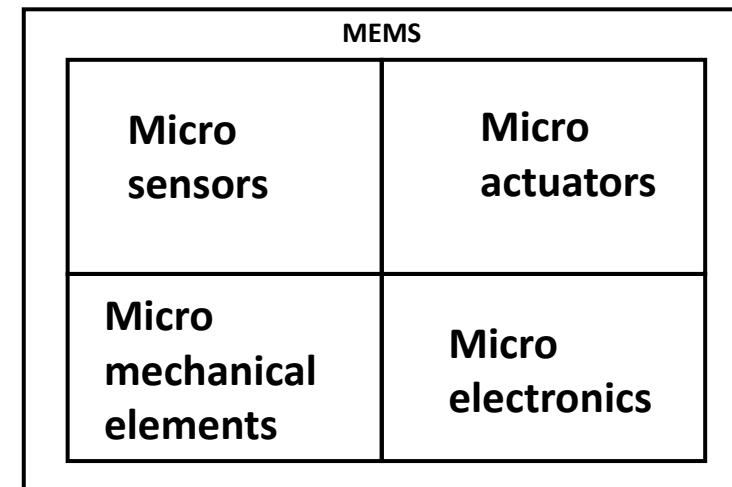
UNIT V

Lecture -1

Fundamentals of MEMS/ fabrication;
Frequently Used Microfabrication Processes

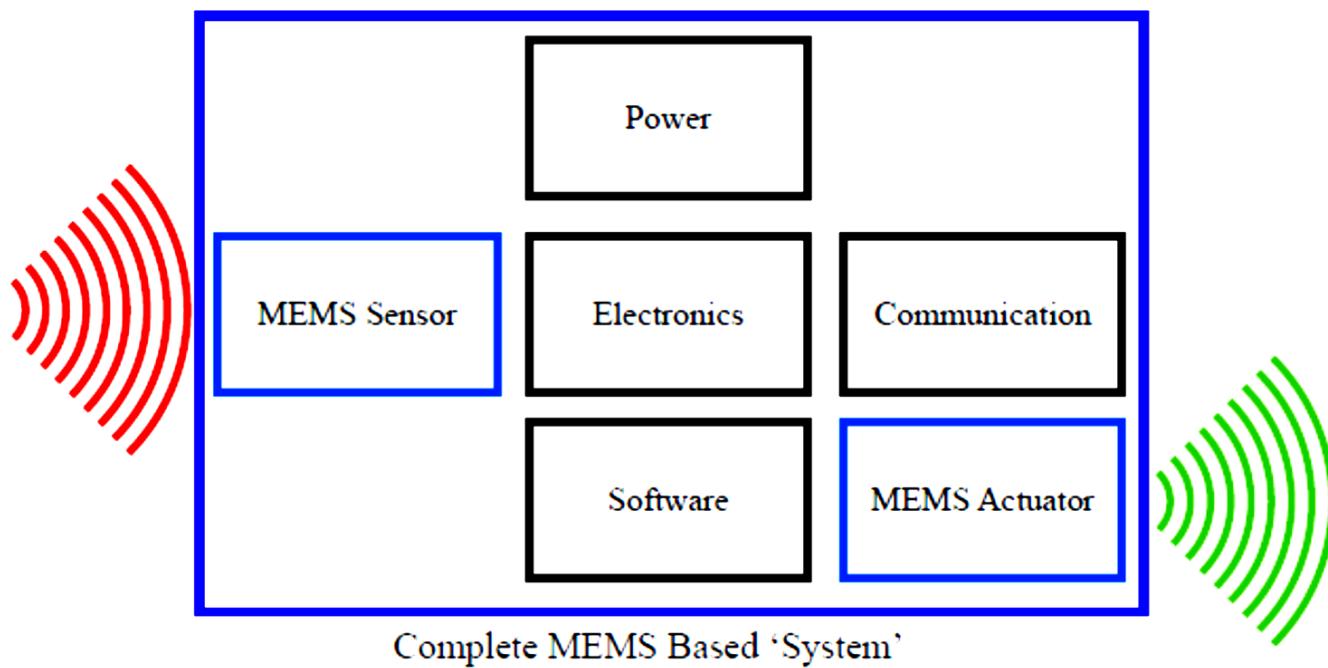
MEMS ***(MicroElectroMechanicalSystems)***

- Micron sized electronic devices with signal processing circuits integrated together typically on a ‘Silicon’ substrate to perform a task.
- MEMS is an integration of Micro sensors, micro actuators, micro mechanical elements and micro electronics on a single silicon platform
- Microelectromechanical systems are also referred to as:
 - Micromachines (Japan)
 - Micro System Technology (MST) (Europe)
 - Microsystems
 - Micro Sensors and Actuators
 - Micro Transducers
- Features:
 - Micro electronics
 - Multiplicity
 - Miniaturization

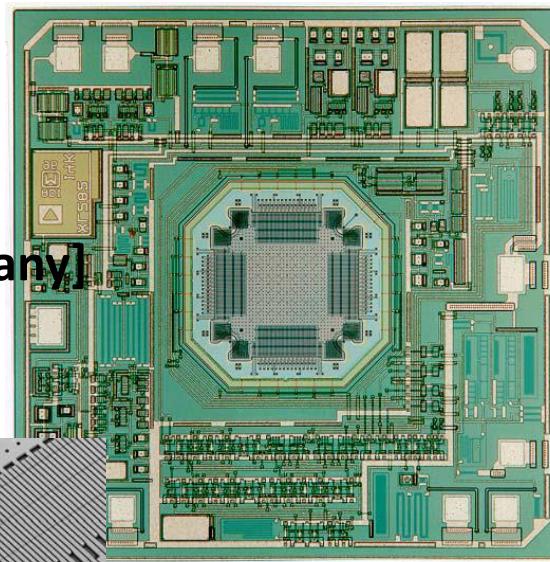
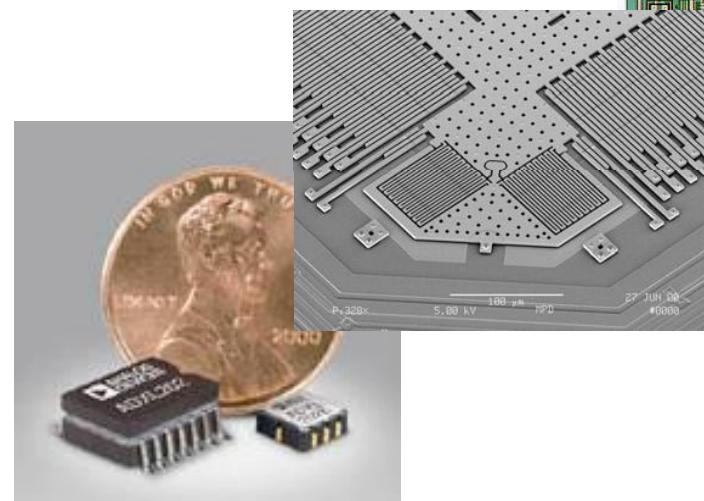


What are MEMS?

The term MEMS generally refers to the micro-scale ‘components’ or micro-scale ‘devices’ within a system. Not the entire system itself. In this sense, the name MEMS is somewhat misleading. In order to create a completely functioning ‘System’ that makes use of MEMS, the system will require various other sub-systems, such as: power, microelectronics, communication and software.



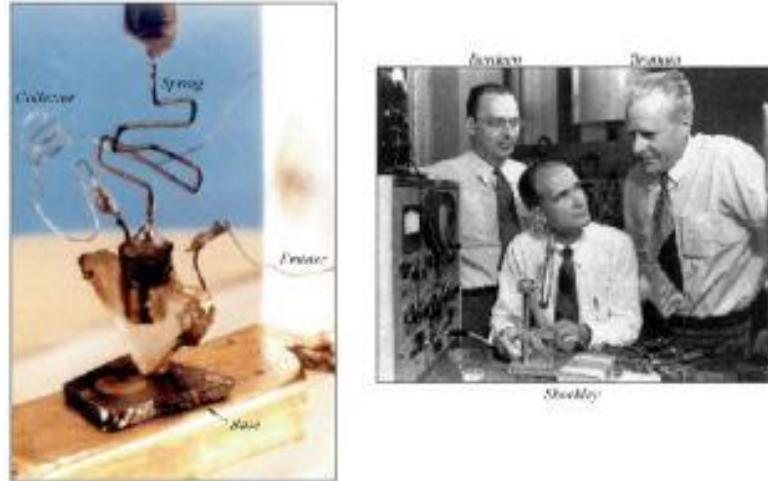
**Accelerometer,
[Analog Devices-company]**



History

- 1st Transistor was designed by “William Shockley, John Bardeen and Walter Brattain” on 1947 in Bell telephone lab, for which they got Nobel Prize on 1956

The first point contact transistor
William Shockley, John Bardeen, and Walter Brattain
Bell Laboratories, Murray Hill, New Jersey (1947)



- In 1953, Silicon substrate surface oxidation was demonstrated, which had opened an window for “Monolithic Transistors”
- 1958 – Integrated circuit (Jack Kilby)
- Gordon Moore (co-founder of Intel) predicted in 1965 that the transistor density of semiconductor chips would double roughly every 18 months.

History of MEMS Technology

- 1959 - “There's Plenty of Room at the Bottom” - Famous talk by Richard P. Feynman
- 1967 - Invention of surface micromachining (Nathanson, Resonant Gate Transistor)
- 1970 - Micromachined silicon pressure sensor demonstrated (Petersen)
- 1970 - First silicon accelerometer demonstrated (Kulite)
- 1977 - First capacitive pressure sensor (Stanford)
- 1984 - First polysilicon MEMS device (Howe, Muller)
- 1988 - Rotary electrostatic side drive motors (Fan, Tai, Muller)
- 1989 - Lateral comb drive (Tang, Nguyen, Howe)
- 1991 - Polysilicon hinges developed (Pister, Judy, Burgett, Fearing)
- 1992 - Multi User MEMS Process (MUMPs) is introduced by MCNC, (now MEMSCAP)
- 1993 - First surface micromachined accelerometer (ADXL50) sold, (Analog Devices)
- 1998 - Demonstration of DMD (Digital Mirror Device), (Texas Instruments)

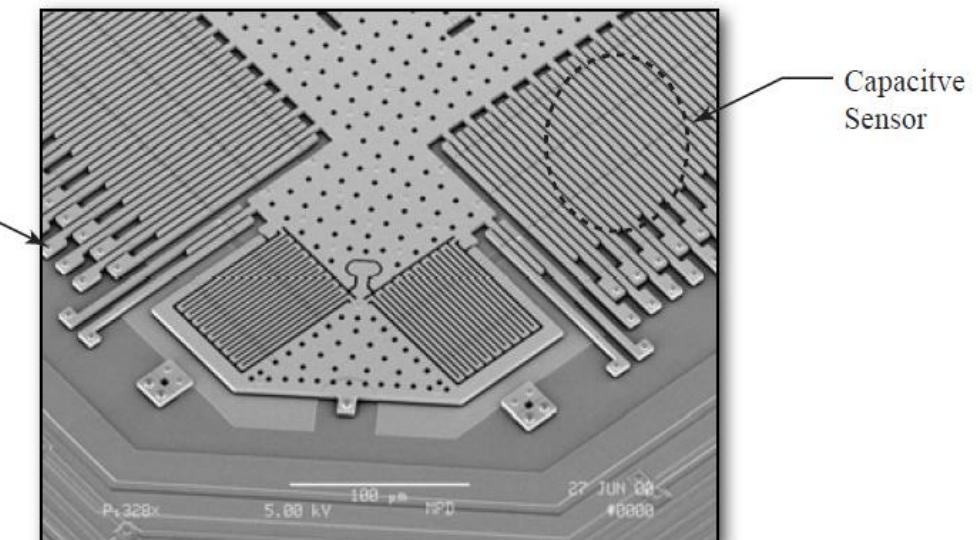
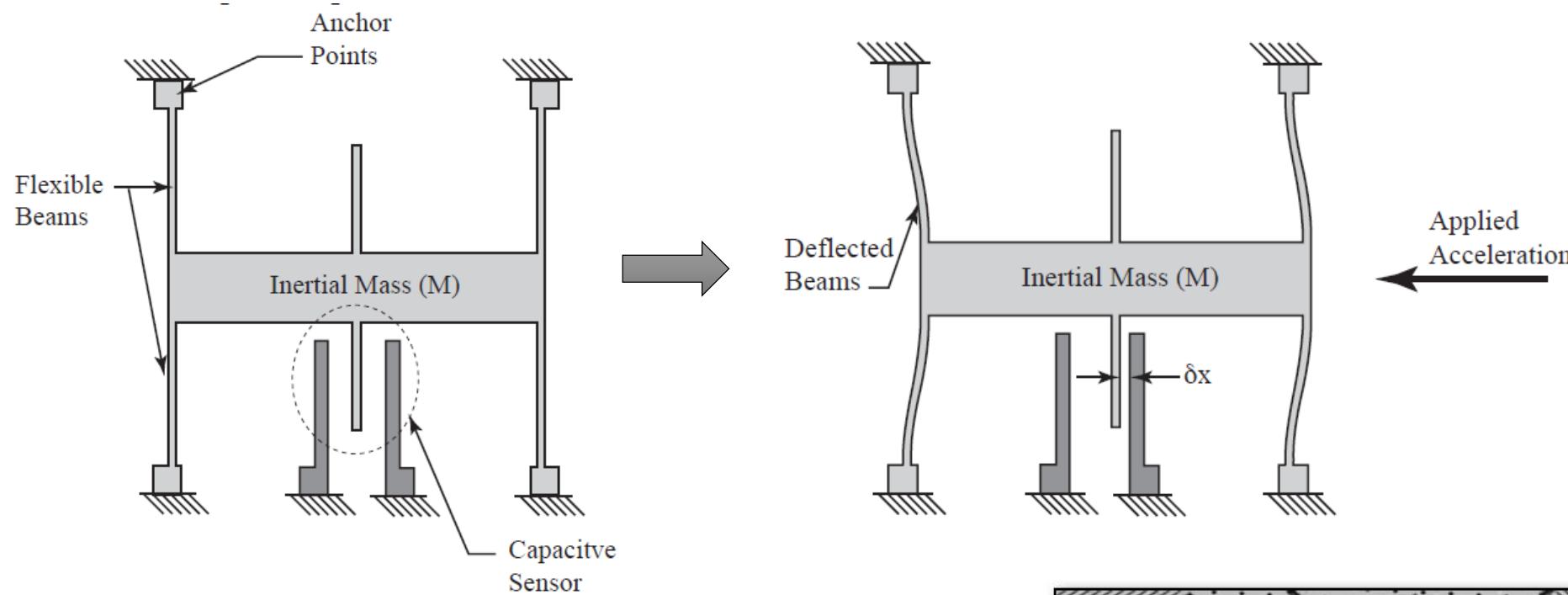
Need for MEMS

- For some applications, scaling devices down to the microscale may allow for some unique advantages. Physical size is only one of many considerations.
- For micro-scale sensors:
 - Higher Sensitivity
 - Better Linearity
 - Better Responsivity
 - Dynamic Range
 - Cost Reduction from Batch Fabrication
- For micro-scale actuators:
 - Dynamic Response Speed
 - Lower Power Consumption
 - Footprint
 - Cost Reduction from Batch Fabrication

How are MEMS made?

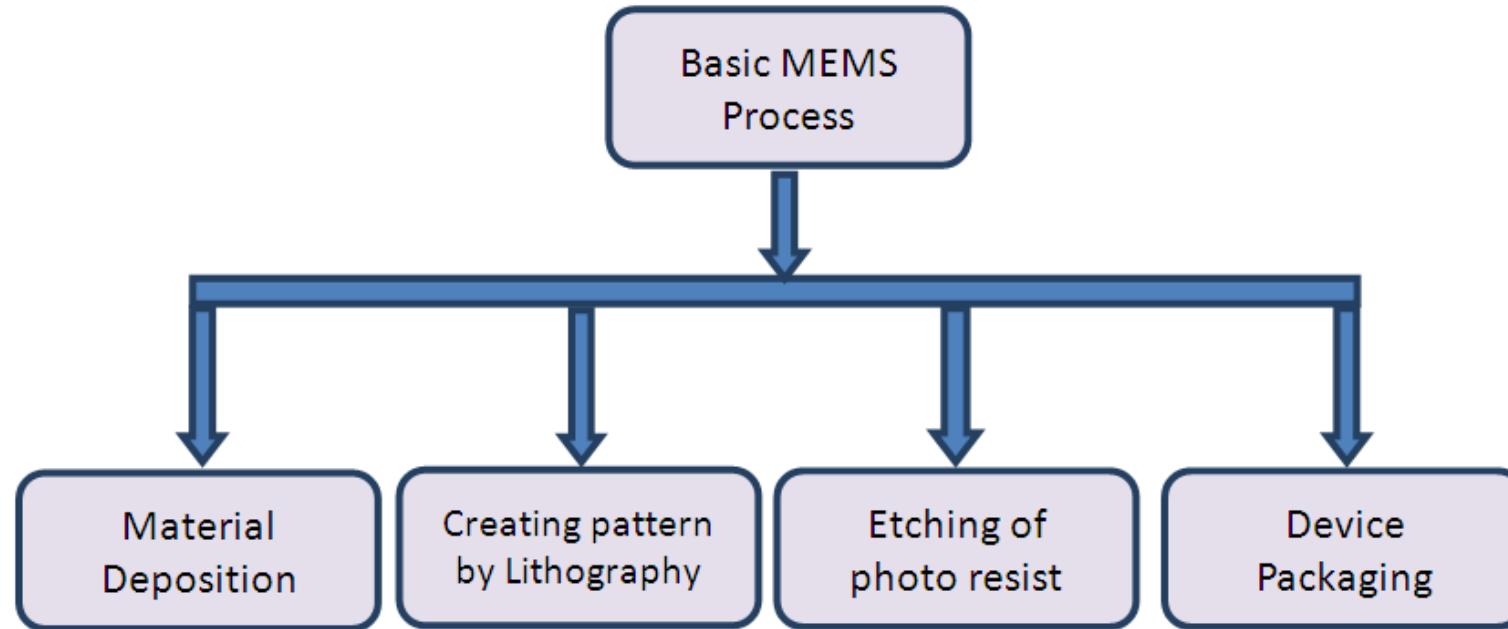
- MEMS are fabricated with a unique set of technologies collectively referred to as ‘microfabrication’ or ‘micromachining’.
- These methods are quite different from macro-scale techniques.
Due to their small size, standard machine tools cannot be used to machine MEMS features.
- Micromachining technology is closely related to IC (integrated circuit) fabrication, with some notable differences.
- There are two main areas of micromachining:
 - Surface Micromachining, which is based on the successive deposition and etching of thin films of material such as silicon nitride, polysilicon, silicon oxide and gold.
 - Bulk Micromachining, which is based on the etching and bonding of thick sheets of material such as silicon oxides and crystalline silicon.

MEMS Working (Accelerometer Principle of Operation)



2-Axis Accelerometer, [Analog Devices]

Fundamentals of MEMS fabrication: Introduction and description of basic processes



Unit V

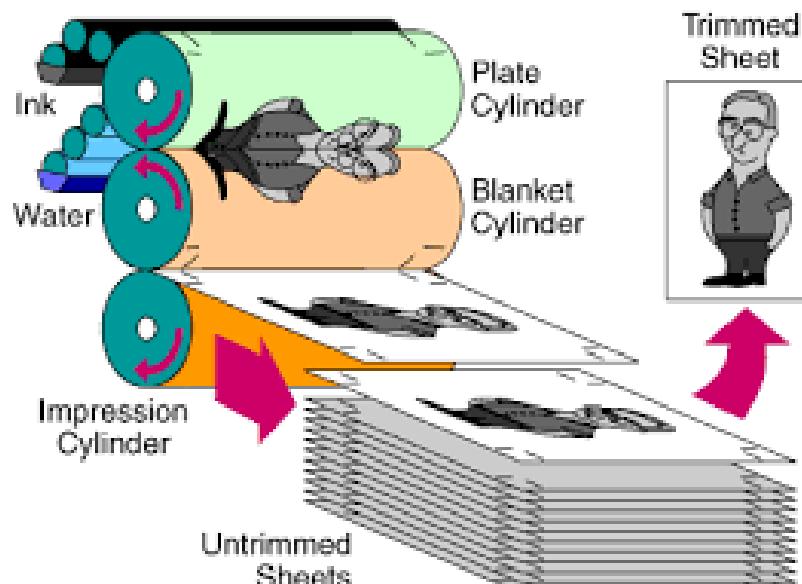
Lecture 2

Topics

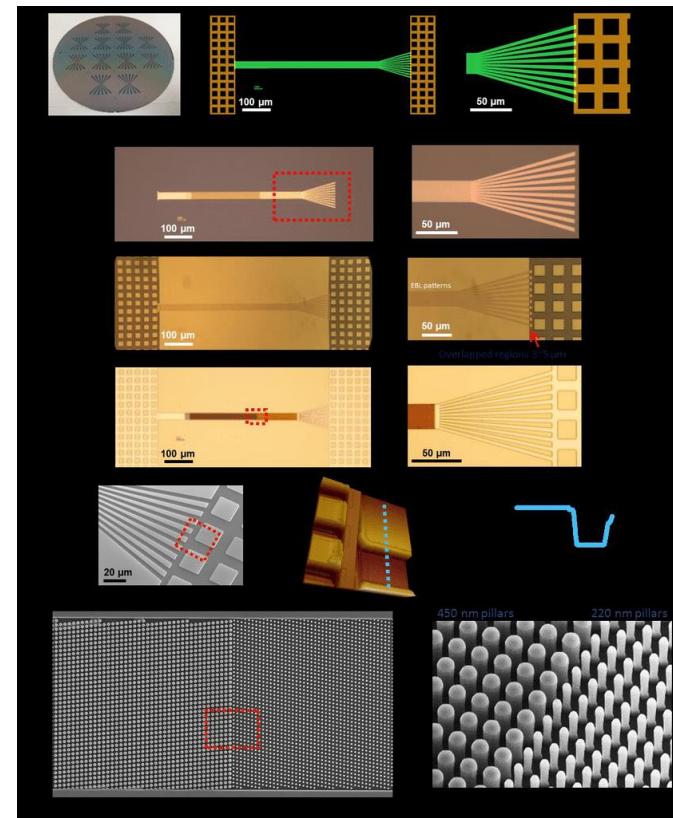
1. Lithography, thin film Deposition
2. Oxidation, Etching (wet and dry)

Lithography Process

- Lithography = Photoengraving
- Lithography in the MEMS context is typically the transfer of a pattern to a photosensitive material by selective exposure to a radiation source such as light.



Offset Lithography



Mixed lithography process for the fabrication of nanopillar (NP) array channels.

Types of lithography :

1. Optical or Photolithography
(Visible, UV, EUV)
2. Soft lithography
3. Electron beam lithography.
4. Ion beam lithography.
5. Ion track lithography.
6. X-ray lithography.
7. Nanoimprint lithography.
(Diblock copolymer, Alumina membrane, Nanochannel glass)
8. Scanning Probe lithography
(voltage pulse, CVD, Local electrodeposition, Dip-pen)

Basic techniques of lithography :

Substrate → Deposition of film → Pattern the film → Etching

Lithography

Masked Lithography

1. Photolithography
2. Projection lithography
3. Deep UV lithography
4. Extreme UV lithography
5. X-ray lithography

Maskless Lithography

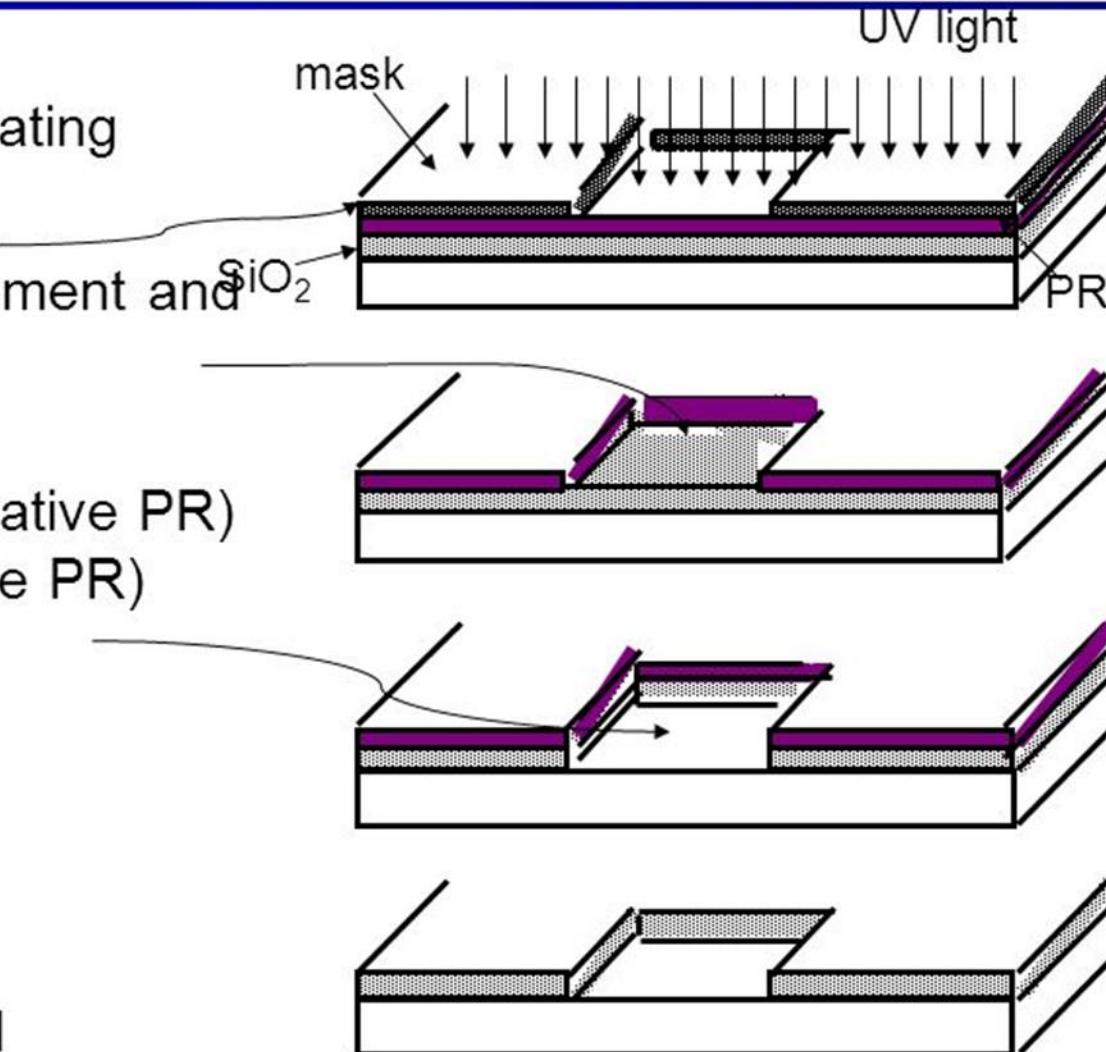
1. Electron beam lithography
2. Focused ion beam lithography
3. Proton beam lithography

Soft lithography

1. Nanoimprint lithography
2. Colloidal lithography
3. Microcontact printing

Patterning - Photolithography

1. Oxidation
2. Photoresist (PR) coating
3. Stepper exposure
4. Photoresist development and SiO_2 bake
5. Acid etching
 - Unexposed (negative PR)
 - Exposed (positive PR)
6. Spin, rinse, and dry
7. Processing step
 - Ion implantation
 - Plasma etching
 - Metal deposition
8. Photoresist removal



Important steps in lithography process

Process steps

- Surface cleaning
- Barrier layer formation (Oxidation), optional
- Spin coating with photoresist
- Soft baking
- Mask alignment and Exposure
- Development
- Hard baking
- Post process cleaning
- Etch back or liftoff

- Surface cleaning

Typical contaminants that must be removed prior to photoresist coating:
dust from scribing or cleaving (minimized by laser scribing) atmospheric dust
(minimized by good clean room practice) abrasive particles (from lapping or
CMP)
lint from wipers (minimized by using lint-free wipers)
photoresist residue from previous photolithography (minimized by performing
Oxygen plasma ashing)
Bacteria (minimized by good DI water system)

Films from other sources

Solvent residue

H₂O residue

Photoresist or developer residue

Oil

Silicone



Oxidation (Barrier layer formation)

Oxidation may be defined as the chemical process in which a substance gains oxygen or loses electrons and hydrogen. When one of the reactants is oxygen, then **oxidation** is the gain of oxygen.

Oxidation of silicon

It occurs immediately to form amorphous **silicon** dioxide film (called native oxide, usually 2-3 nm thick) by exposing a **silicon** surface to oxygen in atmospheric environment.

Thermal Oxidation

In microfabrication, thermal oxidation is a way to produce a thin layer of oxide (usually silicon dioxide) on the surface of a wafer. The technique forces an oxidizing agent to diffuse into the wafer at high temperature and react with it.

Thermal Oxidation of silicon

Thermal oxidation of silicon is usually performed at a temperature between 800 and 1200°C, resulting in oxide layer. It may use either water vapor or molecular oxygen as the oxidant. There are two types wet oxidation and dry oxidation.

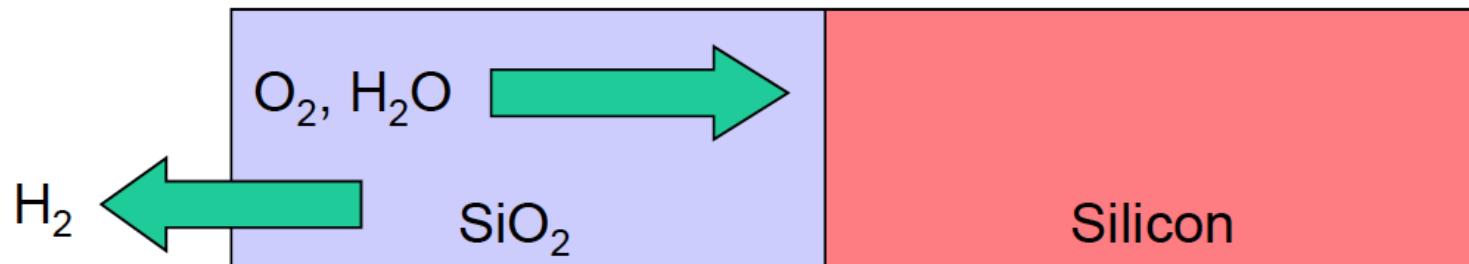
Why thermal Oxidation of silicon

Silicon Dioxide (SiO_2)

- The single thermodynamically stable oxide of silicon.
- Essential to the fabrication of MOS devices.
 - Creates extremely high electronic quality gate oxides.
- Essential to the patterning of silicon for high temperature processing.
 - Photoresist cannot handle temperatures much above 150°C.
 - Patterned SiO_2 can be used for masking diffusions, etches, and other processes up to temperatures of >1400°C.
- *The extreme purity and perfection of the Si/ SiO_2 interface is the ultimate reason why silicon has been the #1 semiconductor for microelectronics.*
 - And is likely to remain so...

Oxidation of Silicon

- Carried out at temperatures of 900 – 1200°C.
- Dry oxidation: N₂ carrier gas + O₂
 - O₂ must diffuse through the growing SiO₂ layer.
- Wet oxidation: N₂ carrier gas + O₂ + H₂O (sat. vapor)
 - H₂O must diffuse through the growing SiO₂ layer.
 - Diffusion of H₂O is much faster than O₂; wet oxides grow faster.
 - H₂ must diffuse back out; usually very rapid and not a limiter.
- SiO₂ grows from the SiO₂/Si interface:
 - Oldest SiO₂ remains on the surface.
 - Youngest SiO₂ finishes at the SiO₂/Si interface.



Photoresist

It is a soft material used in the micro/nano fabrication process for pattern transfer, which changes its chemical properties upon exposure to different radiations like light, x-ray, ion, electron and proton beams

Chemical composition

Photoresists are composed of adhesive agents, sensitizers and solvents.

Binders (~20%)

As a binder Novolac is used, which is a synthetic resin to control the thermal characteristics of the resist.

Sensitizer (~10%)

Sensitizers define the photosensitivity of the resist. Sensitizers are composed of molecules which affect the solubility of the resist if it is exposed to energetic radiation. Thus the lithography has to take place in areas with ambient light which has a low energy.

Solvents (~70%)

Solvents define the viscosity of the resist. By annealing, the solvent is vaporized and the resist is stabilized.

Two types of photoresist

There are two types of photoresist, positive tone and negative tone resist, which are used in different applications.

Positive tone resist

In positive tone resist, the exposed areas become soluble in the developer solutions because the molecular bonding in the resist material will break upon radiation exposure (e.g. PMMA, ZEP520, AZ)

Negative tone resist

In negative tone resist the exposed areas become insoluble in the developer solution because the polymer chains will crosslink in the resist materials upon radiation exposure. (e.g. HSQ, SU8)

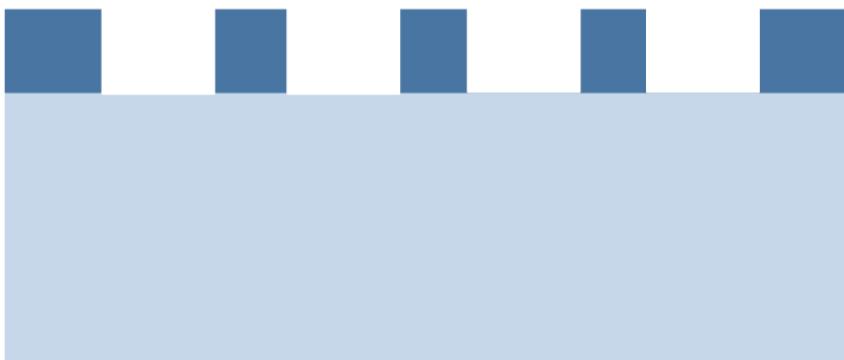
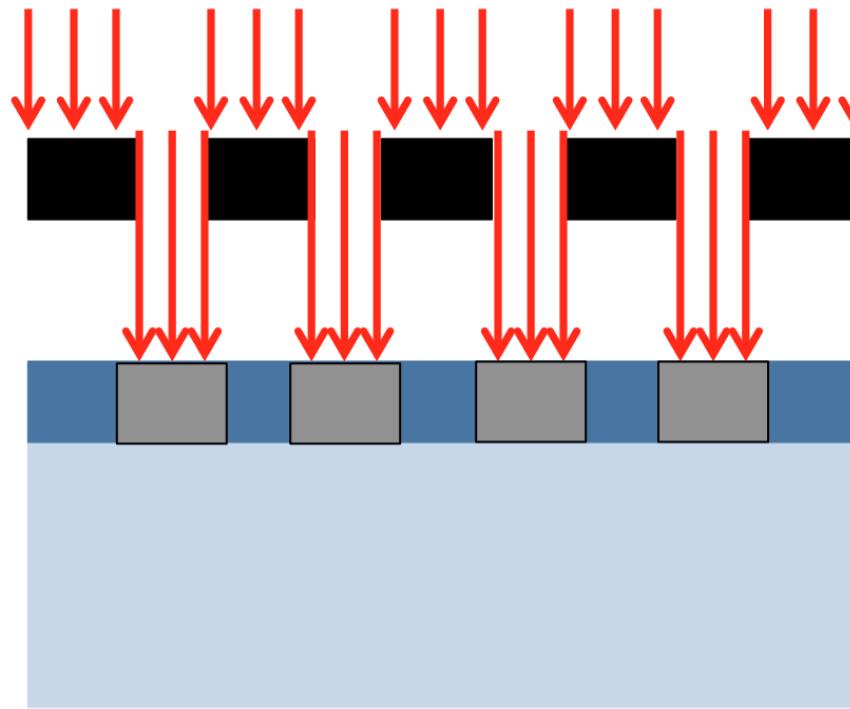
Characteristics of positive resists:

- excellent resolution
- stable against
- developers
- can be developed in aqueous developers
- bad resistance in etching
- or
- or

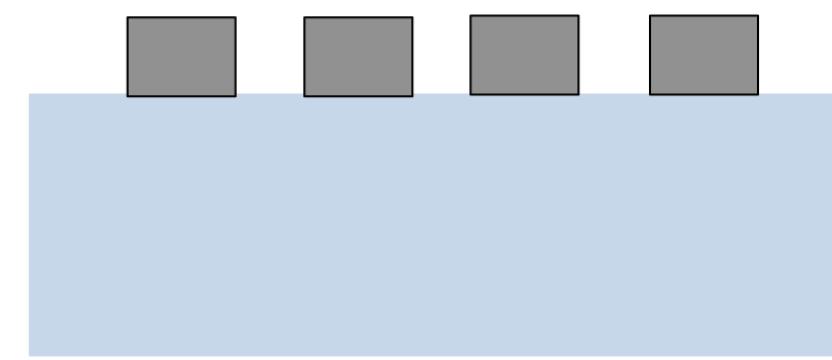
Characteristics of negative resists:

- high sensitiveness
- fair adhesion
- excellent resistance against etch or implantation processes
- cheaper than positive resists
- lower resolution
- organic developers are

Two types of photoresist

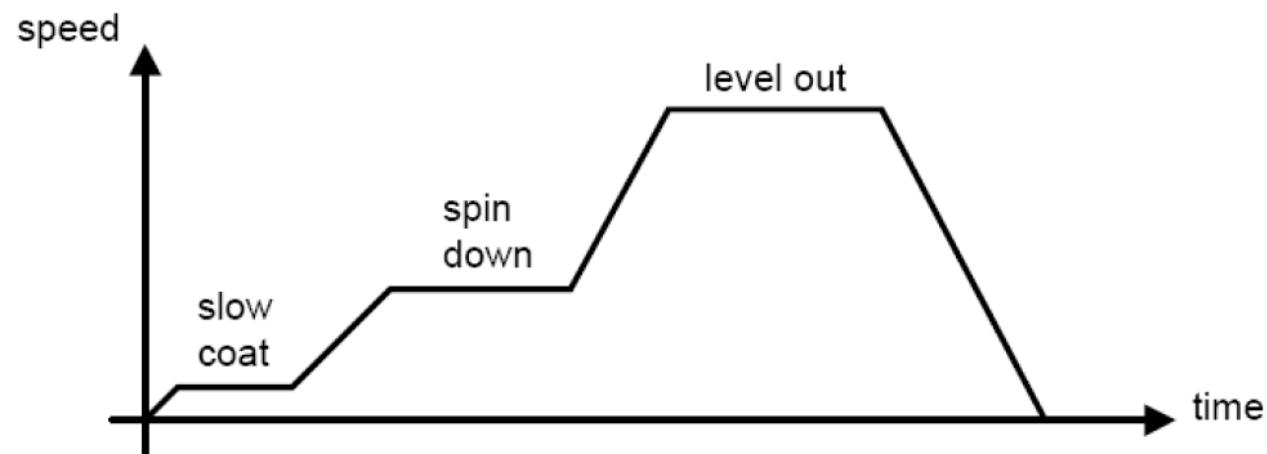
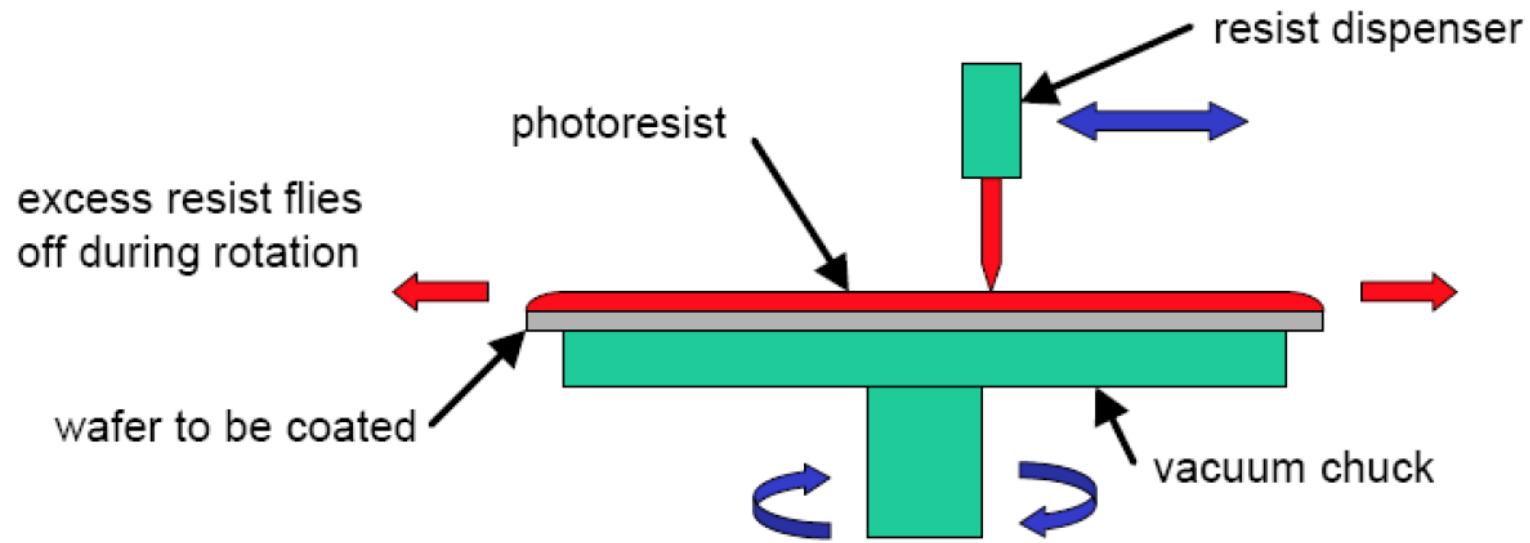


Positive resist



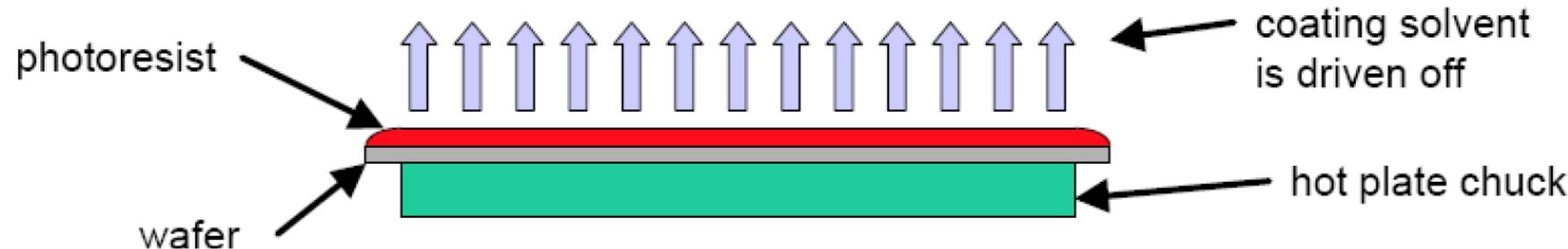
Negative resist

Photoresist Spin Coating

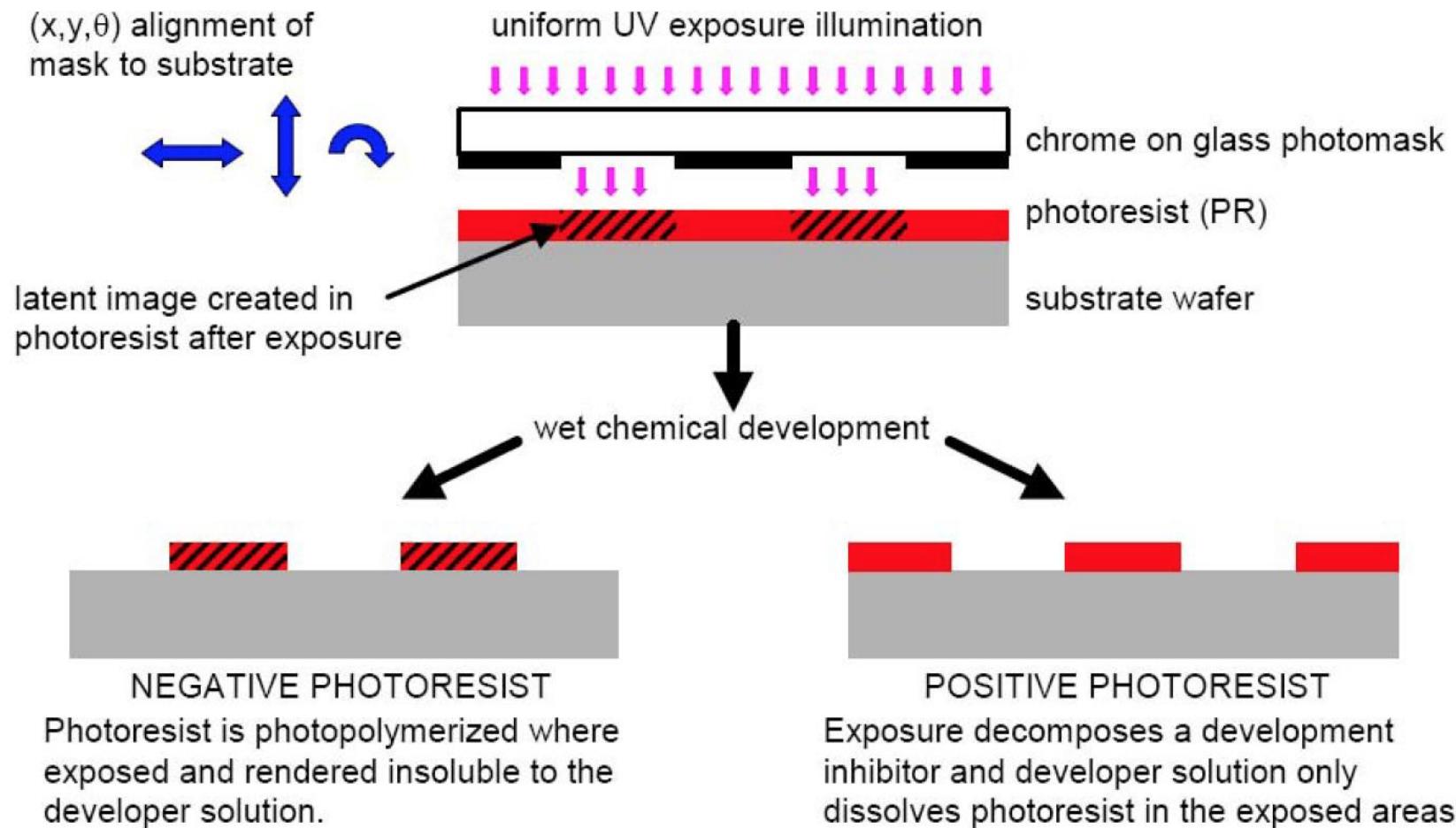


Prebake (Soft Bake) - 1

- Used to evaporate the coating solvent and to densify the resist after spin coating.
- Typical thermal cycles:
 - 90-100°C for 20 min. in a convection oven
 - 75-85°C for 45 sec. on a hot plate
- Commercially, microwave heating or IR lamps are also used in production lines.
- Hot plating the resist is usually faster, more controllable, and does not trap solvent like convection oven baking.



Overview of Align/Expose/Develop Steps



Basics of Photolithography for Processing

- Microfabrication processes:
 - Additive → deposition
 - Subtractive → etching
 - Modifying → doping, annealing, or curing
- Two primary techniques for patterning additive and subtractive processes:
 - Etch-back:
 - photoresist is applied overtop of the layer to be patterned
 - unwanted material is etched away
 - Lift-off:
 - patterned layer is deposited over top of the photoresist
 - unwanted material is lifted off when resist is removed

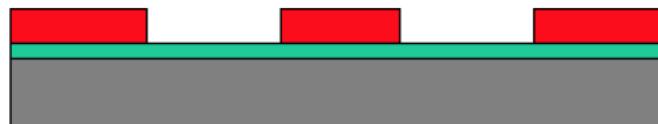
Etch-back

1



deposit thin film of desired material

2



coat and pattern photoresist

3



etch film using photoresist as mask

4



remove photoresist

NOTE: photoresist has same polarity as final film;
photoresist never touches the substrate wafer.

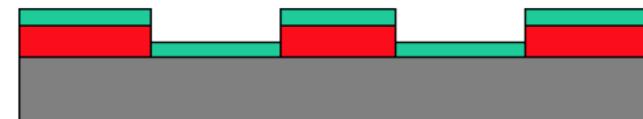
Lift-off

1



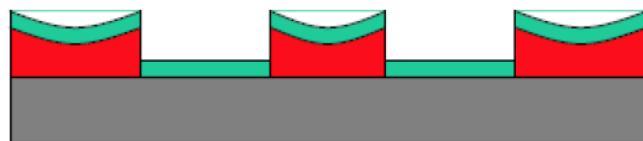
coat and pattern photoresist

2



deposit thin film of desired material

3



swell photoresist with a solvent

4



remove photoresist and thin film above it

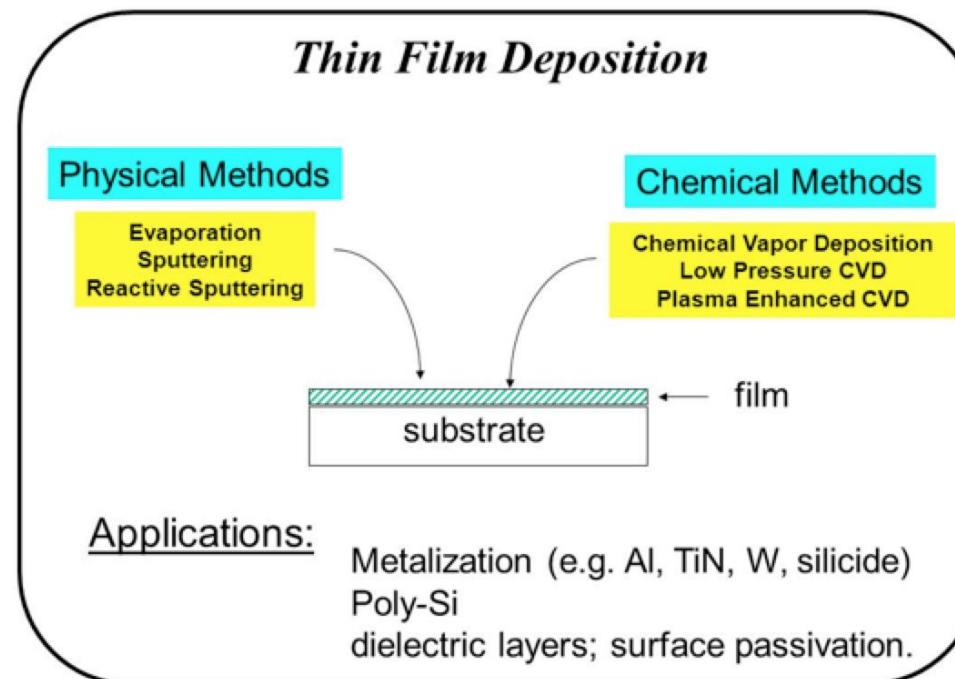
NOTE: photoresist has opposite polarity as final film;
excess deposited film never touches the substrate wafer.

Photoresist Removal (Stripping)

- Want to remove the photoresist and any of its residues.
- Simple solvents are generally sufficient for non-postbaked photoresists:
 - Positive photoresists:
 - acetone
 - trichloroethylene (TCE)
 - phenol-based strippers (Indus-Ri-Chem J-100)
 - Negative photoresists:
 - methyl ethyl ketone (MEK), $\text{CH}_3\text{COC}_2\text{H}_5$
 - methyl isobutyl ketone (MIBK), $\text{CH}_3\text{COC}_4\text{H}_9$
- Plasma etching with O_2 (ashing) is also effective for removing organic polymer debris.
 - Also: Shipley 1165 stripper (contains n-methyl-2-pyrrolidone), which is effective on hard, postbaked resist.

Deposition

It is an additive process by which a thin layer (usually sub micrometer or few micrometer thick) of metallic or dielectric or organic material is coated on the substrate surface



Thin film

Thin film: thickness typically $<1000\text{nm}$.

Special properties of thin films: different from bulk materials, it may be –

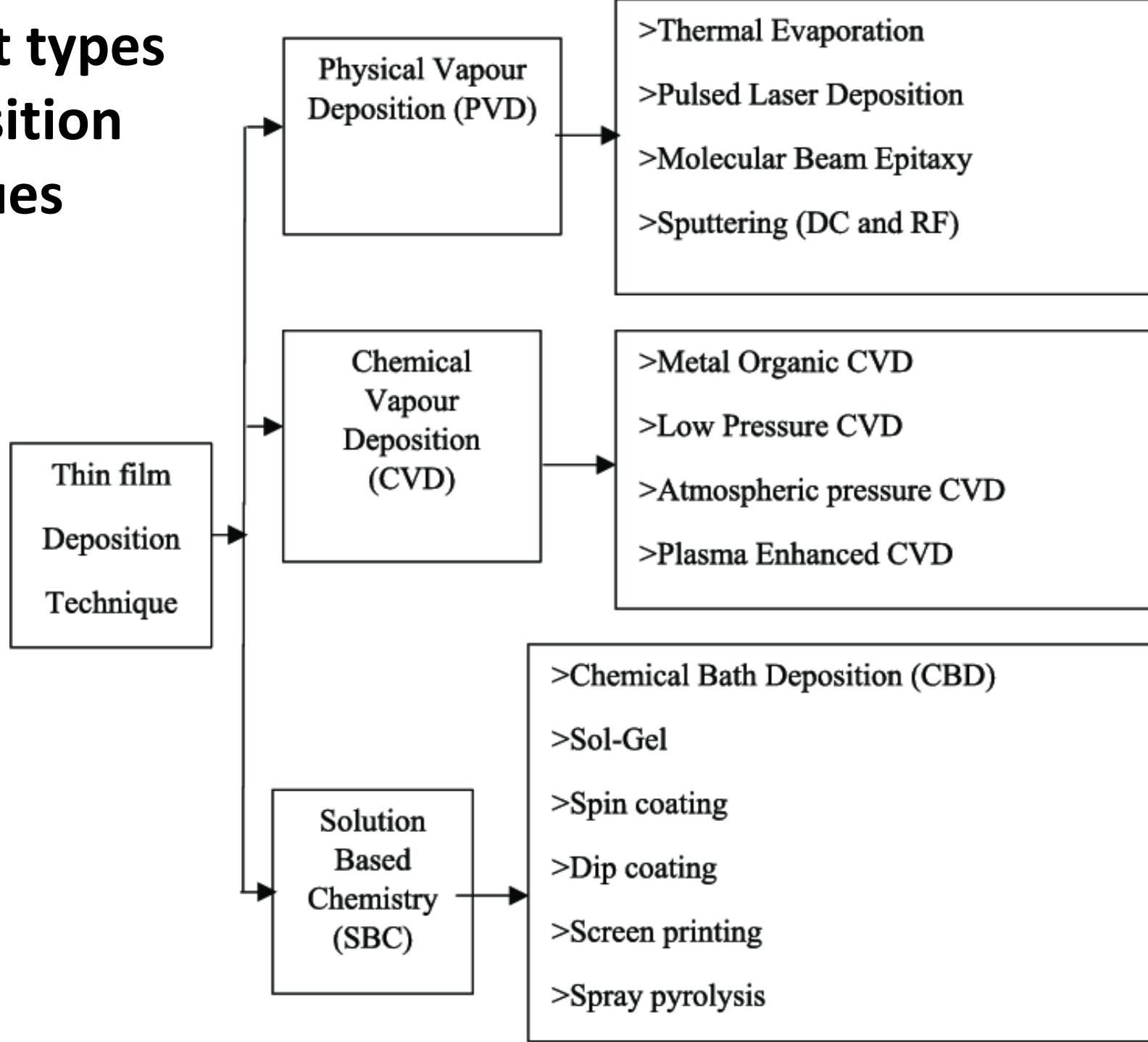
- Not fully dense
- Under stress
- Different defect structures from bulk
- Quasi - two dimensional (very thin films)
- Strongly influenced by surface and interface effects

Typical steps in making thin films:

1. Emission of particles from source (heat, high voltage . . .)
2. Transport of particles to substrate
3. Condensation of particles on substrate

Lithography, thin film deposition and its etching are the three most important processes for micro-nano fabrication.

Different types of deposition techniques



Thin Film Deposition

Thin Film Development Processes

Thin films are deposited by employing the following methods.

- Spin coating
- Thermal oxidation
- LPCVD (Low Pressure Chemical Vapor Deposition)
- PECVD (Plasma Enhanced Chemical Vapor Deposition)
- E-beam evaporation
- Sputtering

Spin Coating

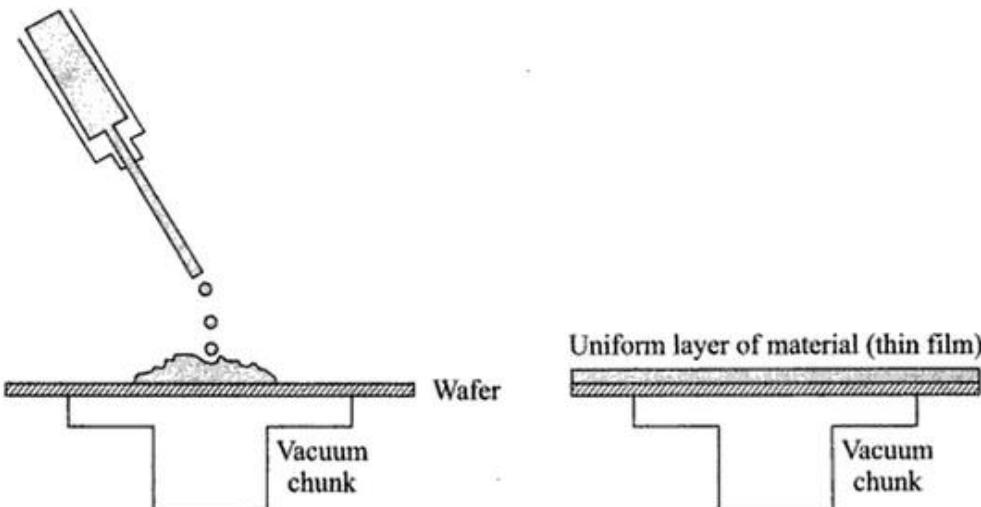
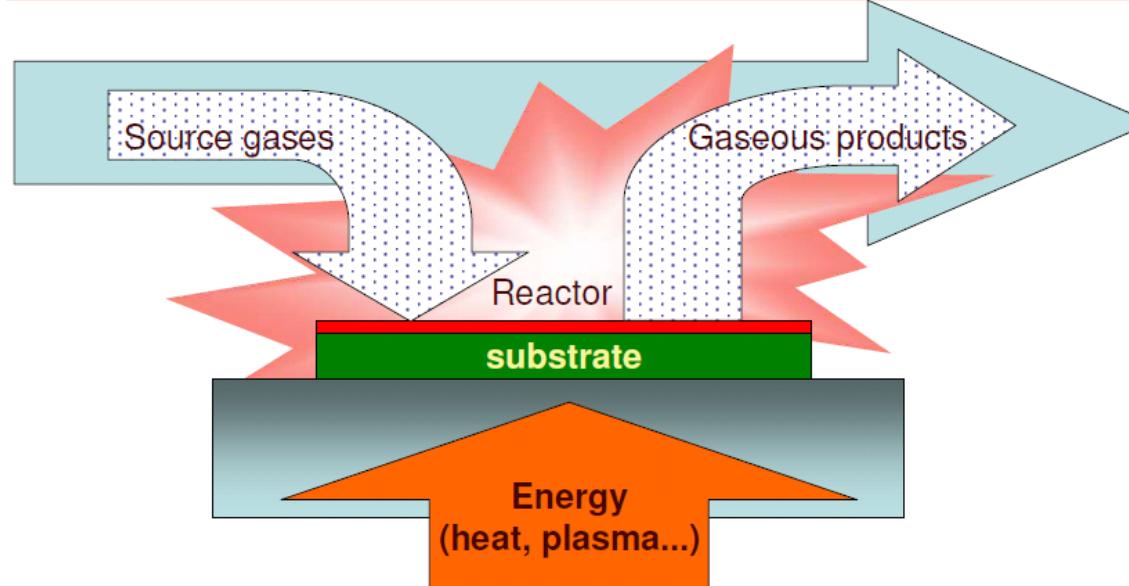


Fig. Spin coating, (a) Before spinning (b) After spinning (MEMS and Nanotechnology Exchange)

The following formula is useful while calculating the time of spin t (seconds), for a given rotational speed w (radians per second).

$$t = \frac{3\mu}{4\rho w^2} \left(\frac{1}{h^2} - \frac{1}{h_0^2} \right)$$

Chemical Vapor Deposition (CVD)



CVD : deposit film through chemical reaction and surface adsorption.

CVD steps:

- Introduce reactive gases to the chamber.
- Activate gases (decomposition) by heat or plasma.
- Gas adsorption by substrate surface .
- Reaction take place on substrate surface, film formed.
- Transport of volatile byproducts away form substrate.
- Exhaust waste.

Chemical vapor deposition (CVD) systems

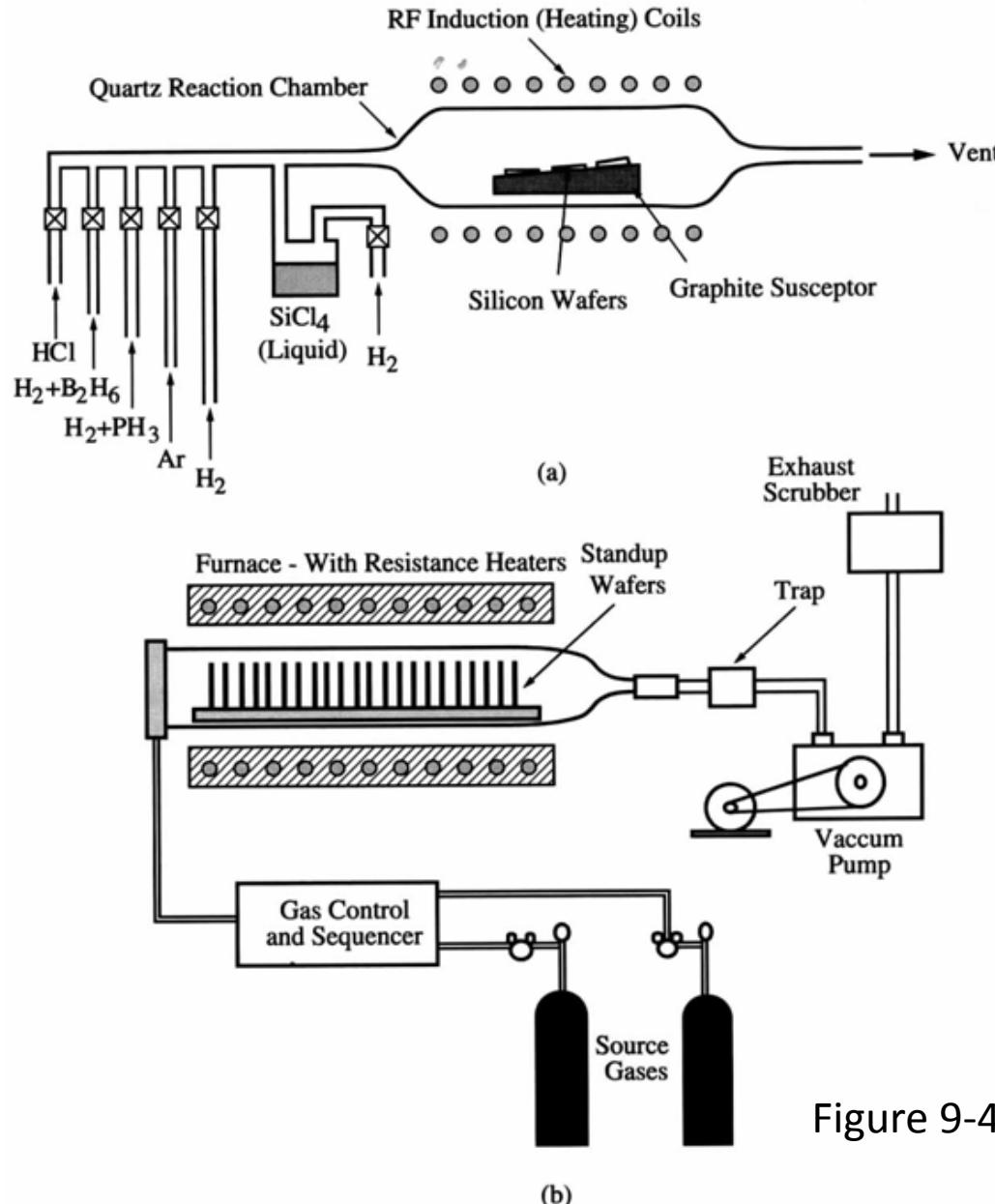
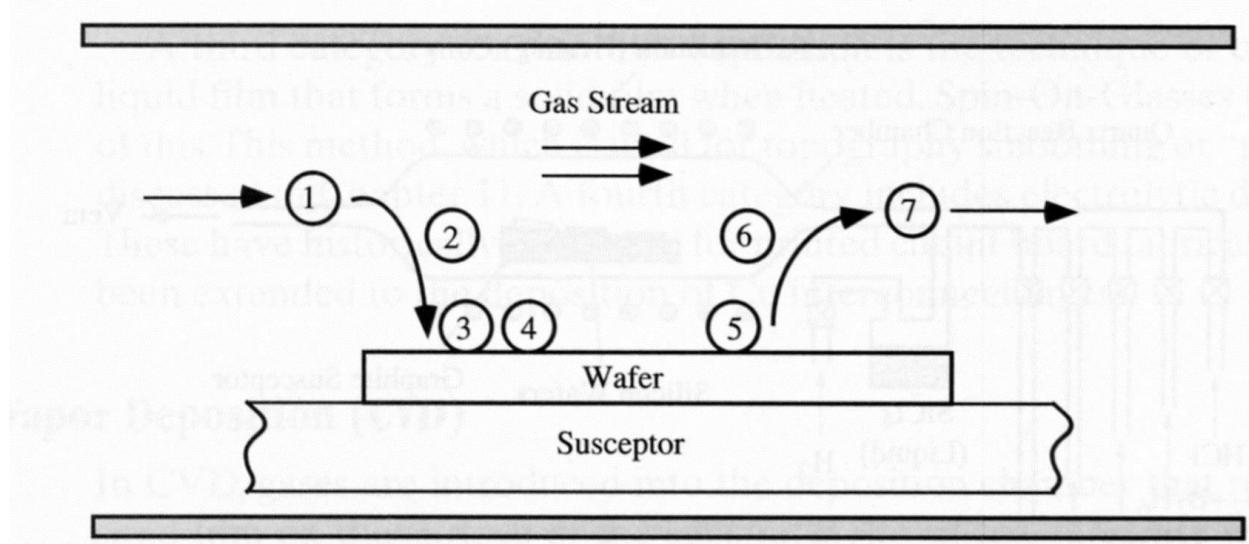


Figure 9-4

Low pressure hot wall system used for deposition of epitaxial silicon.
 $(\text{SiCl}_4 + 2\text{H}_2 \rightarrow \text{Si} + 4\text{HCl})$
e.g. low pressure chemical vapor deposition (LPCVD)

Atmospheric cold-wall system used for deposition of polycrystalline and amorphous films, such as poly-silicon and silicon dioxide.
e.g. plasma enhanced chemical vapor deposition (PECVD)

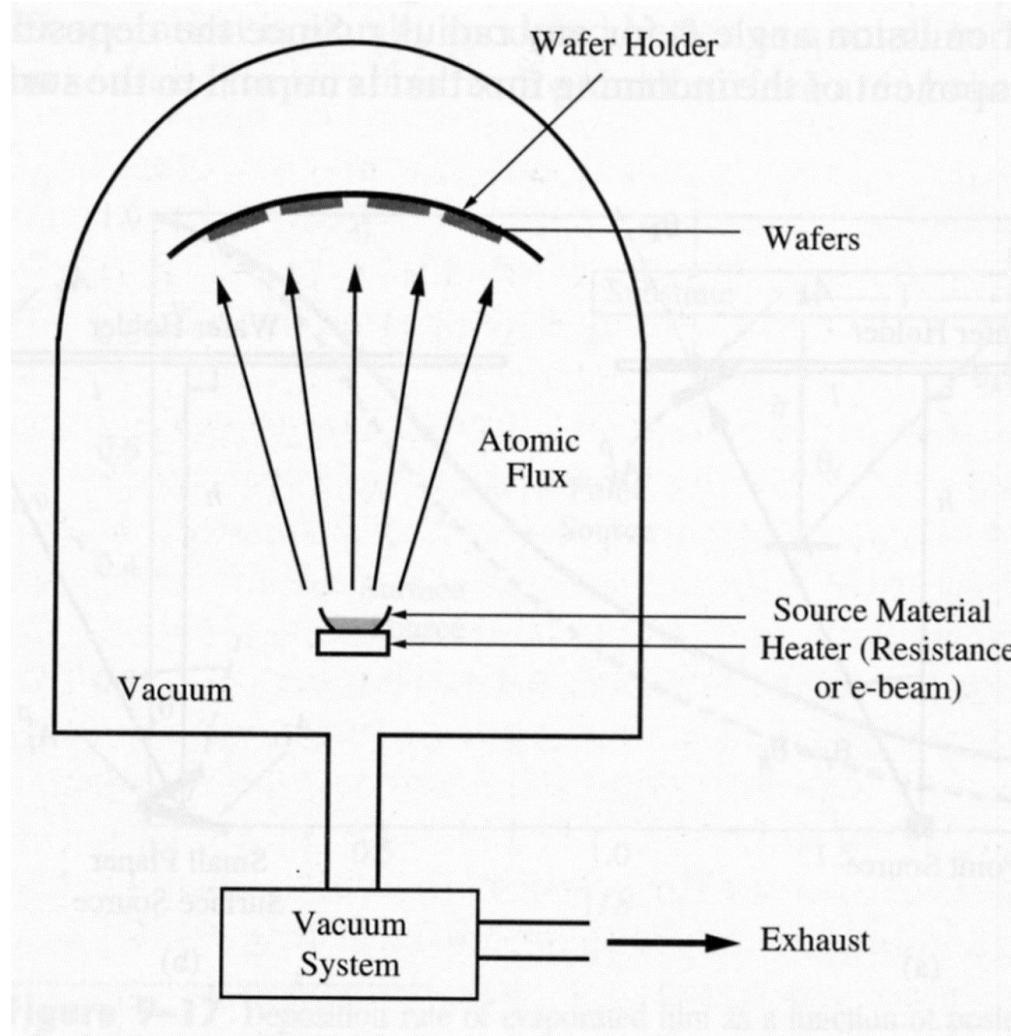
Steps in CVD



1. Transport reactants via forced convection to reaction region
2. Transport reactants via diffusion to wafer surface
3. Adsorb reactants on surface
4. Surface processes: chemical decomposition, surface migration, site incorporation, etc.
5. Desorption from surface
6. Transport byproducts through boundary layer
7. Transport byproducts away from deposition region

Physical Vapor Deposition: PVD

2 types: *evaporation*
and *sputtering*



Advantages:

Versatile – deposits almost any material

Very few chemical reactions

Little wafer damage

Limitations:

Line-of-sight

Shadowing

Thickness uniformity

Difficult to evaporate materials with low vapor pressures

Sputter deposition

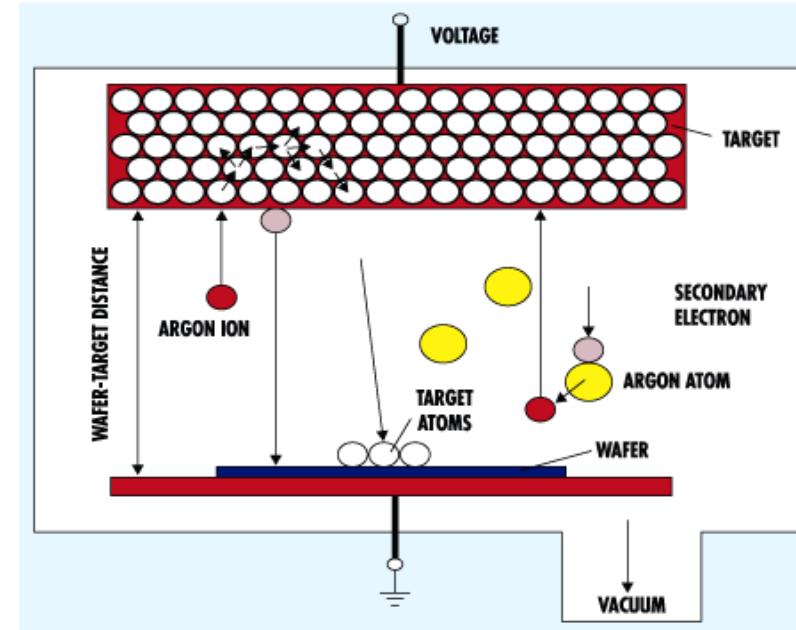
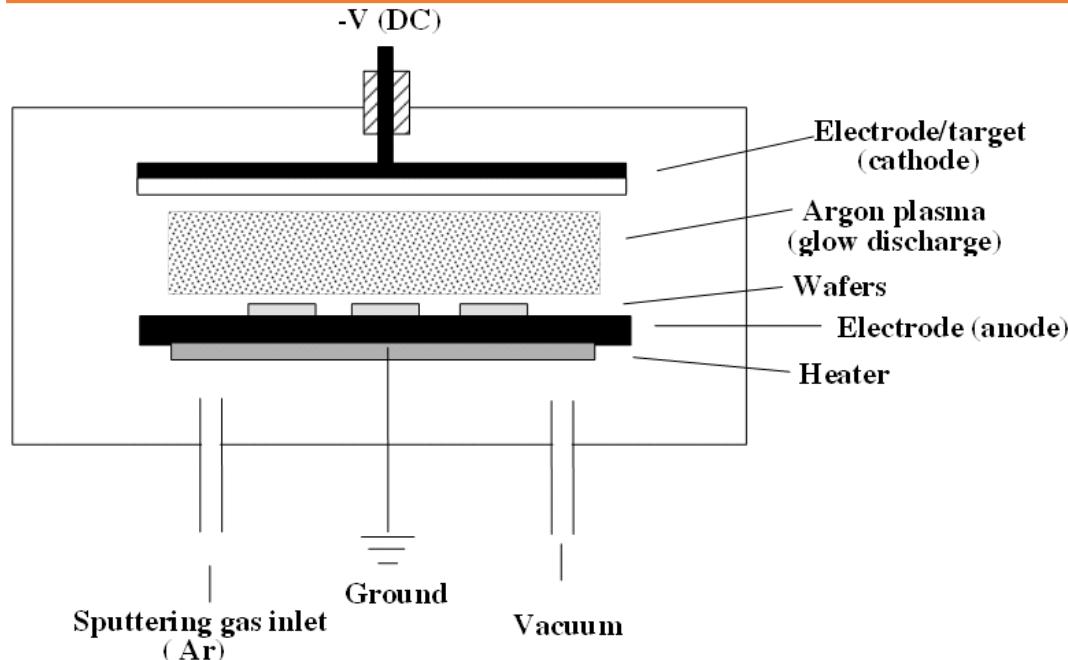
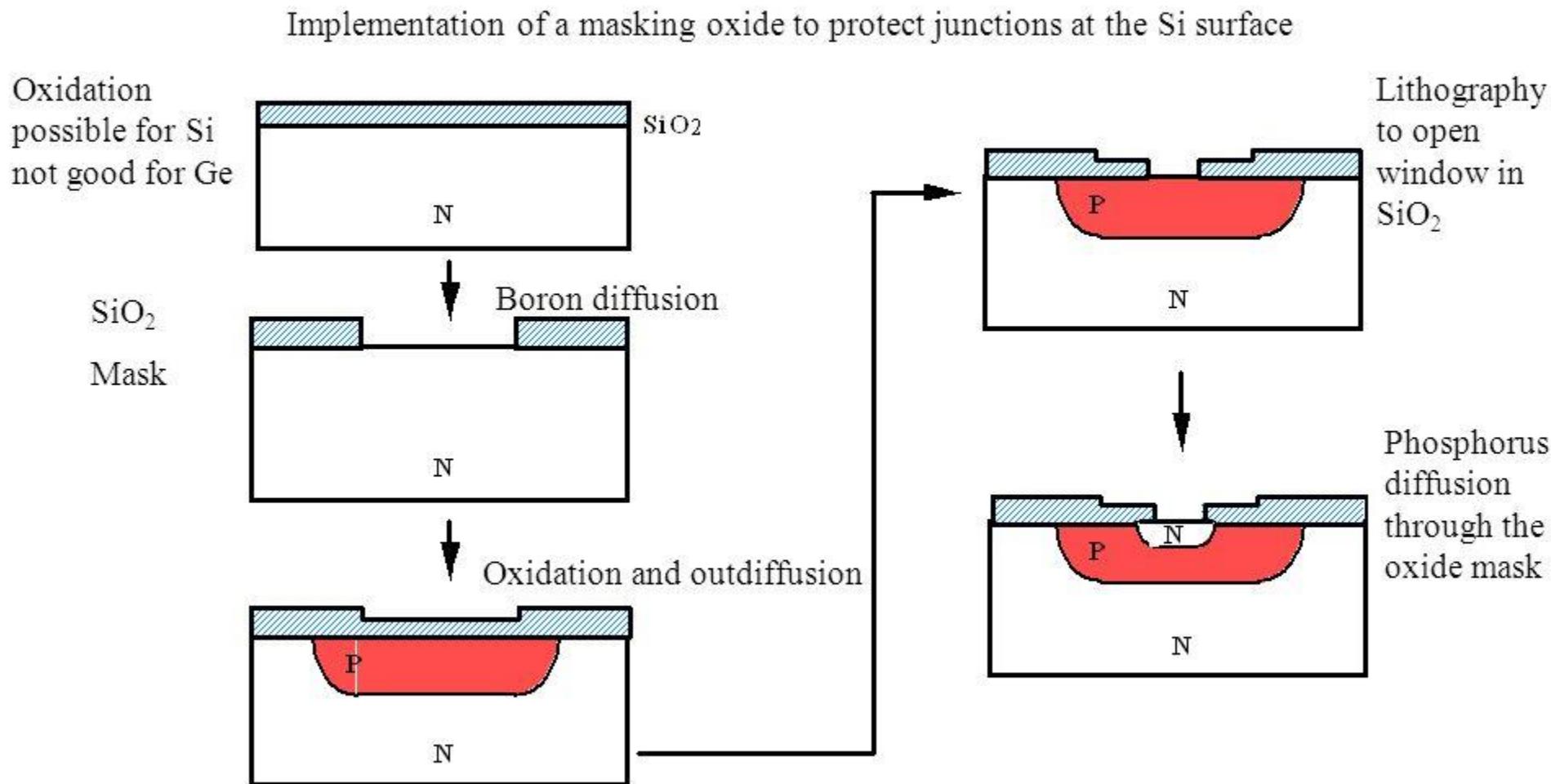


Figure. Schematic diagram of DC-powered sputter deposition equipment.

- Plasma is needed to make the gas conductive, and generated ions can then be accelerated to strike the target.
- Higher pressures than evaporation: 1-100 mTorr.
- Better at depositing alloys and compounds than evaporation.
- The plasma contains \approx equal numbers of positive argon ions and electrons as well as neutral argon atoms. Typically only <0.01% atoms are ionized!

Evolution of the Fabrication Process: The Planar Design of Bipolar Transistors

Beginning of the Silicon Technology and the End of Ge devices



The planar process of Hoerni and Fairchild (1950s)

Unit V

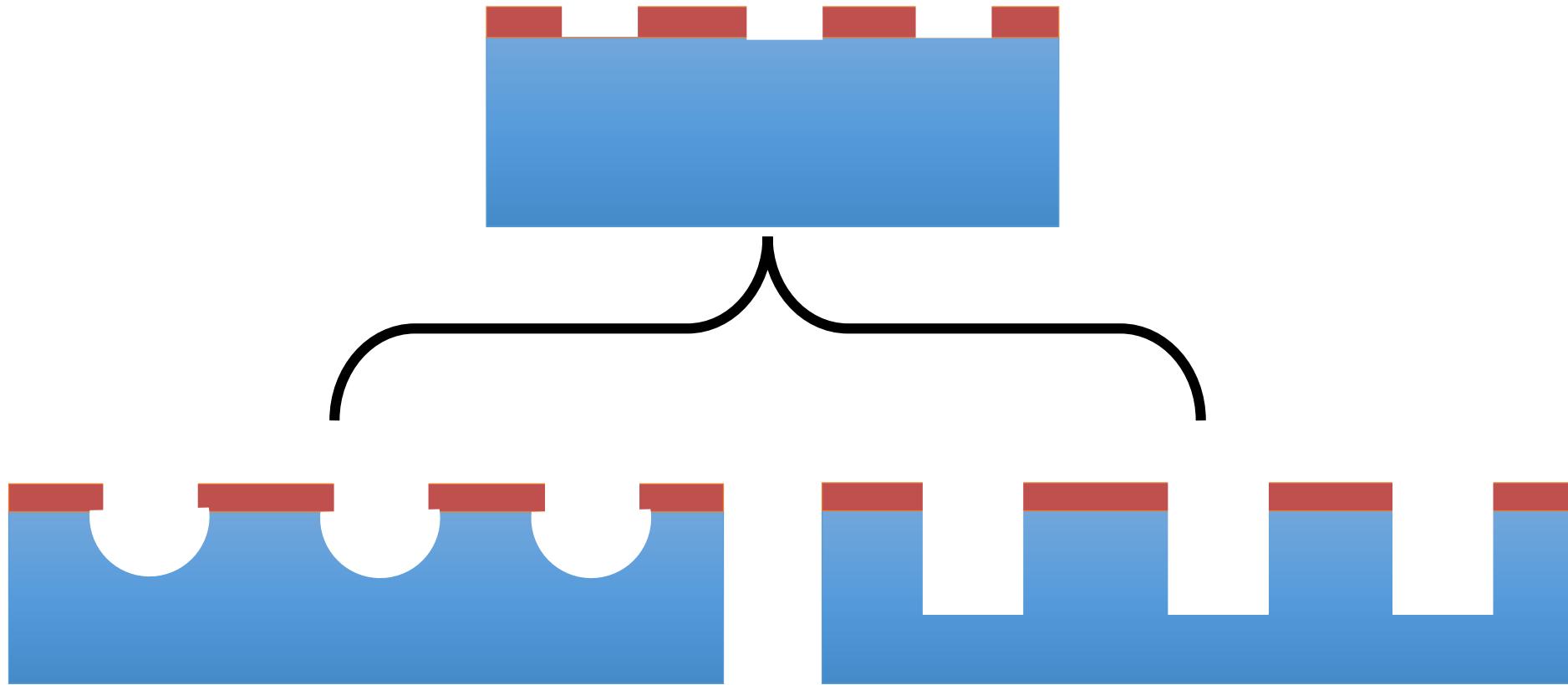
Lecture 3

Topics

1. Etching
2. MEMS fabrication technologies: Bulk micromachining and Structures
3. Surface micromachining and structures

Etching

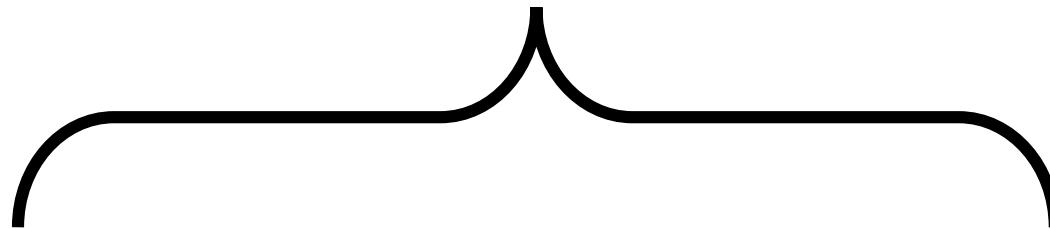
It is a subtractive process by which the material is selectively removed from substrate or other functional layers to form structures or devices.



Isotropic etching

Anisotropic etching

Etching



Wet Etching

Etching is performed by chemical solutions like, Silicon etching using KOH, TMAH

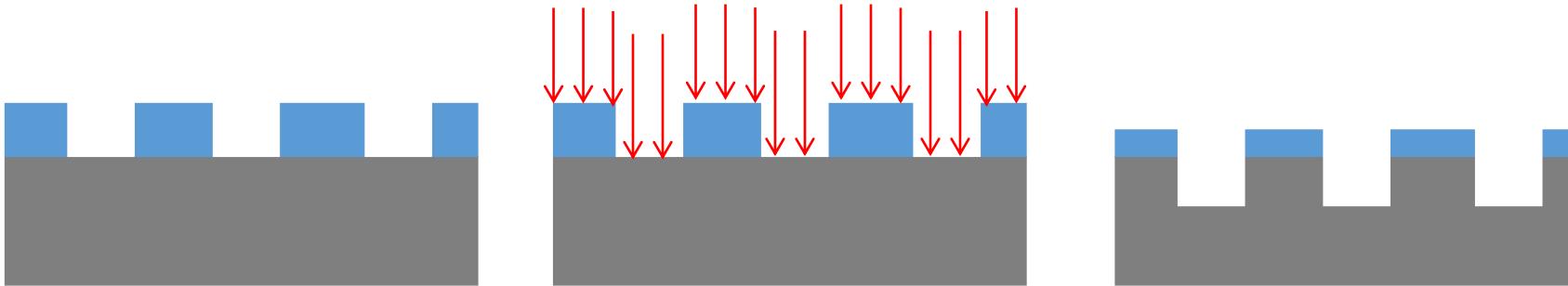
Silicon dioxide etching using HF

Dry Etching

Etching is performed by reactive plasma produced using chemical gases, Silicon etching using CF_4 , SF_6 and XeF Silicon dioxide etching using CHF_3 and CF_4

Etching

Etching is the process of selective removal of materials from a substrate or a wafer to form micro/nano structures and devices or to transfer lithographically generated patterns to a more stable masking materials for further processing.



Based on the methods, etching is classified into two major categories
Wet and dry etching

Wet etching

Wet etching is a material removal process that uses liquid chemicals called etchants to remove materials from a wafer

Etchants for Si

- Potassium hydroxide solution (KOH)
- Tetramethyl ammonium hydroxide solution (TMAH)
- Mixture of hydrofluoric acid, nitric acid, and acetic acid (HNA)

Etching

Etchant for SiO₂

- Hydrofluoric acid (HF)

Dry etching

Dry etching is a material removal process that uses plasmas or etchant gases to remove materials from a wafer. The plasma is produced by the electric breakdown through appropriate gaseous mixtures.

Etching gases for Si

- CF₄ (tetrafluoro methane)
- SF₆ (Hexafluoro methane)
- XeF₂ (Xenondifluoride)

Etching gases for SiO₂

- CF₄ (tetrafluoro methane)
- CHF₃ (trifluoromethane)

Etching

Dry etching is comprised of two processes

1. Physical etching
2. Chemical etching

In physical process heavy ions knock out atoms from the substrate or wafer

In chemical process plasma reacts with the materials and remove it from the wafer

Examples of physical etching

1. Ion milling

Heavy ions will be used to remove materials from exposed region of the wafers (e.g. focused ion beam milling)

2. Laser ablation

High energy laser beams will be used to remove materials from a wafer (e.g. CO₂ lasers for dicing SiO₂ samples)

Examples of chemical etching

1. Reactive ion etching (RIE)
2. Vapour phase etching

Etching

Reactive ion etching (RIE).

It is an etching process used in micro/nanofabrication. It uses chemically reactive plasma to remove materials from the exposed region of a wafer. It is a combination of both physical and chemical etching.

e.g.

Silicon etching using CF_4 or SF_6 plasma
And SiO_2 etching using CHF_3 plasma

There are two types of RIE

1. Capacitively coupled plasma RIE

Plasma is generated between a parallel plate capacitor arrangement
(plasma density is low)

2. Inductively coupled plasma RIE

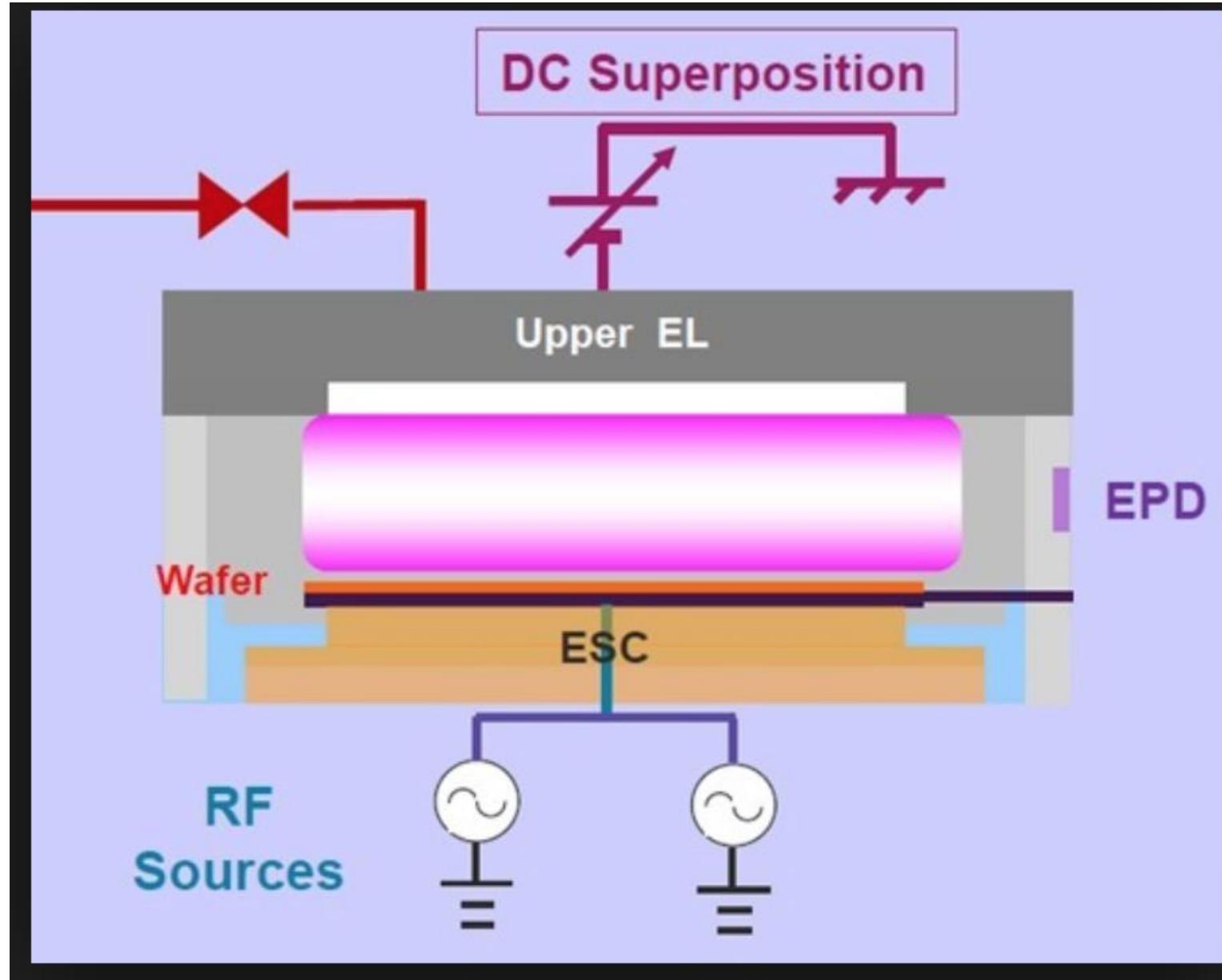
Here the plasma is generated by an induction coil around the parallel plate capacitor arrangement (high plasma density).

Parallel plate arrangement provides sufficient biasing

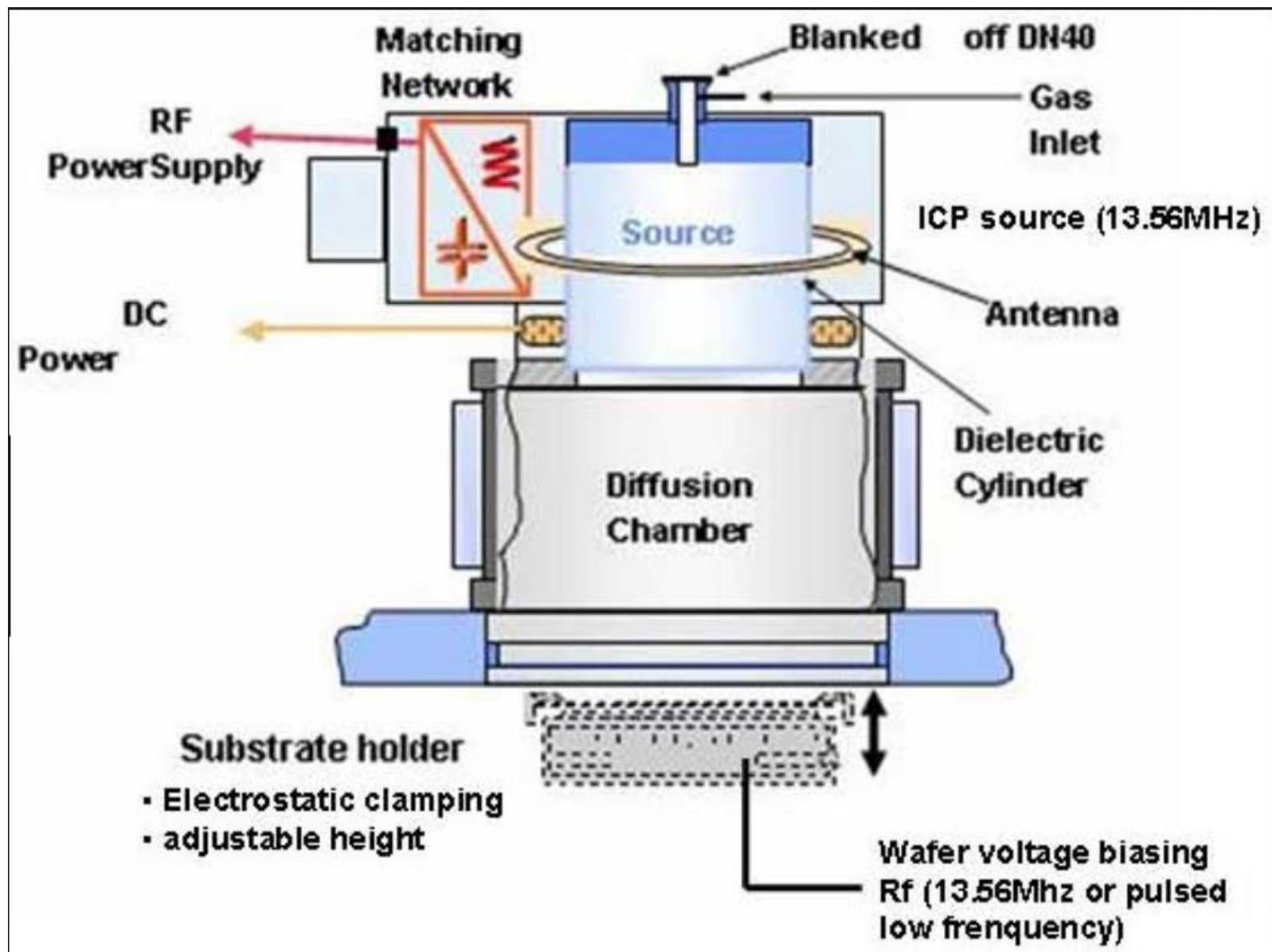


A commercial reactive-ion etching
setup in a cleanroom

Capacitively coupled plasma Reactive-ion etching (CCP RIE)



ICP RIE



Etching

Vapour phase etching

Reactive vapours of acids are used to remove materials from a wafer

e.g.

SiO_2 etching using HF vapour

It is an isotropic etching process

Etching

Based on the etching profile, etching is classified in to two major categories
Isotropic etching and nisotropic etching

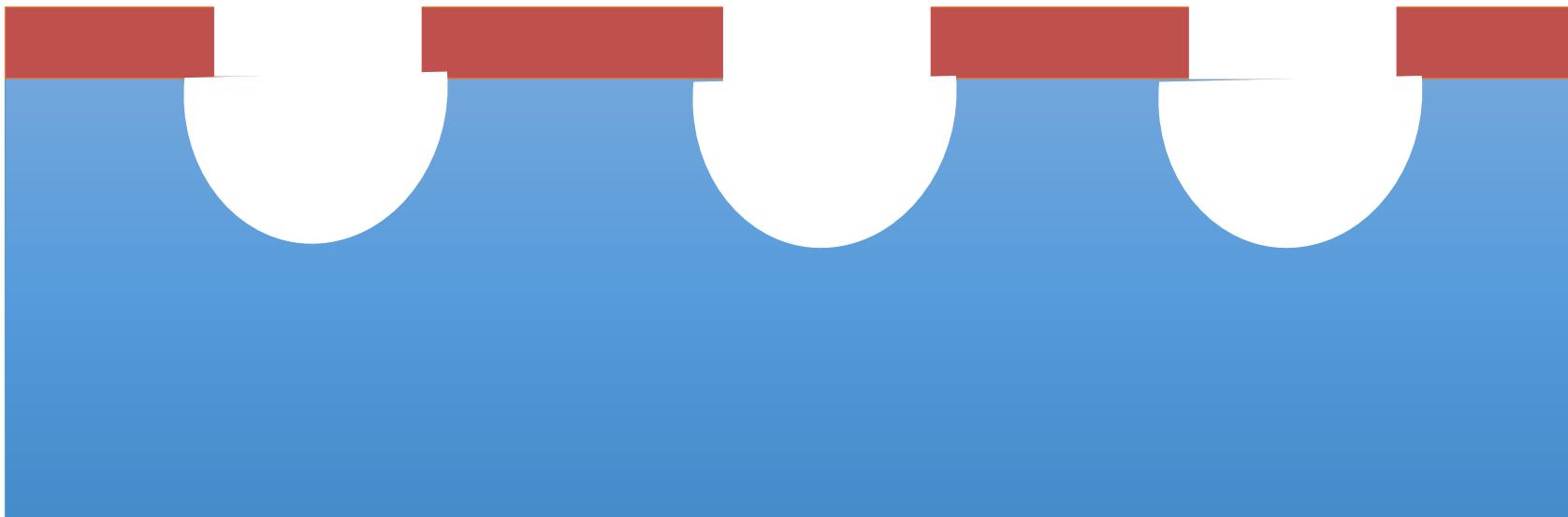
Isotropic etching



Etching

Based on the etching profile, etching is classified in to two major categories
Isotropic etching and nisotropic etching

Isotropic etching



Uniform etch rate in all directions

Horizontal etch rate = vertical etch rate

e.g.

Wet etching of SiO_2 using HF

Reactive ion etching of Si using CF_4 plasma

Etching

Anisotropic etching

Different etch rate in different directions



Direction dependent etch rate
Zero or very small Horizontal etch rate
Large vertical etch rate

Parameters	Dry Etching	Wet etching
Directionality	Good for most materials	Only with crystal materials [Aspect ratio upto 100]
Production automation	Good	Poor
Environmental impact	Low	High
Masking film adherence	Not as critical	Very critical
Selectivity	Poor	Very Good
Materials to be etched	Only certain materials	All
Process scale-up	Difficult	Easy
Cleanliness	Conditionally clean	Good to very good
Equipment cost	Expensive	Less expensive
Operational parameters	Many	Few
Typical etch rate	Slow [0.1µm/min] to fast [6µm/min]	Fast [1µm/min and up]
Control of etch rate	Good in case of slow etch	Difficult
Application:For making very small features in thin films	Possible to etch almost straight down without under cutting	Undercutting problem will occur

MEMS fabrication (Micromachining)

Two types: Bulk and surface micromachining

Bulk micromachining

- Bulk micromachining technique was developed in **1960s** and allows the **selective removal** of significant amounts of silicon from a substrate to form membranes on one side of a wafer, a variety of trenches, holes, or other structures
- The bulk micromachining technique can be divided into **wet etching and dry etching** of silicon according to the phase of etchants. Liquid etchants, almost exclusively relying on aqueous chemicals, are referred to as wet etching, while **vapor and plasma etchants** are referred to as dry etching.
- almost all **pressure sensors and silicon valves** and 90% of **silicon accelerometers** are made by this process.

✓ The microstructures fabricated using bulk micromachining may cover the thickness range from submicron to full wafer **thickness (200 to 500 µm)** and the lateral size range from submicron to the lateral dimensions of a full wafer.

✓ For etching such thick silicon substrate, **Anisotropic wet etchants** such as solutions of potassium hydroxide (**KOH**), ethylene-diamine pyrocatechol (**EDP**), tetra-methyl-ammonium hydroxide (**TMAH**) and **hydrazine-water** are used. These etchants have **different etch rates** in different **crystal orientations** of the silicon

✓ A region at which **wet etching** tends to slow down or diminish is called an '**etch-stop**'. There are several ways in which an etch-stop region can be created; **doping-selective etching (DSE)** and bias-dependent DSE

- Wet etching occurs by dipping substrate into an etching bath or spraying it with etchants which may be acid or alkaline.
- **Wet etching** can either be **isotropic etching or anisotropic** etching depending on the structure of the materials or the etchants used.
- If the material is **amorphous or polycrystalline**, wet etching is always **isotropic** etching.
- During **isotropic etching** (etchants used are acid solution), resist is always undercut, meaning the **deep etching is not practical for MEMS**.

- **Single-crystal** silicon can be **anisotropically** etched. The etching features are determined by the etching speed, which is dependent on the crystal's orientation.
- The **etching slows down** significantly at the **(111)** planes of silicon, relative to other planes.
- Most common etchants used for **anisotropic** etching of silicon include alkali hydroxide etchants (**KOH**, **NaOH**, etc.), ammonium-based solutions {**NH4OH**, **TMAH** [$(CH_3)_4NOH$], etc.} and **EDP** (ethylene diamine pyrocatechol, and water).

□ **Dry etching** occurs through chemical or physical interaction between the **ions in the gas** and the **atoms of the substrate**.

□ **Non-plasma, Isotropic** dry etching can be possible using **xenon difluoride** or a mixture of **inter-halogen gases** and provides very high selectivity for aluminum, silicon dioxide, silicon nitride, photoresist, etc.

□ The most **common dry etching** of bulk silicon are **plasma etching and reactive ion etching (RIE) etching**, where the external energy in the form of RF power drives chemical reactions in low-pressure reaction chambers.

□ A wide variety of **chlorofluorocarbon gases**, **sulfur hexafluoride**, **bromine compounds** and oxygen are commonly used as reactants.

□ The anisotropic dry etching processes are widely used in MEMS because of the **geometry flexibility and less chemical contamination** than in wet etching sometimes.

Isotropic Wet Etchant – HNA (HF, Nitric, Acetic)

Very aggressive acidic mixture attacks Silicon vigorously.
It etches Silicon at the rate of 1-3 micron/min

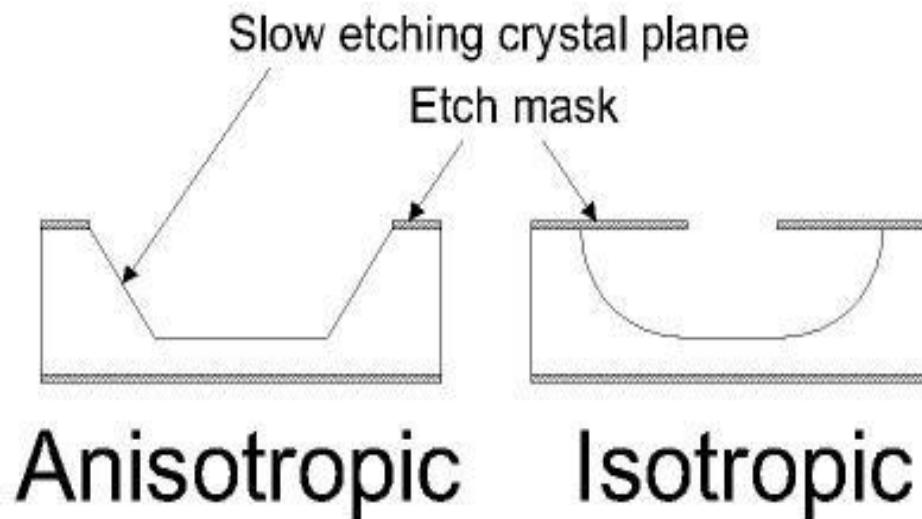


Figure 1: Difference between anisotropic and isotropic wet etching.

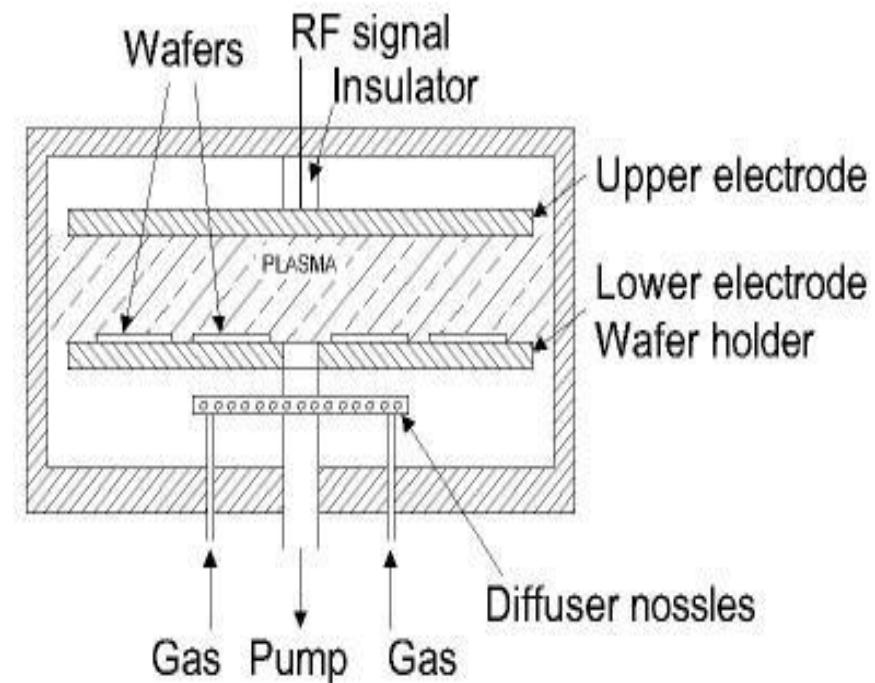
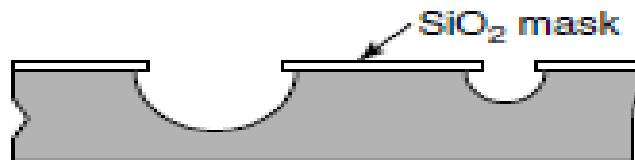
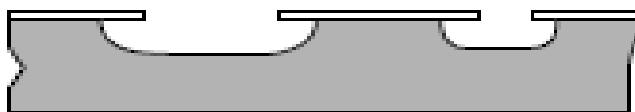


Figure 2: Typical parallel-plate reactive ion etching system.

Isotropic wet etching: agitation

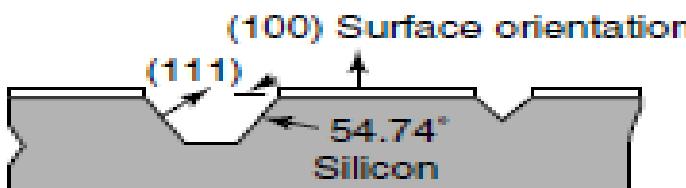


Isotropic wet etching: no agitation

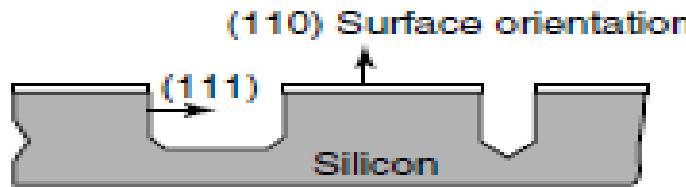


(a)

Anisotropic wet etching: (100) surface

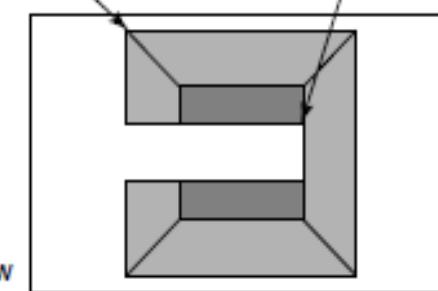


Anisotropic wet etching: (110) surface

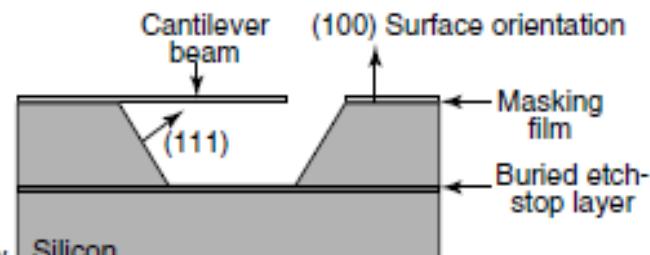


(b)

Concave corner Convex corner

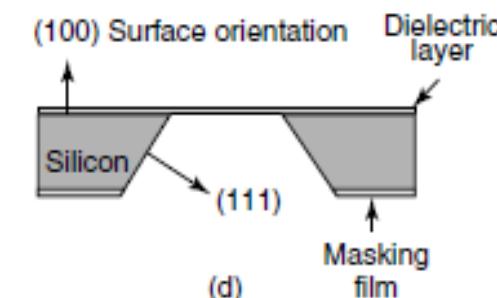


Top view



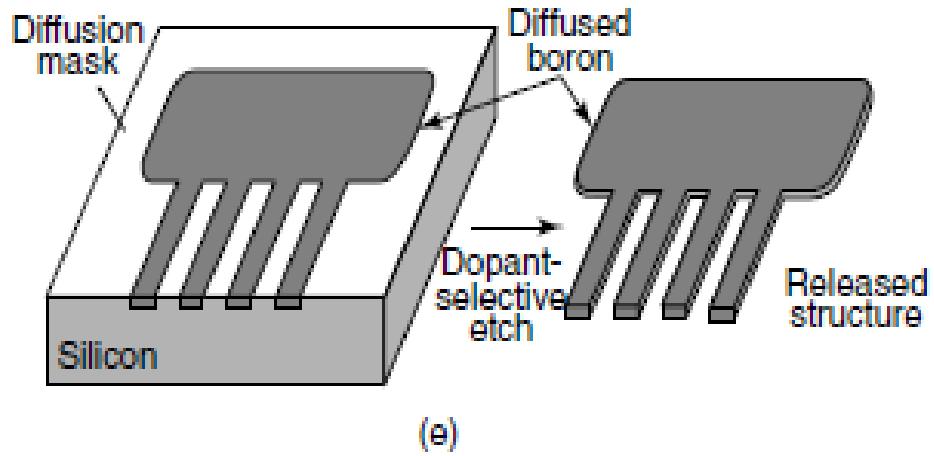
Side view

(c)

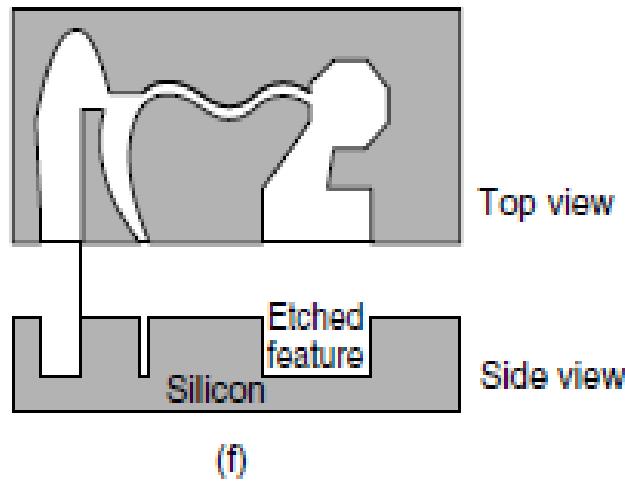


(d)

Bulk silicon micromachining: (a) isotropic etching; (b) anisotropic etching; (c) anisotropic etching with buried etch-stop layer; (d) dielectric membrane released by back-side bulk etching;



(e)



Top view

Side view

(f)

(e) Dopant dependent wet etching. (f) anisotropic dry etching.

Surface micromachining of silicon

- Surface micromachining does **not shape the bulk silicon** but instead **builds structures** on the surface of the silicon by depositing thin films of '**sacrificial layers**' and '**structural layers**' and by removing eventually the sacrificial layers to release the mechanical structures
- The dimensions of these surface micromachined structures can be several orders of magnitude smaller than bulk-micromachined structures. The prime **advantage** of surface-micromachined structures is their **easy integration with IC components**, since the wafer is also the working for IC elements.

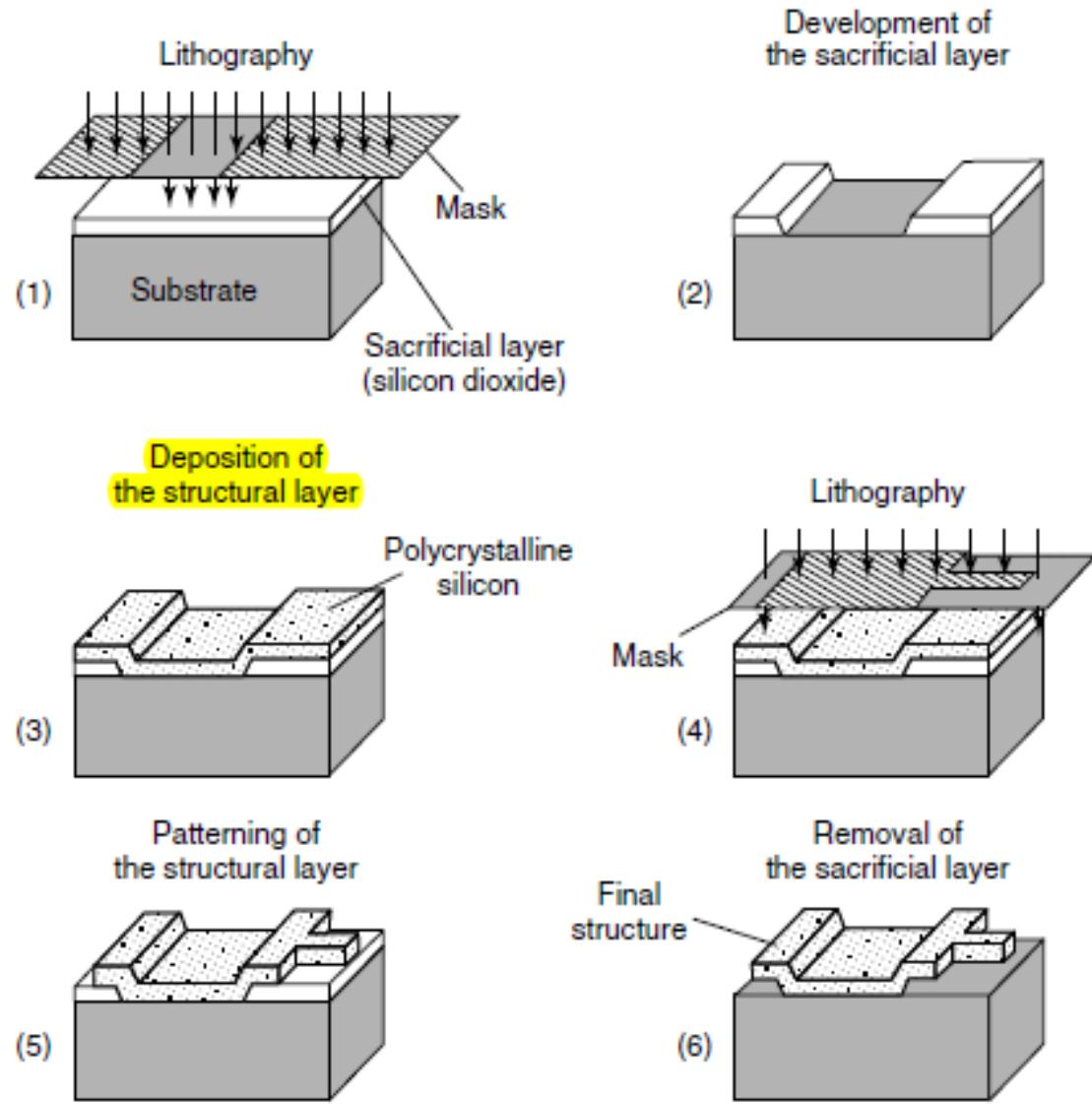


Fig. Processing steps of typical surface micromachining.

- Surface micromachining requires a **compatible set of structural materials, sacrificial materials and chemical etchants.**
- The **sacrificial materials** must have following properties to avoid device failure during fabrication.
 - Good mechanical properties
 - Good adhesion
 - Low residual stresses
 - Etchants selectivity for sacrificial materials
 - Etchants viscosity and surface tension

❖ The common IC compatible materials used in surface micromachining are:

(1) **Polysilicon/Silicon dioxide;**

low-pressure chemical vapor deposition (**LPCVD**) **deposited polysilicon** as the structural material and **LPCVD deposited oxide** as the **sacrificial material**. The **oxide** is readily **dissolved in HF** solution without the polysilicon. Together with this material system, **silicon nitride** is often used for **electrical insulation**

(2) **Polyimide/aluminum;**

in this case polyimide is the **structural material** and **aluminum** is the **sacrificial material**. **Acid-based etchants** are used to dissolve the aluminum sacrificial layer.

(3) **Silicon nitride/polysilicon;**

silicon nitride is used as the **structural material**, whereas polysilicon is the **sacrificial material**. For this material system, silicon anisotropic etchants such as **KOH and EDP** are used to dissolve polysilicon.

(4) **Tungsten/silicon dioxide;**

CVD deposited tungsten is used as the **structural material** with oxide as the **sacrificial material**. HF solution is used to remove the sacrificial oxide.

(5) Other IC-compatible materials such as silicon carbide, diamond-like carbon, zinc oxide, gold, etc. are also used.

Bulk Micromachining

- 1 In this mechanical elements are fabricated by etching away the unwanted part in wafer
- 2 This creates structures inside a substrate
- 3 Larger structures are made with bulk micromachining
- 4 Limited to low aspect ratio in geometry as surface dimensions are much greater than depth as height is limited by thickness of silicon wafer
- 5 Straight forward and well documented processes
- 6 Sacrificial layer is not required
- 7 The process is less expensive but material loss is more
- 8 Mechanical properties are superior
- 9 Dimensional control is good
- 10 CMOS integration is fair
- 11 It causes a well known phenomenon in the micro electronics industry called undercut
- 12 Size is small
- 13 Typically uses wet etching techniques
- 14 Suitable for simple geometry such as thermal sensor, micro machined neuron wells

Surface Micromachining

- 1 In this it is fabricated by building layers on layers
- 2 This creates structures on top of a substrate
- 3 It is difficult to build larger structures
- 4 Not constraints by thickness of silicon wafer, so high aspect ratio geometries can be fabricated using surface micromachining
- 5 Complex masking design and production
- 6 Etching of sacrificial layer is required
- 7 The process is expensive but less material loss
- 8 Mechanical properties are good
- 9 Dimensional control is better
- 10 CMOS integration is good
- 11 It does not cause undercut problem
- 12 Size is smaller
- 13 It uses dry etching techniques
- 14 Suitable for complex geometry such as micro valves and actuators

Unit V

Lecture 6

Topics

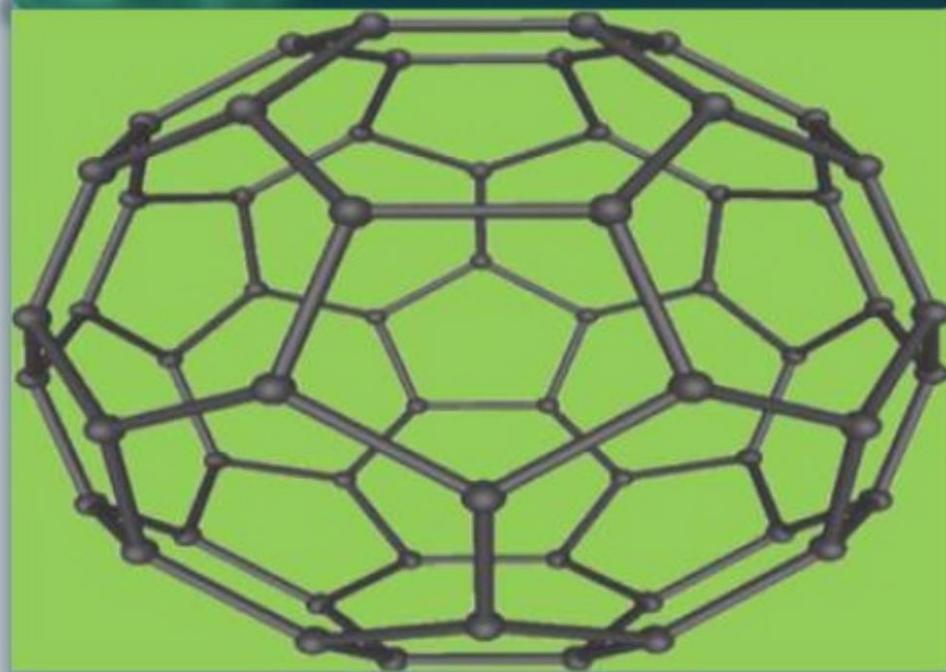
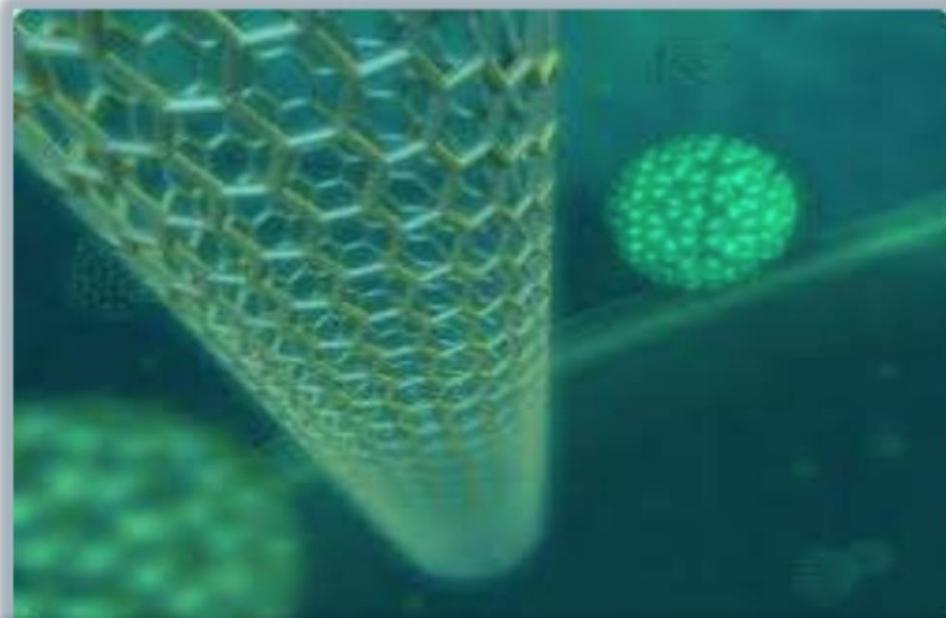
1. Nanotechnology
2. product prospects application trends

NANO & TECHNOLOGY

- A **Nanometre** is a unit of length in the metric system, equal to one billionth of a metre(10^{-9}).
- **Technology** is the making, usage, and knowledge of tools, machines and techniques, in order to solve a problem or perform a specific function.

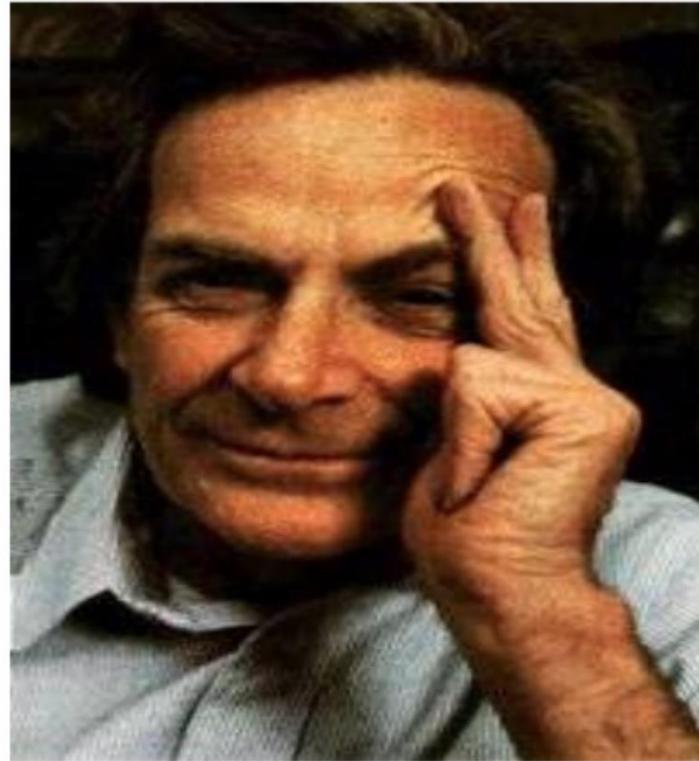
Defination

- **Nanotechnology** is the study of manipulating matter on an atomic scale.
- **Nanotechnology** refers to the constructing and engineering of the functional systems at very micro level or we can say at atomic level.
- A **Nanometer** is one billionth of a meter, roughly the width of three or four atoms. The average human hair is about 25,000 nanometers wide.

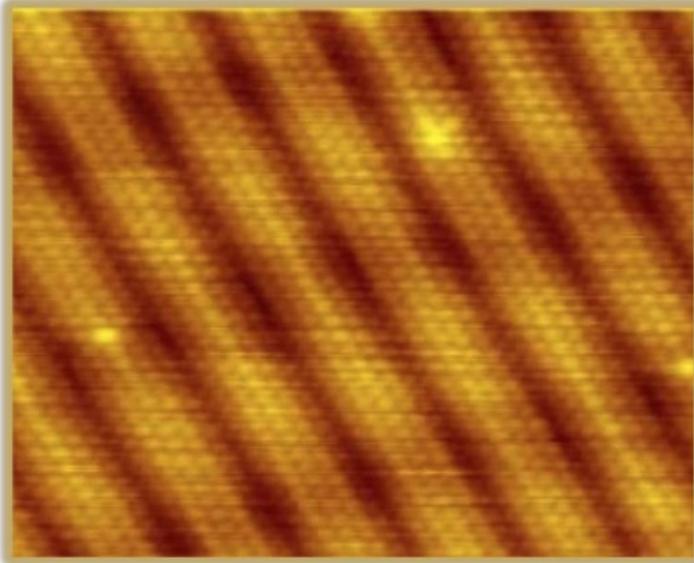


History

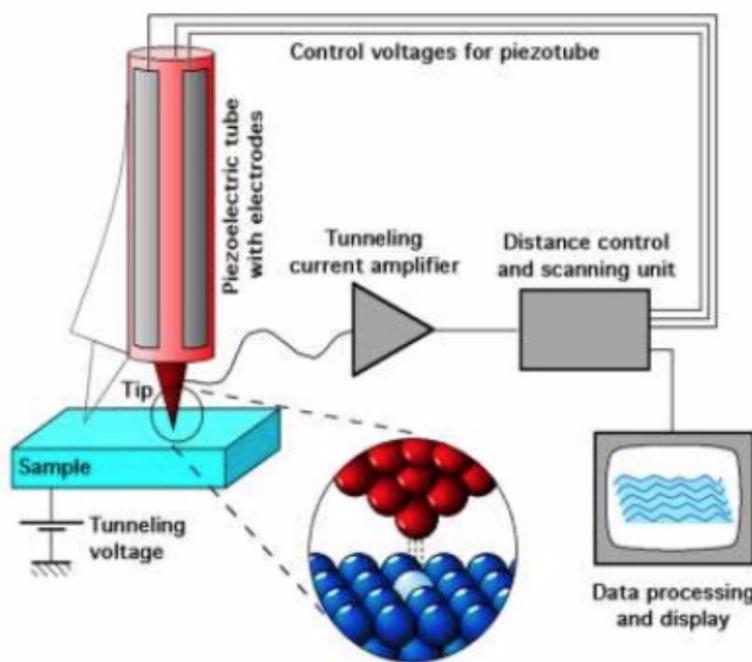
- The first ever concept was presented in 1959 by the famous professor of physics **Dr. Richard P.Feynman**.
- Invention of the **scanning tunneling microscope** in 1981 and the discovery of **fullerene**(C₆₀) in 1985 lead to the emergence of **nanotechnology**.
- The term "**Nano-technology**" had been coined by Norio Taniguchi in 1974



**THERE'S PLENTY
OF
ROOM AT THE
BOTTOM**



- The early 2000s also saw the beginnings of commercial applications of nanotechnology, although these were limited to bulk application of nanomaterials.

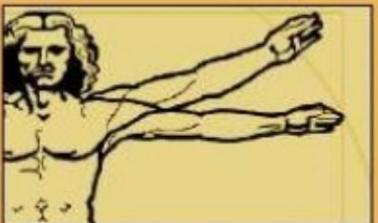


- **Silver nano** platform for using silver- nanoparticles as an **antibacterial agent**, **nanoparticle-based transparent sunscreens**, and **carbon nanotubes** for stain-resistant textiles.

MACRO

MICRO

NANO



PERSON (~6ft tall)
2 billion nm



APPLE (~8cm)
80 million nm



ANT (~5mm)
5 million nm

100,000 nm (.1 mm)



diameter of
a HUMAN
HAIR
75,000 nm

smallest the
EYE CAN SEE
10,000 nm



e. coli
BACTERIA
2,000 nm

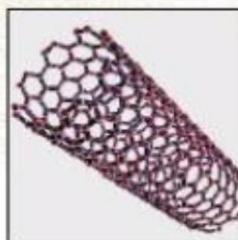
100 nm (.001 mm)



DNA
2 nm

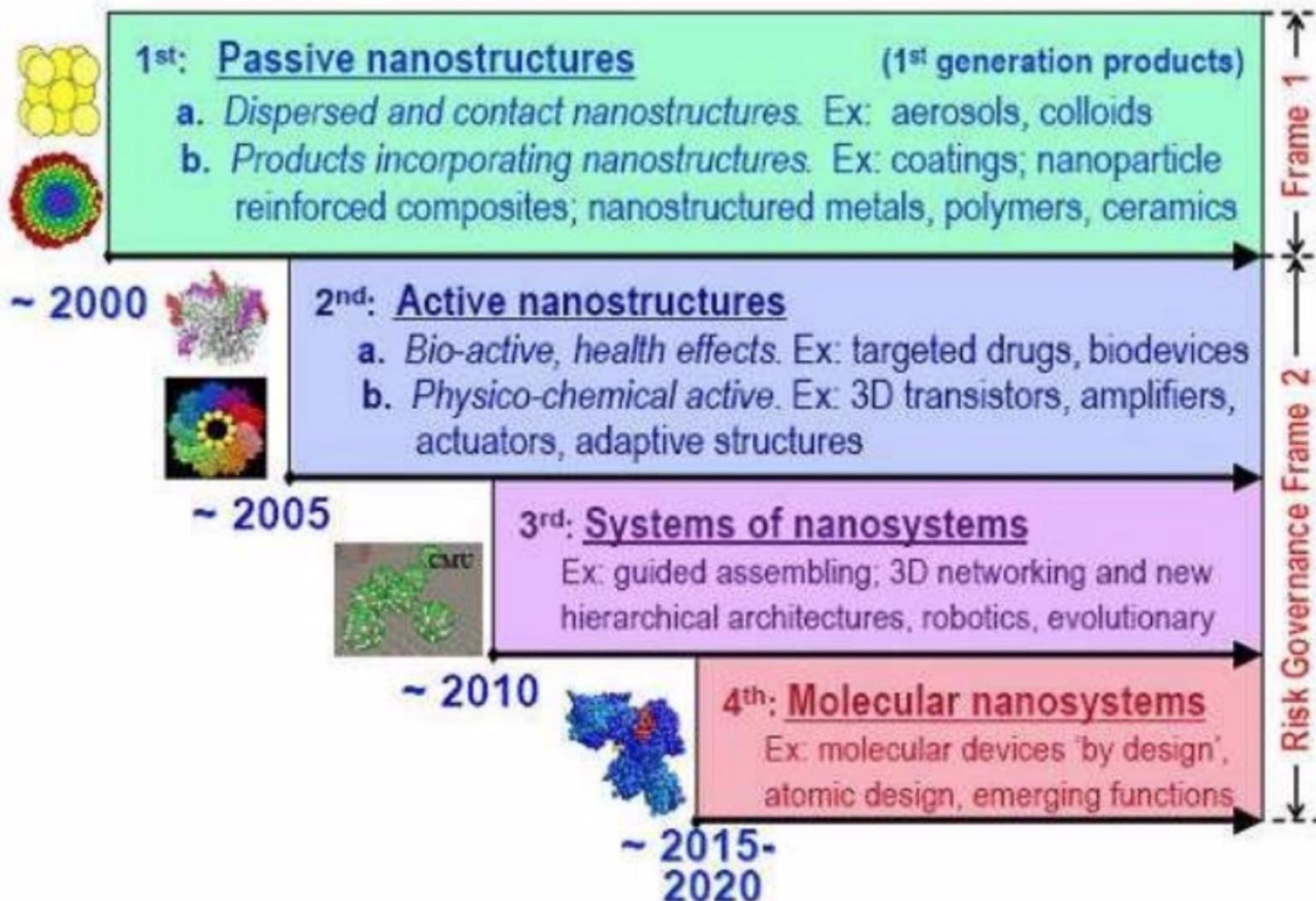


BUCKYBALL
1 nm



diameter of a
CARBON
NANOTUBE
1.3 nm

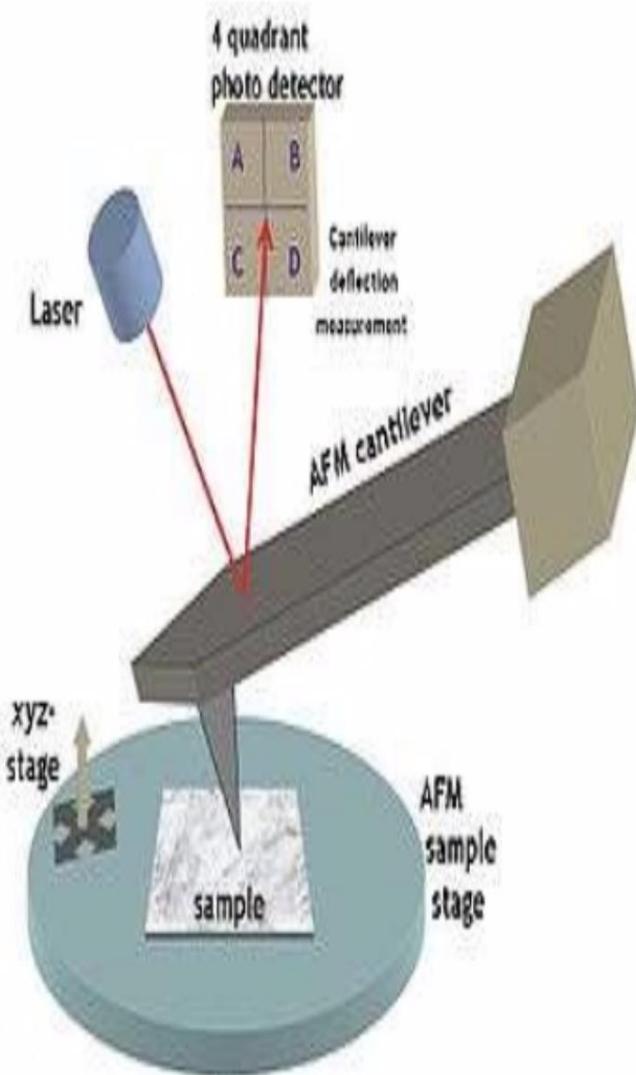
Timeline



Tools & Technology

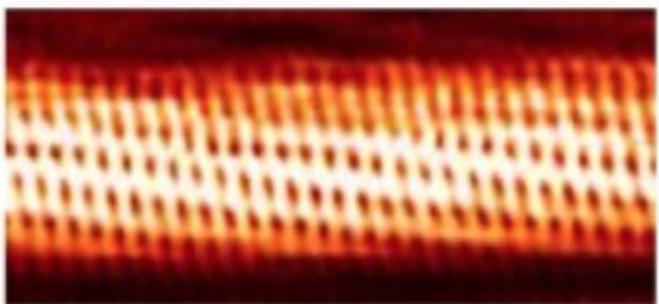
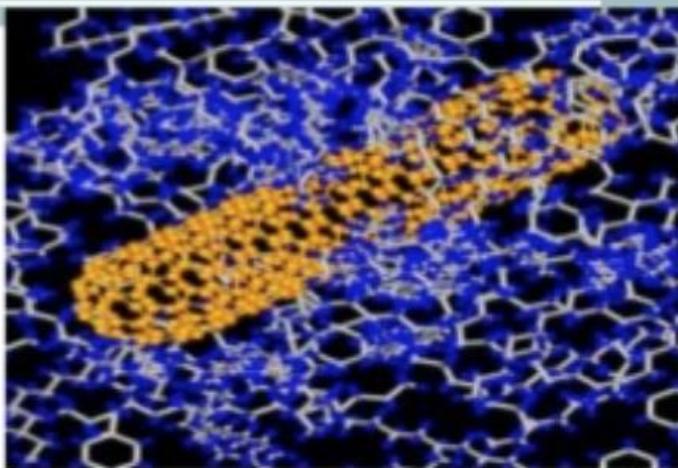
- There are several important modern developments.
 - The **atomic force microscope (AFM)**.
 - The **Scanning Tunneling Microscope (STM)** are scanning probes that launched nanotechnology.
- Various techniques of **nanolithography** such as:
 - optical lithography.
 - X-ray lithography,
 - **Dip pen nanolithography**
 - **Electron beam lithography(inkjet printer)**
were also developed.

Lithography in MEMS context is typically the transfer of a pattern into a photosensitive material by selective exposure to a radiation source such as light.



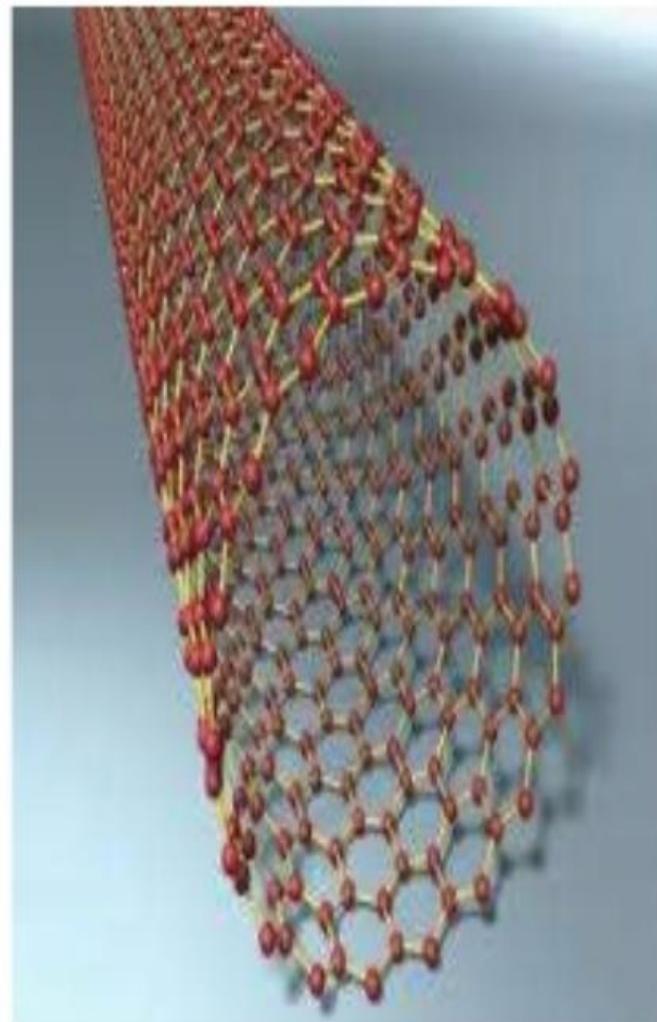
Carbon Nanotube

- Carbon nanotubes are allotropes of carbon with a cylindrical nanostructure.
- They have length-to-diameter ratio of upto 132,000,000:1.
- Nanotubes are members of the fullerene structural family. Their name is derived from their **long, hollow structure** with the walls formed by **one-atom-thick sheets of carbon**, called graphene.
- Properties
 - Highest strength to weight ratio, helps in creating *light weight spacecrafts*.
 - Easily penetrate membranes such as cell walls. Helps in *cancer treatment*.
 - **Electrical resistance** changes significantly when other molecules attach themselves to the carbon atoms. Helps in developing **sensors** that can detect chemical vapours.



Carbon Nanotube

- Application
 - **Easton-Bell Sports, Inc.** using CNT in making **bicycle component**.
 - **Zyvex Technologies** using CNT for manufacturing of light weight boats.
 - Replacing transistors from the silicon chips as they are **small** and **emits less heat**.
 - In electric cables and wires
 - In solar cells
 - In fabrics

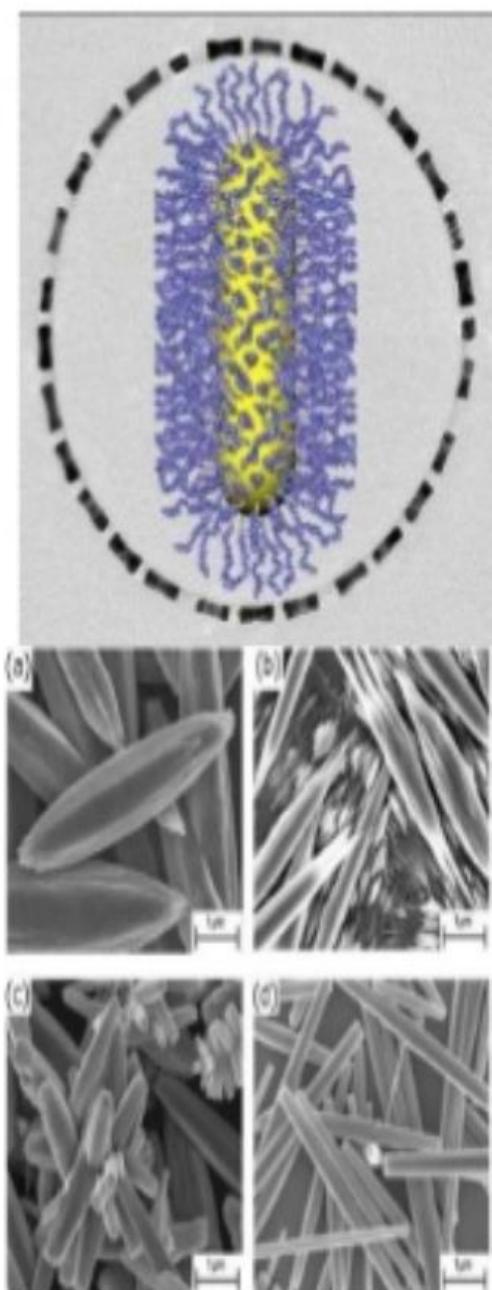


Nanorods(quantum dots)

- Nanorods are one morphology of nanoscale objects.
- Dimensions range from 1–100 nm.
- They may be synthesized from metals or semiconducting materials.
- A combination of ligands act as shape control agents and bond to different facets of the nanorod with different strengths. This allows different faces of the nanorod to grow at different rates, producing an elongated object.

□ USES:

- In display technologies, because the reflectivity of the rods can be changed by changing their orientation with an applied electric field.
- In microelectromechanical systems (MEMS).
- In cancer therapeutics.



Nanobots

- Close to the scale of 10^{-9} .
- Largely in R&d phase .
- Nanobots of 1.5 nanometers across, capable of counting specific molecules in a chemical sample.
- Since nanorobots would be microscopic in size, it would probably be necessary for very large numbers of them to work together to perform microscopic and macroscopic tasks.
- Capable of replication using environmental resources .
- Application:
 - Detection of toxic components in environment.
 - In drug delivery.
 - Biomedical instrumentation.



Unit V

Lecture 6

Topics

1. Approaches in Nanotechnology
2. product prospects application trends

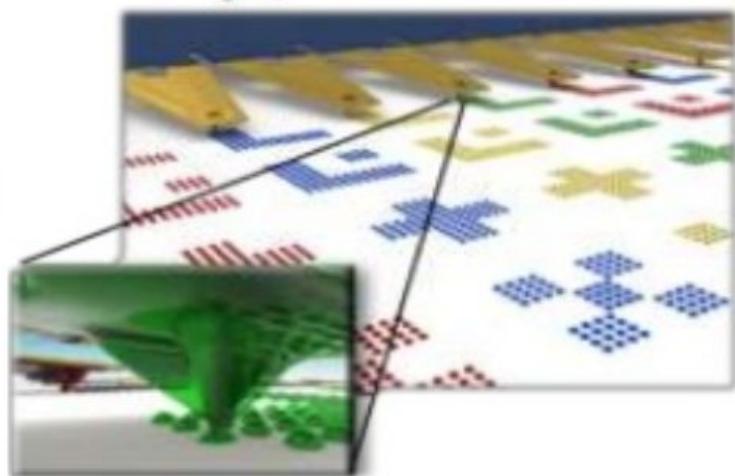
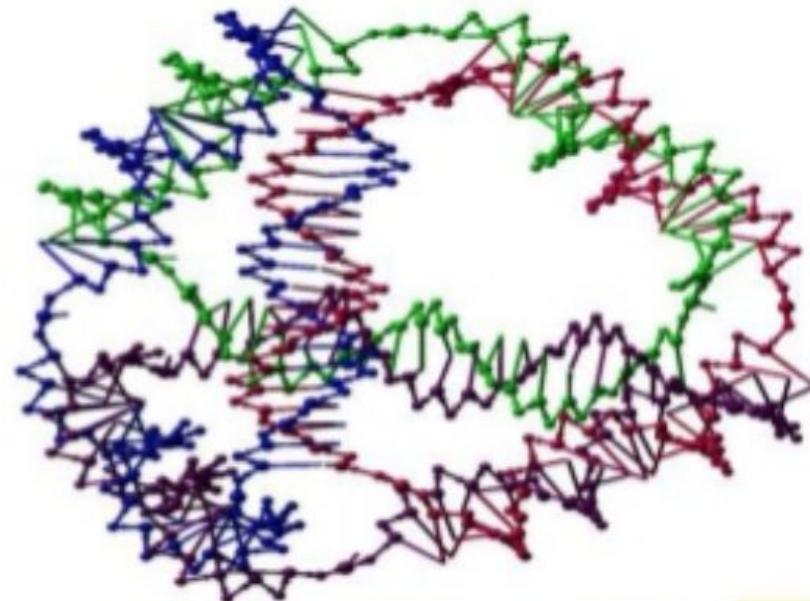
Dr. Renilkumar Mudachathi (Ph.D.)

Approaches in nanotechnology

1. Bottom up:

In the bottom up approach different materials and devices are constructed from molecular components of their own. They chemically assemble themselves by recognizing the molecules of their own breed.

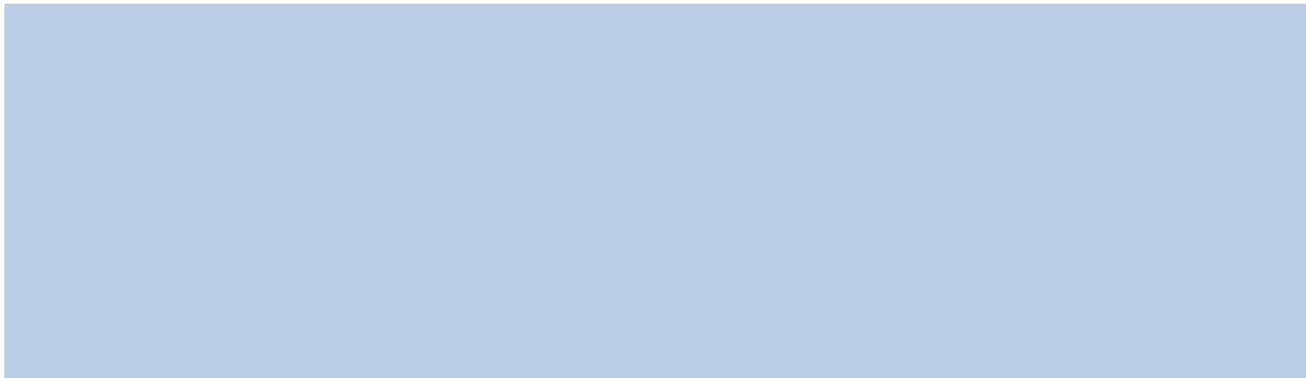
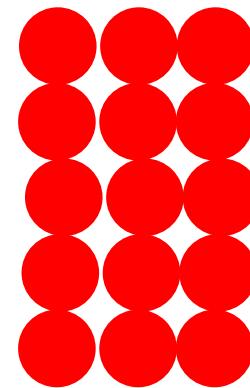
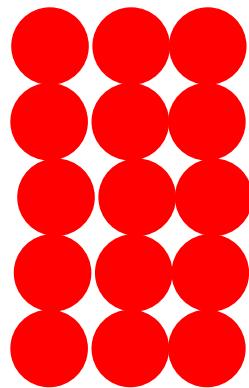
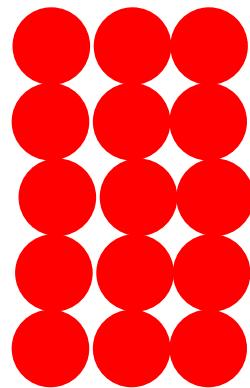
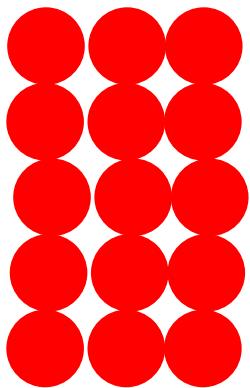
- Examples of molecular self assembly are **Watson crick base pairing , nano-lithography**.

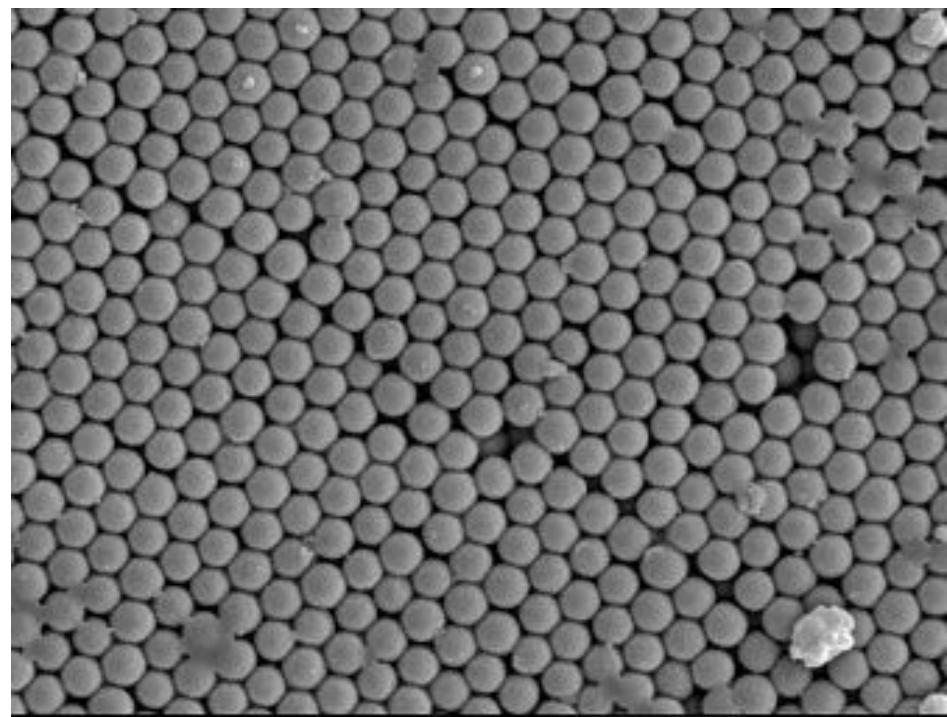
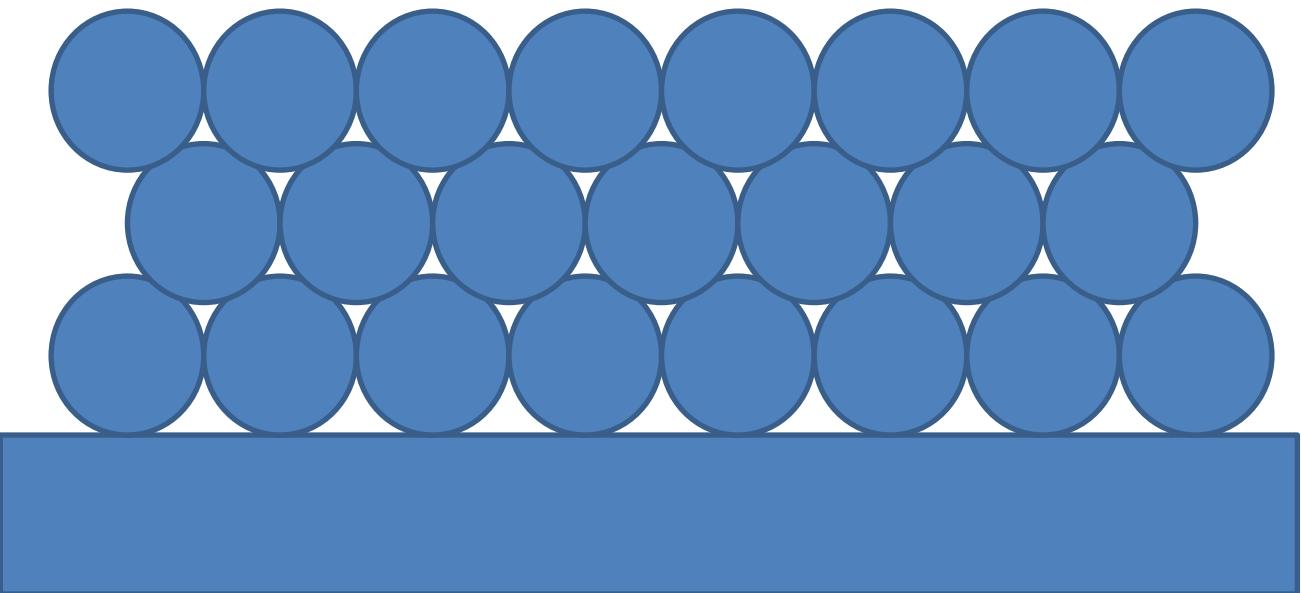


Bottom-up approach

Bottom up fabrication can be likened to building a brick house. Instead of placing bricks one at a time to produce a house, bottom up fabrication techniques place atoms or molecules one at a time to build the desired nanostructure. Such processes are time consuming and so self assembly techniques are employed where the atoms arrange themselves as required.

Self assembling nanomachines are regularly mentioned by science fiction writers but significant obstacles including the laws of physics will need to be overcome or circumvented before this becomes a reality. Other areas involving bottom up fabrication are already quite successful. Manufacturing quantum dots by self assembly. Quantum dots has rendered the top down lithographic approach to semiconductor quantum dot fabrication virtually obsolete.





JEOL

SEI

5.0kV X20,000

1μm

WD 15.0mm

2. Top down:

In top down approach nano objects and materials are created by larger entities without bouncing its atomic reactions usually top down approach is practiced less as compared to the bottom up approach.

- **Solid-state techniques** can also be used to create devices known as **nanoelectromechanical systems** or NEMS, which are related to **microelectromechanical systems** or MEMS.
- MEMS became practical once they could be fabricated using modified semiconductor device fabrication technologies, normally used to make electronics.



Top-down and bottom-up approaches

Top-down approach

Micro/nano electronics and MEMS technologies are relied on top-down approach (lithography based approach)

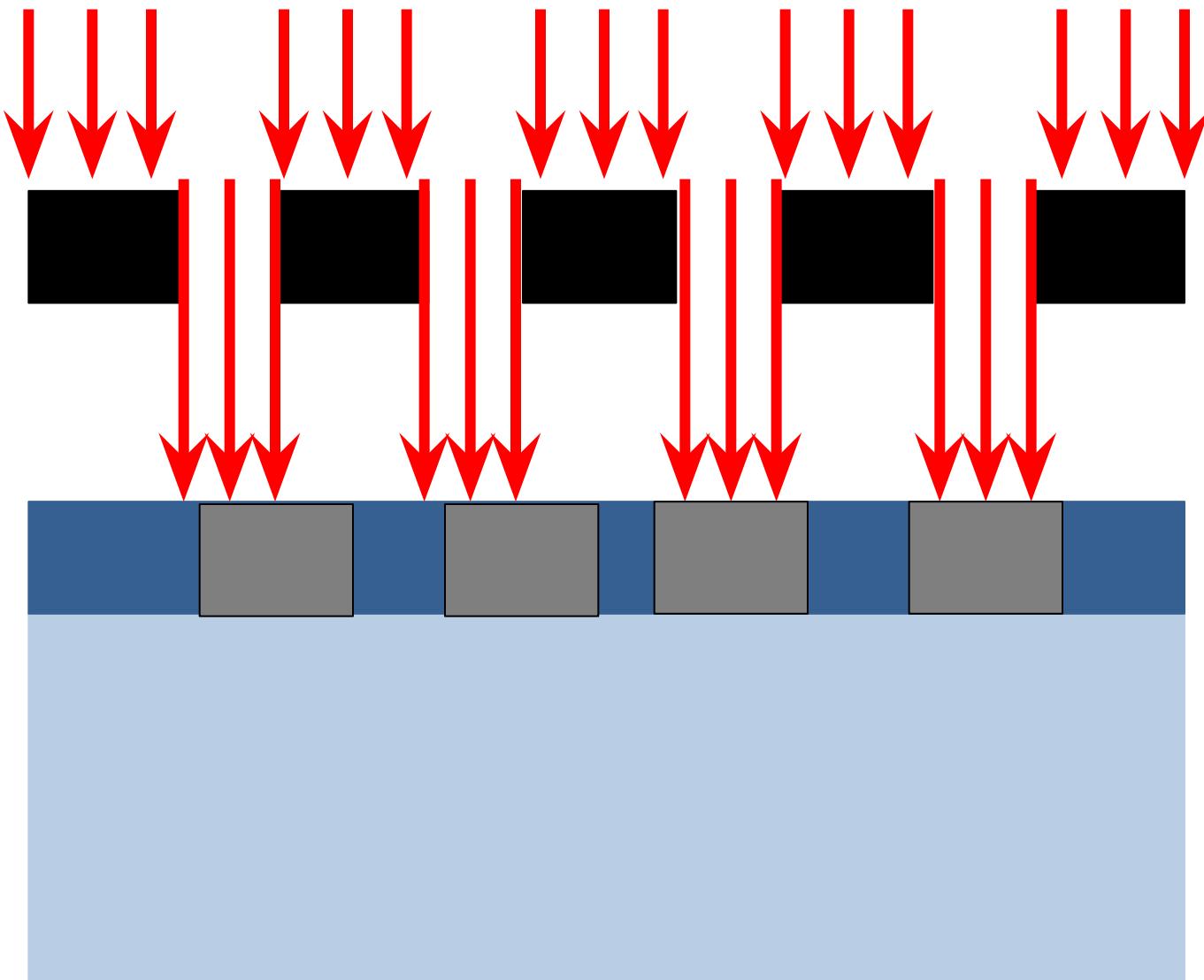
Top down fabrication can be likened to sculpting from a block of stone. A piece of the base material is gradually eroded until the desired shape is achieved. That is, you start at the top of the blank piece and work your way down removing material from where it is not required.

Nanotechnology techniques for top down fabrication vary but can be split into mechanical and chemical fabrication techniques.

The most top down fabrication technique is nanolithography. In this process, required material is protected by a mask and the exposed material is etched away. Depending upon the level of resolution required for features in the final product, etching of the base material can be done chemically using acids or mechanically using ultraviolet light, x-rays or electron beams. This is the technique applied to the manufacture of computer chips.

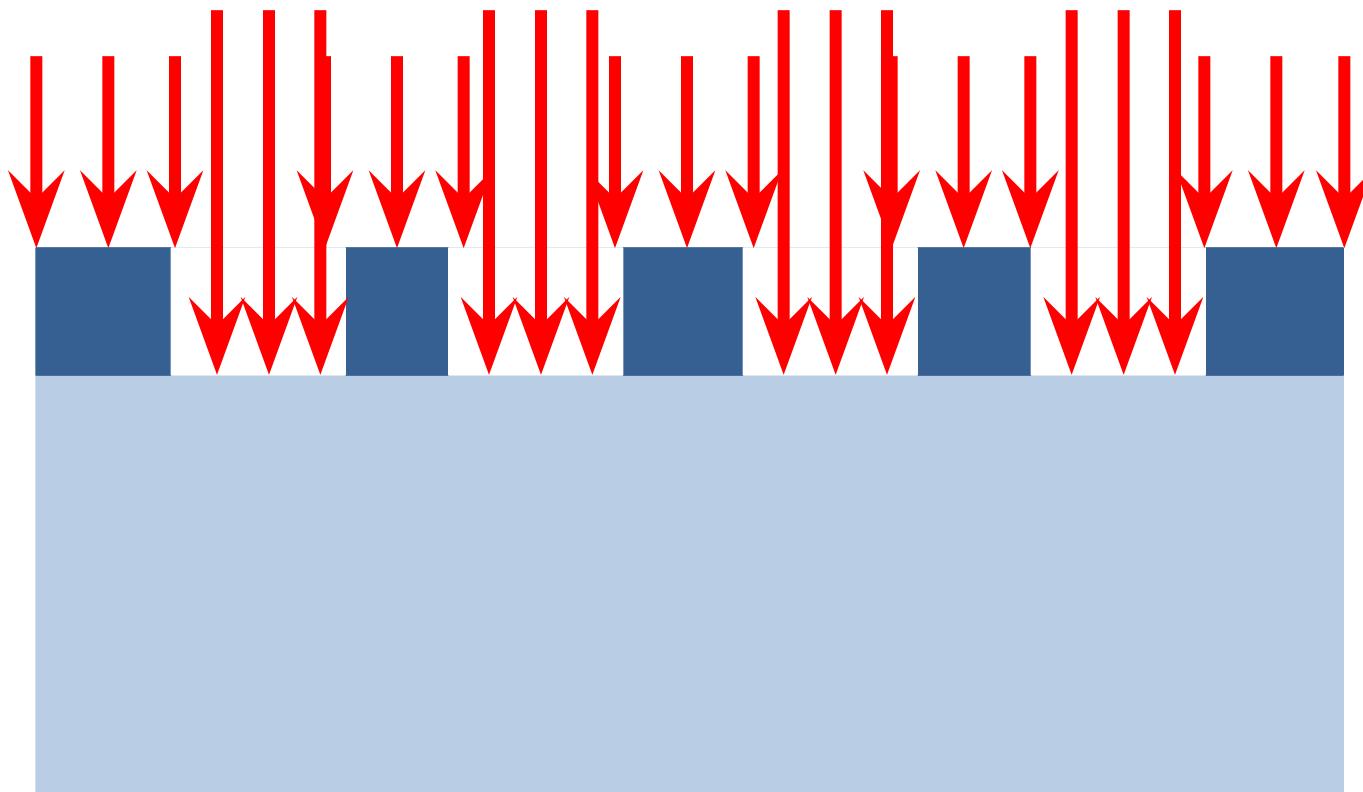
Silicon substrate

PR

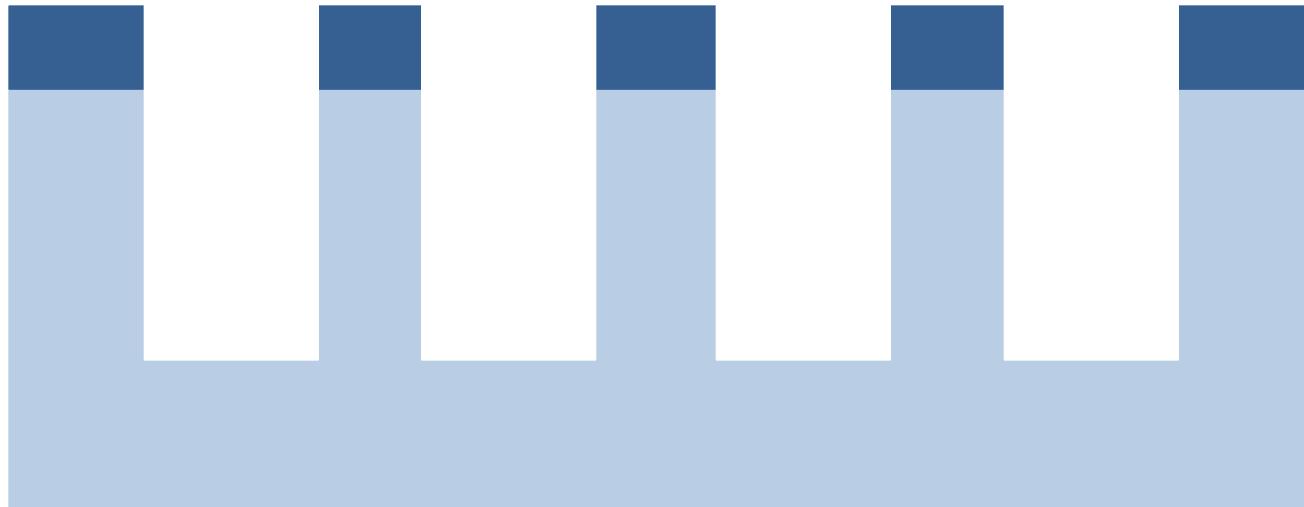


Lithography and developing

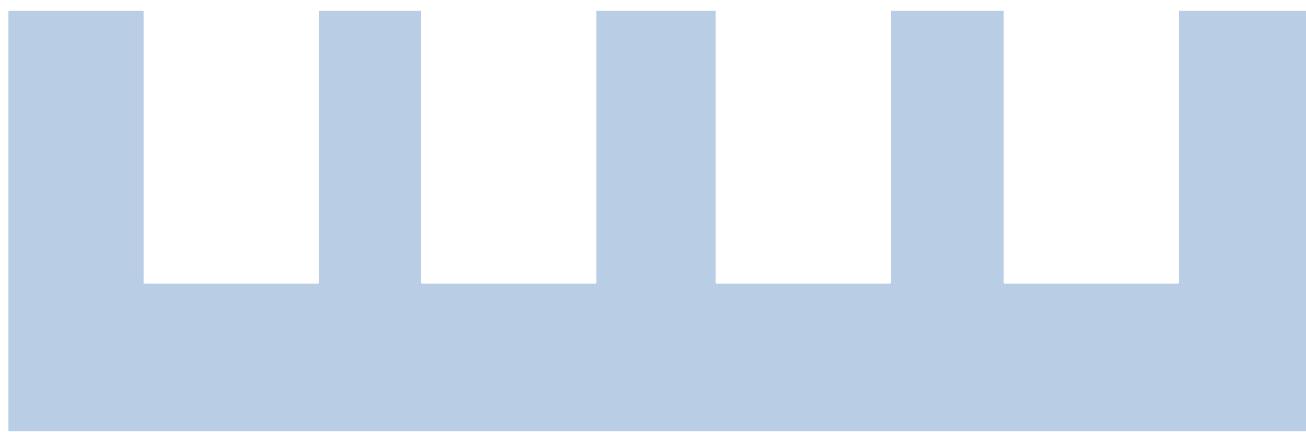
Etching the substrate

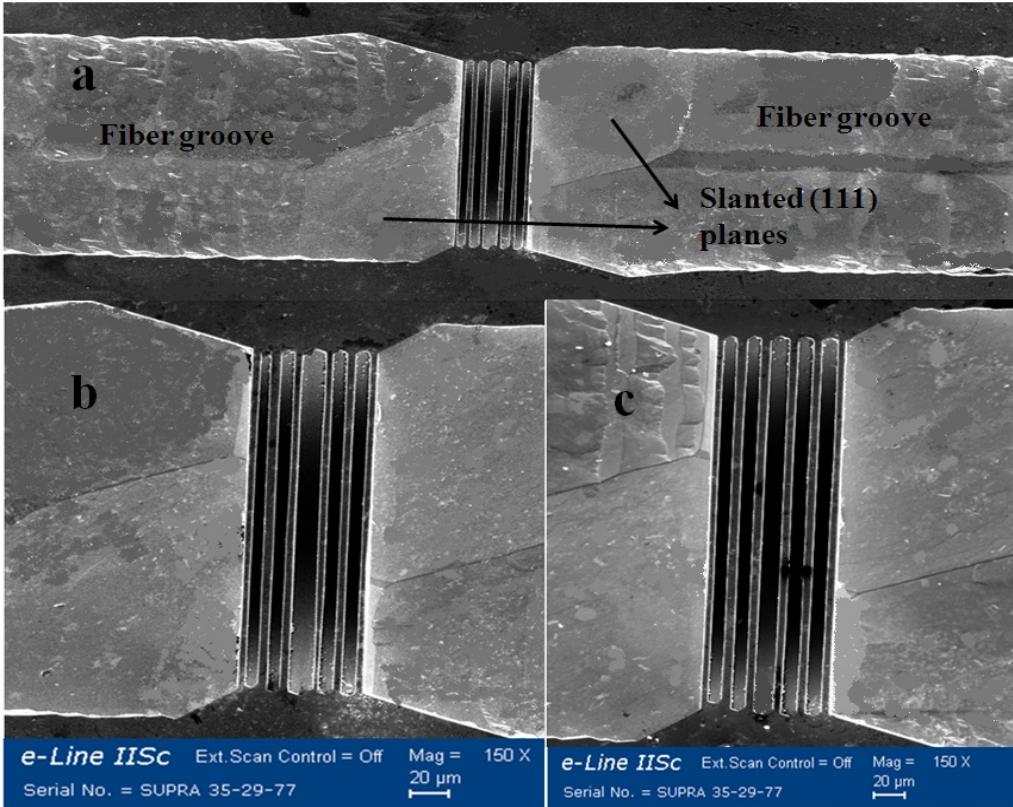


Final device after etching



Final device after cleaning

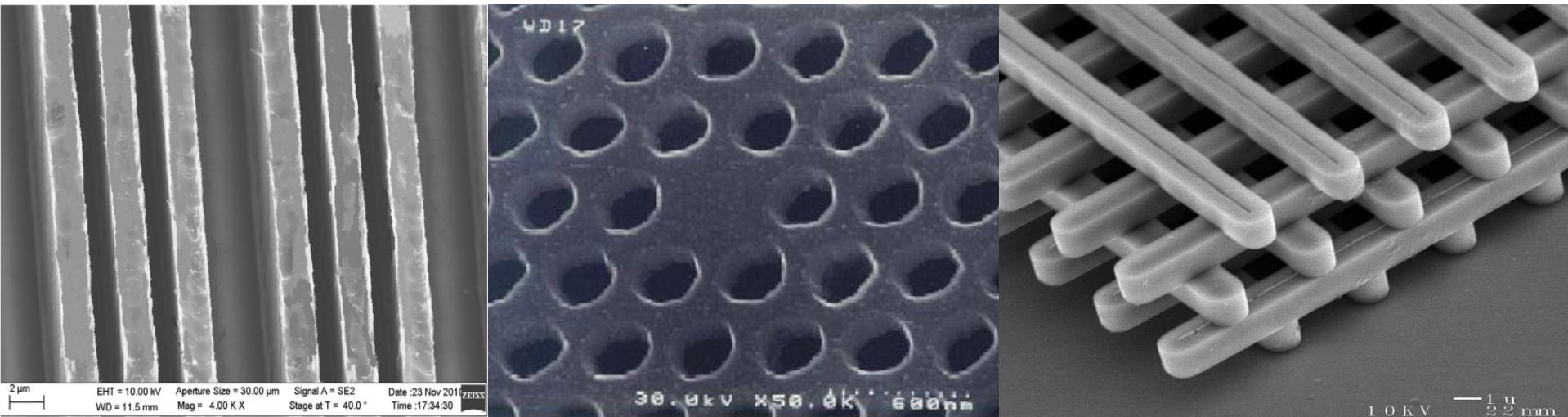




Single layer process
for 1D PCs

Single layer process
for 2D PCs

Multi layer process for
3D PCs



2 μm EHT = 10.00 kV Aperture Size = 30.00 μm Signal A = SE2 Date : 23 Nov 2016 ZEISS
WD = 11.5 mm Mag = 4.00 KX Stage at T = 40.0° Time : 17:34:30

30.0 kV x50.0k 600nm

10 KV 1/2 mm

Materials used

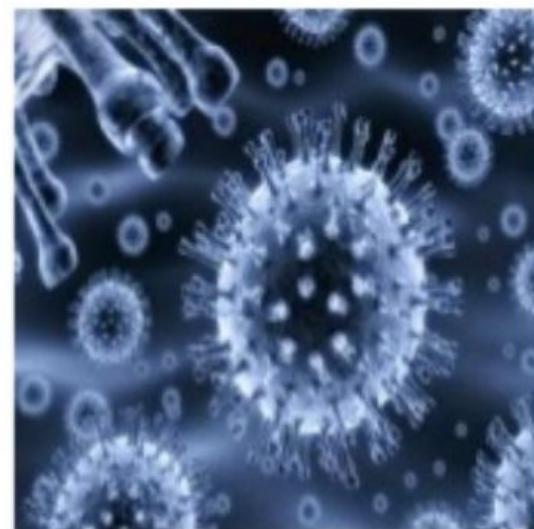
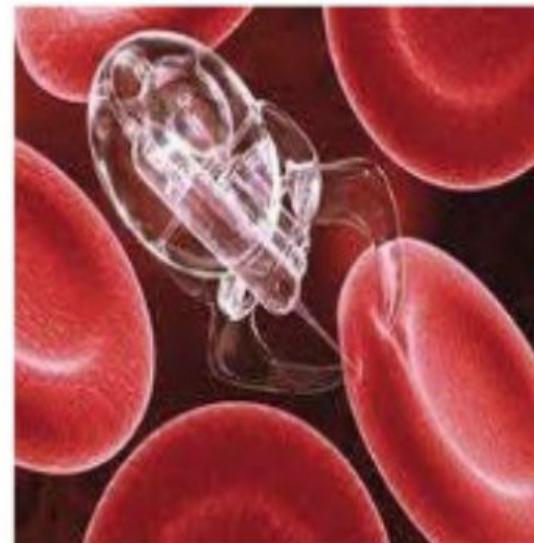
- Zinc oxide:
 - Dirt repellent, hydrophobic , cosmetics & stain resistant.
- Silver ion:
 - Healing property
- Aluminum silicate:
 - Scratch resistance
- Gold ion:
 - Chip fabrication, drug delivery.

Application Of Nanotechnology



Nanotechnology in Drugs(Cancer)

- Provide new options for drug delivery and drug therapies.
- Enable drugs to be delivered to precisely the **right location** in the body and release drug doses on a **predetermined schedule** for optimal treatment.
- Attach the drug to a **nanosized carrier**.
- They become localized at the disease site, i.e cancer tumour.
- Then they release medicine that **kills the tumour**.
- Current treatment is through radiotherapy or chemotherapy.
- Nanobots can **clear the blockage** in arteries.



Nanotechnology in Fabrics

- The properties of familiar materials are being changed by manufacturers who are adding **nano-sized components** to conventional materials to improve performance.
 - For example, some clothing manufacturers are making water and stain repellent clothing using **nano-sized whiskers** in the fabric that cause water to bead up on the surface.
 - In manufacturing **bullet proof jackets**.
 - Making **spill & dirt** resistant, antimicrobial, antibacterial fabrics.



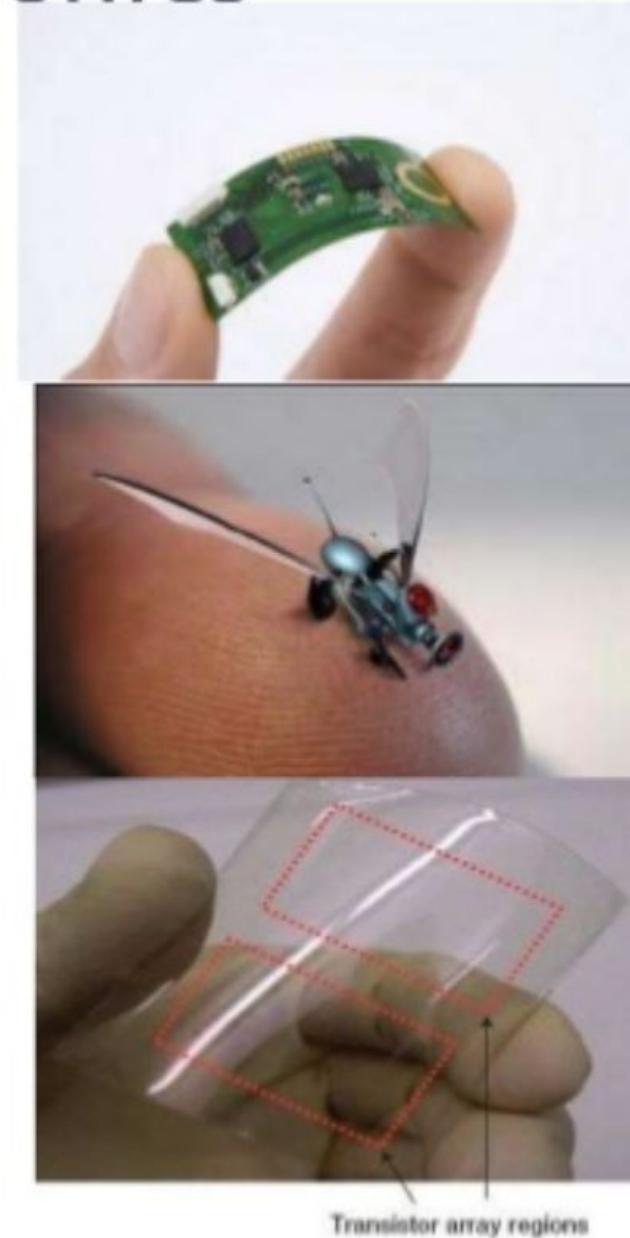
Nanotechnology in Mobile

- Morph, a nanotechnology concept device developed by Nokia Research Center (NRC) and the University of Cambridge (UK).
- The Morph will be **super hydrophobic** making it **extremely dirt repellent**.
- It will be able to **charge itself** from available light sources using photovoltaic **nanowire grass** covering it's surface.
- Nanoscale electronics also allow **stretching**. Nokia envisage that a nanoscale mesh of fibers will allow our mobile devices to be bent, stretched and folded into any number of conceivable shapes.



Nanotechnology in Electronics

- Electrodes made from **nanowires** enable flat panel displays to be flexible as well as thinner than current flat panel displays.
 - Nanolithography is used for fabrication of chips.
 - The transistors are made of nanowires, that are assembled on glass or thin films of **flexible plastic**.
 - E-paper, displays on sunglasses and map on car windshields.

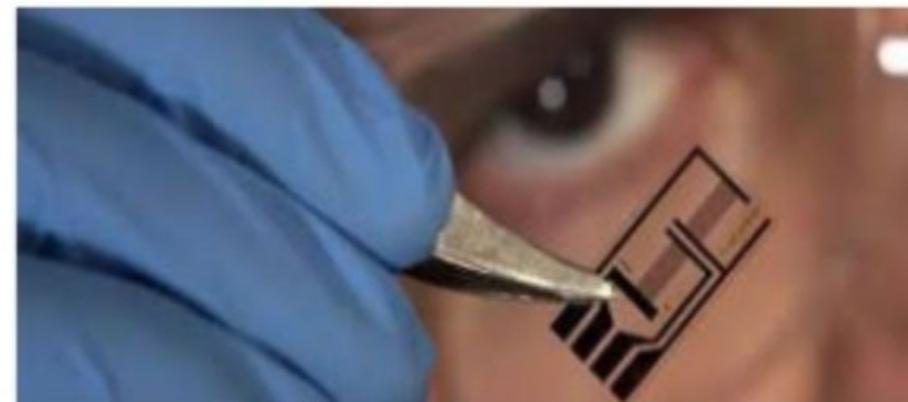
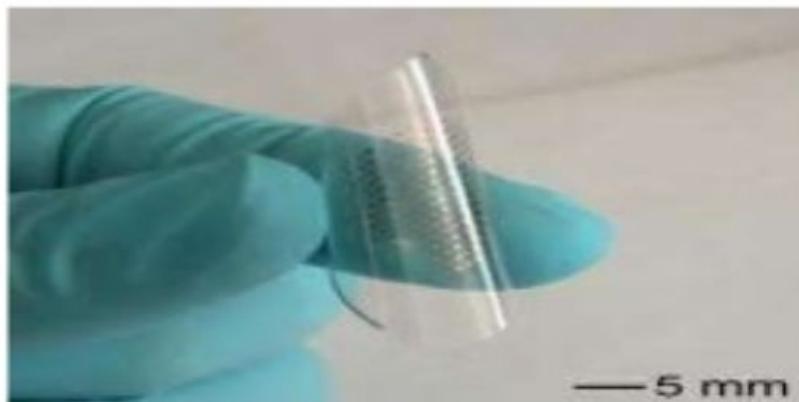


Nanotechnology in computers

- The silicon transistors in your computer may be replaced by transistors based on **carbon nanotubes**.
- A carbon nanotube is a molecule in form of a hollow cylinder with a diameter of around a nanometer which consists of pure carbon.
- **Nanorods** is a upcoming technology in the **displays techniques** due to less consumption of electricity and less heat emission.
- Size of the microprocessors are reduced to greater extend.
- Researchers at North Carolina State University says that growing arrays of magnetic nanoparticles, called **nanodots**.



- Hewlett Packard is developing a memory device that uses **nanowires coated with titanium dioxide**.
- One group of these nanowires is deposited parallel to another group.
- When a perpendicular nanowire is laid over a group of parallel wires, at each intersection a device called a **memristor** is formed.
- A memristor can be used as **a single-component memory cell** in an integrated circuit.
- By reducing the diameter of the nanowires, researchers believe memristor memory chips can achieve **higher memory density than flash memory chips**.
- Magnetic nanowires made of an **alloy of iron and nickel** are being used to create dense memory devices.



- Chips produced by Intel before “i” series processors were between **65nm -45nm**.
- Later with the help of nanotechnology **22nm** chips were made which itself is a milestone.

- **Advantages of using carbon nanotubes:**

- **Faster and smaller-** carbon nanotubes can be used to produce smaller and faster components.
- This will also result in computers that consume **less energy**.
- High speed and high capacity memory.
- Allows circuits to be **more accurate** on the atomic level.

Other uses

- Cutting tools made of **nanocrystalline materials**, such as tungsten carbide, tantalum carbide and titanium carbide, are more wear and **erosion-resistant**, and last longer than their conventional counterparts.
- **Silver nanocrystals** have been embedded in bandages to kill bacteria and prevent infection.
- Nanoparticulate-based **synthetic bone**
 - Formed by manipulating calcium and phosphate at the molecular level.
- **Aerogels** lightest known solid due to good insulating properties is used in space suits and are proposed to use in space craft.

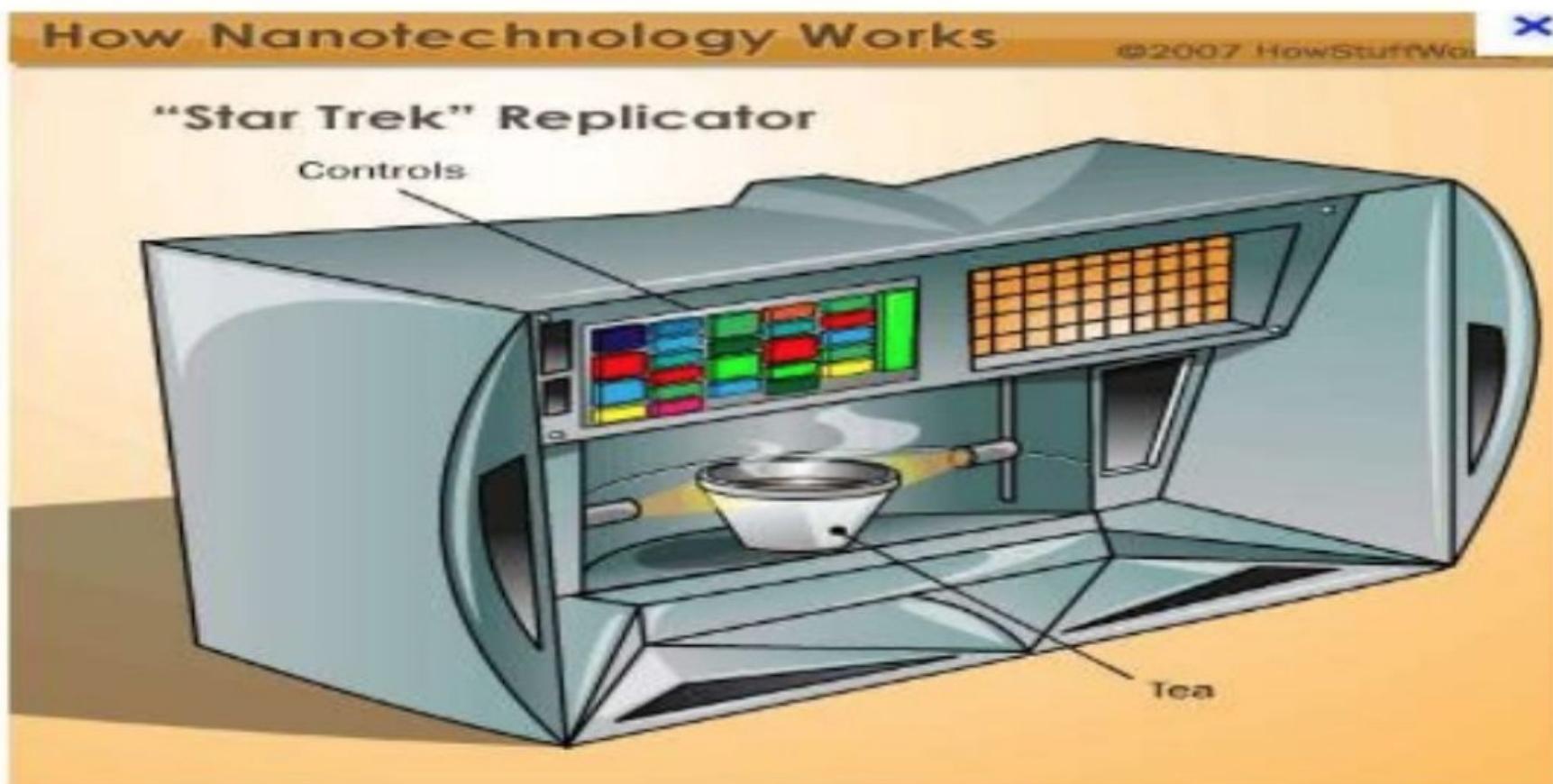
Nanotechnology in India

- IIT Mumbai is the premier organization in the field of nanotechnology.
- Research in the field of health, environment, medicines are still on.
- Starting in 2001 the Government of India launched the Nano Science and Technology Initiative (NSTI).
- Then in 2007 the Nanoscience and Technology Mission 2007 was initiated with an allocation of Rupees 1000 crores for a period of five years.
- The main objectives of the Nano Mission are:
 - basic research promotion,
 - infrastructure development for carrying out front-ranking research,
 - development of nano technologies and their applications,
 - human resource development and
 - international collaborations.

Possibilities for the future

- Nanotechnology may make it possible to manufacture **lighter, stronger, and programmable materials that**
 - require less energy to produce than conventional material
 - and that promise greater fuel efficiency in land transportation, ships, aircraft, and space vehicles.
- The future of nanotechnology could very well include the use of **nanorobotics**.
- These nanorobots have the potential to take on human tasks as well as tasks that humans could never complete. The rebuilding of the depleted ozone layer could potentially be able to be performed.

- There would be an entire nano surgical field to help cure everything from natural aging to **diabetes** to bone spurs.
- There would be almost nothing that couldn't be repaired (eventually) with the introduction of **nano surgery**.



Pitfalls of nanotechnology

- Nano-particles can get into the body through the skin, lungs and digestive system, thus creating free radicals that can cause **cell damage**.
- Once nano-particles are in the bloodstream, they will be able to cross the blood-brain barrier.
- The most dangerous Nano-application use for military purposes is the **Nano-bomb** that contain engineered self multiplying deadly viruses that can continue to wipe out a community, country or even a civilization.
- Nanobots because of their **replicating** behavior can be big threat for GRAY GOO.

Nanotechnology: product prospects - application trends

The Global market by the following Product Segments:

- Nano Devices
- Nano Materials
- Nano Tools.

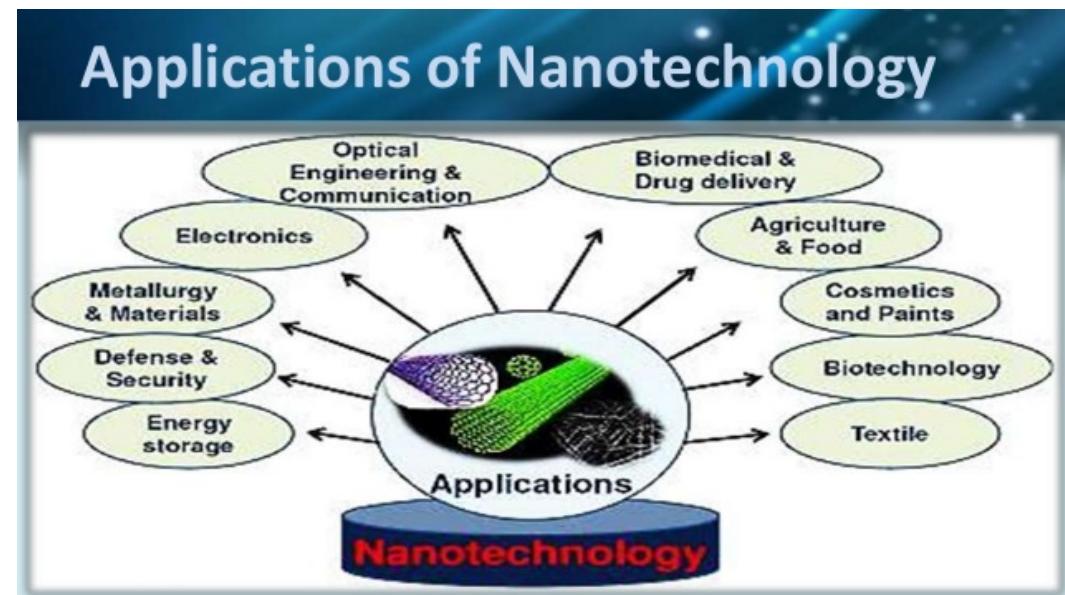
Key and niche players sin the field of Nanotechnology:

- *Advanced Diamond Technologies, Inc. (USA)*
- *Advanced Nano Products Co., Limited (South Korea)*
- *Altair Nanotechnologies Inc. (USA)*
- *Bruker Corporation (USA)*
- *Catalytic Materials, LLC (USA)*
- *Chemat Technology Inc. (USA)*
- *ELITech Group (France)*
- *eSpin Technologies, Inc. (USA)*
- *Hanwha Chemical Corporation (South Korea)*
- *Hybrid Plastics Inc. (USA)*
- *Hyperion Catalysis International, Inc. (USA)*
- *Integran Technologies, Inc. (Canada)*
- *Nanocyl S.A. (Belgium)*
- *Nano Materials Ltd. (Israel)*
- *Nanosys, Inc. (USA)*
- *Quantum Sphere, Inc. (USA)*
- *Rogue Valley Microdevices, Inc. (USA)*
- *Shenzhen Nanotech Port Co., Ltd. (China)*
- *Starpharma Holdings (Australia)*

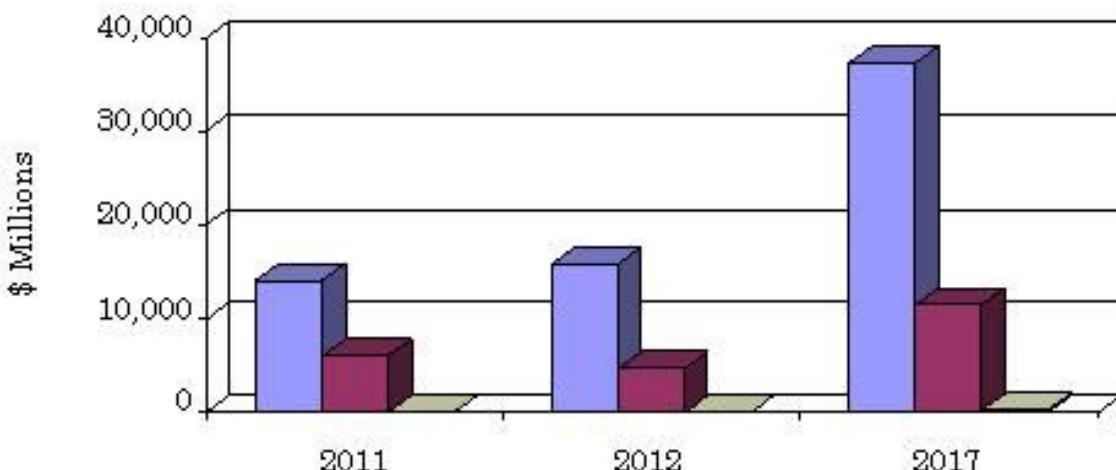
GLOBAL MARKET PERSPECTIVE

Total Companies Profiled: 358 (including Divisions/Subsidiaries 374)

- The United States (184)
- Canada (7)
- Japan (34)
- Europe (118)
 - France (6)
 - Germany (53)
 - The United Kingdom (24)
 - Italy (2)
 - Rest of Europe (33)
- Asia-Pacific (Excluding Japan) (26)
- Middle East (5)



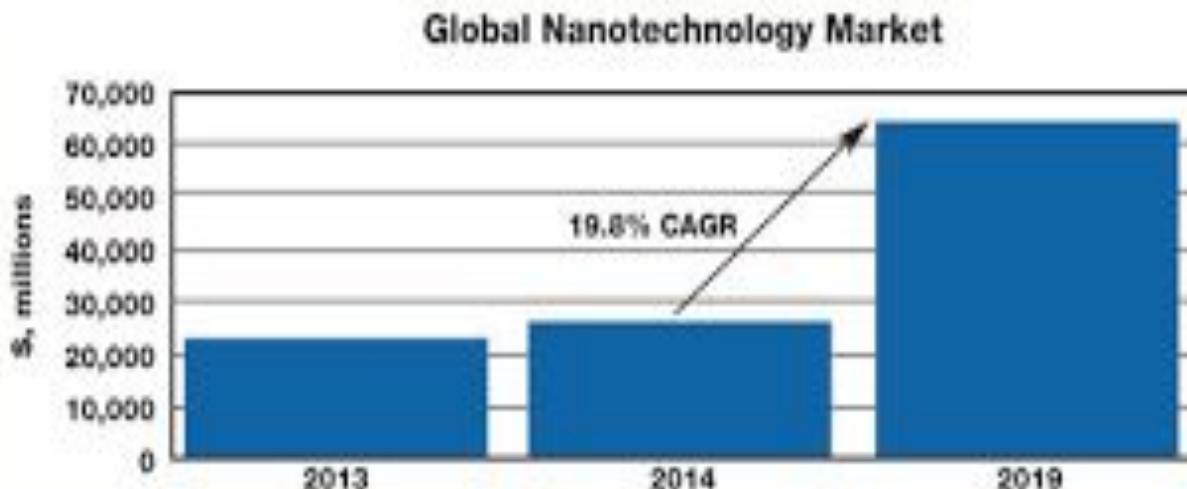
<https://www.slideshare.net/JohnsonYesudasAnthon/aerospace-nanotechnology>



GLOBAL NANOTECHNOLOGY MARKET, 2011-2017

■ Nanomaterials ■ Nanotools □ Nanodevices

[https://www.bccresearch.com/pressroom/nan/global-nanotechnology-market-reach-\\$48.9-billion-2017](https://www.bccresearch.com/pressroom/nan/global-nanotechnology-market-reach-$48.9-billion-2017)



Source: BCC Research (NANO11F), November 2014

<https://www.asminternational.org/c/portal/pdf/download?articleId=25986127&groupId=10192>