EXPERIMENT NO. 10

AIM: To Simulate Study of Convolutional codes

OBJECTIVE: Simulation study of Convolution codes

SOFTWARE: Code block Software, Turbo C++.

THEORY:

This experiment describes the encoder and decoder structures for convolutional codes. The encoder will be represented in many different but equivalent ways. Also, the main decoding strategy for convolutional codes, based on the Viterbi Algorithm, will be described. A firm understanding of convolutional codes is an important prerequisite to the understanding of turbo codes. 2.1 Encoder Structure

A convolutional code introduces redundant bits into the data stream through the use of linear shift registers as shown in Figure 2.1.

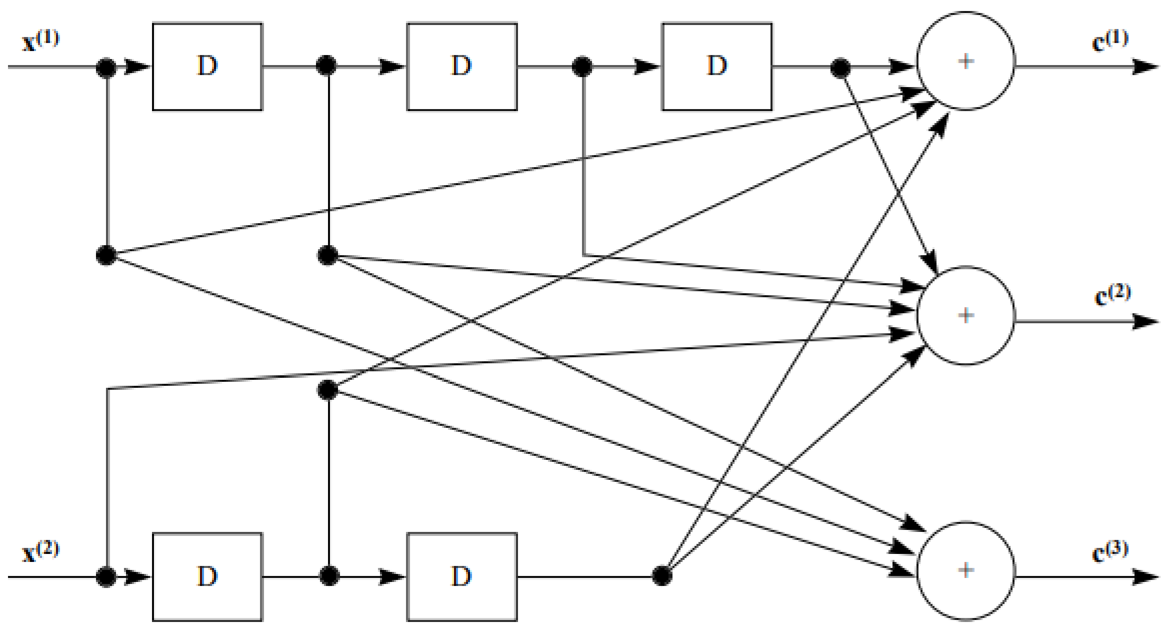

Figure 2.1: Example convolutional encoder where $x^{(i)}$ is an input information bit stream and $c^{(i)}$ is an output encoded bit stream [Wic95].

The information bits are input into shift registers and the output encoded bits are obtained by modulo-2 addition of the input information bits and the contents of the shift registers. The connections to the modulo-2 adders were developed heuristically with no algebraic or combinatorial foundation.

The code rate r for a convolutional code is defined as

$$r = \frac{k}{n}$$

where k is the number of parallel input information bits and n is the number of parallel output encoded bits at one time interval. The constraint length K for a convolutional code is defined as

$$K = m + 1$$

where m is the maximum number of stages (memory size) in any shift register. The shift registers store the state information of the convolutional encoder and the constraint length relates the number of bits upon which the output depends. For the convolutional encoder shown in Figure 2.1, the code rate r=2/3, the maximum memory size m=3, and the constraint length K=4. A convolutional code can become very complicated with various code rates and constraint lengths. As a result, a simple convolutional code will be used to describe the code properties as shown in Figure 2.2.

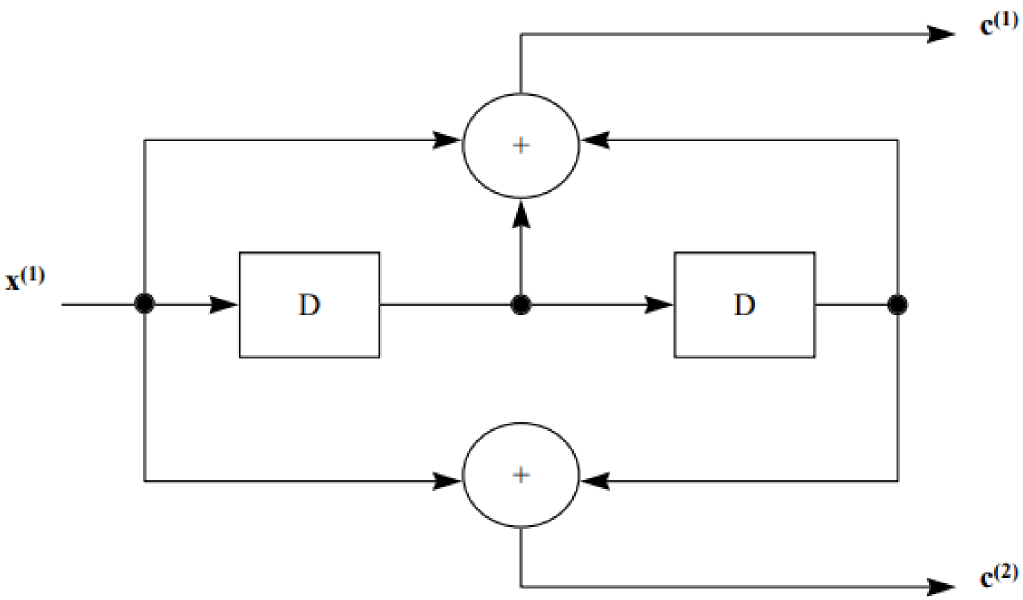

Figure 2.2: Convolutional encoder with k=1, n=2, r=1/2, m=2, and K=3.

Encoder Representations

The encoder can be represented in several different but equivalent ways. They are

1. Generator Representation
2. Tree Diagram Representation
3. State Diagram Representation
4. Trellis Diagram Representation

1. Generator Representation

Generator representation shows the hardware connection of the shift register taps to the modulo-2 adders. A generator vector represents the position of the taps for an output. A “1” represents a connection and a “0” represents no connection. For example, the two generator vectors for the encoder in Figure 2.2 are g1 = [111] and g2 = [101] where the subscripts 1 and 2 denote the corresponding output terminals.

2 Tree Diagram Representation

The tree diagram representation shows all possible information and encoded sequences for the convolutional encoder. Figure 2.3 shows the tree diagram for the encoder in Figure 2.2 for four input bit intervals.

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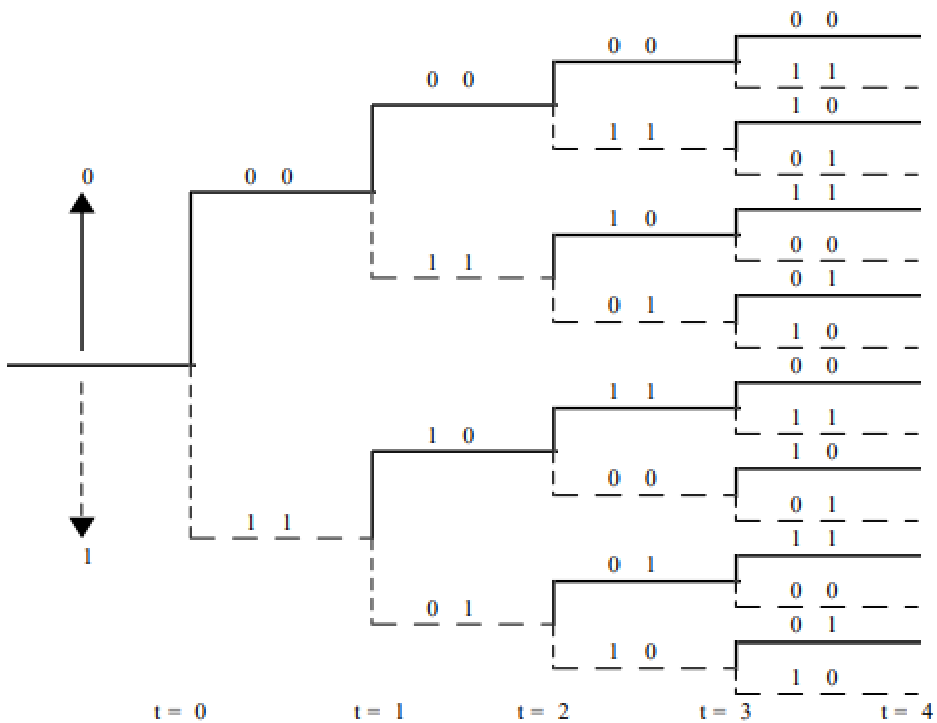

Figure 2.3: Tree diagram representation of the encoder in Figure 2.2 for four input bit intervals.

In the tree diagram, a solid line represents input information bit 0 and a dashed line represents input information bit 1. The corresponding output encoded bits are shown on the branches of the tree. An input information sequence defines a specific path through the tree diagram from left to right. For example, the input information sequence Fu-hua Huang Chapter 2. Convolutional Codes 7 x={1011} produces the output encoded sequence c={11, 10, 00, 01}. Each input information bit corresponds to branching either upward (for input information bit 0) or downward (for input information bit 1) at a tree node.

3 State Diagram Representation The state diagram shows the state information of a convolutional encoder. The state information of a convolutional encoder is stored in the shift registers. Figure 2.4 shows the state diagram of the encoder in Figure 2.2.

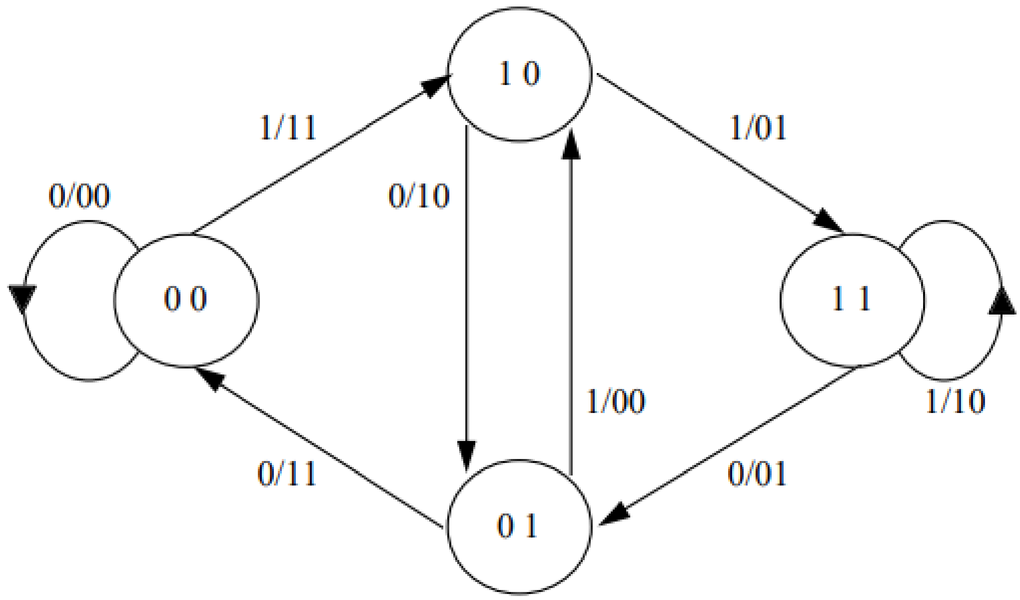

Figure 2.4: State diagram representation of the encoder in Figure 2.2.

In the state diagram, the state information of the encoder is shown in the circles. Each new input information bit causes a transition from one state to another. The path information between the states, denoted as x/c, represents input information bit x and output encoded bits c. It is customary to begin convolutional encoding from the all zero state. For example, the input information sequence x={1011} (begin from the all zero state) leads to the state transition sequence s={10, 01, 10, 11} and produces the output encoded sequence c={11, 10, 00, 01}. Figure 2.5 shows the path taken through the state diagram for the given example.

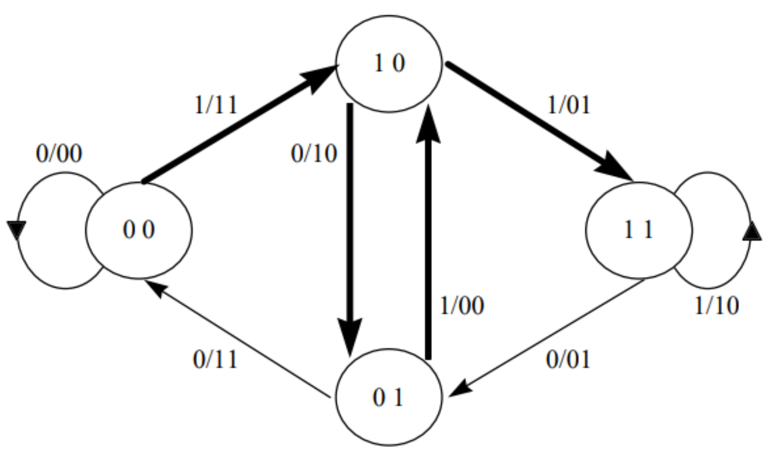

Figure 2.5: The state transitions (path) for input information sequence {1011}.

4 Trellis Diagram Representation

The trellis diagram is basically a redrawing of the state diagram. It shows all possible state transitions at each time step. Frequently, a legend accompanies the trellis diagram to show the state transitions and the corresponding input and output bit mappings (x/c). This compact representation is very helpful for decoding convolutional codes as discussed later. Figure 2.6 shows the trellis diagram for the encoder in Figure 2.2.

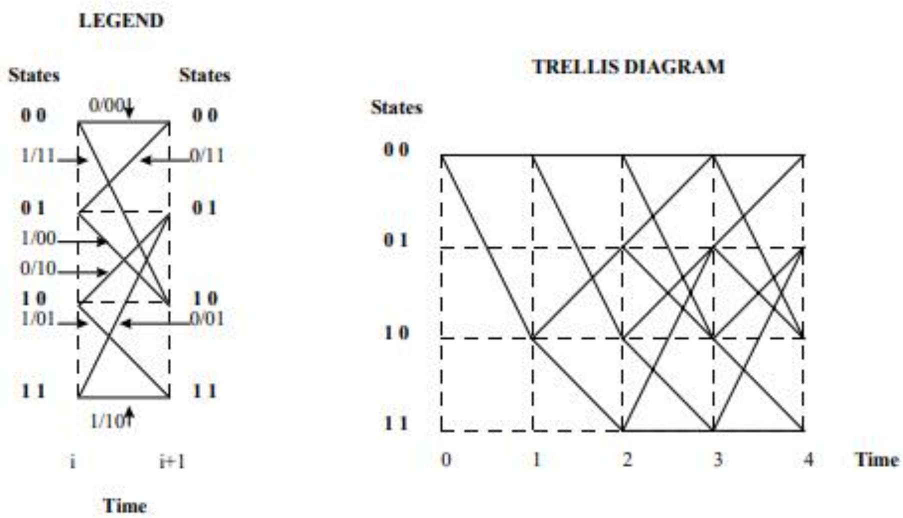

Figure 2.6: Trellis diagram representation of the encoder in Figure 2.2 for four input bit intervals.

Figure 2.7 shows the trellis path for the state transitions in Figure 2.5.

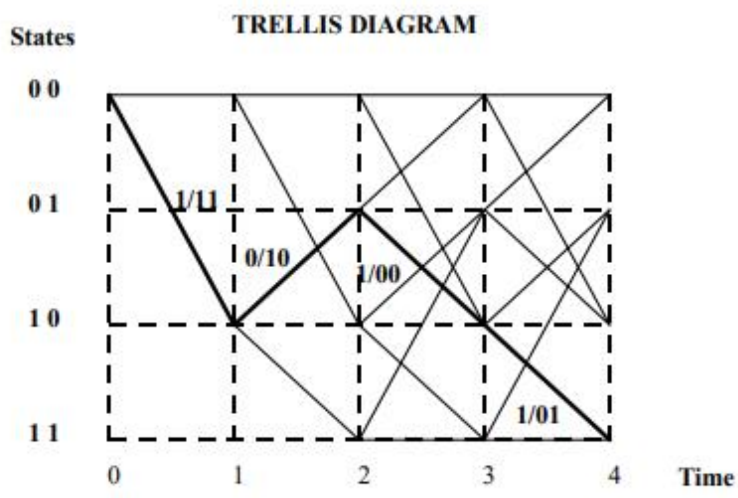

Figure 2.7: Trellis path for the state transitions in Figure 2.5.

Flowchart:

Algorithm:

Program:

Input,

Output,

Result:

Questions:

1. Define code rate related to convolutional codes?
2. Define coding gain and constraint Length?
3. Explain the methods of decoding of convolutional coding?

Conclusion:

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Timely Submission(10)	Journal Presenattaion(10)	Performance (10)	Understanding(10)	Oral(10)	Total (50)
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