# Project#3

***Course:*** Operating System

***Name:*** Fei Gao

## Replacement Algorithm

### FIFO

```
int fifo()
{
    int next = 0;
    if(counter < NUM_FRAME)
        next = counter;
    else counter = 0;
    counter++;
    return next;

}
```

### LRU

```
int lru()
{

    if(lru_flag == 1)
    {
        head = list_remove(head, frameIndex);
        head = list_insert_head(head, frameIndex);
    }
    if(lru_flag == 2)
    {
        while(head -> next != NULL)
        {
            head = head -> next;
        }
        frameIndex = head -> data;
        while(head -> prev != NULL)
        {
            head = head -> prev;
        }
        head = list_remove_tail(head);
        head = list_insert_head(head, frameIndex);
        return frameIndex;
    }
    else
    {
        head = list_remove(head, frameIndex);
        head = list_insert_head(head, frameIndex);
    }
    return 0;
}
```

## Clock

```
int clock()
{
    while(clockCounter[fifo_flag] == 1)
    {
        clockCounter[fifo_flag] = 0;
        fifo_flag++;
        fifo_flag = fifo_flag%NUM_FRAME;
    }
    clockCounter[fifo_flag] = 1;
    int fifo_pre = fifo_flag;
    fifo_flag++;

    return fifo_pre;
}
```

# Running Result

**Set `vm.h` as 0 3 8 2**

`./vm 1 < test_cases/belady_input.txt`

```
root@Discuz_for_Athens:/home/demo/project3/Fei/2/OS_Proj3# ./vm 1 < test_cases/belad
y_input.txt
Replacement Policy: 1 - FIFO
[pid 0, R] TLB:miss, Page:miss, 0x100 -> 0x0
[pid 0, R] TLB:miss, Page:miss, 0x200 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x300 -> 0x200
[pid 0, R] TLB:miss, Page:miss, 0x400 -> 0x0
[pid 0, R] TLB:miss, Page:miss, 0x100 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x200 -> 0x200
[pid 0, R] TLB:miss, Page:miss, 0x500 -> 0x0
[pid 0, R] TLB:miss, Page:hit, 0x100 -> 0x100
[pid 0, R] TLB:miss, Page:hit, 0x200 -> 0x200
[pid 0, R] TLB:miss, Page:miss, 0x300 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x400 -> 0x200
[pid 0, R] TLB:miss, Page:hit, 0x500 -> 0x0
====================================
Request: 12
Page Hit: 3 (25.00%)
Page Miss: 9 (75.00%)
TLB Hit: 0 (0.00%)
TLB Miss: 12 (100.00%)
Disk read: 9
Disk write: 0
```

`./vm 1 < test_cases/example_input.txt`

```
root@Discuz_for_Athens:/home/demo/project3/Fei/2/OS_Proj3# ./vm 1 < test_cases/examp
le_input.txt
Replacement Policy: 1 - FIFO
[pid 0, R] TLB:miss, Page:miss, 0x700 -> 0x0
[pid 0, R] TLB:miss, Page:miss, 0x0 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x100 -> 0x200
[pid 0, R] TLB:miss, Page:miss, 0x200 -> 0x0
[pid 0, R] TLB:miss, Page:hit, 0x0 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x300 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x0 -> 0x200
[pid 0, R] TLB:miss, Page:miss, 0x400 -> 0x0
[pid 0, R] TLB:miss, Page:miss, 0x200 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x300 -> 0x200
[pid 0, R] TLB:miss, Page:miss, 0x0 -> 0x0
[pid 0, R] TLB:miss, Page:hit, 0x300 -> 0x200
[pid 0, R] TLB:miss, Page:hit, 0x200 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x100 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x200 -> 0x200
[pid 0, R] TLB:miss, Page:hit, 0x0 -> 0x0
[pid 0, R] TLB:miss, Page:hit, 0x100 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x700 -> 0x0
[pid 0, R] TLB:miss, Page:miss, 0x0 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x100 -> 0x200
====================================
Request: 20
Page Hit: 5 (25.00%)
Page Miss: 15 (75.00%)
TLB Hit: 0 (0.00%)
TLB Miss: 20 (100.00%)
Disk read: 15
Disk write: 0
```

`./vm 2 < test_cases/example_input.txt`

```
root@Discuz_for_Athens:/home/demo/project3/Fei/2/OS_Proj3# ./vm 2 < test_cases/examp
le_input.txt
Replacement Policy: 2 - LRU
[pid 0, R] TLB:miss, Page:miss, 0x700 -> 0x0
[pid 0, R] TLB:miss, Page:miss, 0x0 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x100 -> 0x200
[pid 0, R] TLB:miss, Page:miss, 0x200 -> 0x0
[pid 0, R] TLB:miss, Page:hit, 0x0 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x300 -> 0x200
[pid 0, R] TLB:miss, Page:hit, 0x0 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x400 -> 0x0
[pid 0, R] TLB:miss, Page:miss, 0x200 -> 0x200
[pid 0, R] TLB:miss, Page:miss, 0x300 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x0 -> 0x0
[pid 0, R] TLB:miss, Page:hit, 0x300 -> 0x100
[pid 0, R] TLB:miss, Page:hit, 0x200 -> 0x200
[pid 0, R] TLB:miss, Page:miss, 0x100 -> 0x0
[pid 0, R] TLB:miss, Page:hit, 0x200 -> 0x200
[pid 0, R] TLB:miss, Page:miss, 0x0 -> 0x100
[pid 0, R] TLB:miss, Page:hit, 0x100 -> 0x0
[pid 0, R] TLB:miss, Page:miss, 0x700 -> 0x200
[pid 0, R] TLB:miss, Page:hit, 0x0 -> 0x100
[pid 0, R] TLB:miss, Page:hit, 0x100 -> 0x0
====================================
Request: 20
Page Hit: 8 (40.00%)
Page Miss: 12 (60.00%)
TLB Hit: 0 (0.00%)
TLB Miss: 20 (100.00%)
Disk read: 12
Disk write: 0
```

**Set `vm.h` as 0 4 8 2**

```
./vm 1 < test_cases/belady_input.txt
```

```
root@Discuz_for_Athens:/home/demo/project3/Fei/2/OS_Proj3# ./vm 1 < test_cases/belad
y_input.txt
Replacement Policy: 1 - FIFO
[pid 0, R] TLB:miss, Page:miss, 0x100 -> 0x0
[pid 0, R] TLB:miss, Page:miss, 0x200 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x300 -> 0x200
[pid 0, R] TLB:miss, Page:miss, 0x400 -> 0x300
[pid 0, R] TLB:miss, Page:hit, 0x100 -> 0x0
[pid 0, R] TLB:miss, Page:hit, 0x200 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x500 -> 0x0
[pid 0, R] TLB:miss, Page:miss, 0x100 -> 0x100
[pid 0, R] TLB:miss, Page:miss, 0x200 -> 0x200
[pid 0, R] TLB:miss, Page:miss, 0x300 -> 0x300
[pid 0, R] TLB:miss, Page:miss, 0x400 -> 0x0
[pid 0, R] TLB:miss, Page:miss, 0x500 -> 0x100
====================================
Request: 12
Page Hit: 2 (16.67%)
Page Miss: 10 (83.33%)
TLB Hit: 0 (0.00%)
TLB Miss: 12 (100.00%)
Disk read: 10
Disk write: 0
```

**Set `vm.h` as 4 8 8 2**

```
./vm 1 < test_cases/small_input.txt
```

```
root@Discuz_for_Athens:/home/demo/project3/Fei/2/OS_Proj3# ./vm 1 < test_cases/small
_input.txt
Replacement Policy: 1 - FIFO
[pid 0, W] TLB:miss, Page:miss, 0x4a8 -> 0xa8
[pid 0, W] TLB:miss, Page:miss, 0x7ae -> 0x1ae
[pid 1, W] TLB:miss, Page:miss, 0x303 -> 0x203
[pid 1, W] TLB:miss, Page:miss, 0x42e -> 0x32e
[pid 1, R] TLB:miss, Page:miss, 0x6ec -> 0x4ec
[pid 1, R] TLB:hit, Page:hit, 0x439 -> 0x339
[pid 1, W] TLB:miss, Page:miss, 0x7d0 -> 0x5d0
[pid 1, W] TLB:miss, Page:miss, 0x16 -> 0x616
[pid 0, R] TLB:hit, Page:hit, 0x742 -> 0x142
[pid 0, W] TLB:miss, Page:miss, 0x6e3 -> 0x7e3
[pid 1, W] TLB:miss, Page:miss, 0x5eb -> 0xeb
[pid 1, R] TLB:miss, Page:hit, 0x38e -> 0x28e
[pid 1, R] TLB:miss, Page:hit, 0x7bc -> 0x5bc
[pid 1, R] TLB:miss, Page:miss, 0x11e -> 0x11e
[pid 0, W] TLB:miss, Page:miss, 0x3e5 -> 0x2e5
[pid 1, W] TLB:hit, Page:hit, 0xac -> 0x6ac
[pid 1, W] TLB:miss, Page:hit, 0x52e -> 0x2e
[pid 0, W] TLB:miss, Page:miss, 0x471 -> 0x371
[pid 1, W] TLB:miss, Page:hit, 0x6a6 -> 0x4a6
[pid 1, R] TLB:hit, Page:hit, 0xd9 -> 0x6d9
====================================
Request: 20
Page Hit: 8 (40.00%)
Page Miss: 12 (60.00%)
TLB Hit: 4 (20.00%)
TLB Miss: 16 (80.00%)
Disk read: 12
Disk write: 4
```

`./vm 2 < test_cases/small_input.txt`

```
root@Discuz_for_Athens:/home/demo/project3/Fei/2/OS_Proj3# ./vm 2 < test_cases/small
_input.txt
Replacement Policy: 2 - LRU
[pid 0, W] TLB:miss, Page:miss, 0x4a8 -> 0xa8
[pid 0, W] TLB:miss, Page:miss, 0x7ae -> 0x1ae
[pid 1, W] TLB:miss, Page:miss, 0x303 -> 0x203
[pid 1, W] TLB:miss, Page:miss, 0x42e -> 0x32e
[pid 1, R] TLB:miss, Page:miss, 0x6ec -> 0x4ec
[pid 1, R] TLB:hit, Page:hit, 0x439 -> 0x339
[pid 1, W] TLB:miss, Page:miss, 0x7d0 -> 0x5d0
[pid 1, W] TLB:miss, Page:miss, 0x16 -> 0x616
[pid 0, R] TLB:hit, Page:hit, 0x742 -> 0x142
[pid 0, W] TLB:miss, Page:miss, 0x6e3 -> 0x7e3
[pid 1, W] TLB:miss, Page:miss, 0x5eb -> 0xeb
[pid 1, R] TLB:miss, Page:hit, 0x38e -> 0x28e
[pid 1, R] TLB:miss, Page:hit, 0x7bc -> 0x5bc
[pid 1, R] TLB:miss, Page:miss, 0x11e -> 0x41e
[pid 0, W] TLB:miss, Page:miss, 0x3e5 -> 0x3e5
[pid 1, W] TLB:hit, Page:hit, 0xac -> 0x6ac
[pid 1, W] TLB:miss, Page:hit, 0x52e -> 0x2e
[pid 0, W] TLB:miss, Page:miss, 0x471 -> 0x171
[pid 1, W] TLB:miss, Page:miss, 0x6a6 -> 0x7a6
[pid 1, R] TLB:hit, Page:hit, 0xd9 -> 0x6d9
====================================
Request: 20
Page Hit: 7 (35.00%)
Page Miss: 13 (65.00%)
TLB Hit: 4 (20.00%)
TLB Miss: 16 (80.00%)
Disk read: 13
Disk write: 4
```