EE520 | EE620 Project 2 Assignment

Assigned: Friday, October 03

Project 2 Due: Friday, October 31, 11:59 PM

Revision History:

1	Original created by: Dorin Patru, PhD
2	Updates for EE651 by: Mark A. Indovina
3	Updates for EE520 | EE 620 by: Mark A. Indovina
4	Updates for EE520 | EE 620 by: Mark A. Indovina
5	Updates for EE520 | EE 620 by: Mark A. Indovina

The grade for this project will be based on:

1. On the timely completion of your EDA Tutorial 2 assignment.
2. On the timely completion of your Project 2 assignment.
3. On a ~5 min. oral presentation and defense of your work, which you will give during lab as organized by the instructor and TA during the week the Project 2 is due, using the presentation template *mai_ee520_ee620_proj2_def_template.ppt* on mycourses. Your Project 2 Presentation (PPT only) is due online **1 hour before class on the day of your presentation**.
4. On the following files uploaded to the mycourses Project 2 Report dropbox:
    a. On the Project 2 engineering report (engineering report details are described later in this document), uploaded as a PDF copy to the mycourses drop box (PDF only), due: Friday, October 31, 11:59 PM.
    b. On the Project 2 database copy, uploaded to the mycourses drop box, due: Friday, October 31, 11:59 PM.
    c. NOTE: Due to the size of the files submitted, the mycourses Project 2 Report dropbox is configured to only keep one submission, therefore if you complete 3 submissions, only the files included with the last submission are kept. However, a submission is one or more files, therefore all required Project 2 files must be uploaded simultaneously as one submission to the mycourses dropbox.

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1. INTRODUCTION

    1. Follow the naming conventions for Project 1 where **fml** stands for the initials of your **first**, **middle** and **last** names.
    2. Follow all design and layout guidelines as noted in the Project 1 handout, including unique requirements per your assigned "bit code".
    3. Cell port/label/pin names can only use letters and numbers, must start with a letter, are case sensitive, and the MUST MATCH on all views (symbol, schematic, layout, verilog, functional). Industry standard is to use UPPERCASE letters for standard cell pin names. Note that use of any special characters in pin names will cause errors in downstream tools.

2. Project 2 ASSIGNMENT

    1. Enhance your standard cell library with the following gates/cells:
        a. A rising edge triggered D Flip Flop, DFF (library cell fml_dff), using two-phase non-overlapping clocks, per the MUX2 Implementation as shown in handout *mai_proj2_req_update.pdf*. The result is a circuit with 3 inputs, and 2 outputs.
        b. An XOR2 (library cell fml_xor2) gate. You can modify your AOI or OAI for this purpose.
    2. Using gates from your standard cell library capture the schematic of a Full Adder (FA) in a new cell at one hierarchical level (library cell fml_fa). Manually place the cells, and auto-route following the steps in EDA Tutorial 2. The result is a circuit with 3 inputs, and 2 outputs.
    3. For the DFF, XOR2, and FA, you must create all cell views as required in the Project 1 handout. Note: the Verilog module for your DFF is coded as a D-type master-slave flip-flop modeled using gate level primitives.
    4. Document Propagation Delay for the following paths:
        a. For the XOR2:
            i. A → Y↑
            ii. A → Y↓
            iii. B → Y↑
            iv. B → Y↓
        b. For the FA:
            i. A → S↑
            ii. A → S↓
            iii. B → S↑
            iv. B → S↓
            v. CI → S↑
            vi. CI → S↓
            vii. A → CO↑
            viii. A → CO↓
            ix. B → CO↑

x. B → CO↓
xi. CI → CO↑
xii. CI → CO↓

c. For the DFF (see mai_ff_clock_constraint_measure.pdf):
   i. Ø1 → Q↑
   ii. Ø1 → Q↓
   iii. Ø1 → QN↑
   iv. Ø1 → QN↓
   v. Ø1 → minimum pulse width high
   vi. Ø2 → minimum pulse width high
   vii. Ø1↓ → Ø2↑ minimum guard time

5. Using gates from your standard cell library capture the schematic of a Boundary Scan Cell (BSC) in a new cell at one hierarchical level (library cell fml_bsc). The schematic of a typical boundary scan cell is attached. Manually place the cells, and auto-route following the steps in EDA Tutorial 2. See the file mai_boundary_scan_overview.pdf for more Boundary Scan design details.
6. Using gates from your standard cell library capture the schematic of a 5-bit Boundary Scan Register (BSR) in a new cell at one hierarchical level (library cell fml_bsr5). Manually place all cells at one hierarchical level, and auto-route following the steps in EDA Tutorial 2.
7. Instantiate the FA and the 5-bit BSR (BSSUM) in a new cell at one hierarchical level (library cell fml_bssum). Manually connect 3 outputs of the register to the 3 inputs of the FA, and the 2 outputs of the FA to the inputs of the remaining 2 bits of the BSR. Tie unused BSR inputs to VDD or GND, your choice.

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8. Finally, instantiate both your BSSUM cell and the corner/quarter pad frame cell provided into a new cell, BSTEST (library cell fml_bstest). Connect all signals to the I/O pads using M2 and/or M3, and VDD and GND using M1. The latter should be as large as possible (see 10 below).
    c. Although your DFF requires two-phase non-overlapping clocks, the two-phase non-overlapping clocks are brought into your chip using I/O pads as follows:
        i. ClockDR:
            1. Ø1 ~ CDR1
            2. Ø2 ~ CDR2
        ii. UpdateDR:
            1. Ø1 ~ UDR1
            2. Ø2 ~ UDR2
9. Take care with the placement of cells as you build higher level blocks. Since these cells will eventually be stitched together as larger blocks and placed in the corner/quarter frame provided, poor early placement will eventually cause your final cell to not fit into the area allotted. You have been warned!
10. Build your blocks so that you can efficiently strap your rows with VCC / GND as shown in Figure 1 (layer colors in this example are not correct). Note that the power strapping should be at least 30 λ wide. The final connections from the straps to the VDD / GND pads should be at least 40 λ wide.

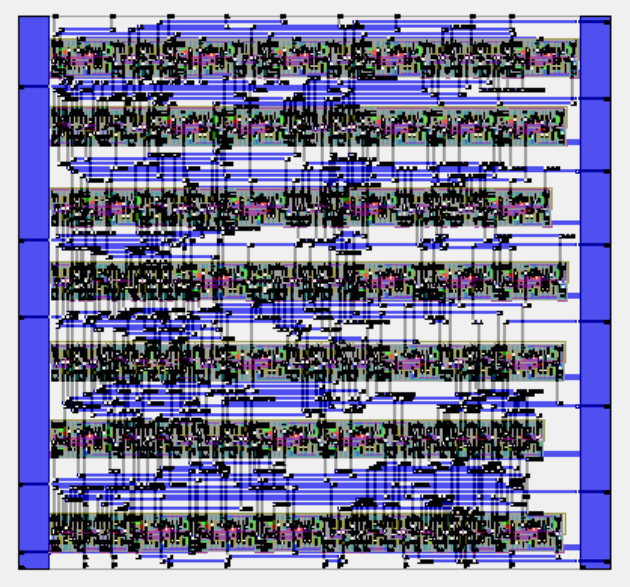

Figure 1 Example Standard Cell Block Layout

11. When routing cells follow these guidelines:
    a. After generating the initial layout from the schematic (*Design->Gen From Source*), manually place the VDD and GND pins and associated labels on top of a standard cell VDD / GND bus. For cells with multiple rows manually insert the power strapping (as noted in 10 above)

before exporting to the router. To efficiently constrain the router, the power strapping should be outside the PR boundary. Once in the router you must make M1 non-routable such that the router cannot route VDD / GND nets.

b. Since you will be using these cells with other routed cells and the quarter cell, optimize the pin placement (top, bottom, left, and right) to minimize routing when you place cells together as you build larger blocks.
c. Routing channel height:
    i. 26 λ top and bottom
    ii. 52 λ between rows

12. Due to the limited space in the quarter cell, floor plan your modes to leave adequate space on the left and right sides of your rows of cells for power strapping.
13. Cells must be designed so that they can be abutted horizontally (including flipped horizontally) without introducing design rule violations - test that your cells can be abutted in rows by placing multiple cells (of various types, including flipping each horizontally) in rows in a test layout and running DRC.
14. Cells must be designed so that they can be flipped and abutted horizontally GND to GND (preferred orientation) or VDD to VDD without introducing DRC or LVS violations - test that your cells can be flipped and abutted in rows by placing multiple cells (of various types) in a test schematic and rows in a test layout and running DRC and LVS.
15. All interconnections within the cell will be made using POLY1 (any direction), M1 (any direction) exclusively
    a. As a last resort and only if necessary to achieve an optimal cell design:
        i. You can use M2 (horizontal direction only)
        ii. You can use M3 (vertical direction only)
        iii. Note however that the auto router used in later labs will be routing using M2 (horizontal direction) and M3 (vertical direction). Any deviation from these strict rules horizontal / vertical rules and the router will create shorts.
16. All cells, including routed cells, must DRC and LVS clean (no warnings or errors).

3. PROJECT GRADING

As noted earlier, the grade for this project will be based on:

1. On the timely completion of your EDA Tutorial 2 assignment.
2. On the timely completion of your Project 2 assignment.
3. On a ~5 min. oral presentation and defense of your work, which you will give during lab as organized by the instructor and TA during the week the Project 2 is due, using the presentation template *mai_ee520_ee620_proj2_f2013_def_template.ppt* on mycourses. Your Project 2 Presentation (PPT only) is due online **1 hour before lab on the day of your presentation**.
4. On the Project 2 engineering project report (PDF only) which is due online **Friday, October 31, 11:59 PM**. The project report will contain:
    d. A title page. At a minimum your name, course name, name of library described in the report.
    e. A second, written discussion section presented in two parts as follows:
        i. A Design Constraints & Discussion section describing your library design constrains based on your individual "bit code". You should discuss how you approached designing your cells, including transistor sizing, etc. Comment here on any unfinished or not verified work.
        ii. A Final Remarks & Conclusion section discussion what went well, areas for improvement, and your overall thoughts on Project 1 and 2 and how you will utilize what you've learned as you design larger, more sophisticated digital systems.
    f. A third section which includes datasheets for all cells of your library, including the ones you have created for Project 1 and 2. Include all data sheet data as specified in Project 1 assignment handout, and include timing arc measurements and parasitic notes for the DFF, XOR2, and FA cells.
    g. A forth section which includes the schematic and layout views of each cell created using your library cells, ie your FA, BSR, BSSUM, and BSTEST cells.
    h. A fifth section which includes labeled, detailed simulation waveforms for cell BSSUM**.**
    i. You will be submitting a written report, and the quality of your library and block designs, comments, and summary will be evaluated based on your ability to communicate to others. Please take care with your grammar, punctuation and style. Points will be docked for poorly written documents.
    j. If you plan to print a hardcopy for yourself, make sure to change the black background to white before sending to the printer (instructions shown in Project 1 handout)

k. An example final project report can be found on mycourses as *ee520_eee620_example_project2_report.pdf*.

5. A copy of your database uploaded to mycourses per instructions found in *mai_520_620-database-upload.pdf* due: **Friday, October 31, 11:59 PM**.

Table 1 Project 2 Grading:

EDA Tutorial 2 Score	5%
Project 1 Feedback Updates Score	15%
All Cell Schematics Score	15%
All Cell Layouts Score	15%
All Cell Simulation Results Score (Except BSSUM)	15%
BSSUM Simulation Results Score	5%
Defense Score	5%
Project 2 Final Report Score (Including readability, grammar, spelling, format)	20%
Overall Quality Score	5%
Late Deduction	0%
Graded Total	**100%**

NOTE: Due to the size of the files submitted, the mycourses Project 2 Report dropbox is configured to only keep one submission, therefore if you complete 3 submissions, only the files included with the last submission are kept. However, a submission is one or more files, therefore all required Project 2 files must be uploaded simultaneously as one submission to the mycourses dropbox.

4. PROJECT PRESENTATION DELIVERABLE

Create your presentation using PowerPoint and upload to the drop box on mycourses. No printed version is necessary for the instructor.

5. PROJECT REPORT DELIVERABLE

Print your final project report to PDF and upload to the drop box on mycourses. No printed version is necessary for the instructor. Your final report must be one file containing all information required.

If you plan to print a hardcopy for yourself, you may want to change the black background to white before sending to the printer (instructions shown below). Do not change the background to white for the PDF version of your report.

For your records (and resume): It is recommended that you create a full color PDF plot of your final quarter cell layout. Ask for help if you cannot determine how to print to Postscript from the Cadence tools and convert your Postscript file to PDF.

6. PROJECT QUARTER CELL

Directions for accessing the quarter cell library will be discussed during the lab and can be found in the file *mai_corner_cell.pdf* posted to mycourses.

Figure 2 Project Corner Cell

7. BRIEF BOUNDARY SCAN OVERVIEW

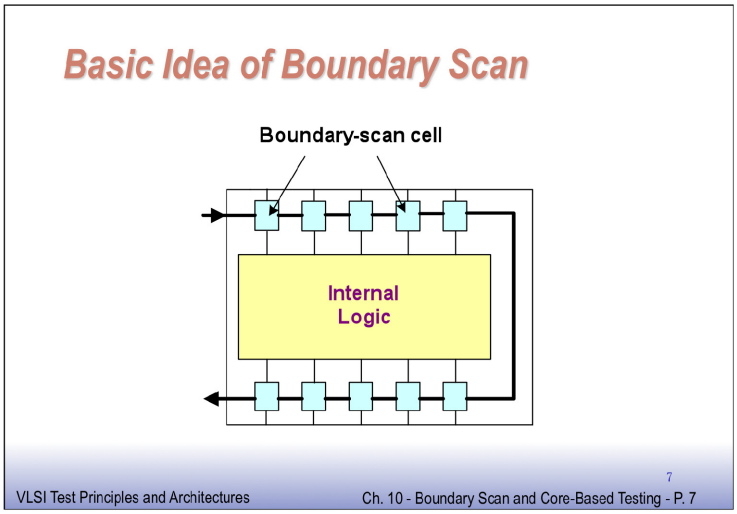

Figure 3 Boundary Scan Chain

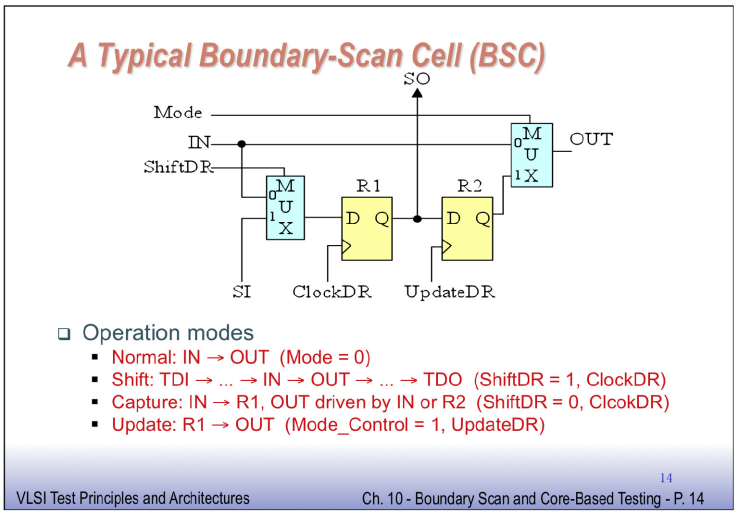

Figure 4 Boundary Scan Cell

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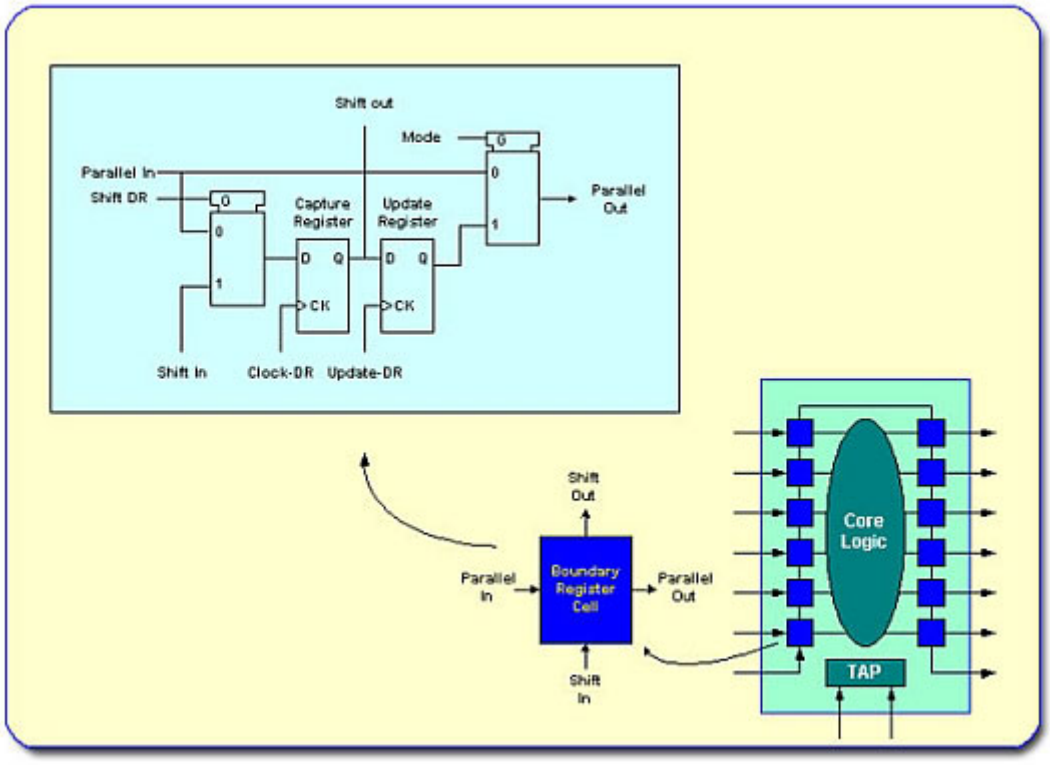

Figure 5 Boundary Scan showing TAP

Boundary Scan example only: A Test Access Port (TAP) is NOT required by Project 2