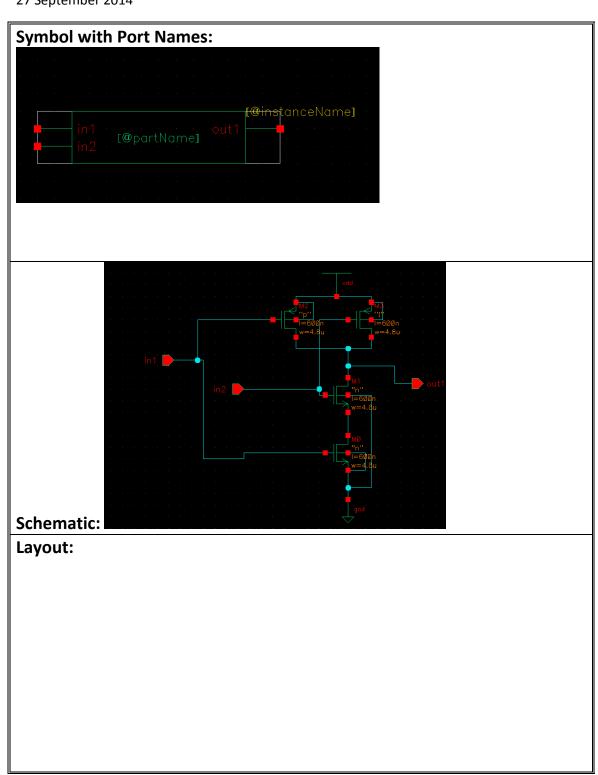
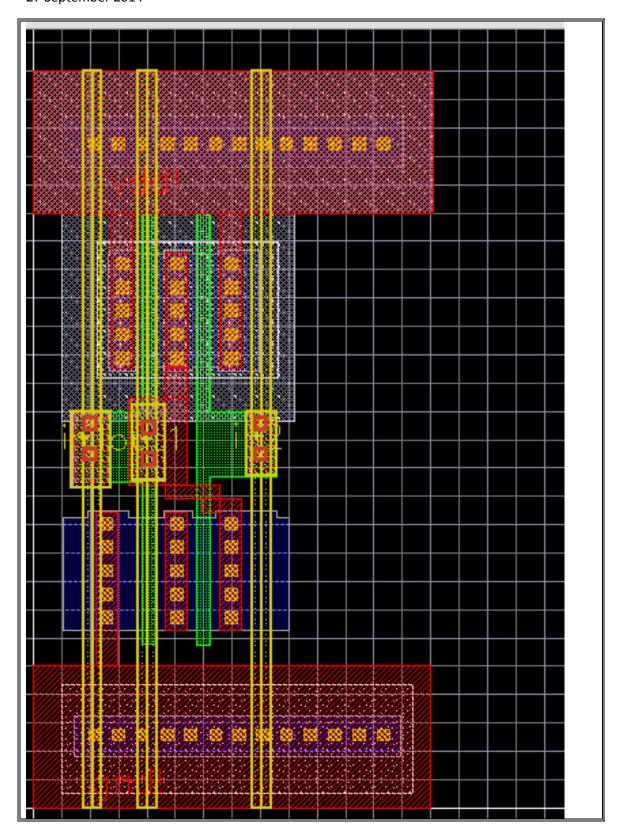
Name:_			

Library Name:	
Cell Name:	Zxw_nand
Function/Truth Table:	
0 0	1
0 1	1
1 0	1
1 1	0
Propagation Delay:	
Layout Area: 522.26um^2	





```
Verilog Model:
module zxw_nand (in1,in2,out1 );
         input in1;
         input in2;
         output out1;
         nand(out1,in1,in2);
endmodule
Comments/Notes:
zxw_nand.sp = (~/ee620) - GVIEW1
 <u>File Edit Jools Syntax Buffers Window Help</u>
 .SUBCKT zxw_nand vdd! gnd! in1 in2 out1
 * caps2d version: 7
    TRANSISTOR CARDS
RESISTOR AND CAP/DIODE CARDS
    Re1
Re2
Re3
Re4
Re5
Re6
Rc1
Rc2
Rc3
Rc4
Rc5
Rc6
Rc7
Rc8
Rc9
Rc10
Rc11
Rb1
Rb2
Rb3
     CAPACITOR CARDS
```

Name:	

<b>2</b> z	xw_nand	l.sp = (	(~/ee62	20) - G	VIEW1
	<u>E</u> dit				
				2	9
	DECT	TSTOP	AND CA	יחדחים	E CAPI
1	NESI	ISI OK	AND CA		
te1	inl# inl#		.n1#5 .n1#1		2.5015
te2 te3	inl#		.n1#1		2.5015
e4	in2#	# <u>1</u> i	.n 2#2	42	2.5000
te5 te6	in 24 in 24		.n2#3 .n2#4		). 8358 3. 3358
tc1	in1#	# <mark>1</mark> i	.n1#2	20	.5000
tc2	out]		ut1#4		6709
tc3 tc4	out] out]		ut1#1 ut1#5	1.747	E-02 ).5064
tc5	in2#	#5 i	.n 2#1	(	.5000
tc6 tc7	gnd! gnd!		ind! ind!#2		7. 7583 5. 4359
tc8	vdd!		dd!#3		). 5194
lc9	vdd!		dd!	5.549	
tc10 tc11			rdd!#4 rdd!#3		), 4445 5, 1538
tb1	inl	i	.n1#2	(	.5000
tb2	out]		ut1		. 0000
tb3	in2	1	.n 2#5		.5000
	CAPA	ACITOR	CARDS		
:1	in1#		ınd!#2		
:2 3	out] vdd!		.n1#5 .n1#4	2.616 9.349	
.4	vdd!		nd!#1		
.5	out]		dd!	3.994	
:6 :7	out]		.n2#2 rdd!#4	2.124 5.223	
:8	out]	l#5 i	.n 2#2	2,850	E-17
:9 :10	inl# outl		.n2#4 ind!#2	2.856	
:11		l#4 i		2.079	
:12		#4 i		2.694	
:13	out]	l#1 i !#2 i		3.569 1.279	
:15	in1#	#6 i	.n 2#3	1.003	E-17
:16 :17	vdd!			3.117	
:18	out] out]		.n2#2  nd!#1	7, 543	
:19	vdd!	!#1 i	n2#4	1.535	E-16
:20		l#4 i !#2 i		4.687 1.177	
.2.1	vuu.		1129	1.17.	2-10

