

**fml_lib : Standard Cell Library
&
Corner Cell Design Report**

EE 651

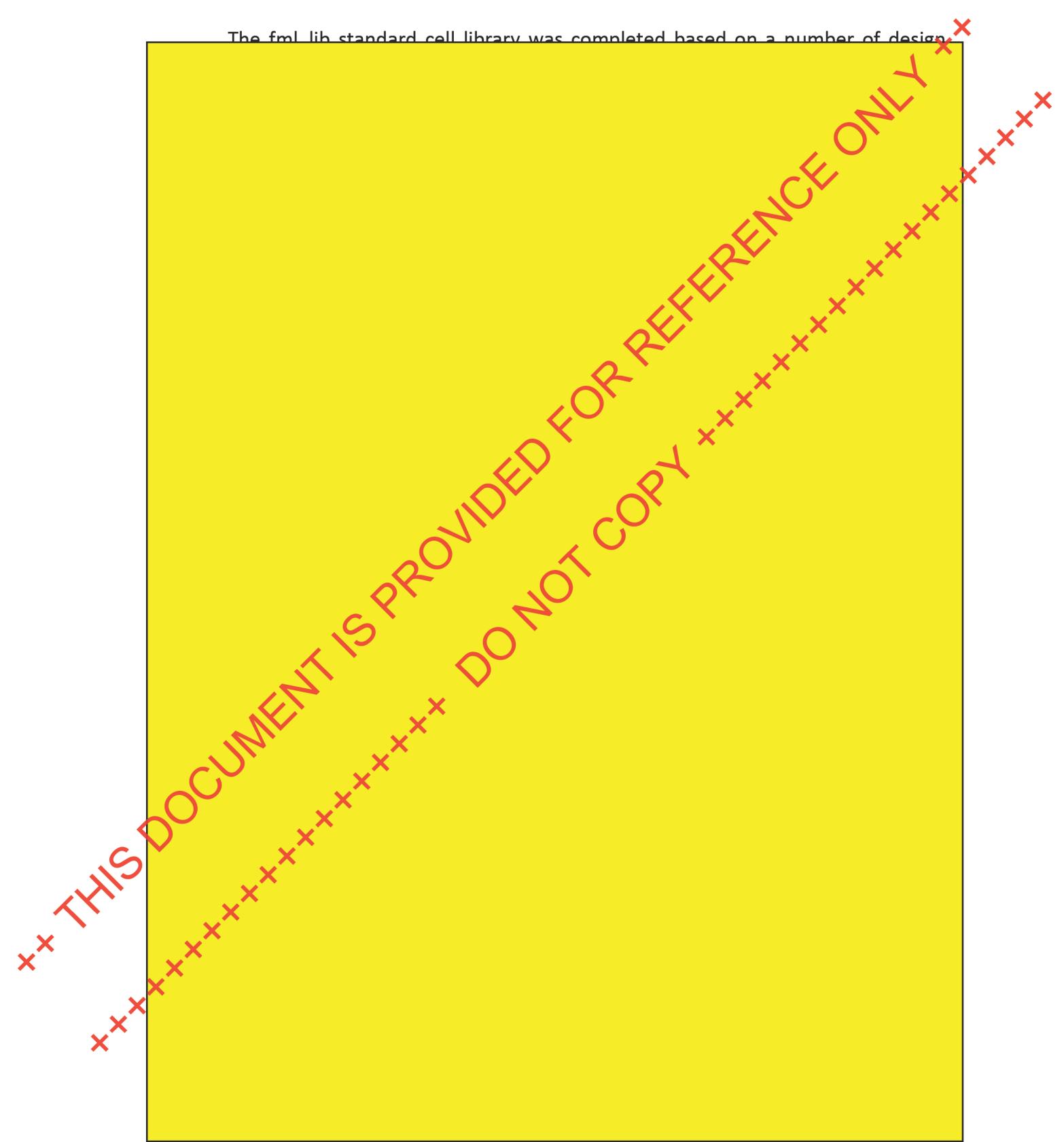
EE Student

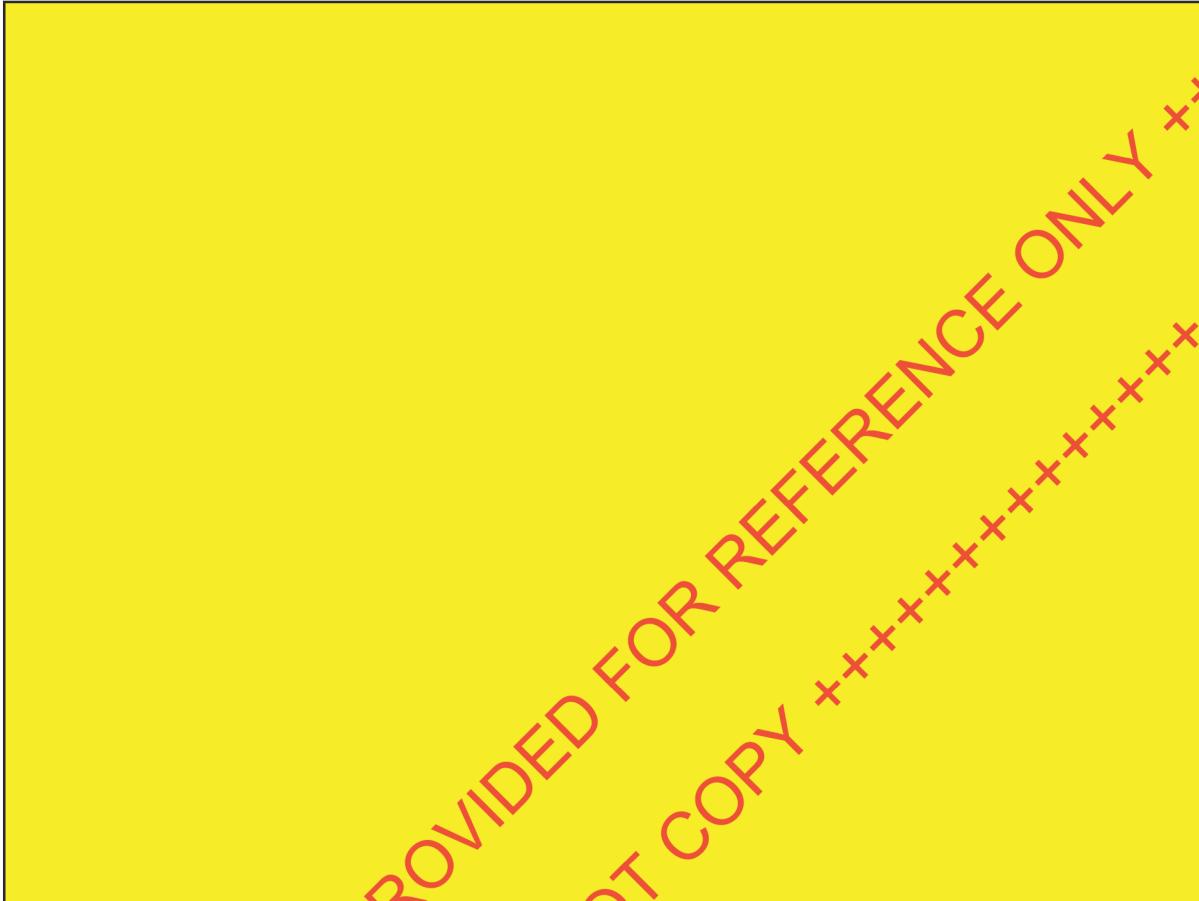
February 12th, 2013

*Many thanks to Jamison Whitesell for allowing his final report
to be used as an example document.*

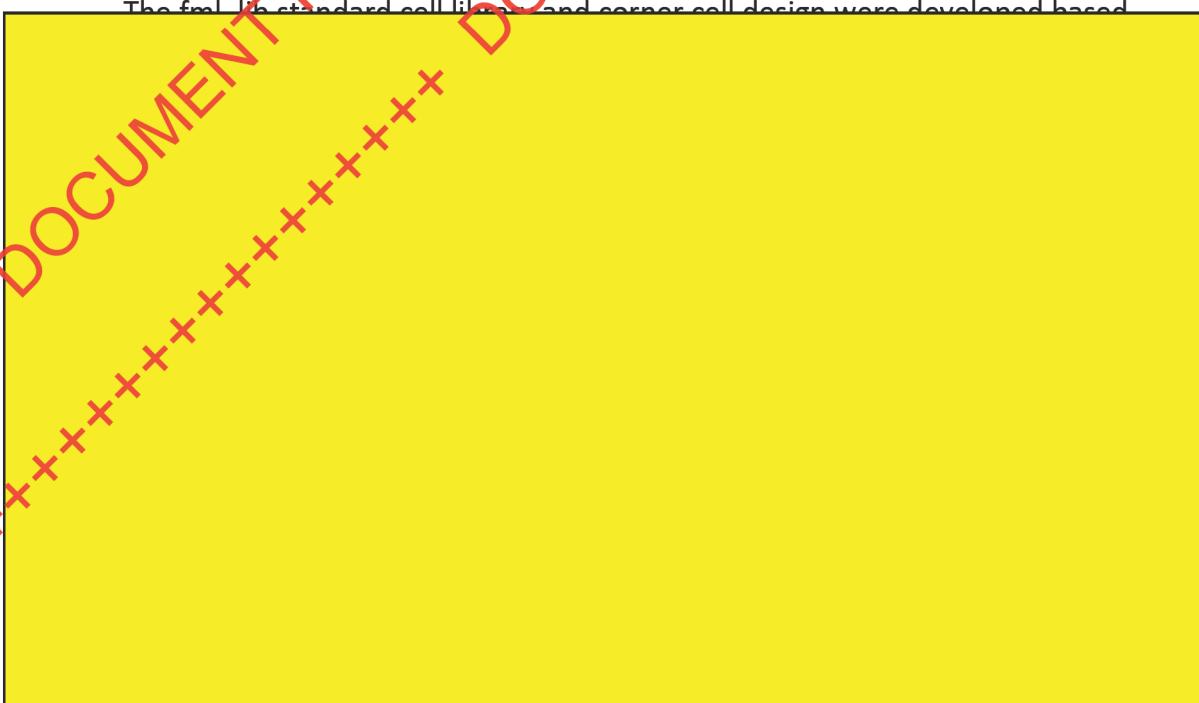
Design Constraints & Discussion

The fml.lib standard cell library was completed based on a number of design constraints.





Final Remarks and Conclusion



fml_lib: Standard Cell Library & Corner Cell Design Report

Standard Cell Datasheets

fml_inv:

Truth Table:

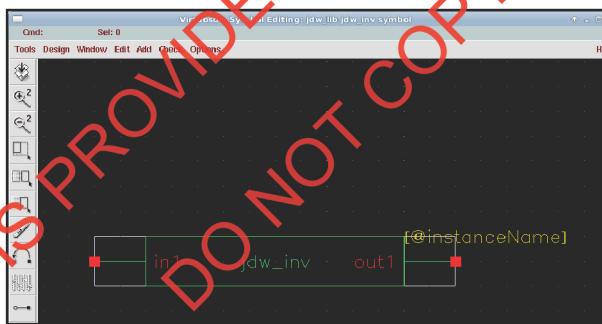
In1	Out1
0	1
1	0

Propagation Delay:

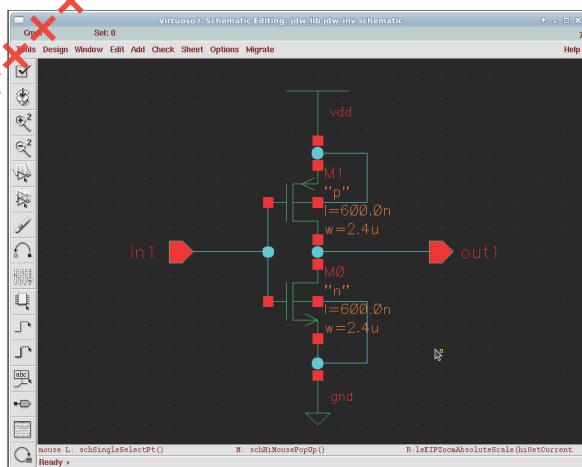
$\tau_{pd}: 0 \rightarrow 1$	-4.961 ns
$\tau_{pd}: 1 \rightarrow 0$	11.1935 ns

$$\text{Layout Area: } (24\lambda)(100\lambda) = 2400\lambda^2$$

Symbol:

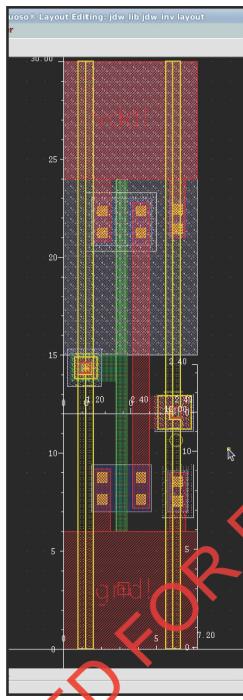


Schematic:



fml_lib: Standard Cell Library & Corner Cell Design Report

Layout:



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fml_lib: Standard Cell Library & Corner Cell Design Report

fml_nand2:

Truth Table:

In1	In2	Out1
0	0	1
0	1	1
1	0	1
1	1	0

Propagation Delay:

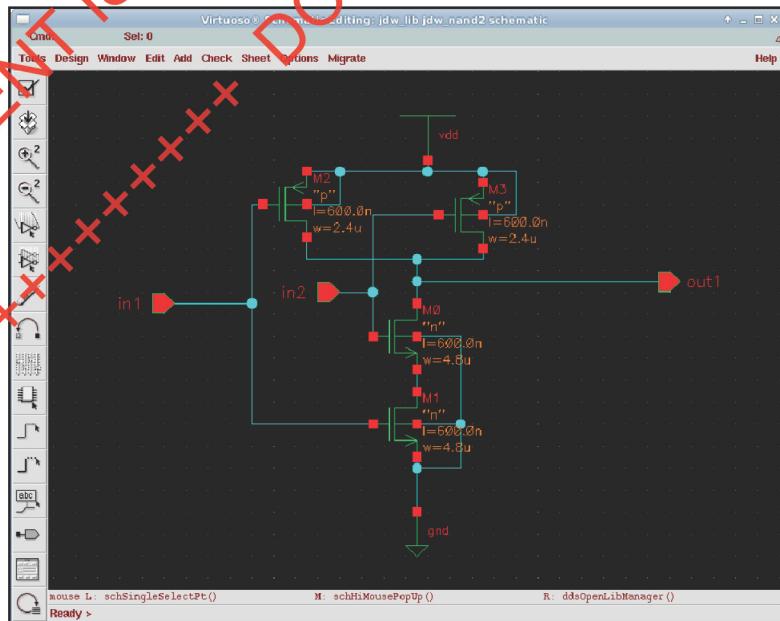
$\tau_{pd}: 11 \rightarrow 00$	5.811 ns
$\tau_{pd}: 00 \rightarrow 11$	-1.085 ns
$\tau_{pd}: 01 \rightarrow 11$	-14.731 ns

Layout Area: $(32\lambda)(100\lambda) = 3200\lambda^2$

Symbol:

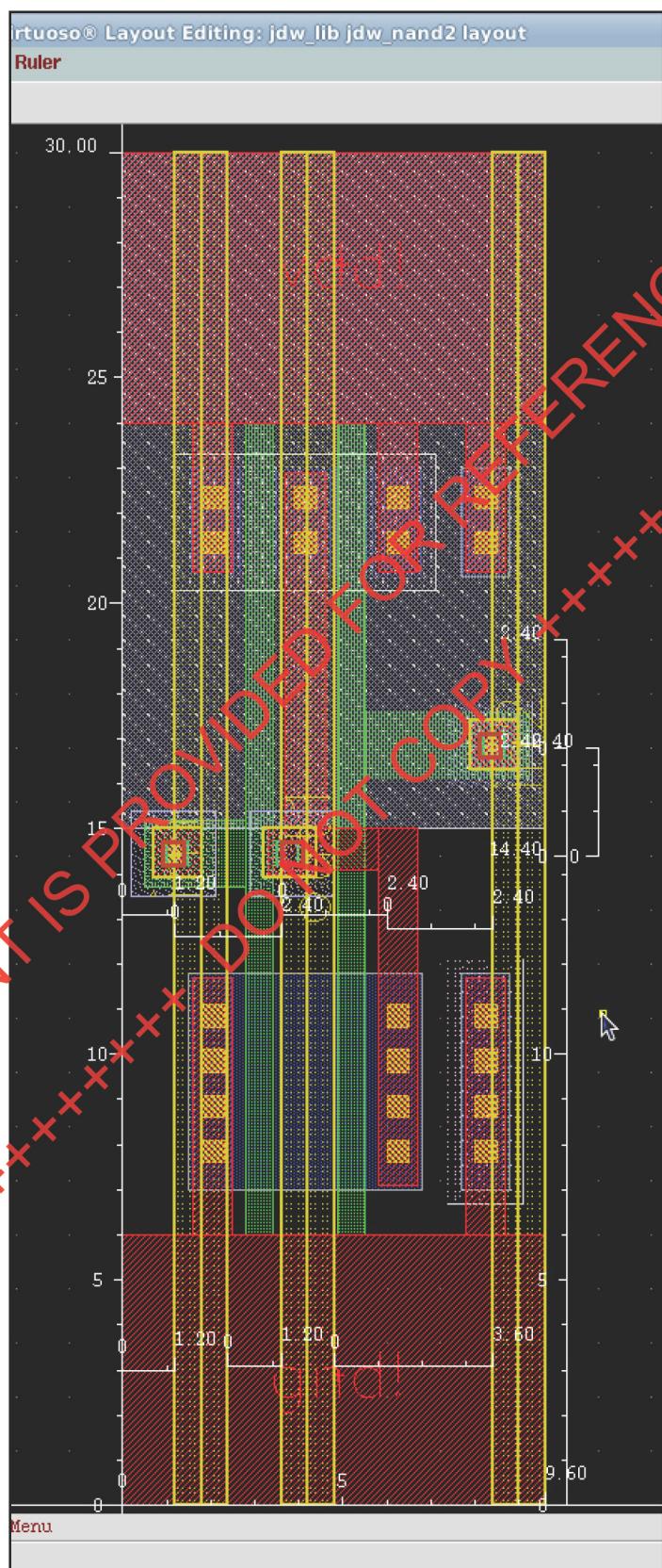


Schematic:



fml_lib: Standard Cell Library & Corner Cell Design Report

Layout:



fml_nor2:

Truth Table:

In1	In2	Out1
0	0	1
0	1	0
1	0	0
1	1	0

Propagation Delay:

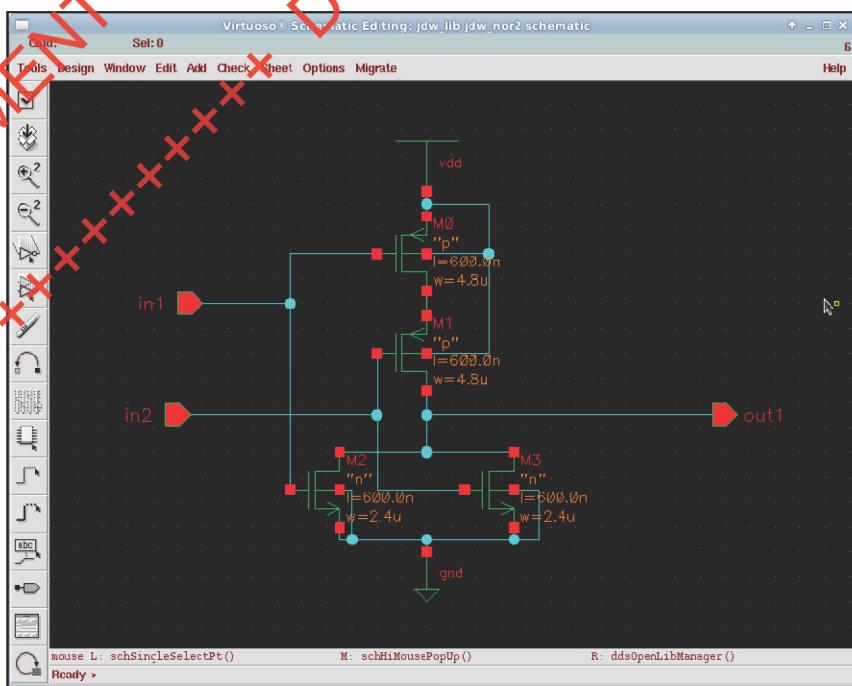
$\tau_{pd}: 11 \rightarrow 00$	17.179 ns
$\tau_{pd}: 00 \rightarrow 11$	-12.509 ns
$\tau_{pd}: 01 \rightarrow 11$	8.103 ns

$$\text{Layout Area: } (32\lambda)(100\lambda) = 3200\lambda^2$$

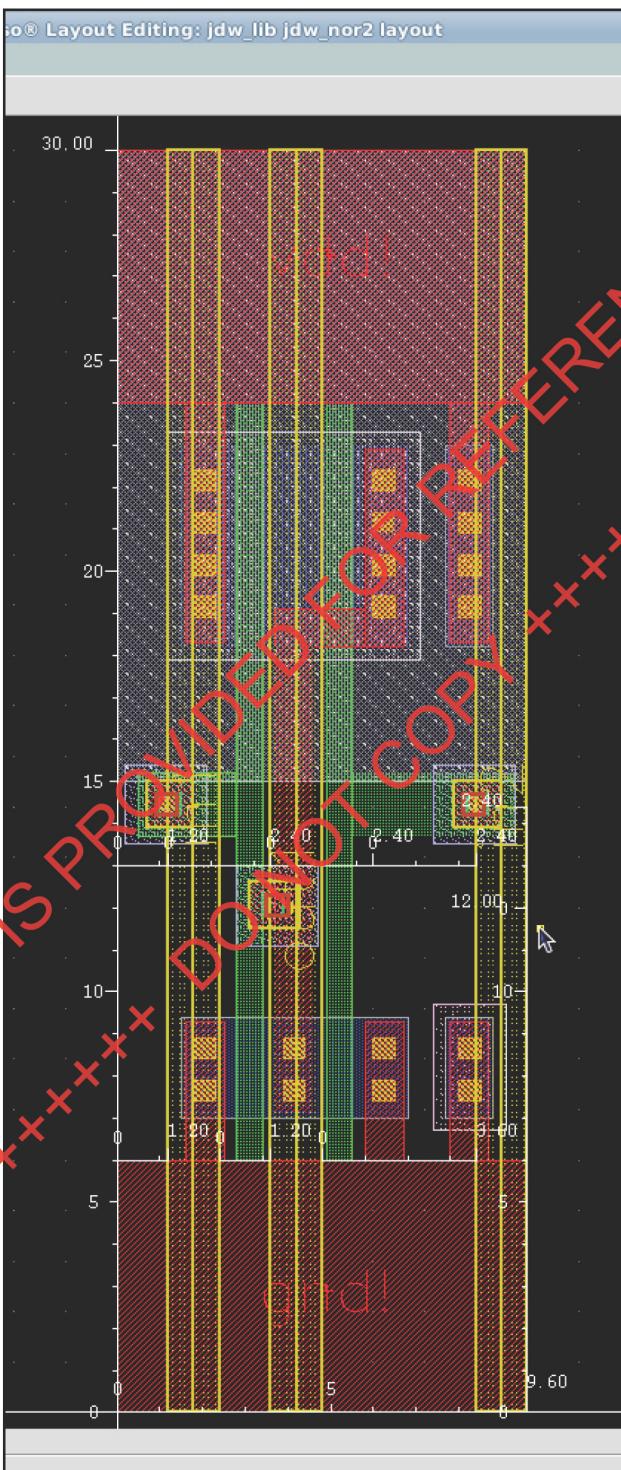
Symbol:



Schematic:



Layout:



fml_oai22:

Truth Table:

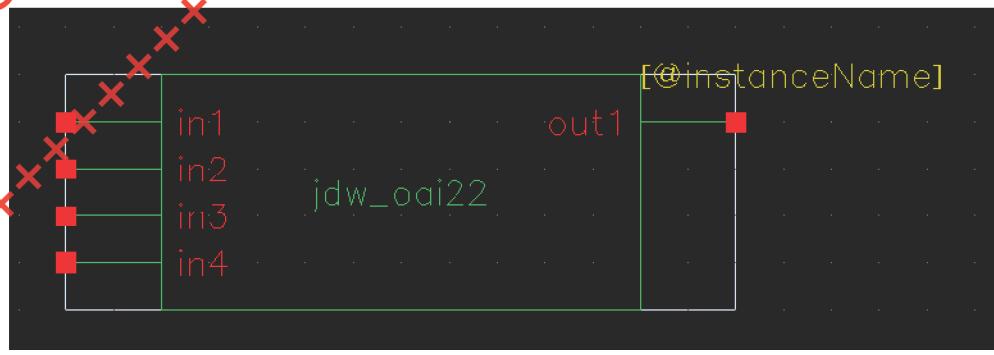
In1	In2	In3	In4	Out1
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	1	0	0
1	1	1	1	0

Propagation Delay:

$\tau_{pd}: 0000 \rightarrow 1111$	-8.368 ns
$\tau_{pd}: 1111 \rightarrow 0000$	12.652 ns
$\tau_{pd}: 0011 \rightarrow 1111$	-18.109 ns

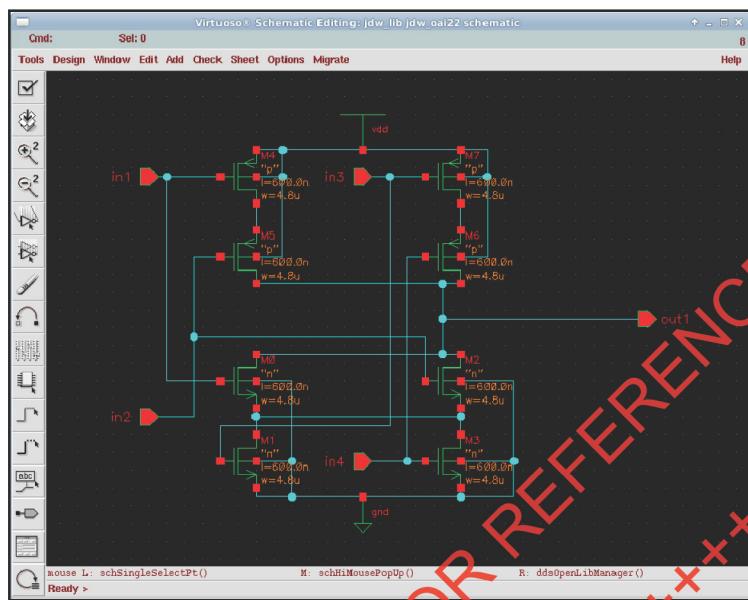
Layout Area: $(56\lambda)(100\lambda) = 5600\lambda^2$

Symbol:

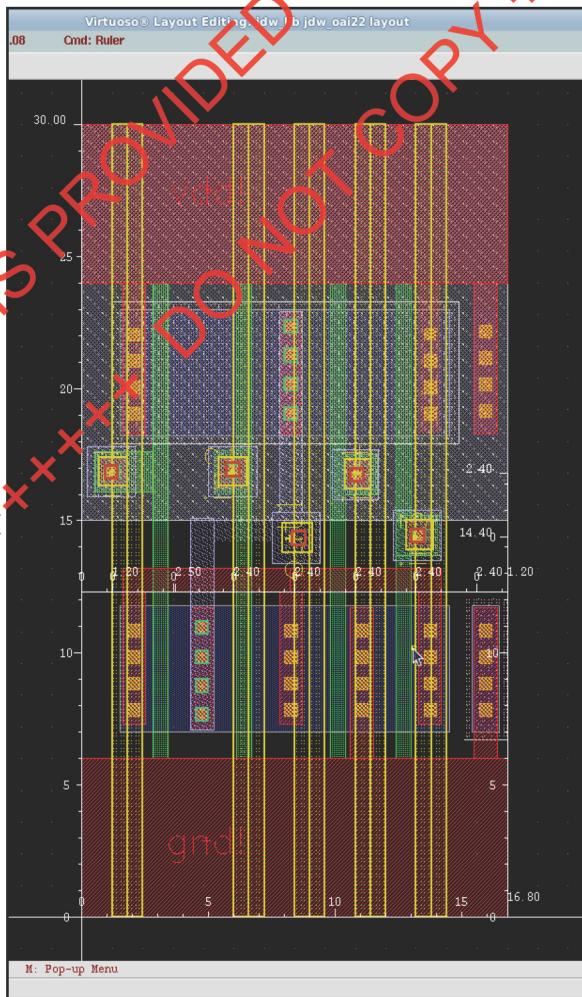


fml_lib: Standard Cell Library & Corner Cell Design Report

Schematic:



Layout:



fml_lib: Standard Cell Library & Corner Cell Design Report

fml_tgmux:

Truth Table:

S	In1	In2	Out1
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Propagation Delay:

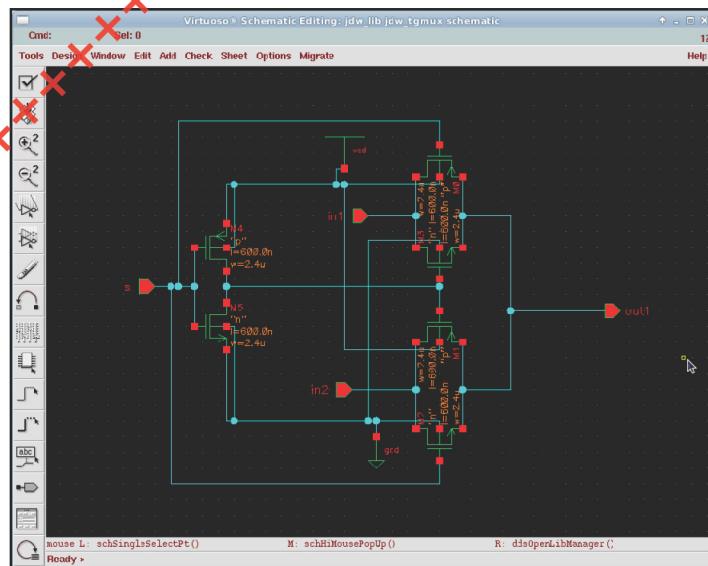
Select 0: 0→1	0.34 ns
Select 0: 1→0	0.26 ns
Select 1: 0→1	0.285 ns
Select 1: 1→0	0.285 ns
Select 0→1 : 0→1	5.51 ns
Select 1→0 : 1→0	9.13 ns
Select 1→0 : 0→1	10.844 ns
Select 0→1: 1→0	-5.046 ns

Layout Area: $(64\lambda)(100\lambda) = 6400 \mu m^2$

Symbol:

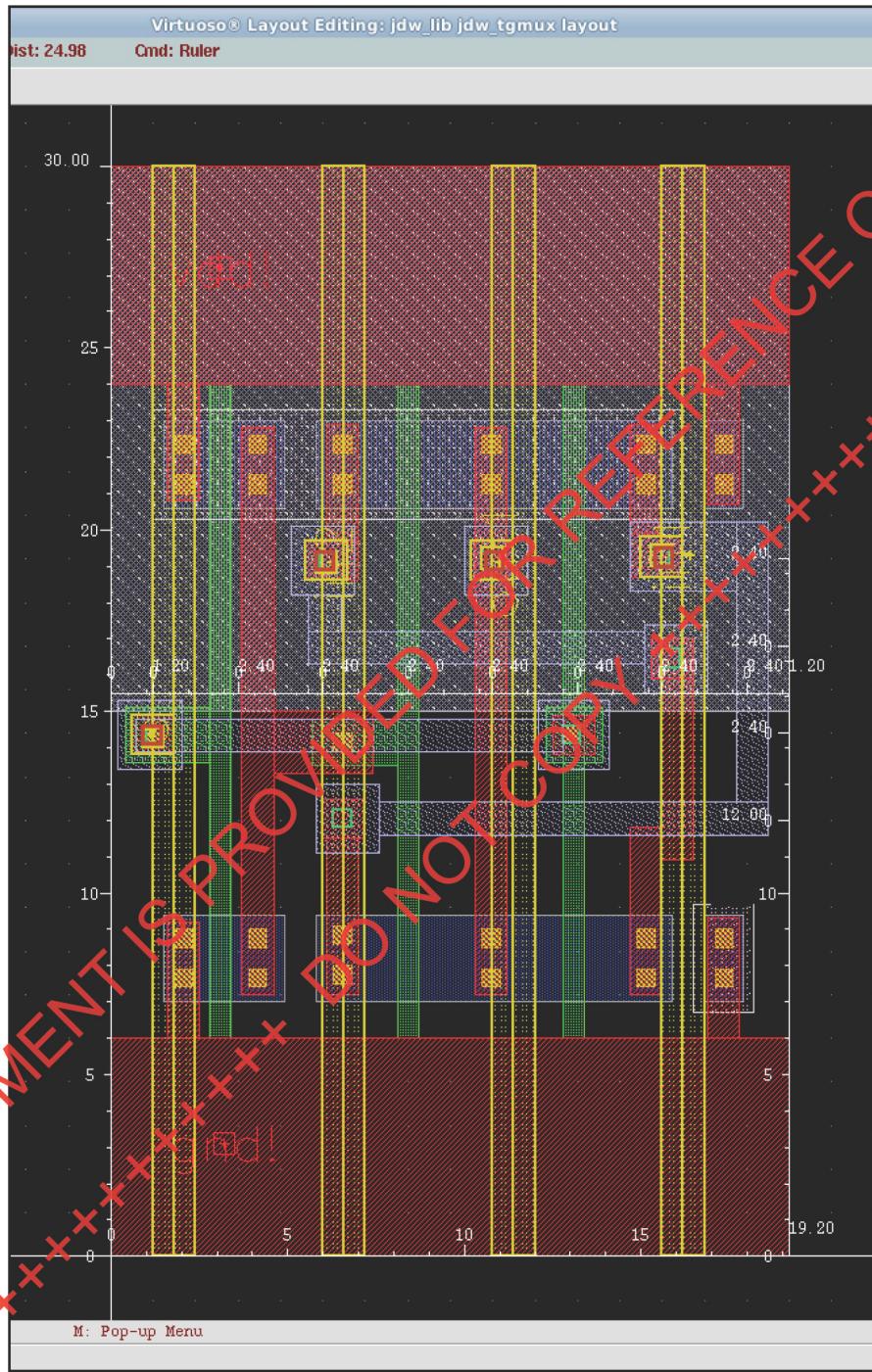


Schematic:



fml_lib: Standard Cell Library & Corner Cell Design Report

Layout:



fml_xor2:

Truth Table:

In1	In2	Out1
0	0	0
0	1	1
1	0	1
1	1	0

Propagation Delay:

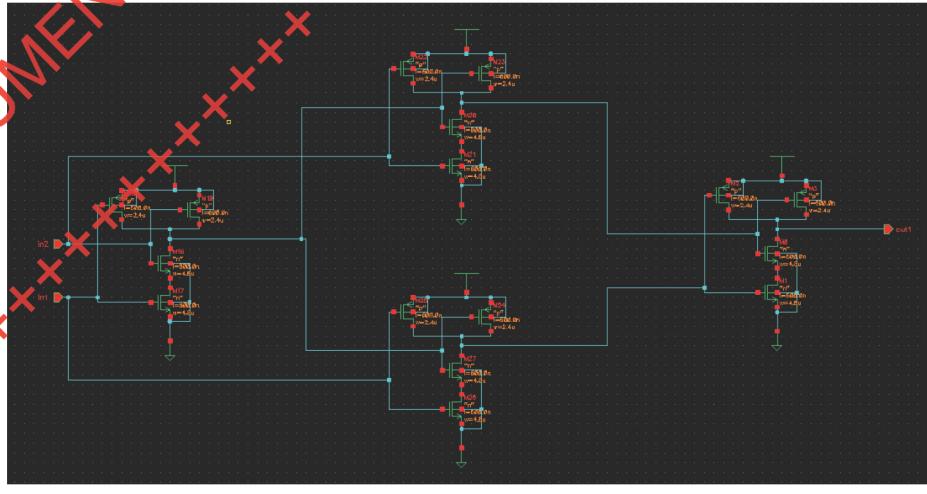
$\tau_{pd}: 11 \rightarrow 10$	15.423 ns
$\tau_{pd}: 10 \rightarrow 00$	-17.8 ns
$\tau_{pd}: 00 \rightarrow 10$	14.63 ns

Layout Area: $(96\lambda)(100\lambda) = 9600\lambda^2$

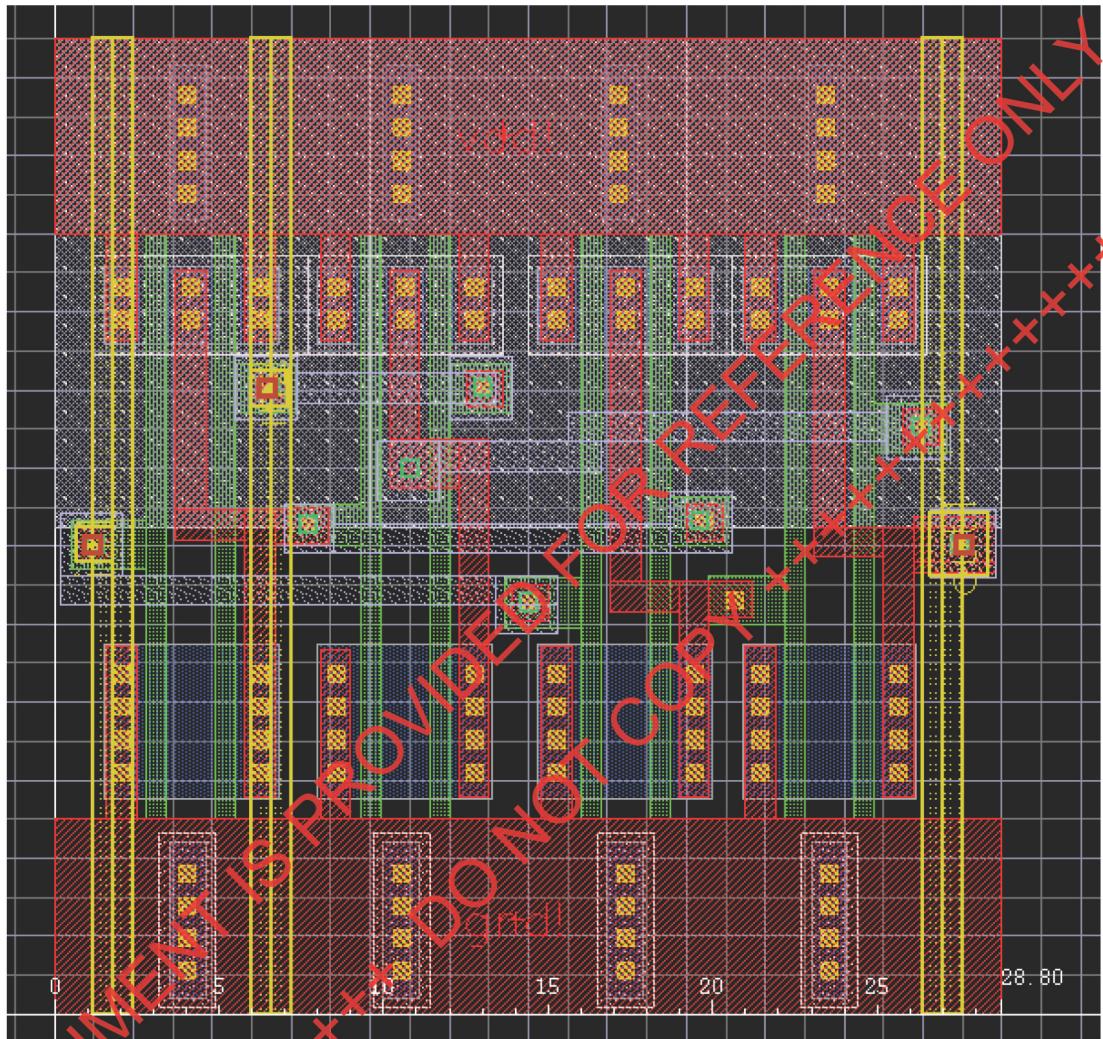
Symbol:



Schematic:



Layout:



fml_dff:

Truth Table:

D	Phi2	Q	Qbar
0	↑	0	1
1	↑	1	0

Propagation Delay:

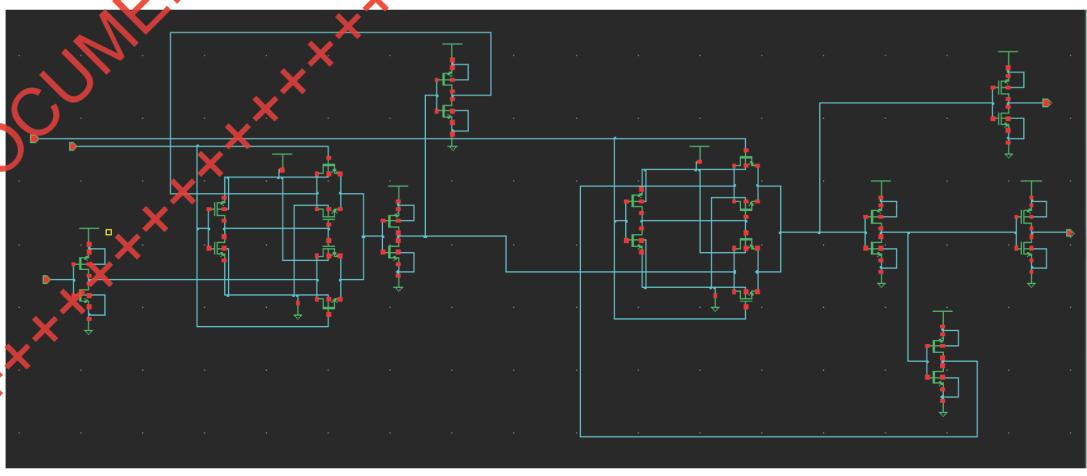
τ_{pd} : Q 0 → 1, Phi2 ↑	3.189 ns
τ_{pd} : Q' 1 → 0, Phi2 ↑	3.31 ns

$$\text{Layout Area: } (240\lambda)(100\lambda) = \mathbf{24,000\lambda^2}$$

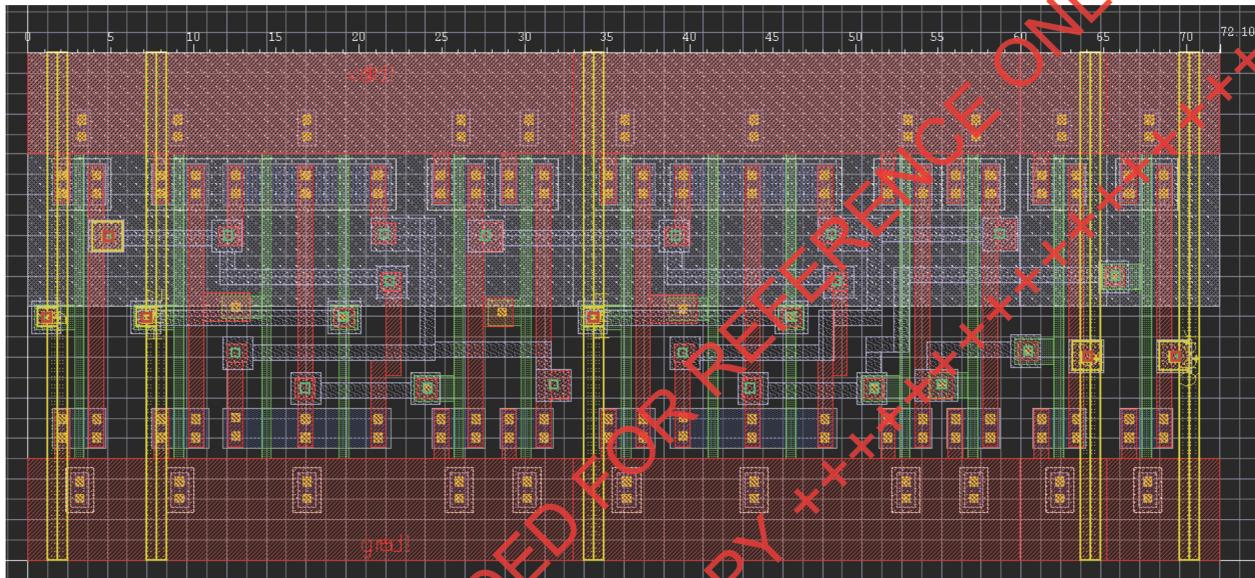
Symbol:



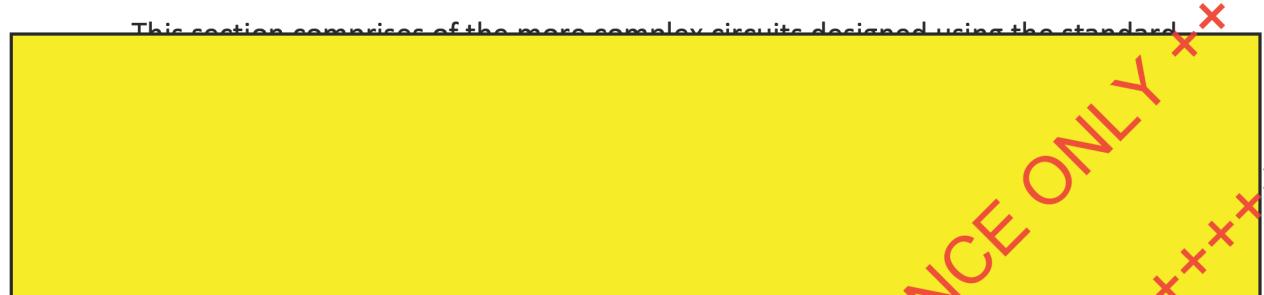
Schematic:



Layout:



Complex Circuit Designs



Full Adder:

Truth Table:

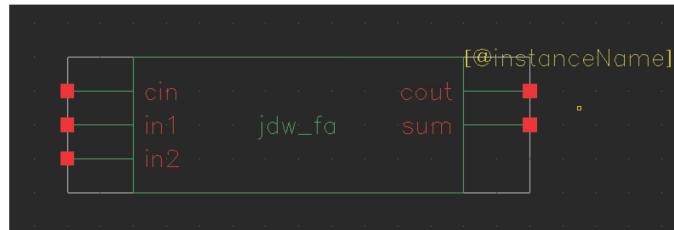
In1	In2	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Propagation Delay:

$\tau_{pd}: 111 \rightarrow 110$	18.136 ns
$\tau_{pd}: 110 \rightarrow 001$	2.694 ns
$\tau_{pd}: 000 \rightarrow 011$	14.01 ns
$\tau_{pd}: 011 \rightarrow 010$	-8.23 ns
$\tau_{pd}: 010 \rightarrow 101$	16.83 ns
$\tau_{pd}: 101 \rightarrow 100$	17.7 ns

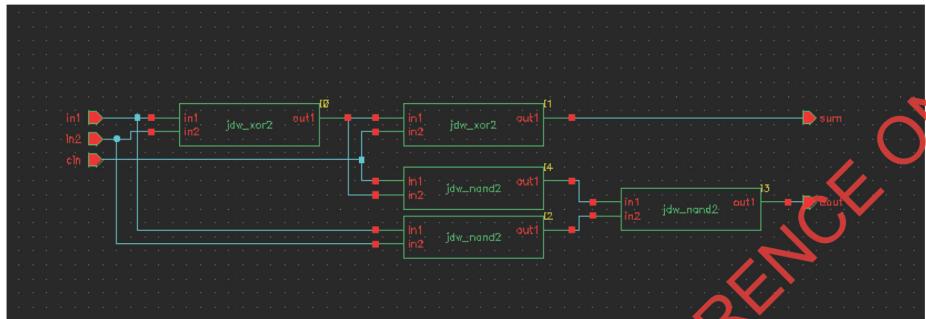
Layout Area: $(45.6 \text{ } \mu\text{m})(88.8 \text{ } \mu\text{m}) = 4,050 \text{ } \mu\text{m}^2$

Symbol:

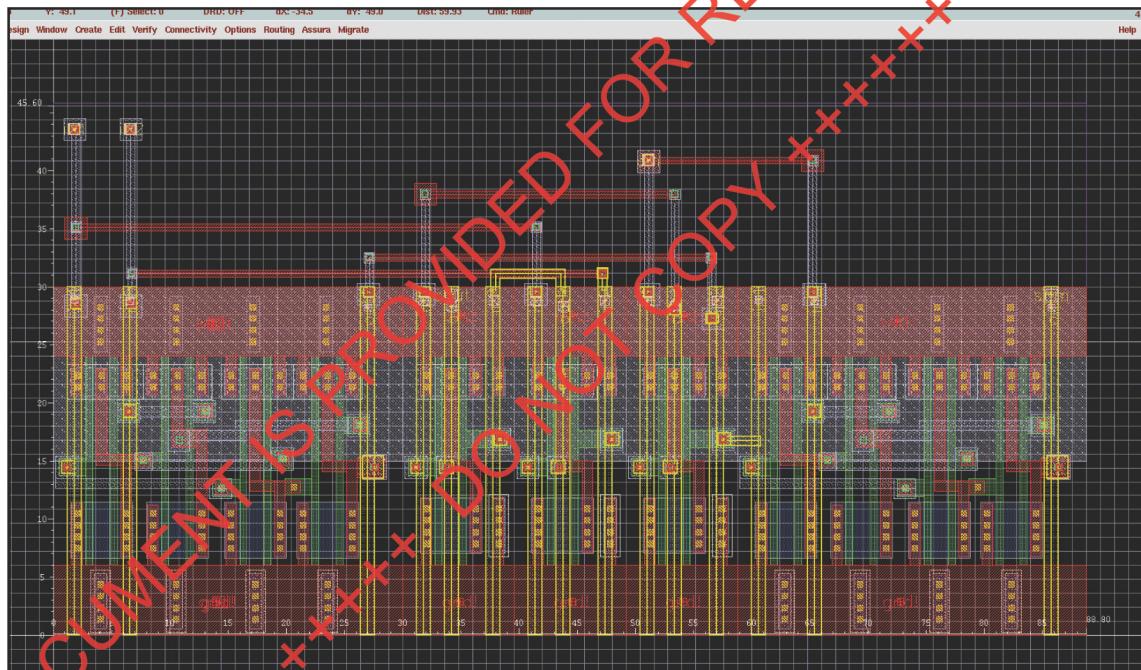


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Schematic:

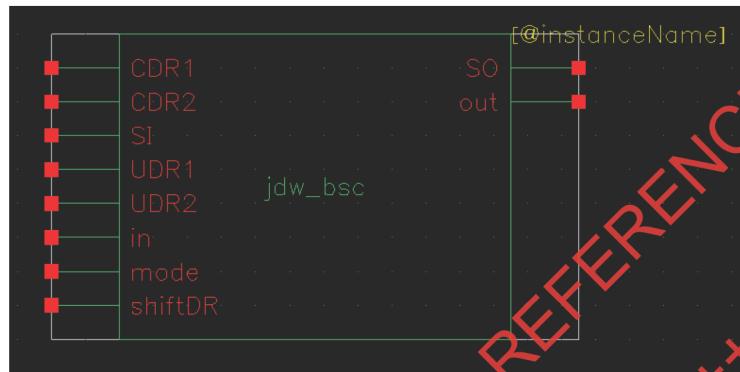


Layout:

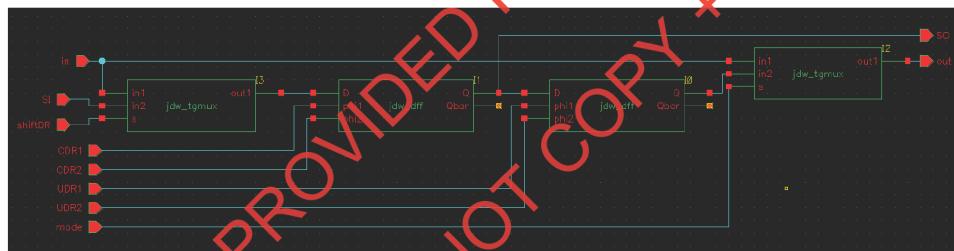


Boundary Scan Cell:

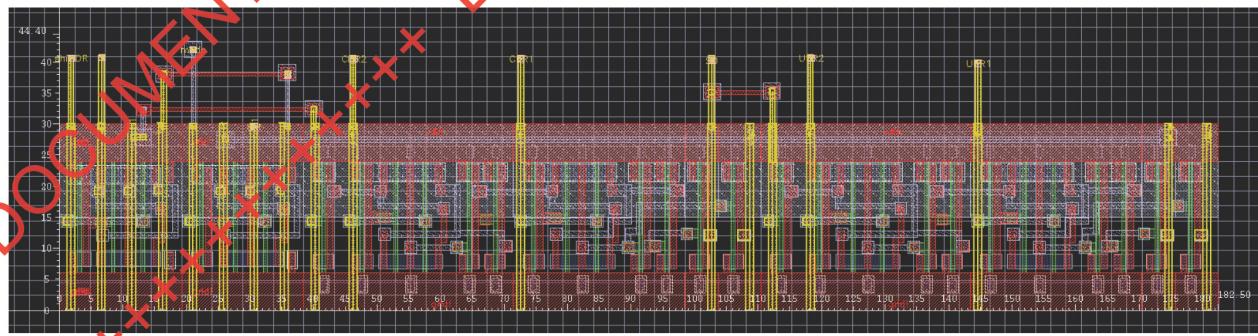
Symbol:



Schematic:

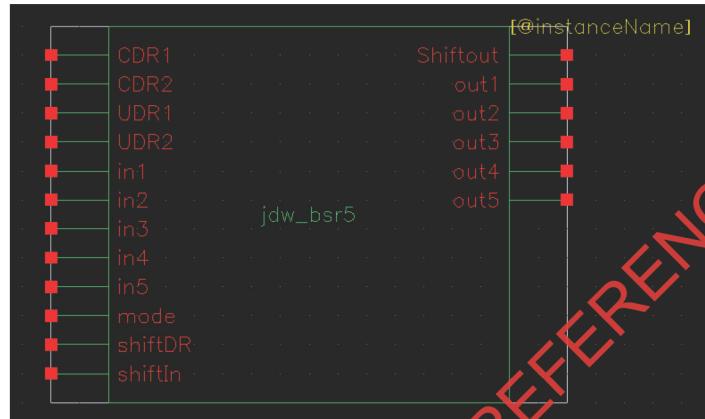


Layout:

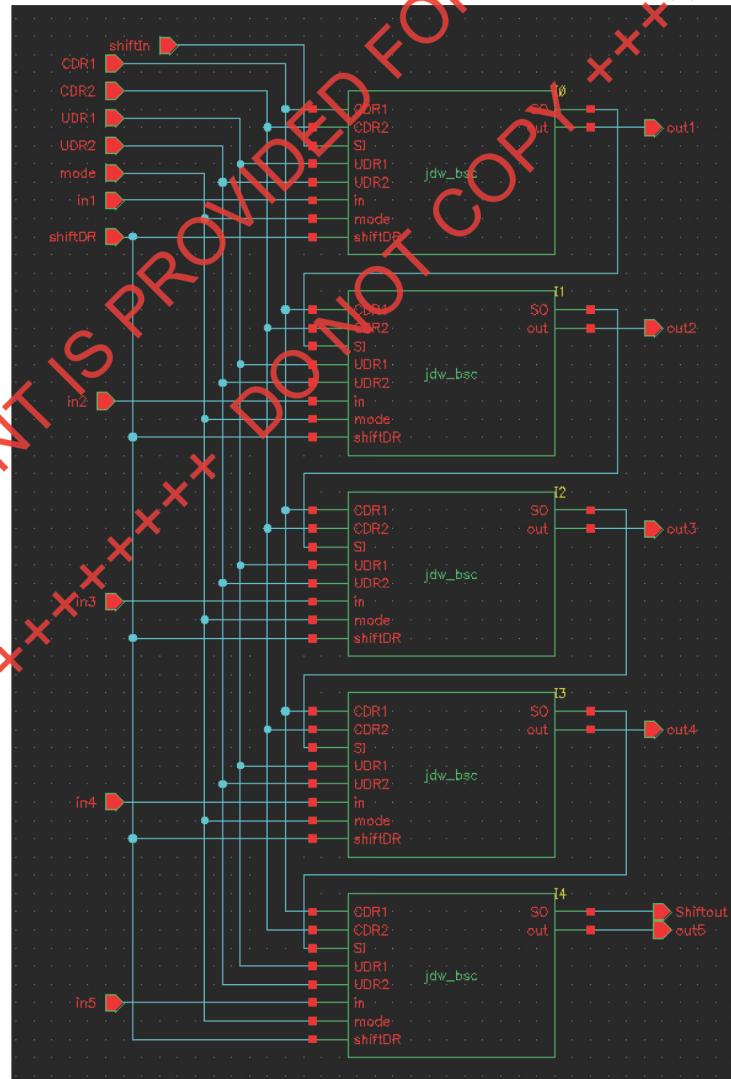


Boundary Scan Register:

Symbol:

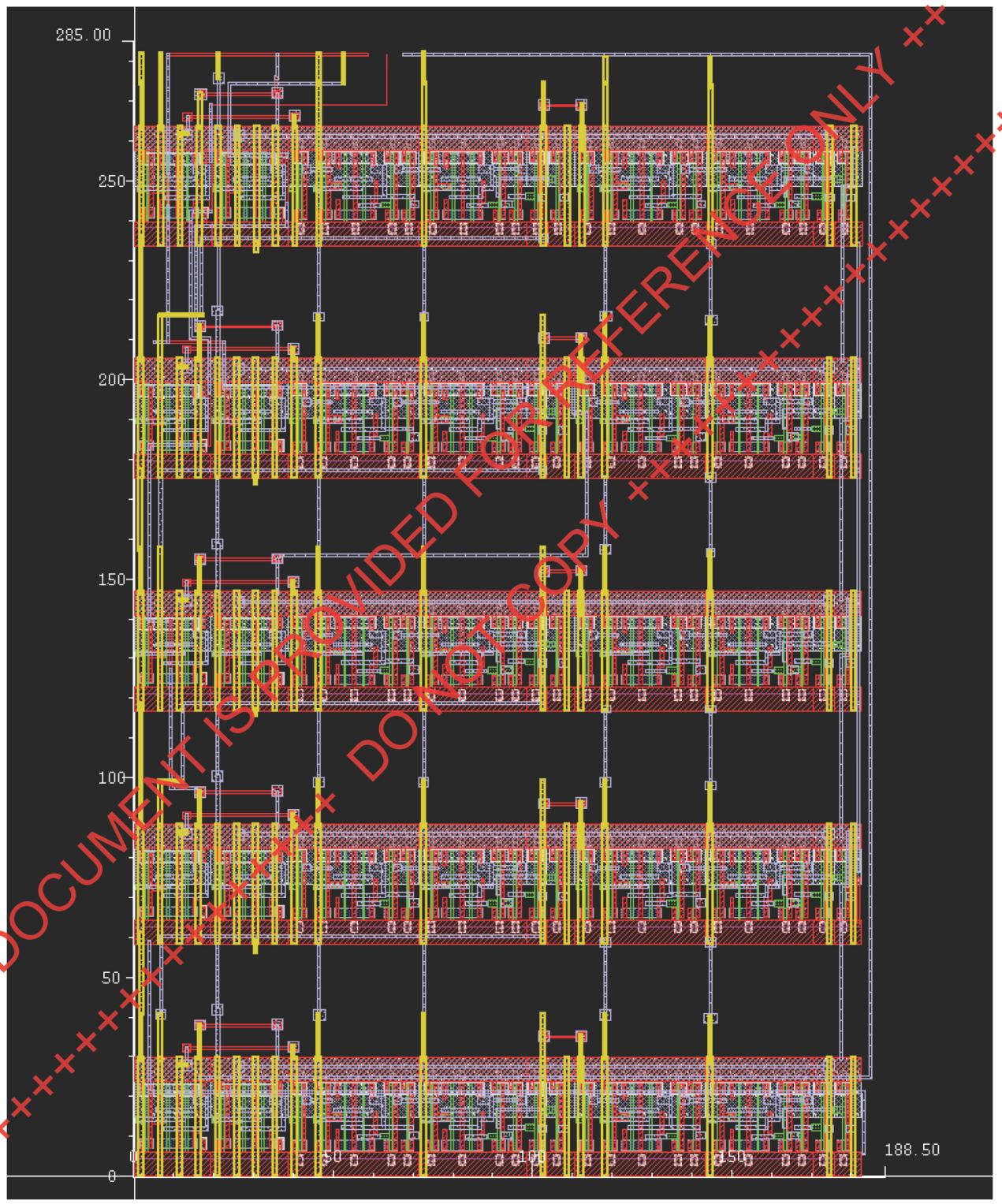


Schematic:



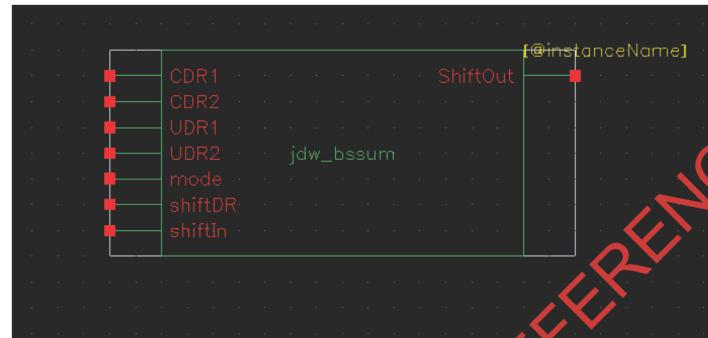
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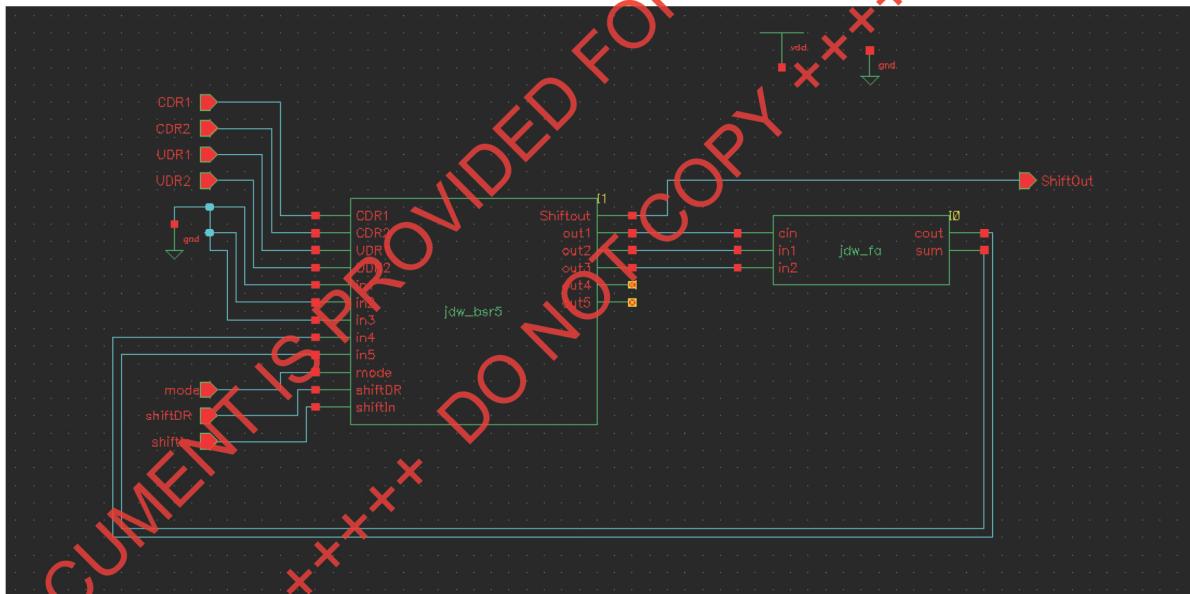


Boundary Scan Sum:

Symbol:

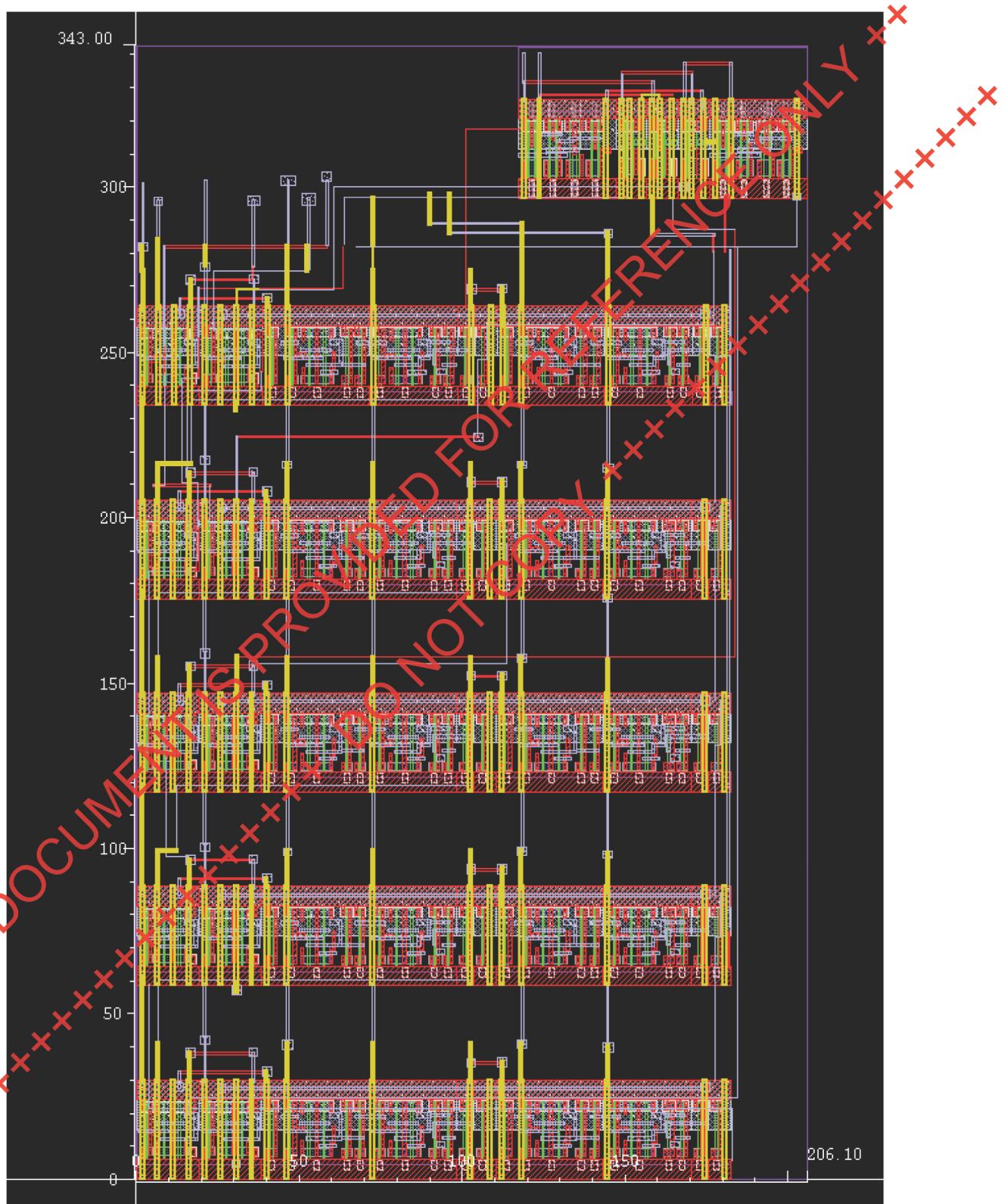


Schematic:



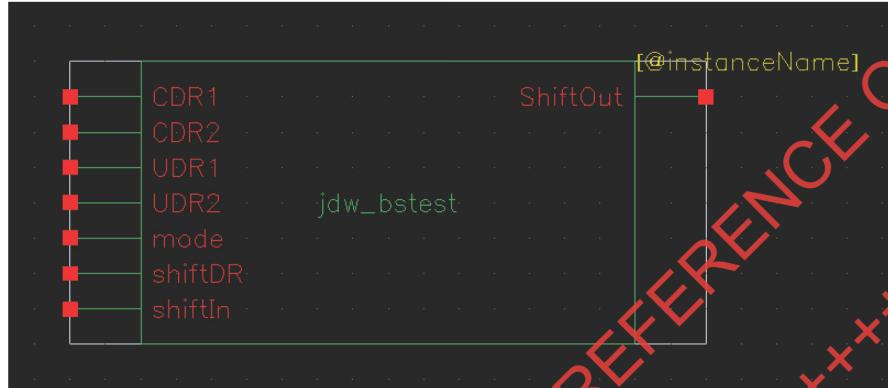
fml_lib: Standard Cell Library & Corner Cell Design Report

Layout:

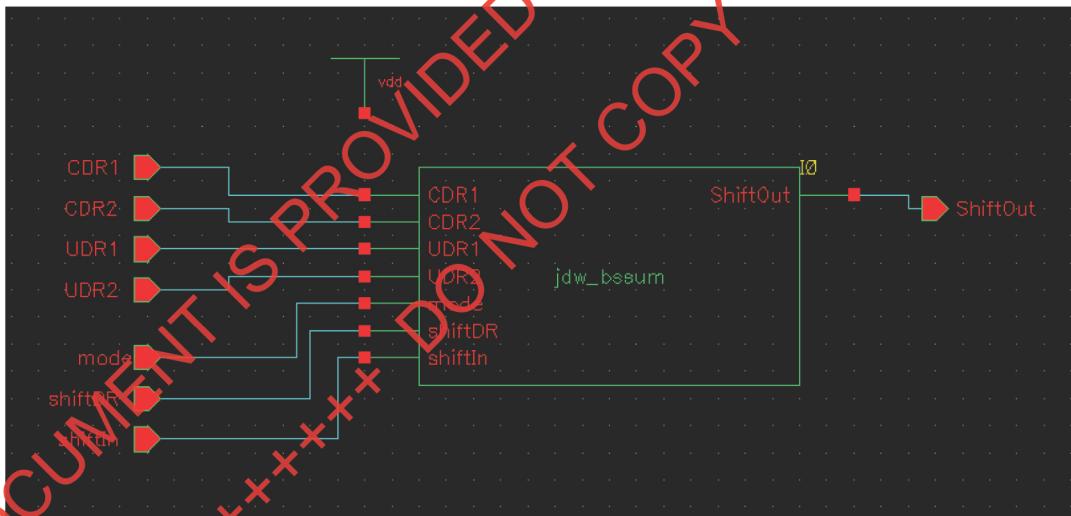


Boundary Scan Test:

Symbol:

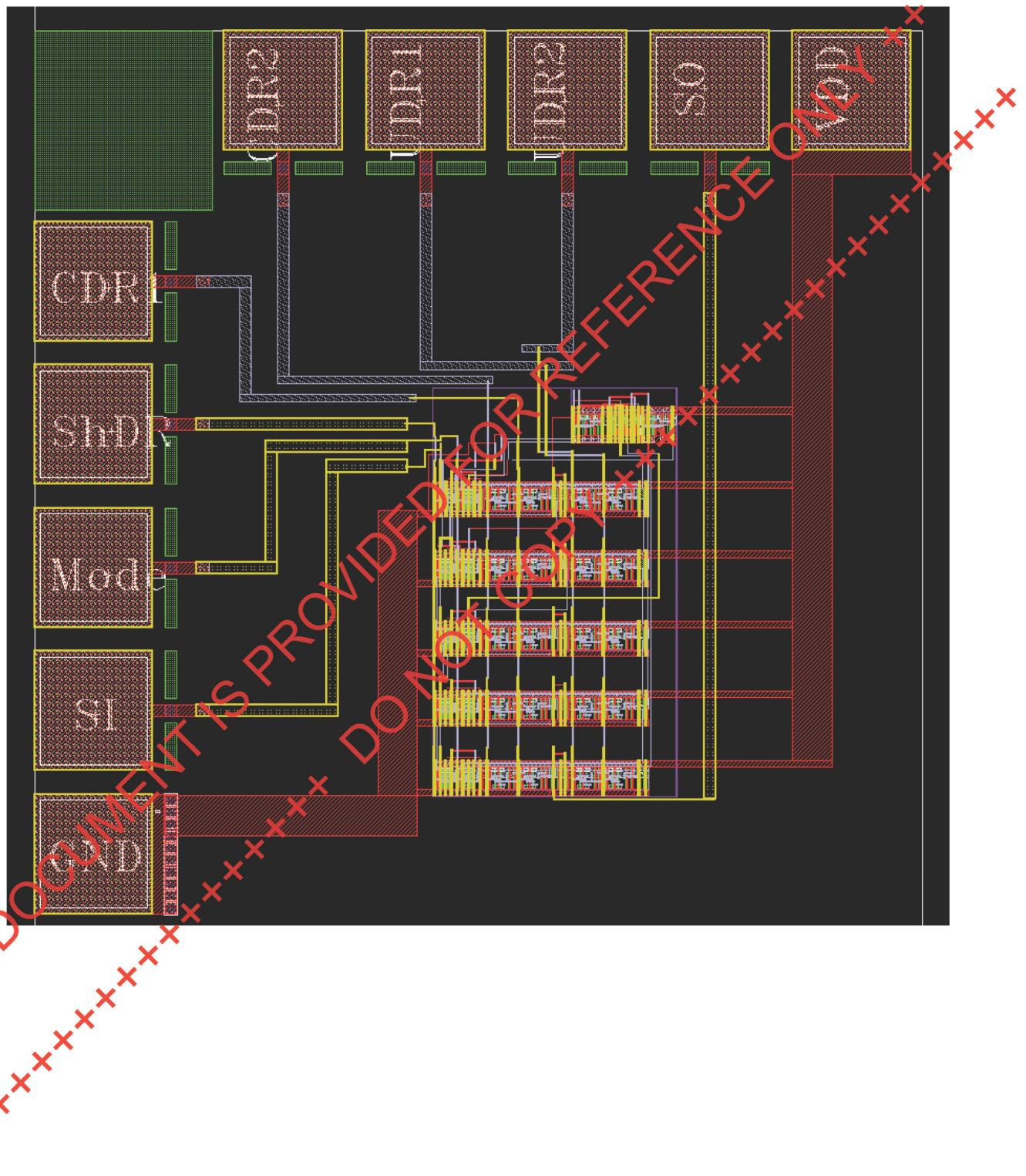


Schematic:



fml_lib: Standard Cell Library & Corner Cell Design Report

Layout:



Finis