EE520 | EE620 Project 1 Assignment

Assigned: Wednesday, September 02

Project 1 Due: Friday, September 26, 1:00 PM

Revision History:

1	Original created by: Dorin Patru, PhD
2	Updates for EE651 by: Mark A. Indovina
3	Updates for EE520 | EE 620 by: Mark A. Indovina
4	Updates for EE520 | EE 620 by: Mark A. Indovina

The grade for this project will be based on:

1. On the timely completion of your EDA Tutorial 1 assignment.
2. On the timely completion of your Project 1 assignment.
3. On a 5 min. oral presentation and defense of your work as organized by the instructor and TA during the week the Project 1 is due.
4. On the following files uploaded to the mycourses Project 1 Report dropbox:
    a. On the Project 1 engineering report (engineering report details are described later in this document), uploaded as a PDF copy to the mycourses drop box (PDF only), due: Friday, September 26, 1:00 PM.
    b. On the Project 1 database copy, uploaded to the mycourses drop box, due: Friday, September 26, 1:00 PM.
    c. NOTE: Due to the size of the files submitted, the mycourses Project 1 Report dropbox is configured to only keep one submission, therefore if you complete 3 submissions, only the files included with the last submission are kept. However, a submission is one or more files, therefore all required Project 1 files must be uploaded simultaneously as one submission to the mycourses dropbox.

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1. GENERAL DESIGN SPECIFICATIONS

Design a library of digital standard cells for the AMIS 0.5µm CMOS Technology using the technology micron based rules. The name of your library will be **fml_lib**, where **fml** stands for the initials of your **first**, **middle** and **last** names.

You will have to:

1. Draw the transistor level schematic of each gate; size transistors appropriately.
2. Analyze the time domain behavior of the gates using transient analysis. For simulation purposes, load the output node of each gate with a capacitance of 100 fF. Simulate for all specified input combinations.
3. For the Inverter only, show the rise/fall transfer characteristics as labeled plots included within the comments/notes section of the datasheet.
4. Layout all required gates.
5. Create a symbol, and a Verilog gate level primitive model for all required gates
6. Extract parasitics and document these in the comments/notes section of the datasheet.

The following gates are mandatory for all students:

1. Inverter: fml_inv[1]
2. Two input NAND gate: fml_nand2
3. Two input NOR gate: fml_nor2
4. Four Input, two-level complex logic function[1]
5. 2-to-1 MUX[1]

Note: fml_inv is a NEW cell designed from scratch to the specifications described in this document; it is NOT a copy of the inverter, *fml_inv1*, you created in EDA Tutorial 1.

Each student must also follow the INDIVIDUAL DESIGN SPECIFICATIONS described in this document. Individual Design Specifications are determined by decoding the assigned 6-bit code per requirements defined in Table 2. In addition, each gate will be designed per the CELL DESIGN GUIDELINES, and GENERAL STANDARD CELL LAYOUT GUIDELINES also described in this document.

[1] Individual Design Specifications are determined by decoding the assigned 6-bit code per requirements defined in Table 2.

Publish an engineering project report based on cell datasheets following the template report for each gate, as shown in the document *mai_ee520_ee620_proj1_cell_datasheet_template.doc*, which is posted on mycourses. Print to PDF and upload your report to Project 1 drop box on mycourses. No printed version is necessary for the instructor. If you plan to print a hardcopy for yourself, make sure to change the black background to white before sending to the printer (instructions shown below).

2. PROJECT GRADING

As noted earlier, the grade for this project will be based on:

1. On the timely completion of your EDA Tutorial 1 assignment.
2. On the timely completion of your Project 1 assignment.
3. On a 5 min. oral presentation and defense of your work as organized by the instructor and TA during the week the Project 1 is due. Cell(s) will be picked at random and you will be asked to run DRC and LVS checks during your presentation.
4. On the electronic Project 1 report (PDF only) due: Friday, September 26, 1:00 PM.
5. On a copy of your database uploaded to mycourses per instructions found in *mai_520_620-database-upload.pdf* due: Friday, September 26, 1:00 PM.

Table 1 Project 1 Grading:

EDA Tutorial 1 Score	5%
All Cell Schematics Score	20%
All Cell Layouts Score	20%
All Cell Simulation Results Score	20%
All Cell Datasheets Score (Including readability, grammar, spelling, format)	25%
Defense Score	5%
Overall quality Score	5%
Late Deduction	0%
Graded Total	**100%**

3. CELL DESIGN GUIDELINES

A) $\lambda = 0.3\ \mu m$

B) $W/L = 8\lambda/2\lambda = 2.4\ \mu m/0.6\ \mu m$, $W/L = 12\lambda/2\lambda = 3.6\ \mu m/0.6\ \mu m$

1) All devices should be drawn with minimum L (2λ)

C) Document Propagation Delay for the following paths:

1) For the Inverter:
   a. A → Y ↑
   b. A → Y ↓
2) For the NAND2:
   a. A → Y ↑
   b. A → Y ↓
   c. B → Y ↑
   d. B → Y ↓
3) For the NOR2:
   a. A → Y ↑
   b. A → Y ↓
   c. B → Y ↑
   d. B → Y ↓
4) For the AOI22:
   a. A0 → Y ↑
   b. A0 → Y ↓
   c. A1 → Y ↑
   d. A1 → Y ↓
   e. B0 → Y ↑
   f. B0 → Y ↓
   g. B1 → Y ↑
   h. B1 → Y ↓
5) For the OAI22:
   a. A0 → Y ↑
   b. A0 → Y ↓
   c. A1 → Y ↑
   d. A1 → Y ↓
   e. B0 → Y ↑
   f. B0 → Y ↓
   g. B1 → Y ↑
   h. B1 → Y ↓
6) For the MUX2:
   a. A → Y ↑
   b. A → Y ↓
   c. B → Y ↑
   d. B → Y ↓
   e. S → Y ↑

f. S → Y ↓

D) Use 500 ps for the input waveform rise and fall times when simulating with Spice (Cadence Spectre).
E) For simulation purposes, load the output of node each gate with a capacitance of 100 fF.
F) Use a test schematic to simulate your cells. This test schematic would contain an instance of your cell, load capacitance, input pulse generators, VDD and GND symbols.
G) Cell port/label/pin names can only use letters and numbers, must start with a letter, are case sensitive, and the MUST MATCH on all views (symbol, schematic, layout, verilog, functional). Industry standard is to use UPPERCASE letters for standard cell pin names. Note that use of any special characters in pin names will cause errors in downstream tools.

4. INDIVIDUAL DESIGN SPECIFICATIONS

NAME: _____

Bit Code: _____
B5/B4/B3/B2/B1/B0

Table 2 Individual Design Specifications

Bit	Value='1'	Value='0'	Comments
B5	Inverter X2	Inverter X1	The Inverter X2[2] (X2 Drive Strength) is designed using PMOS and NMOS transistors that are double in width, i.e. (2*W), with W defined per B3 & B2
B4	Horizontal	Vertical	Defines the orientation of the MOS transistor channel width in the layout
B3	12/2	8/2	Defines the W/L ratio of the NMOS transistors in λ/λ
B2	2xB3	1xB3	Defines the W/L ratio of the PMOS transistors in λ/λ (*Note: defined as a multiple of the W/L ratio of the NMOS transistors*)
B1	AOI (4 input)	OAI (4 input)	Defines the type of the additional gate to be implemented *Where:* *A ~ AND* *O ~ OR* *I ~ Invert*
B0	Transmission Gate 2-to-1 MUX	CMOS 2-to-1 MUX	Defines the type of the MUX to be implemented

[2] A gate with X2 drive strength will have essentially the same rise/fall time while driving a capacitance of 2C farads as that of a gate with X1 drive strength driving a capacitance of C farads.

5. GENERAL STANDARD CELL LAYOUT GUIDELINES

(*Expanded from above, and discussed as needed in lab and class.*)

1. $\lambda = 0.3\ \mu m$
2. Cell Height: $104\ \lambda = 31.2\ \mu m$
    a. Cell Height is a multiple of 8 lambda ($8\ \lambda = 2.4\ \mu m$)
    b. Suggested wiring tracks
        i. $4\ \lambda$ width, $4\ \lambda$ spacing from neighbor = $8\ \lambda$ pitch
3. Cell width multiple of 8 lambda ($8\ \lambda = 2.4\ \mu m$)
    a. Suggested wiring tracks
        i. $4\ \lambda$ width, $4\ \lambda$ spacing from neighbor = $8\ \lambda$ pitch
4. Origin of cell at 0,0 in lower left hand corner
5. nMOS at bottom and pMOS at top
6. All gates include well and substrate contacts
7. VDD / GND:
    a. M1 only
    b. VDD at top, and GND at bottom of cell
    c. $20\ \lambda = 6\ \mu m$ in vertical width
    d. Horizontal width as necessary to accommodate cell contents
    e. Designed so that cells can abut without additional metal
8. Clock lines:
    a. M2 only
    b. $10\ \lambda = 3\ \mu m$ wide
9. Cells must be designed so that they can be abutted horizontally without introducing design rule violations - test that your cells can be abutted in rows by placing multiple cells (of various types) in rows in a test layout and running DRC.
10. Cells must be designed so that they can be flipped and abutted horizontally VDD to VDD without introducing DRC or LVS violations - test that your cells can be flipped and abutted in rows by placing multiple cells (of various types) in a test schematic and rows in a test layout and running DRC and LVS.
11. All interconnections within the cell will be made using POLY1 (any direction), M1 (any direction) exclusively
    a. As a last resort and only if necessary to achieve an optimal cell design:
        i. You can use M2 (horizontal direction only)
        ii. You can use M3 (vertical direction only)
        iii. Note however that the auto router used in later labs will be routing using M2 (horizontal direction) and M3 (vertical direction). Any deviation from these strict rules horizontal / vertical rules and the router will create shorts.

12. Place the bulk connections under the VDD & GND straps (VDD at top, and GND at bottom of cell) to make room for your cell design as shown in Figure 1:

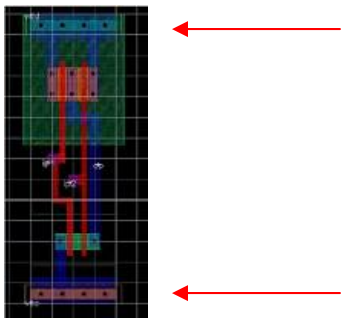

Figure 1 Layout with Bulk Connections under VDD / GND

13. Routing Tracks & Input(s) / Output(s) Ports:
    a. M3 only
    b. Vertical orientation
    c. Span full height of cell
    d. Per Figure 2, to help the routing tools, all I/O ports should fall in the center of horizontal (x-direction) and vertical (y-direction) routing tracks or channels with a pitch of 8 λ.
        i. As shown in Figure 2, the first and last ½ vertical track (4 λ) is not used and creates a vertical "feed through" routing channel when cells abut.
        ii. A cell is designed using an 8 λ grid and has the first possible I/O port location in the center of the first full vertical routing track - 8 λ inside the left edge of the cell.
        iii. Therefore the final width of the cell should be a multiple of 8 λ
        iv. Cell height (104 λ) is a multiple of 8 λ routing tracks.

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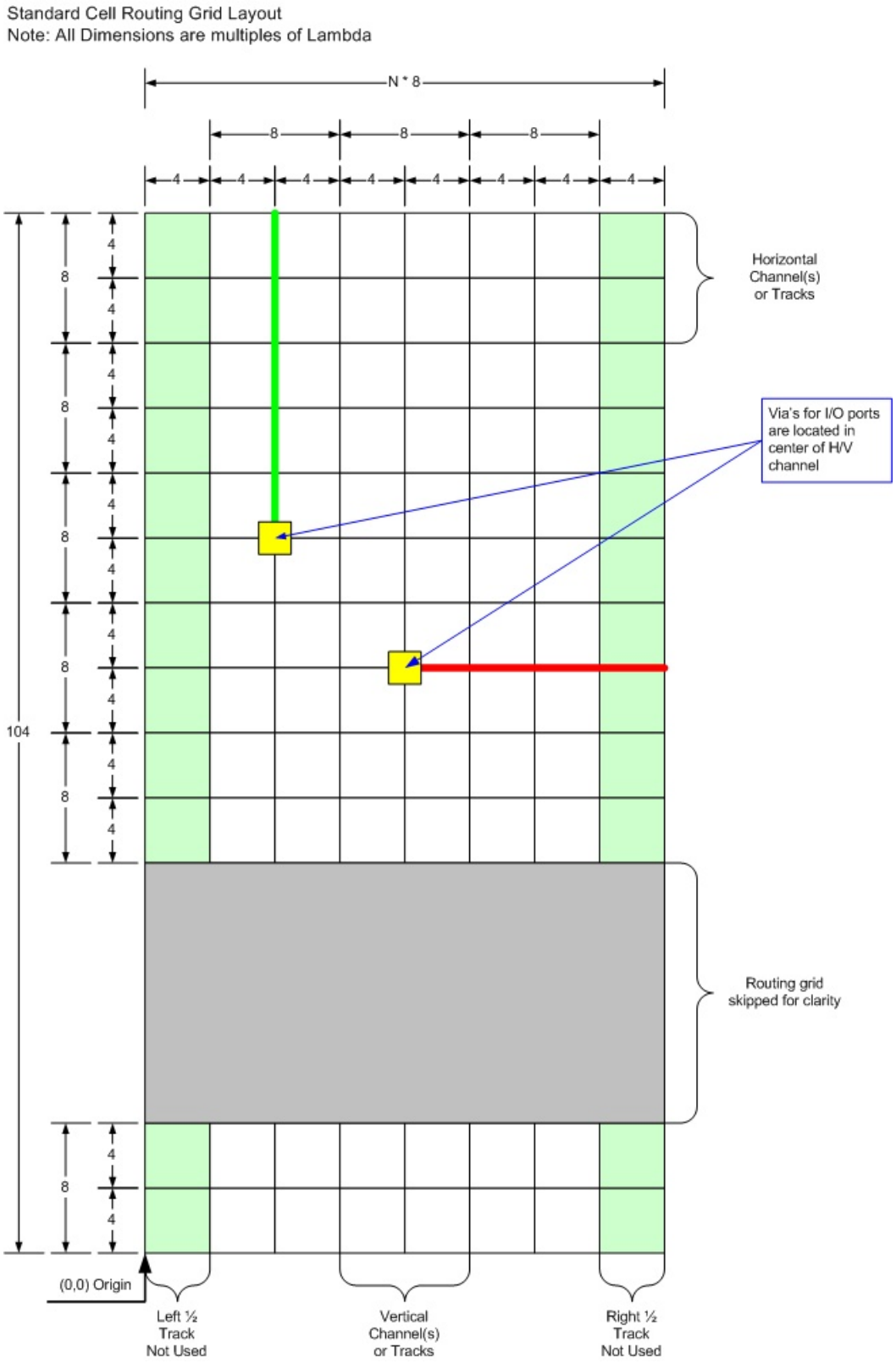

Figure 2 Routing Grid Layout

14. Cells must be prepared for use with routing tools:
    a. As shown in Figure 2, routing is done in the channels between cell rows
    b. Your I/O ports should have labels on M3|drw
    c. VDD / GND are global signals. Place labels on M1|drw, and use labels:
        i. vdd! and gnd!
    d. Once you have labeled everything, you need to create pins from labels:
        i. For the labels on M3|drw, choose Pin Layer M3|pn
        ii. For the labels on M1|drw, choose Pin Layer M1|pn
        iii. Use the Create→Pins From Labels utility in Virtuoso to generate pins.
        iv. Pins must be placed on the metal layer the signal is on, with a layer purpose of Pin (pn)
15. As shown in Figure 3, the TUB and N-Field layer regions cover the same area as the VDD strap; you must also maintain a 4λ notch on the left [A], and an 8λ notch on the right [B] of the cell for the embedded feed-through track. VDD & GND straps extend the width of the cell. For clarity the cell height shown in not to scale Figure 3 and is compressed.

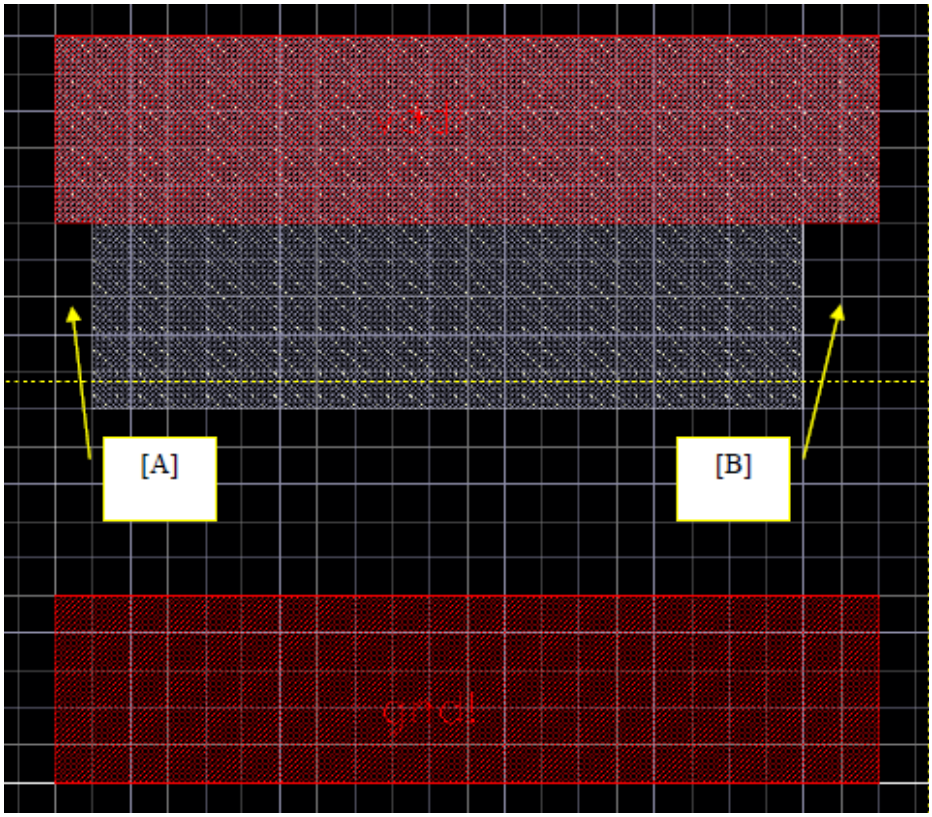

Figure 3 TUB, N-Field regions and VDD, GND Strapping (*For Clarity the Cell Height is Compressed*)

16. All cells must DRC and LVS clean (no warnings or errors)
17. Utilize the Virtuoso display grid to make layout to the routing grid easier as shown in Figure 4:

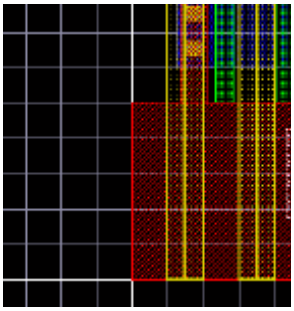

Figure 4 Cutout of Layout Window Showing 4 λ Display Grid

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5. EXAMPLE DATASHEET

Library Name:	
Cell Name:	
Function/Truth Table:	
Propagation Delay:	
Layout Area:	
Symbol with Port Names:	
Schematic:	
Layout:	
Verilog Model:	
Comments/Notes:	

Figure 5 Example Cell Date Sheet

[CONTINUED NEXT PAGE]

5. APPENDIX

Please use the following instructions if you are going to print a hardcopy of your data sheet(s).

Using ALT-PRT_SCR, copy/paste the window containing the schematic into a word file.

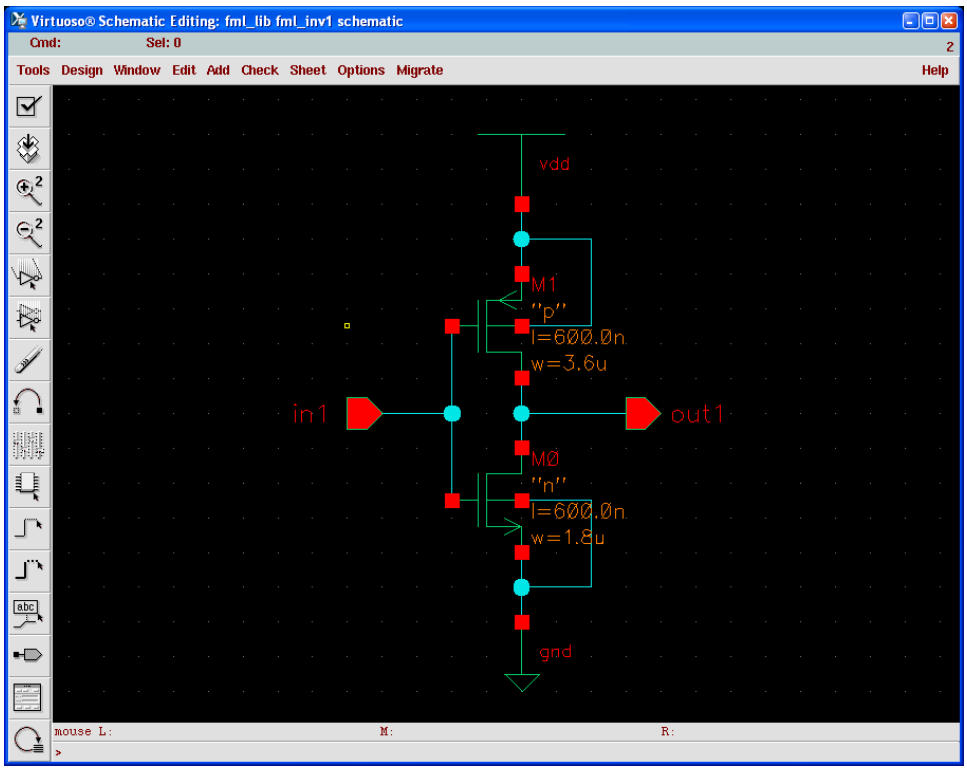

Figure 6 Original Composer Schematic Image

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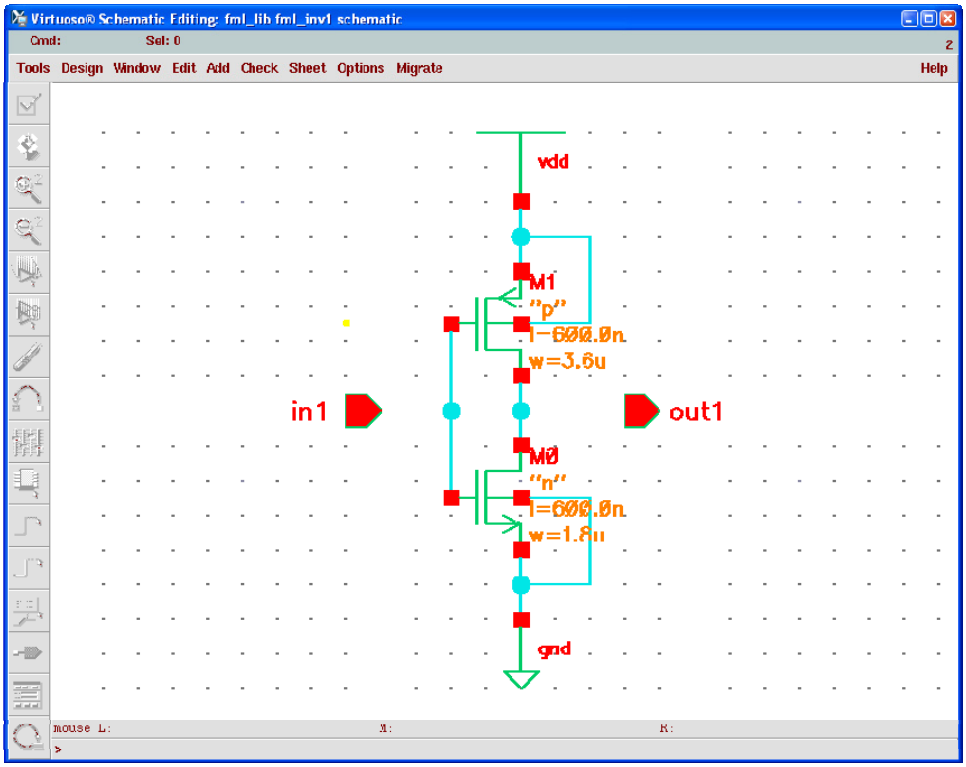

Figure 7 Color Modified Composer Schematic Image

Once placed into your word file, right click on the image and select SHOW PICTURE TOOLBAR. Once this opens, towards the right hand side there is a command SELECT TRANSPARENT COLOR. Click on it and then click anywhere on the black background in your window. See the result above.