Rochester Institute of Technology

EE520 Design of Digital Systems

Subject: Project 2 enhancing project 1 with XOR, rising edge triggered D Flip Flop and Full adder

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Course: Design of Digital Systems

Library : zxw_lib

Design constraint library with NMOS 8 lambda/2 lambda, PMOS being 16 lambda/2 lambdas twice the size of NMOS. The design of transistors is unskewed. The design is vertical as in tutorial 1 which was done in the first week of the class. The CMOS is used for multiplexer. AOI is implemented according to those above specifications in project 1. In project 2, XOR, rising edge triggered d flip flop and full adder is implemented. XOR implementation is simple since project 1 introduces the use of layout virtuoso software, and inverter, NAND, NOR, AOI and 2 to 1 multiplexer gates are successfully implemented before this project 2. XOR is tested with timing simulation diagram. The full adder can be tested using BSTEST simulation. D flip flop can be tested looking at output changes as input in timing simulation diagram only when clock goes from zero to one. The full adder in the project is finished routing cells being minimized and following the routing channel height guidelines 26 lambdas at top and bottom, and 52 lambdas between rows. For full adder, 52 lambdas between rows do not need to be considered.

For inverter, NMOS is 2.4um and PMOS is 4.8um. Using this as reference, NAND NMOS is 4.8um and PMOS is 4.8um. The equations for transistor sizing are W=1/R and R of PMOS = 2R of NMOS. Only look at the worst case of transistors to do sizing. For the parallel transistors case, the worst case is when only one transistor is on while for transistors in series, all transistors have to be on. As similar to calculating NAND, NOR NMOS is 2.4um for NMOS and

9.6um for PMOS. NMOS is minimum size which is 2.4um. To calculate PMOS, [1/(1/Wp+1/Wp)] being equal to 4.8 is used.

Project 2 layouts were minimized as possible to fit in corner cell. Finger transistors were not used in this project and sizing of PMOS and NMOS was not huge. Thus, there was not much concern in this project about fitting the implemented layouts cells in corner cell. Layouts were minimized as much as possible to decrease parasitic capacitances. From BSTEST layout, it can be clearly seen that the layout of this project is using less than 70% of all available spacing.

Timing diagram should be simulated first to check functionality of schematic. In this project, Layout of multiplexer logic failed. This delayed ability to finish project completely in time. The d flip flop and multiplexer were fixed in time although BSTEST layouts were not completed in time.

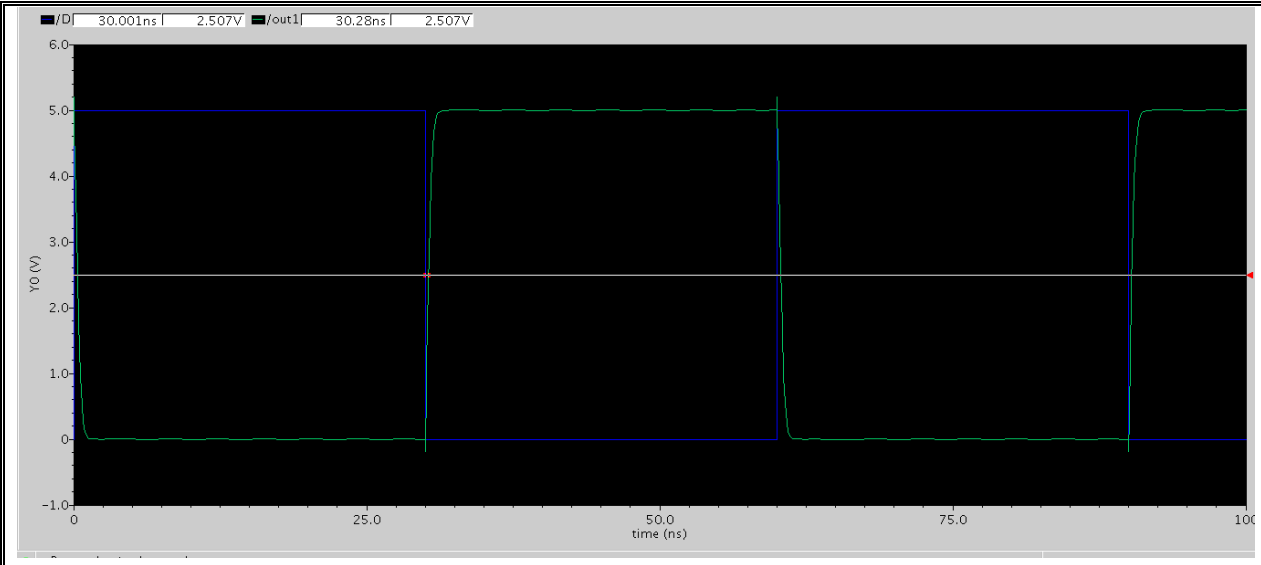
The project 1 was finished in time without cell sizes minimized to the most minimum size. There was problem with server for waveform simulation right before project was due. It could be expected in industry. It is employee's responsibility to start work early and finish in time; it also depends on manager's leniency on deadline. Project 1 cell layouts were later corrected to most minimum size being optimized to decrease time delay, decrease parasitic capacitance and increase performance. When doing layout, pins names should be capital letters which are industry standard. In this project, this was accidentally ignored; the finishing layouts and simulation was first priority. The later optimization of project 1 cells took some time away from finishing project 2. Since finger transistors were not used in project 1, there was little space for two contacts in the middle of cells after minimizing cells and had difficulty in putting two contacts for inputs and outputs. 1 week was spent on moving the NMOS and PMOS around until the poly was noticed that it could pass through metal 1 of ground without shorting the cells. The poly didn't move contacts of the metal 1 in both ground and Vdd. The DRC and LVS clean of the layout confirm the validity of using poly passing through ground metal.

For project 2, the timing simulation of XOR is similar to project 1 simulation. Matching the truth logic of gate with the simulation diagram verify the functionality of XOR. Propagation delay is extracted by observing the timing delay difference between 50% of output and 50% of input assuming other inputs are constant. For DFF simulation, in addition to the logic verification, the minimum pulse width of clock 1 and clock 2, and the guard time were observed and included in lab report. The BSSUM simulation needed more time and could not be included in this lab report. The simulation needed manual timing inputs with careful consideration.

These projects take a lot of time. The layouts being minimized as much as possible when not familiar with the tools are hard. The layouts are relatively easily minimized when tools become familiar as time goes on although it takes time and effort. Project 1 layouts are at the

best situation. If the layouts were to be implemented again, the poly connecting input or output contacts would not pass through the ground and VDD metals. There will be other ways to do it although it will take more time. Pin names will be changed to capital letters. For improving project 2, BSSUM simulation could be finished considering more time is available and not a lot of other classes work. Project 2 layouts were optimized. All project 1 and 2 cell layouts are completed successfully without DRC and LVS errors and warnings.

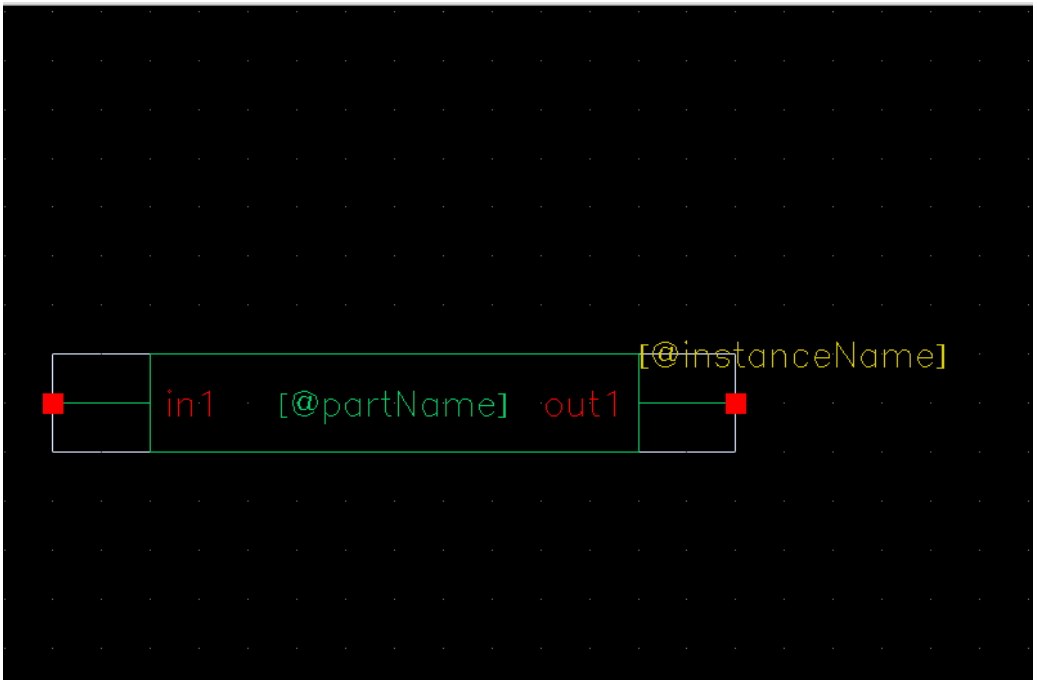
Cell Name:	**Zxw_inv**
Function/Truth Table:	
A	**Y**
0	**1**
1	**0**
Propagation Delay:	

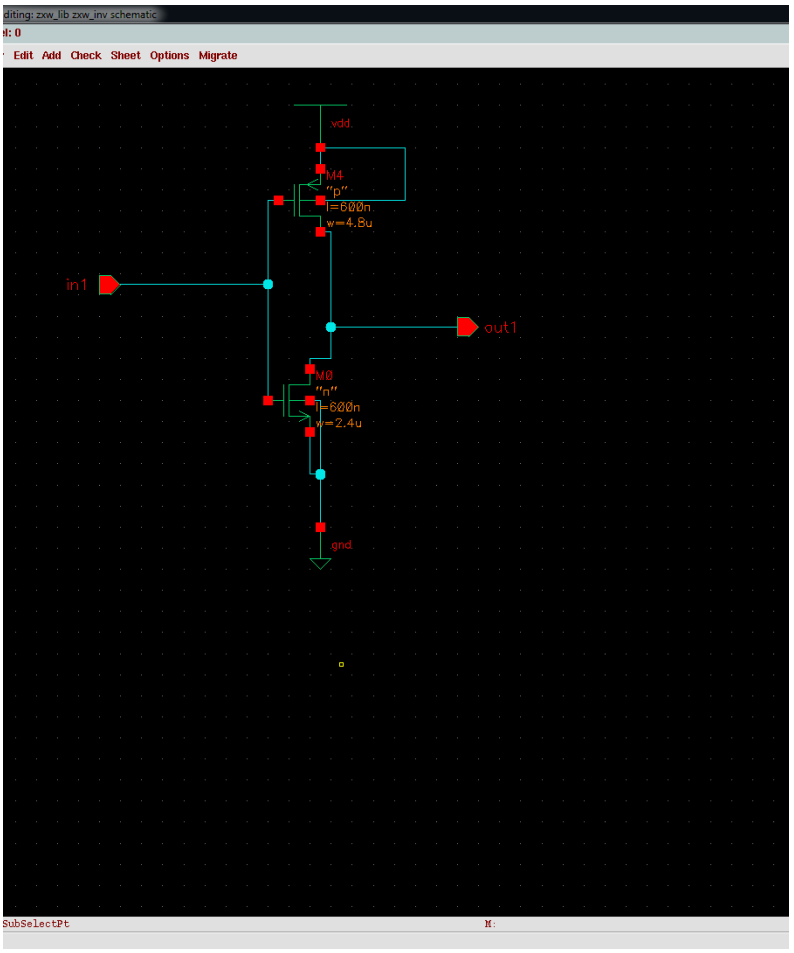


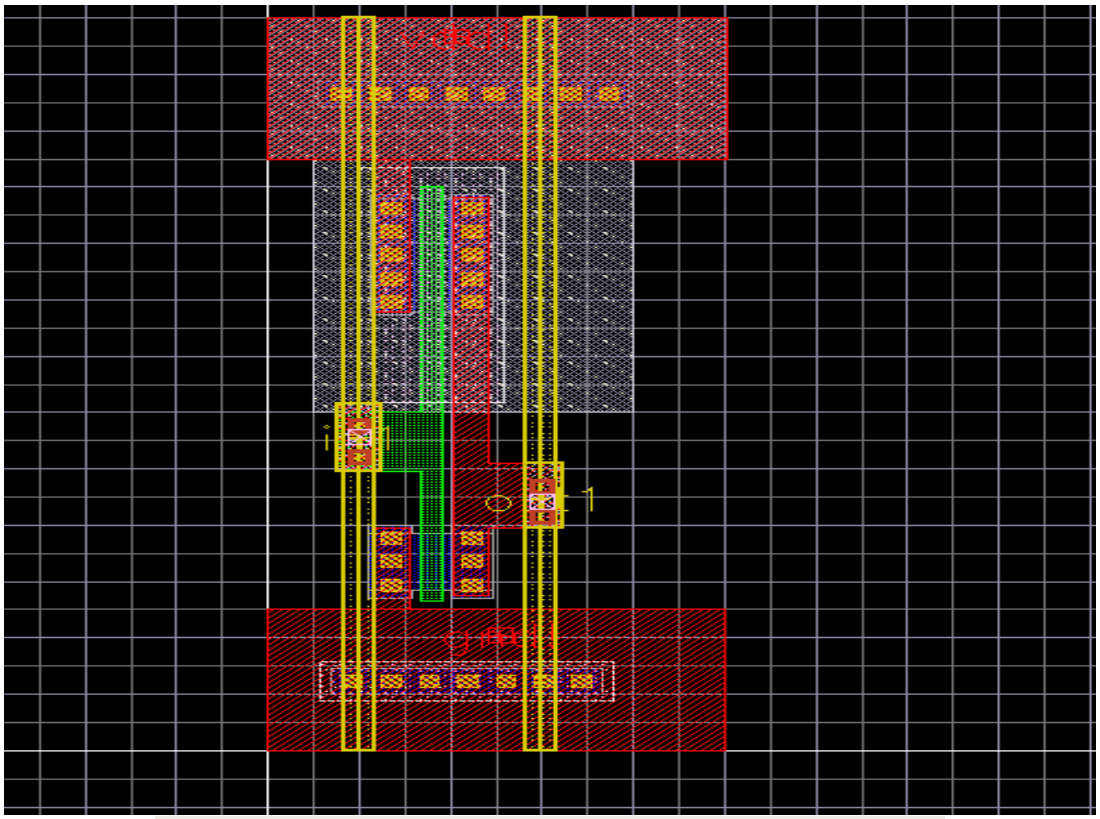
Layout 374.4 um^2

A Y ↑ .342ns

A Y↓ .28ns


[@instanceName]
in1
[@partName]
out1


Edit Add Check Sheet Options Migrate
vdd
M4
"p"
l=600n
w=4.8u
in1
out1
M0
"n"
l=600n
w=2.4u
gnd
SubSelectPt



```
//Verilog HDL for "zxw_lib", "zxw_inv" "zxw_inv"

module zxw_inv ( out1, in1 );

  output out1;
  input in1;
  not(out1,in1);
endmodule
~
~
```

zxw_inv.sp = (~/ee620) - GVIEW

File Edit Tools Syntax Buffers Window Help

```
M0      out1#3  in1#6   gnd!#3  gnd!#1  nmos    L=0.6   W=2.4
+ AD=3.89       AS=4.045        PD=6.4  PS=6.5
M4      out1#4  in1#4   vdd!#3  vdd!#1  pmos    L=0.6   W=4.8
+ AD=6.57       AS=6.57 PD=8    PS=8
*
*
*       RESISTOR AND CAP/DIODE CARDS
*
Re1     in1#4   in1#5     391.9460
Re2     in1#5   in1#1      19.2000
Re3     in1#5   in1#6     249.4459
Rc1     in1#1   in1#2      20.5000
Rc2     out1#1  out1#2      0.5433
Rc3     out1#2  out1#3     26.8841
Rc4     out1#2  out1#4     20.9163
Rc5     gnd!    gnd!#2  1.240E-02
Rc6     gnd!#2  gnd!#3     26.9329
Rc7     gnd!#1  gnd!#2     14.2857
Rc8     vdd!#2  vdd!    1.728E-02
Rc9     vdd!    vdd!#3     20.4560
Rc10    vdd!#1  vdd!#2     10.0000
Rb1     in1     in1#2       0.5000
Rb2     out1#1  out1        0.5000
*
*       CAPACITOR CARDS
*
*
C1      out1    vdd!    1.222E-16
C2      in1#5   gnd!#1  5.743E-16
C3      out1#2  gnd!#1  2.843E-16
C4      out1#4  in1#5   5.198E-17
C5      gnd!#3  out1#3  1.069E-16
C6      out1    gnd!#1  3.653E-16
C7      out1    vdd!#1  2.474E-16
C8      out1#4  in1#4   1.877E-16
C9      vdd!#1  in1#4   3.898E-17
C10     in1#6   gnd!#1  3.531E-16
C11     vdd!#3  in1#4   1.776E-16
C12     in1#1   gnd!#1  7.440E-16
C13     out1#3  in1#6   9.305E-17
C14     gnd!#3  in1#5   7.055E-18
C15     out1#1  gnd!#1  3.668E-16
C16     gnd!#3  in1#6   1.032E-16
C17     out1#2  in1#6   2.143E-17
C18     in1#1   gnd!#3  2.116E-17
C19     out1#2  in1#5   2.814E-16
C20     in1#1   out1#2  3.521E-17
C21     vdd!#1  gnd!#1  1.899E-16
```

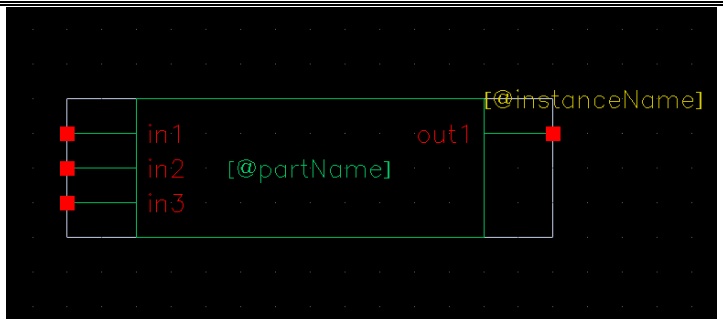
Library Name:	Zxw_lib
Cell Name:	Zxw_mux2

Function/Truth Table:

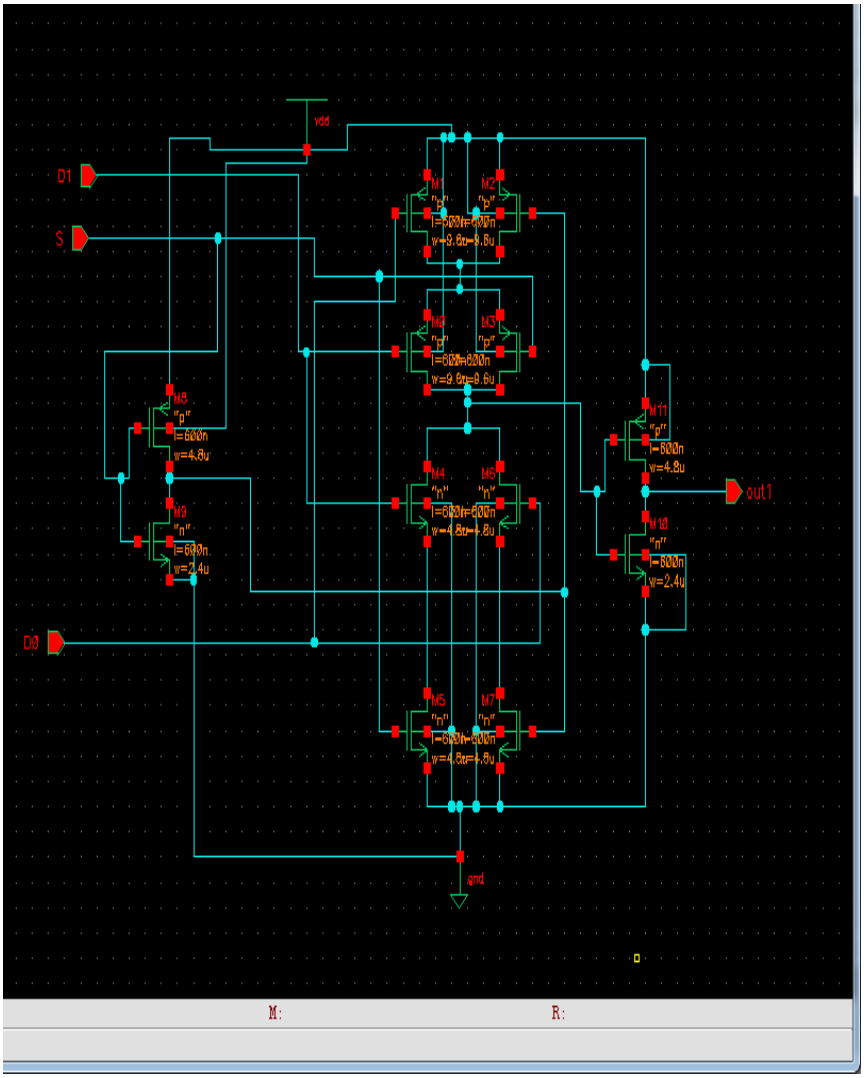
S A1 A0	Y
0 0 0	0
0 0 1	0
0 1 0	1
0 1 1	1
1 0 0	0
1 0 1	1
1 1 0	0
1 1 1	1

A1	Y ↑	.473n	
A1	Y↓	.507ns	
A0	Y ↑	.383n	
A0	Y↓	.442n	
S	Y ↑	.322n	
S	Y↓	.372n	

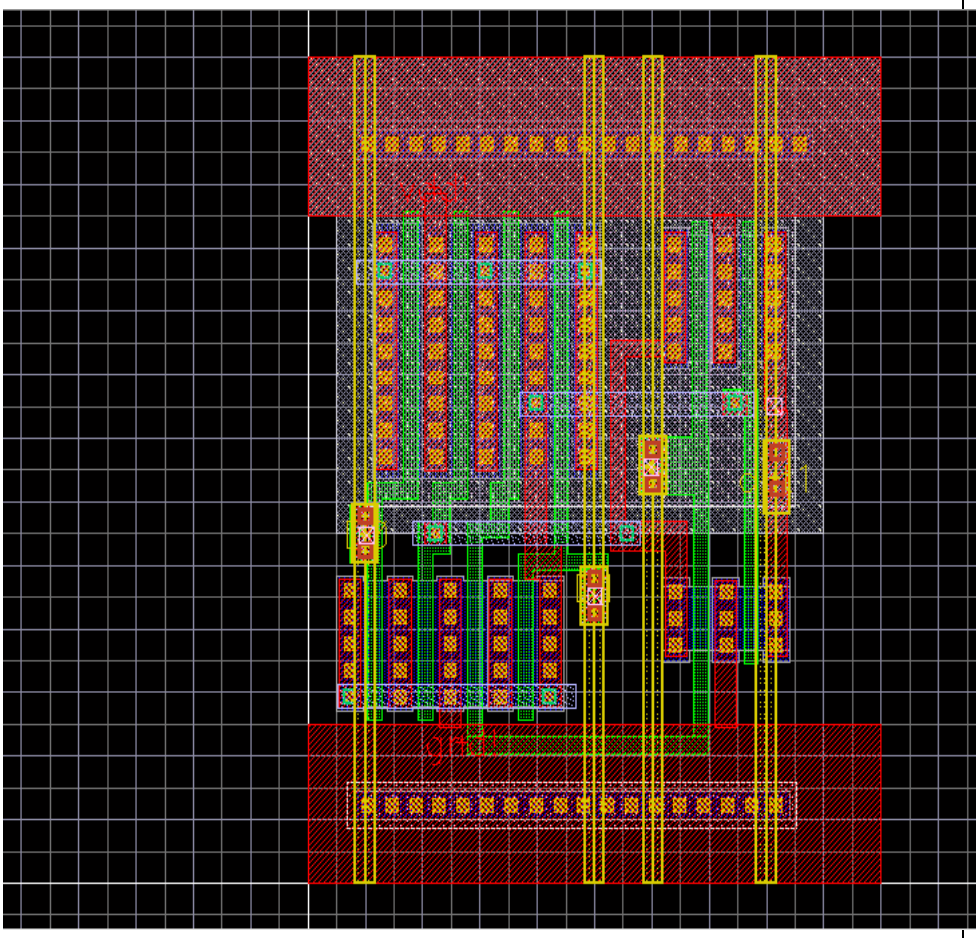
Symbol with Port Names:


[@instanceName]
in1
in2
in3
[@partName]
out1

Schematic:


vdd
D1
S
D0
out1
gnd
M:
R:

Layout:



Layout 748.8 um^2

Verilog Model:

```
module zxw_mux2 (in1,in2,in3,in4,out1);
  Input in1;
  Input in2;
  Input in3;
  Input in4;
output out1;
```

and(a1, in1,in2);

and (a2,in3,in4);

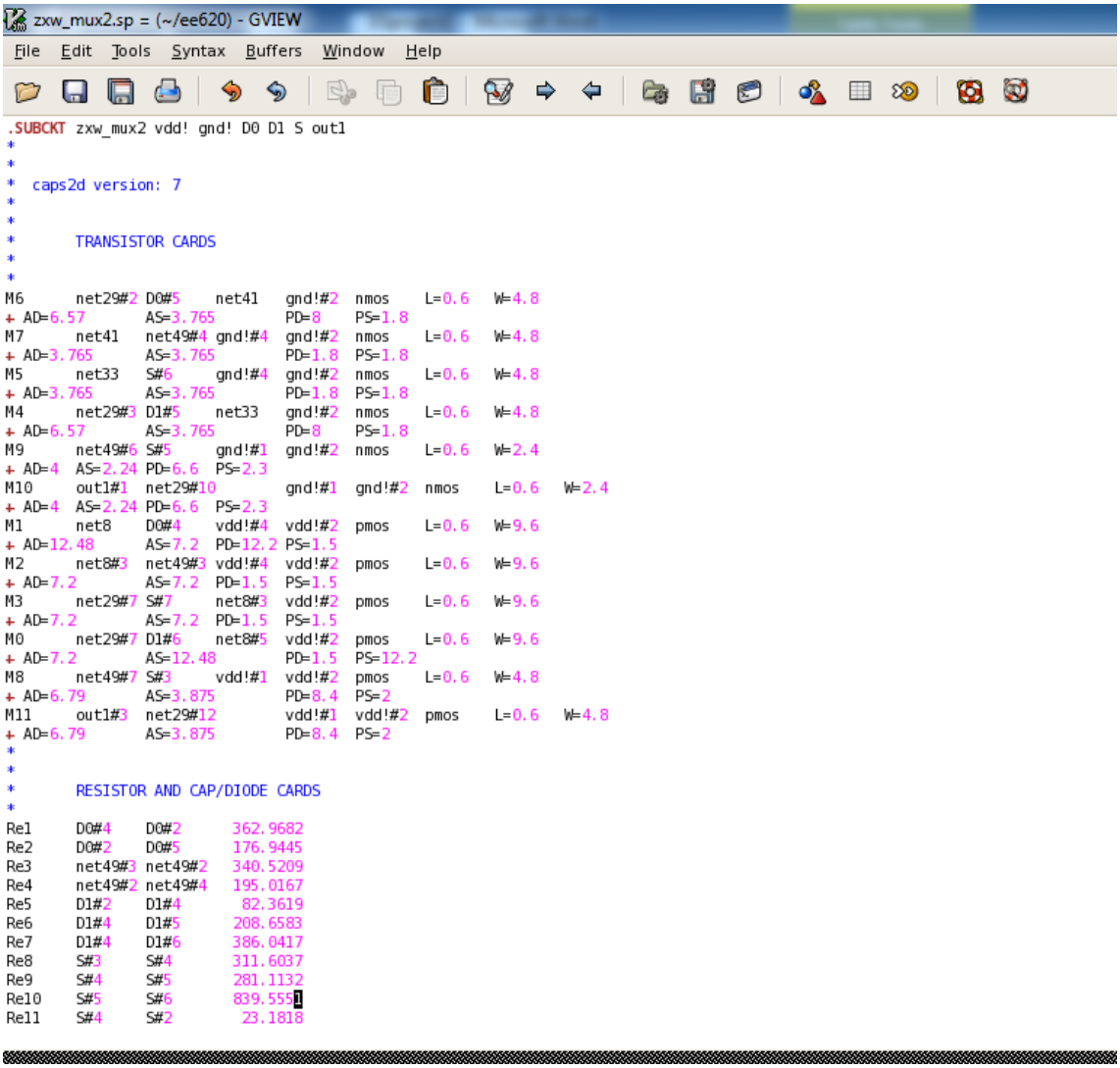
or(a3,a1,a2);

endmodule

Comments/Notes:

*****

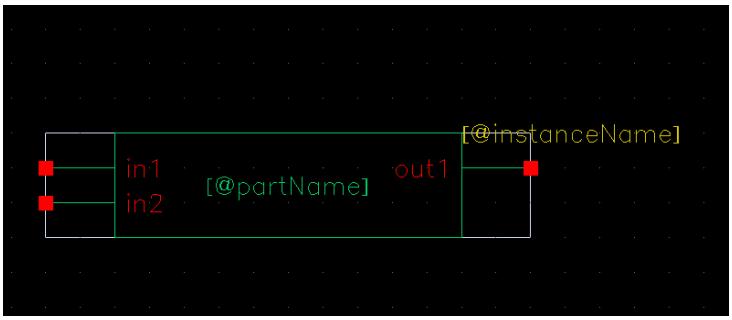
***Parasitic capacitance sheets**



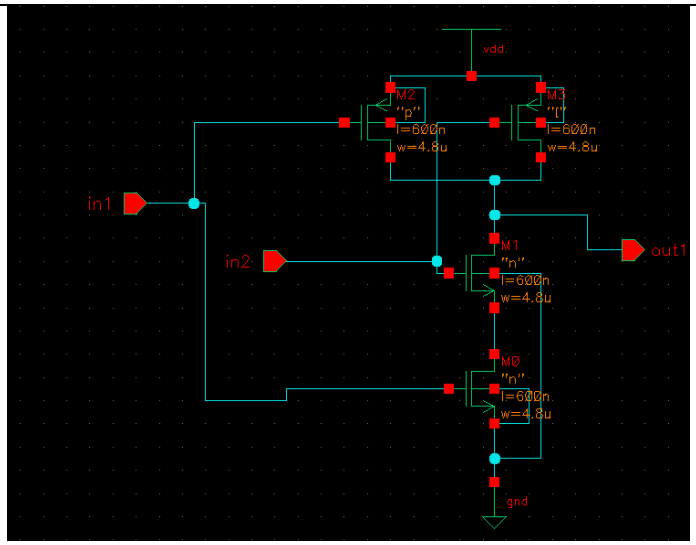

```
.SUBCKT zxw_mux2 vdd! gnd! D0 D1 S out1
*
*
*  caps2d version: 7
*
*
*       TRANSISTOR CARDS
*
*
M6      net29#2 D0#5    net41   gnd!#2  nmos    L=0.6   W=4.8
+ AD=6.57       AS=3.765        PD=8    PS=1.8
M7      net41   net49#4 gnd!#4  gnd!#2  nmos    L=0.6   W=4.8
+ AD=3.765      AS=3.765        PD=1.8  PS=1.8
M5      net33   S#6     gnd!#4  gnd!#2  nmos    L=0.6   W=4.8
+ AD=3.765      AS=3.765        PD=1.8  PS=1.8
M4      net29#3 D1#5    net33   gnd!#2  nmos    L=0.6   W=4.8
+ AD=6.57       AS=3.765        PD=8    PS=1.8
M9      net49#6 S#5     gnd!#1  gnd!#2  nmos    L=0.6   W=2.4
+ AD=4  AS=2.24 PD=6.6  PS=2.3
M10     out1#1  net29#10        gnd!#1  gnd!#2  nmos    L=0.6   W=2.4
+ AD=4  AS=2.24 PD=6.6  PS=2.3
M1      net8    D0#4    vdd!#4  vdd!#2  pmos    L=0.6   W=9.6
+ AD=12.48      AS=7.2  PD=12.2 PS=1.5
M2      net8#3  net49#3 vdd!#4  vdd!#2  pmos    L=0.6   W=9.6
+ AD=7.2        AS=7.2  PD=1.5  PS=1.5
M3      net29#7 S#7     net8#3  vdd!#2  pmos    L=0.6   W=9.6
+ AD=7.2        AS=7.2  PD=1.5  PS=1.5
M0      net29#7 D1#6    net8#5  vdd!#2  pmos    L=0.6   W=9.6
+ AD=7.2        AS=12.48        PD=1.5  PS=12.2
M8      net49#7 S#3     vdd!#1  vdd!#2  pmos    L=0.6   W=4.8
+ AD=6.79       AS=3.875        PD=8.4  PS=2
M11     out1#3  net29#12        vdd!#1  vdd!#2  pmos    L=0.6   W=4.8
+ AD=6.79       AS=3.875        PD=8.4  PS=2
*
*
*       RESISTOR AND CAP/DIODE CARDS
*
Re1     D0#4    D0#2      362.9682
Re2     D0#2    D0#5      176.9445
Re3     net49#3 net49#2   340.5209
Re4     net49#2 net49#4   195.0167
Re5     D1#2    D1#4       82.3619
Re6     D1#4    D1#5      208.6583
Re7     D1#4    D1#6      386.0417
Re8     S#3     S#4       311.6037
Re9     S#4     S#5       281.1132
Re10    S#5     S#6       839.5551
Re11    S#4     S#2        23.1818
```


Library Name:	
Cell Name:	**Zxw_nand2**
Function/Truth Table:	
0 0	**1**
0 1	**1**
1 0	**1**
1 1	**0**
Propagation Delay:	
A **Y↑**	**.310ns**
A **Y↓**	**.426n**
B **Y↑**	**.384ns**
B **Y↓**	**.390ns**

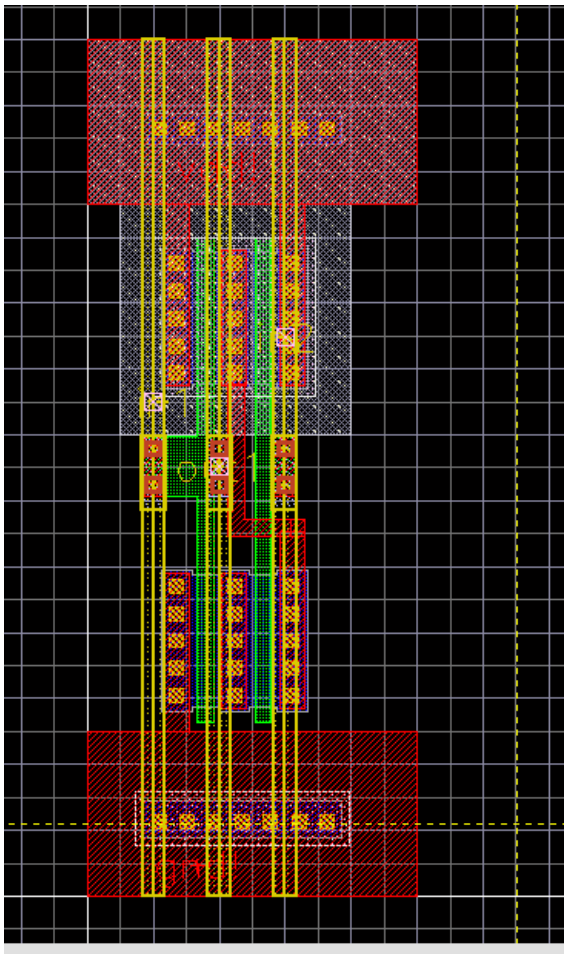
Symbol with Port Names:



Schematic:



Layout:



<u>Layout</u> 374.4 um^2

Verilog Model:

```
module zxw_nand (in1,in2,out1 );


        input in1;

        input in2;

        output out1;

        nand(out1,in1,in2);

endmodule
```

zxw_nand2.sp = (~/ee620) - GVIEW

File Edit Tools Syntax Buffers Window Help

```
.SUBCKT zxw_nand2 vdd! gnd! in1 in2 out1
*
*
*  caps2d version: 7
*
*
*       TRANSISTOR CARDS
*
*
M2      out1#3  in2#3   net4    gnd!#1  nmos    L=0.6   W=4.8
+ AD=6.57       AS=3.765        PD=8    PS=1.8
M3      net4    in1#6   gnd!#2  gnd!#1  nmos    L=0.6   W=4.8
+ AD=3.765      AS=6.57 PD=1.8  PS=8
M0      out1#5  in1#4   vdd!#4  vdd!#2  pmos    L=0.6   W=4.8
+ AD=3.765      AS=6.57 PD=1.8  PS=8
M1      out1#5  in2#4   vdd!#1  vdd!#2  pmos    L=0.6   W=4.8
+ AD=3.765      AS=6.57 PD=1.8  PS=8
*
*
*       RESISTOR AND CAP/DIODE CARDS
*
Re1     in1#4   in1#5     264.9745
Re2     in1#5   in1#1      21.8182
Re3     in1#5   in1#6     312.4745
Re4     in2#1   in2#2      26.6667
Re5     in2#2   in2#3     294.4413
Re6     in2#2   in2#4     244.4413
Rc1     in1#1   in1#2      20.5000
Rc2     in2#5   in2#1       0.5000
Rc3     out1#3  out1#4     16.9026
Rc4     out1#4  out1#1  1.159E-02
Rc5     out1#4  out1#5     20.6351
Rc6     vdd!#1  vdd!#3     20.4591
Rc7     vdd!#3  vdd!    1.274E-02
Rc8     vdd!    vdd!#4     20.4579
Rc9     vdd!#2  vdd!#3     11.4286
Rc10    gnd!#1  gnd!       14.3091
Rc11    gnd!    gnd!#2     16.3670
Rb1     in1#3   in1#2       0.5000
Rb2     out1#1  out1        1.0000
Rb3     in2#6   in2#5       0.5000
Ra1     in1     in1#3       0.1175
Ra3     in2     in2#6       0.2350
*
*       CAPACITOR CARDS
*
*
C1      out1#3  in2#2   6.475E-17
```

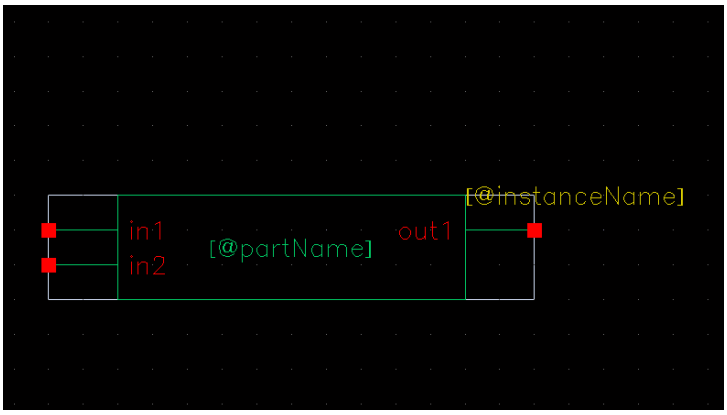

Library Name:	
Cell Name:	**Zxw_nor**
Function/Truth Table:	

f0 0	**1**
0 1	**0**
1 0	**0**
1 1	**0**

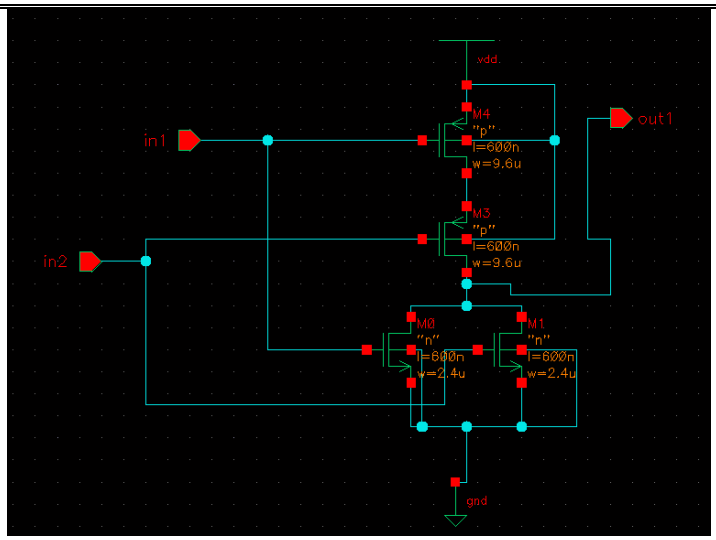
Propagation Delay:

A **Y↑**	**.36ns**
A **Y↓**	**.29ns**
B **Y↑**	**.2529ns**
B **Y↓**	**.31ns**

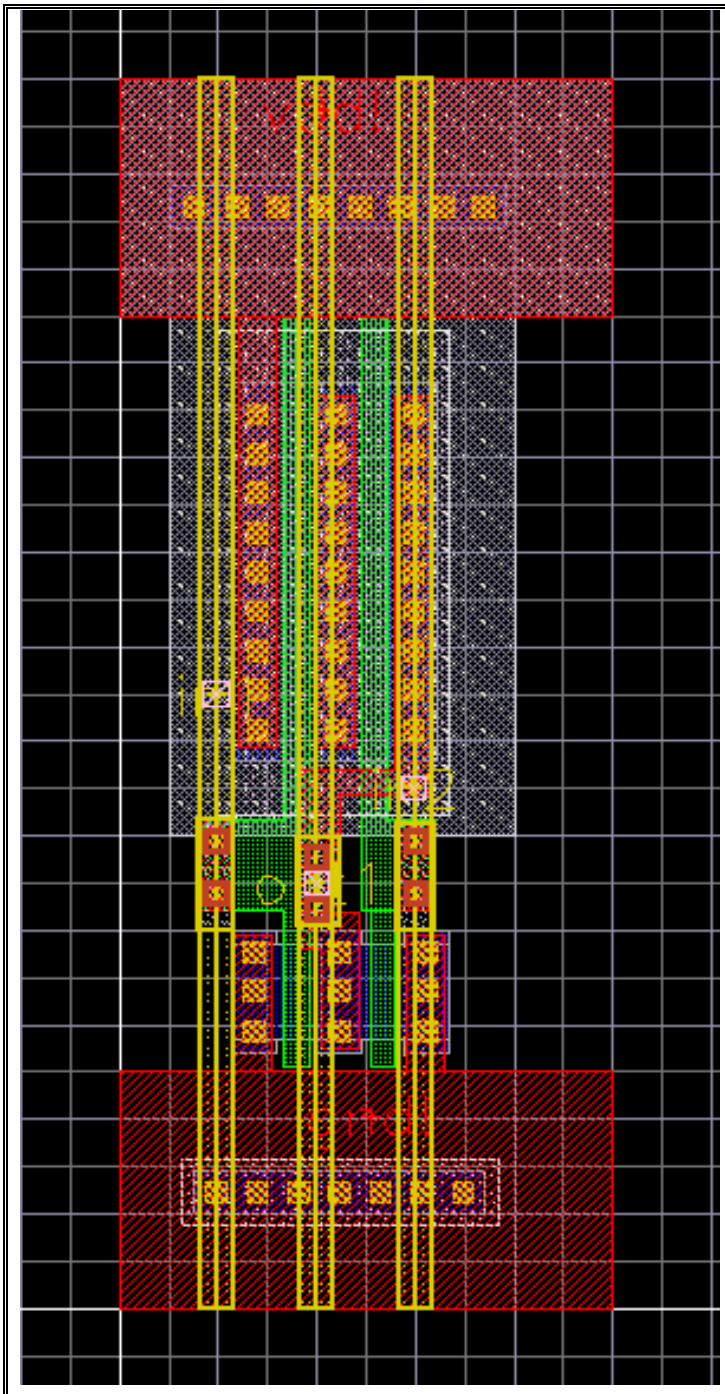
Symbol with Port Names:



Schematic:


vdd
M4
"p"
l=600n
w=9.6u
in1
out1
M3
"p"
l=600n
w=9.6u
in2
M0
"n"
l=600n
w=2.4u
M1
"n"
l=600n
w=2.4u
gnd

Layout:



Layout 374.4 um^2


```
.SUBCKT zxw_nor2 vdd! gnd! in1 in2 out1
*
*
*  caps2d version: 7
*
*
*       TRANSISTOR CARDS
*
*
M1      out1#4  in2#4   gnd!#1  gnd!#2  nmos    L=0.6   W=2.4
+ AD=2.185      AS=3.89 PD=2.2  PS=6.4
M0      out1#4  in1#6   gnd!#4  gnd!#2  nmos    L=0.6   W=2.4
+ AD=2.185      AS=3.89 PD=2.2  PS=6.4
M3      out1#3  in2#3   net29   vdd!#1  pmos    L=0.6   W=9.6
+ AD=11.52      AS=6.24 PD=12   PS=1.3
M4      net29   in1#4   vdd!#3  vdd!#1  pmos    L=0.6   W=9.6
+ AD=6.24       AS=12.48        PD=1.3  PS=12.2
*
*
*       RESISTOR AND CAP/DIODE CARDS
*
Re1     in1#4   in1#5     367.2919
Re2     in1#5   in1#1      21.5217
Re3     in1#5   in1#6     154.7919
Re4     in2#1   in2#2      29.1304
Re5     in2#2   in2#3     349.4290
Re6     in2#2   in2#4     140.2702
Rc1     in1#1   in1#2      20.5000
Rc2     out1#3  out1#1     12.0720
Rc3     out1#1  out1#4     26.8997
Rc4     in2#5   in2#1       0.5000
Rc5     gnd!#1  gnd!       26.9210
Rc6     gnd!    gnd!#3  1.063E-02
Rc7     gnd!#3  gnd!#4     26.9347
Rc8     gnd!#2  gnd!#3     14.2857
Rc9     vdd!#2  vdd!    1.735E-02
Rc10    vdd!    vdd!#3     11.7920
Rc11    vdd!#1  vdd!#2     10.0000
Rb1     in1#3   in1#2       0.5000
Rb2     out1#1  out1        1.0000
Rb3     in2#6   in2#5       0.5000
Ra1     in1     in1#3       0.2175
Ra3     in2     in2#6       0.1000
*
*       CAPACITOR CARDS
*
*
C1      out1#1  gnd!#1  1.568E-17
```

Verilog Model:

```
module zxw_nor ( in1,in2,out1);
        input in1;
        input in2;
        output out1;
        nor(out1,in1,in2);
endmodule
```

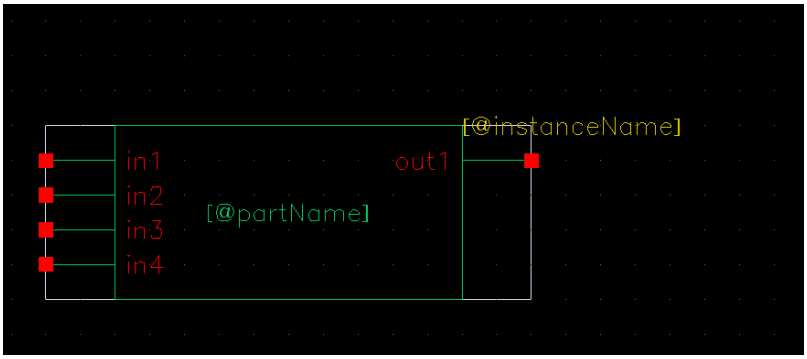
.

Library Name:	
Cell Name:	**Zxw_aoi**
Function/Truth Table:	
0000	**1**
0001	**1**
0010	**1**
0011	**0**
0100	**1**
0101	**1**
0110	**1**

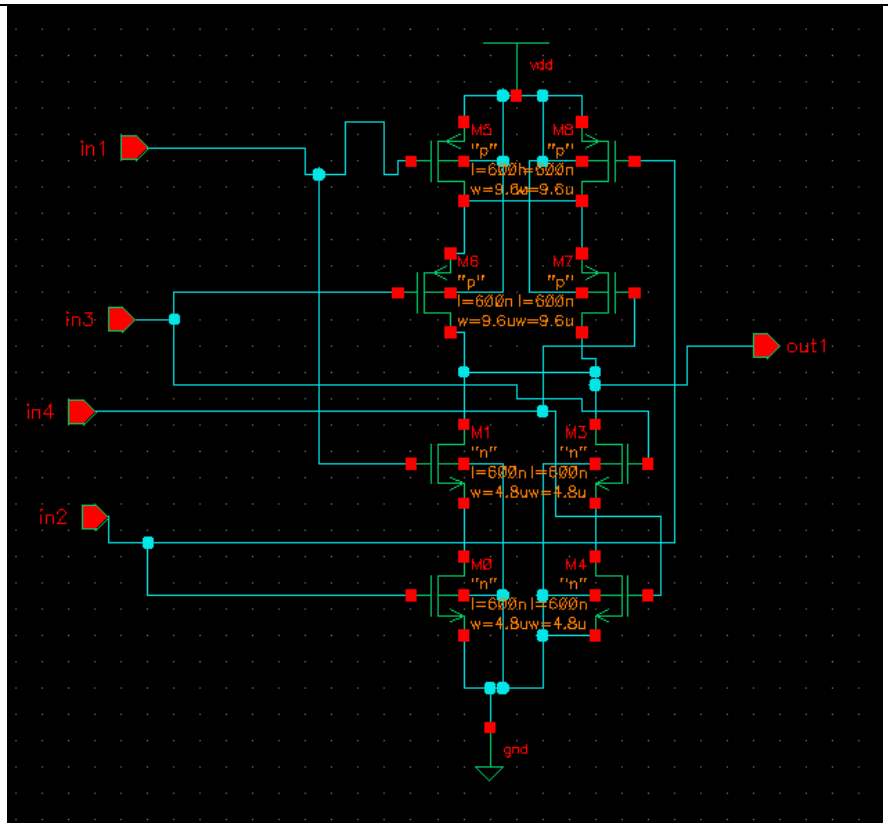
0111	**0**
1000	**1**
1001	**1**
1010	**1**
1011	**0**
1100	**0**
1101	**0**
1110	**0**
1111	**0**
Propagation Delay:	
A0 **Y↑**	**.370ns**
A0 **Y ↓**	**.545ns**
A1 **Y↑**	**.397ns**
A1 **Y ↓**	**.541ns**
B0 **Y↑**	**.712ns**

B0 **Y↓**	**.375ns**
B1 **Y↑**	**.339ns**
B1 **Y↓**	**.374ns**

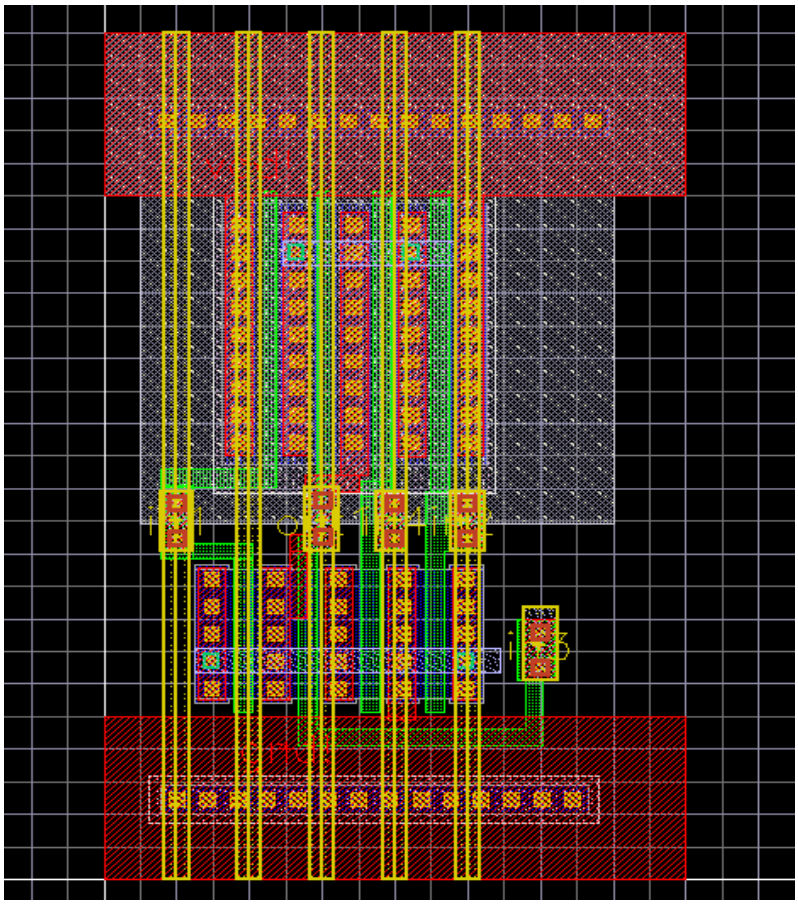
Symbol with Port Names:



Schematic:



Layout:



<u>Layout</u> 599.04 um^2

Verilog Model:

```
module zxw_aoi (in1,in2,in3,in4,out1 );
        input in1;
        input in2;
        input in3;
        input in4;
        output out1;
        and(a,in1,in2);
```

```
        and(b,in3,in4);

        or(c,a,b);

        not(out1,c);


endmodule
```

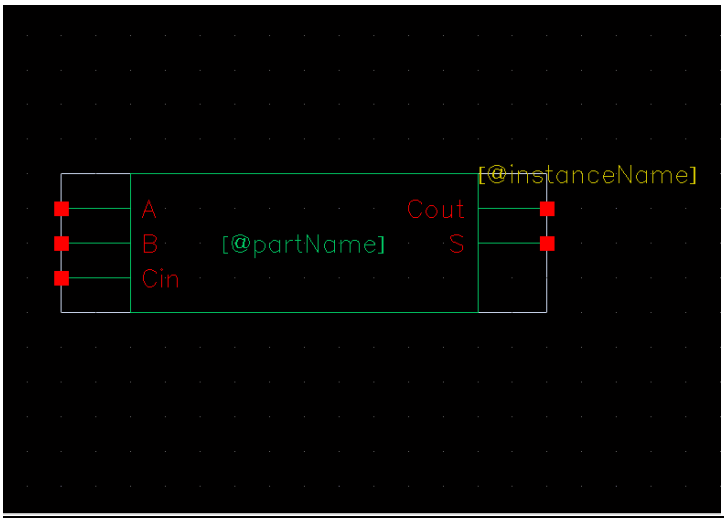
zxw_aoi2.sp = (~/ee620) - GVIEW

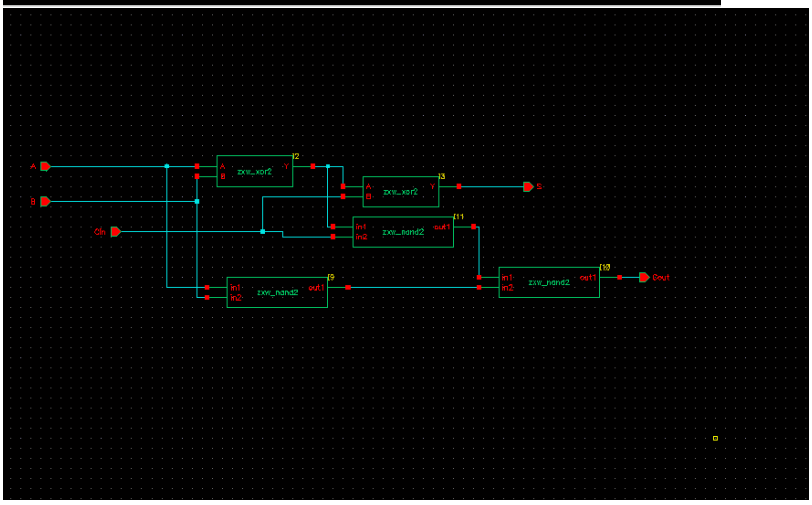
File Edit Tools Syntax Buffers Window Help

```
.SUBCKT zxw_aoi2 vdd! gnd! in1 in2 in3 in4 out1
*
*
*  caps2d version: 7
*
*
*       TRANSISTOR CARDS
*
*
M0      net33#4 in2#5   gnd!#1  gnd!#2  nmos    L=0.6   W=4.8
+ AD=6.57       AS=3.765        PD=8    PS=1.8
M4      net21   in4#3   gnd!#1  gnd!#2  nmos    L=0.6   W=4.8
+ AD=3.765      AS=3.765        PD=1.8  PS=1.8
M3      out1#4  in3#2   net21   gnd!#2  nmos    L=0.6   W=4.8
+ AD=3.765      AS=3.765        PD=1.8  PS=1.8
M1      out1#4  in1#5   net33#2 gnd!#2  nmos    L=0.6   W=4.8
+ AD=3.765      AS=6.57 PD=1.8  PS=8
M5      net12   in1#4   vdd!#4  vdd!#2  pmos    L=0.6   W=9.6
+ AD=6.24       AS=11.52        PD=1.3  PS=12
M6      out1#3  in3#1   net12   vdd!#2  pmos    L=0.6   W=9.6
+ AD=6.24       AS=6.24 PD=1.3  PS=1.3
M7      out1#3  in4#1   net12#3 vdd!#2  pmos    L=0.6   W=9.6
+ AD=6.24       AS=6.24 PD=1.3  PS=1.3
M8      net12#3 in2#6   vdd!#1  vdd!#2  pmos    L=0.6   W=9.6
+ AD=6.24       AS=11.52        PD=1.3  PS=12
*
*
*       RESISTOR AND CAP/DIODE CARDS
*
Re1     in1#4   in1#1     418.3636
Re2     in1#1   in1#5     262.3004
Re3     in4#1   in4#2     305.9051
Re4     in4#2   in4#3     174.5000
Re5     in2#1   in2#4      30.9091
Re6     in2#4   in2#5     186.1363
Re7     in2#4   in2#6     328.9197
Re8     in3#1   in3#2     556.0237
Re9     in3#2   in3#3     694.7712
Rc1     in1#1   in1#2      20.5000
Rc2     net33   net33#2    17.0944
Rc3     net12   net12#2    12.3944
Rc4     out1#3  out1#1     11.7946
Rc5     out1#1  out1#4     16.2544
Rc6     in4#4   in4#2      20.5000
Rc7     net12#3 net12#4    12.3944
Rc8     net33#3 net33#4    16.0944
Rc10    in3#3   in3#4       0.5000
Rc11    vdd!#1  vdd!#3     11.6769
```

Cell Name:	**Zxw_fa**
Function/Truth Table:	
A B Cin	**Cout Y**
0 0 0	**0 0**
0 0 1	**1 0**
0 1 0	**1 0**
0 1 1	**1 0**
1 0 0	**0 1**
1 0 1	**0 1**
1 1 0	**0 1**
1 1 1	**1 1**
A **Sum ↑**	**1.304ns**
A **Sum ↓**	**1.055ns**
B **Sum↑**	**.964ns**

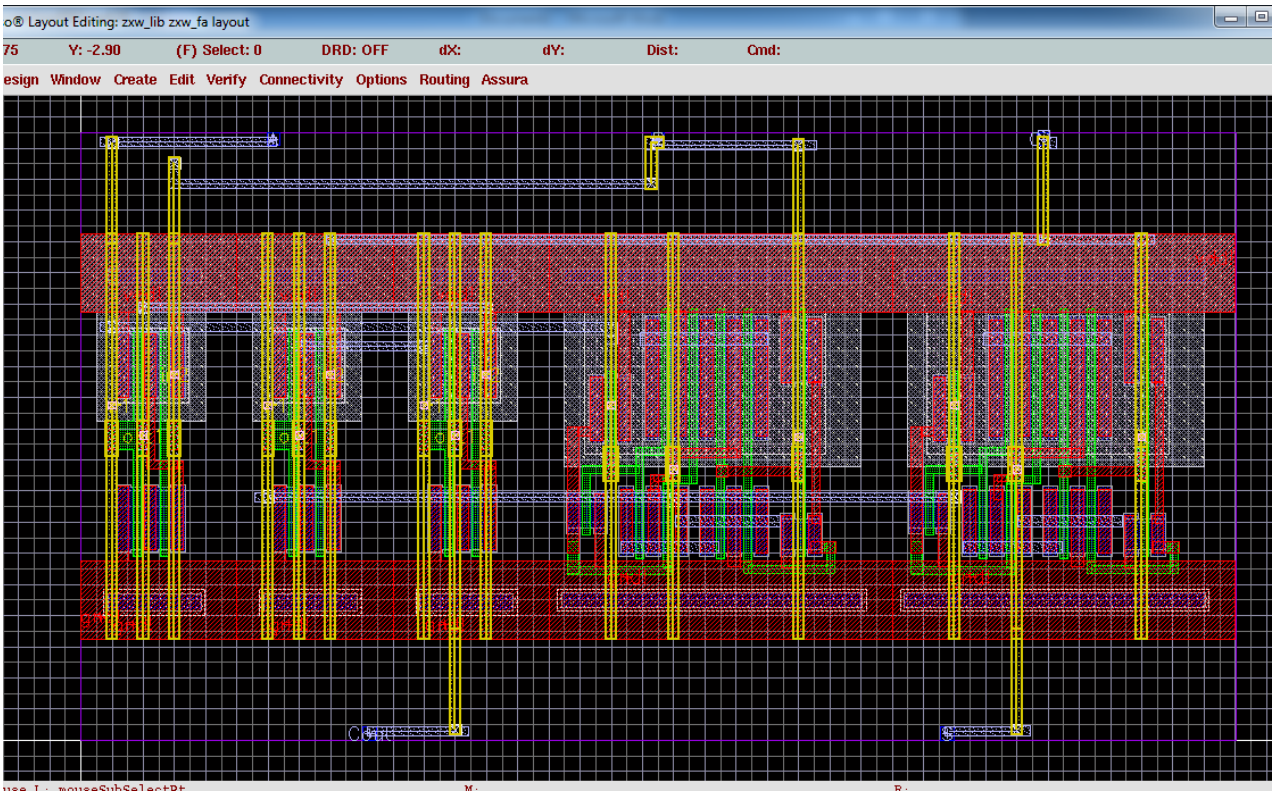
B **Sum ↓**	**1.03ns**
Cin **Sum ↑**	**.501ns**
Cin **Sum ↓**	**.455ns**
A **Cout ↑**	**.745ns**
A **Cout ↓**	**.748ns**
B **Cout ↑**	**.678ns**
B **Cout ↓**	**.274ns**
Cin **Cout ↑**	**.673ns**
Cin **Cout ↓**	**.251ns**

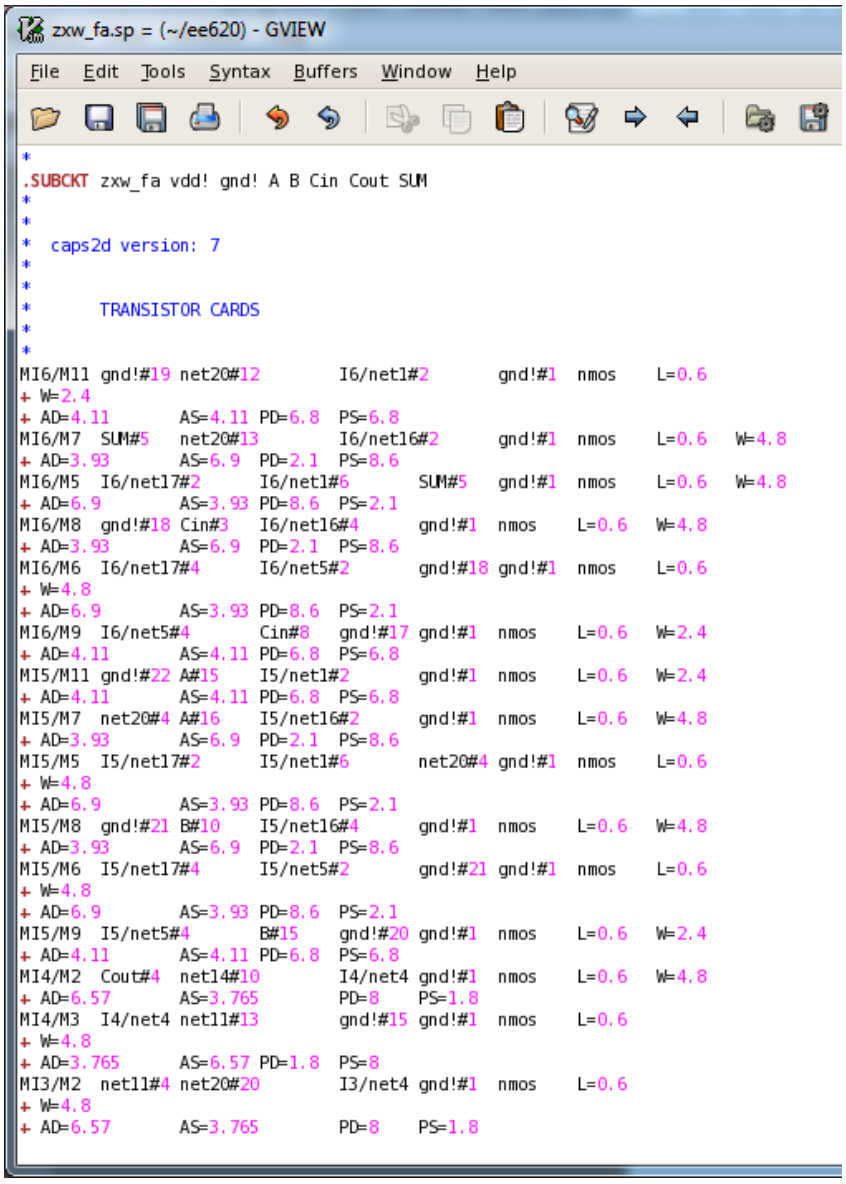





```
module zxw_fa ( Cout, S, A, B, Cin );

  input Cin;

  output S;

  input A;

  output Cout;

  input B;
```

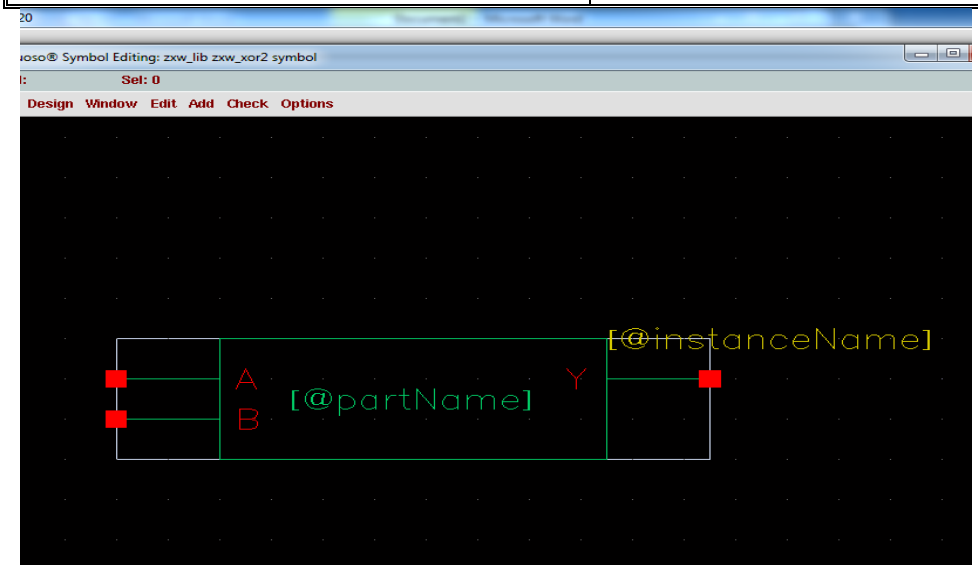
```
  xor(C,A,B);
  xor(S,C,Cin);
  nand(D,C,Cin);
  nand(E,A,B);
  nand(Cout,E,D);

endmodule
```

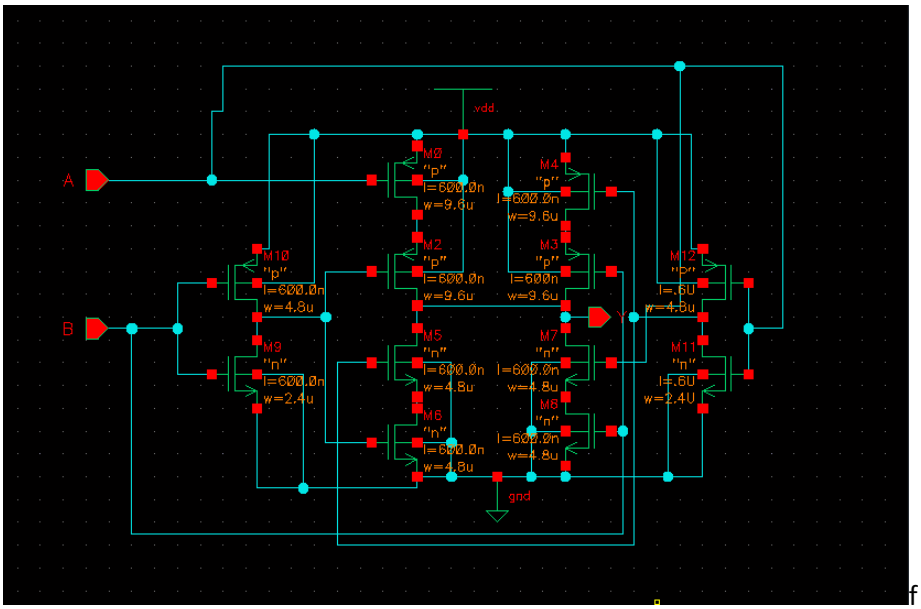

o® Layout Editing: zxw_lib zxw_fa layout
75 Y: -2.90 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd:
esign Window Create Edit Verify Connectivity Options Routing Assura



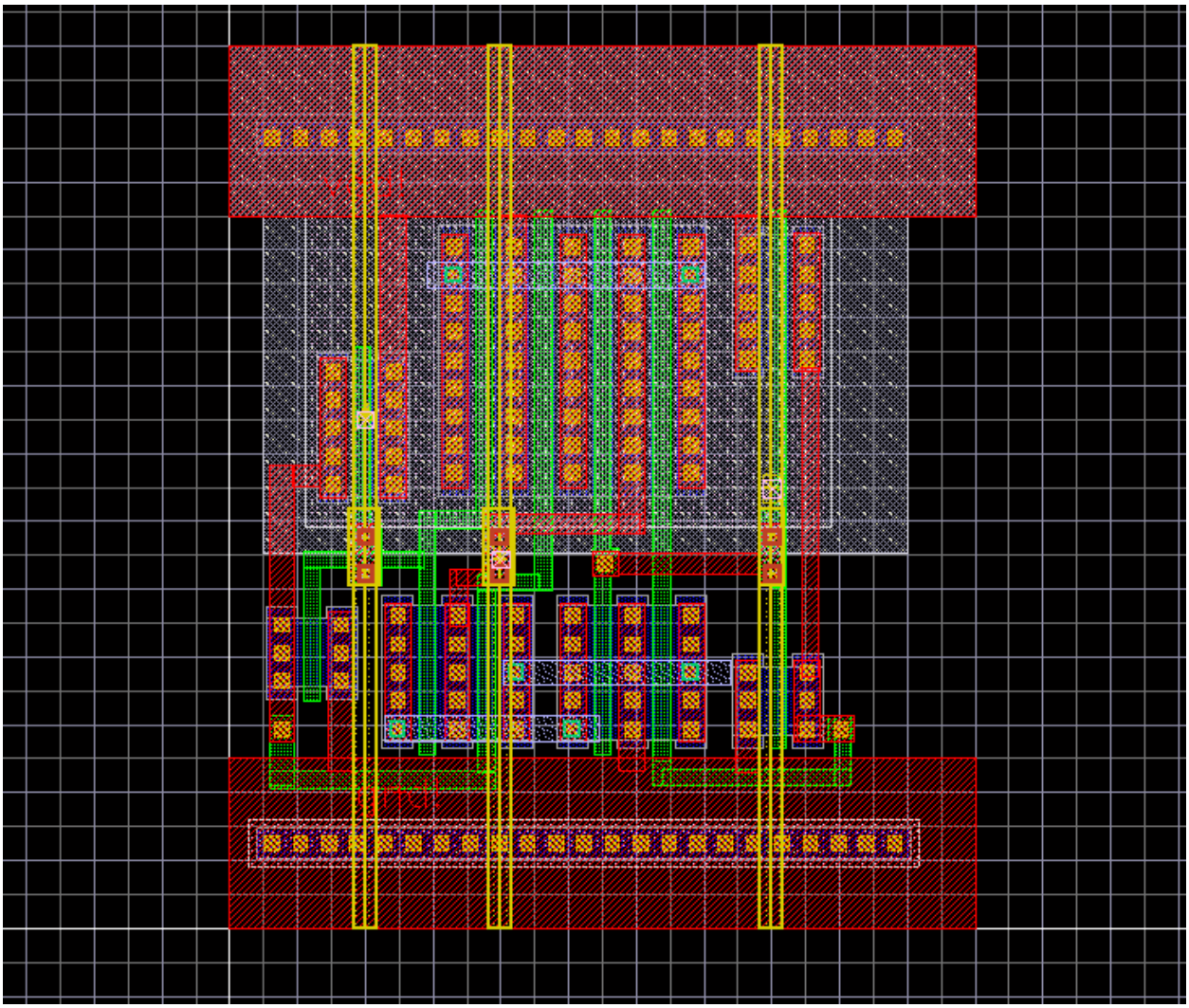
Cell Name:	**Zxw_xor**
Function/Truth Table:	
A1 A0	**Y**
0 0	**0**

0 1	**1**
1 0	**1**
1 1	**0**
B **Y↑**	**. 568 ns**
B **Y ↓**	**. 536 ns**
A **Y↑**	**. 548ns**
A **Y ↓**	**.534 ns**




vdd
gnd
A
B
Y
M0
"p"
l=600.0n
w=9.6u
M4
"p"
l=600.0n
w=9.6u
M2
"p"
l=600.0n
w=9.6u
M3
"p"
l=600n
w=9.6u
M10
"p"
l=600.0n
w=4.8u
M12
"p"
l=.6u
w=4.8u
M5
"n"
l=600.0n
w=4.8u
M7
"n"
l=600.0n
w=4.8u
M9
"n"
l=600.0n
w=2.4u
M11
"n"
l=.6u
w=2.4u
M6
"n"
l=600.0n
w=4.8u
M8
"n"
l=600.0n
w=4.8u

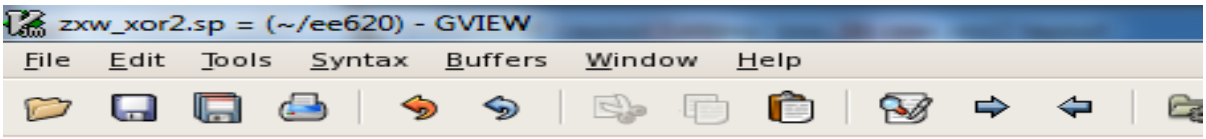
f



Layout 2776.8 um^2

```
module zxw_xor2 (A,B,Y );

    input A,B;

    output Y;

    xor(Y,A,B);
```

endmodule

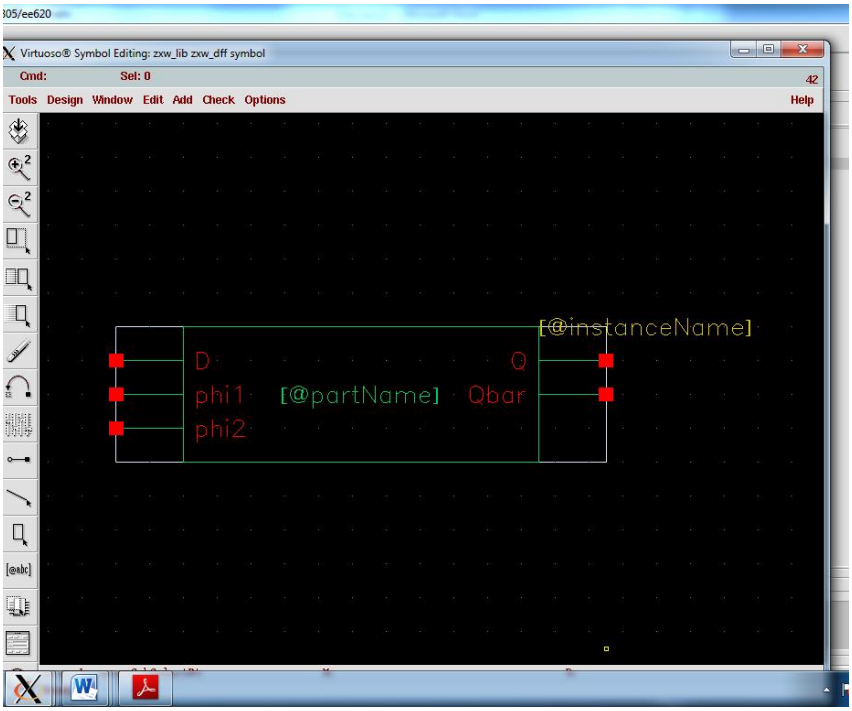


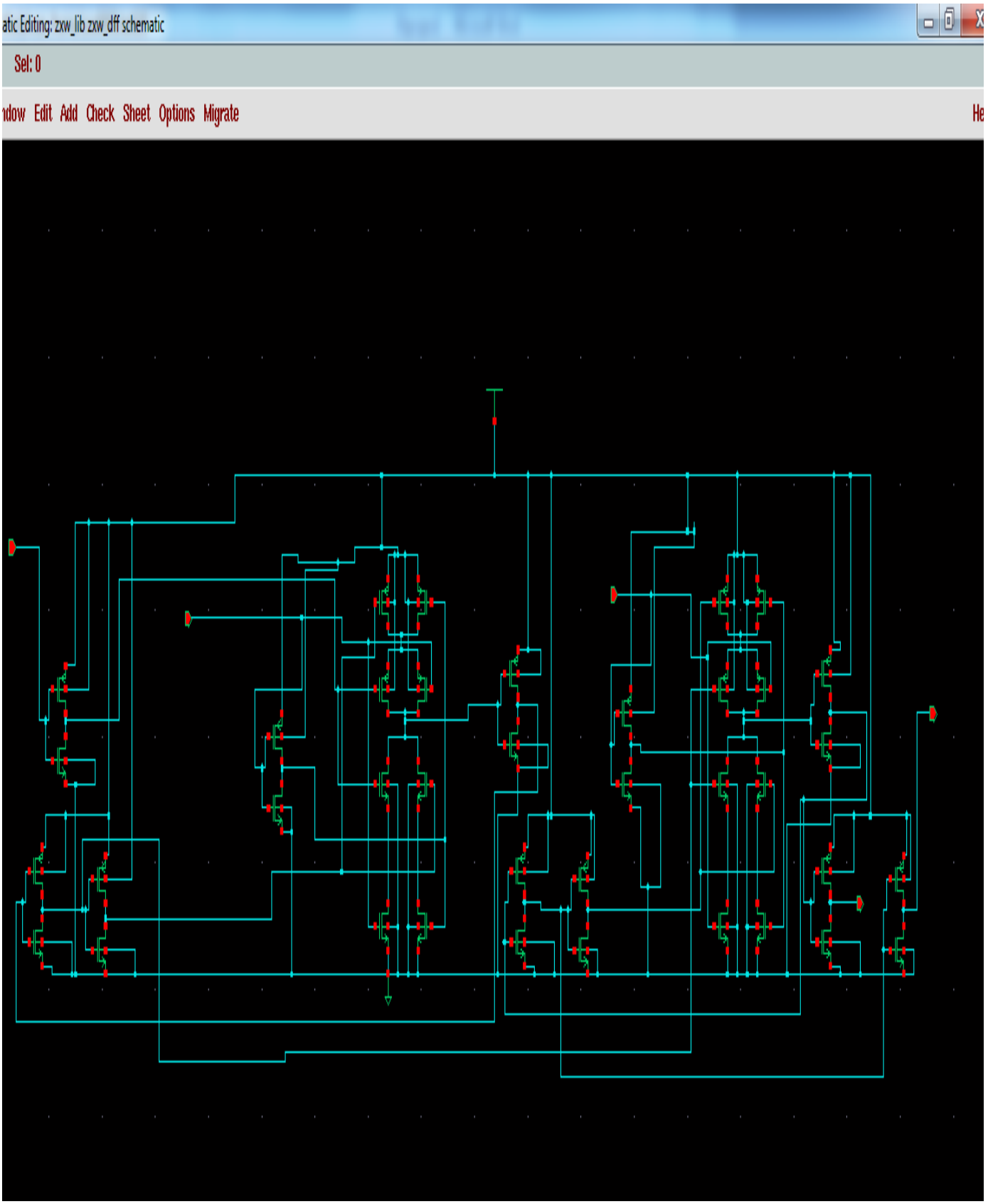

```
.SUBCKT zxw_xor2 vdd! gnd! A B Y
*
*
*  caps2d version: 7
*
*
*       TRANSISTOR CARDS
*
*
M11      net1#2  A#6      gnd!#6  gnd!#2  nmos     L=0.6    W=2.4
+ AD=4.11        AS=4.11  PD=6.8   PS=6.8
M7       Y#4     A#7      net16#2 gnd!#2  nmos     L=0.6    W=4.8
+ AD=3.93        AS=6.9   PD=2.1   PS=8.6
M5       Y#4     net1#6   net17#2 gnd!#2  nmos     L=0.6    W=4.8
+ AD=3.93        AS=6.9   PD=2.1   PS=8.6
M8       net16#4 B#3      gnd!#7  gnd!#2  nmos     L=0.6    W=4.8
+ AD=6.9         AS=3.93  PD=8.6   PS=2.1
M6       net17#4 net5#2   gnd!#7  gnd!#2  nmos     L=0.6    W=4.8
+ AD=6.9         AS=3.93  PD=8.6   PS=2.1
M9       net5#4  B#8      gnd!#1  gnd!#2  nmos     L=0.6    W=2.4
+ AD=4.11        AS=4.11  PD=6.8   PS=6.8
M12      net1    A#8      vdd!#8  vdd!#2  pmos     L=0.6    W=4.8
+ AD=6.79        AS=7.03  PD=8.4   PS=8.5
M0       net44   A#4      vdd!#7  vdd!#2  pmos     L=0.6    W=9.6
+ AD=12.48       AS=7.2   PD=12.2  PS=1.5
M4       net33   net1#5   vdd!#7  vdd!#2  pmos     L=0.6    W=9.6
+ AD=7.2         AS=7.2   PD=1.5   PS=1.5
M3       Y#3     B#1      net33   vdd!#2  pmos     L=0.6    W=9.6
+ AD=7.2         AS=7.2   PD=1.5   PS=1.5
M2       Y#3     net5     net44#3 vdd!#2  pmos     L=0.6    W=9.6
+ AD=7.2         AS=12.48         PD=1.5   PS=12.2
M10      net5#6  B#6      vdd!#1  vdd!#2  pmos     L=0.6    W=4.8
+ AD=6.79        AS=6.79  PD=8.4   PS=8.4
*
*
*       RESISTOR AND CAP/DIODE CARDS
*
Re1      A#4     A#5       424.8754
Re2      A#5     A#1        75.9090
Re3      A#1     A#6       225.7579
Re4      A#5     A#7       198.8517
Re5      A#1     A#8       203.0000
Re6      net1#5  net1#6    626.0237
Re7      net1#6  net1#4    584.4108
Re8      B#1     B#2       350.8333
Re9      B#2     B#3       185.0000
Re10     B#6     B#7       422.0797
Re11     B#7     B#8       241.2903
```

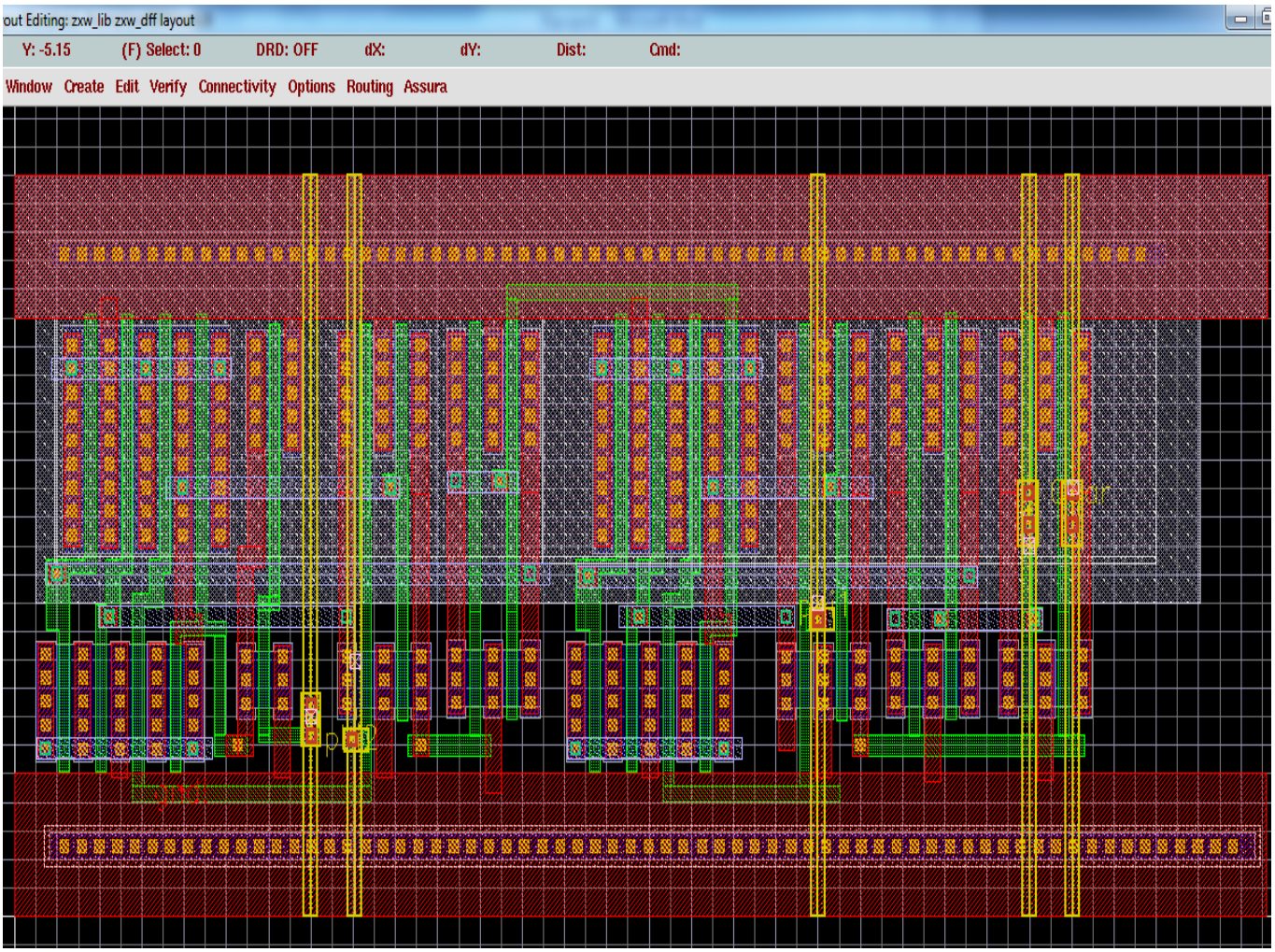
zxw_DFF

clk	Set	D	Q	Qbar
0	0	-	1	0
0	1	-	0	1
0 to 1	1	1	1	0
0 to 1	1	0	0	1

Phi1 **Q↑**	**2.04ns**
Phi1 **Q ↓**	**2.98ns**
Phi1 **Qbar↑**	**1.87ns**
Phi1 **Qbar↓**	**1.94ns**
Phi1 **minimum pulse width**	**450ps**
Phi2 **minimum pulse width**	**440ps**
Guard time	**1ps**


Virtuoso® Symbol Editing: zxw_lib zxw_dff symbol
Cmd:
Sel: 0
Tools Design Window Edit Add Check Options
Help
[@instanceName]
D
phi1
phi2
[@partName]
Q
Qbar

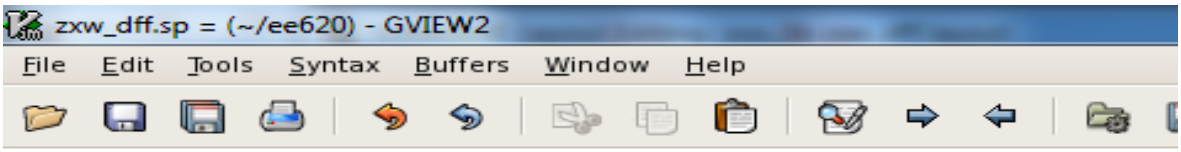

atic Editing: zxw_lib zxw_dff schematic
Sel: 0
ndow Edit Add Check Sheet Options Migrate
He



Layout 2096.6 um^2

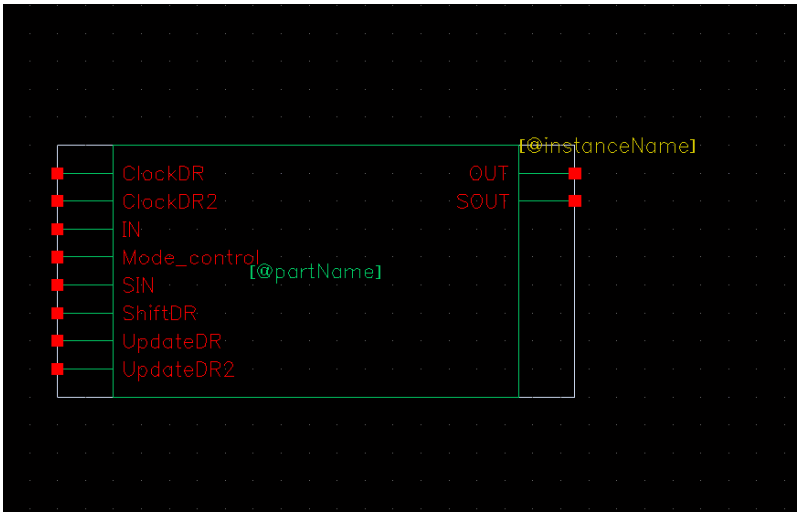
```
module zxw_dff ( Q, Qbar, D,phi2,phi1 );
        input D,phi2,phi1;
        output Q,Qbar;
        not(A,D);


        not(s2,phi2);
        fand(and1,s2,C);            // in2 is not feedback inverter
```

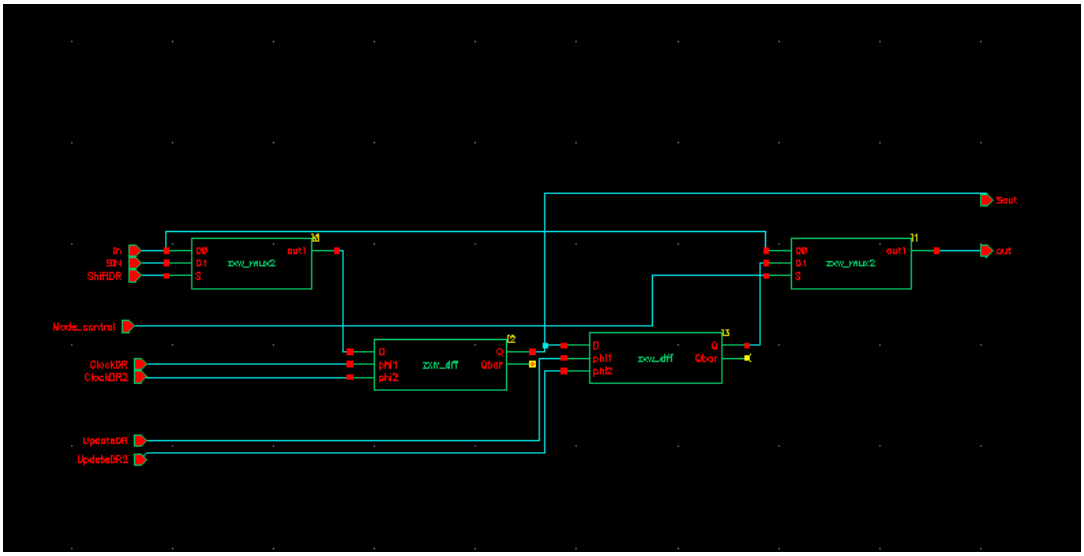
```
        and(and2,phi2,A);  // in3 is D
        or (Y,and1,and2);

        not(B,Y);
        not(C,B);

        not(s1,phi1);
        and(and3,s1,E);
        and(and4,phi1,B);
        or(Z,and3,and4);

        not(D,Z);
        not(E,D);
        not(Qbar,Z);
        not(Q,D);
endmodule
```

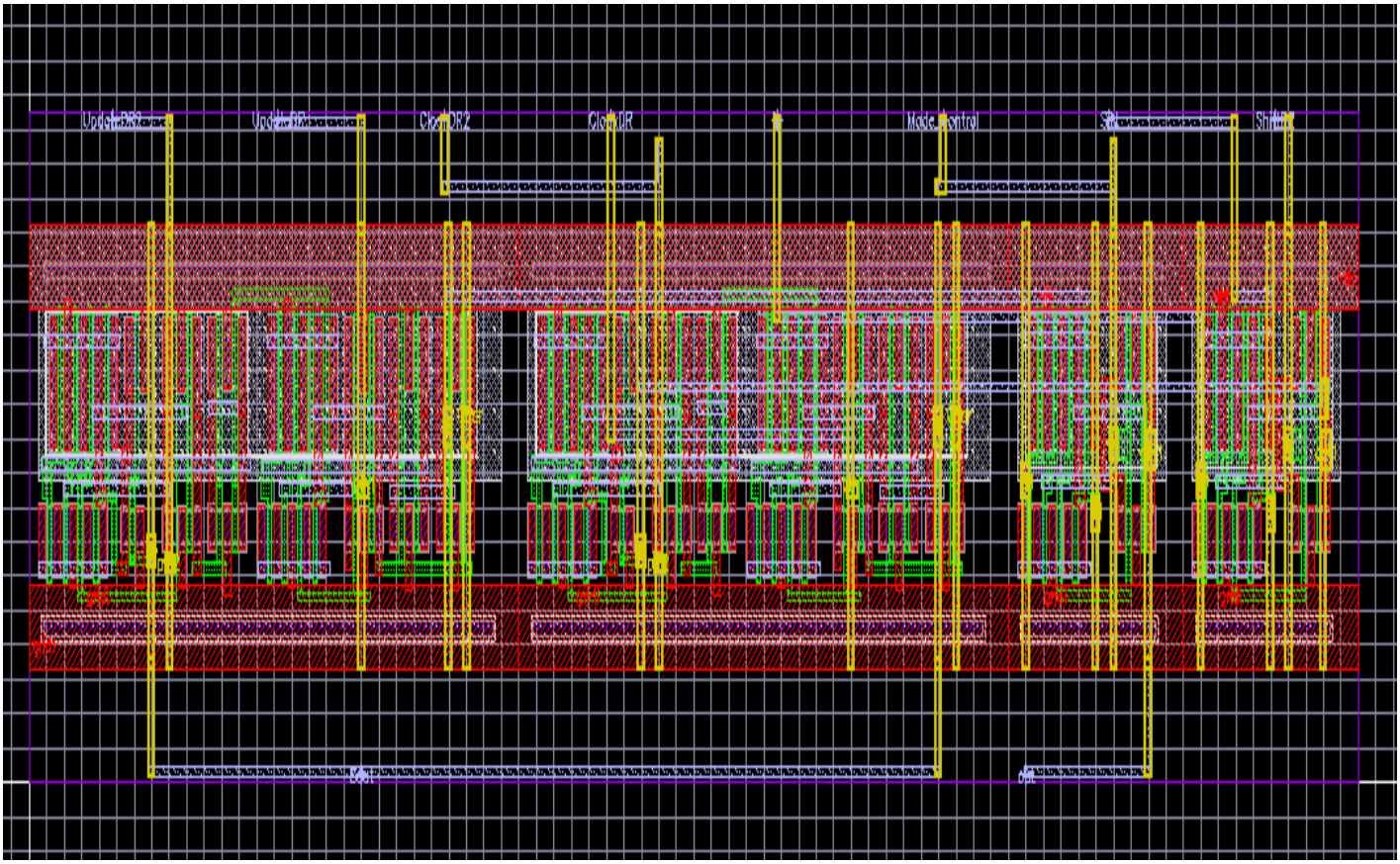



```
.SUBCKT zxw_dff gnd! D Q Qbar phi1 phi2
*
*
*  caps2d version: 7
*
*
*       TRANSISTOR CARDS
*
*
M50     net0183#2       net0346#4       net0268 gnd!#1  nmos    L=0.6
+ W=4.8
+ AD=6.57       AS=3.765        PD=8    PS=1.8
M51     net0268 net076#4        gnd!#16 gnd!#1  nmos    L=0.6
+ W=4.8
+ AD=3.765      AS=3.765        PD=1.8  PS=1.8
M49     net0260 phi1#5  gnd!#16 gnd!#1  nmos    L=0.6   W=4.8
+ AD=3.765      AS=3.765        PD=1.8  PS=1.8
M48     net0183#3       net0130#6       net0260 gnd!#1  nmos    L=0.6
+ W=4.8
+ AD=6.57       AS=3.765        PD=8    PS=1.8
M10     net076#7        phi1#4  gnd!#15 gnd!#1  nmos    L=0.6   W=2.4
+ AD=4  AS=2.24 PD=6.6  PS=2.3
M36     net0255#2       net0183#11      gnd!#15 gnd!#1  nmos    L=0.6
+ W=2.4
+ AD=4  AS=2.24 PD=6.6  PS=2.3
M27     net0261#3       net0255#8       gnd!#14 gnd!#1  nmos    L=0.6
+ W=2.4
+ AD=4.11       AS=2.295        PD=6.8  PS=2.4
M26     net0346#7       net0261#8       gnd!#14 gnd!#1  nmos    L=0.6
+ W=2.4
+ AD=4.11       AS=2.295        PD=6.8  PS=2.4
M31     Q#3     net0261#11      gnd!#13 gnd!#1  nmos    L=0.6   W=2.4
+ AD=4.11       AS=2.295        PD=6.8  PS=2.4
M30     Qbar#3  net0255#6       gnd!#13 gnd!#1  nmos    L=0.6   W=2.4
+ AD=4.11       AS=2.295        PD=6.8  PS=2.4
M45     net0187#2       net0286#4       net0216 gnd!#1  nmos    L=0.6
+ W=4.8
+ AD=6.57       AS=3.765        PD=8    PS=1.8
M46     net0216 net0220#4       gnd!#12 gnd!#1  nmos    L=0.6
+ W=4.8
+ AD=3.765      AS=3.765        PD=1.8  PS=1.8
M44     net0208 phi2#6  gnd!#12 gnd!#1  nmos    L=0.6   W=4.8
+ AD=3.765      AS=3.765        PD=1.8  PS=1.8
M43     net0187#3       net0211#3       net0208 gnd!#1  nmos    L=0.6
+ W=4.8
+ AD=6.57       AS=3.765        PD=8    PS=1.8
M20     net0211#6       D#4     gnd!#19 gnd!#1  nmos    L=0.6   W=2.4
+ AD=4  AS=4    PD=6.6  PS=6.6
```

BSC cell

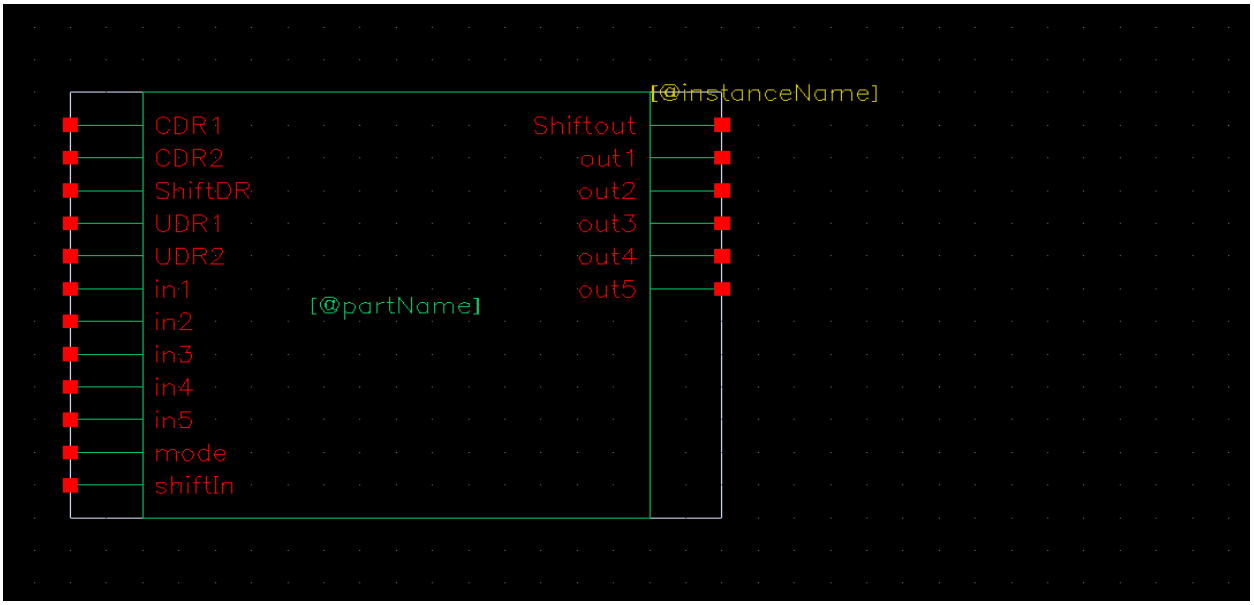

[@instanceName]
ClockDR
ClockDR2
IN
Mode_control
SIN
ShiftDR
UpdateDR
UpdateDR2
OUT
SOUT
[@partName]

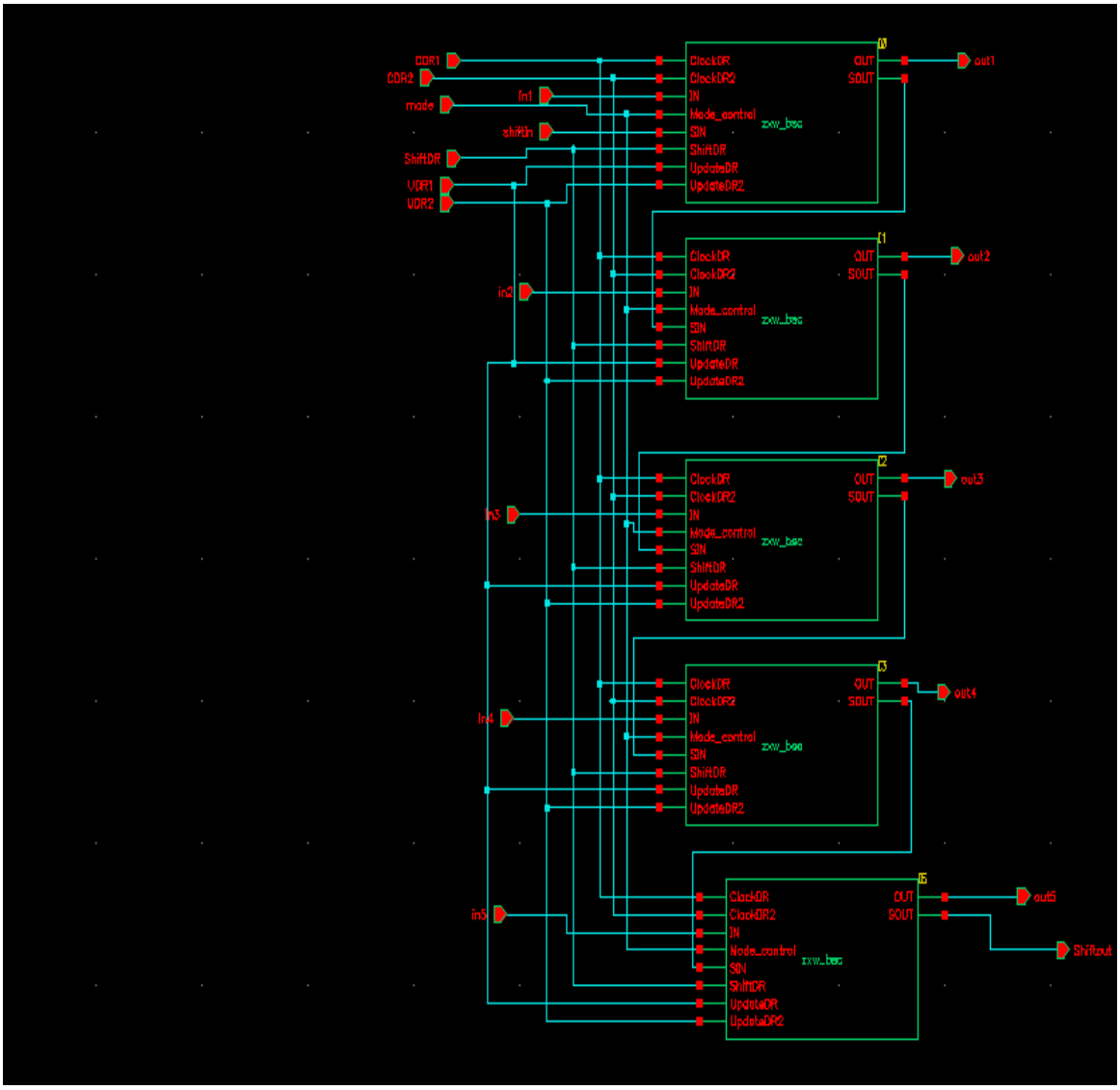

Sout
out
Mode_control
ClockDR
ClockDR2
UpdateDR
UpdateDR2

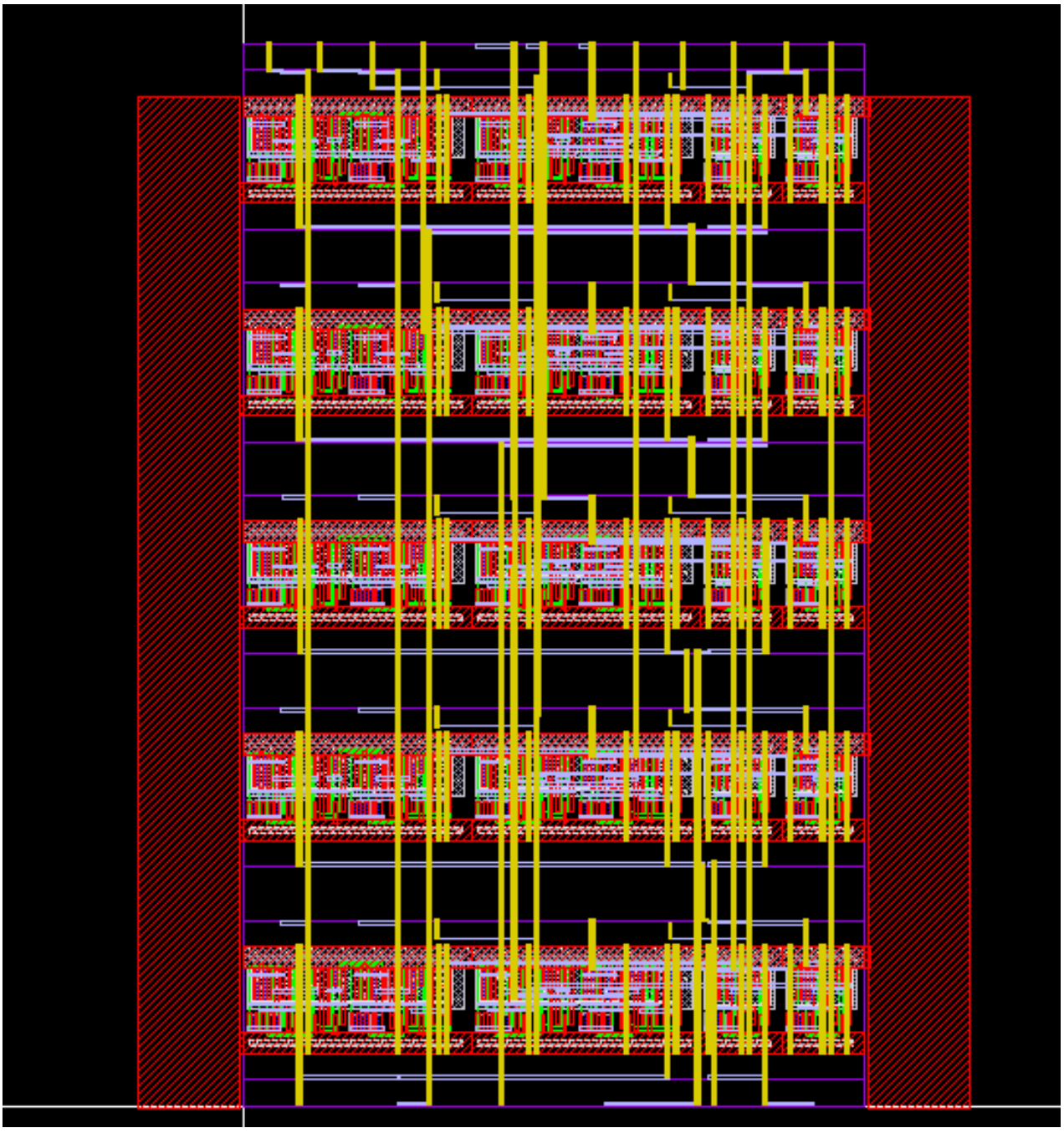


Layout 8534 um^2

BSR5

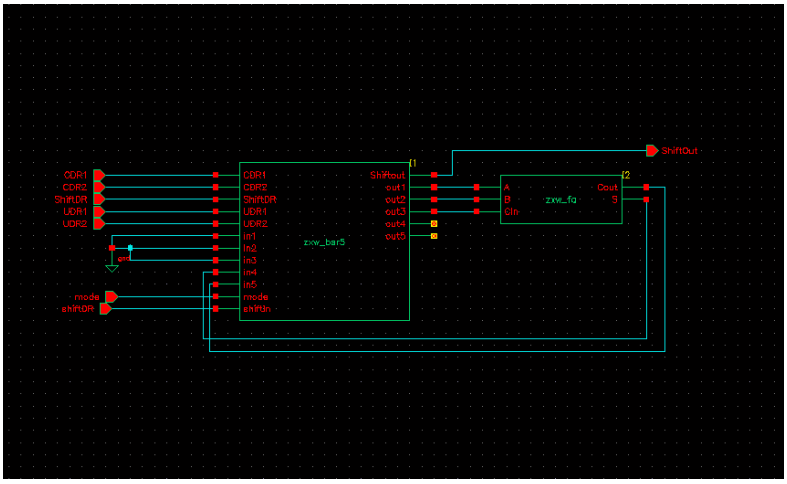

[@instanceName]
CDR1
CDR2
ShiftDR
UDR1
UDR2
in1
in2
in3
in4
in5
mode
shiftIn
[@partName]
Shiftout
out1
out2
out3
out4
out5

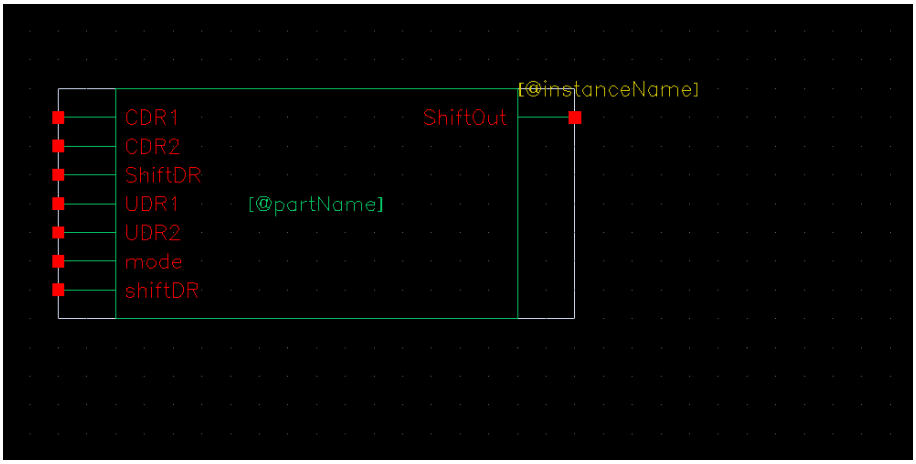

CDR1
CDR2
mode
in1
shiftin
ShiftDR
VDR1
VDR2
ClockDR
ClockDR2
IN
Mode_control
SIN
ShiftDR
UpdateDR
UpdateDR2
OUT
SOUT
zxw_bsc
I0
out1
I1
out2
in2
I2
out3
in3
I3
out4
in4
I5
out5
in5
Shiftout



Layout 76310.5 um^2

BSSUM





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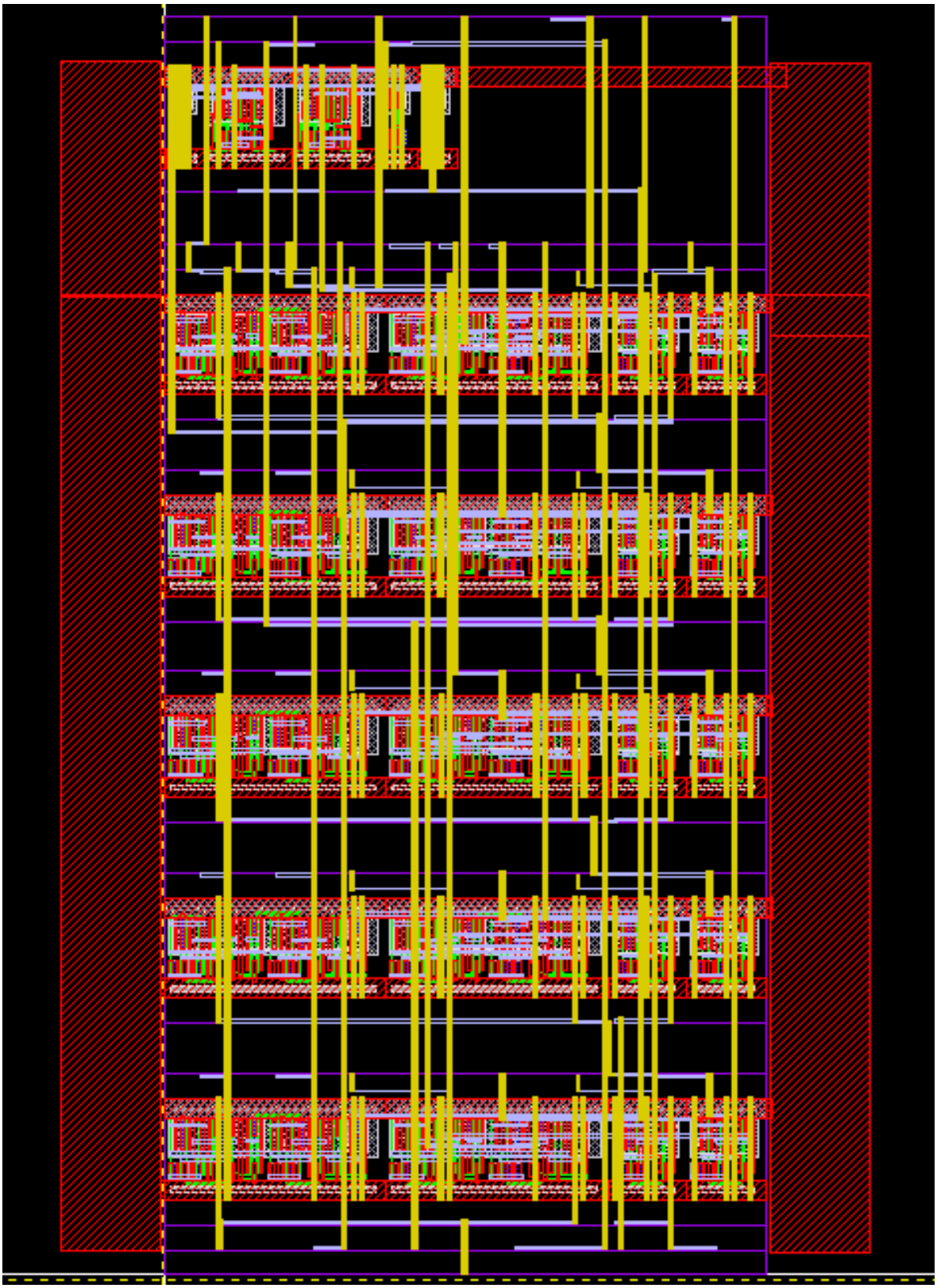
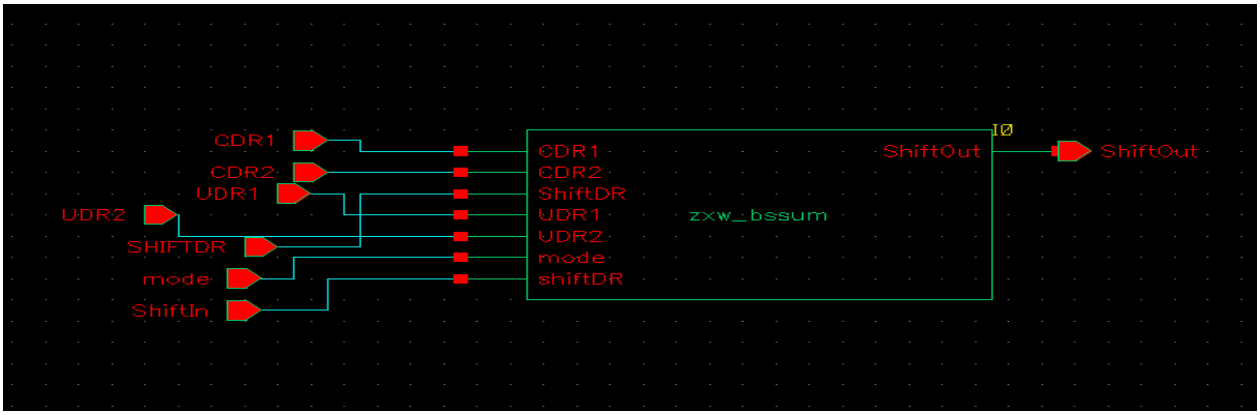


Layout 95639.6um^2

BSTEST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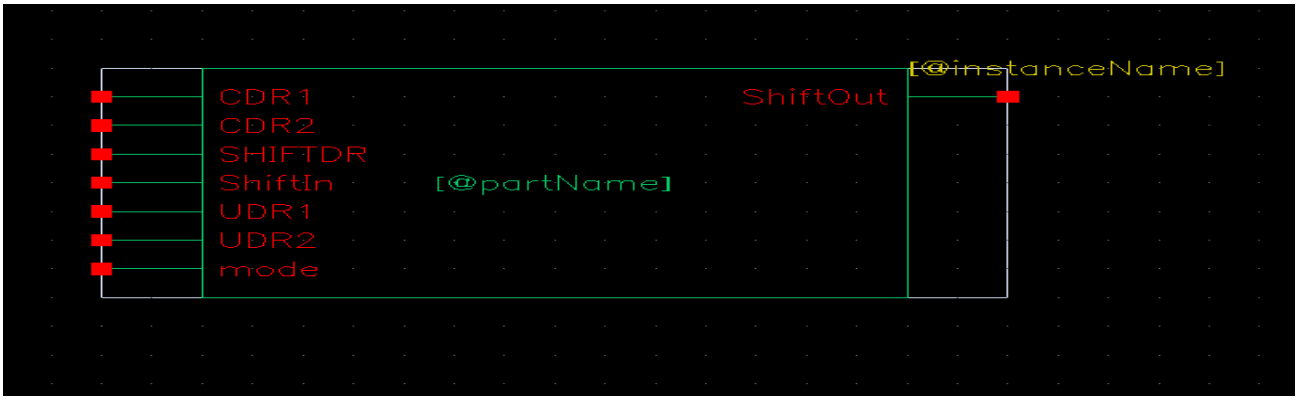
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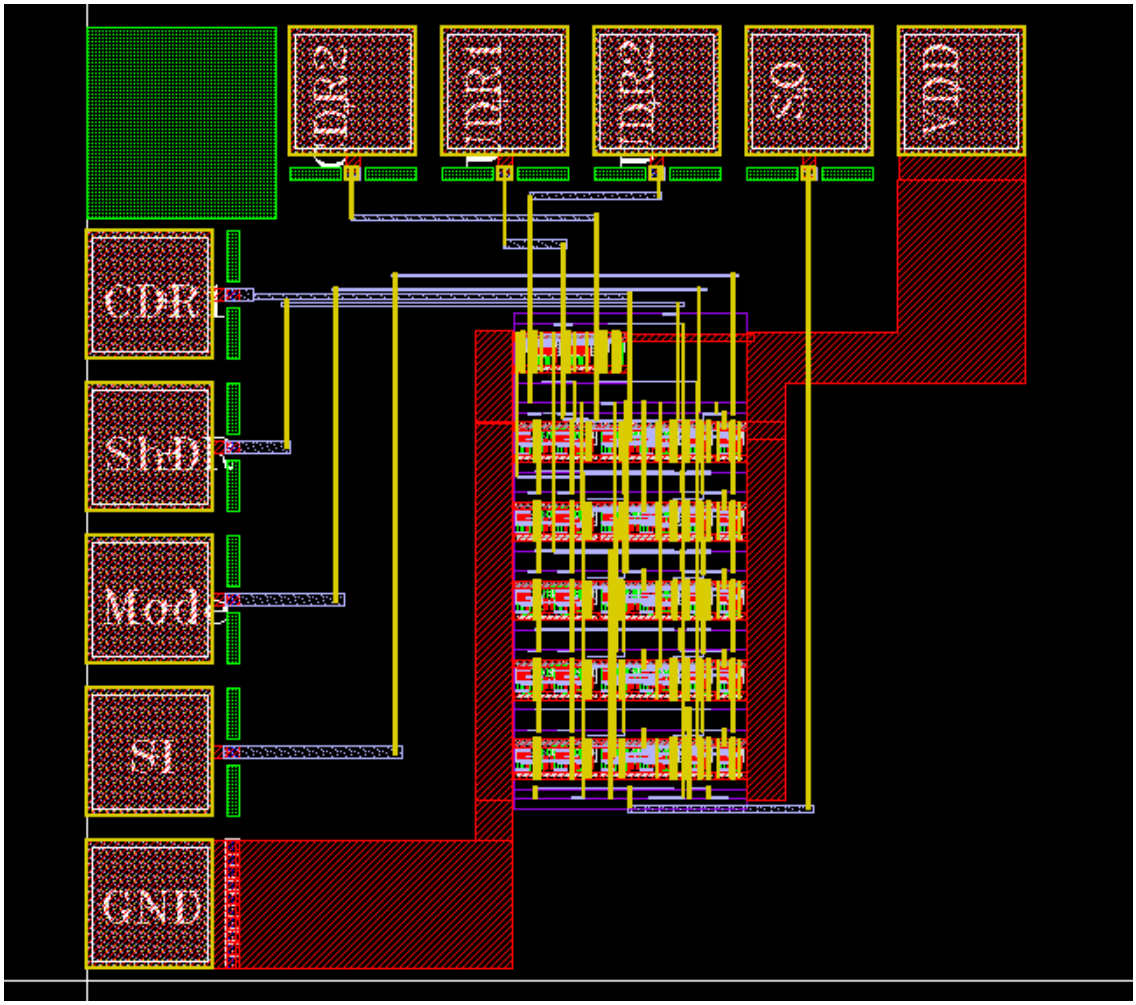

Layout 563475 um^2