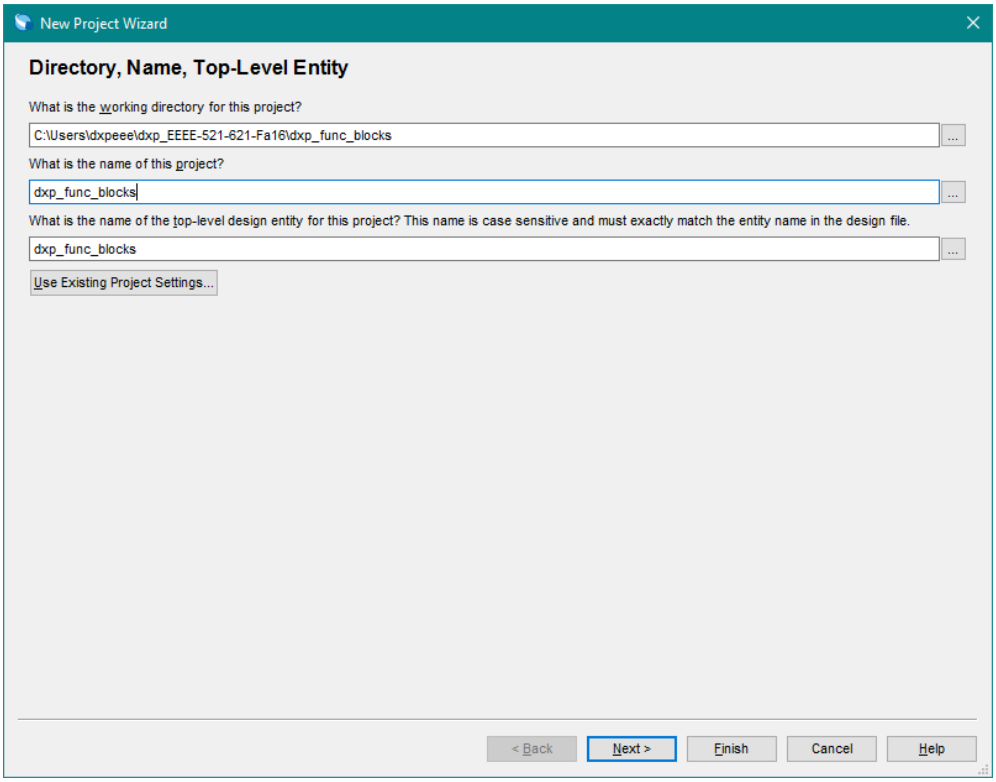
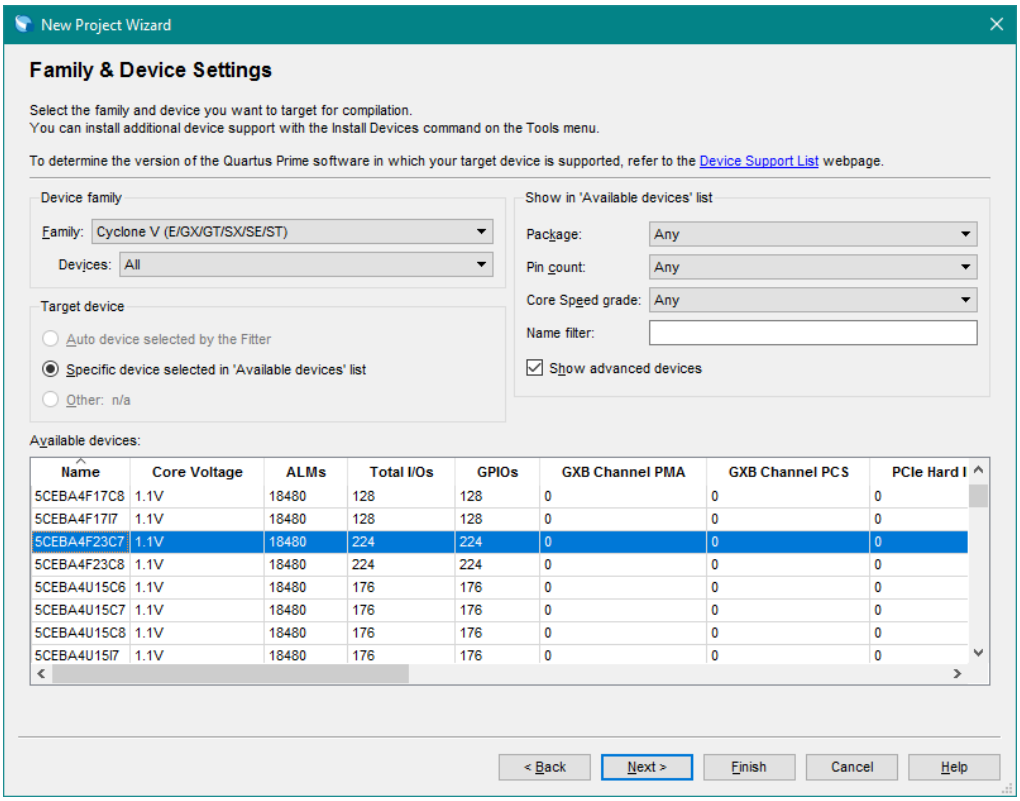
EEEE-521-621-Lab1

1) From mycourses download on your desktop this pdf file.
2) The goal of this lab is to create and instantiate functional blocks that you may use during the next labs. You will create these functional blocks using the "IP Catalog". Once created, these blocks can be instantiated in a higher level schematic, a vhdl design file, or a verilog design file.
3) Start by creating a new project in your working directory: fml_EEEE-521_Fa16 or fml_EEEE-621_Fa16. The **new directory and project names** are fml_func_blocks. In all screen captures, you'll see instead of fml my initials dxp. Click "File > New Project Wizard":

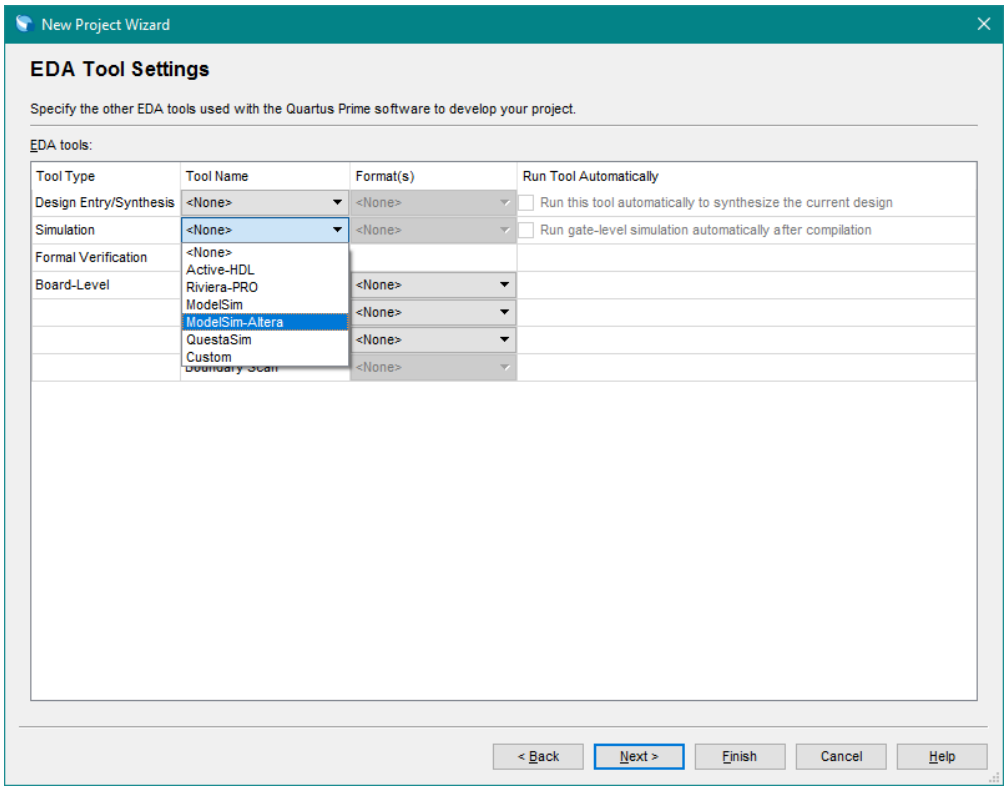


4) Click Next twice. In the 3rd step select the proper device (5CEBA4F23C7):

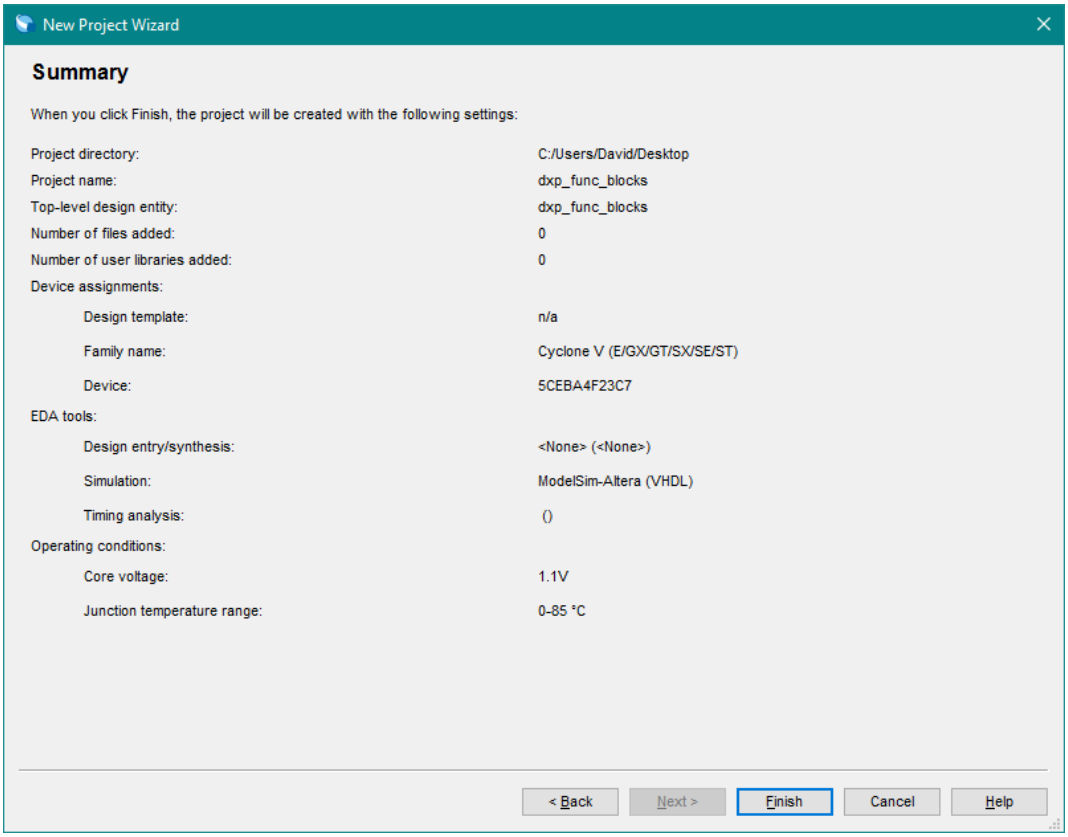


5) In step 4 of 5 choose to simulate the tool ModelSim-Altera. The next tab Format(s) will automatically be set to VHDL. This setting relates to the format of the testbench, which will

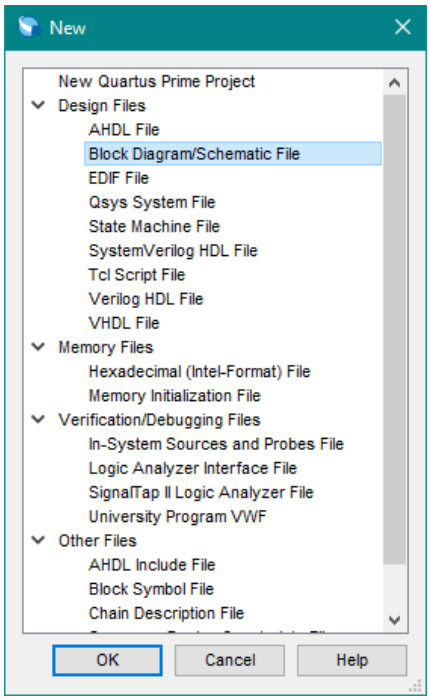
have to be in one of the HDL languages even if your design is captured entirely in schematic.



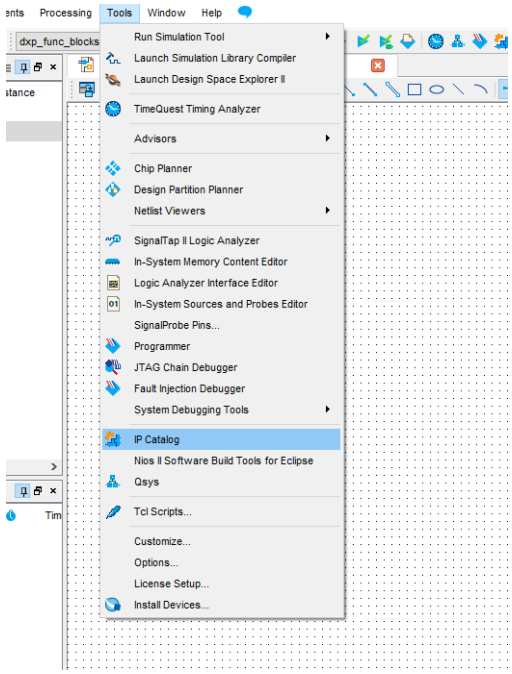
6) Click Next and after you check your Summary to match the one below, click Finish.



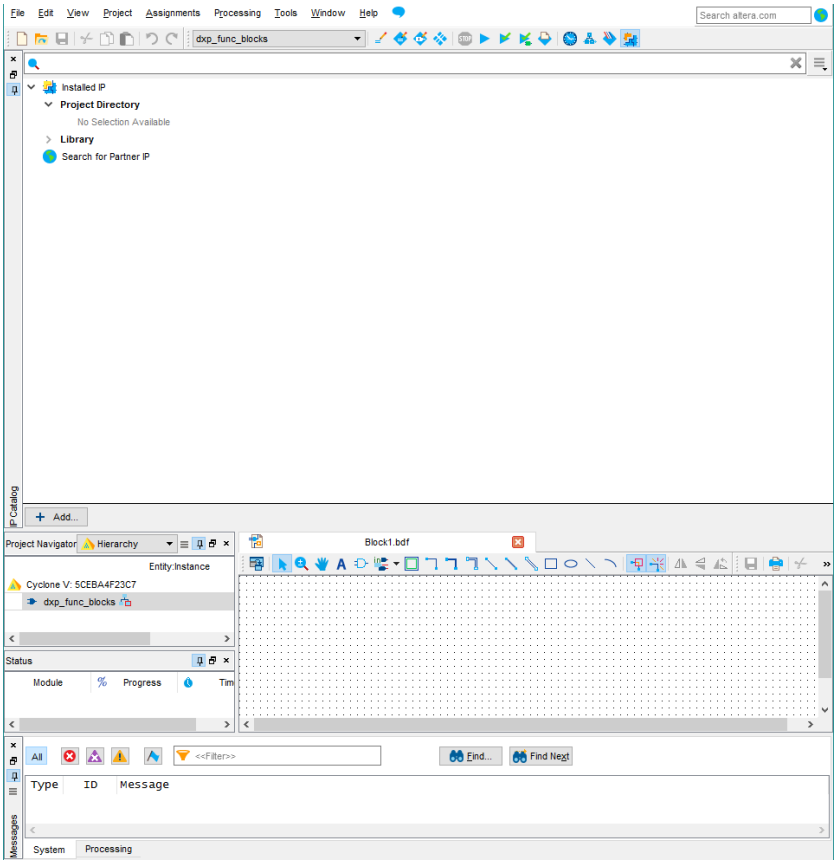
7) Next you create the top-level design file. Choose File > New and select block diagram / schematic file, even if you'll capture your designs later in a HDL.



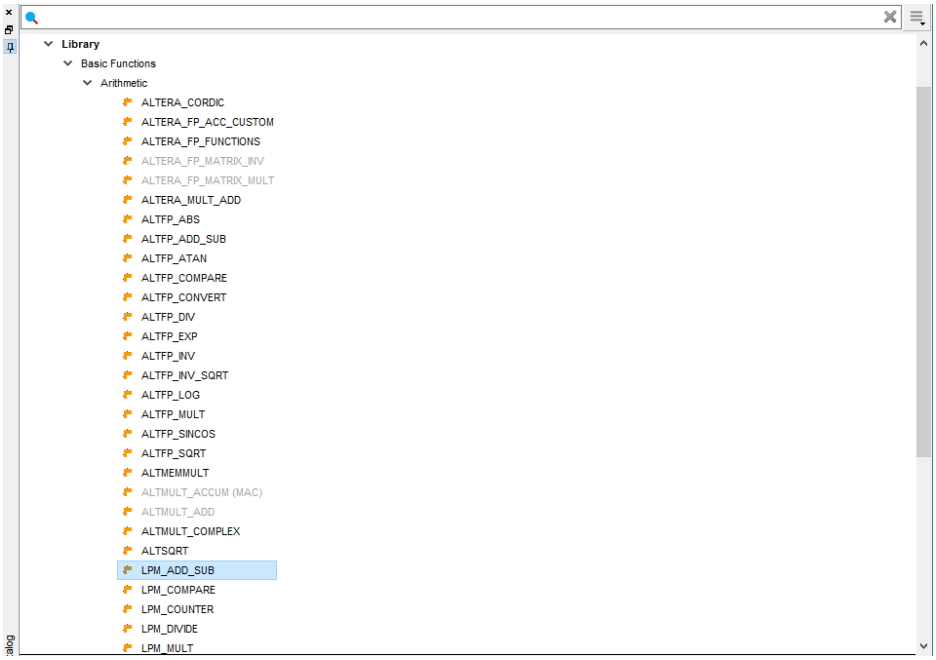
8) Before we can save the file, we need to at least add/instantiate a component.
9) The first component we will create is and add/subtract unit. Click on the "Tools" drop-down menu.



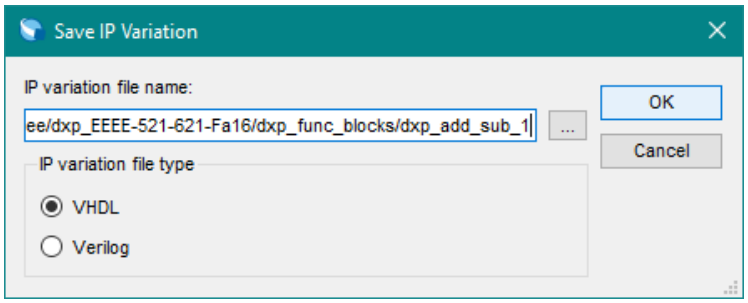
10) In the menu, click on the "IP Catalog". Another window pops up. Expand the library menu.



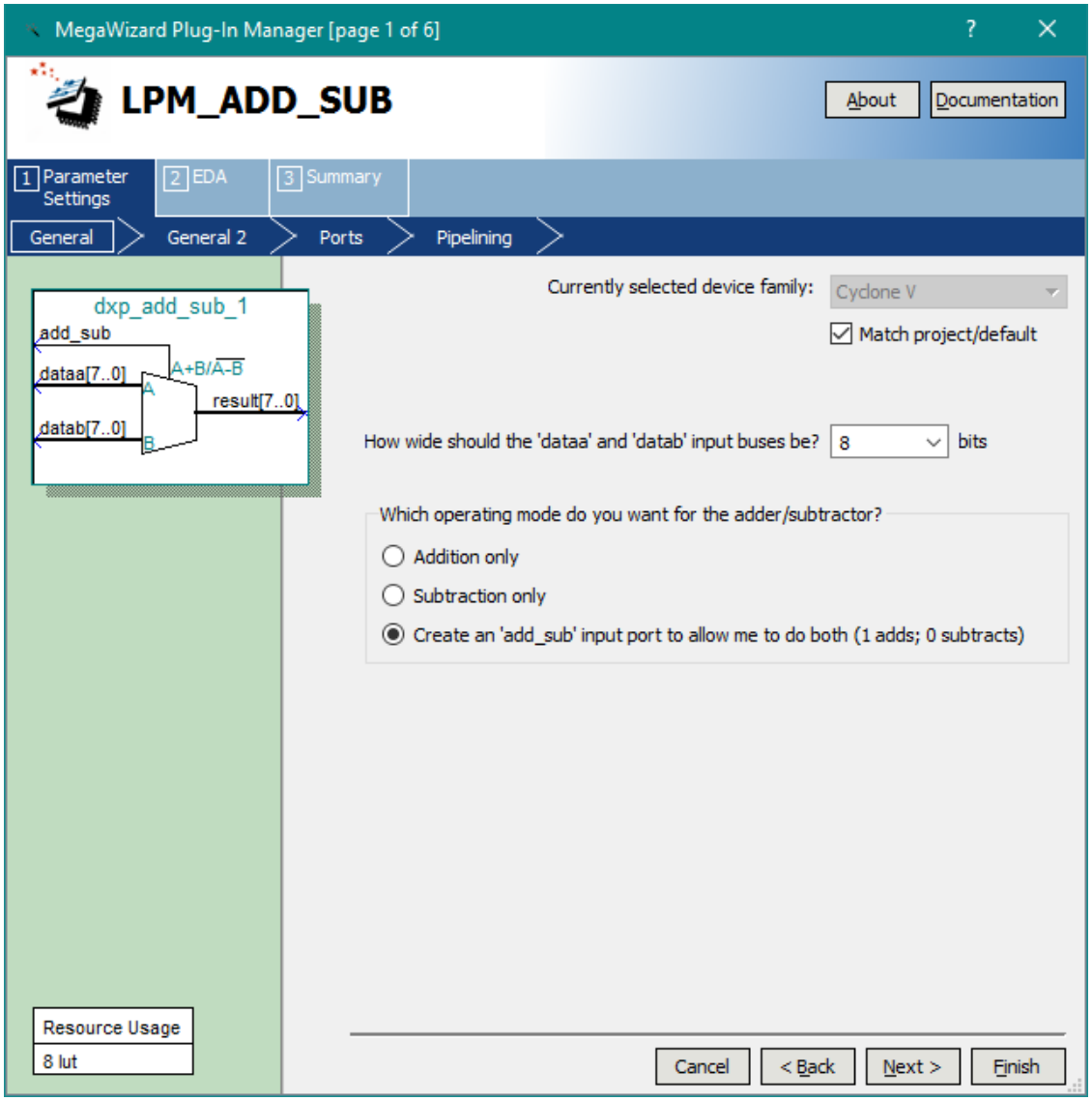
11) Select "LPM_ADD_SUB" under "Library → Basic Functions → Arithmetic". Double click, and a small window pops up.



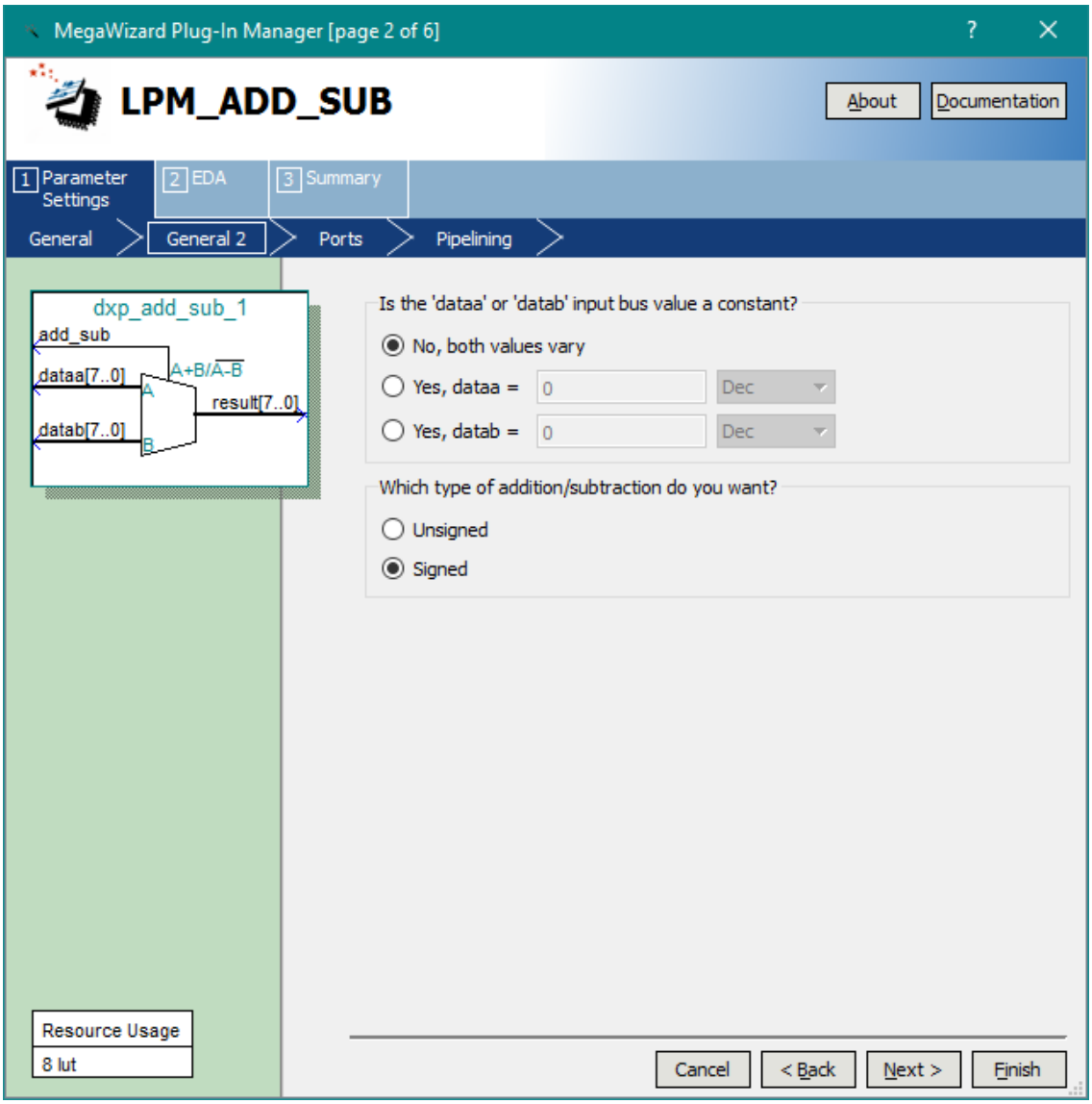
12) Select the HDL language in which the component will be created. You need to choose one even if you choose to use schematic only for design capture. Before clicking next, give the component the name fml_add_sub_1.



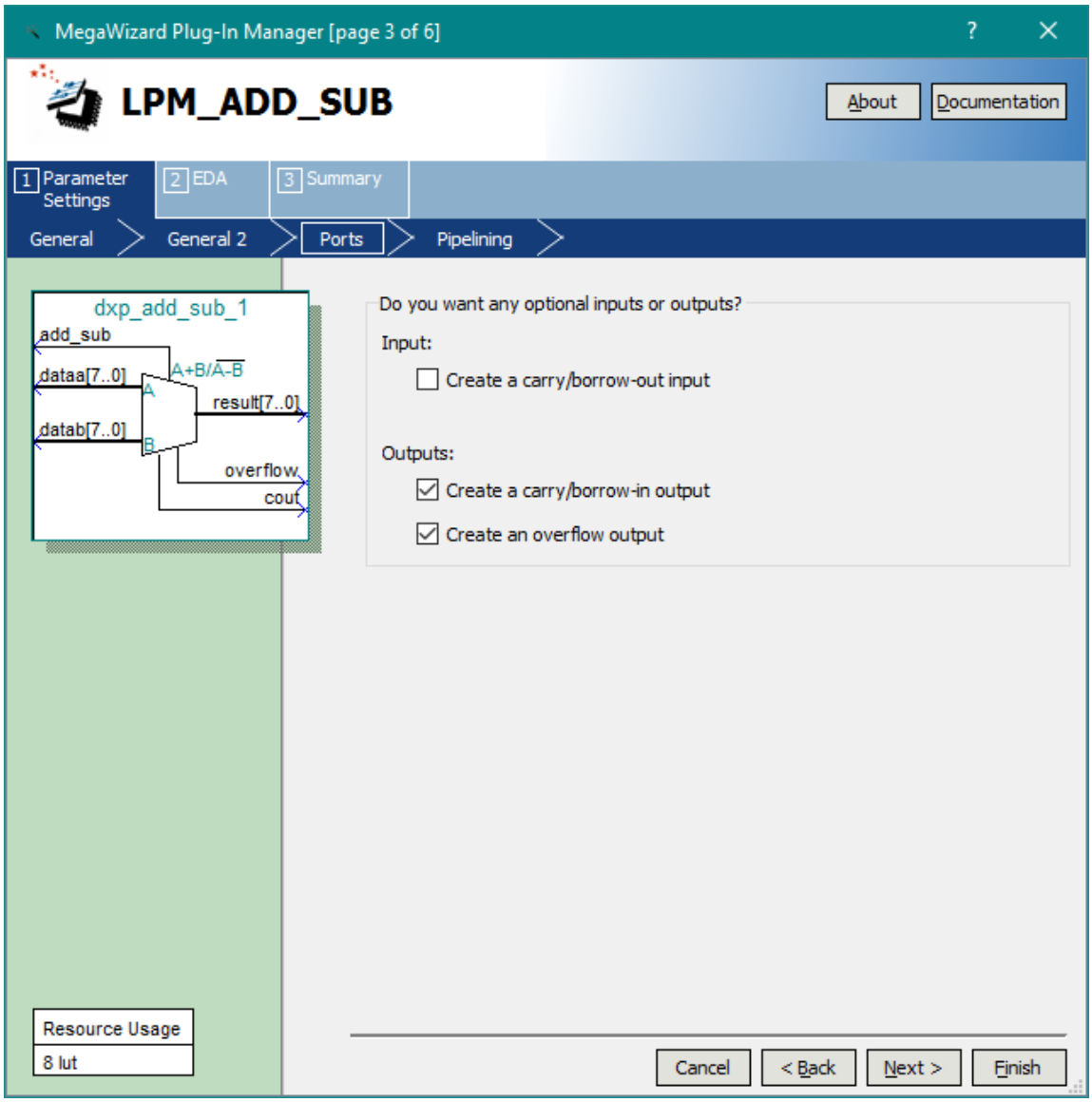
13) In the next window choose to create an add_sub input and keep the default 8-bit bus width.



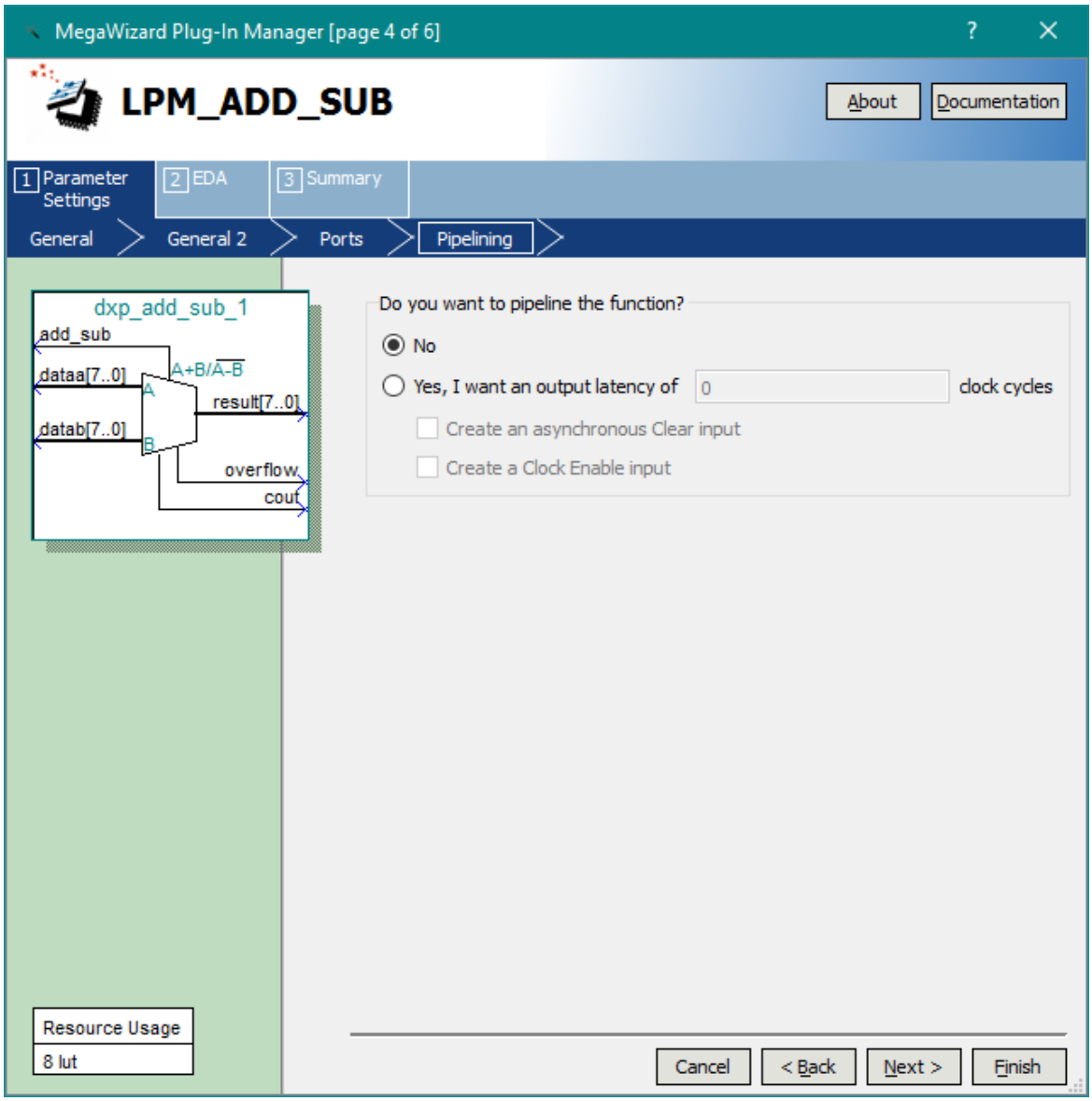
14) In the next window both values vary and the operands are signed.



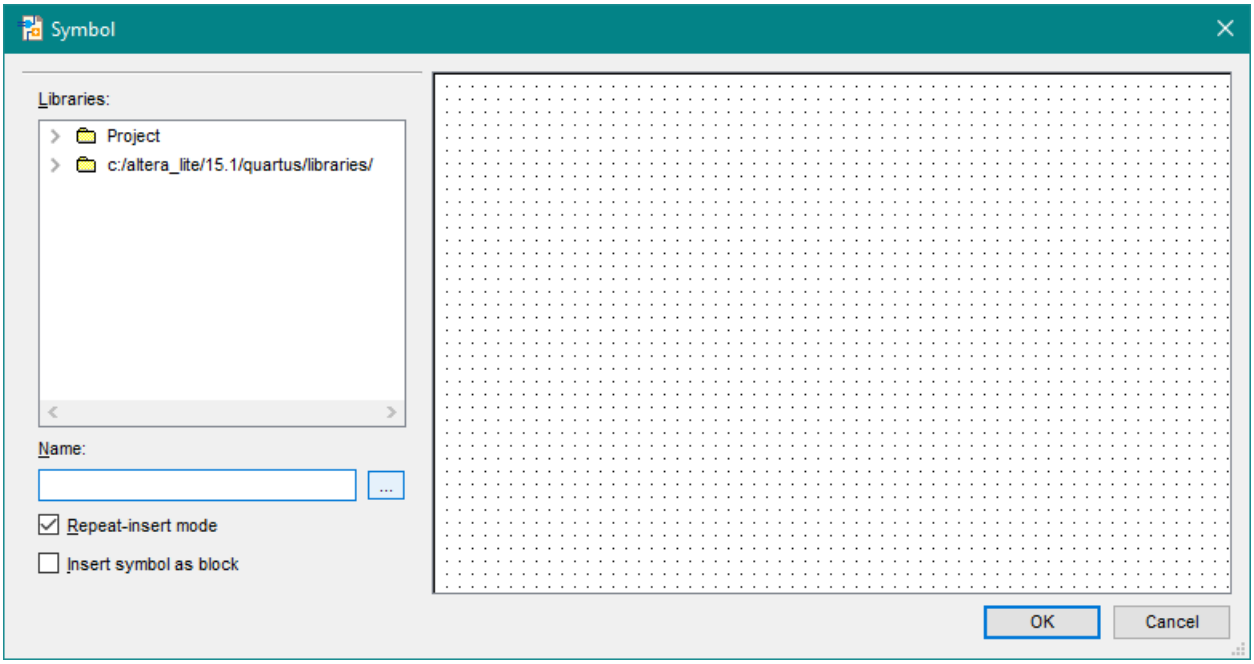
15) In the next window choose to create a carry and overflow outputs.

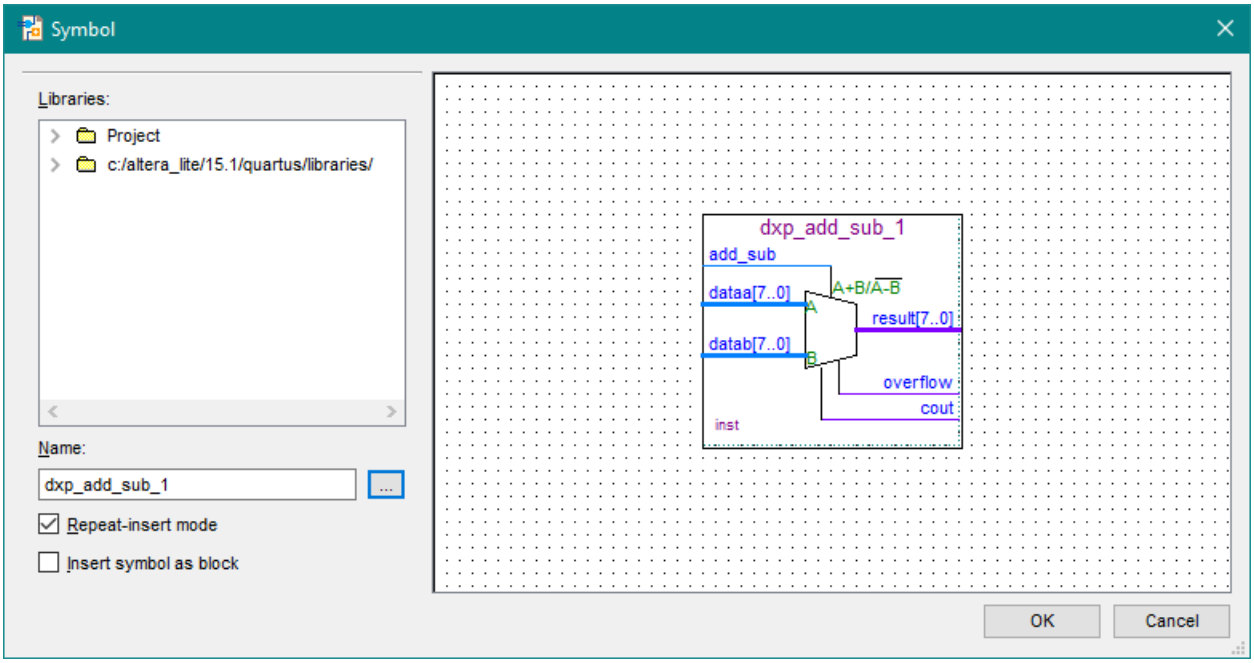


16) For now, in the next window keep the default choice of not pipelining the function.

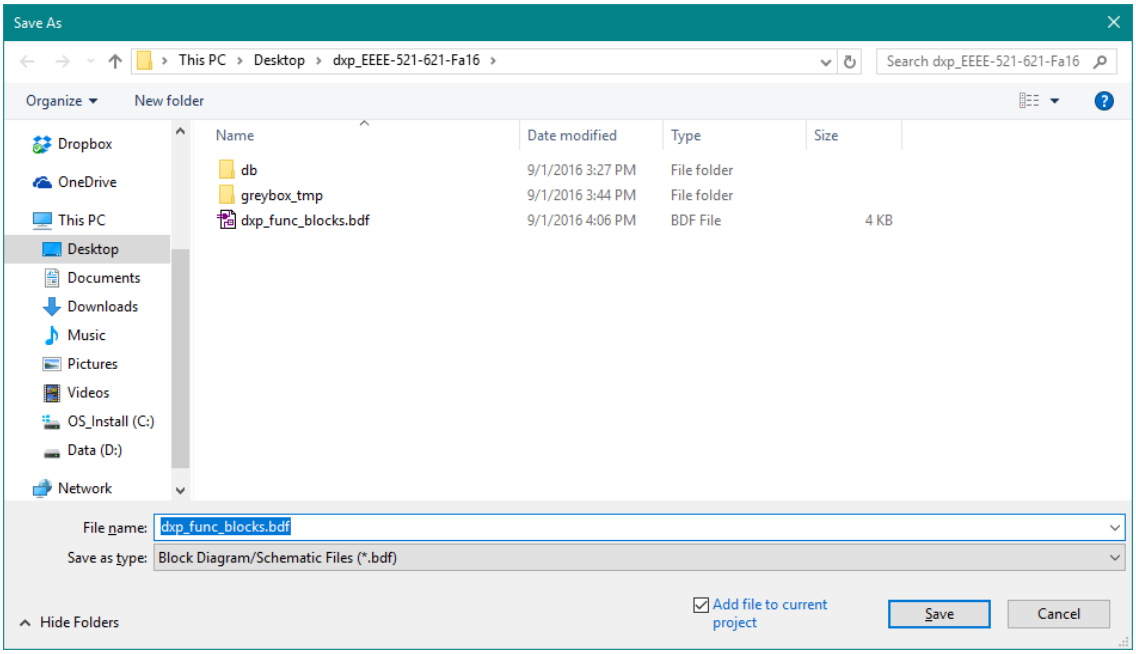


17) Click next twice. Check the box next to fml_add_sub_1.bsf ("Quartus Prime symbol file"). Click Finish. The component is now available for instantiation. Click on the symbol icon again, and the following menu will pop up. Click on the "…" button, navigate to your root project directory, and select the created ".bsf" file.

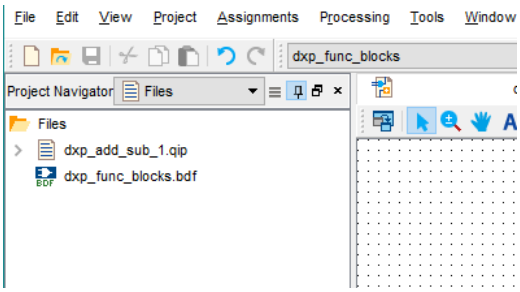




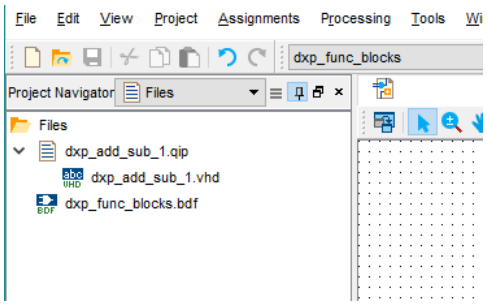
18) Click OK and place the component somewhere in the schematic. Now click Save and keep the default suggested name. This file is now set as the top-level entity.



19) In the Project Navigator window click on the Files tab.



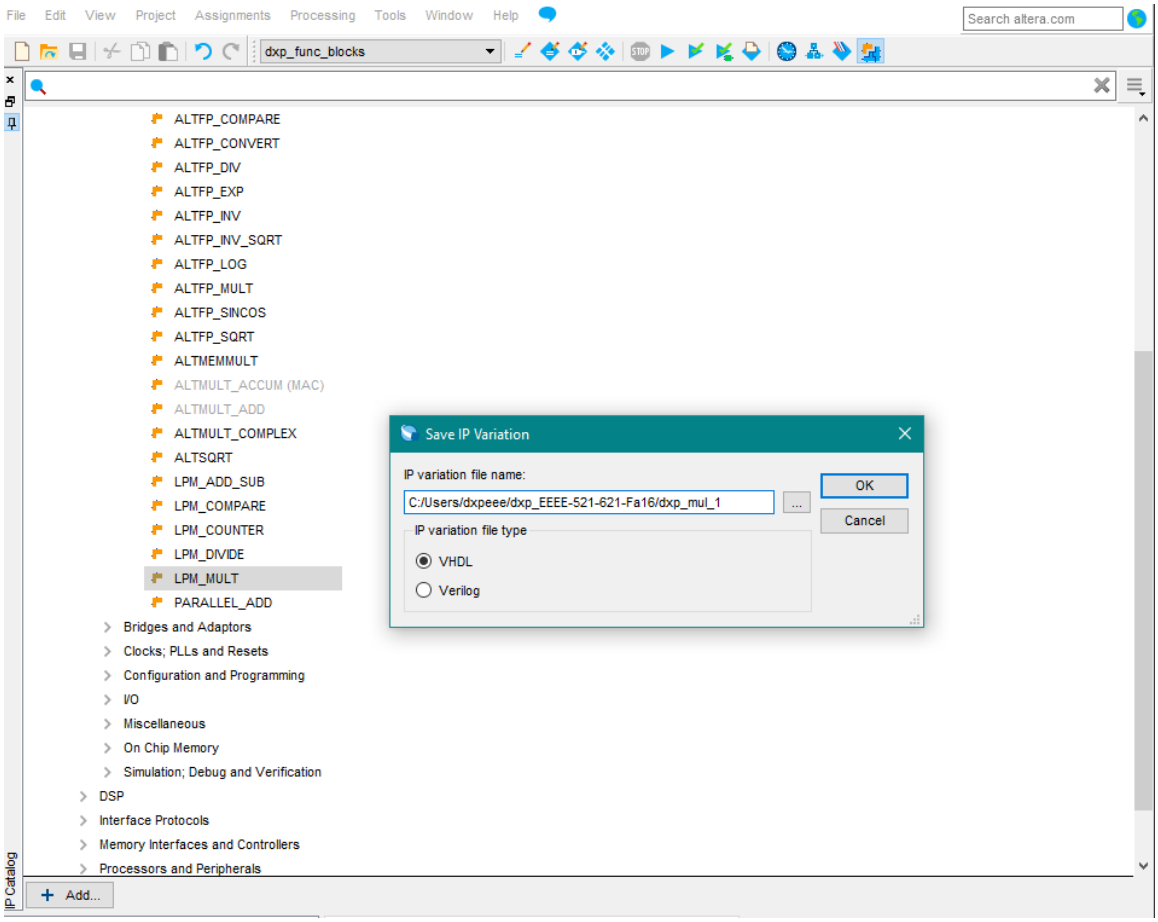
20) Now, expand the fml_add_sub_1.qip.

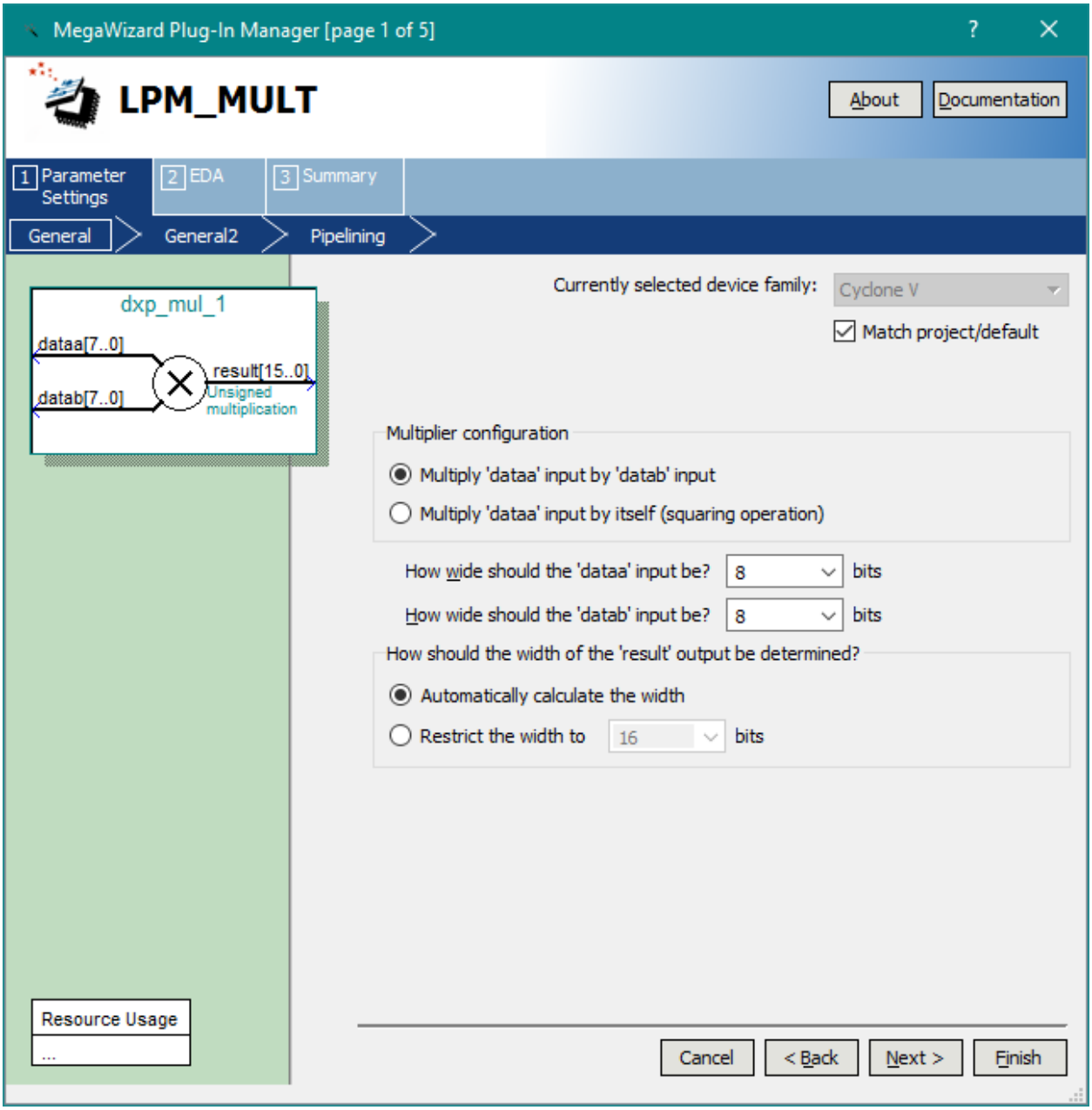


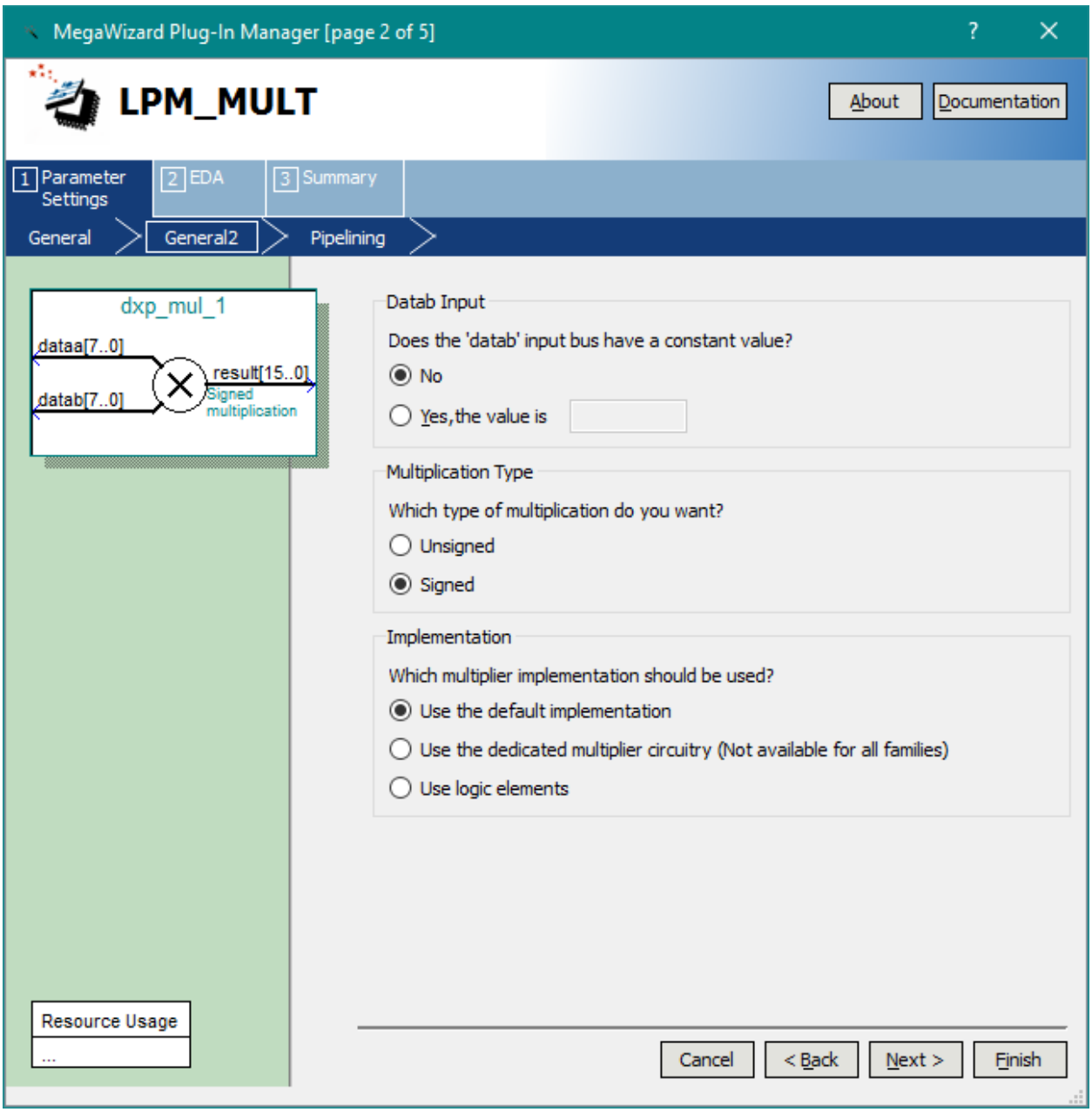
21) If you will use this component in schematic only, you simply call and instantiate it using its symbol, as you have done already. If you will use/call this component from a higher hierarchical level using VHDL or Verilog, you'll need to copy/paste and add the *.vhd or *.v file to that project. **Add only the *.vhd or *.v and NOT the *.qip!**

22) In this lab you will continue to create and add other functional blocks to this schematic. No wiring or verification through simulation will be performed. In the following steps only relevant intermediate windows are shown. All instantiated components will be shown at the end.

23) The next component is a multiplier.




MegaWizard Plug-In Manager [page 1 of 5]
LPM_MULT
About
Documentation
1 Parameter Settings
2 EDA
3 Summary
General
General2
Pipelining
dxp_mul_1
dataa[7..0]
datab[7..0]
result[15..0]
Unsigned multiplication
Currently selected device family:
Cyclone V
Match project/default
Multiplier configuration
Multiply 'dataa' input by 'datab' input
Multiply 'dataa' input by itself (squaring operation)
How wide should the 'dataa' input be?
8
bits
How wide should the 'datab' input be?
8
bits
How should the width of the 'result' output be determined?
Automatically calculate the width
Restrict the width to
16
bits
Resource Usage
...
Cancel
< Back
Next >
Finish


MegaWizard Plug-In Manager [page 2 of 5]
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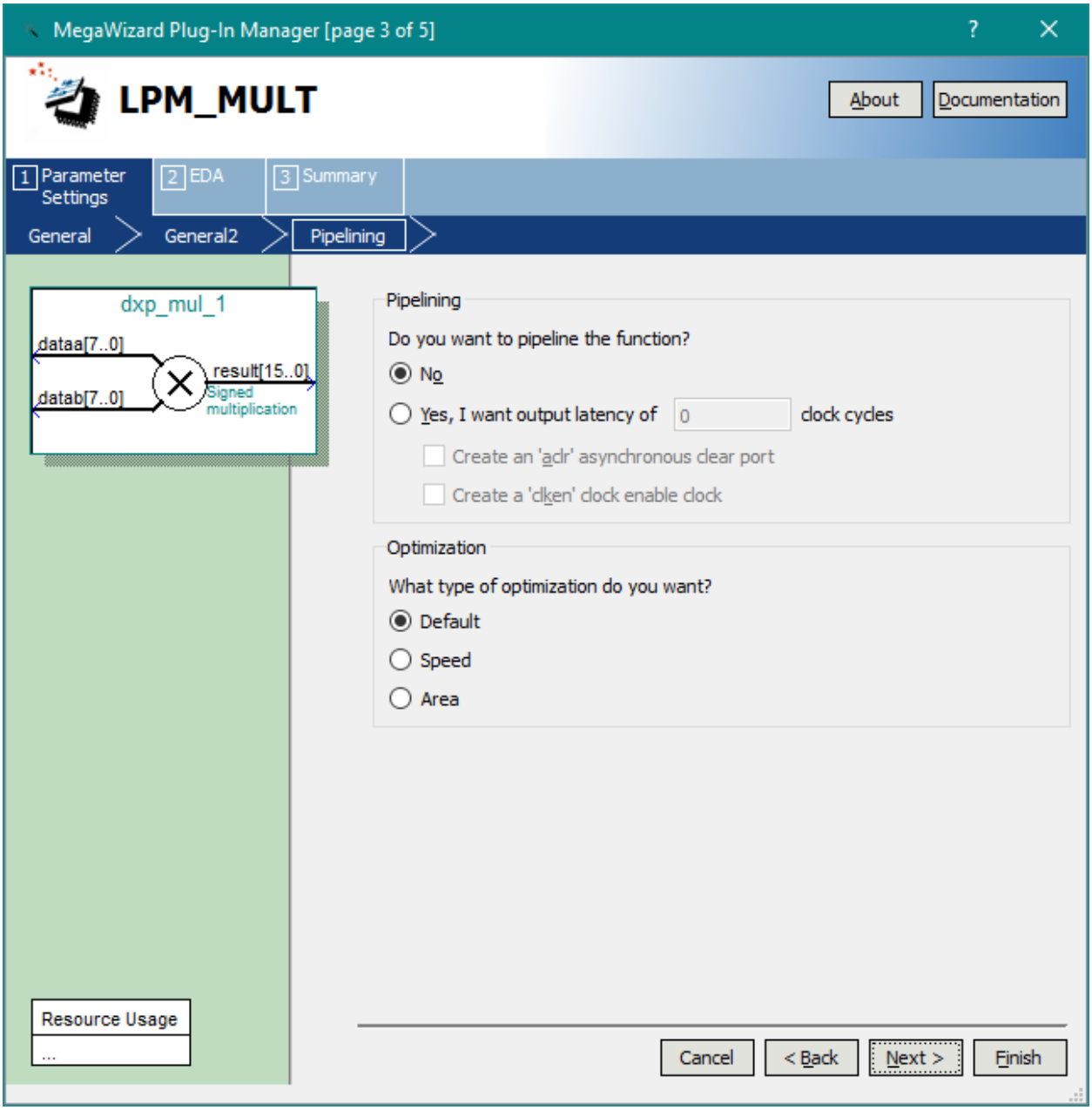
Pipelining
dxp_mul_1
dataa[7..0]
datab[7..0]
result[15..0]
Signed multiplication
Datab Input
Does the 'datab' input bus have a constant value?
No
Yes, the value is
Multiplication Type
Which type of multiplication do you want?
Unsigned
Signed
Implementation
Which multiplier implementation should be used?
Use the default implementation
Use the dedicated multiplier circuitry (Not available for all families)
Use logic elements
Resource Usage
...
Cancel
< Back
Next >
Finish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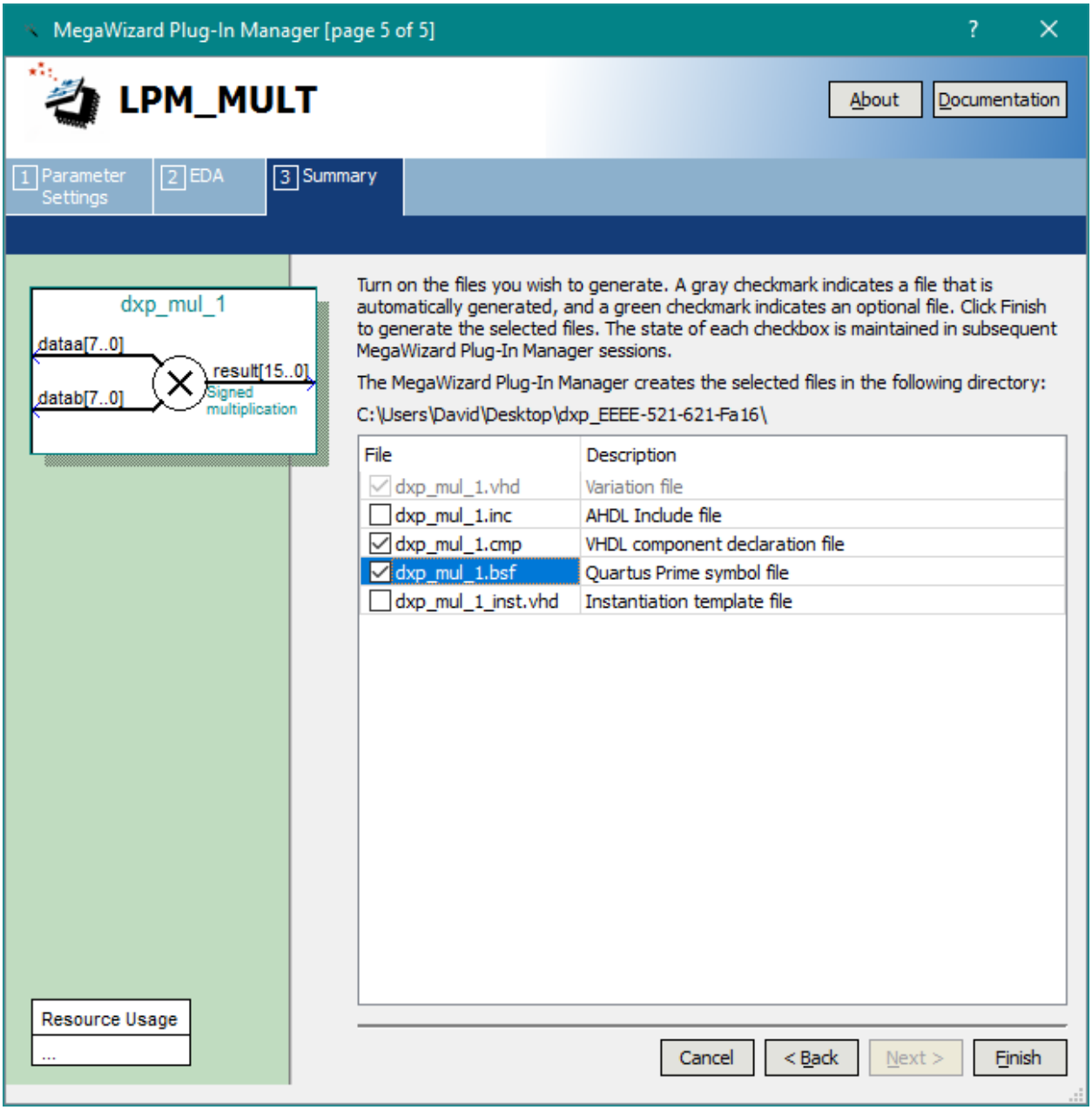
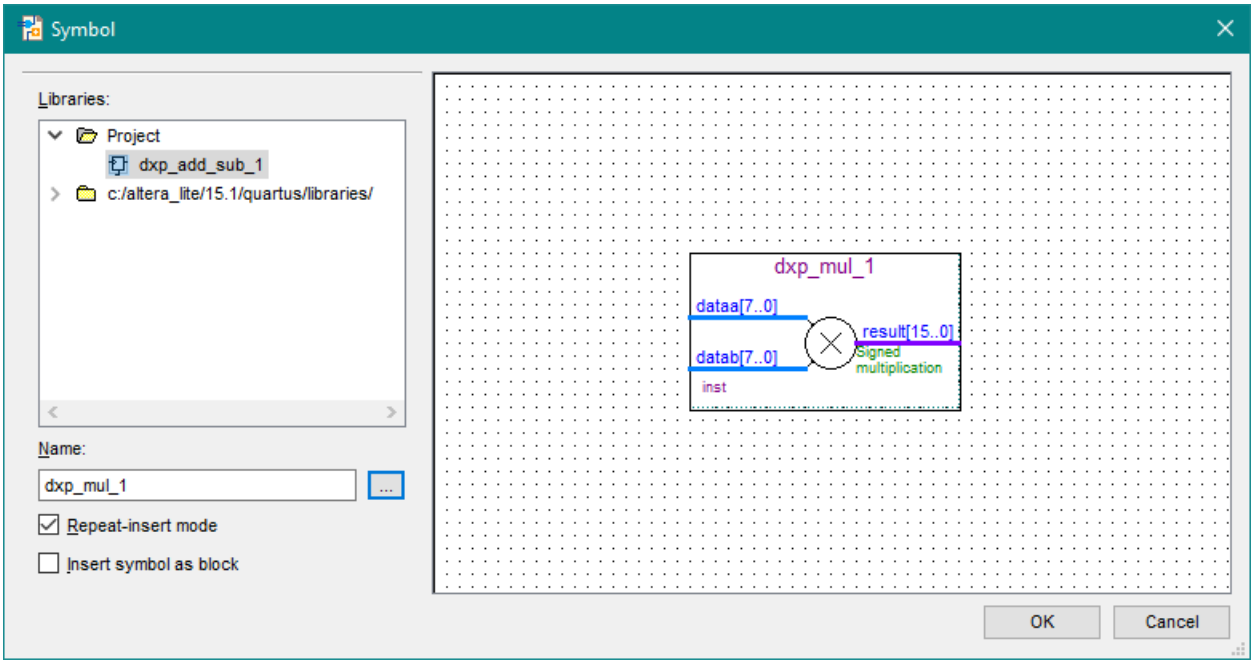
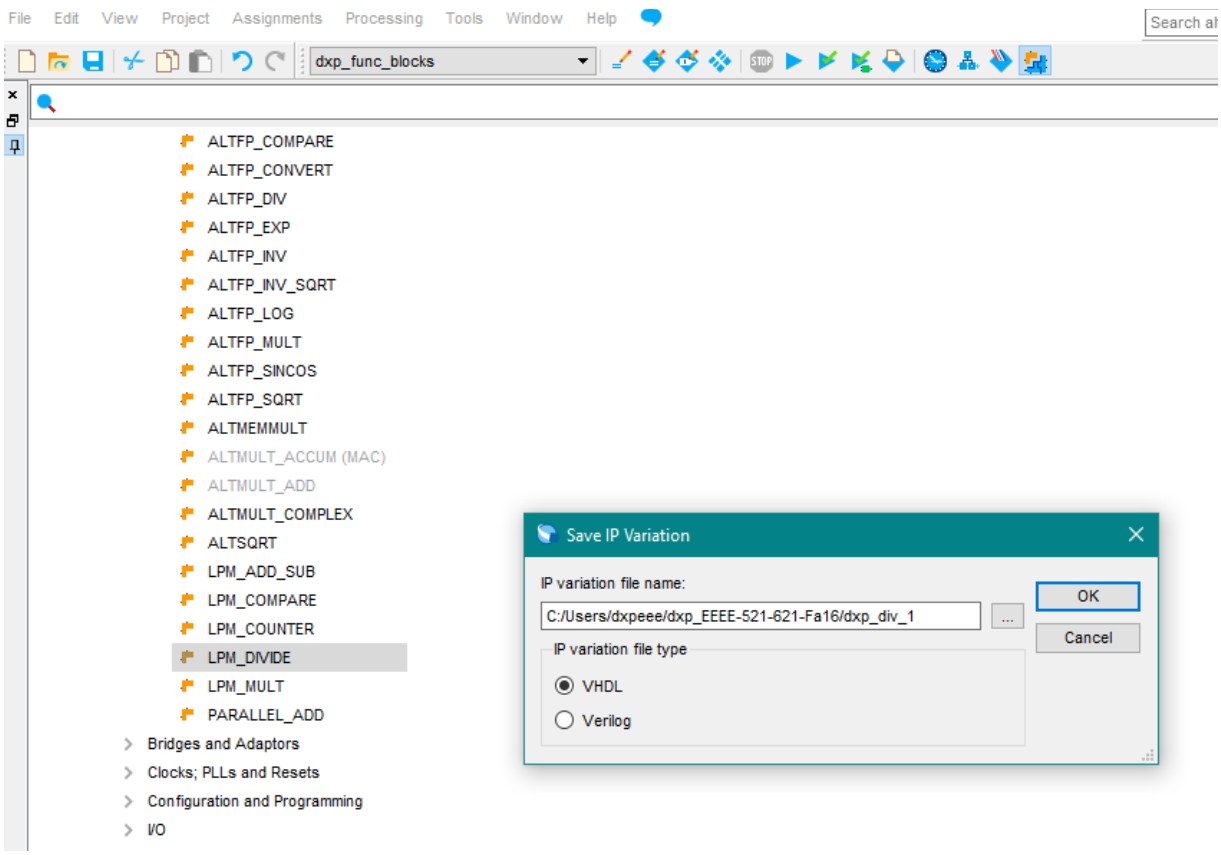
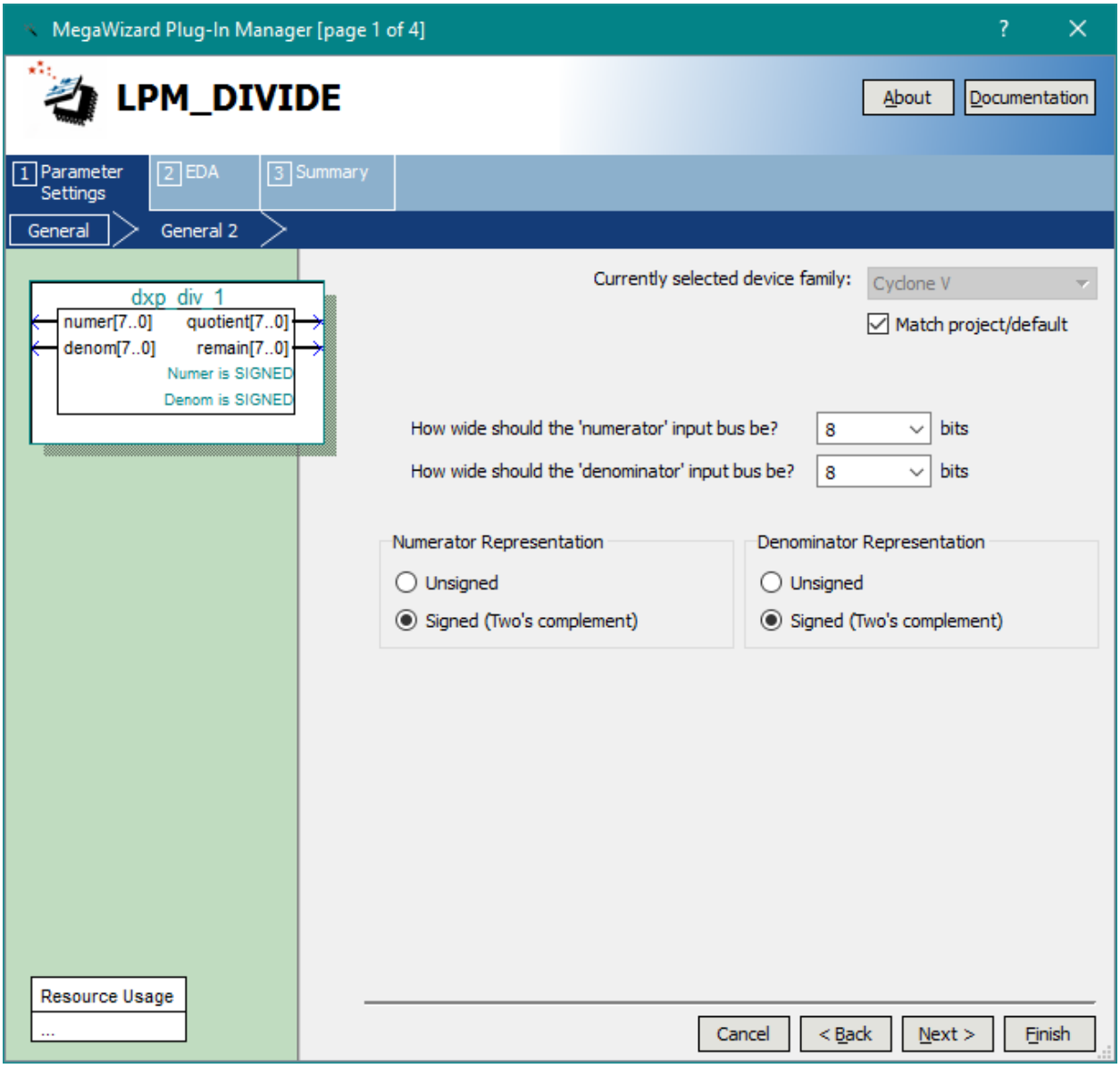
General2
Pipelining
dxp_mul_1
dataa[7..0]
datab[7..0]
result[15..0]
Signed multiplication
Pipelining
Do you want to pipeline the function?
No
Yes, I want output latency of
0
clock cycles
Create an 'aclr' asynchronous clear port
Create a 'clken' clock enable clock
Optimization
What type of optimization do you want?
Default
Speed
Area
Resource Usage
...
Cancel
< Back
Next >
Finish


MegaWizard Plug-In Manager [page 5 of 5]
LPM_MULT
About
Documentation
1 Parameter Settings
2 EDA
3 Summary
dxp_mul_1
dataa[7..0]
datab[7..0]
result[15..0]
Signed multiplication
Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.
The MegaWizard Plug-In Manager creates the selected files in the following directory:
C:\Users\David\Desktop\dxp_EEEE-521-621-Fa16\
File
Description
dxp_mul_1.vhd
Variation file
dxp_mul_1.inc
AHDL Include file
dxp_mul_1.cmp
VHDL component declaration file
dxp_mul_1.bsf
Quartus Prime symbol file
dxp_mul_1_inst.vhd
Instantiation template file
Resource Usage
...
Cancel
< Back
Next >
Finish



24) The third component is a divider.




MegaWizard Plug-In Manager [page 1 of 4]
LPM_DIVIDE
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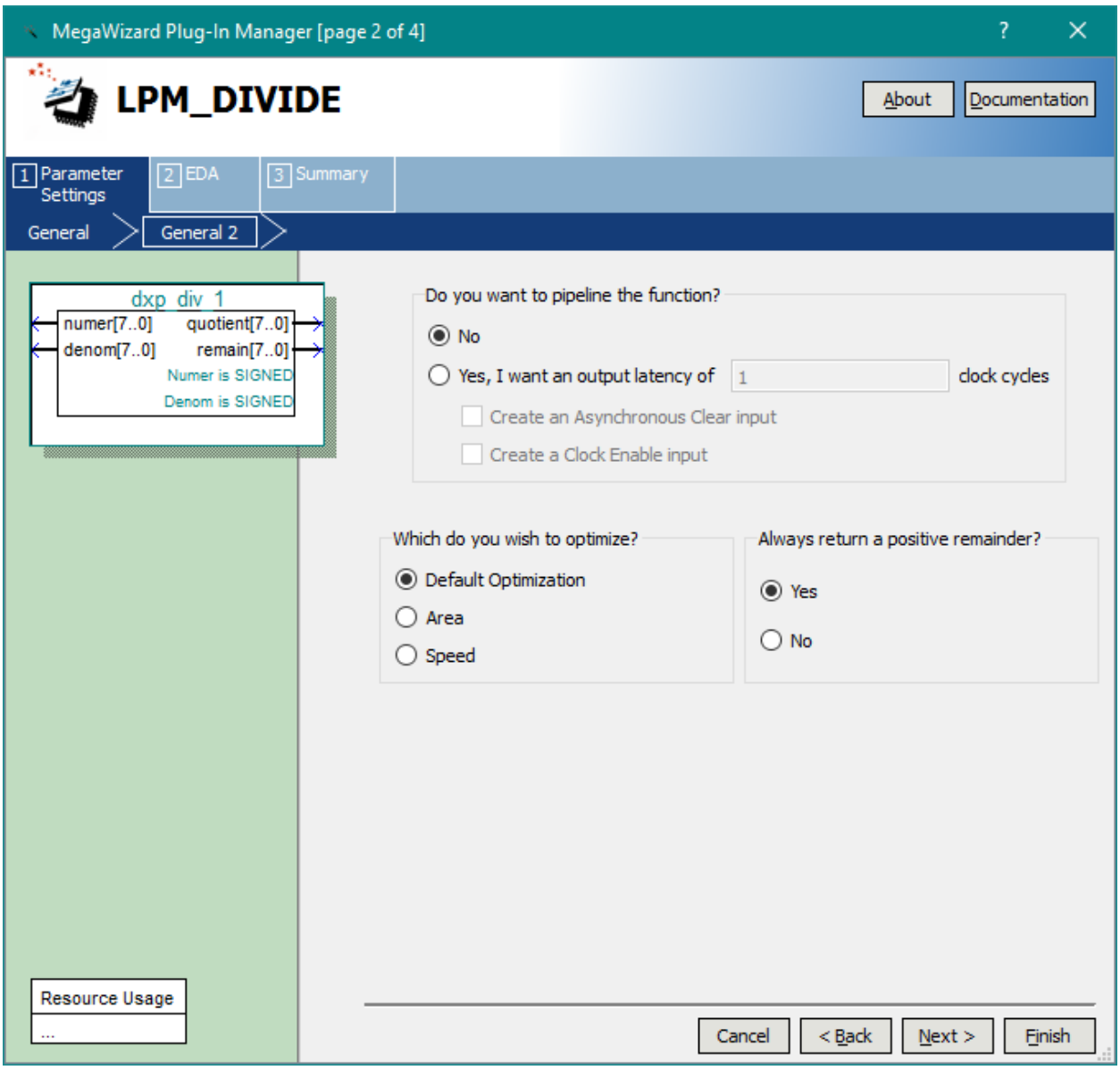
General
General 2
dxp_div_1
numer[7..0]
denom[7..0]
quotient[7..0]
remain[7..0]
Numer is SIGNED
Denom is SIGNED
Currently selected device family:
Cyclone V
Match project/default
How wide should the 'numerator' input bus be?
8
bits
How wide should the 'denominator' input bus be?
8
bits
Numerator Representation
Unsigned
Signed (Two's complement)
Denominator Representation
Unsigned
Signed (Two's complement)
Resource Usage
...
Cancel
< Back
Next >
Finish


MegaWizard Plug-In Manager [page 2 of 4]
LPM_DIVIDE
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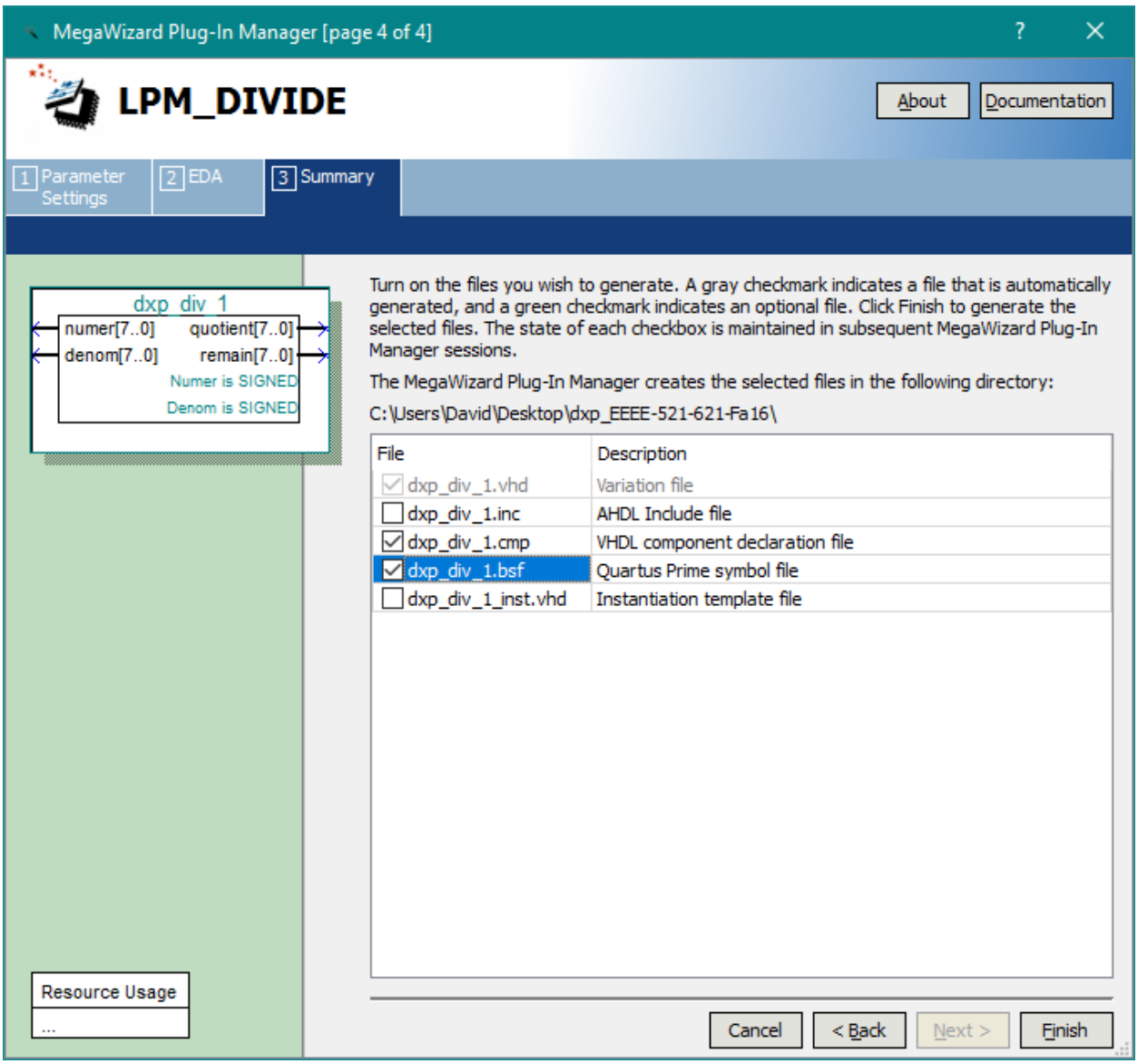
General
General 2
dxp_div_1
numer[7..0]
denom[7..0]
quotient[7..0]
remain[7..0]
Numer is SIGNED
Denom is SIGNED
Do you want to pipeline the function?
No
Yes, I want an output latency of
1
clock cycles
Create an Asynchronous Clear input
Create a Clock Enable input
Which do you wish to optimize?
Default Optimization
Area
Speed
Always return a positive remainder?
Yes
No
Resource Usage
...
Cancel
< Back
Next >
Finish


MegaWizard Plug-In Manager [page 4 of 4]
LPM_DIVIDE
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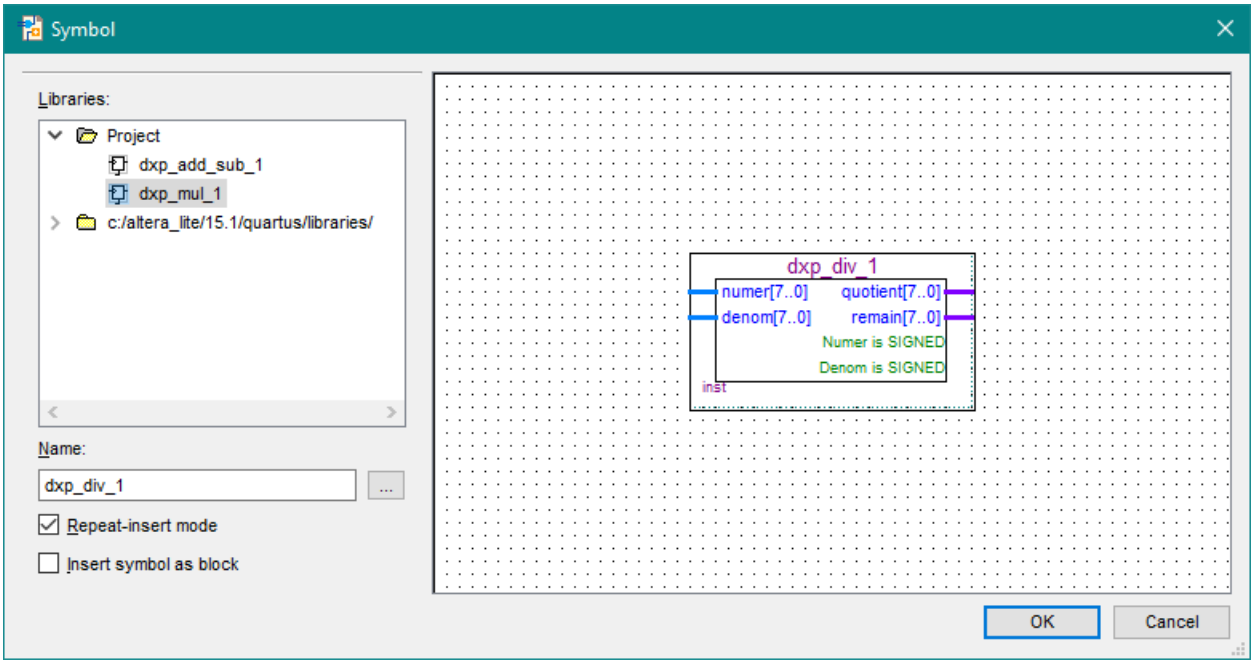
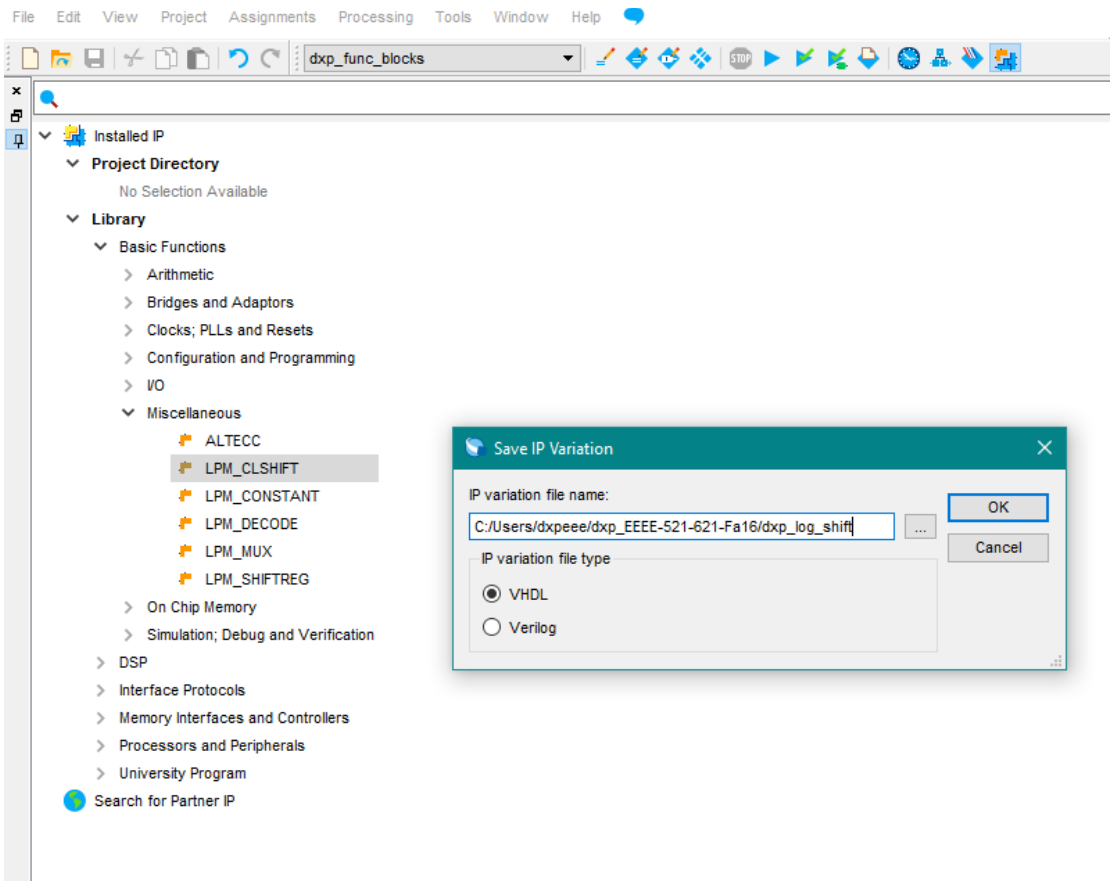
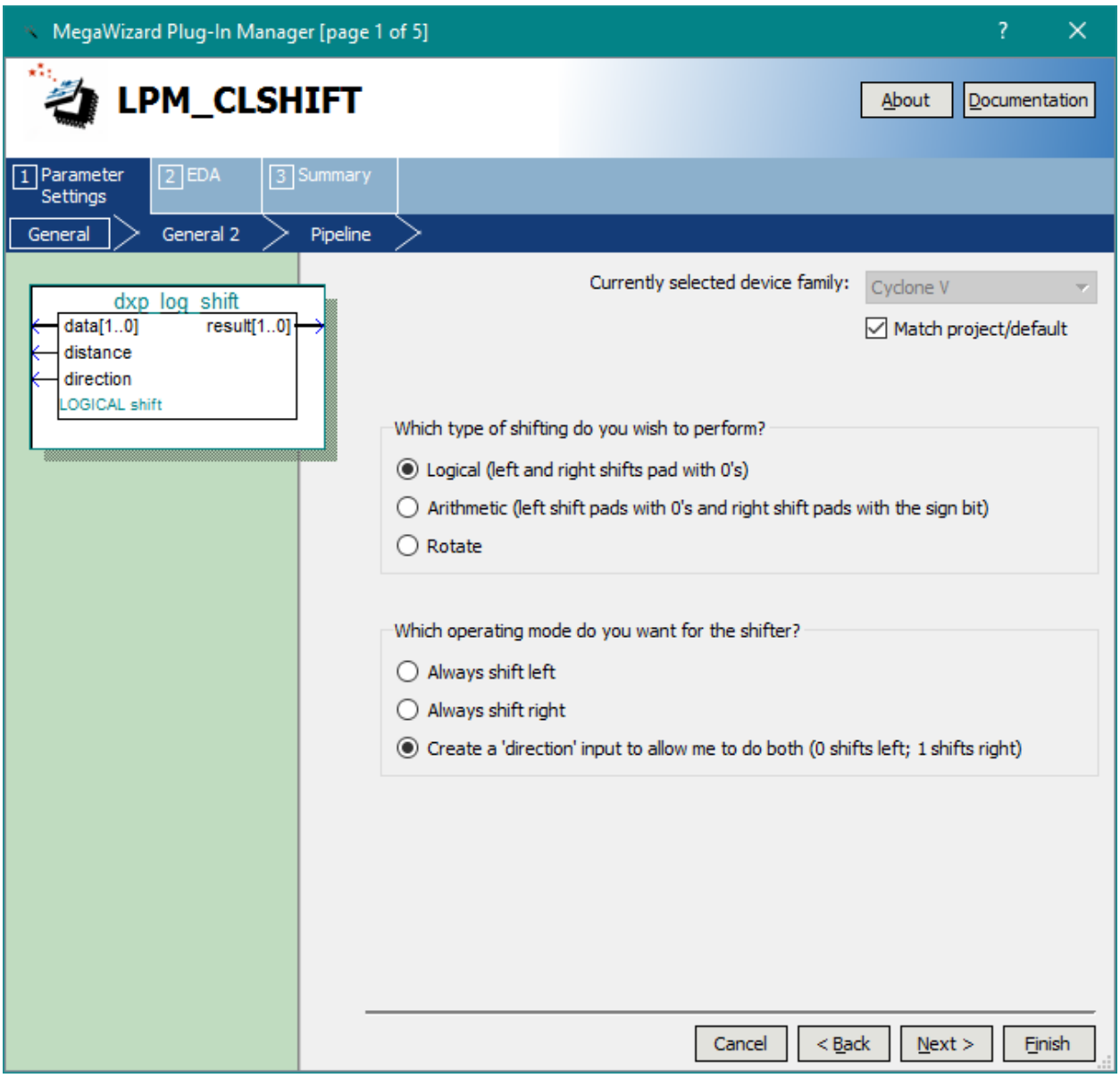
dxp_div_1
numer[7..0]
denom[7..0]
quotient[7..0]
remain[7..0]
Numer is SIGNED
Denom is SIGNED
Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.
The MegaWizard Plug-In Manager creates the selected files in the following directory:
C:\Users\David\Desktop\dxp_EEEE-521-621-Fa16\
File
Description
dxp_div_1.vhd
Variation file
dxp_div_1.inc
AHDL Include file
dxp_div_1.cmp
VHDL component declaration file
dxp_div_1.bsf
Quartus Prime symbol file
dxp_div_1_inst.vhd
Instantiation template file
Resource Usage
...
Cancel
< Back
Next >
Finish



25) The fourth component is a logical shifter. Find this under "Library → Basic Functions → Miscellaneous".




MegaWizard Plug-In Manager [page 1 of 5]
LPM_CLSHIFT
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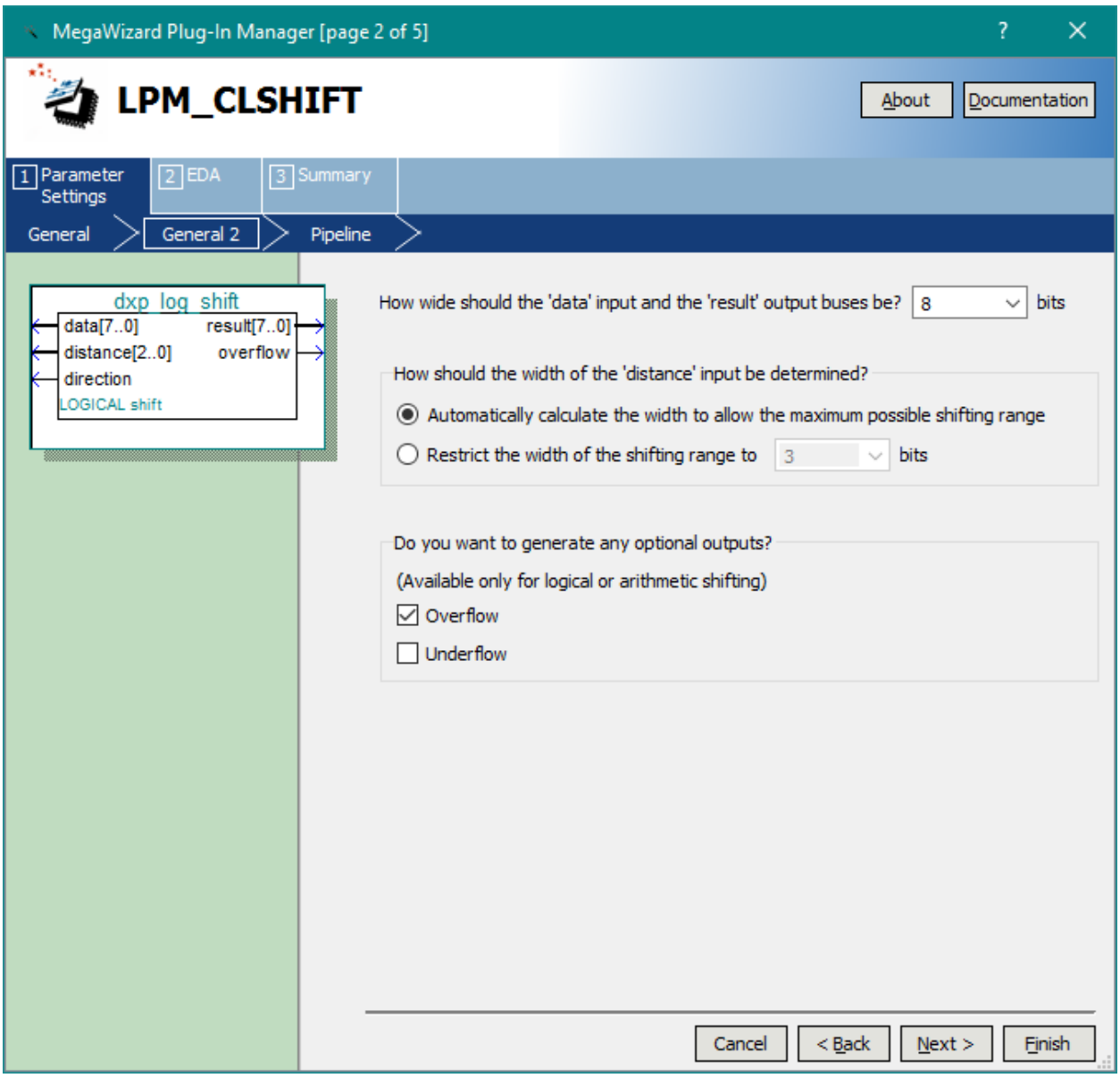
General
General 2
Pipeline
dxp_log_shift
data[1..0]
result[1..0]
distance
direction
LOGICAL shift
Currently selected device family:
Cyclone V
Match project/default
Which type of shifting do you wish to perform?
Logical (left and right shifts pad with 0's)
Arithmetic (left shift pads with 0's and right shift pads with the sign bit)
Rotate
Which operating mode do you want for the shifter?
Always shift left
Always shift right
Create a 'direction' input to allow me to do both (0 shifts left; 1 shifts right)
Cancel
< Back
Next >
Finish


MegaWizard Plug-In Manager [page 2 of 5]
LPM_CLSHIFT
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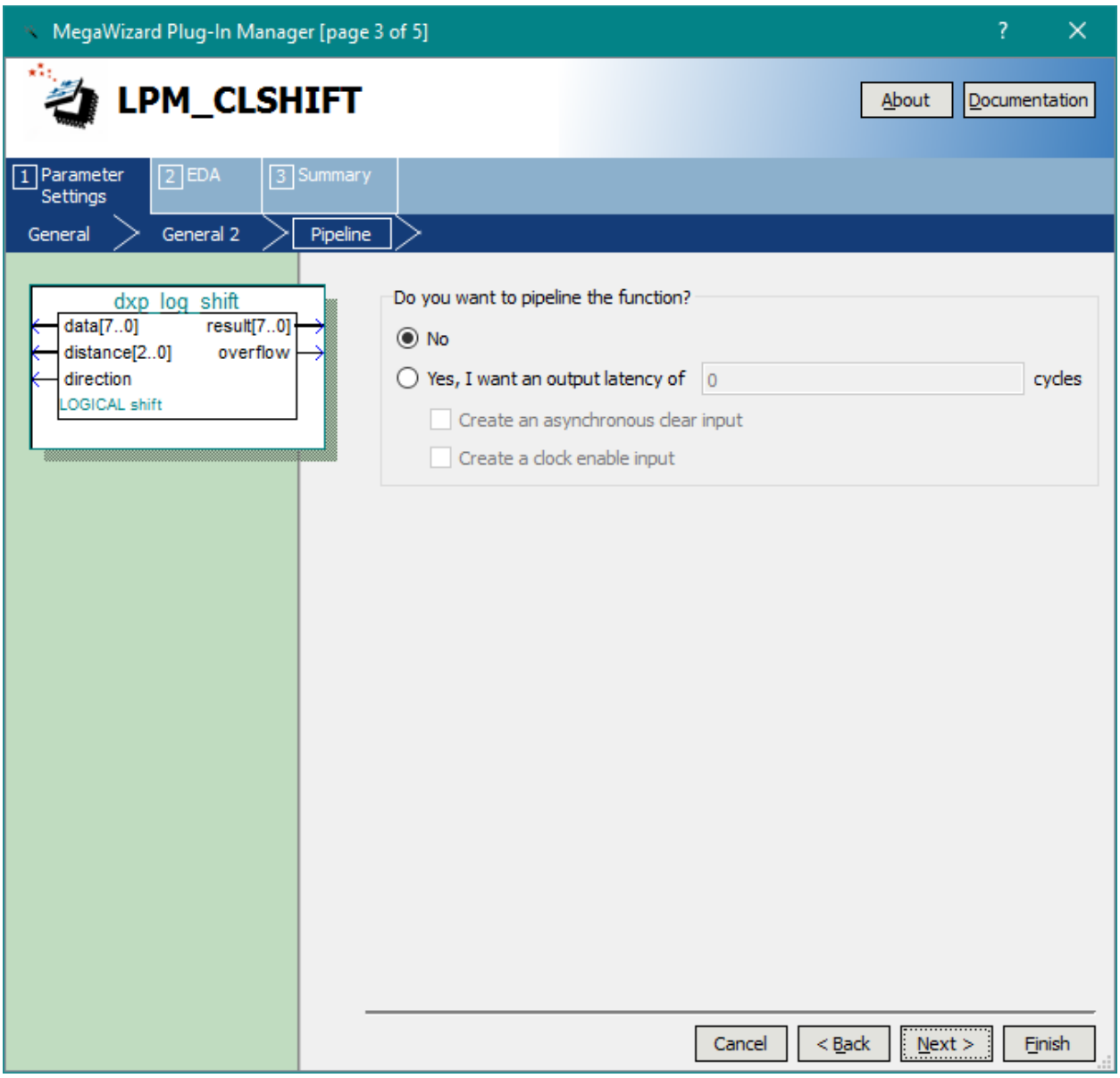
General 2
Pipeline
dxp_log_shift
data[7..0]
distance[2..0]
direction
LOGICAL shift
result[7..0]
overflow
How wide should the 'data' input and the 'result' output buses be? 8 bits
How should the width of the 'distance' input be determined?
Automatically calculate the width to allow the maximum possible shifting range
Restrict the width of the shifting range to 3 bits
Do you want to generate any optional outputs?
(Available only for logical or arithmetic shifting)
Overflow
Underflow
Cancel
< Back
Next >
Finish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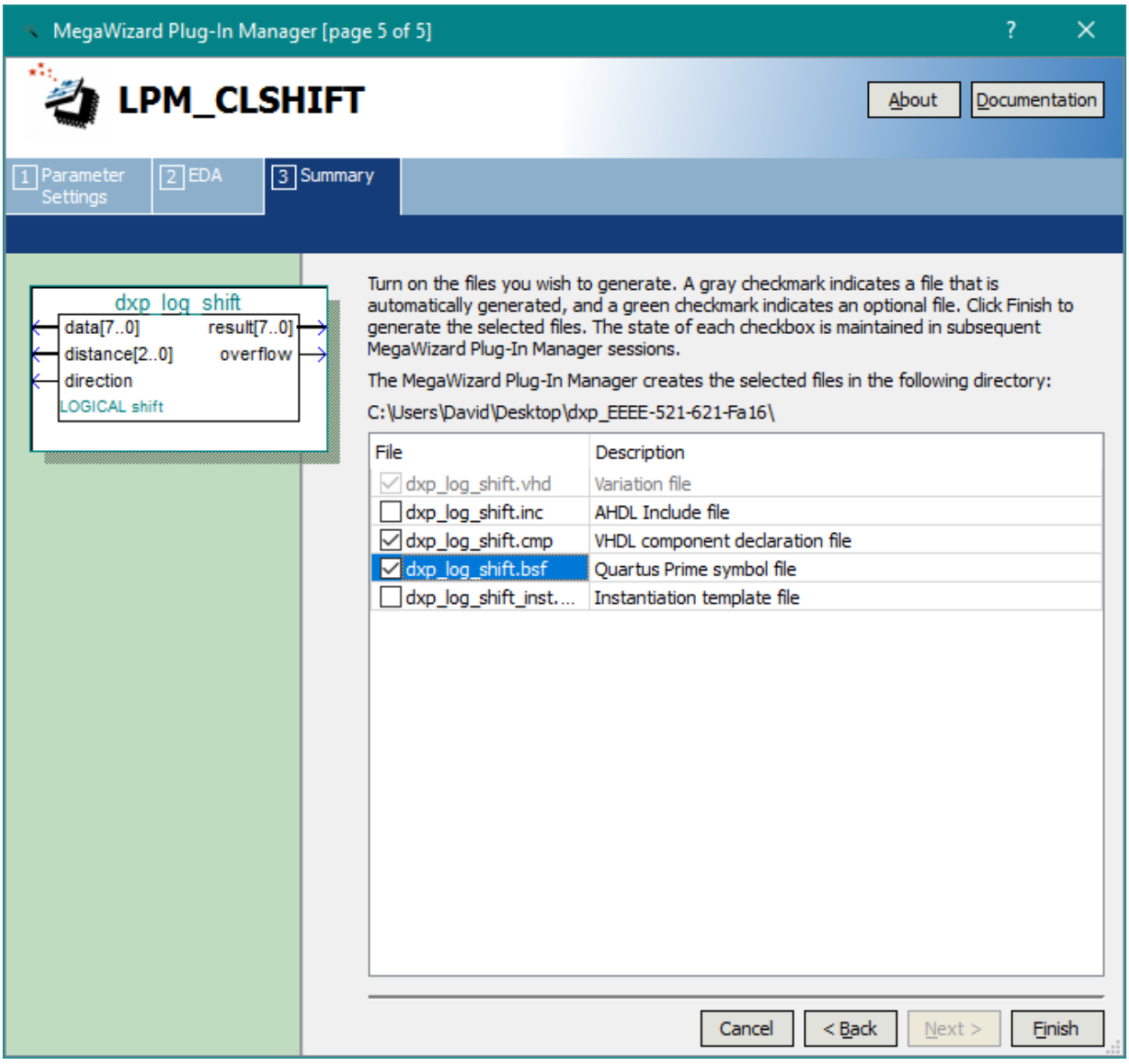
General 2
Pipeline
dxp_log_shift
data[7..0]
distance[2..0]
direction
LOGICAL shift
result[7..0]
overflow
Do you want to pipeline the function?
No
Yes, I want an output latency of
0
cycles
Create an asynchronous clear input
Create a clock enable input
Cancel
< Back
Next >
Finish


MegaWizard Plug-In Manager [page 5 of 5]
LPM_CLSHIFT
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dxp_log_shift
data[7..0]
distance[2..0]
direction
LOGICAL shift
result[7..0]
overflow
Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.
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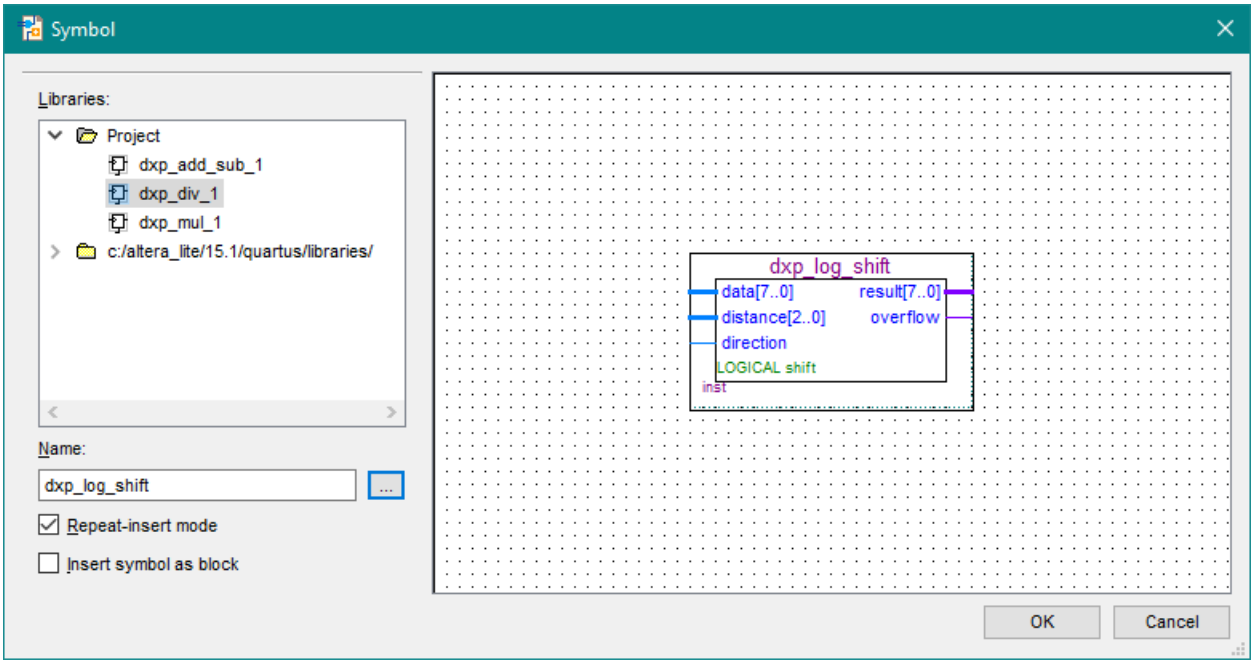
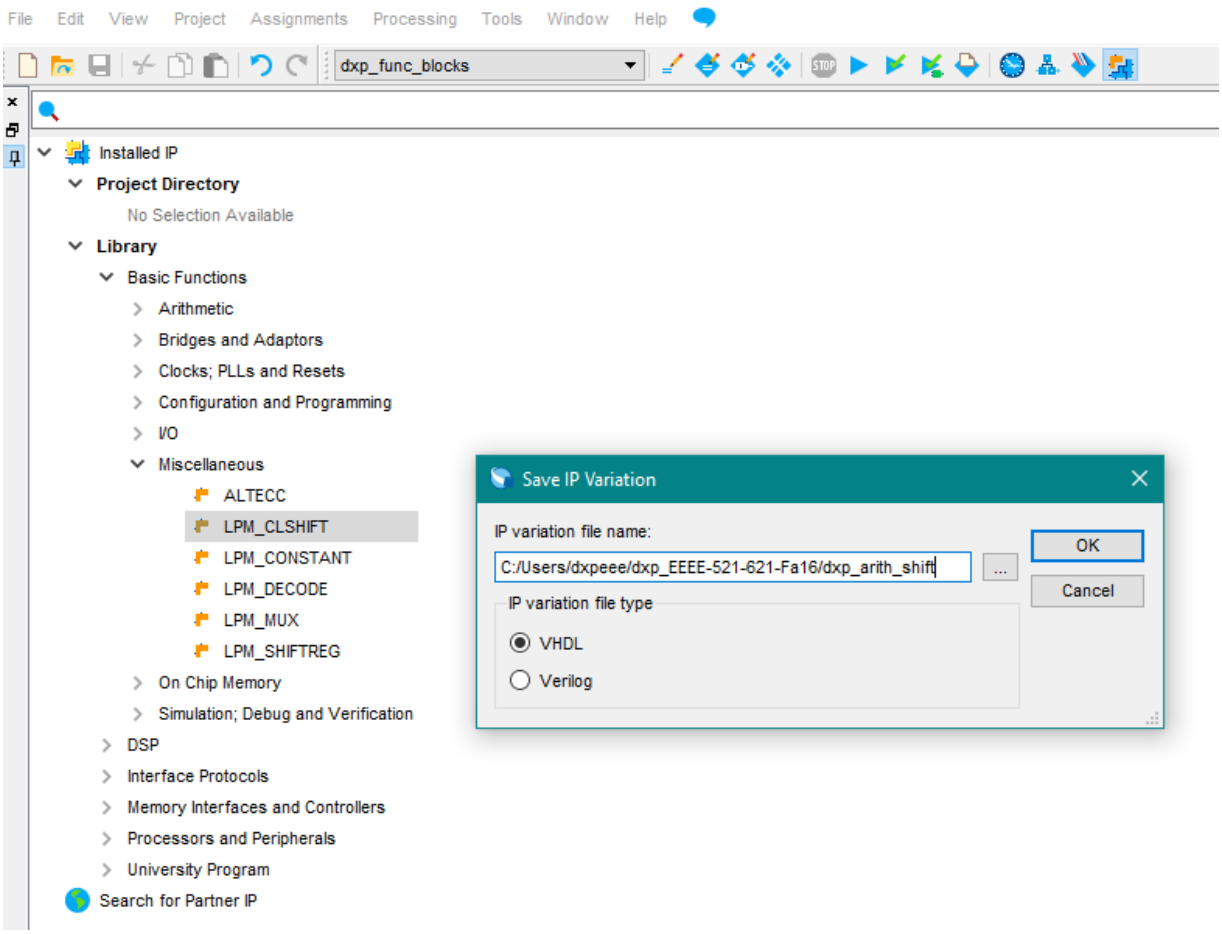
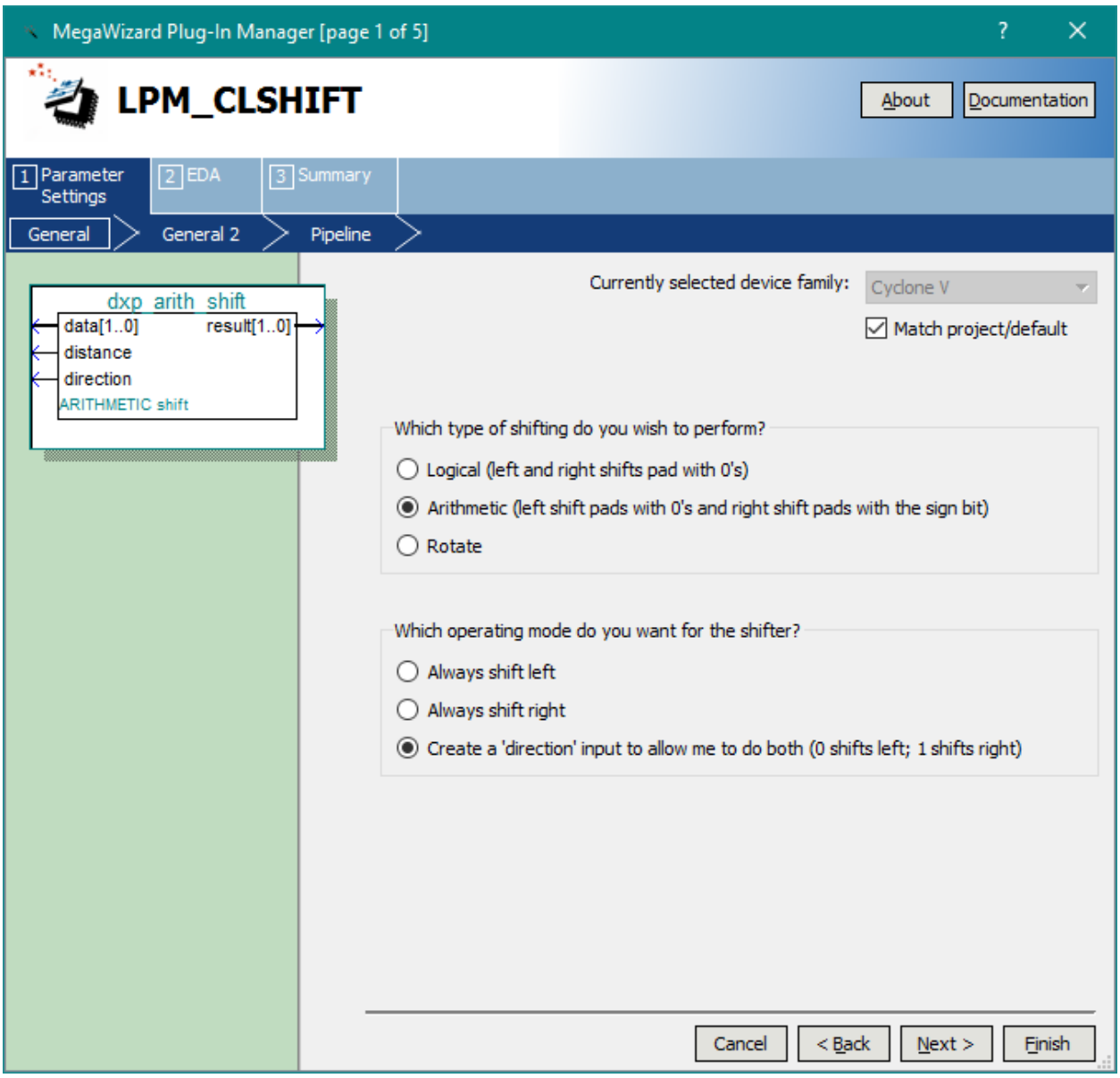
C:\Users\David\Desktop\dxp_EEEE-521-621-Fa16\
File
Description
dxp_log_shift.vhd
Variation file
dxp_log_shift.inc
AHDL Include file
dxp_log_shift.cmp
VHDL component declaration file
dxp_log_shift.bsf
Quartus Prime symbol file
dxp_log_shift_inst....
Instantiation template file
Cancel
< Back
Next >
Finish



26) The fifth component is an arithmetic shifter.

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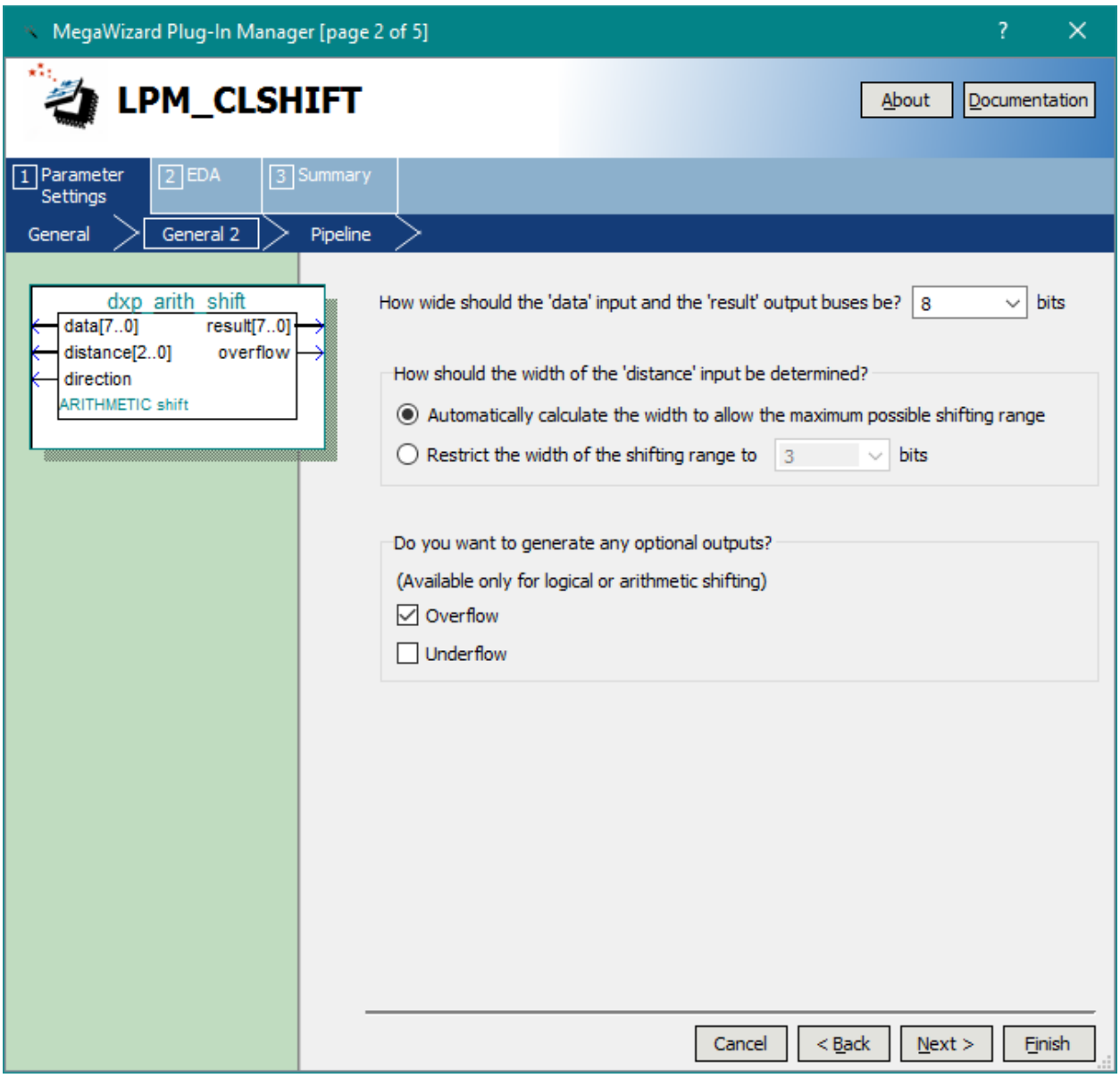
result[1..0]
distance
direction
ARITHMETIC shift
Currently selected device family:
Cyclone V
Match project/default
Which type of shifting do you wish to perform?
Logical (left and right shifts pad with 0's)
Arithmetic (left shift pads with 0's and right shift pads with the sign bit)
Rotate
Which operating mode do you want for the shifter?
Always shift left
Always shift right
Create a 'direction' input to allow me to do both (0 shifts left; 1 shifts right)
Cancel
< Back
Next >
Finish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dxp_arith_shift
data[7..0]
distance[2..0]
direction
ARITHMETIC shift
result[7..0]
overflow
How wide should the 'data' input and the 'result' output buses be? 8 bits
How should the width of the 'distance' input be determined?
Automatically calculate the width to allow the maximum possible shifting range
Restrict the width of the shifting range to 3 bits
Do you want to generate any optional outputs?
(Available only for logical or arithmetic shifting)
Overflow
Underflow
Cancel
< Back
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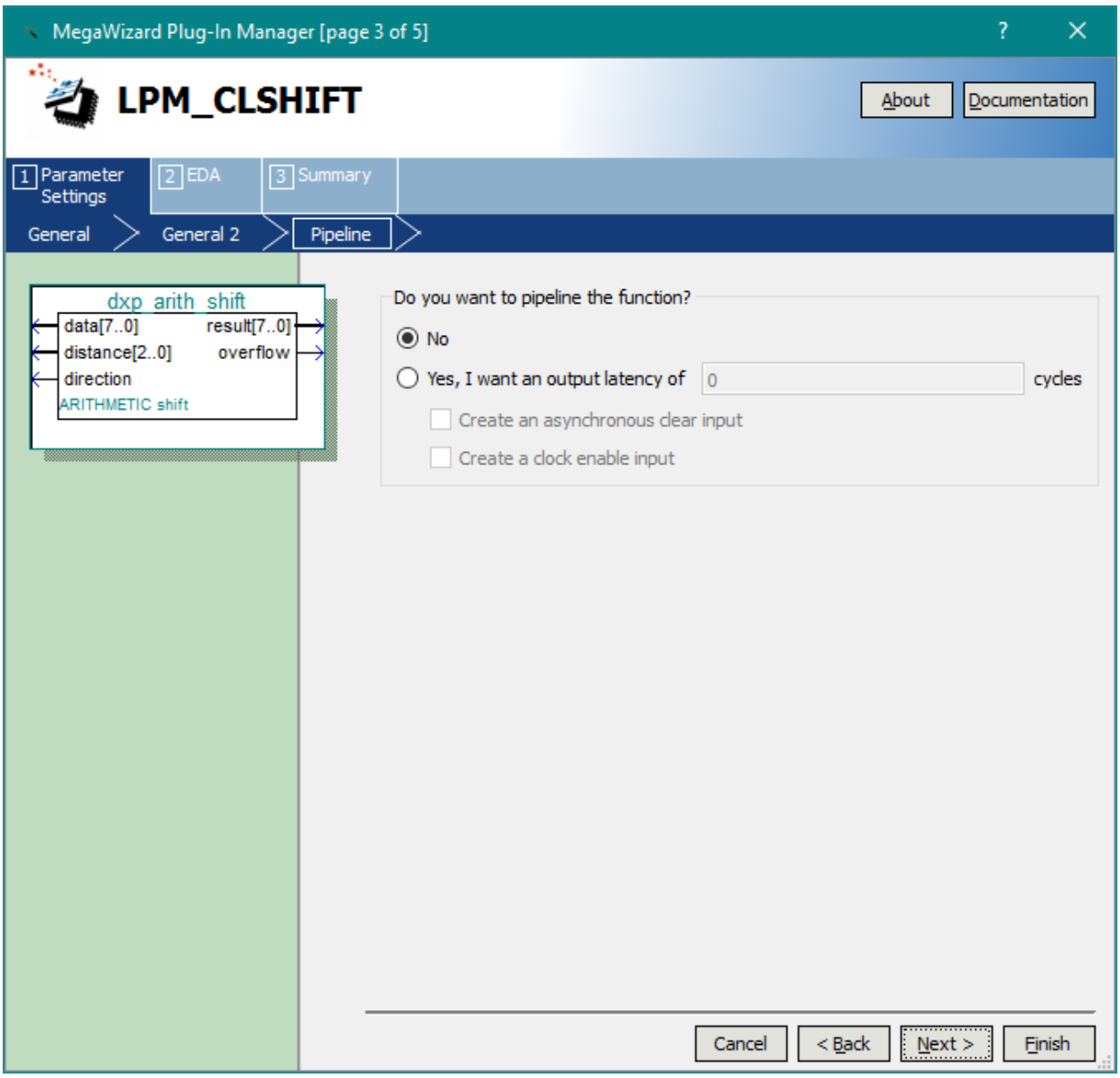
Finish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dxp_arith_shift
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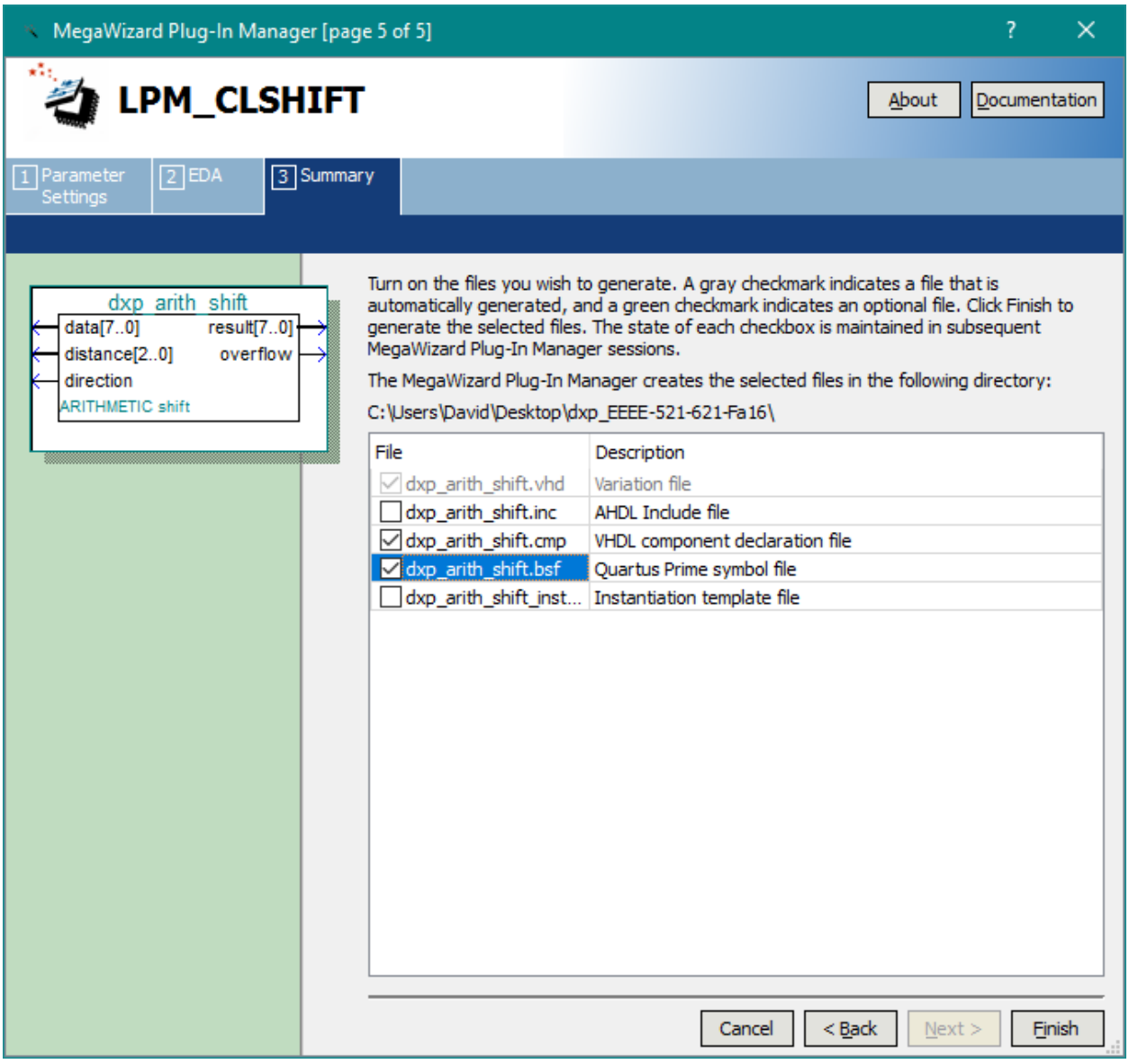
distance[2..0]
direction
ARITHMETIC shift
result[7..0]
overflow
Do you want to pipeline the function?
No
Yes, I want an output latency of
0
cycles
Create an asynchronous clear input
Create a clock enable input
Cancel
< Back
Next >
Finish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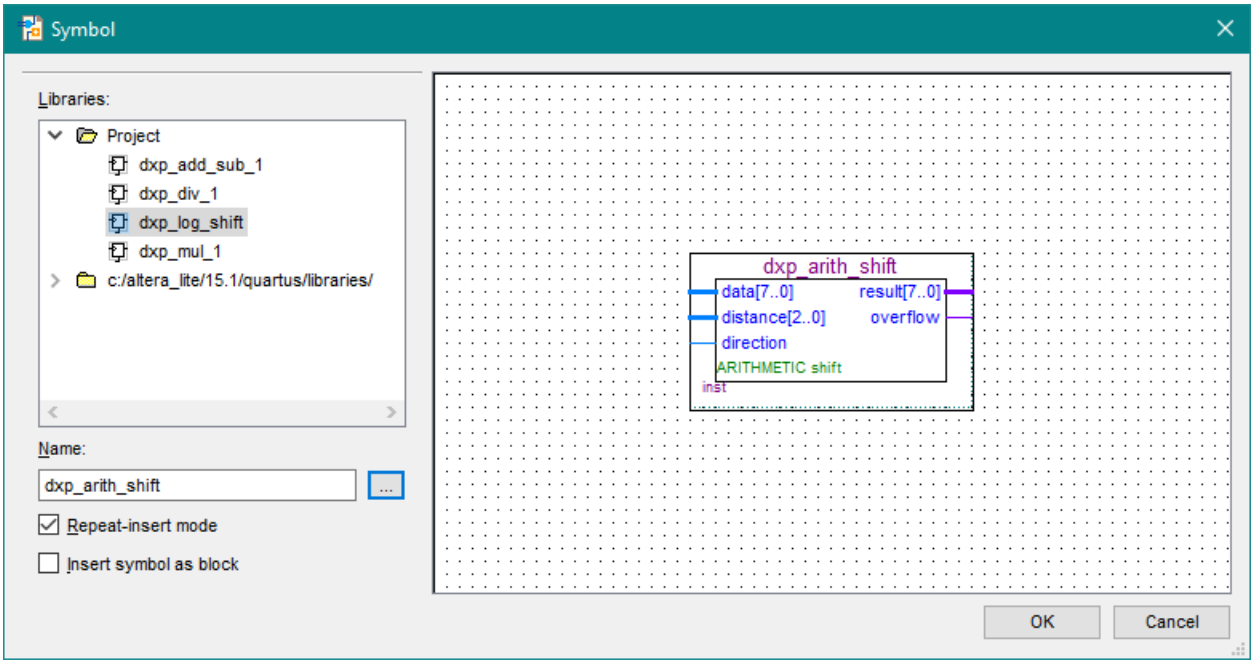
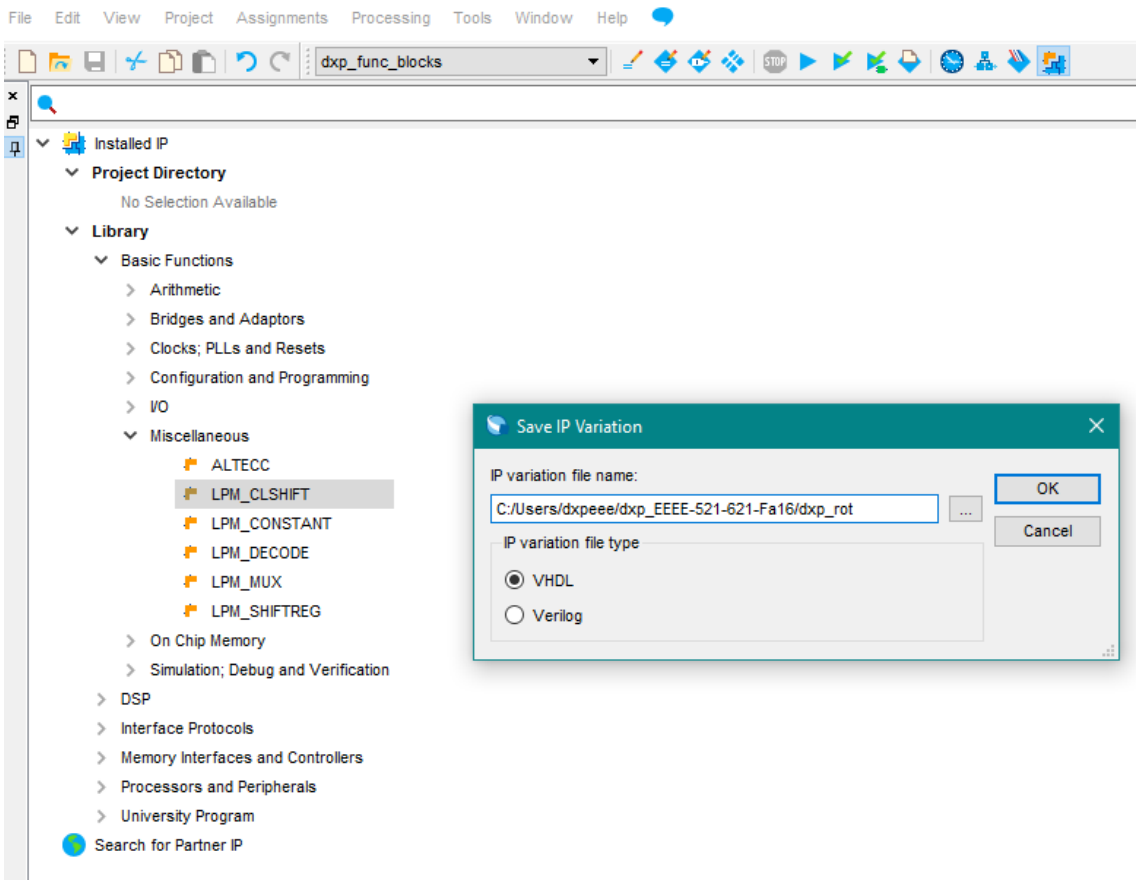
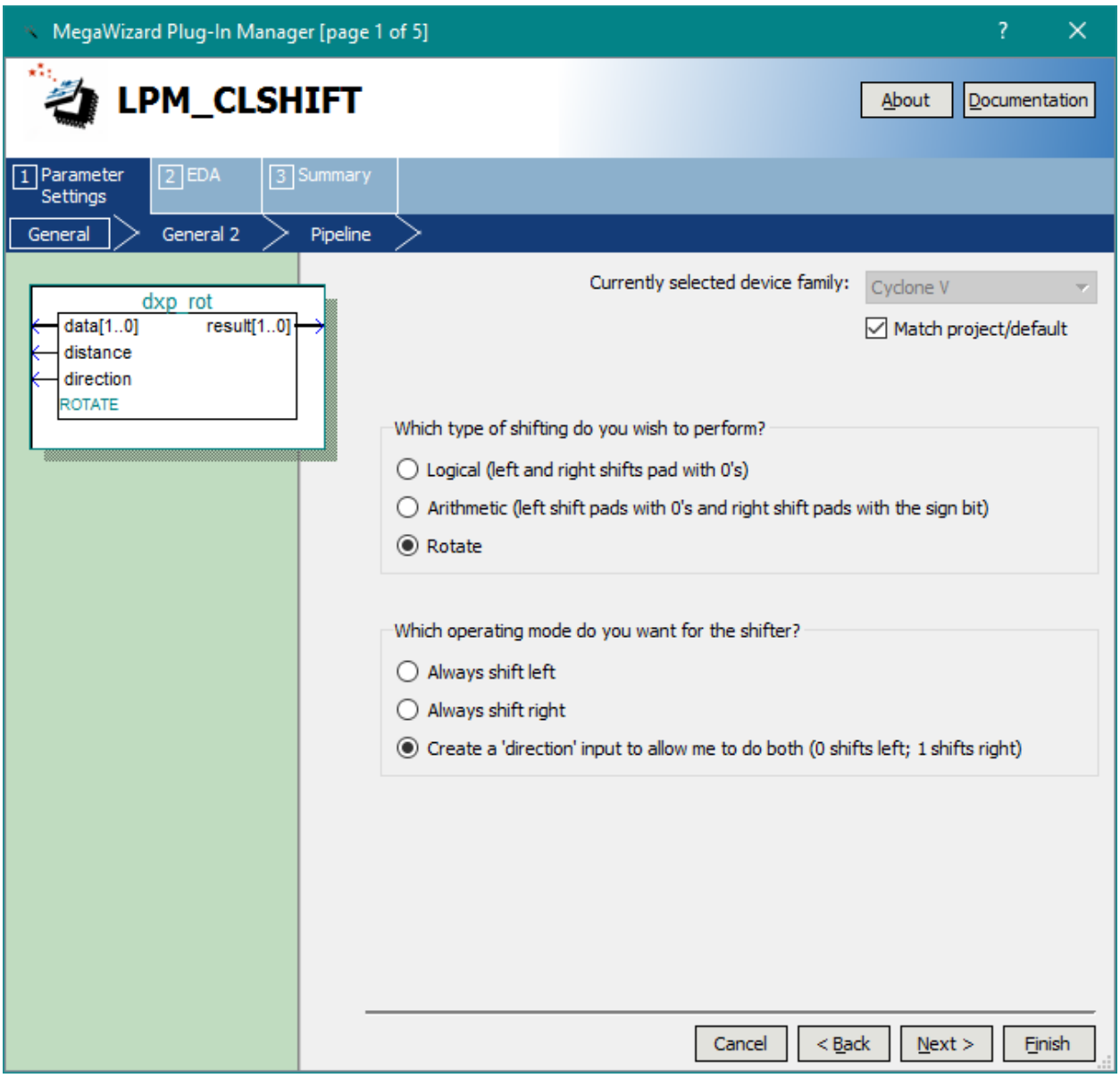
data[7..0]
distance[2..0]
direction
ARITHMETIC shift
result[7..0]
overflow
Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.
The MegaWizard Plug-In Manager creates the selected files in the following directory:
C:\Users\David\Desktop\dxp_EEEE-521-621-Fa16\
File
Description
dxp_arith_shift.vhd
Variation file
dxp_arith_shift.inc
AHDL Include file
dxp_arith_shift.cmp
VHDL component declaration file
dxp_arith_shift.bsf
Quartus Prime symbol file
dxp_arith_shift_inst...
Instantiation template file
Cancel
< Back
Next >
Finish



27) The sixth component is a rotate functional unit.

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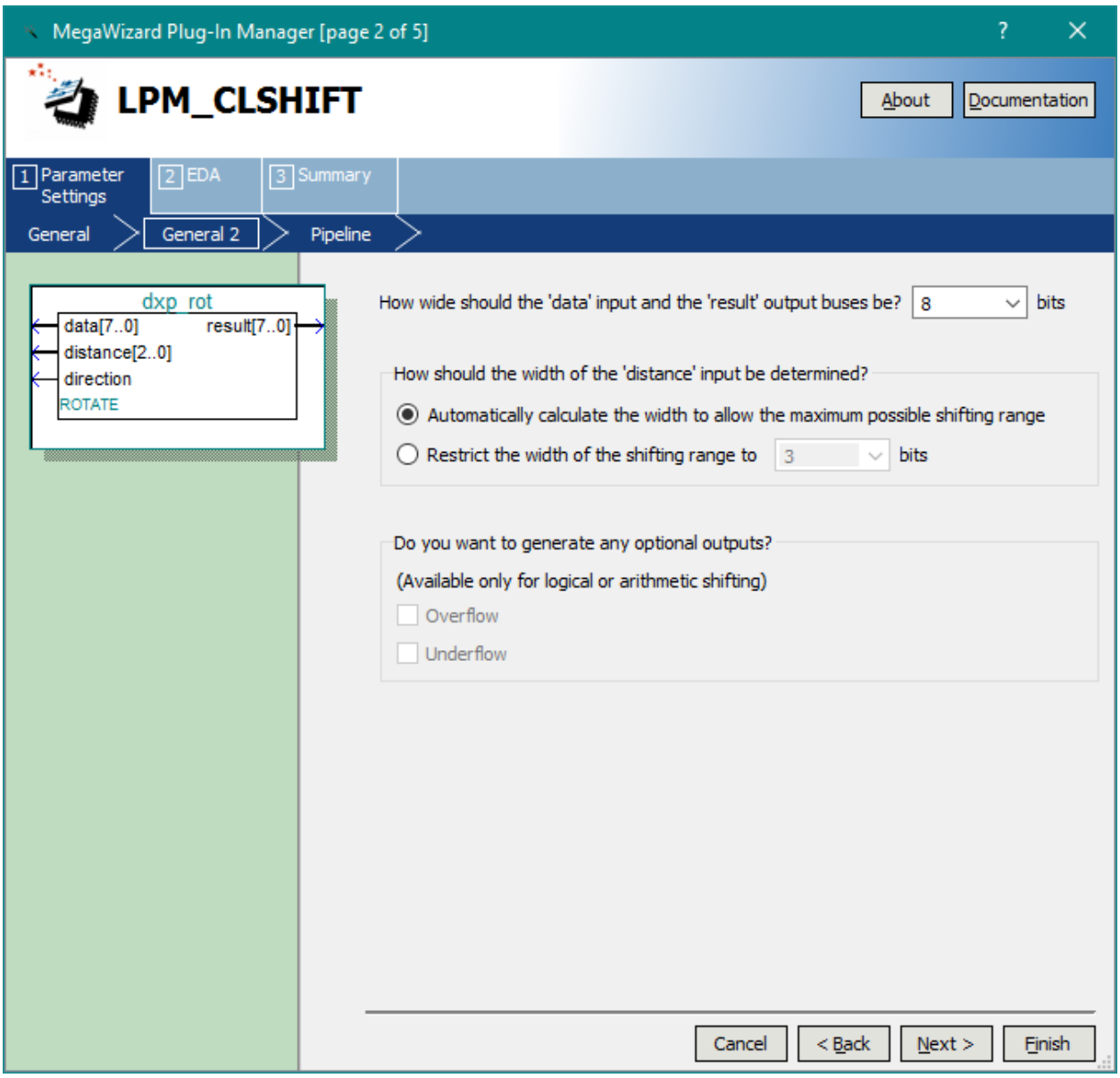
data[1..0]
result[1..0]
distance
direction
ROTATE
Currently selected device family:
Cyclone V
Match project/default
Which type of shifting do you wish to perform?
Logical (left and right shifts pad with 0's)
Arithmetic (left shift pads with 0's and right shift pads with the sign bit)
Rotate
Which operating mode do you want for the shifter?
Always shift left
Always shift right
Create a 'direction' input to allow me to do both (0 shifts left; 1 shifts right)
Cancel
< Back
Next >
Finish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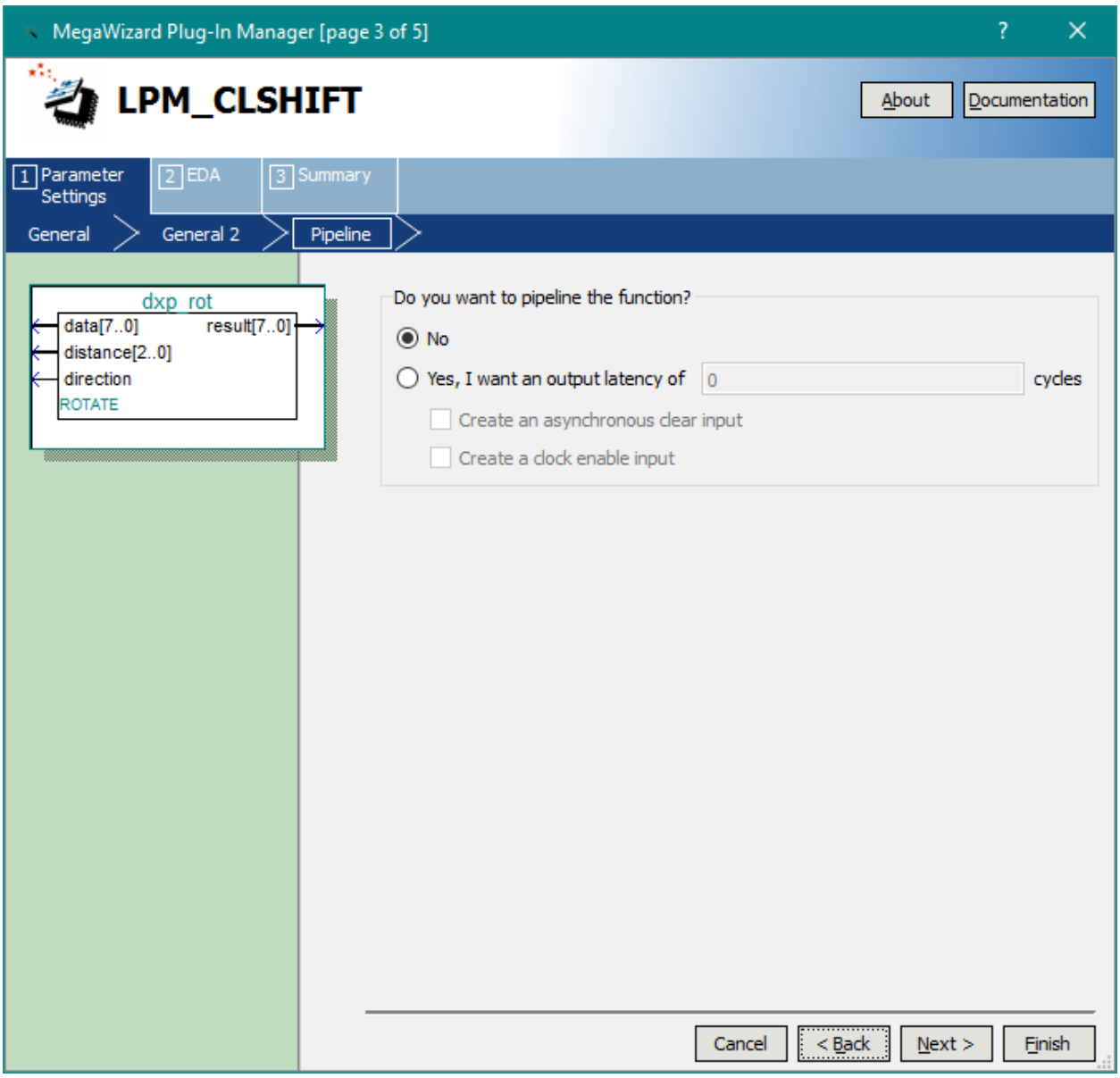
data[7..0]
distance[2..0]
direction
ROTATE
result[7..0]
How wide should the 'data' input and the 'result' output buses be? 8 bits
How should the width of the 'distance' input be determined?
Automatically calculate the width to allow the maximum possible shifting range
Restrict the width of the shifting range to 3 bits
Do you want to generate any optional outputs?
(Available only for logical or arithmetic shifting)
Overflow
Underflow
Cancel
< Back
Next >
Finish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3 Summary
General
General 2
Pipeline
dxp_rot
data[7..0]
distance[2..0]
direction
ROTATE
result[7..0]
Do you want to pipeline the function?
No
Yes, I want an output latency of
0
cycles
Create an asynchronous clear input
Create a clock enable input
Cancel
< Back
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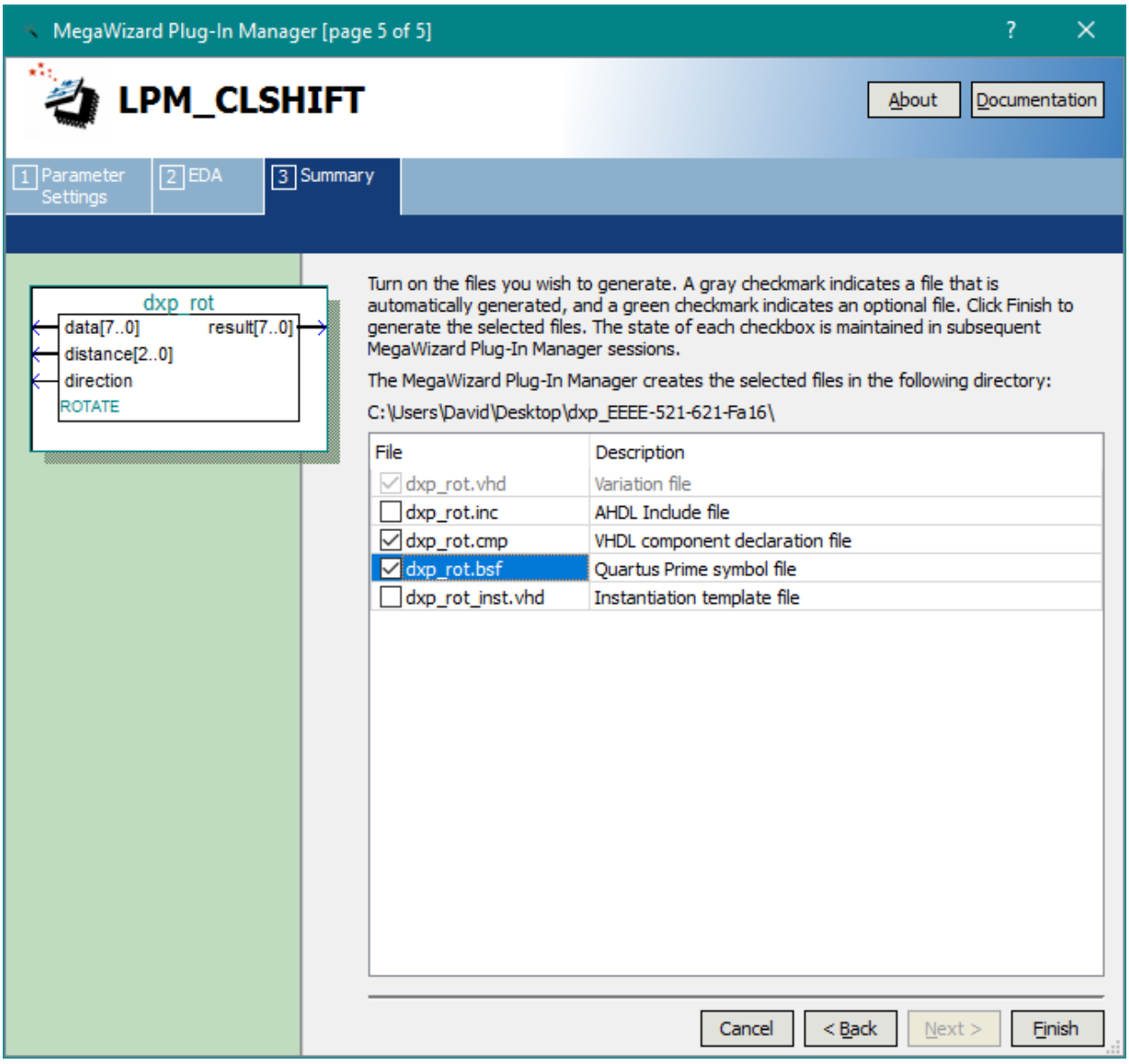
Finish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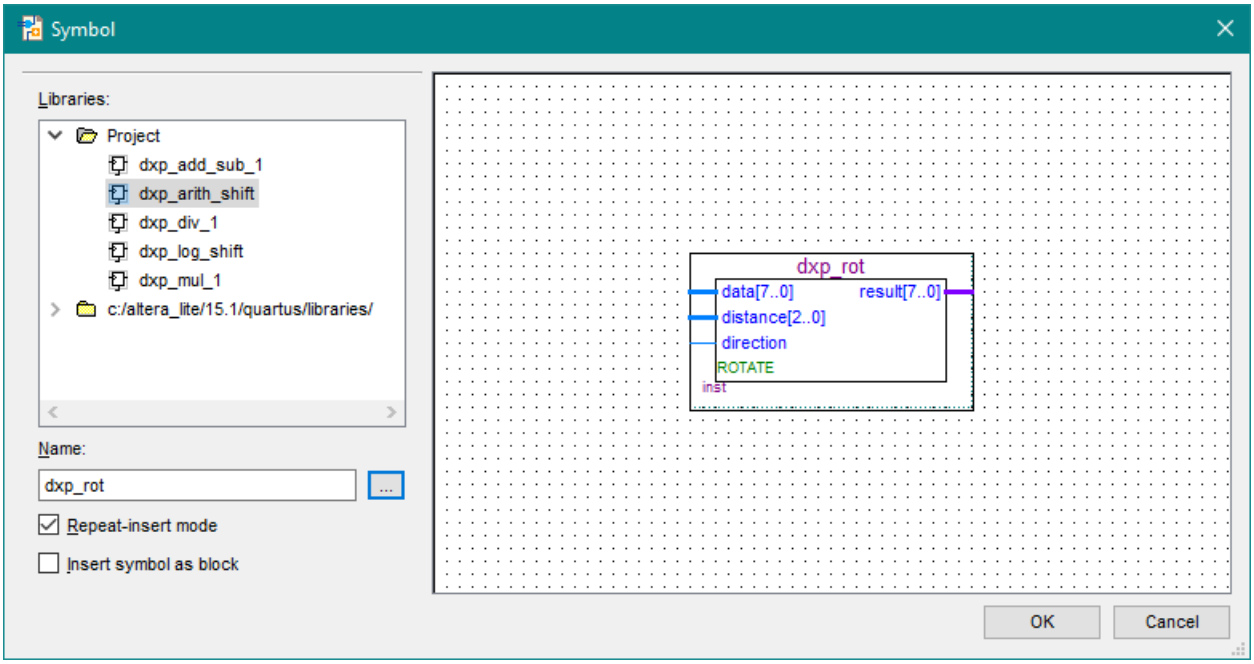
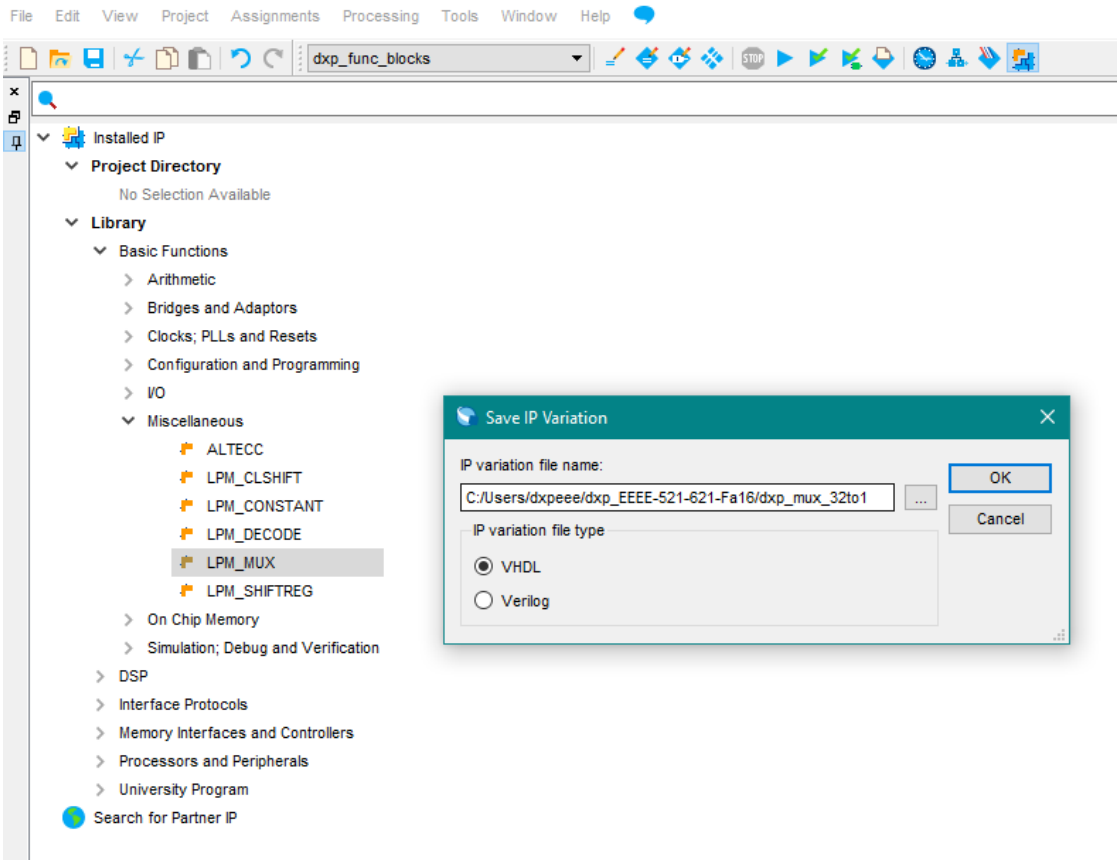
dxp_rot
data[7..0]
result[7..0]
distance[2..0]
direction
ROTATE
Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.
The MegaWizard Plug-In Manager creates the selected files in the following directory:
C:\Users\David\Desktop\dxp_EEEE-521-621-Fa16\
File
Description
dxp_rot.vhd
Variation file
dxp_rot.inc
AHDL Include file
dxp_rot.cmp
VHDL component declaration file
dxp_rot.bsf
Quartus Prime symbol file
dxp_rot_inst.vhd
Instantiation template file
Cancel
< Back
Next >
Finish



28) The seventh component is a 32-to-1 multiplexer.



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LPM_MUX

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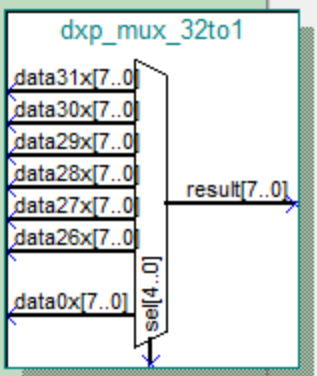

Currently selected device family: Cyclone V

☑ Match project/default

How many 'data' inputs do you want? 32

How wide should the 'data' input and the 'result' output buses be? 8 bits

Do you want to pipeline the multiplexer?

- ◉ No
- ○ Yes, I want an output latency of 1 clock cycles
  - ☐ Create an asynchronous Clear input
  - ☐ Create a Clock Enable input

Resource Usage

...

Cancel | < Back | Next > | Finish

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LPM_MUX

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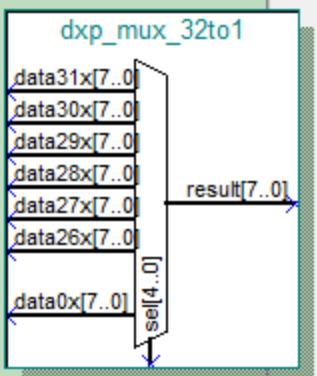
1 Parameter Settings | 2 EDA | 3 Summary



Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.

The MegaWizard Plug-In Manager creates the selected files in the following directory:

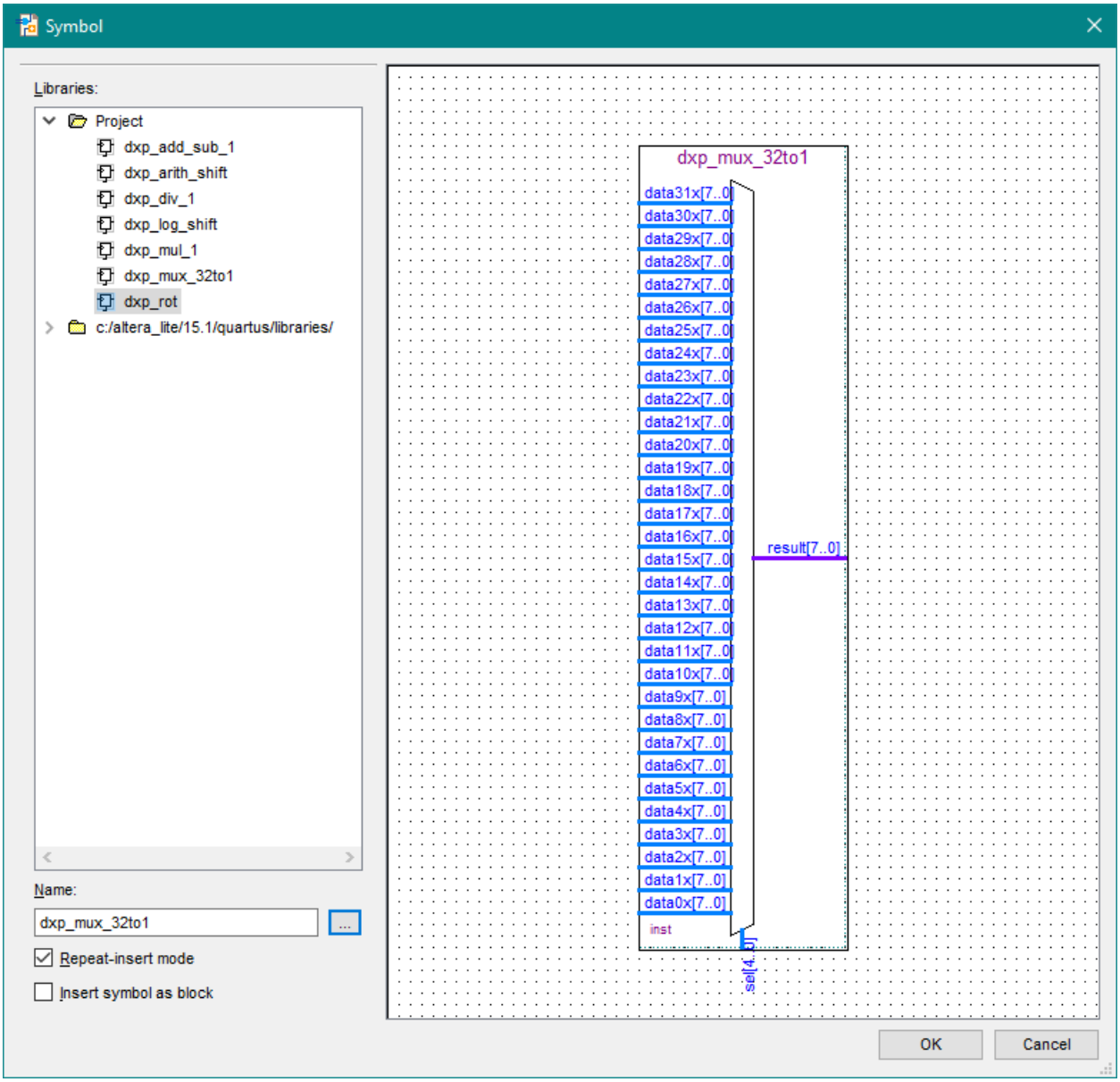
C:\Users\David\Desktop\dxp_EEEE-521-621-Fa16\

File	Description
☑ dxp_mux_32to1.vhd	Variation file
☐ dxp_mux_32to1.inc	AHDL Include file
☑ dxp_mux_32to1.cmp	VHDL component declaration file
☑ dxp_mux_32to1.bsf	Quartus Prime symbol file
☐ dxp_mux_32to1_in...	Instantiation template file

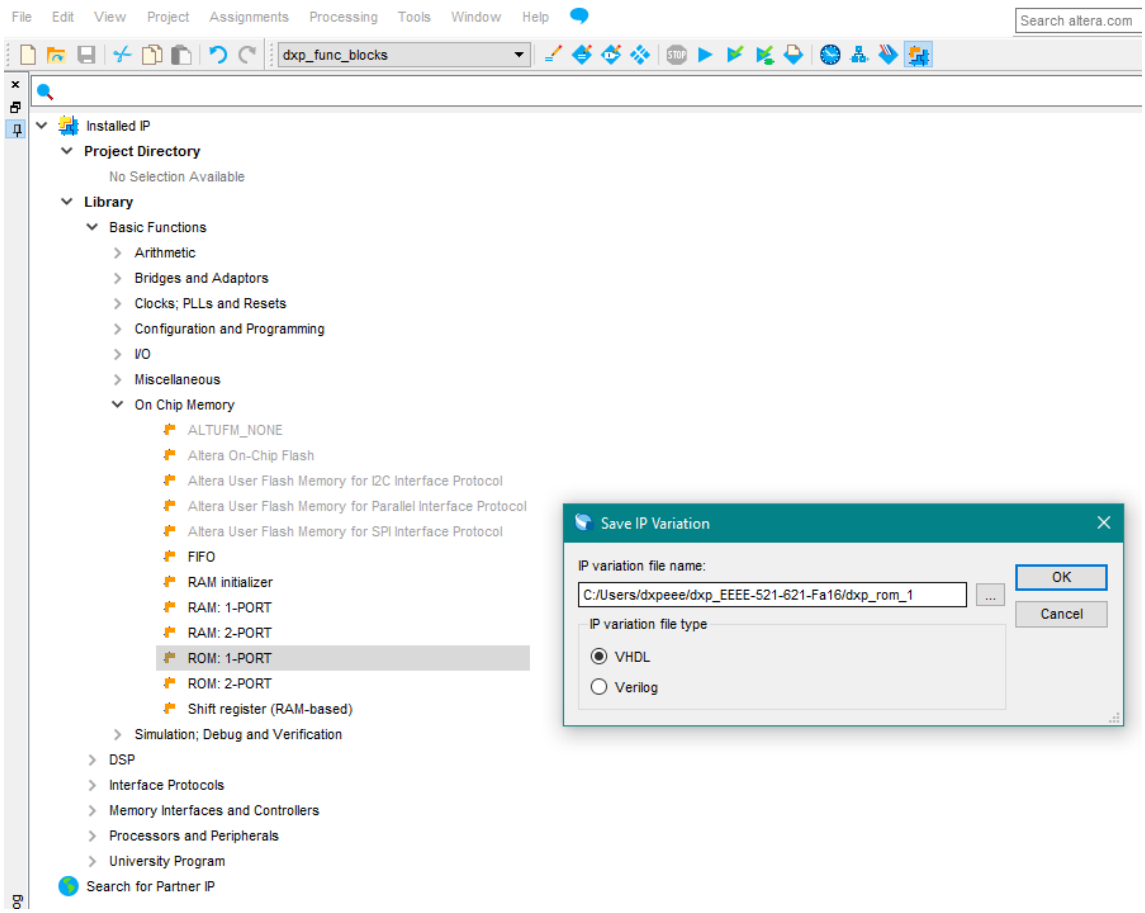
Resource Usage

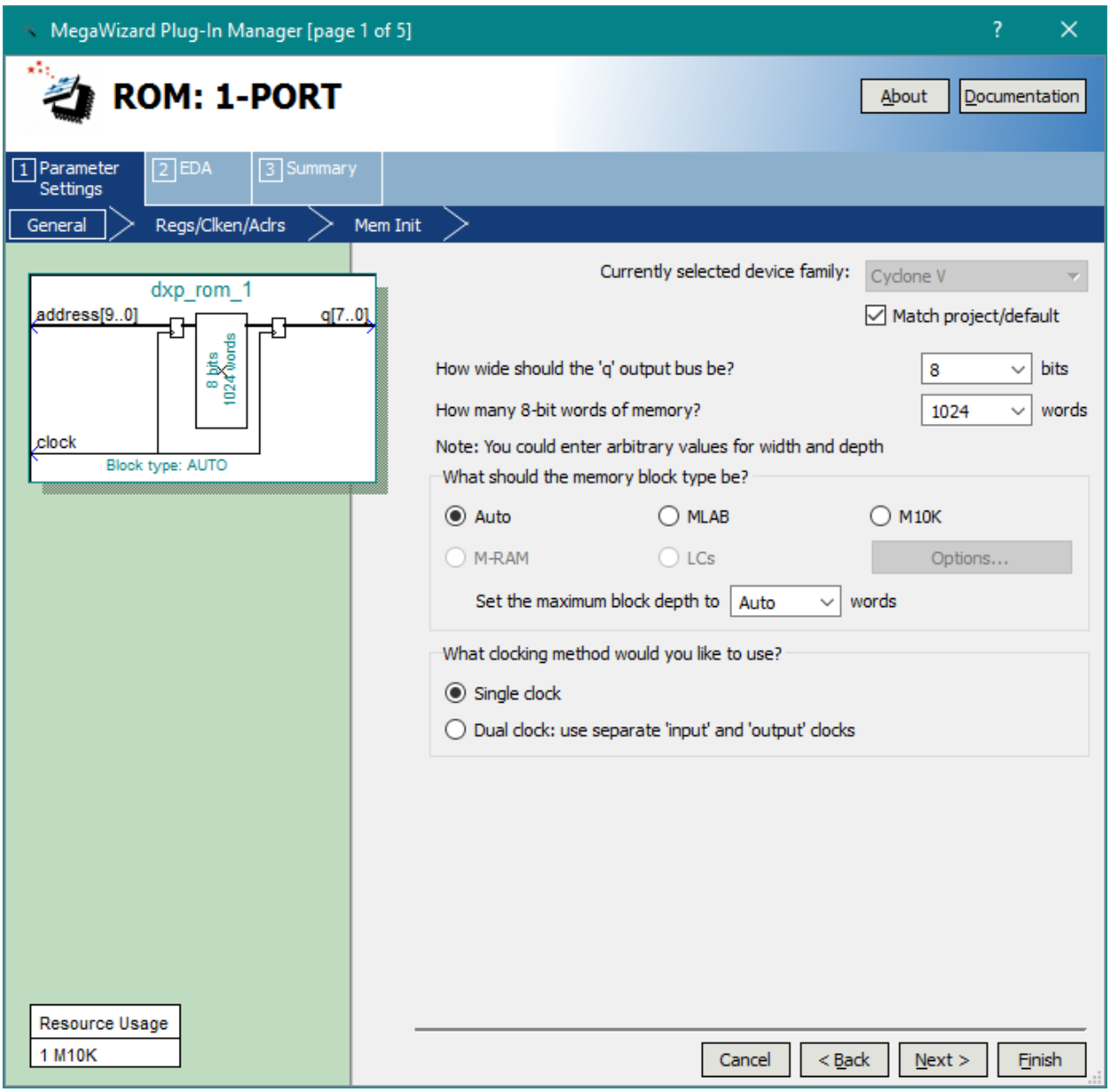
...

Cancel | < Back | Next > | Finish



29) The eight' component is a ROM, located under "Library → Basic Functions → On Chip Memory".


File
Edit
View
Project
Assignments
Processing
Tools
Window
Help
Search altera.com
dxp_func_blocks
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
Arithmetic
Bridges and Adaptors
Clocks; PLLs and Resets
Configuration and Programming
I/O
Miscellaneous
On Chip Memory
ALTUFM_NONE
Altera On-Chip Flash
Altera User Flash Memory for I2C Interface Protocol
Altera User Flash Memory for Parallel Interface Protocol
Altera User Flash Memory for SPI Interface Protocol
FIFO
RAM initializer
RAM: 1-PORT
RAM: 2-PORT
ROM: 1-PORT
ROM: 2-PORT
Shift register (RAM-based)
Simulation; Debug and Verification
DSP
Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
Save IP Variation
IP variation file name:
C:/Users/dxpeee/dxp_EEEE-521-621-Fa16/dxp_rom_1
...
OK
Cancel
IP variation file type
VHDL
Verilog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ROM: 1-PORT
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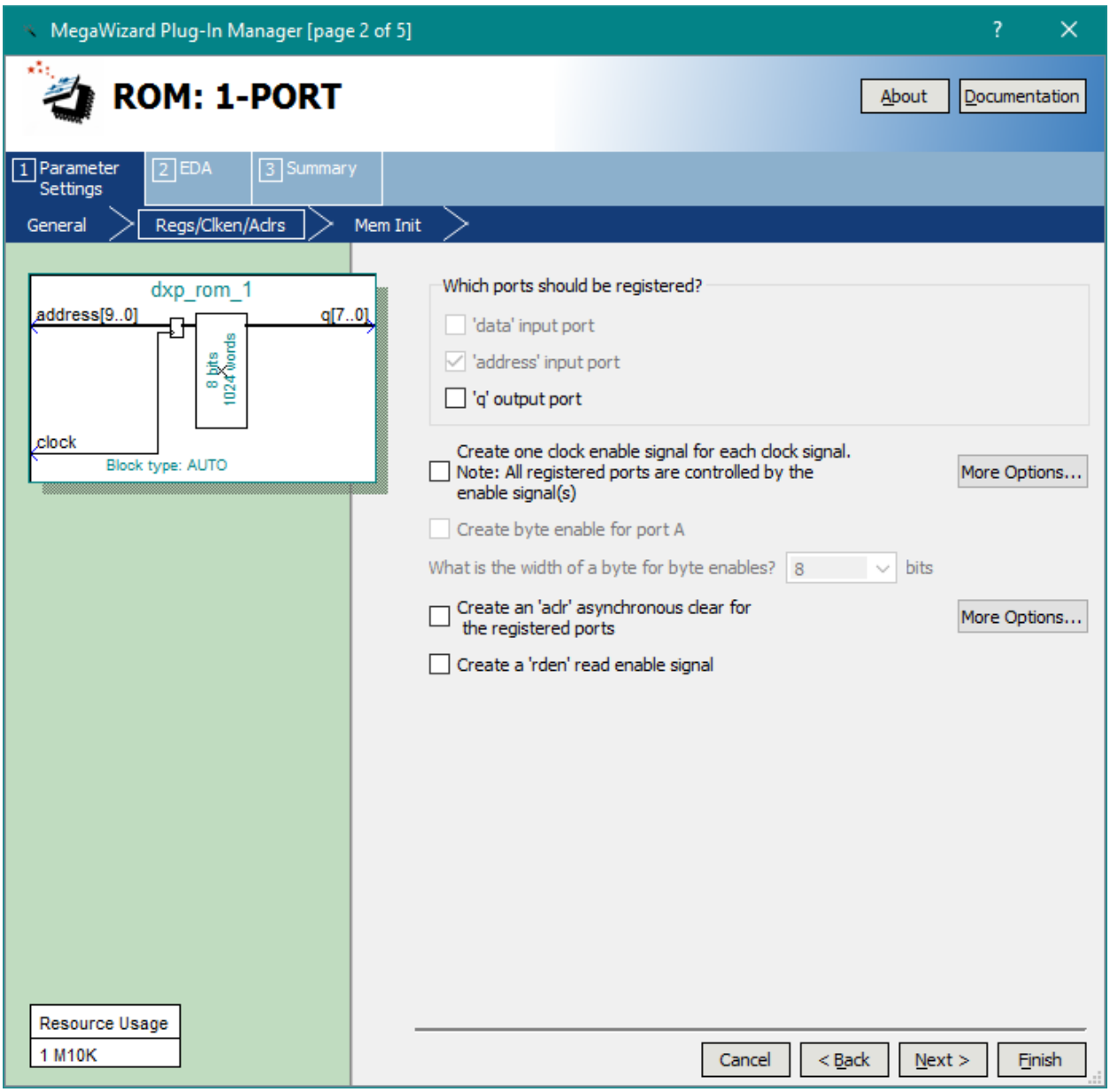
3 Summary
General
Regs/Clken/Adrs
Mem Init
dxp_rom_1
address[9..0]
q[7..0]
8 bits
1024 words
clock
Block type: AUTO
Currently selected device family:
Cyclone V
Match project/default
How wide should the 'q' output bus be?
8
bits
How many 8-bit words of memory?
1024
words
Note: You could enter arbitrary values for width and depth
What should the memory block type be?
Auto
MLAB
M10K
M-RAM
LCs
Options...
Set the maximum block depth to
Auto
words
What clocking method would you like to use?
Single clock
Dual clock: use separate 'input' and 'output' clocks
Resource Usage
1 M10K
Cancel
< Back
Next >
Finish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ROM: 1-PORT
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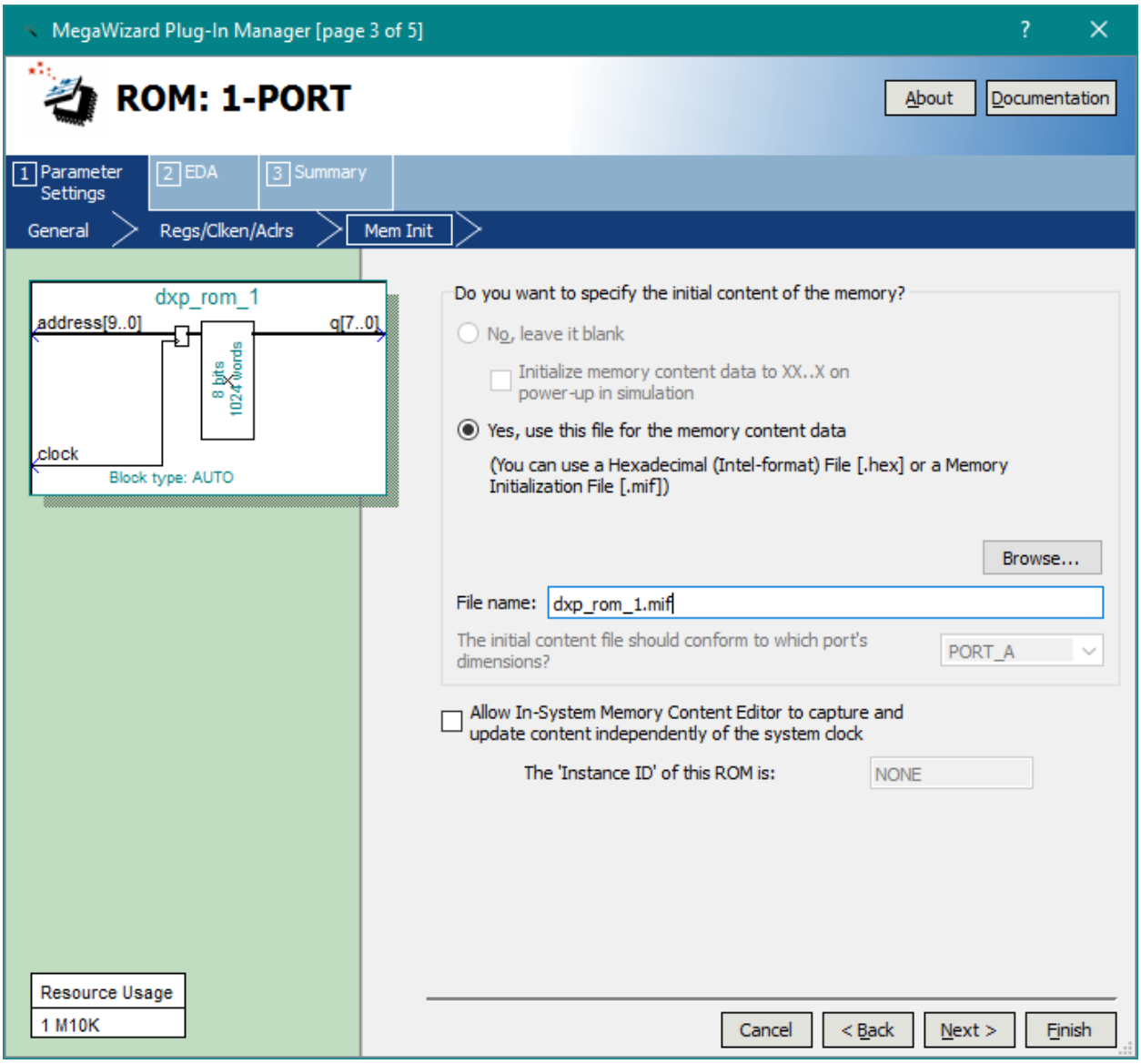
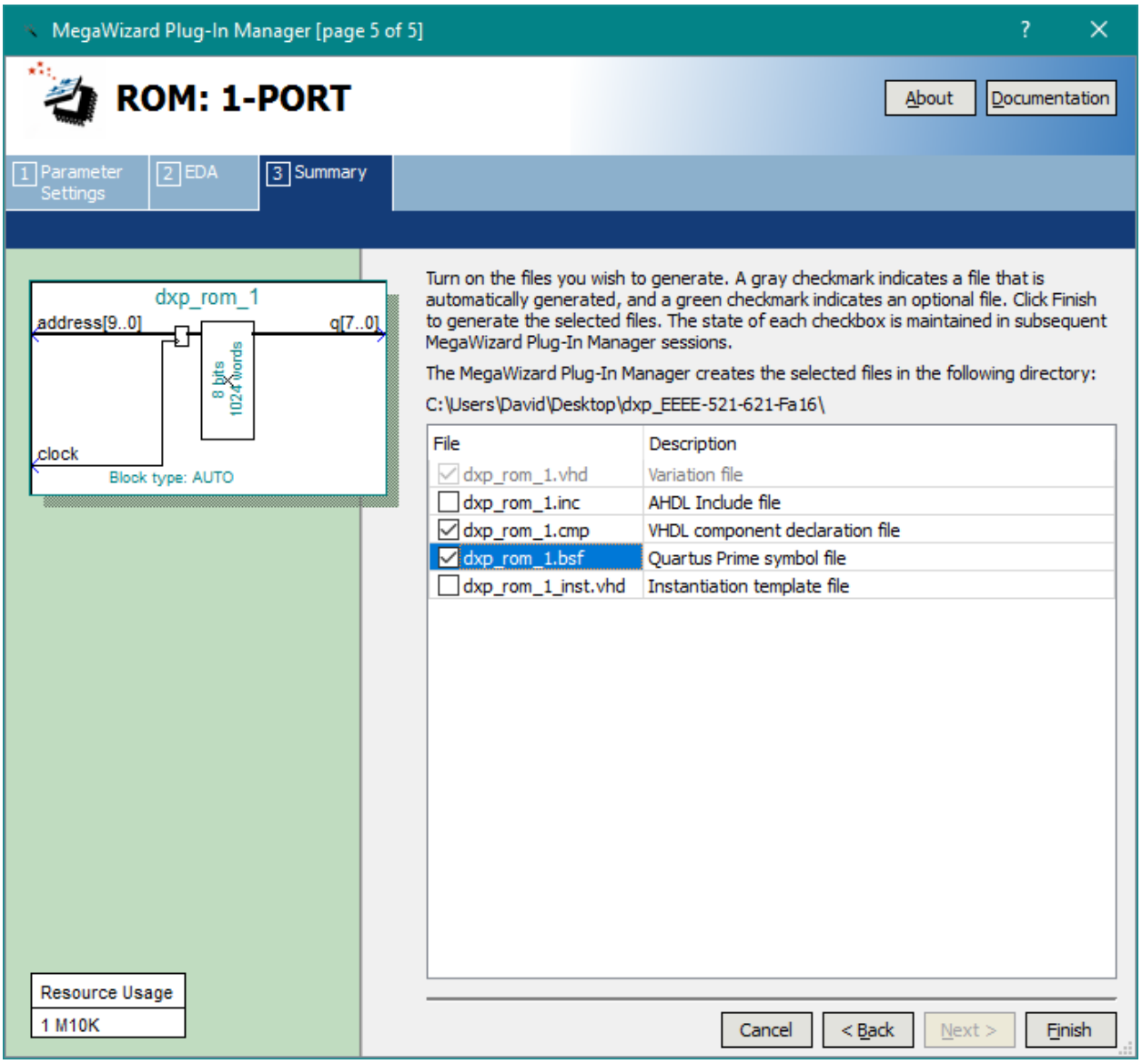
3 Summary
General
Regs/Clken/Adrs
Mem Init
dxp_rom_1
address[9..0]
q[7..0]
8 bits
1024 words
clock
Block type: AUTO
Which ports should be registered?
'data' input port
'address' input port
'q' output port
Create one clock enable signal for each clock signal. Note: All registered ports are controlled by the enable signal(s)
More Options...
Create byte enable for port A
What is the width of a byte for byte enables?
8
bits
Create an 'aclr' asynchronous clear for the registered ports
More Options...
Create a 'rden' read enable signal
Resource Usage
1 M10K
Cancel
< Back
Next >
Finish



Add the fml_rom_1.mif file to your project directory and project.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dxp_rom_1
address[9..0]
q[7..0]
clock
8 bits
1024 words
Block type: AUTO
Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.
The MegaWizard Plug-In Manager creates the selected files in the following directory:
C:\Users\David\Desktop\dxp_EEEE-521-621-Fa16\
File
Description
dxp_rom_1.vhd
Variation file
dxp_rom_1.inc
AHDL Include file
dxp_rom_1.cmp
VHDL component declaration file
dxp_rom_1.bsf
Quartus Prime symbol file
dxp_rom_1_inst.vhd
Instantiation template file
Resource Usage
1 M10K
Cancel
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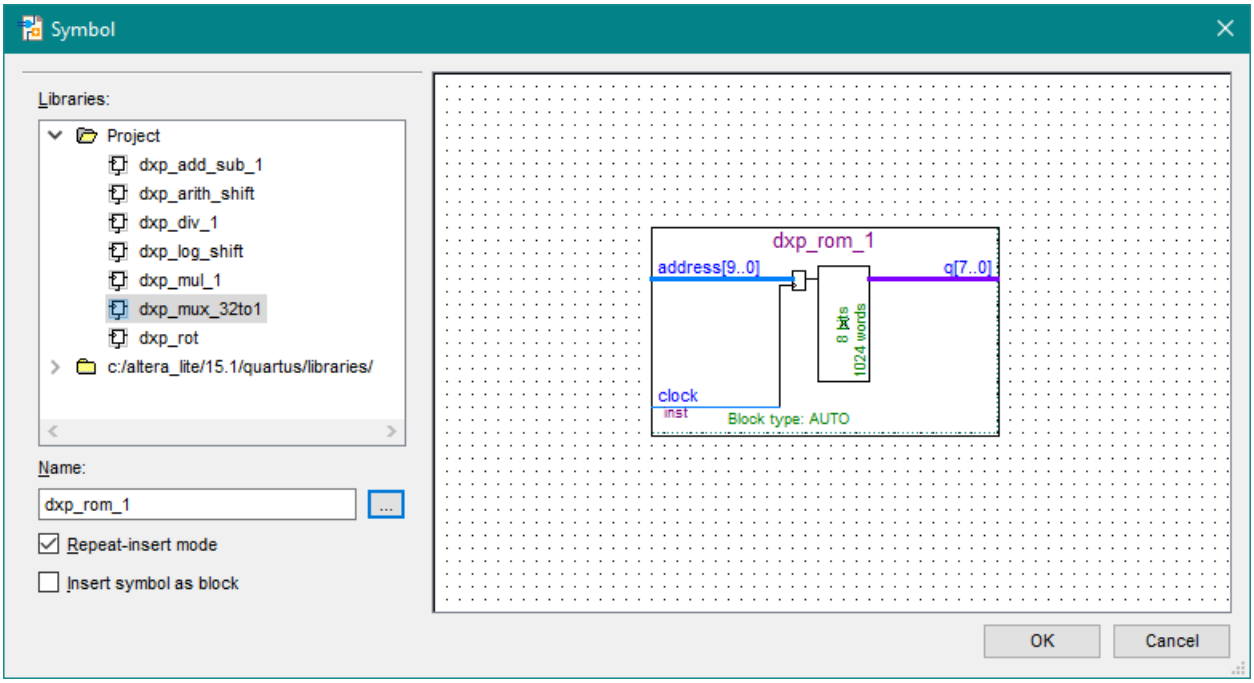
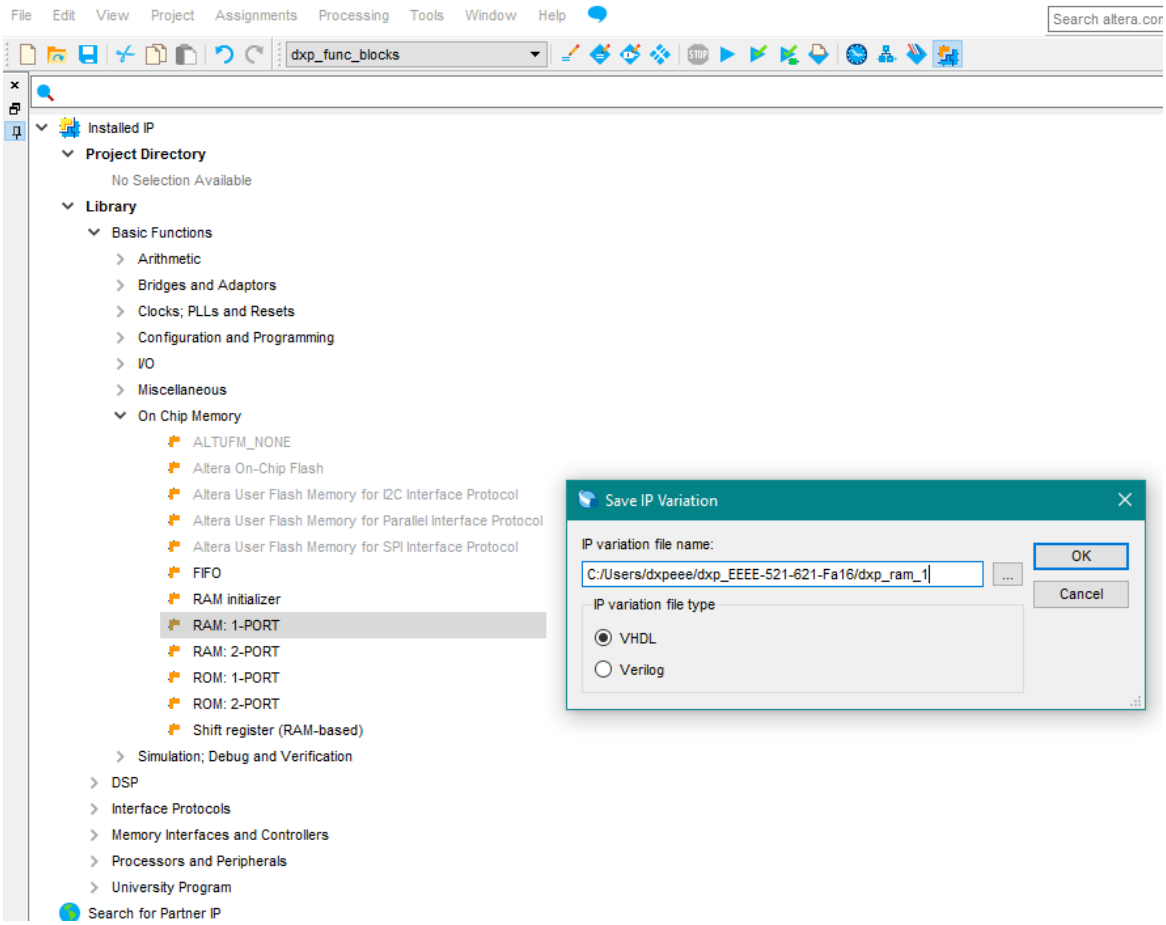
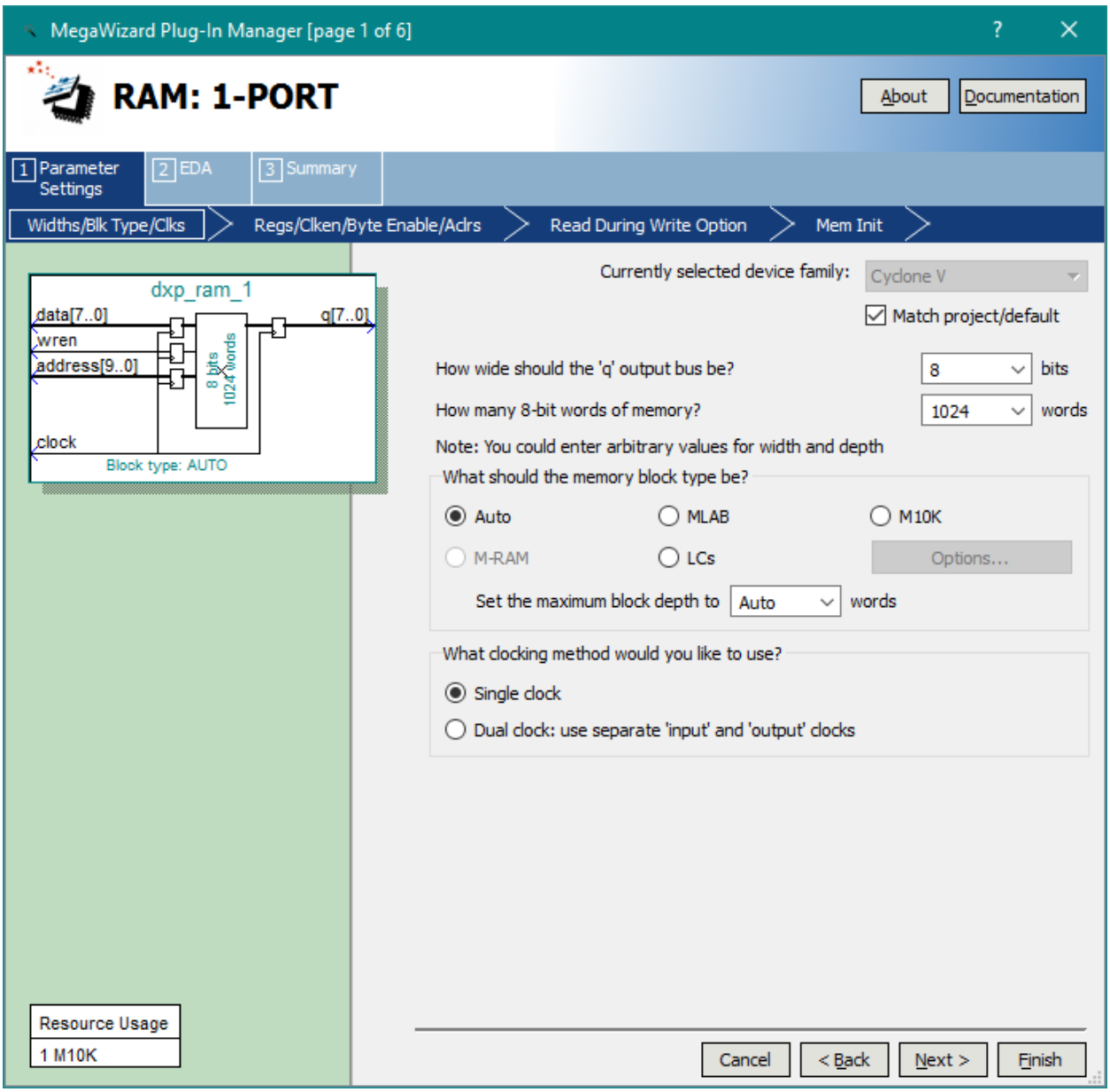
Finish



30) The ninth component is a RAM.




MegaWizard Plug-In Manager [page 1 of 6]
RAM: 1-PORT
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Widths/Blk Type/Clks
Regs/Clken/Byte Enable/Adrs
Read During Write Option
Mem Init
dxp_ram_1
data[7..0]
wren
address[9..0]
clock
q[7..0]
8 bits
1024 words
Block type: AUTO
Currently selected device family:
Cyclone V
Match project/default
How wide should the 'q' output bus be?
8
bits
How many 8-bit words of memory?
1024
words
Note: You could enter arbitrary values for width and depth
What should the memory block type be?
Auto
MLAB
M10K
M-RAM
LCs
Options...
Set the maximum block depth to
Auto
words
What clocking method would you like to use?
Single clock
Dual clock: use separate 'input' and 'output' clocks
Resource Usage
1 M10K
Cancel
< Back
Next >
Finish

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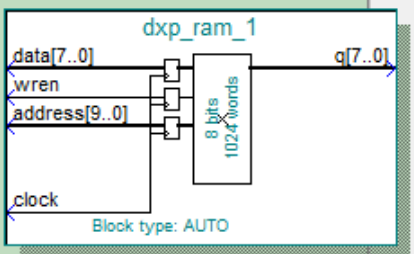
RAM: 1-PORT

About | Documentation

1 Parameter Settings | 2 EDA | 3 Summary

Widths/Blk Type/Clks > Regs/Clken/Byte Enable/Aclrs > Read During Write Option > Mem Init



Which ports should be registered?

- [x] 'data' and 'wren' input ports
- [x] 'address' input port
- [ ] 'q' output port

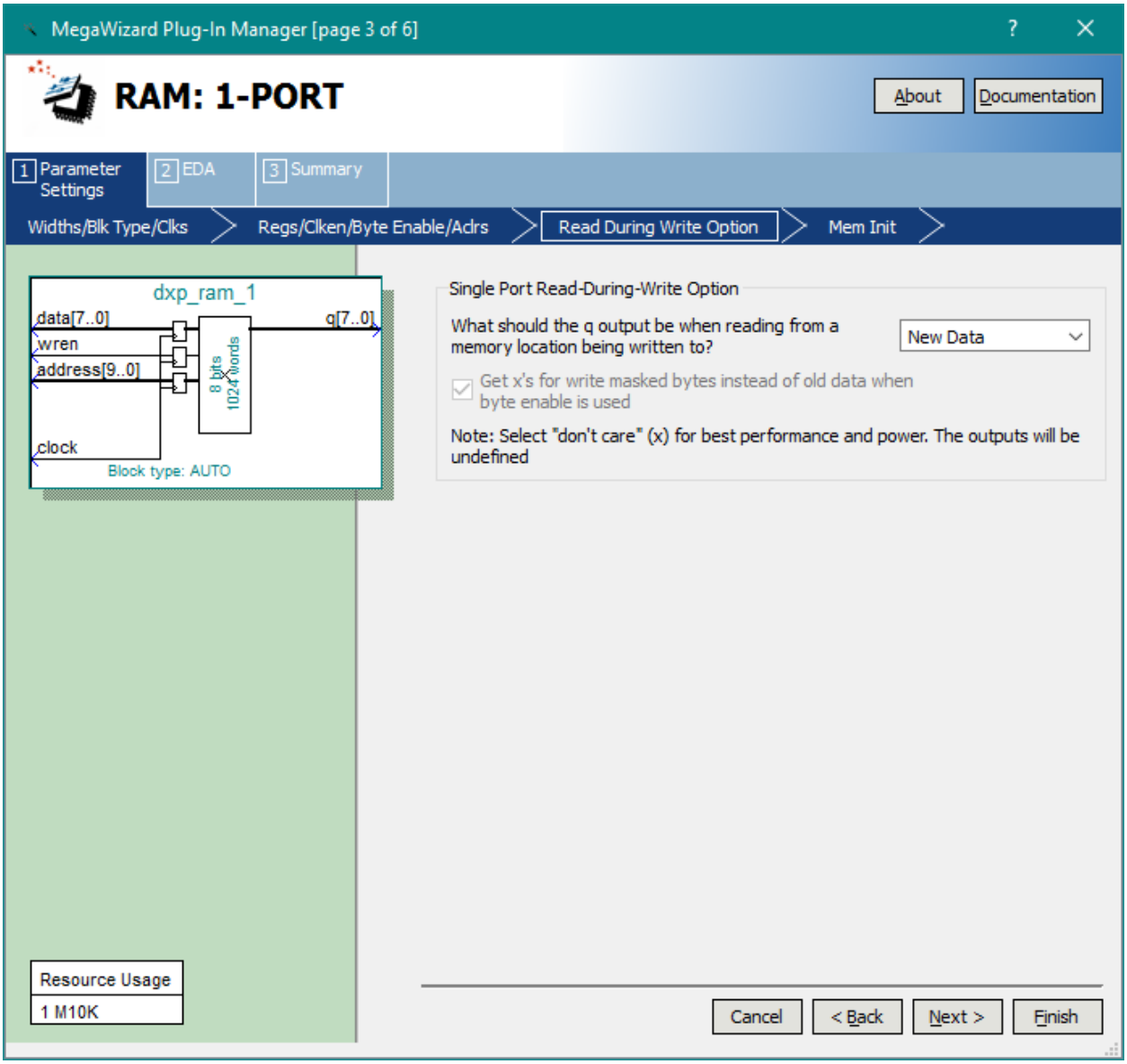
- [ ] Create one clock enable signal for each clock signal. Note: All registered ports are controlled by the enable signal(s) — More Options...
- [ ] Create byte enable for port A

What is the width of a byte for byte enables? 8 bits

- [ ] Create an 'aclr' asynchronous clear for the registered ports — More Options...
- [ ] Create a 'rden' read enable signal

Resource Usage
1 M10K

Cancel | < Back | Next > | Finish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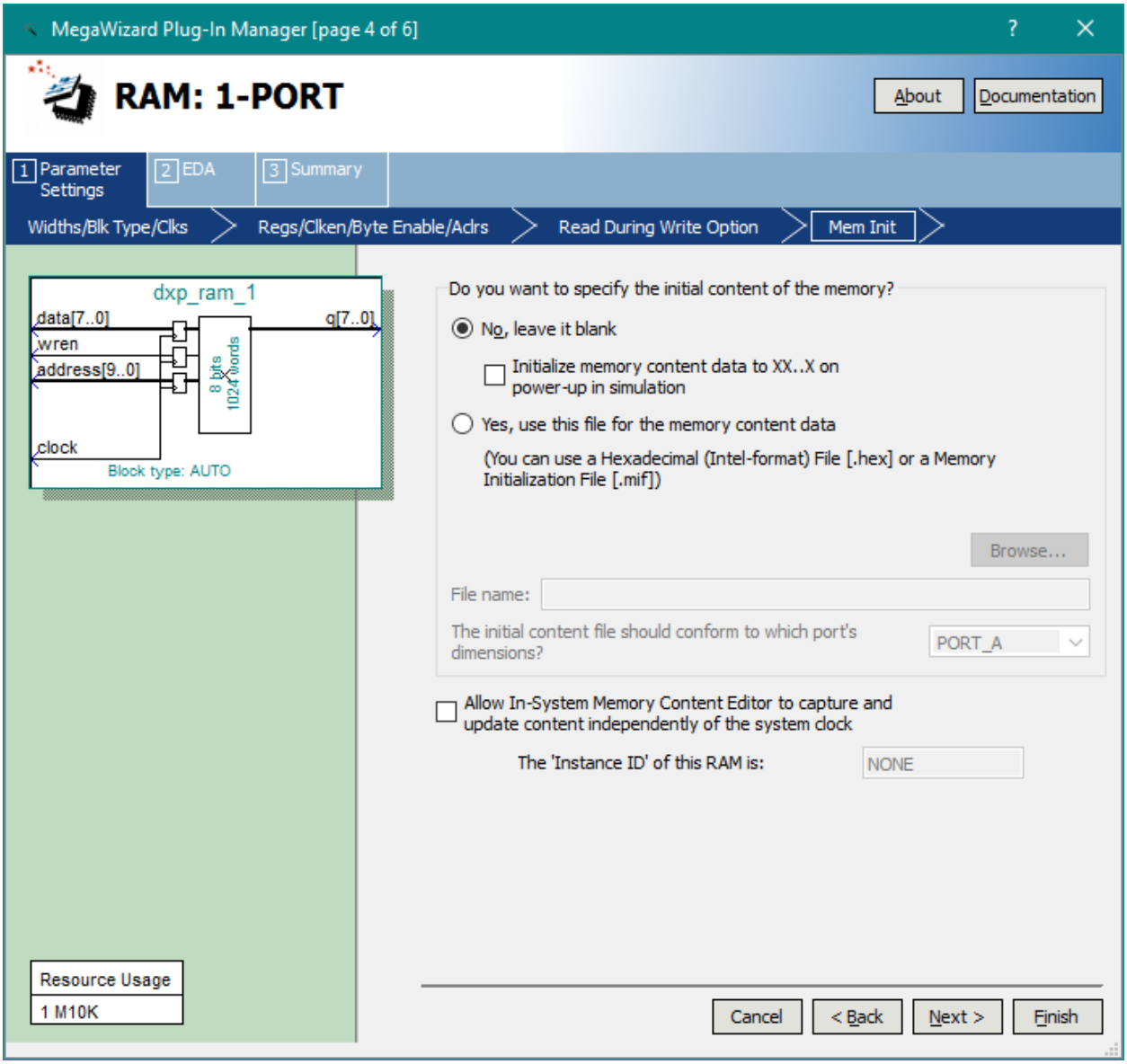
Widths/Blk Type/Clks
Regs/Clken/Byte Enable/Adrs
Read During Write Option
Mem Init
dxp_ram_1
data[7..0]
wren
address[9..0]
clock
q[7..0]
8 bits
1024 words
Block type: AUTO
Single Port Read-During-Write Option
What should the q output be when reading from a memory location being written to?
New Data
Get x's for write masked bytes instead of old data when byte enable is used
Note: Select "don't care" (x) for best performance and power. The outputs will be undefined
Resource Usage
1 M10K
Cancel
< Back
Next >
Finish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Regs/Clken/Byte Enable/Adrs
Read During Write Option
Mem Init
dxp_ram_1
data[7..0]
wren
address[9..0]
clock
q[7..0]
8 bits
1024 words
Block type: AUTO
Do you want to specify the initial content of the memory?
No, leave it blank
Initialize memory content data to XX..X on power-up in simulation
Yes, use this file for the memory content data
(You can use a Hexadecimal (Intel-format) File [.hex] or a Memory Initialization File [.mif])
Browse...
File name:
The initial content file should conform to which port's dimensions?
PORT_A
Allow In-System Memory Content Editor to capture and update content independently of the system clock
The 'Instance ID' of this RAM is:
NONE
Resource Usage
1 M10K
Cancel
< Back
Next >
Finish

MegaWizard Plug-In Manager [page 6 of 6]

RAM: 1-PORT

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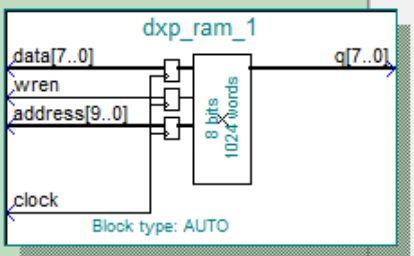


Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.

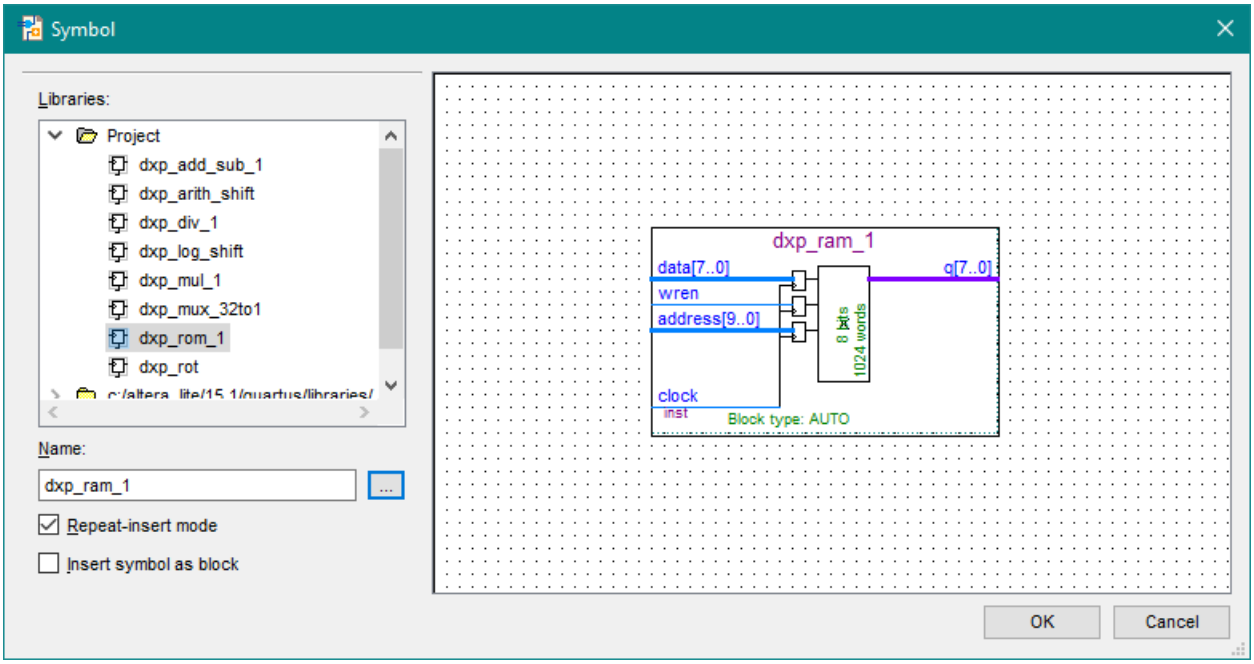
The MegaWizard Plug-In Manager creates the selected files in the following directory:

C:\Users\David\Desktop\dxp_EEEE-521-621-Fa16\

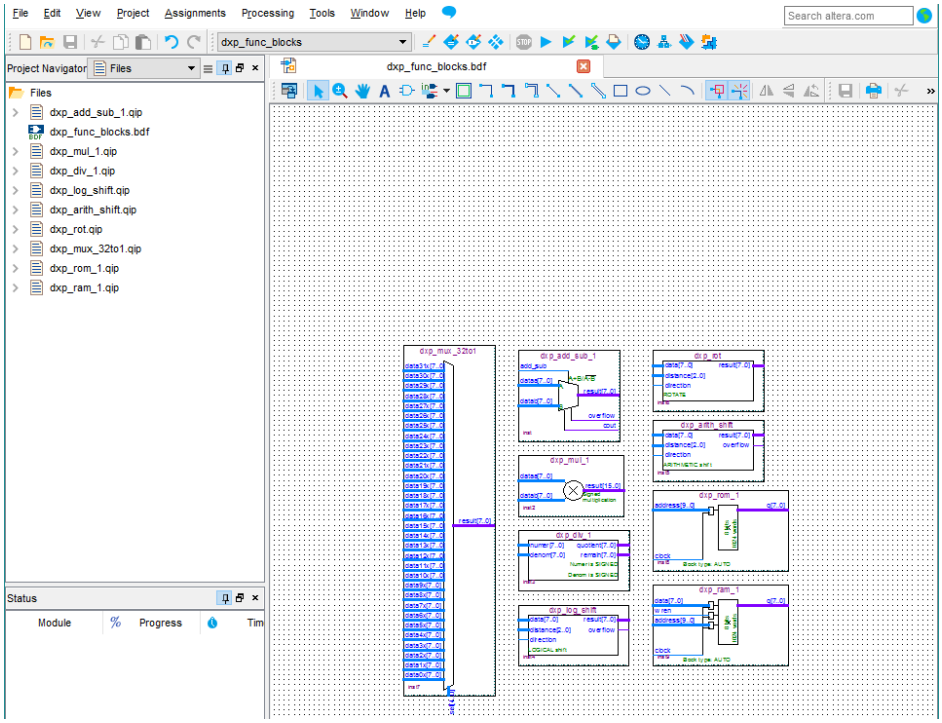
File	Description
☑ dxp_ram_1.vhd	Variation file
☐ dxp_ram_1.inc	AHDL Include file
☑ dxp_ram_1.cmp	VHDL component declaration file
☑ dxp_ram_1.bsf	Quartus Prime symbol file
☐ dxp_ram_1_inst.vhd	Instantiation template file

Resource Usage
1 M10K

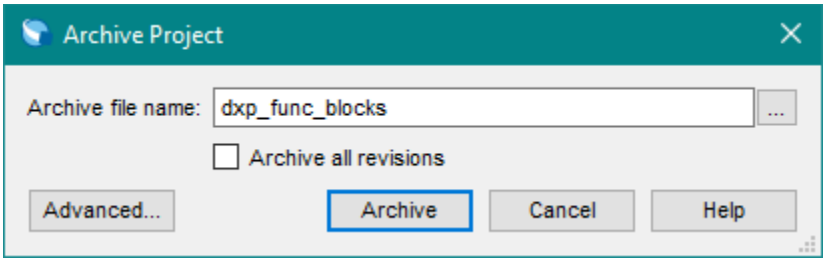
Cancel | < Back | Next > | Finish



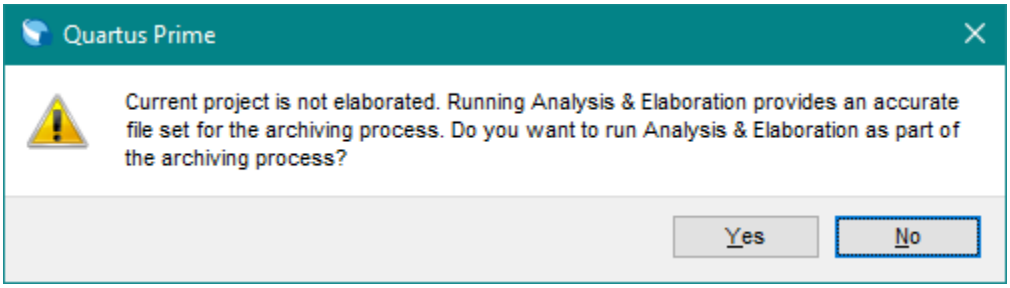
31) You will use these components in later designs. These are synthesized based on Altera intimate knowledge of tis FPGA fabric. Our goal is to evaluate various computer architectures and organizations from a system level point of view. Therefore, we will use the most efficient functional block implementations possible.



32) Take some time to double click and inspect the *.vhd or *.v files. The most important information is that related to the input / output ports. You'll need this when you'll instantiate these components in a higher hierarchical level.
33) Archive the project by running Project > Archive Project.



Choose not to run analysis and synthesis at this time.



34) Show your final schematic to the TA.
35) Close this project.
36) Write your report and upload it along with your project archives in the dropbox on mycourses, as described in the lab policy.
37) This concludes this week's lab.
38) **Grading**:
    a. 3 points for each component created correctly ➔ 3x9=27
    b. 3 points for submitting the report and archived project – the only time points will be given for these two items.