EEEE-521-621-Lab6

1) From mycourses download the following file: dxpRISC521pipe_v.qar or dxpRISC51pipe_vhdl.qar.
2) The goal of this lab is to design and verify the remaining instructions of your fmlRISC521pipe or fmlRISC621pipe. This is the pipelined version of the non-pipelined processor you designed in labs 2 and 3.
3) **Grading**:
    a. 521:
        i. LD, ST (all addressing modes): 2 x 4 = 8 points.
        ii. SWAP and CPY: 2 x 2 = 4 points.
        iii. JMP (all 9 conditions): 2 x 9 = 18 points.
        iv. Total = 30 points.
    b. 621:
        i. LD, ST (all addressing modes): 2 x 4 = 8 points.
        ii. SWAP and CPY: 2 x 2 = 4 points.
        iii. CALL, RET, JMP (all 9 conditions): 3 x 6 = 18 points.
        iv. Total = 30 points.