EEEE-521-621-Lab2

1) From mycourses download the following files: dxpRISC521_rom1.mif and either dxpRISC521_v.qar or dxpRISC51_vhdl.qar.
2) The goal of this lab is to design and verify all manipulation instructions of your fmlRISC521 or fmlRISC621.
3) Open the project archive provided. Analyze and synthesize, and then verify using ModelSimAltera. Except for selecting to view the internal signals, all else is setup for you in this project.
4) The memory initialization file dxpRISC521_rom1.mif contains not only a test sequence for manipulation instructions, but also for transfer and flow control instructions. The latter two categories will be designed and verified during the next lab.
5) Modify the code so that it fits your individual design specifications.
6) For 621 students: you will have to augment the code with all your other manipulation instructions.
7) Both VHDL and Verilog codes are not 100% verified, i.e. the code could be cleaned and some parts written more efficiently. You are allowed and encouraged to change it in any way you see fit.
8) Once all your manipulation instruction cycles are working, archive the project and load it on mycourses along with your report.
9) Time permitting, demo it to the TA. Note: only the TA will assign a grade.
10) This concludes this week's lab.
11) **Grading**:
    a. 521:
        i. ADD, SUB, ADDC, SUBC, NOT, AND, OR: 3 x 7 = 21 points.
        ii. SHRA and ROTRA: 2 x 4 = 8 points.
        iii. Report: 1 point.
        iv. Total = 30 points.
    b. 621:
        i. Currently provided instructions: 1 x 9 = 9 points.
        ii. Additional instructions: 2 x 11 = 22 points.
        iii. Report: 1 point.
        iv. Total possible = 32 points. Total maximum awarded: 30 points. NO bonus points!