factors by inspection:

$$\frac{i_{e8}}{i_{b8}} = \beta_8 + 1$$
$$\frac{i_{b8}}{i_{c7}} = \frac{R_5}{R_5 + R_{i4}}$$
$$\frac{i_{c7}}{i_{b7}} = \beta_7$$
$$\frac{i_{b7}}{i_{c5}} = \frac{R_3}{R_3 + R_{i3}}$$
$$\frac{i_{c5}}{i_{b5}} = \beta_5$$
$$\frac{i_{b5}}{i_{c2}} = \frac{(R_1 + R_2)}{(R_1 + R_2) + R_{i2}}$$
$$\frac{i_{c2}}{i_i} = \beta_2$$

These ratios can be easily evaluated and their values used to determine the voltage gain.

With a little practice, it is possible to carry out such an analysis very quickly, foregoing explicitly labeling the signal currents on the circuit diagram. One simply "walks through" the circuit, from input to output, or vice versa, determining the current-transmission factors one at a time, in a chainlike fashion.

EXERCISE

9.24 Use the values of input resistance found in Example 9.8 to evaluate the seven current-transmission factors and hence the overall current gain and voltage gain.

Ans. The current-transmission factors in the order of their listing are 101, 0.0492, 100, 0.0126, 100, 0.8879, 100 A/A; the overall current gain is 55599 A/A; the voltage gain is 8257 V/V. This value differs slightly from that found in Example 9.8, because of the various approximations made in the example (e.g., $\alpha \simeq 1$).

Summary

- The differential-pair or differential-amplifier configuration is the most widely used building block in analog IC design. The input stage of every op amp is a differential amplifier.
- There are two reasons for preferring differential to single-ended amplifiers: Differential amplifiers are insensitive to interference, and they do not need bypass and coupling capacitors.
- For a MOS (bipolar) pair biased by a current source I, each device operates at a drain (collector, assuming $\alpha = 1$) current of $I/2$ and a corresponding overdrive voltage V_{OV} (no counterpart in bipolar). Each device has $g_m = I/V_{OV}$ ($\alpha I/2V_T$, for bipolar) and $r_o = |V_A|/(I/2)$.
- With the two input terminals connected to a suitable dc voltage V_{CM}, the bias current I of a perfectly symmetrical differential pair divides equally between the

two transistors of the pair, resulting in a zero voltage difference between the two drains (collectors). To steer the current completely to one side of the pair, a difference input voltage v_{id} of at least $\sqrt{2}V_{OV}$ ($4V_T$ for bipolar) is needed.

- Superimposing a differential input signal v_{id} on the dc common-mode input voltage V_{CM} such that $v_{I1} = V_{CM} + v_{id}/2$ and $v_{I2} = V_{CM} - v_{id}/2$ causes a virtual signal ground to appear on the common-source (common-emitter) connection. In response to v_{id}, the current in Q_1 increases by $g_m v_{id}/2$ and the current in Q_2 decreases by $g_m v_{id}/2$. Thus, voltage signals of $\pm g_m(R_D \| r_o) v_{id}/2$ develop at the two drains (collectors, with R_D replaced by R_C). If the output voltage is taken single-endedly, that is, between one of the drains (collectors) and ground, a differential gain of $\frac{1}{2}g_m(R_D \| r_o)$ is realized. When the output is taken differentially, that is, between the two drains (collectors), the differential gain realized is twice as large: $g_m(R_D \| r_o)$.
- The analysis of a differential amplifier to determine differential gain, differential input resistance, frequency response of differential gain, and so on is facilitated by employing the differential half-circuit, which is a common-source (common-emitter) transistor biased at $I/2$.
- An input common-mode signal v_{icm} gives rise to drain (collector) voltage signals that are ideally equal and given by $-v_{icm}(R_D/2R_{SS})$[$-v_{icm}(R_C/2R_{EE})$ for the bipolar pair], where R_{SS} (R_{EE}) is the output resistance of the current source that supplies the bias current I. When the output is taken single-endedly, a common-mode gain of magnitude $|A_{cm}| = R_D/2R_{SS}$ ($R_C/2R_{EE}$ for the bipolar case) results. Taking the output differentially results, in the perfectly matched case, in zero A_{cm} (infinite CMRR). Mismatches between the two sides of the pair make A_{cm} finite even when the output is taken differentially: A mismatch ΔR_D causes $|A_{cm}| = (R_D/2R_{SS})(\Delta R_D/R_D)$; a mismatch Δg_m causes $|A_{cm}| = (R_D/2R_{SS})(\Delta g_m/g_m)$. Corresponding expressions apply for the bipolar pair.
- While the input differential resistance R_{id} of the MOS pair is infinite, that for the bipolar pair is only $2r_\pi$ but can be increased to $2(\beta+1)(r_e + R_e)$ by including resistances R_e in the two emitters. The latter action, however, lowers A_d.
- Mismatches between the two sides of a differential pair result in a differential dc output voltage V_O even when the two input terminals are tied together and connected to a dc voltage V_{CM}. This signifies the presence of an input offset voltage $V_{OS} \equiv V_O/A_d$. In a MOS pair there are three main sources for V_{OS}:

$$\Delta R_D \Rightarrow V_{OS} = \frac{V_{OV}}{2}\frac{\Delta R_D}{R_D}$$

$$\Delta(W/L) \Rightarrow V_{OS} = \frac{V_{OV}}{2}\frac{\Delta(W/L)}{W/L}$$

$$\Delta V_t \Rightarrow V_{OS} = \Delta V_t$$

For the bipolar pair there are two main sources:

$$\Delta R_C \Rightarrow V_{OS} = V_T\frac{\Delta R_C}{R_C}$$

$$\Delta I_S \Rightarrow V_{OS} = V_T\frac{\Delta I_S}{I_S}$$

- A popular circuit in both MOS and bipolar analog ICs is the current-mirror-loaded differential pair. It realizes a high differential gain $A_d = g_m(R_{o\ \text{pair}} \| R_{o\ \text{mirror}})$ and a low common-mode gain, $|A_{cm}| = 1/2g_{m3}R_{SS}$ for the MOS circuit ($r_{o4}/\beta_3 R_{EE}$ for the bipolar circuit), as well as performing the differential-to-single-ended conversion with no loss of gain.
- The CMOS two-stage amplifier studied in Section 9.6.1 is intended for use as part of an IC system and thus is required to drive only small capacitive loads. Therefore it does not have an output stage with a low output resistance.
- A multistage amplifier typically consists of three or more stages: an input stage having a high input resistance, a reasonably high gain, and, if differential, a high CMRR; one or two intermediate stages that realize the bulk of the gain; and an output stage having a low output resistance. In designing and analyzing a multistage amplifier, the loading effect of each stage on the one that precedes it must be taken into account.