9/16/2016

Chapter 5 - MOSFETS

→ In this chapter:

1- The physical structure of MOS transistors and how it works

2- How voltage between two terminals of transistor controls the current.

3- How to analyze and design circuits with MOS transistors, resistors and DC sources

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Intro:

3-terminal devices (MOSFETs, BJT's) → voltage between 2 terminals control current in third.

MOSFETs (actually a 4-T device)
- Analog circuits → amplifiers, filters, rectifiers, regulators . . .
- Digital circuits → logic.

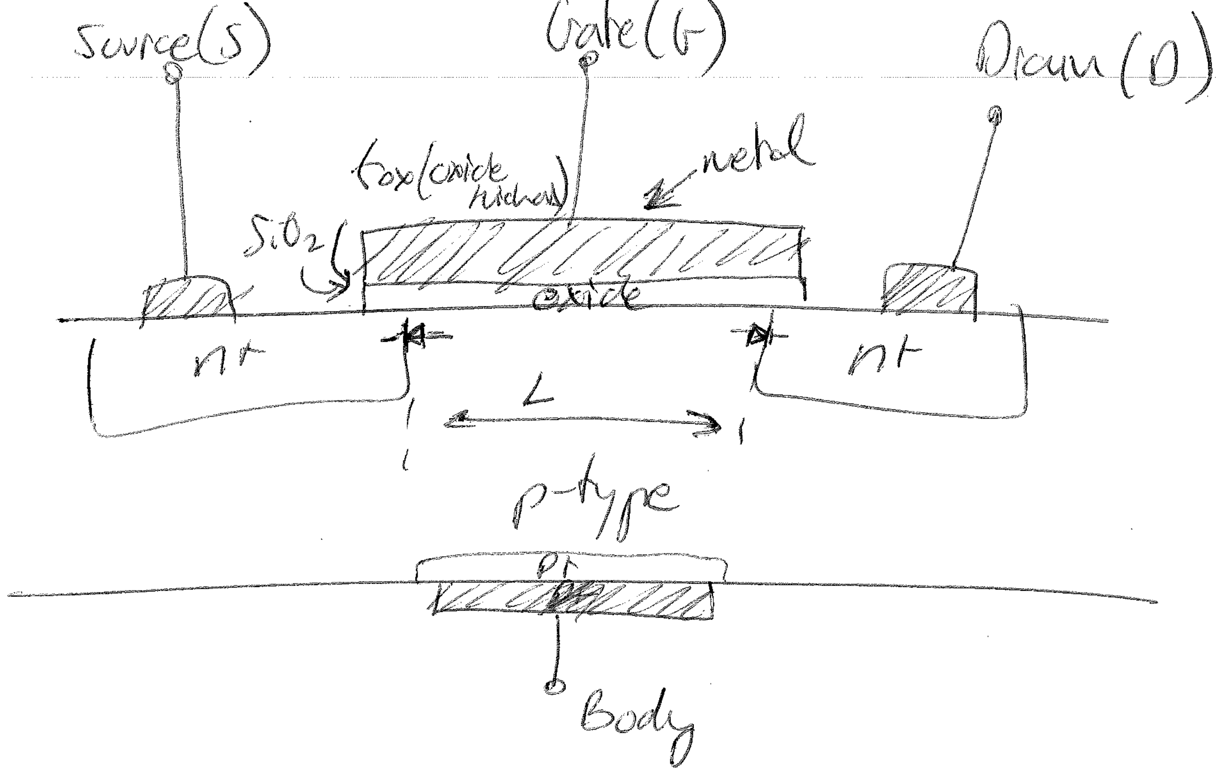
BJT's
- Analog.

5.1 - Device structure and physical operation.

Metal Oxide Semiconductor Field Effect Trans'.

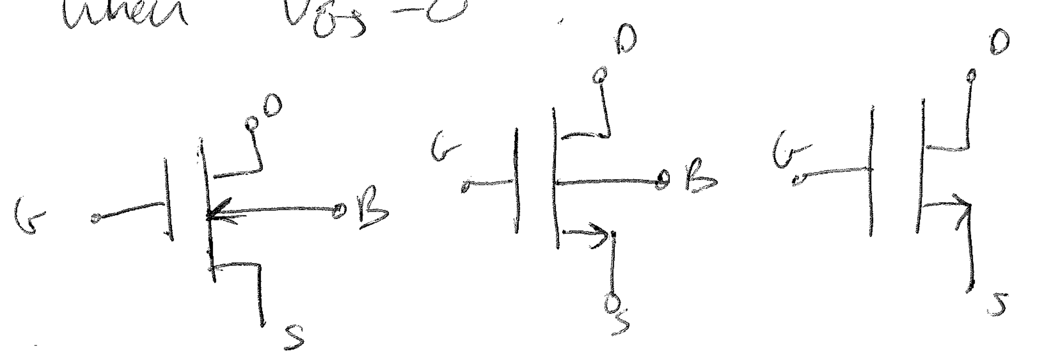
MOSFET

→ Enhancement mode → most popular.



→ Generally source and Body are connected together to ensure $V_D > V_B$ (PN diodes are shut off))

→ Back to back diodes prevent current when $V_{GS} \leq 0$



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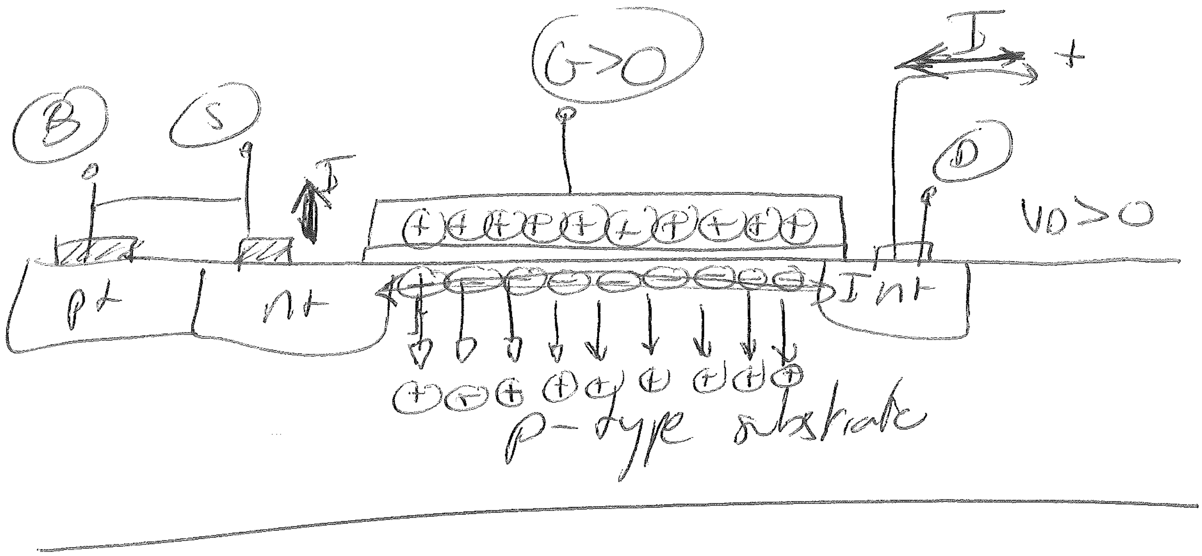
5.1.3 Creating a channel for current flow.



→ n-channel MOSFET or NMOS transistor.

→ NMOS ~~A~~ is formed in p-type substrates.
The channel is created by inverting the substrate surface from p to n-type.
The induced channel → inversion layer.
→ enhances the channel.

→ Value for which V_{GS} is sufficient to invert the surface is called the threshold voltage → V_t (0.3 → 1.0V)
$\neq V_T$ (thermal voltage of diode)

→ Field effect by charge on gate.
~~enhances~~

→ At $V_{GS} = V_t$ → voltage on channel is just inverted and equal to 0. Higher voltages will affect the ~~width~~ depth of inversion layer.

$V_{ov} = V_{GS} - V_t$

→ over-drive voltage (voltage of ~~V_{GS}~~ V_{GS} higher than V_t

→ Charge in channel:

$$|Q| = C_{ox}(W \cdot L) v_{ov}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$\epsilon_{ox} = 3.9 \cdot \epsilon_0 = 3.9 \cdot 8.854 \times 10^{-12} \ F/m = 3.45 \times 10^{-11} \ F/m$$

for typical $t_{ox} \simeq 4nm$

$$C_{ox} = \frac{3.45 \times 10^{-11} \ F/m}{4 \times 10^{-9} \ m} = 8.6 \times 10^{-3} \ F/m^2$$

$$\downarrow$$

$$8.6 \times 10^{-15} \ F/\mu m^2$$

$$8.6 \times 10 \ fF/\mu m^2$$

typical $W = 0.78\mu m$ $L = 0.18\mu m$

$$C = C_{ox} \frac{W}{L} = 8.6 \ fF/\mu m^2 \cdot 0.78\mu m \cdot 0.18\mu m$$

$$\boxed{C = 1.1 \ fF}$$

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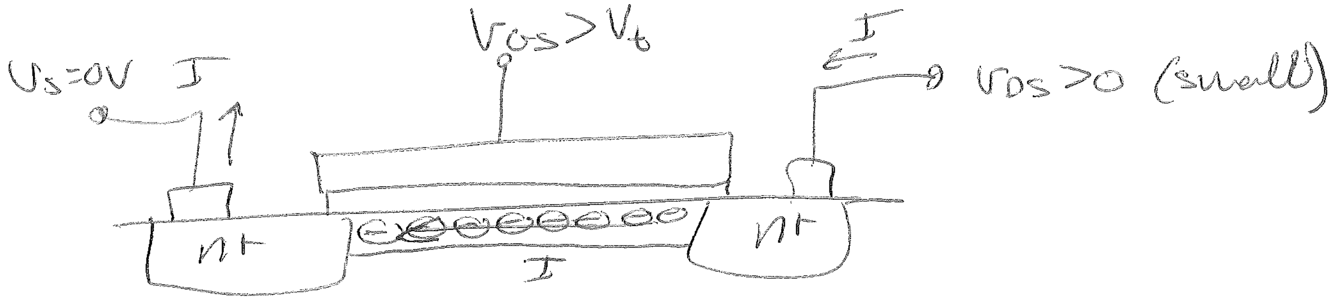
5.1.4. Applying a small V_{DS}.



→ current is opposite of direction of electrons. (negative charges)

→ electrons move from ⊖ to ⊕
→ current flows from ⊕ to ⊖.
→ current goes from drain to source (source is source of electrons).

→ since V_{DS} is small voltage on channel is $V_{OV} = V_{GS} - V_t$

$$\frac{Q}{\text{unit length}} = C_{ox} W \cdot V_{OV}$$

V_{DS} lead to E field $= \frac{V_{DS}}{L}$

Electron drift velocity $= \mu_n |E| = \mu_n \frac{V_{DS}}{L}$

μ_n → electron mobility.

$$i_D = \text{charge} \times \text{drift velocity} = \left[(\mu_n C_{ox}) \left(\frac{W}{L} \right) V_{OV} \right] \cdot V_{DS}$$

$\therefore \quad v_{OV} = v_{GS} - V_t$

$$i_D = \left[(\mu_n C_{ox}) \left(\frac{W}{L} \right) (v_{GS} - V_t) \right] v_{DS}$$

linear equation depends on value of v_{GS} and v_{DS}.

conductance of channel $\left(\frac{1}{\text{Resistance}} \right)$ $\quad g_{DS} = \frac{1}{r_{DS}}$

$$g_{DS} = (\mu_n C_{ox}) \left(\frac{W}{L} \right) (v_{GS} - V_t)$$

$\mu_n C_{ox} \rightarrow$ process technology $\quad \boxed{k'_n = \mu_n C_{ox}}$

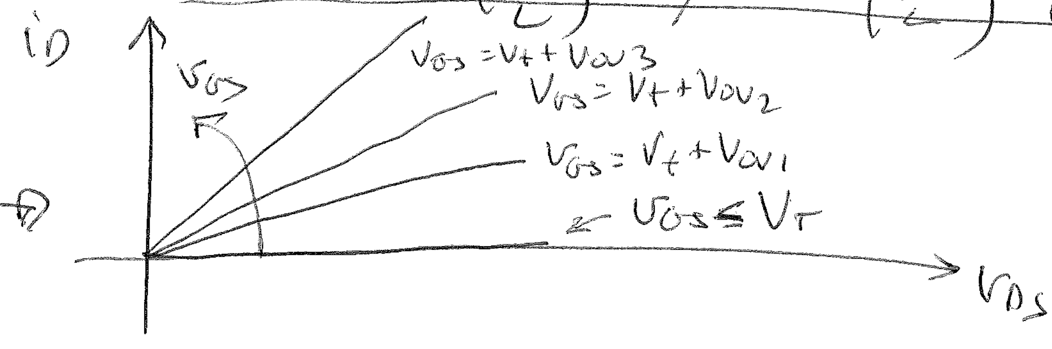
process transconductance parameter. $\left[\frac{m^2}{V \cdot s} \right]$

$k'_n \rightarrow \left[\frac{A}{V^2} \right]$ $\qquad \left[\frac{F}{m^2} \right]$

$\frac{W}{L} \rightarrow$ designer chosen for Lmh.

MOSFET transconductance parameter k_n

$$\underline{k_n \equiv k'_n \left(\frac{W}{L} \right) = \mu_n C_{ox} \left(\frac{W}{L} \right) \quad \left[\frac{A}{V^2} \right]}$$



lec 11 ↑
lec 12 ↓

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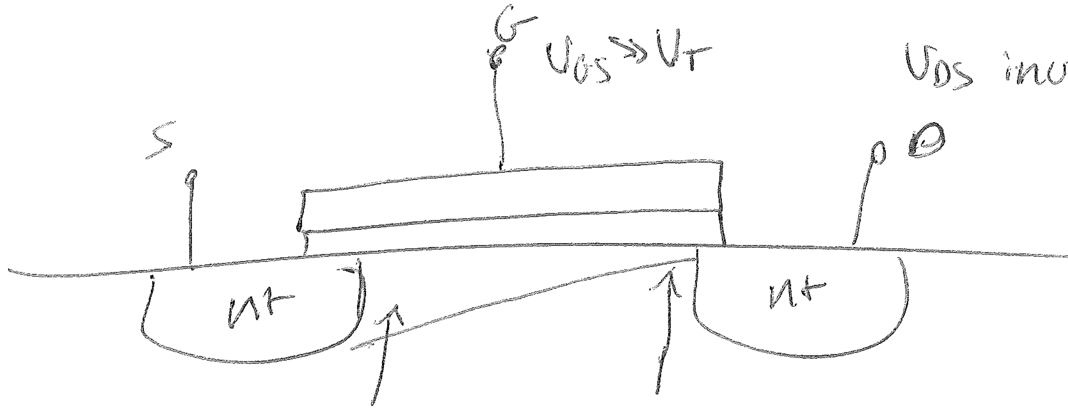
Electronics 1.

5.1.5 Operation as V_{DS} is increased:

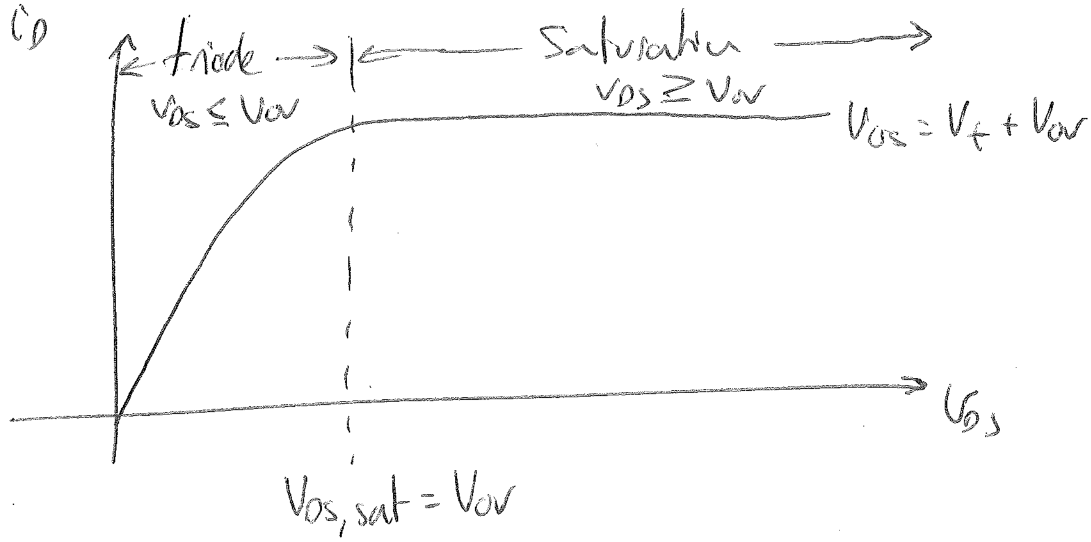
$V_{ov} = V_{GS} - V_T$

V_{DS} increases.



Channel voltage = $V_t + V_{ov}$
source side

$V_t + V_{ov} - V_{DS}$
drain side.



$$i_D = k'_n\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \quad \text{for } V_{DS} < V_{GS} - V_t$$

$v_{DS} < V_{ov}$

5.1.6 Operation for $v_{DS} \geq V_{ov}$; channel pinch-off and current saturation.

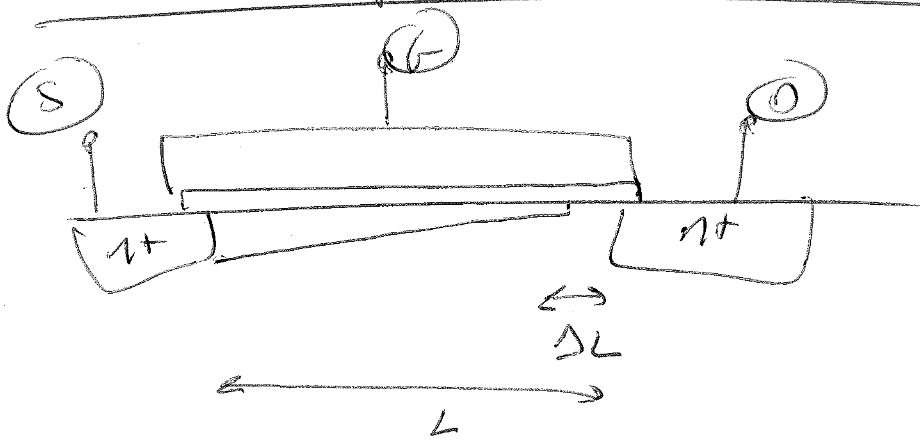
→ When $v_{DS} \geq V_{ov}$ $\quad v_{DS} \geq V_{GS} - V_T$, $v_{GD} = V_t$

and channel depth is zero at drain end. Channel is pinched off → current saturates.

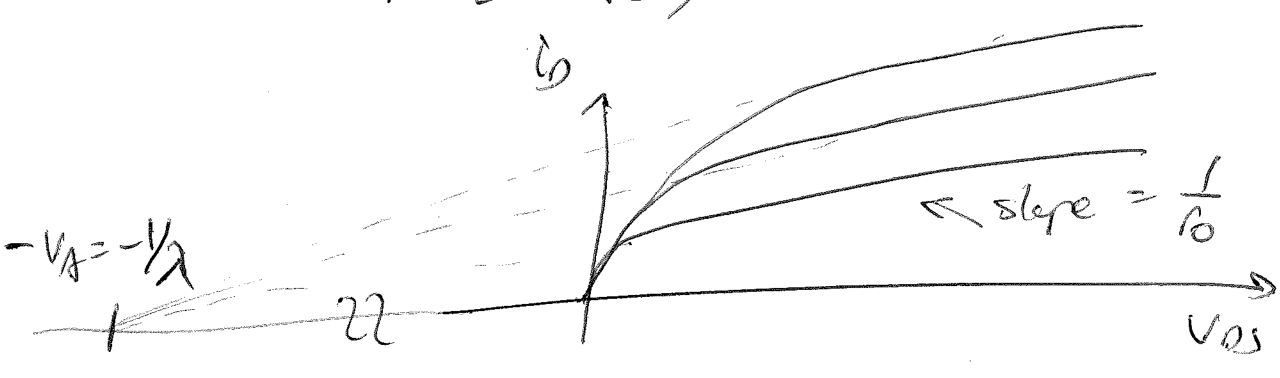
$$V_{DS,sat} = V_{ov} = V_{GS} - V_t$$

$$i_{D_{sat}} = \frac{1}{2} k'n \left(\frac{W}{L}\right) (v_{GS} - V_t)^2$$

5.2.4 Finite output resistance in saturation.



$$i_{D,sat} = \frac{1}{2} k'n \left(\frac{W}{L}\right) (v_{GS} - V_t)^2 (1 + \lambda v_{DS})$$



cont'd

r_o cont's

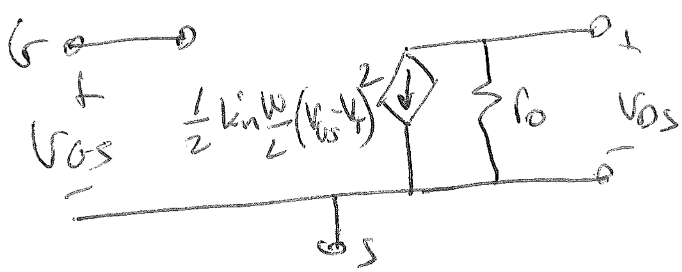
$$r_o = \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}\ \text{constant}}$$

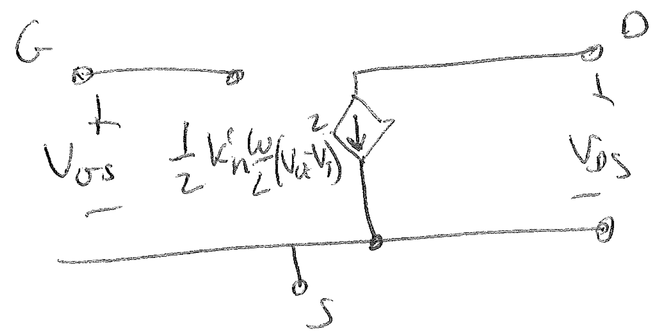
$$r_o = \left[\lambda \frac{k'_n}{2}\frac{W}{L}(V_{GS}-V_{TN})^2\right]^{-1}$$

$$r_o = \frac{1}{\lambda I_D} \quad \text{OR} \quad r_o = \frac{V_A}{I'_D}$$

where $I'_D = \frac{1}{2}k'_n\frac{W}{L}(V_{GS}-V_{TN})^2$

Large signal equivalent-circuit model.





w/ r_o

w/o r_o

ex NMOS fabricated w/ 0.18-μm process w/ $L = 0.18\,\mu m$

$W = 2\,\mu m$. $C_{ox} = 8.6\ fF/\mu m^2$ $\mu_n = 450\ cm^2/V\cdot s$

$V_{tn} = 0.5V$.

→ Find V_{GS} and V_{DS} to operate MOSFET at edge of saturation with $I_D = 100\,\mu A$.

* First find process transconductance k_n'

$$k_n' = \mu_n C_{ox} = (450\ cm^2/V\cdot s)(8.6\times10^{-15}\ \frac{F}{\mu m^2}) = 387\,\mu A/V^2$$

5.4 Body effect - Role of substrate.

Effect of V_{SB} on the channel can be represented as a change in threshold voltage V_t.

$$V_t = V_{t0} + \gamma\left[\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right]$$

V_{t0} = threshold voltage for $V_{SB} = 0$

ϕ_F = physical parameter → $2\phi_F = 0.6V$

$$\gamma = \frac{\sqrt{2qN_A\epsilon_s}}{C_{ox}}$$

$q = 1.6\times10^{-19}\ C$

N_A - doping concentration

$\epsilon_{si} = 1.04\times10^{-12}\ F/cm$

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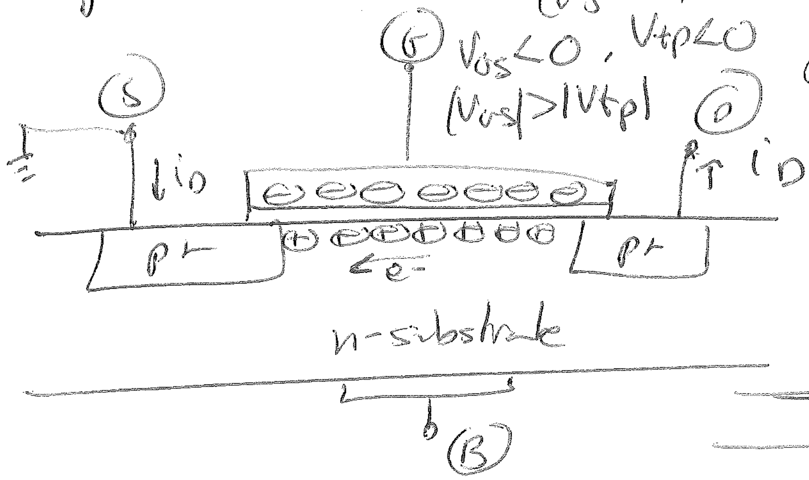
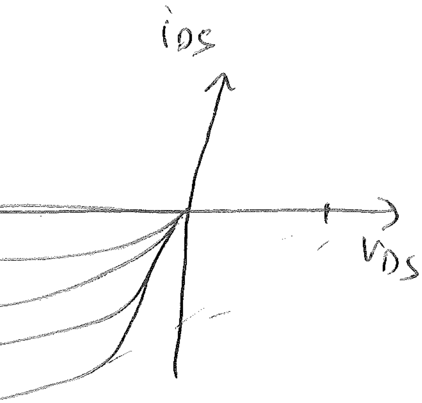
5.1.7. The p-channel MOSFET.





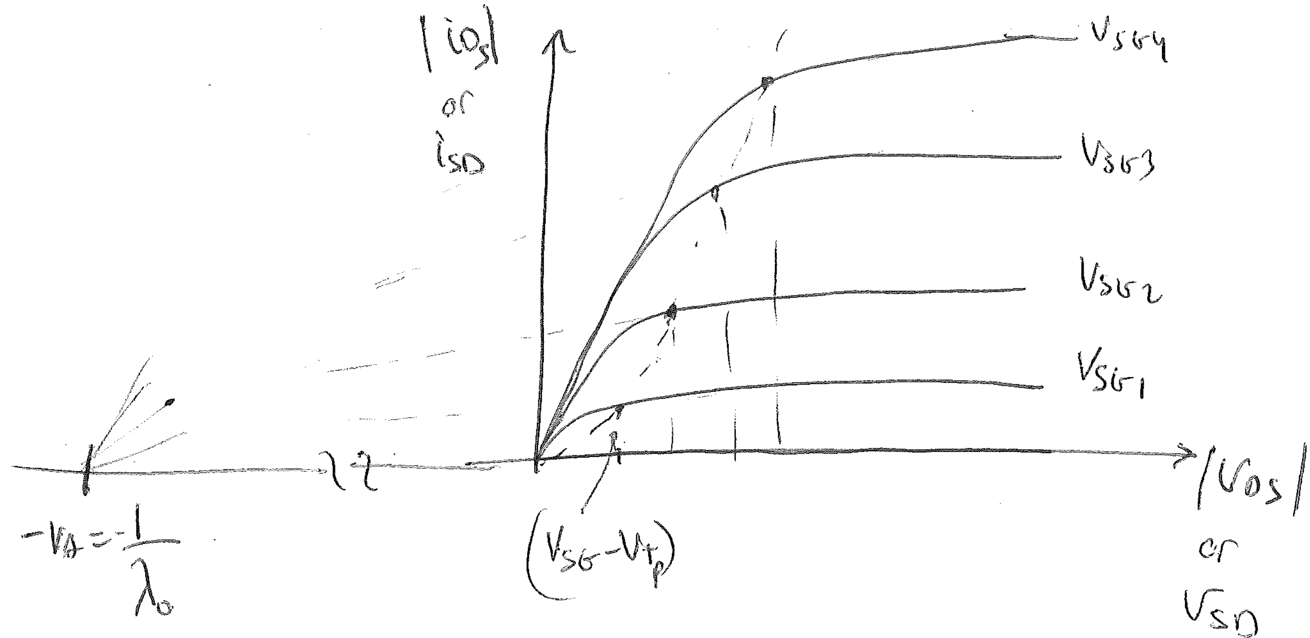
Avoid dealing w/ negative signs.

To meet channel $|V_{GS}| \geq |V_{tp}|$

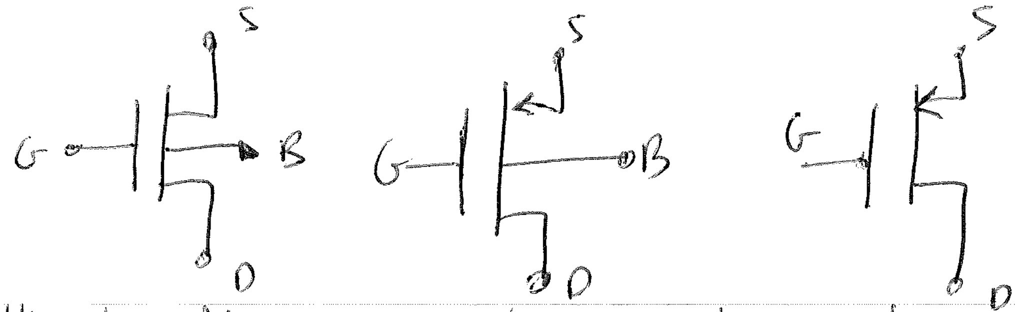
PMOS $k_p' = \mu_p C_{ox}$ $(\mu_p < \mu_n)$

$\mu_p = \frac{1}{4}$ to $\frac{1}{2}\mu_n$

Transistor transconductance parameter: $k_p = k_p'\left(\frac{W}{L}\right) = \mu_p C_{ox}\frac{W}{L}$



→ PMOS symbols and conventions:



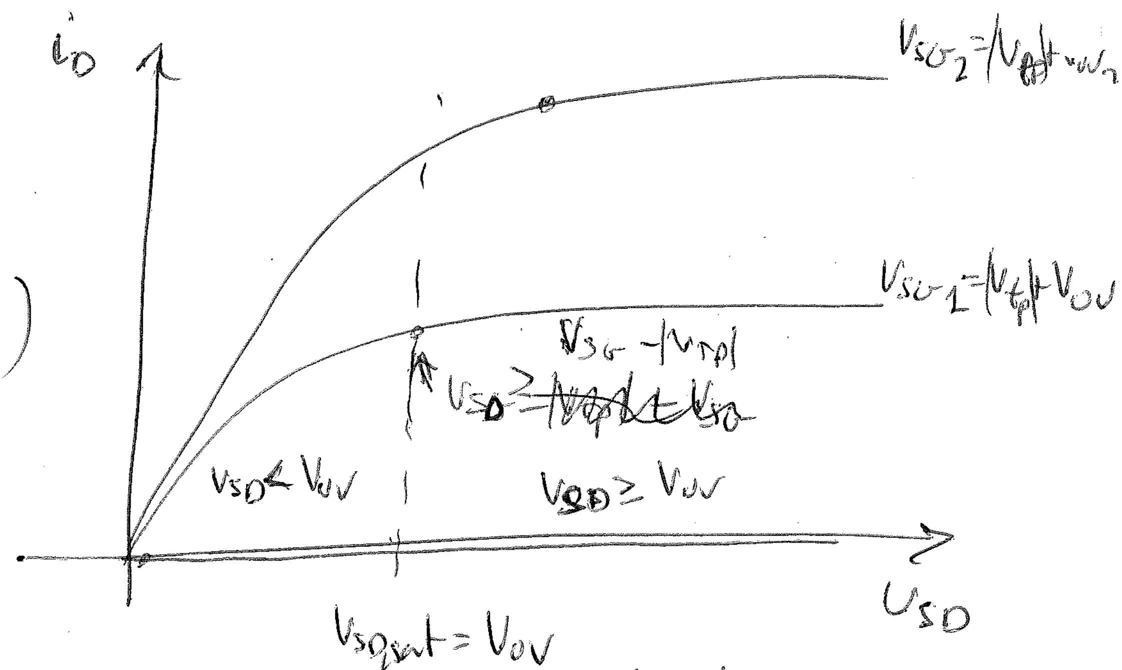
→ Although V_{tp} is negative, write as $|V_{tp}|$

→ Generally draw p-channel devices with their sources on top so current flows from top to bottom.

→ Write voltage w/ respect to drain to make them positive and simplify analysis.

→ Therefore

$v_{OV} = (v_{SG} - |V_{tp}|)$



Triode region

$v_{SD} < v_{SG} - |V_{tp}|$

$$i_D = k_p'\left(\frac{W}{L}\right)\left[(v_{SG} - |V_{tp}|)v_{SD} - \frac{1}{2}v_{SD}^2\right]$$

Saturation region.

$v_{SD} \geq v_{SG} - |V_{tp}|$

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(v_{SG} - |V_{tp}|)^2$$

Example 8.2 $\qquad$ 9/23/2016 ②

NMOS $\quad L = 0.18\,\mu m,\ W = 2\,\mu m$

$C_{ox} = 8.6\ fF/\mu m^2,\ \mu_n = 450\ cm^2/V\cdot s,\ V_{tn} = 0.5V$

a) Find V_{GS} and V_{DS} at edge of saturation when $I_D = 100\,\mu A$.

→ First find k_n' (process transconductance parameter).

$$k_n' = \mu_n C_{ox} = 450\ \frac{cm^2}{V\cdot s} \cdot 8.6\,fF/\mu m^2$$

$cm^2 \rightarrow 1\times10^{-4}\ m^2$

~~$450\,cm^2 \rightarrow 450\times10^{-4}\ m^2$~~

$\mu m^2 \rightarrow 1\times10^{-12}\ m^2$

$$450\times10^{-4}\ \frac{m^2}{V\cdot s}\ 8.6\times10^{-15} / 1\times10^{-12}\ m^2$$

$$k_n' = 387\times10^{-6}\ A/V^2$$

→ Find transistor transconductance:

$$k_n = k_n'\left(\frac{W}{L}\right) = 387\times10^{-6}\ A/V^2 \left(\frac{2\,\mu m}{0.18\,\mu m}\right) = 4.3\ mA/V^2$$

$4.3\times10^{-3}\ A/V^2$

→ Use saturation equation

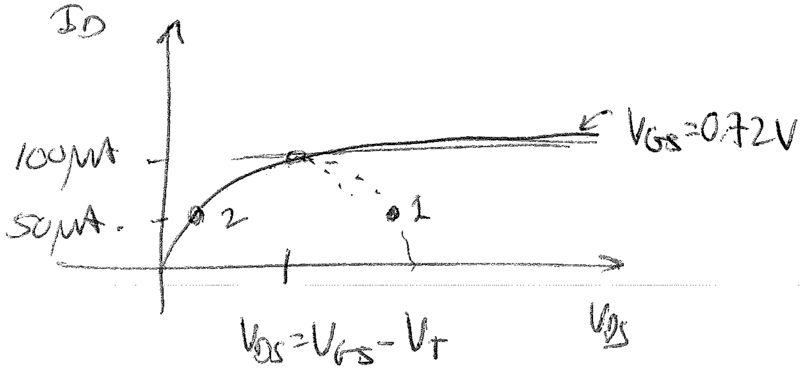
$$I_{D_{sat}} = \frac{1}{2}k_n(V_{GS}-V_T)^2 \qquad V_{GS}-V_T = V_{OV}$$

$$100\,\mu A = \frac{1}{2}(4.3\times10^{-3})\frac{A}{V^2}(V_{OV})^2$$

$$V_{OV}^2 = (V_{GS}-V_T)^2 = 46\ mV \rightarrow V_{OV} = V_{GS}-V_T = 0.22\ V = \sqrt{0.046}$$

$$\therefore\ V_{GS} = 0.22 + 0.5 = 0.72V.$$

(b) ~~Find~~ If V_{GS} is kept constant find V_{DS} for $I_D = 50\mu A$.



$V_{DS} = V_{GS} - V_T$

$V_{DS_{sat}} = 0.72 - 0.5 = 0.22V$

I_D in triode region (parabollic region)

$$I_D = k_n\left[(V_{GS}-V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$50\times10^{-6}A = 4.3\times10^{-3}\frac{A}{V^2}\left[(0.72-0.5)(V_{DS}) - \frac{1}{2}V_{DS}^2\right]$$

$$\frac{50\times10^{-6}\cancel{A}}{4.3\times10^{-3}\cancel{A}/V^2} = 0.22V_{DS} - 0.5V_{DS}^2$$

$$0.5V_{DS}^2 - 0.22V_{DS} + 0.011 = 0$$

$$V_{DS} = \frac{-b \pm \sqrt{b^2-4ac}}{2a}$$

$$V_{DS_1} = \frac{0.22 + \sqrt{(0.22)^2 - 4(0.5\cdot0.011)}}{2\cdot(0.5)} = 0.39V$$

$$V_{DS_2} = \frac{0.22 - \sqrt{(0.22)^2 - 4(0.5)(0.011)}}{2(0.5)} = 0.06V$$

$V_{DS_1} > V_{DS,sat}$ (not possible for this case)

$V_{DS_2} = 0.06V \leftarrow$ correct answer.

lec 13 ↑

lec 14 ↓

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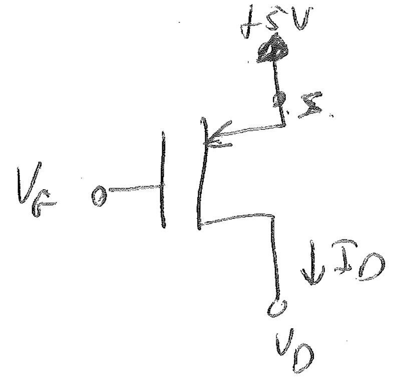
(3)

5.7 PMOS transistor $V_{tp} = -1V$, $k'_p = 60\,\mu A/V^2$

$\frac{W}{L} = 10$



a) Find V_G range for which transistor conducts.

when ~~V_{GS}~~ $V_{SG} \geq |V_{tp}| = 1V$

$\Rightarrow V_G \leq 5-1 = 4V$

$V_G \leq 4V$ $\qquad V_{SG} \geq 1V$

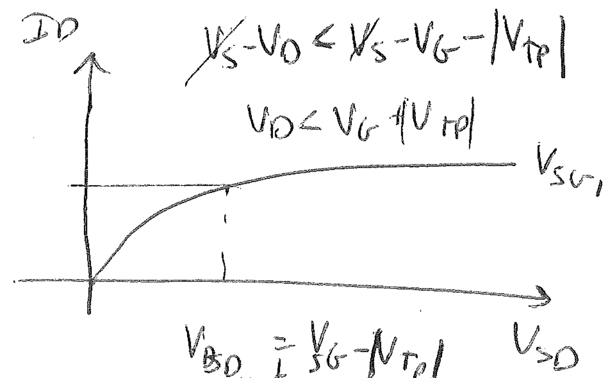
b) ~~In terms of V_G, find the range of V_D for triode (parabolic) operation.~~

~~Triode when $V_{GD} \geq |V_{tp}| = 1V$~~

~~$\Rightarrow V_D \geq V_G + 1$~~

$\cancel{V_S} - V_D < \cancel{V_S} - V_G - |V_{TP}|$

$V_D < V_G + |V_{TP}|$



c) ~~For saturation.~~

~~$V_{DG} \leq |V_{tp}| = 1V$~~

~~$\Rightarrow V_D \leq V_G + 1$~~

~~$V_{SD} < V_{SG} - |V_{Tp}|$~~ $\qquad$ ~~$V_{SD} > V_{SG} - V_{TP}$~~

~~$V_D < V_G |V_{Tp}|$~~ $\qquad$ ~~$V_D > V_G - V_{TP}$~~

~~$V_{DG} > |V_{TP}|$~~ $\qquad$ ~~$V_{DG} < |V_{TP}|$~~

~~$V_G < V_D + 1$~~

d) Assuming $\lambda = 0$, find values of $|V_{ov}|$ and V_G and range of V_D to operate in sat $I_{D_{sat}} = 75\,\mu A$

$$I_D = \frac{1}{2} k'_p \frac{W}{L} \left(V_{SG} - |V_{Tp}|\right)^2$$

$$75 \times 10^{-6} A = \frac{1}{2}\, 60 \times 10^{-6} \frac{A}{V^2} (10) \left(V_{SG} - |V_{tp}|\right)^2$$

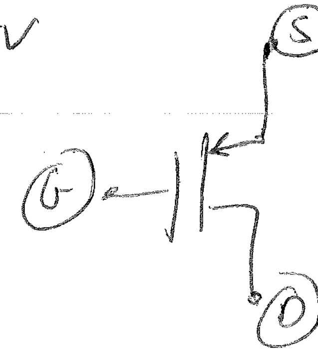
$$\left(V_{SG} - V_T\right)^2 = 0.25V \qquad \left(V_{SG} - V_T\right) = 0.5\,V$$

$\therefore \quad V_{SG} - |V_{Tp}| = 0.5V = |V_{ov}|$

$V_{SG} = 0.5V + |V_{Tp}| = 1.5V$

$\Rightarrow \quad V_{SG} = V_S - V_G \quad \rightarrow \quad V_G = V_S - V_{SG} = 5V - 1.5V = 3.5V$

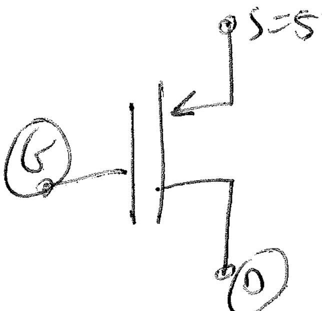
$V_D \leq V_G + 1 = 4.5V \qquad V_D \leq 4.5V$



(e) If $\lambda = -0.02V^{-1}$, find r_o at $|V_{ov}| = 0.5V = |V_{SG} - |V_{Tp}||$

$$r_o = \frac{1}{|\lambda| I_D} = \frac{1}{|0.02|(75\times10^{-6}A)} = 667k\Omega$$

(f) Find I_D at $V_{ov} = 0.5V$ ($V_{SG} - V_T = 0.5V$) with $\lambda = -0.02V^{-1}$, at $V_D = 3V$



$$I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)|V_{ov}|^2(1+|\lambda||V_{SD}|)$$

$V_{SD} = V_S - V_D$

$V_{SD} = 5V - 3V$

$V_{SD} = 2V$

$$I_D = (75\mu A)(1 + (0.02V^{-1})(2V))$$

$$\boxed{I_D = 75\times10^{-6} \times 1.04 = 78\times10^{-6}\ \text{Amp}}$$

$V_{SD} = 2V$

$V_{SD} = V_S - V_D = 5V$

5.3 MOSFET CIRCUITS AT DC.

→ Quick DC analysis:
→ Generally neglect channel-length modulation

→ $V_{OV} = V_{GS} - V_{tn}$ → NMOS

$V_{OV} = V_{SG} - |V_{tp}|$ → PMOS

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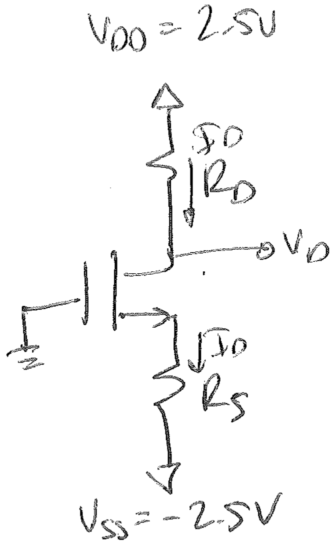
ex. 5.3



Find R_D and R_S for transistor $I_D = 0.4$ mA and $V_D = 0.5V$. NMOS $V_{tn} = 0.7V$
$\mu_n C_{ox} = 100 \mu A/V^2$, $L = 1\mu m$, $W = 32\mu m$. $\lambda = 0$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{(2.5 - 0.5)V}{0.4 \times 10^{-3} A}$$

$R_D = 5 \times 10^3 \Omega$.

→ Need V_s to find R_s.

Since $V_D = 0.5 > V_G$ $(V_G = 0V)$. ~~V_{DS}~~ Assume saturation

$V_{DS} \geq (V_{GS} - V_T)$
sat

And $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \underbrace{(V_{GS} - V_T)^2}_{(V_{OV})^2}$

$0.4 \times 10^{-3} = \frac{1}{2} 100 \times 10^{-6} A/V^2 \left(\frac{32}{1}\right) V_{OV}^2$

$V_{OV} = 0.5V$ $\quad (V_{GS} - V_T) = 0.5V$

$V_{GS} = 1.2V$

$\underset{0V}{V_G} - V_s = 1.2V$

$V_G - V_S - V_T = 0.5$

$0V - V_S - 0.7 = 0.5$

$\boxed{V_S = -1.2V}$

If $V_S = -1.2V$ then

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-1.2 - (-2.5)\,V}{0.4mA}$$

$$\boxed{R_S = 3.25\,k\Omega}$$

HW #3

5.18, 5.19, 5.27, 5.38, 5.39, 5.44, 5.45

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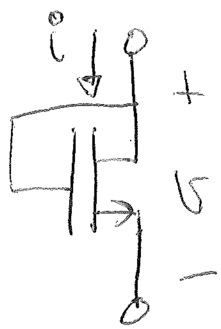
→ Diode-connected transistor

$V_{DS} = V_{GS} - V_t$

ex. 5.4 (pg 278)



→ Gate and drain terminals connected together. $V_{GD} = 0, < V_{tn}$

→ Find i-v relationship in terms of k_n and V_{tn}. Neglect ~~$\lambda = 0$~~ (λ).

→ $v_D = v_G$, implies operation in saturation mode.

$$i_D = \frac{1}{2} k_n \left(\frac{W}{L}\right) (v_{GS} - V_{tn})^2$$

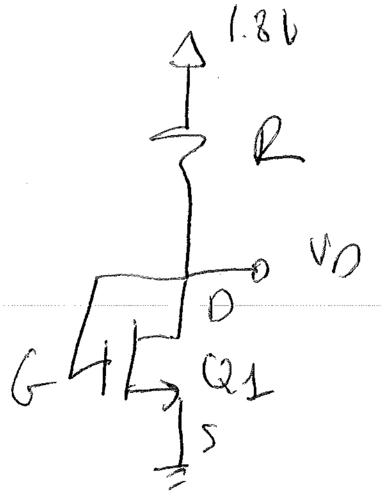
$$i = i_d \qquad v = v_{GS}$$

$$\therefore \boxed{i = \frac{1}{2} k_n (v - V_{tn})^2}$$

lec 14 ↑
lec 15 ↓

Find R for $V_D = 0.7V$.

D.59.



$V_{tn} = 0.8V$

$\mu_n C_{ox} = 0.4 mA/V^2$ $\qquad \lambda = 0$

$\frac{W}{L} = \frac{0.72 \mu m}{0.18 \mu m} = 4.0$

Sat. mode $(V_{GD} = 0 < V_{tn})$

$V_D = 0.7V = 1.8 - I_D R_D$

$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_D - V_{tn})^2 = 0.032 mA$

$\therefore R = \frac{1.8 - 0.7}{0.032 mA} = 34.4 k\Omega$.

$V_{GS} -$

$V_{DS} \geq V_{GS} - V_T$

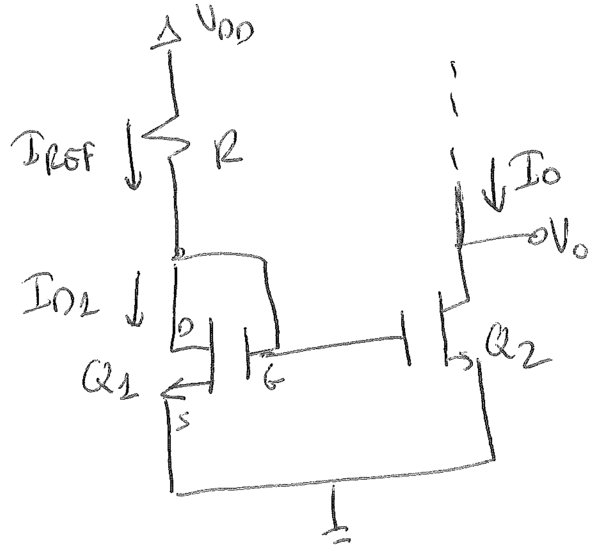
$V_D - V_S \geq V_G - V_S - V_T$

$V_D - V_G > V_T$

9/29/2016

8.2.1 – Current Sources, current Mirrors,

<u>Basic MOSFET Current Source.</u>



$Q_1 \rightarrow$ "Heart" of circuit.
Diode connected → always sat.

$$I_{D1} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 (V_{GS} - V_{TN})^2 \quad (1)$$

(assume $\lambda_0 \rightarrow 0$)

Drain current supplied thru V_{DD} and Resistor R (external to circuit)
Gate current → 0

$$\therefore I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R} \quad (2)$$

→ Equations (1) + (2) used to determine ~~I_{REF}~~ R for a set I_{REF}.

→ Q_2 → has same V_{GS} as Q_1 (also in saturation)

$$\therefore I_o = I_{D2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_2 (V_{GS} - V_{TN})^2 \rightarrow (3)$$

From (1) and (3)
$$\frac{I_o}{I_{REF}} = \frac{\frac{1}{2} k_n' \left(\frac{W}{L}\right)_2 (V_{GS} - V_{TN})^2}{\frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 (V_{GS} - V_{TN})^2} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}$$

→ If $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$ then $I_{REF} = I_o$ → "current mirror"

→ Scaling $\left(\frac{W}{L}\right)_1$ to $\left(\frac{W}{L}\right)_2$ scales I_o to I_{REF} → current gain or current transfer ratio.

Effect of V_O and I_O

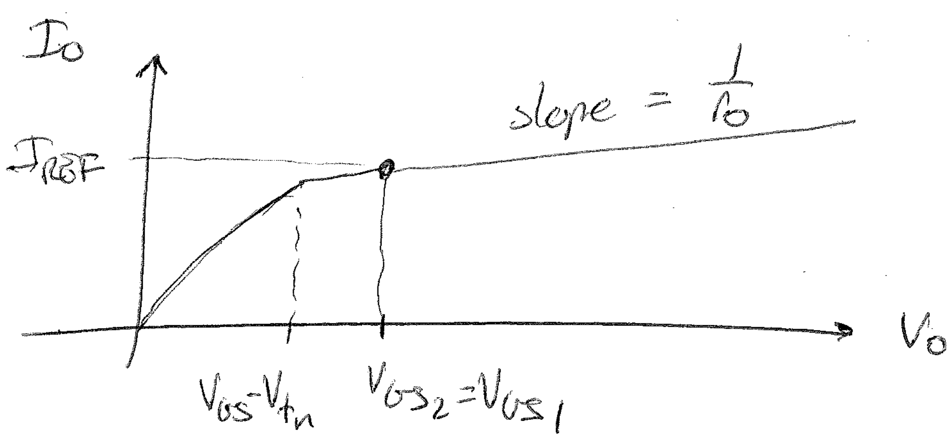
→ Q_2 must remain in saturation.

$\therefore \quad V_O = V_{DS_2} \geq V_{GS_2} - V_{tn} \quad$ or $\quad V_O \geq V_{OV}$

V_{OV} generally a few tenths of volts.

→ Also channel-length modulation λ can have significant effect on the operation of the current source.

As V_O increases beyond initial value of V_{GS_1}, I_O increases according to r_{o_2} of Q_2.



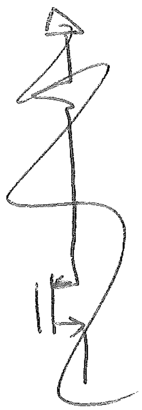
$\therefore$ Output resistance of current source

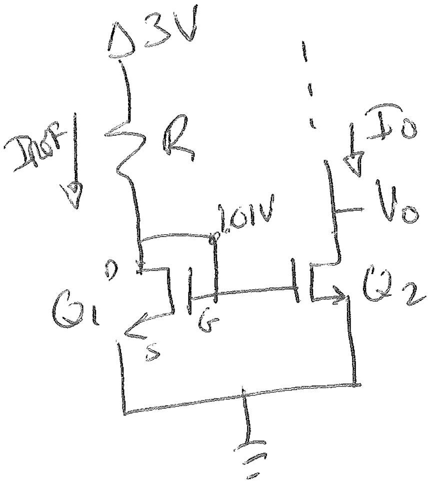
$$R_O = \frac{\Delta V_O}{\Delta I_O} = r_{o2} = \frac{V_{A2}}{I_O} = \frac{1}{\lambda_2 I_O}$$

→ use long channel trans. to get high R_O.

Also $I_O = \frac{(W/L)_2}{(W/L)_1} I_{REF}\left(1 + \frac{V_O - V_{GS}}{V_{A2}}\right)$ take into account channel length mod.

Ex. 8.1 – Current mirror example: 9/29/2016 (2)





a)

$V_{DD} = 3V$

$I_{REF} = 100\mu A$

Design circuit for $I_O = 100\mu A$.

Find R for $Q_1 = Q_2$ and $L = 1\mu m$, $W = 10\mu m$, $V_{tn} = 0.7V$

$k'_n = 200\ \mu A/V^2$.

a) $Q_1 = Q_2$ in saturation $V_D = V_G$

$$\therefore\ I_{D1} = I_{REF} = \frac{1}{2} k'_n \left(\frac{W}{L}\right)_1 \underbrace{(V_{GS} - V_T)^2}_{(V_{OV})^2}$$

$$100\times10^{-6} A = \frac{1}{2}\, 200\times10^{-6} A/V^2 \left(\frac{10}{1}\right) V_{OV}^2$$

$$V_{OV}^2 = \cancel{0.316V \rightarrow V_{OV}}\ \frac{2 \cdot 100\times10^{-6}}{200\times10^{-6}} \frac{1}{10}$$

$$\sqrt{(V_{OV})^2} = \sqrt{0.2}$$

$$V_{OV} = V_{GS} - V_T = 0.316V$$

$$V_{GS} = 0.316V + 0.7V = 1.01 \text{ Volt.}$$

$$\boxed{R = \frac{3V - 1.01V}{100\times10^{-6} A} = 19.83\ k\Omega}$$

b) Find lowest possible value of V_O?

$$\boxed{V_{Omin} = V_{GS} - V_T = V_{OV} = 0.316V}$$

c) Assuming $V_A' = 20V/\mu m$ (length dependent early voltage) find output resistance of the current source.

$$R_o = r_{o2} = \frac{V_{A2}}{I_{D2}}$$

$V_{A2} = V_A' \times (\text{length})$

$V_{A2} = 20V/\mu m \times 1\mu m = 20V$

$$\boxed{R_o = \frac{20V}{100\mu A} = 200k\Omega}$$

d) Find change in output current resulting from a +1-V change in V_o.

$\Delta V_o = \Delta I_o \cdot r_o \longrightarrow \Delta V_o = 1V,\ r_o = 200k\Omega.$

$$\boxed{\Delta I_o = \frac{1V}{200k\Omega} = 5\mu A}$$

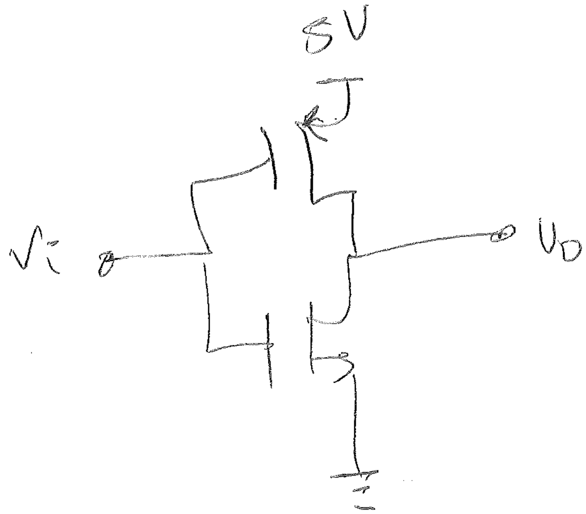
HW #4:

5.46, 5.50, 5.61

↳ sol: (a) R: ~~21~~ kΩ (b) $W_2 = 14.4\mu m$ $R_2 = 3.1k\Omega$

$V_{DS} = V_{GS} - V_T = 0.25V$

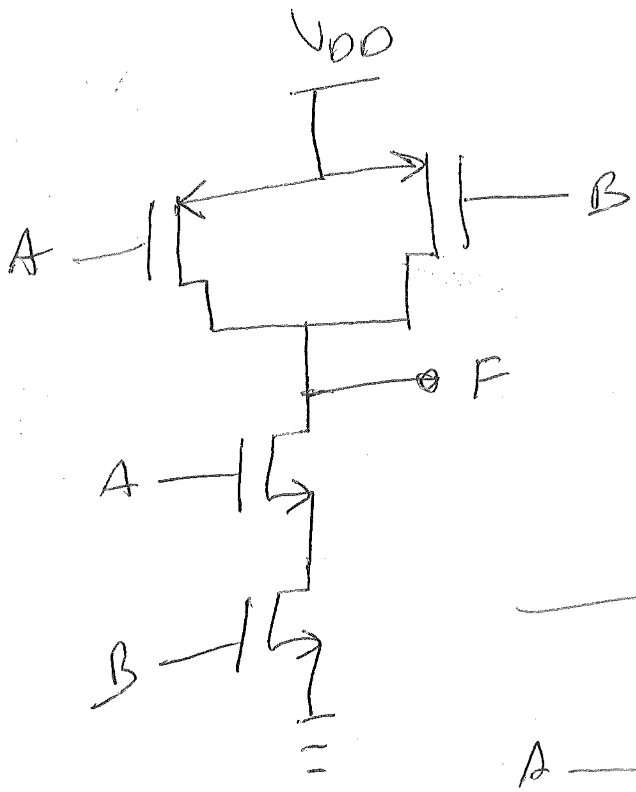
CMOS-LOGIC QUIZ 9/30/2016



Q1: Is the top transistor?

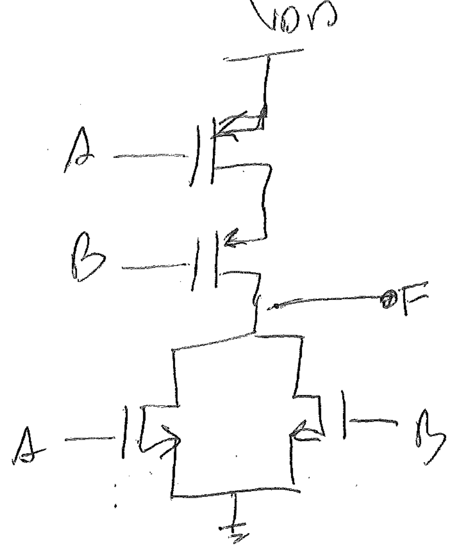
A: PMOS

B: NMOS



A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

NAND



A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

NOR