

## Computer Simulation Problems

**SIM** Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

## Section 7.1: Basic Principles

7.1 For the MOS amplifier of Fig. 7.2(a) with  $V_{DD} = 5$  V,  $V_i = 0.5$  V,  $k_n = 10 \text{ mA/V}^2$ , and  $R_D = 20 \text{ k}\Omega$ , determine the coordinates of the active-region segment (AB) of the VTC [Fig. 7.2(b)].

**D** 7.2 For the MOS amplifier of Fig. 7.2(a) with  $V_{DD} = 5$  V and  $k_n = 5 \text{ mA/V}^2$ , it is required to have the end point of the VTC, point B, at  $V_{DS} = 0.5$  V. What value of  $R_D$  is required? If the transistor is replaced with another having twice the value of the transconductance parameter  $k_n$ , what new value of  $R_D$  is needed?

**D** 7.3 It is required to bias the MOS amplifier of Fig. 7.3 at point Q for which  $V_{ov} = 0.2$  V and  $V_{DS} = 1$  V. Find the required value of  $R_D$  when  $V_{DD} = 5$  V,  $V_i = 0.5$  V, and  $k_n = 10 \text{ mA/V}^2$ . Also specify the coordinates of the VTC end point B. What is the small-signal voltage gain of this amplifier? Assuming linear operation, what is the maximum allowable negative signal swing at the output? What is the corresponding peak input signal?

7.4 The MOS amplifier of Fig. 7.4(a), when operated with  $V_{DD} = 2$  V, is found to have a maximum small-signal voltage gain magnitude of 14 V/V. Find  $V_{ov}$  and  $V_{DS}$  for bias point Q at which a voltage gain of  $-12$  V/V is obtained.

7.5 Consider the amplifier of Fig. 7.4(a) for the case  $V_{DD} = 5$  V,  $R_D = 24 \text{ k}\Omega$ ,  $k'_n(W/L) = 1 \text{ mA/V}^2$ , and  $V_i = 1$  V.

- Find the coordinates of the two end points of the saturation-region segment of the amplifier transfer characteristic, that is, points A and B on the sketch of Fig. 7.4(b).
- If the amplifier is biased to operate with an overdrive voltage  $V_{ov}$  of 0.5 V, find the coordinates of the bias point

Q on the transfer characteristic. Also, find the value of  $I_D$  and of the incremental gain  $A_v$  at the bias point.

- For the situation in (b), and disregarding the distortion caused by the MOSFET's square-law characteristic, what is the largest amplitude of a sine-wave voltage signal that can be applied at the input while the transistor remains in saturation? What is the amplitude of the output voltage signal that results? What gain value does the combination of these amplitudes imply? By what percentage is this gain value different from the incremental gain value calculated above? Why is there a difference?

7.6 Various measurements are made on an NMOS amplifier for which the drain resistor  $R_D$  is  $20 \text{ k}\Omega$ . First, dc measurements show the voltage across the drain resistor,  $V_{RD}$ , to be 1.5 V and the gate-to-source bias voltage to be 0.7 V. Then, ac measurements with small signals show the voltage gain to be  $-10 \text{ V/V}$ . What is the value of  $V_i$  for this transistor? If the process transconductance parameter  $k'_n$  is  $200 \mu\text{A/V}^2$ , what is the MOSFET's  $W/L$ ?

\*7.7 The expression for the incremental voltage gain  $A_v$  given in Eq. (7.16) can be written as

$$A_v = -\frac{2(V_{DD} - V_{DS})}{V_{ov}}$$

where  $V_{DS}$  is the bias voltage at the drain. This expression indicates that for given values of  $V_{DD}$  and  $V_{ov}$ , the gain magnitude can be increased by biasing the transistor at a lower  $V_{DS}$ . This, however, reduces the allowable output signal swing in the negative direction. Assuming linear operation around the bias point, show that the largest possible negative output signal peak  $\hat{v}_o$  that is achievable while the transistor remains saturated is

$$\hat{v}_o = (V_{DS} - V_{ov}) / \left( 1 + \frac{1}{|A_v|} \right)$$

For  $V_{DD} = 5$  V and  $V_{ov} = 0.5$  V, provide a table of values for  $A_v$ ,  $\hat{v}_o$ , and the corresponding  $\hat{v}_i$  for  $V_{DS} = 1$  V, 1.5 V, 2 V, and 2.5 V. If  $k'_n(W/L) = 1 \text{ mA/V}^2$ , find  $I_D$  and  $R_D$  for the design for which  $V_{DS} = 1$  V.

**D** \*7.8 Design the MOS amplifier of Fig. 7.4(a) to obtain maximum gain while allowing for an output voltage swing of at least  $\pm 0.5$  V. Let  $V_{DD} = 5$  V, and utilize an overdrive

voltage of approximately 0.2 V.

- Specify  $V_{DS}$  at the bias point.
- What is the gain achieved? What is the signal amplitude  $\hat{v}_{gs}$  that results in the 0.5-V signal amplitude at the output?
- If the dc bias current in the drain is to be 100  $\mu\text{A}$ , what value of  $R_D$  is needed?
- If  $k'_n = 200 \mu\text{A/V}^2$ , what  $W/L$  ratio is required for the MOSFET?

\*7.9 Figure P7.9 shows an amplifier in which the load resistor  $R_D$  has been replaced with another NMOS transistor  $Q_2$  connected as a two-terminal device. Note that because  $v_{DG}$  of  $Q_2$  is zero, it will be operating in saturation at all times, even when  $v_t = 0$  and  $i_{D2} = i_{D1} = 0$ . Note also that the two transistors conduct equal drain currents. Using  $i_{D1} = i_{D2}$ , show that for the range of  $v_t$  over which  $Q_1$  is operating in saturation, that is, for

$$V_{ii} \leq v_t \leq v_o + V_{ii}$$

the output voltage will be given by

$$v_o = V_{DD} - V_t + \sqrt{\frac{(W/L)_1}{(W/L)_2}} V_t - \sqrt{\frac{(W/L)_1}{(W/L)_2}} v_t$$

where we have assumed  $V_{ii} = V_{ii} = V_t$ . Thus the circuit functions as a linear amplifier, even for large input signals. For  $(W/L)_1 = (50 \mu\text{m}/0.5 \mu\text{m})$  and  $(W/L)_2 = (5 \mu\text{m}/0.5 \mu\text{m})$ , find the voltage gain.

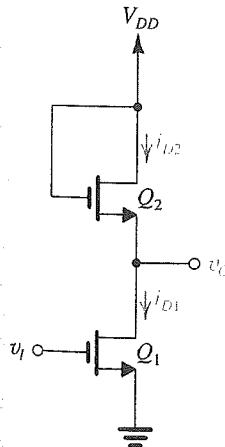


Figure P7.9

7.10 A BJT amplifier circuit such as that in Fig. 7.6 is operated with  $V_{CC} = +5 \text{ V}$  and is biased at  $V_{CE} = +1 \text{ V}$ . Find the voltage gain, the maximum allowed output negative swing without the transistor entering saturation, and the corresponding maximum input signal permitted.

7.11 For the amplifier circuit in Fig. 7.6 with  $V_{CC} = +5 \text{ V}$  and  $R_C = 1 \text{k}\Omega$ , find  $V_{CE}$  and the voltage gain at the following dc collector bias currents: 0.5 mA, 1 mA, 2.5 mA, 4 mA, and 4.5 mA. For each, give the maximum possible positive- and negative-output signal swing as determined by the need to keep the transistor in the active region. Present your results in a table.

D 7.12 Consider the CE amplifier circuit of Fig. 7.6 when operated with a dc supply  $V_{CC} = +5 \text{ V}$ . It is required to find the point at which the transistor should be biased; that is, find the value of  $V_{CE}$  so that the output sine-wave signal  $v_{ce}$  resulting from an input sine-wave signal  $v_{be}$  of 5-mV peak amplitude has the maximum possible magnitude. What is the peak amplitude of the output sine wave and the value of the gain obtained? Assume linear operation around the bias point. (Hint: To obtain the maximum possible output amplitude for a given input, you need to bias the transistor as close to the edge of saturation as possible without entering saturation at any time, that is, without  $v_{ce}$  decreasing below 0.3 V.)

7.13 A designer considers a number of low-voltage BJT amplifier designs utilizing power supplies with voltage  $V_{CC}$  of 1.0, 1.5, 2.0, or 3.0 V. For transistors that saturate at  $V_{CE} = 0.3 \text{ V}$ , what is the largest possible voltage gain achievable with each of these supply voltages? If in each case biasing is adjusted so that  $V_{CE} = V_{CC}/2$ , what gains are achieved? If a negative-going output signal swing of 0.4 V is required, at what  $V_{CE}$  should the transistor be biased to obtain maximum gain? What is the gain achieved with each of the supply voltages? (Notice that all of these gains are independent of the value of  $I_C$  chosen!)

D \*7.14 A BJT amplifier such as that in Fig. 7.6 is to be designed to support relatively undistorted sine-wave output signals of peak amplitudes  $P$  volt without the BJT entering saturation or cutoff and to have the largest possible voltage gain, denoted  $A_v$  V/V. Show that the minimum supply voltage  $V_{CC}$  needed is given by

$$V_{CC} = V_{CESat} + P + |A_v| V_T$$

Also, find  $V_{CC}$ , specified to the nearest 0.5 V, for the following situations:

- (a)  $A_v = -20 \text{ V/V}, P = 0.2 \text{ V}$
- (b)  $A_v = -50 \text{ V/V}, P = 0.5 \text{ V}$
- (c)  $A_v = -100 \text{ V/V}, P = 0.5 \text{ V}$
- (d)  $A_v = -100 \text{ V/V}, P = 1.0 \text{ V}$
- (e)  $A_v = -200 \text{ V/V}, P = 1.0 \text{ V}$
- (f)  $A_v = -500 \text{ V/V}, P = 1.0 \text{ V}$
- (g)  $A_v = -500 \text{ V/V}, P = 2.0 \text{ V}$

7.15 The transistor in the circuit of Fig. P7.15 is biased at a dc collector current of 0.3 mA. What is the voltage gain? (Hint: Use Thévenin's theorem to convert the circuit to the form in Fig. 7.6.)

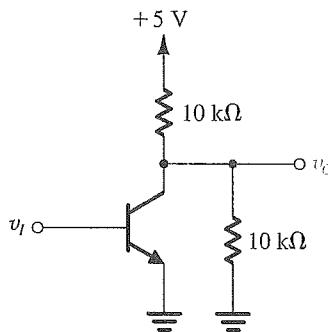


Figure P7.15

7.16 Sketch and label the voltage-transfer characteristics of the *pnp* amplifiers shown in Fig. P7.16.

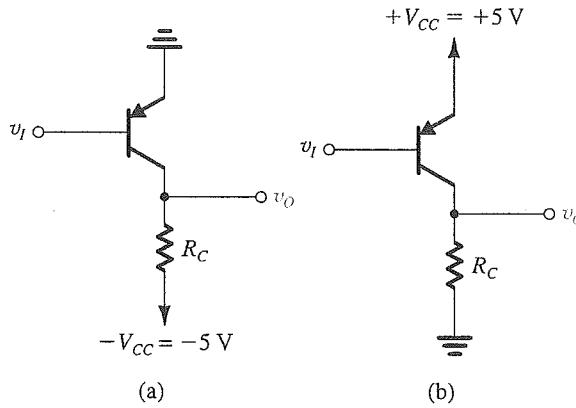


Figure P7.16

\*7.17 In deriving the expression for small-signal voltage gain  $A_v$  in Eq. (7.21) we neglected the Early effect. Derive this expression including the Early effect by substituting

$$i_C = I_s e^{v_{BE}/V_T} \left( 1 + \frac{v_{CE}}{V_A} \right)$$

in Eq. (7.4) and including the factor  $(1 + V_{ce}/V_A)$  in Eq. (7.11). Show that the gain expression changes to

$$A_v = \frac{-I_c R_c / V_T}{\left[ 1 + \frac{I_c R_c}{V_A + V_{CE}} \right]} = -\frac{(V_{CC} - V_{CE}) / V_T}{\left[ 1 + \frac{V_{CC} - V_{CE}}{V_A + V_{CE}} \right]}$$

For the case  $V_{CC} = 5 \text{ V}$  and  $V_{CE} = 3 \text{ V}$ , what is the gain without and with the Early effect taken into account? Let  $V_A = 100 \text{ V}$ .

7.18 When the amplifier circuit of Fig. 7.6 is biased with a certain  $V_{BE}$ , the dc voltage at the collector is found to be  $+2 \text{ V}$ . For  $V_{CC} = +5 \text{ V}$  and  $R_c = 1 \text{ k}\Omega$ , find  $I_c$  and the small-signal voltage gain. For a change  $\Delta v_{BE} = +5 \text{ mV}$ , calculate the resulting  $\Delta v_o$ . Calculate it two ways: by using the transistor exponential characteristic  $\Delta i_c$ , and approximately, using the small-signal voltage gain. Repeat for  $\Delta v_{BE} = -5 \text{ mV}$ . Summarize your results in a table.

\*7.19 Consider the amplifier circuit of Fig. 7.6 when operated with a supply voltage  $V_{CC} = +3 \text{ V}$ .

- (a) What is the theoretical maximum voltage gain that this amplifier can provide?
- (b) What value of  $V_{CE}$  must this amplifier be biased at to provide a voltage gain of  $-60 \text{ V/V}$ ?
- (c) If the dc collector current  $I_c$  at the bias point in (b) is to be  $0.5 \text{ mA}$ , what value of  $R_c$  should be used?
- (d) What is the value of  $V_{BE}$  required to provide the bias point mentioned above? Assume that the BJT has  $I_s = 10^{-15} \text{ A}$ .
- (e) If a sine-wave signal  $v_{be}$  having a  $5\text{-mV}$  peak amplitude is superimposed on  $V_{BE}$ , find the corresponding output voltage signal  $v_{ce}$  that will be superimposed on  $V_{CE}$  assuming linear operation around the bias point.
- (f) Characterize the signal current  $i_c$  that will be superimposed on the dc bias current  $I_c$ .

- (g) What is the value of the dc base current  $I_b$  at the bias point? Assume  $\beta = 100$ . Characterize the signal current  $i_b$  that will be superimposed on the base current  $I_b$ .
- (h) Dividing the amplitude of  $v_{be}$  by the amplitude of  $i_b$ , evaluate the incremental (or small-signal) input resistance of the amplifier.
- (i) Sketch and clearly label correlated graphs for  $v_{be}$ ,  $v_{ce}$ ,  $i_c$ , and  $i_b$  versus time. Note that each graph consists of a dc or average value and a superimposed sine wave. Be careful of the phase relationships of the sine waves.

7.20 The essence of transistor operation is that a change in  $v_{be}$ ,  $\Delta v_{be}$ , produces a change in  $i_c$ ,  $\Delta i_c$ . By keeping  $\Delta v_{be}$  small,  $\Delta i_c$  is approximately linearly related to  $\Delta v_{be}$ ,  $\Delta i_c = g_m \Delta v_{be}$ , where  $g_m$  is known as the transistor transconductance. By passing  $\Delta i_c$  through  $R_c$ , an output voltage signal  $\Delta v_o$  is obtained. Use the expression for the small-signal voltage gain in Eq. (7.20) to derive an expression for  $g_m$ . Find the value of  $g_m$  for a transistor biased at  $I_c = 0.5$  mA.

7.21 The purpose of this problem is to illustrate the application of graphical analysis to the circuit shown in Fig. P7.21. Sketch  $i_c - v_{ce}$  characteristic curves for the BJT for  $i_b = 10 \mu A$ ,  $20 \mu A$ ,  $30 \mu A$ , and  $40 \mu A$ . Assume the lines to be horizontal (i.e., neglect the Early effect), and let  $\beta = 100$ . For  $V_{cc} = 5$  V and  $R_c = 1 \text{ k}\Omega$ , sketch the load line. What peak-to-peak collector voltage swing will result for  $i_b$  varying

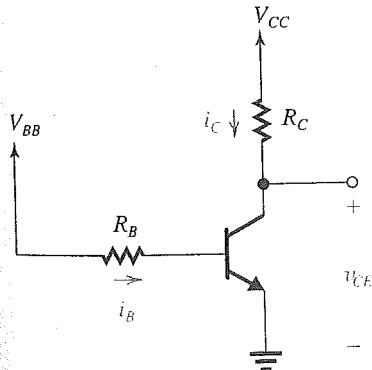


Figure P7.21

over the range  $10 \mu A$  to  $40 \mu A$ ? If the BJT is biased at  $V_{ce} = \frac{1}{2}V_{cc}$ , find the value of  $I_c$  and  $I_b$ . If at this current  $V_{be} = 0.7$  V and if  $R_B = 100 \text{ k}\Omega$ , find the required value of  $V_{BB}$ .

\*7.22 Sketch the  $i_c - v_{ce}$  characteristics of an *n-p-n* transistor having  $\beta = 100$  and  $V_A = 100$  V. Sketch characteristic curves for  $i_b = 20 \mu A$ ,  $50 \mu A$ ,  $80 \mu A$ , and  $100 \mu A$ . For the purpose of this sketch, assume that  $i_c = \beta i_b$  at  $v_{ce} = 0$ . Also, sketch the load line obtained for  $V_{cc} = 10$  V and  $R_c = 1 \text{ k}\Omega$ . If the dc bias current into the base is  $50 \mu A$ , write the equation for the corresponding  $i_c - v_{ce}$  curve. Also, write the equation for the load line, and solve the two equations to obtain  $V_{ce}$  and  $I_c$ . If the input signal causes a sinusoidal signal of  $30-\mu\text{A}$  peak amplitude to be superimposed on  $I_b$ , find the corresponding signal components of  $i_c$  and  $v_{ce}$ .

### Section 7.2: Small-Signal Operation and Models

\*7.23 This problem investigates the nonlinear distortion introduced by a MOSFET amplifier. Let the signal  $v_{gs}$  be a sine wave with amplitude  $V_{gs}$ , and substitute  $v_{gs} = V_{gs} \sin \omega t$  in Eq. (7.28). Using the trigonometric identity  $\sin^2 \theta = \frac{1}{2} - \frac{1}{2} \cos 2\theta$ , show that the ratio of the signal at frequency  $2\omega$  to that at frequency  $\omega$ , expressed as a percentage (known as the second-harmonic distortion) is

$$\text{Second-harmonic distortion} = \frac{1}{4} \frac{V_{gs}}{V_{ov}} \times 100$$

If in a particular application  $V_{gs}$  is  $10 \text{ mV}$ , find the minimum overdrive voltage at which the transistor should be operated so that the second-harmonic distortion is kept to less than 1%.

7.24 Consider an NMOS transistor having  $k_n = 10 \text{ mA/V}^2$ . Let the transistor be biased at  $V_{ov} = 0.2$  V. For operation in saturation, what dc bias current  $I_D$  results? If a  $0.02$ -V signal is superimposed on  $V_{gs}$ , find the corresponding increment in collector current by evaluating the total collector current  $i_D$  and subtracting the dc bias current  $I_D$ . Repeat for a  $-0.02$ -V signal. Use these results to estimate  $g_m$  of the FET at this bias point. Compare with the value of  $g_m$  obtained using Eq. (7.33).

7.25 Consider the FET amplifier of Fig. 7.10 for the case  $V_t = 0.4$  V,  $k_n = 5 \text{ mA/V}^2$ ,  $V_{GS} = 0.6$  V,  $V_{DD} = 1.8$  V, and  $R_D = 10 \text{ k}\Omega$ .

- Find the dc quantities  $I_D$  and  $V_{DS}$ .
- Calculate the value of  $g_m$  at the bias point.
- Calculate the value of the voltage gain.
- If the MOSFET has  $\lambda = 0.1 \text{ V}^{-1}$ , find  $r_o$  at the bias point and calculate the voltage gain.

D \*7.26 An NMOS amplifier is to be designed to provide a 0.20-V peak output signal across a 20-k $\Omega$  load that can be used as a drain resistor. If a gain of at least 10 V/V is needed, what  $g_m$  is required? Using a dc supply of 1.8 V, what values of  $I_D$  and  $V_{OV}$  would you choose? What  $W/L$  ratio is required if  $\mu_n C_{ox} = 200 \text{ }\mu\text{A/V}^2$ ? If  $V_t = 0.4$  V, find  $V_{GS}$ .

D \*7.27 In this problem we investigate an optimum design of the CS amplifier circuit of Fig. 7.10. First, use the voltage gain expression  $A_v = -g_m R_D$  together with Eq. (7.42) for  $g_m$  to show that

$$A_v = -\frac{2I_D R_D}{V_{OV}} = -\frac{2(V_{DD} - V_{DS})}{V_{OV}}$$

Next, let the maximum positive input signal be  $\hat{v}_i$ . To keep the second-harmonic distortion to an acceptable level, we bias the MOSFET to operate at an overdrive voltage  $V_{OV} \gg \hat{v}_i$ . Let  $V_{OV} = m\hat{v}_i$ . Now, to maximize the voltage gain  $|A_v|$ , we design for the lowest possible  $V_{DS}$ . Show that the minimum  $V_{DS}$  that is consistent with allowing a negative signal voltage swing at the drain of  $|A_v| \hat{v}_i$ , while maintaining saturation-mode operation is given by

$$V_{DS} = \frac{V_{OV} + \hat{v}_i + 2V_{DD}(\hat{v}_i/V_{OV})}{1 + 2(\hat{v}_i/V_{OV})}$$

Now, find  $V_{OV}$ ,  $V_{DS}$ ,  $A_v$ , and  $\hat{v}_o$  for the case  $V_{DD} = 2.5$  V,  $\hat{v}_i = 20 \text{ mV}$ , and  $m = 15$ . If it is desired to operate this transistor at  $I_D = 200 \text{ }\mu\text{A}$ , find the values of  $R_D$  and  $W/L$ , assuming that for this process technology  $k'_n = 100 \text{ }\mu\text{A/V}^2$ .

7.28 In the table below, for MOS transistors operating under a variety of conditions, complete as many entries as possible. Although some data is not available, it is always possible to calculate  $g_m$  using one of Eqs. (7.40), (7.41), or (7.42). Assume  $\mu_n = 500 \text{ cm}^2/\text{V}\cdot\text{s}$ ,  $\mu_p = 250 \text{ cm}^2/\text{V}\cdot\text{s}$ , and  $C_{ox} = 0.4 \text{ fF}/\mu\text{m}^2$ .

Case	Type	$I_D$ (mA)	Voltages (V)		Dimensions ( $\mu\text{m}$ )				
			$ V_{GS} $	$ V_t $	$V_{OV}$	$W$	$L$	$W/L$	$K(W/L)$
a	N	1	3	2			1		
b	N	1		0.7	0.5				
c	N	10			2		1		
d	N	0.5			0.5				
e	N	0.1				10	2		
f	N		1.8	0.8		40	4		
g	P	0.5						25	
h	P		3	1					0.5
i	P	10				4000	2		
j	P	10			4				
k	P				1	30	3		
l	P				5				0.08

= Multisim/PSpice; \* = difficult problem; \*\* = more difficult; \*\*\* = very challenging; D = design problem

7.29 An NMOS technology has  $\mu_n C_{ox} = 250 \mu\text{A/V}^2$  and  $V_t = 0.5 \text{ V}$ . For a transistor with  $L = 0.5 \mu\text{m}$ , find the value of  $W$  that results in  $g_m = 2 \text{ mA/V}$  at  $I_D = 0.25 \text{ mA}$ . Also, find the required  $V_{GS}$ .

7.30 For the NMOS amplifier in Fig. P7.30, replace the transistor with its T equivalent circuit, assuming  $\lambda = 0$ . Derive expressions for the voltage gains  $v_s/v_i$  and  $v_d/v_i$ .

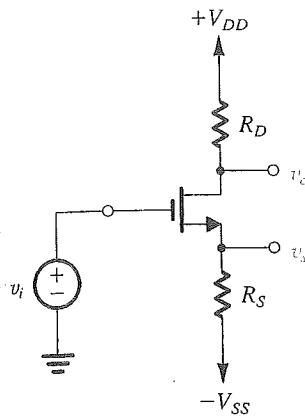


Figure P7.30

**SIM** 7.31 In the circuit of Fig. P7.31, the NMOS transistor has  $|V_t| = 0.5 \text{ V}$  and  $V_A = 50 \text{ V}$  and operates with  $V_D = 1 \text{ V}$ . What is the voltage gain  $v_o/v_i$ ? What do  $V_D$  and the gain become for  $I$  increased to 1 mA?

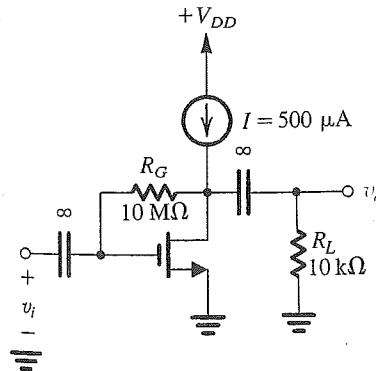


Figure P7.31

7.32 For a 0.18-μm CMOS fabrication process:  $V_m = 0.5 \text{ V}$ ,  $V_{tp} = -0.5 \text{ V}$ ,  $\mu_n C_{ox} = 400 \mu\text{A/V}^2$ ,  $\mu_p C_{ox} = 100 \mu\text{A/V}^2$ ,  $C_{ox} = 8.6 \text{ fF}/\mu\text{m}^2$ ,  $V_A$  (n-channel devices) =  $5L$  (μm), and  $|V_A|$  (p-channel devices) =  $6L$  (μm). Find the small-signal model parameters ( $g_m$  and  $r_o$ ) for both an NMOS and a PMOS transistor having  $W/L = 10 \mu\text{m}/0.5 \mu\text{m}$  and operating at  $I_D = 100 \mu\text{A}$ . Also, find the overdrive voltage at which each device must be operating.

\*7.33 Figure P7.33 shows a discrete-circuit amplifier. The input signal  $v_{sig}$  is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite). All capacitors behave as short circuits for signals and as open circuits for dc.

- If the transistor has  $V_t = 1 \text{ V}$ , and  $k_n = 4 \text{ mA/V}^2$ , verify that the bias circuit establishes  $V_{GS} = 1.5 \text{ V}$ ,  $I_D = 0.5 \text{ mA}$ , and  $V_D = +7.0 \text{ V}$ . That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.
- Find  $g_m$  and  $r_o$  if  $V_A = 100 \text{ V}$ .
- Draw a complete small-signal equivalent circuit for the amplifier, assuming all capacitors behave as short circuits at signal frequencies.
- Find  $R_{in}$ ,  $v_{gs}/v_{sig}$ ,  $v_o/v_{gs}$ , and  $v_o/v_{sig}$ .

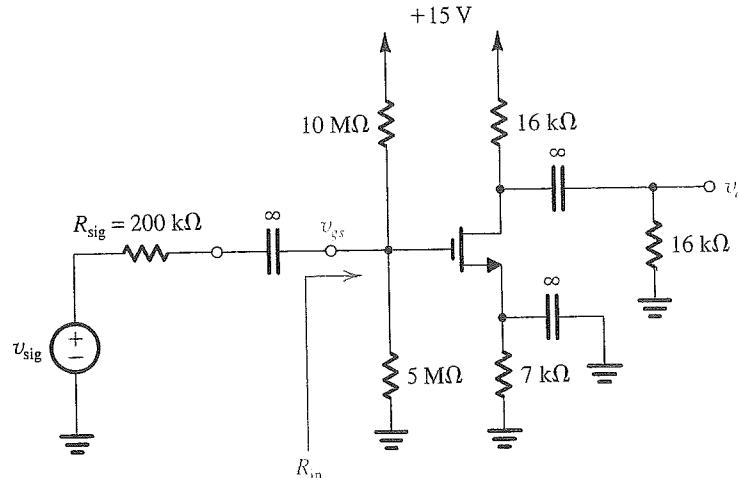


Figure P7.33

## CHAPTER 7 PROBLEMS

**7.34** Consider a transistor biased to operate in the active mode at a dc collector current  $I_C$ . Calculate the collector signal current as a fraction of  $I_C$  (i.e.,  $i_c/I_C$ ) for input signals  $v_{be}$  of +1 mV, -1 mV, +2 mV, -2 mV, +5 mV, -5 mV, +8 mV, -8 mV, +10 mV, -10 mV, +12 mV, and -12 mV. In each case do the calculation two ways:

- (a) using the exponential characteristic, and
- (b) using the small-signal approximation.

Present your results in the form of a table that includes a column for the error introduced by the small-signal approximation. Comment on the range of validity of the small-signal approximation.

**7.35** An *npn* BJT with grounded emitter is operated with  $V_{BE} = 0.700$  V, at which the collector current is 0.5 mA. A 5-k $\Omega$  resistor connects the collector to a +5-V supply. What is the resulting collector voltage  $V_C$ ? Now, if a signal applied to the base raises  $v_{BE}$  to 705 mV, find the resulting total collector current  $i_C$  and total collector voltage  $v_C$  using the exponential  $i_C-v_{BE}$  relationship. For this situation, what are  $v_{be}$  and  $v_c$ ? Calculate the voltage gain  $v_c/v_{be}$ . Compare with the value obtained using the small-signal approximation, that is,  $-g_m R_C$ .

**7.36** A transistor with  $\beta = 100$  is biased to operate at a dc collector current of 0.5 mA. Find the values of  $g_m$ ,  $r_\pi$ , and  $r_e$ . Repeat for a bias current of 50  $\mu$ A.

**7.37** A *pnp* BJT is biased to operate at  $I_C = 1.0$  mA. What is the associated value of  $g_m$ ? If  $\beta = 100$ , what is the value of the small-signal resistance seen looking into the emitter ( $r_e$ )? Into the base ( $r_\pi$ )? If the collector is connected to a 5-k $\Omega$  load, with a signal of 5-mV peak applied between base and emitter, what output signal voltage results?

**D 7.38** A designer wishes to create a BJT amplifier with a  $g_m$  of 30 mA/V and a base input resistance of 3000  $\Omega$  or more.

What collector-bias current should he choose? What is the minimum  $\beta$  he can tolerate for the transistor used?

**7.39** A transistor operating with nominal  $g_m$  of 40 mA/V has a  $\beta$  that ranges from 50 to 150. Also, the bias circuit, being less than ideal, allows a  $\pm 20\%$  variation in  $I_C$ . What are the extreme values found of the resistance looking into the base?

**7.40** In the circuit of Fig. 7.20,  $V_{BE}$  is adjusted so that  $V_C = 1$  V. If  $V_{CC} = 3$  V,  $R_C = 2$  k $\Omega$ , and a signal  $v_{be} = 0.005 \sin \omega t$  volts is applied, find expressions for the total instantaneous quantities  $i_C(t)$ ,  $v_C(t)$ , and  $i_B(t)$ . The transistor has  $\beta = 100$ . What is the voltage gain?

**D \*7.41** We wish to design the amplifier circuit of Fig. 7.20 under the constraint that  $V_{CC}$  is fixed. Let the input signal  $v_{be} = \hat{V}_{be} \sin \omega t$ , where  $\hat{V}_{be}$  is the maximum value for acceptable linearity. For the design that results in the largest signal at the collector, without the BJT leaving the active region, show that

$$R_C I_C = (V_{CC} - 0.3) / \left( 1 + \frac{\hat{V}_{be}}{V_T} \right)$$

and find an expression for the voltage gain obtained. For  $V_{CC} = 3$  V and  $\hat{V}_{be} = 5$  mV, find the dc voltage at the collector, the amplitude of the output voltage signal, and the voltage gain.

**7.42** The table below summarizes some of the basic attributes of a number of BJTs of different types, operating as amplifiers under various conditions. Provide the missing entries. (Note: Isn't it remarkable how much two parameters can reveal?)

**7.43** A BJT is biased to operate in the active mode at a dc collector current of 1 mA. It has a  $\beta$  of 100 and  $V_A$  of 100 V. Give the four small-signal models (Figs. 7.25 and 7.27) of the BJT complete with the values of their parameters.

Transistor	a	b	c	d	e	f	g
$\alpha$	1.000						
$\beta$							
$I_C$ (mA)	1.00	100	1.00	$\infty$		0.90	
$I_E$ (mA)			1.00				
$I_B$ (mA)		1.00	0.020			5	
$g_m$ (mA/V)							
$r_e$ ( $\Omega$ )				25	100	1.10	
$r_\pi$ ( $\Omega$ )					10.1 k $\Omega$	700	

 = Multisim/PSpice; \* = difficult problem; \*\* = more difficult; \*\*\* = very challenging; D = design problem

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7.44 Using the T model of Fig. 7.26(a), show that the input resistance between base and emitter, looking into the base, is equal to  $r_\pi$ .

7.45 Show that the collector current provided by the model of Fig. 7.26(b) is equal to that provided by the model in Fig. 7.26(a).

7.46 Show that the hybrid- $\pi$  model of Fig. 7.24(b) is the incremental version of the large-signal model of Fig. 6.5(d).

7.47 Show that the T model of Fig. 7.26(b) is the incremental version of the large-signal model of Fig. 6.5(b).

7.48 The transistor amplifier in Fig. P7.48 is biased with a current source  $I$  and has a very high  $\beta$ . Find the dc voltage at the collector,  $V_C$ . Also, find the value of  $r_e$ . Replace the transistor with the T model of Fig. 7.26(b) (note that the dc current source  $I$  should be replaced with an open circuit). Hence find the voltage gain  $v_c/v_i$ .

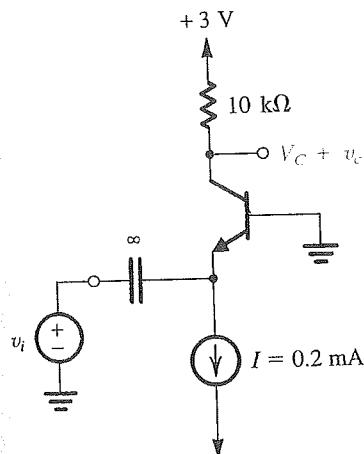


Figure P7.48

7.49 For the conceptual circuit shown in Fig. 7.23,  $R_C = 2 \text{ k}\Omega$ ,  $g_m = 50 \text{ mA/V}$ , and  $\beta = 100$ . If a peak-to-peak output voltage of 1 V is measured at the collector, what are the peak-to-peak values of  $v_{be}$  and  $i_b$ ?

7.50 Figure P7.50 shows the circuit of an amplifier fed with a signal source  $v_{sig}$  with a source resistance  $R_{sig}$ . The bias circuitry is not shown. Replace the BJT with its hybrid- $\pi$  equivalent circuit of Fig. 7.24(a). Find the input resistance  $R_{in} \equiv v_\pi/v_b$ , the voltage transmission from source to amplifier

input,  $v_\pi/v_{sig}$ , and the voltage gain from base to collector,  $v_o/v_\pi$ . Use these to show that the overall voltage gain  $v_o/v_{sig}$  is given by

$$\frac{v_o}{v_{sig}} = -\frac{\beta R_C}{r_\pi + R_{sig}}$$

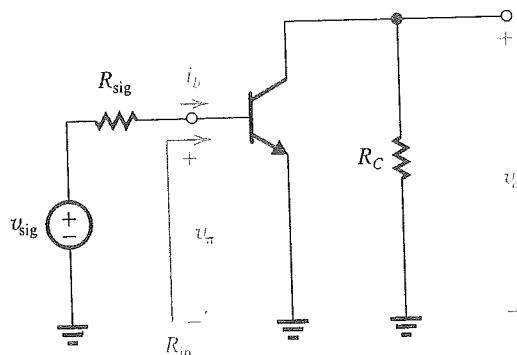


Figure P7.50

7.51 Figure P7.51 shows a transistor with the collector connected to the base. The bias arrangement is not shown. Since a zero  $v_{BC}$  implies operation in the active mode, the BJT can be replaced by one of the small-signal models of Figs. 7.24 and 7.26. Use the model of Fig. 7.26(b) and show that the resulting two-terminal device, known as a diode-connected transistor, has a small-signal resistance  $r$  equal to  $r_e$ .

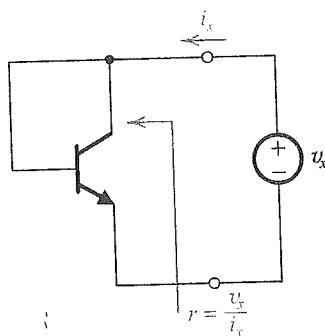


Figure P7.51

7.52 Figure P7.52 shows a particular configuration of BJT amplifiers known as "emitter follower." The bias arrangement is not shown. Replace the BJT with its T equivalent-circuit

## CHAPTER 7 PROBLEMS

model of Fig. 7.26(b). Show that

$$R_{in} \equiv \frac{v_i}{i_b} = (\beta + 1)(r_e + R_e)$$

$$\frac{v_o}{v_i} = \frac{R_e}{R_e + r_e}$$

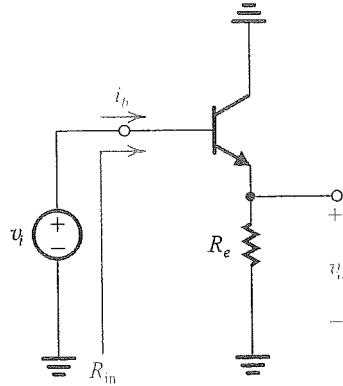


Figure P7.52

- 7.53 For the circuit shown in Fig. P7.53, draw a complete small-signal equivalent circuit utilizing an appropriate T model for the BJT (use  $\alpha = 0.99$ ). Your circuit should show the values of all components, including the model parameters. What is the input resistance  $R_{in}$ ? Calculate the overall voltage gain ( $v_o/v_{sig}$ ).

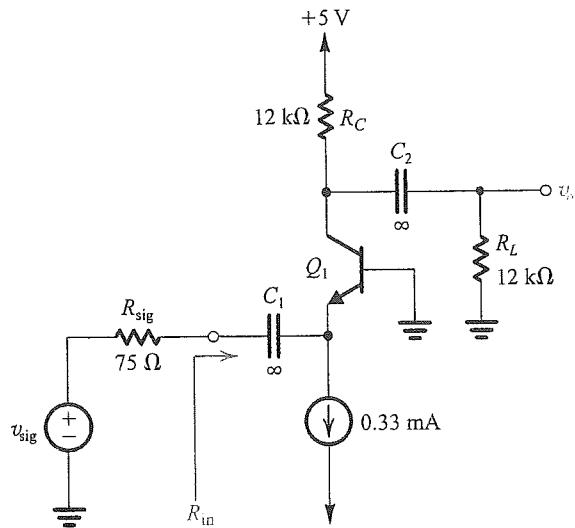


Figure P7.53

- 7.54 In the circuit shown in Fig. P7.54, the transistor has a  $\beta$  of 200. What is the dc voltage at the collector? Replacing the BJT with one of the hybrid- $\pi$  models (neglecting  $r_o$ ), draw the equivalent circuit of the amplifier. Find the input resistances  $R_{in}$  and  $R_{in}'$  and the overall voltage gain ( $v_o/v_{sig}$ ). For an output signal of  $\pm 0.4$  V, what values of  $v_{sig}$  and  $v_b$  are required?

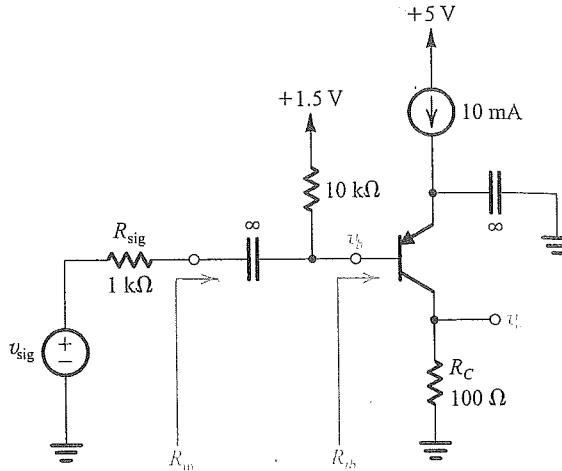


Figure P7.54

- 7.55 Consider the augmented hybrid- $\pi$  model shown in Fig. 7.25(a). Disregarding how biasing is to be done, what is the largest possible voltage gain available for a signal source connected directly to the base and a very-high-resistance load? Calculate the value of the maximum possible gain for  $V_A = 25$  V and  $V_A = 125$  V.

- D 7.56 Redesign the circuit of Fig. 7.30(a) by raising the resistor values by a factor  $n$  to increase the resistance seen by the input  $v_i$  to  $75 \Omega$ . What value of voltage gain results? Grounded-base circuits of this kind are used in systems such as cable TV, in which, for highest-quality signaling, load resistances need to be "matched" to the equivalent resistances of the interconnecting cables.

- D \*7.57 Design an amplifier using the configuration of Fig. 7.30(a). The power supplies available are  $\pm 5$  V. The input signal source has a resistance of  $50 \Omega$ , and it is required that the amplifier input resistance match this value. (Note that  $R_{in} = r_e \parallel R_E \simeq r_e$ .) The amplifier is to have the greatest possible voltage gain and the largest possible output signal but retain small-signal linear operation (i.e., the signal component across the base-emitter junction should be limited to no more

than 10 mV). Find appropriate values for  $R_E$  and  $R_C$ . What is the value of voltage gain realized from signal source to output?

\*7.58 The transistor in the circuit shown in Fig. P7.58 is biased to operate in the active mode. Assuming that  $\beta$  is very large, find the collector bias current  $I_C$ . Replace the transistor with the small-signal equivalent-circuit model of Fig. 7.26(b) (remember to replace the dc power supply with a short circuit). Analyze the resulting amplifier equivalent circuit to show that

$$\frac{v_{o1}}{v_i} = \frac{R_E}{R_E + r_e}$$

$$\frac{v_{o2}}{v_i} = \frac{-\alpha R_C}{R_E + r_e}$$

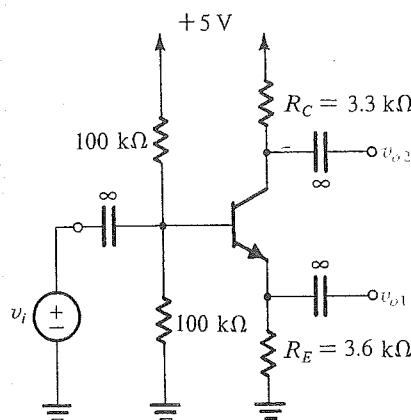


Figure P7.58

Find the values of these voltage gains (for  $\alpha \approx 1$ ). Now, if the terminal labeled  $v_{o1}$  is connected to ground, what does the voltage gain  $v_{o2}/v_i$  become?

### Section 7.3: Basic Configurations

7.59 An amplifier with an input resistance of  $100 \text{ k}\Omega$ , an open-circuit voltage gain of  $100 \text{ V/V}$ , and an output resistance of  $100 \Omega$  is connected between a  $20\text{-k}\Omega$  signal source and a  $2\text{-k}\Omega$  load. Find the overall voltage gain  $G_v$ . Also find the current gain, defined as the ratio of the load current to the current drawn from the signal source.

D 7.60 Specify the parameters  $R_{in}$ ,  $A_{vo}$ , and  $R_o$  of an amplifier that is to be connected between a  $100\text{-k}\Omega$  source and a  $2\text{-k}\Omega$  load and is required to meet the following specifications:

- No more than 5% of the signal strength is lost in the connection to the amplifier input;
- If the load resistance changes from the nominal value of  $2\text{k}\Omega$  to a low value of  $1\text{k}\Omega$ , the change in output voltage is limited to 5% of nominal value; and
- The nominal overall voltage gain is  $10 \text{ V/V}$ .

7.61 Figure P7.61 shows an alternative equivalent-circuit representation of an amplifier. If this circuit is to be equivalent to that in Fig. 7.34(b) show that  $G_m = A_{vo}/R_o$ . Also convince yourself that the transconductance  $G_m$  is defined as

$$G_m = \left. \frac{i_o}{v_i} \right|_{R_L=0}$$

and hence is known as the short-circuit transconductance. Now, if the amplifier is fed with a signal source ( $v_{sig}, R_{sig}$ ) and is connected to a load resistance  $R_L$  show that the gain of the amplifier proper  $A_v$  is given by  $A_v = G_m(R_o \parallel R_L)$  and the overall voltage gain  $G_v$  is given by

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} G_m (R_o \parallel R_L)$$

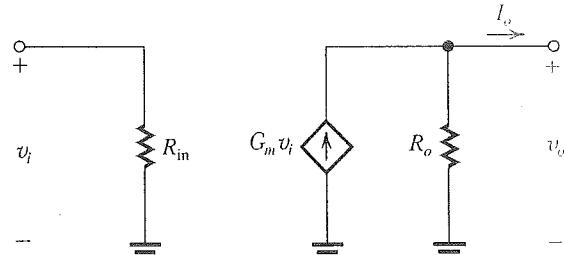


Figure P7.61

7.62 An alternative equivalent circuit of an amplifier fed with a signal source ( $v_{sig}, R_{sig}$ ) and connected to a load  $R_L$  is shown in Fig. P7.62. Here  $G_{vo}$  is the open-circuit overall voltage gain,

$$G_{vo} = \left. \frac{v_o}{v_{sig}} \right|_{R_L=\infty}$$

and  $R_{\text{out}}$  is the output resistance with  $v_{\text{sig}}$  set to zero. This is different than  $R_o$ . Show that

$$G_{vo} = \frac{R_i}{R_i + R_{\text{sig}}} A_{vo}$$

where  $R_i = R_{\text{in}}|_{R_L=\infty}$ .

Also show that the overall voltage gain is

$$G_v = G_{vo} \frac{R_L}{R_L + R_{\text{out}}}$$

**\*\*7.63** Most practical amplifiers have internal feedback that make them non-unilateral. In such a case,  $R_{\text{in}}$  depends on  $R_L$ . To illustrate this point we show in Fig. P7.63 the equivalent circuit of an amplifier where a feedback resistance  $R_f$  models the internal feedback mechanism that is present in this amplifier. It is  $R_f$  that makes the amplifier non-unilateral. Show that

$$R_{\text{in}} = R_1 \parallel \left[ \frac{R_f + (R_2 \parallel R_L)}{1 + g_m(R_2 \parallel R_L)} \right]$$

$$A_{vo} = -g_m R_2 \frac{1 - 1/(g_m R_f)}{1 + (R_2/R_f)}$$

$$R_o = R_2 \parallel R_f$$

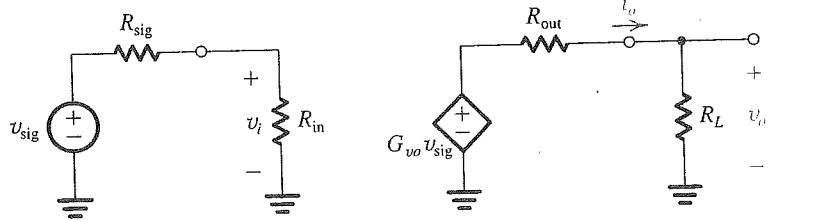


Figure P7.62

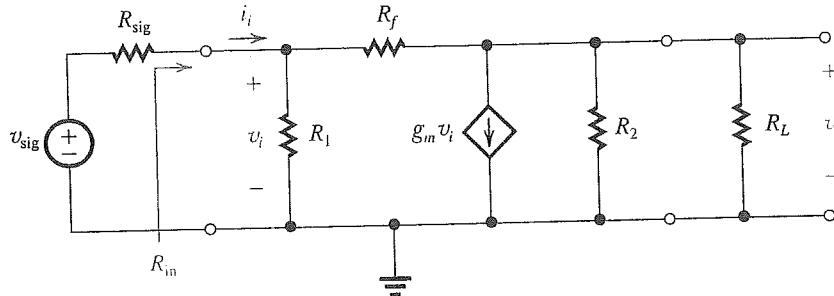


Figure P7.63

Evaluate  $R_{\text{in}}$ ,  $A_{vo}$ , and  $R_o$  for the case  $R_1 = 100 \text{ k}\Omega$ ,  $R_f = 1 \text{ M}\Omega$ ,  $g_m = 100 \text{ mA/V}$ ,  $R_2 = 100 \Omega$ , and  $R_L = 1 \text{ k}\Omega$ . Which of the amplifier characteristic parameters is most affected by  $R_f$  (that is, relative to the case with  $R_f = \infty$ )? For  $R_{\text{sig}} = 100 \text{ k}\Omega$  determine the overall voltage gain,  $G_v$ , with and without  $R_f$  present.

**7.64** Calculate the overall voltage gain of a CS amplifier fed with a  $1-\text{M}\Omega$  source and connected to a  $10-\text{k}\Omega$  load. The MOSFET has  $g_m = 2 \text{ mA/V}$ , and a drain resistance  $R_D = 10 \text{ k}\Omega$  is utilized.

**7.65** A CS amplifier utilizes a MOSFET with  $\mu_n C_{ox} = 400 \mu\text{A/V}^2$  and  $W/L = 10$ . It is biased at  $I_D = 320 \mu\text{A}$  and uses  $R_D = 10 \text{ k}\Omega$ . Find  $R_{\text{in}}$ ,  $A_{vo}$ , and  $R_o$ . Also, if a load resistance of  $10 \text{ k}\Omega$  is connected to the output, what overall voltage gain  $G_v$  is realized? Now, if a  $0.2\text{-V}$  peak sine-wave signal is required at the output, what must the peak amplitude of  $v_{\text{sig}}$  be?

**7.66** A common-source amplifier utilizes a MOSFET operated at  $V_{ov} = 0.25 \text{ V}$ . The amplifier feeds a load resistance  $R_L = 15 \text{ k}\Omega$ . The designer selects  $R_D = 2R_L$ . If it is required to realize an overall voltage gain  $G_v$  of  $-10 \text{ V/V}$  what  $g_m$  is needed? Also specify the bias current  $I_D$ . If, to increase the output signal swing,  $R_D$  is reduced to  $R_D = R_L$ , what does  $G_v$  become?

= Multisim/PSpice; \* = difficult problem; \*\* = more difficult; \*\*\* = very challenging; D = design problem

**7.67** Two identical CS amplifiers are connected in cascade. The first stage is fed with a source  $v_{sig}$  having a resistance  $R_{sig} = 200 \text{ k}\Omega$ . A load resistance  $R_L = 10 \text{ k}\Omega$  is connected to the drain of the second stage. Each MOSFET is biased at  $I_D = 0.3 \text{ mA}$  and operates with  $V_{ov} = 0.2 \text{ V}$ . Each stage utilizes a drain resistance  $R_D = 10 \text{ k}\Omega$ .

- (a) Sketch the equivalent circuit of the two-stage amplifier.
- (b) Calculate the overall voltage gain  $G_v$ .

**7.68** A CE amplifier utilizes a BJT with  $\beta = 100$  biased at  $I_C = 0.5 \text{ mA}$ ; it has a collector resistance  $R_C = 10 \text{ k}\Omega$ . Find  $R_{in}$ ,  $R_{out}$ , and  $A_{vo}$ . If the amplifier is fed with a signal source having a resistance of  $10 \text{ k}\Omega$ , and a load resistance  $R_L = 10 \text{ k}\Omega$  is connected to the output terminal, find the resulting  $A_v$  and  $G_v$ . If the peak voltage of the sine wave appearing between base and emitter is to be limited to  $5 \text{ mV}$ , what  $\hat{v}_{sig}$  is allowed, and what output voltage signal appears across the load?

**D \*7.69** In this problem we investigate the effect of the inevitable variability of  $\beta$  on the realized gain of the CE amplifier. For this purpose, use the overall gain expression in Eq. (7.114).

$$|G_v| = \frac{R'_L}{(R_{sig}/\beta) + (1/g_m)}$$

where  $R'_L = R_L \parallel R_C$ .

Consider the case  $R'_L = 10 \text{ k}\Omega$  and  $R_{sig} = 10 \text{ k}\Omega$ , and let the BJT be biased at  $I_C = 1 \text{ mA}$ . The BJT has a nominal  $\beta$  of 100.

- (a) What is the nominal value of  $|G_v|$ ?
- (b) If  $\beta$  can be anywhere between 50 and 150, what is the corresponding range of  $|G_v|$ ?
- (c) If in a particular design, it is required to maintain  $|G_v|$  within  $\pm 20\%$  of its nominal value, what is the maximum allowable range of  $\beta$ ?
- (d) If it is not possible to restrict  $\beta$  to the range found in (c), and the designer has to contend with  $\beta$  in the range 50 to 150, what value of bias current  $I_C$  would result in  $|G_v|$  falling in a range of  $\pm 20\%$  of a new nominal value? What is the nominal value of  $|G_v|$  in this case?

**7.70** Two identical CE amplifiers are connected in cascade. The first stage is fed with a source  $v_{sig}$  having a resistance  $R_{sig} = 10 \text{ k}\Omega$ . A load resistance  $R_L = 10 \text{ k}\Omega$  is connected to the collector of the second stage. Each BJT is biased at  $I_C = 0.25 \text{ mA}$  and has  $\beta = 100$ . Each stage utilizes a collector resistance  $R_C = 10 \text{ k}\Omega$ .

- (a) Sketch the equivalent circuit of the two-stage amplifier.
- (b) Find the overall voltage gain,  $v_{o2}/v_{sig}$ .

**7.71** A MOSFET connected in the CS configuration has a transconductance  $g_m = 5 \text{ mA/V}$ . When a resistance  $R_s$  is connected in the source lead, the effective transconductance is reduced to  $2 \text{ mA/V}$ . What do you estimate the value of  $R_s$  to be?

**7.72** A CS amplifier using an NMOS transistor with  $g_m = 2 \text{ mA/V}$  is found to have an overall voltage gain of  $-10 \text{ V/V}$ . What value should a resistance  $R_s$  inserted in the source lead have to reduce the overall voltage gain to  $-5 \text{ V/V}$ ?

**7.73** The overall voltage gain of a CS amplifier with a resistance  $R_s = 0.5 \text{ k}\Omega$  in the source lead was measured and found to be  $-10 \text{ V/V}$ . When  $R_s$  was shorted, but the circuit operation remained linear, the gain doubled. What must  $g_m$  be? What value of  $R_s$  is needed to obtain an overall voltage gain of  $-16 \text{ V/V}$ ?

**7.74** A CE amplifier utilizes a BJT with  $\beta = 100$  biased at  $I_C = 0.5 \text{ mA}$  and has a collector resistance  $R_C = 12 \text{ k}\Omega$  and a resistance  $R_e = 250 \Omega$  connected in the emitter. Find  $R_{in}$ ,  $A_{vo}$ , and  $R_{out}$ . If the amplifier is fed with a signal source having a resistance of  $10 \text{ k}\Omega$ , and a load resistance  $R_L = 12 \text{ k}\Omega$  is connected to the output terminal, find the resulting  $A_v$  and  $G_v$ . If the peak voltage of the sine wave appearing between base and emitter is to be limited to  $5 \text{ mV}$ , what  $\hat{v}_{sig}$  is allowed, and what output voltage signal appears across the load?

**D 7.75** Design a CE amplifier with a resistance  $R_e$  in the emitter to meet the following specifications:

- (i) Input resistance  $R_{in} = 15 \text{ k}\Omega$ .
- (ii) When fed from a signal source with a peak amplitude of  $0.15 \text{ V}$  and a source resistance of  $30 \text{ k}\Omega$ , the peak amplitude of  $v_o$  is  $5 \text{ mV}$ .

Specify  $R_e$  and the bias current  $I_C$ . The BJT has  $\beta = 74$ . If the total resistance in the collector is  $6 \text{ k}\Omega$ , find the overall voltage gain  $G_v$  and the peak amplitude of the output signal  $v_o$ .

**SIM D 7.76** Inclusion of an emitter resistance  $R_e$  reduces the variability of the gain  $G_v$  due to the inevitable wide variance in the value of  $\beta$ . Consider a CE amplifier operating between a signal source with  $R_{sig} = 10 \text{ k}\Omega$  and a total collector resistance  $R_C \parallel R_L$  of  $10 \text{ k}\Omega$ . The BJT is biased at  $I_C = 1 \text{ mA}$  and its  $\beta$  is specified to be nominally 100 but can lie in the range of 50 to 150. First determine the nominal value and the range of

$|G_v|$  without resistance  $R_e$ . Then select a value for  $R_e$  that will ensure that  $|G_v|$  be within  $\pm 20\%$  of its new nominal value. Specify the value of  $R_e$ , the new nominal value of  $|G_v|$ , and the expected range of  $|G_v|$ .

7.77 A CG amplifier using an NMOS transistor for which  $g_m = 2 \text{ mA/V}$  has a  $5\text{-k}\Omega$  drain resistance  $R_D$  and a  $5\text{-k}\Omega$  load resistance  $R_L$ . The amplifier is driven by a voltage source having a  $750\text{-}\Omega$  resistance. What is the input resistance of the amplifier? What is the overall voltage gain  $G_v$ ? By what factor must the bias current  $I_D$  of the MOSFET be changed so that  $R_{in}$  matches  $R_{sig}$ ?

7.78 A CG amplifier when fed with a signal source having  $R_{sig} = 100 \Omega$  is found to have an overall voltage gain of  $12 \text{ V/V}$ . When a  $100\text{-}\Omega$  resistance was added in series with the signal generator the overall voltage gain decreased to  $10 \text{ V/V}$ . What must  $g_m$  of the MOSFET be? If the MOSFET is biased at  $I_D = 0.25 \text{ mA}$ , at what overdrive voltage must it be operating?

D 7.79 A CB amplifier is operating with  $R_L = 10 \text{ k}\Omega$ ,  $R_C = 10 \text{ k}\Omega$ , and  $R_{sig} = 50 \Omega$ . At what current  $I_C$  should the transistor be biased for the input resistance  $R_{in}$  to equal that of the signal source? What is the resulting overall voltage gain? Assume  $\alpha \approx 1$ .

7.80 For the circuit in Fig. P7.80, let  $R_{sig} \gg r_e$  and  $\alpha \approx 1$ . Find  $v_o$ .

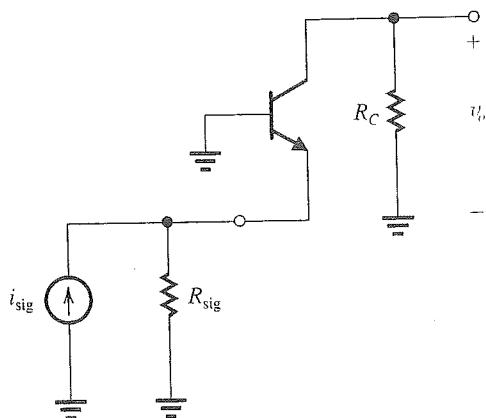


Figure P7.80

7.81 A CB amplifier is biased at  $I_E = 0.2 \text{ mA}$  with  $R_C = R_L = 10 \text{ k}\Omega$  and is driven by a signal source with  $R_{sig} = 0.5 \text{ k}\Omega$ . Find the overall voltage gain  $G_v$ . If the maximum signal amplitude of the voltage between base and emitter is limited to  $10 \text{ mV}$ ,

what are the corresponding amplitudes of  $v_{sig}$  and  $v_o$ ? Assume  $\alpha \approx 1$ .

7.82 A source follower is required to connect a high-resistance source to a load whose resistance is nominally  $2 \text{ k}\Omega$  but can be as low as  $1.5 \text{ k}\Omega$  and as high as  $5 \text{ k}\Omega$ . What is the maximum output resistance that the source follower must have if the output voltage is to remain within  $\pm 10\%$  of nominal value? If the MOSFET has  $k_n = 2.5 \text{ mA/V}^2$ , at what current  $I_D$  must it be biased? At what overdrive voltage is the MOSFET operating?

D 7.83 A source follower is required to deliver a  $0.5\text{-V}$  peak sinusoid to a  $2\text{-k}\Omega$  load. If the peak amplitude of  $v_{gs}$  is to be limited to  $50 \text{ mV}$ , and the MOSFET transconductance parameter  $k_n = 5 \text{ mA/V}^2$ , what is the lowest value of  $I_D$  at which the MOSFET can be biased? At this bias current, what are the maximum and minimum currents that the MOSFET will be conducting (at the positive and negative peaks of the output sine wave)? What must the peak amplitude of  $v_{sig}$  be?

D 7.84 An emitter follower is required to deliver a  $0.5\text{-V}$  peak sinusoid to a  $2\text{-k}\Omega$  load. If the peak amplitude of  $v_{be}$  is to be limited to  $5 \text{ mV}$ , what is the lowest value of  $I_E$  at which the BJT can be biased? At this bias current, what are the maximum and minimum currents that the BJT will be conducting (at the positive and negative peaks of the output sine wave)? If the resistance of the signal source is  $200 \text{ k}\Omega$ , what value of  $G_v$  is obtained? Thus determine the required amplitude of  $v_{sig}$ . Assume  $\beta = 100$ .

7.85 An emitter follower with a BJT biased at  $I_c = 2 \text{ mA}$  and having  $\beta = 100$  is connected between a source with  $R_{sig} = 10 \text{ k}\Omega$  and a load  $R_L = 0.5 \text{ k}\Omega$ :

- Find  $R_{in}$ ,  $v_b/v_{sig}$ , and  $v_o/v_{sig}$ .
- If the signal amplitude across the base-emitter junction is to be limited to  $10 \text{ mV}$ , what is the corresponding amplitude of  $v_{sig}$  and  $v_o$ ?
- Find the open-circuit voltage gain  $G_{vo}$  and the output resistance  $R_{out}$ . Use these values first to verify the value of  $G_v$  obtained in (a), then to find the value of  $G_v$  obtained with  $R_L$  reduced to  $250 \Omega$ .

7.86 An emitter follower is operating at a collector bias current of  $0.5 \text{ mA}$  and is used to connect a  $10\text{-k}\Omega$  source to a  $1\text{-k}\Omega$  load. If the nominal value of  $\beta$  is  $100$ , what output resistance  $R_{out}$  and overall voltage gain  $G_v$  result? Now if

transistor  $\beta$  is specified to lie in the range 50 to 150, find the corresponding range of  $R_{\text{out}}$  and  $G_v$ .

**7.87** An emitter follower, when driven from a 5-k $\Omega$  source, was found to have an output resistance  $R_{\text{out}}$  of 150  $\Omega$ . The output resistance increased to 250  $\Omega$  when the source resistance was increased to 10 k $\Omega$ . Find the overall voltage gain when the follower is driven by a 10-k $\Omega$  source and loaded by a 1-k $\Omega$  resistor.

**7.88** For the general amplifier circuit shown in Fig. P7.88 neglect the Early effect.

- (a) Find expressions for  $v_c/v_{\text{sig}}$  and  $v_o/v_{\text{sig}}$ .
- (b) If  $v_{\text{sig}}$  is disconnected from node X, node X is grounded, and node Y is disconnected from ground and connected to  $v_{\text{sig}}$ , find the new expression for  $v_c/v_{\text{sig}}$ .

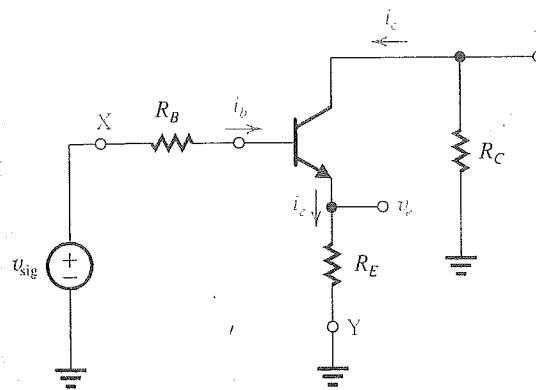


Figure P7.88

**7.89** When the Early effect is neglected, the overall voltage gain of a CE amplifier with a collector resistance  $R_C = 10 \text{ k}\Omega$  is calculated to be  $-100 \text{ V/V}$ . If the BJT is biased at  $I_C = 1 \text{ mA}$  and the Early voltage is 100 V, provide a better estimate of the voltage gain  $G_v$ .

**\*7.90** Show that when  $r_o$  is taken into account, the voltage gain of the source follower becomes

$$G_v = \frac{v_o}{v_{\text{sig}}} = \frac{R_L \parallel r_o}{(R_L \parallel r_o) + \frac{1}{g_m}}$$

Now, with  $R_L$  removed, the voltage gain is carefully measured and found to be 0.98. Then, when  $R_L$  is connected and its value is varied, it is found that the gain is halved at  $R_L = 500 \Omega$ . If the amplifier remained linear throughout this measurement, what must the values of  $g_m$  and  $r_o$  be?

**D 7.91** In this problem, we investigate the effect of changing the bias current  $I_C$  on the overall voltage gain  $G_v$  of a CE amplifier. Consider the situation of a CE amplifier operating with a signal source having  $R_{\text{sig}} = 10 \text{ k}\Omega$  and having  $R_C \parallel R_L = 10 \text{ k}\Omega$ . The BJT is specified to have  $\beta = 100$  and  $V_A = 25 \text{ V}$ . Use Eq. (7.114) (with  $r_o$  included in parallel with  $R_C$  and  $R_L$  in the numerator) to find  $|G_v|$  at  $I_C = 0.1 \text{ mA}, 0.2 \text{ mA}, 0.5 \text{ mA}, 1.0 \text{ mA}$ , and  $1.25 \text{ mA}$ . Observe the effect of  $r_o$  on limiting  $|G_v|$  as  $I_C$  is increased. Find the value of  $I_C$  that results in  $|G_v| = 50 \text{ V/V}$ .

### Section 7.4: Biasing

**D 7.92** Consider the classical biasing scheme shown in Fig. 7.48(c), using a 9-V supply. For the MOSFET,  $V_t = 1 \text{ V}$ ,  $\lambda = 0$ , and  $k_n = 2 \text{ mA/V}^2$ . Arrange that the drain current is 1 mA, with about one-third of the supply voltage across each of  $R_s$  and  $R_D$ . Use 22 M $\Omega$  for the larger of  $R_{G1}$  and  $R_{G2}$ . What are the values of  $R_{G1}$ ,  $R_{G2}$ ,  $R_s$ , and  $R_D$  that you have chosen? Specify them to two significant digits. For your design, how far is the drain voltage from the edge of saturation?

**D 7.93** Using the circuit topology displayed in Fig. 7.48(e), arrange to bias the NMOS transistor at  $I_D = 0.5 \text{ mA}$  with  $V_D$  midway between cutoff and the beginning of triode operation. The available supplies are  $\pm 5 \text{ V}$ . For the NMOS transistor,  $V_t = 1.0 \text{ V}$ ,  $\lambda = 0$ , and  $k_n = 1 \text{ mA/V}^2$ . Use a gate-bias resistor of 10 M $\Omega$ . Specify  $R_s$  and  $R_D$  to two significant digits.

**D \*7.94** In an electronic instrument using the biasing scheme shown in Fig. 7.48(c), a manufacturing error reduces  $R_s$  to zero. Let  $V_{DD} = 15 \text{ V}$ ,  $R_{G1} = 10 \text{ M}\Omega$ , and  $R_{G2} = 5.1 \text{ M}\Omega$ . What is the value of  $V_G$  created? If supplier specifications allow  $k_n$  to vary from 0.2 to 0.3 mA/V $^2$  and  $V_t$  to vary from 1.0 V to 1.5 V, what are the extreme values of  $I_D$  that may result? What value of  $R_s$  should have been installed to limit the maximum value of  $I_D$  to 1.5 mA? Choose an appropriate standard 5% resistor value (refer to Appendix J). What extreme values of current now result?

**7.95** An NMOS transistor is connected in the bias circuit of Fig. 7.48(c), with  $V_G = 5 \text{ V}$  and  $R_s = 3 \text{ k}\Omega$ . The transistor has  $V_t = 1 \text{ V}$  and  $k_n = 2 \text{ mA/V}^2$ . What bias current results? If a transistor for which  $k_n$  is 50% higher is used, what is the resulting percentage increase in  $I_D$ ?

**SIM 7.96** The bias circuit of Fig. 7.48(c) is used in a design with  $V_G = 5 \text{ V}$  and  $R_s = 2 \text{ k}\Omega$ . For a MOSFET with

$k_n = 2 \text{ mA/V}^2$ , the source voltage was measured and found to be 2 V. What must  $V_t$  be for this device? If a device for which  $V_t$  is 0.5 V less is used, what does  $V_s$  become? What bias current results?

**D 7.97** Design the circuit of Fig. 7.48(e) for a MOSFET having  $V_t = 1 \text{ V}$  and  $k'_n W/L = 4 \text{ mA/V}^2$ . Let  $V_{DD} = V_{SS} = 5 \text{ V}$ . Design for a dc bias current of 0.5 mA and for the largest possible voltage gain (and thus the largest possible  $R_D$ ) consistent with allowing a 2-V peak-to-peak voltage swing at the drain. Assume that the signal voltage on the source terminal of the FET is zero.

**SIM D 7.98** Design the circuit in Fig. P7.98 so that the transistor operates in saturation with  $V_D$  biased 1 V from the edge of the triode region, with  $I_D = 1 \text{ mA}$  and  $V_D = 3 \text{ V}$ , for each of the following two devices (use a 10- $\mu\text{A}$  current in the voltage divider):

- (a)  $|V_t| = 1 \text{ V}$  and  $k'_n W/L = 0.5 \text{ mA/V}^2$
- (b)  $|V_t| = 2 \text{ V}$  and  $k'_n W/L = 1.25 \text{ mA/V}^2$

For each case, specify the values of  $V_G$ ,  $V_D$ ,  $V_S$ ,  $R_1$ ,  $R_2$ ,  $R_S$ , and  $R_D$ .

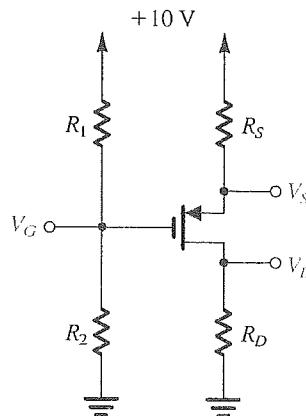


Figure P7.98

**D \*\*7.99** A very useful way to characterize the stability of the bias current  $I_D$  is to evaluate the sensitivity of  $I_D$  relative to a particular transistor parameter whose variability might be large. The sensitivity of  $I_D$  relative to the MOSFET parameter  $K \equiv \frac{1}{2} k' (W/L)$  is defined as

$$S_K^{I_D} \equiv \frac{\partial I_D / I_D}{\partial K / K} = \frac{\partial I_D}{\partial K} \frac{K}{I_D}$$

and its value, when multiplied by the variability (or tolerance) of  $K$ , provides the corresponding expected variability of  $I_D$ ,

$$\frac{\Delta I_D}{I_D} = S_K^{I_D} \left( \frac{\Delta K}{K} \right)$$

The purpose of this problem is to investigate the use of the sensitivity function in the design of the bias circuit of Fig. 7.48(e).

- (a) Show that for  $V_t$  constant,

$$S_K^{I_D} = 1 / \left( 1 + 2\sqrt{KI_D}R_S \right)$$

- (b) For a MOSFET having  $K = 100 \mu\text{A/V}^2$  with a variability of  $\pm 10\%$  and  $V_t = 1 \text{ V}$ , find the value of  $R_S$  that would result in  $I_D = 100 \mu\text{A}$  with a variability of  $\pm 1\%$ . Also, find  $V_{GS}$  and the required value of  $V_{SS}$ .
- (c) If the available supply  $V_{SS} = 5 \text{ V}$ , find the value of  $R_S$  for  $I_D = 100 \mu\text{A}$ . Evaluate the sensitivity function, and give the expected variability of  $I_D$  in this case.

**D \*\*7.100** The variability ( $\Delta I_D / I_D$ ) in the bias current  $I_D$  due to the variability ( $\Delta V_t / V_t$ ) in the threshold voltage  $V_t$  can be evaluated from

$$\frac{\Delta I_D}{I_D} = S_{V_t}^{I_D} \left( \frac{\Delta V_t}{V_t} \right)$$

where  $S_{V_t}^{I_D}$ , the sensitivity of  $I_D$  relative to  $V_t$ , is defined as

$$S_{V_t}^{I_D} = \frac{\partial I_D}{\partial V_t} \frac{V_t}{I_D}$$

- (a) For the case of a MOSFET biased with a fixed  $V_{GS}$ , show that

$$S_{V_t}^{I_D} = - \frac{2V_t}{V_{ov}}$$

and find the variability in  $I_D$  for  $V_t = 0.5 \text{ V}$  and  $\Delta V_t / V_t = \pm 5\%$ . Let the MOSFET be biased at  $V_{ov} = 0.25 \text{ V}$ .

- (b) For the case of a MOSFET biased with a fixed gate voltage  $V_G$  and a resistance  $R_S$  included in the source lead, show that

$$S_{V_t}^{I_D} = - \frac{2V_t}{V_{ov} + 2I_D R_S}$$

For the same parameters given in (a), find the required value of  $(I_D R_S)$  and  $V_G$  to limit  $\Delta I_D / I_D$  to  $\pm 5\%$ . What value of  $R_S$  is needed if  $I_D$  is  $100 \mu\text{A}$ ?

**SIM** 7.101 In the circuit of Fig. 7.50, let  $R_G = 10 \text{ M}\Omega$ ,  $R_D = 10 \text{ k}\Omega$ , and  $V_{DD} = 10 \text{ V}$ . For each of the following two transistors, find the voltages  $V_D$  and  $V_G$ .

- (a)  $V_t = 1 \text{ V}$  and  $k_n = 0.5 \text{ mA/V}^2$
- (b)  $V_t = 2 \text{ V}$  and  $k_n = 1.25 \text{ mA/V}^2$

D 7.102 Using the feedback bias arrangement shown in Fig. 7.50 with a 5-V supply and an NMOS device for which  $V_t = 1 \text{ V}$  and  $k_n = 10 \text{ mA/V}^2$ , find  $R_D$  to establish a drain current of 0.2 mA.

D 7.103 Figure P7.103 shows a variation of the feedback-bias circuit of Fig. 7.50. Using a 5-V supply with an NMOS transistor for which  $V_t = 0.8 \text{ V}$ ,  $k_n = 8 \text{ mA/V}^2$ , and  $\lambda = 0$ , provide a design that biases the transistor at  $I_D = 1 \text{ mA}$ , with  $V_{DS}$  large enough to allow saturation operation for a 2-V negative signal swing at the drain. Use  $22 \text{ M}\Omega$  as the largest resistor in the feedback-bias network. What values of  $R_{G1}$  and  $R_{G2}$  have you chosen? Specify all resistors to two significant digits.

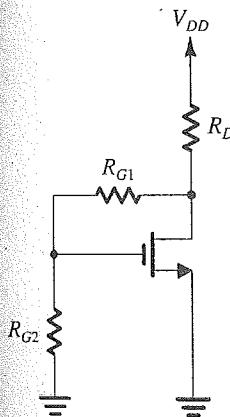


Figure P7.103

D 7.104 For the circuit in Fig. 7.51(a), neglect the base current  $I_B$  in comparison with the current in the voltage divider. It is required to bias the transistor at  $I_C = 1 \text{ mA}$ , which requires selecting  $R_{B1}$  and  $R_{B2}$  so that  $V_{BE} = 0.710 \text{ V}$ . If  $V_{CC} = 3 \text{ V}$ , what must the ratio  $R_{B1}/R_{B2}$  be? Now, if  $R_{B1}$  and  $R_{B2}$  are 1% resistors, that is, each can be in the range of 0.99 to 1.01 of its nominal value, what is the range obtained for  $V_{BE}$ ? What is the corresponding range of  $I_C$ ? If  $R_C = 2 \text{ k}\Omega$ , what is

the range obtained for  $V_{CE}$ ? Comment on the efficacy of this biasing arrangement.

D 7.105 It is required to bias the transistor in the circuit of Fig. 7.51(b) at  $I_C = 1 \text{ mA}$ . The transistor  $\beta$  is specified to be nominally 100, but it can fall in the range of 50 to 150. For  $V_{CC} = +3 \text{ V}$  and  $R_C = 2 \text{ k}\Omega$ , find the required value of  $R_B$  to achieve  $I_C = 1 \text{ mA}$  for the "nominal" transistor. What is the expected range for  $I_C$  and  $V_{CE}$ ? Comment on the efficacy of this bias design.

D 7.106 Consider the single-supply bias network shown in Fig. 7.52(a). Provide a design using a 9-V supply in which the supply voltage is equally split between  $R_C$ ,  $V_{CE}$ , and  $R_E$  with a collector current of 0.6 mA. The transistor  $\beta$  is specified to have a minimum value of 90. Use a voltage-divider current of  $I_E/10$ , or slightly higher. Since a reasonable design should operate for the best transistors for which  $\beta$  is very high, do your initial design with  $\beta = \infty$ . Then choose suitable 5% resistors (see Appendix J), making the choice in a way that will result in a  $V_{BB}$  that is slightly higher than the ideal value. Specify the values you have chosen for  $R_E$ ,  $R_C$ ,  $R_I$ , and  $R_2$ . Now, find  $V_B$ ,  $V_E$ ,  $V_C$ , and  $I_C$  for your final design using  $\beta = 90$ .

D 7.107 Repeat Problem 7.106, but use a voltage-divider current that is  $I_E/2$ . Check your design at  $\beta = 90$ . If you have the data available, find how low  $\beta$  can be while the value of  $I_C$  does not fall below that obtained with the design of Problem 7.106 for  $\beta = 90$ .

D \*7.108 It is required to design the bias circuit of Fig. 7.52 for a BJT whose nominal  $\beta = 100$ .

- (a) Find the largest ratio  $(R_B/R_E)$  that will guarantee  $I_E$  remains within  $\pm 5\%$  of its nominal value for  $\beta$  as low as 50 and as high as 150.
- (b) If the resistance ratio found in (a) is used, find an expression for the voltage  $V_{BB} \equiv V_{CC}R_2/(R_1 + R_2)$  that will result in a voltage drop of  $V_{CC}/3$  across  $R_E$ .
- (c) For  $V_{CC} = 5 \text{ V}$ , find the required values of  $R_1$ ,  $R_2$ , and  $R_E$  to obtain  $I_E = 0.5 \text{ mA}$  and to satisfy the requirement for stability of  $I_E$  in (a).
- (d) Find  $R_C$  so that  $V_{CE} = 1.0 \text{ V}$  for  $\beta$  equal to its nominal value.

Check your design by evaluating the resulting range of  $I_E$ .

**D \*7.109** Consider the two-supply bias arrangement shown in Fig. 7.53 using  $\pm 5$ -V supplies. It is required to design the circuit so that  $I_C = 0.5$  mA and  $V_C$  is placed 2 V above  $V_E$ .

- For  $\beta = \infty$ , what values of  $R_E$  and  $R_C$  are required?
- If the BJT is specified to have a minimum  $\beta$  of 50, find the largest value for  $R_B$  consistent with the need to limit the voltage drop across it to one-tenth the voltage drop across  $R_E$ .
- What standard 5% resistor values (see Appendix J) would you use for  $R_B$ ,  $R_E$ , and  $R_C$ ? In making your selection, use somewhat lower values in order to compensate for the low- $\beta$  effects.
- For the values you selected in (c), find  $I_C$ ,  $V_B$ ,  $V_E$ , and  $V_C$  for  $\beta = \infty$  and for  $\beta = 50$ .

**D \*7.110** Utilizing  $\pm 3$ -V power supplies, it is required to design a version of the circuit in Fig. 7.53 in which the signal will be coupled to the emitter and thus  $R_B$  can be set to zero. Find values for  $R_E$  and  $R_C$  so that a dc emitter current of 0.4 mA is obtained and so that the gain is maximized while allowing  $\pm 1$  V of signal swing at the collector. If temperature increases from the nominal value of  $25^\circ\text{C}$  to  $125^\circ\text{C}$ , estimate the percentage change in collector bias current. In addition to the  $-2\text{ mV}/^\circ\text{C}$  change in  $V_{BE}$ , assume that the transistor  $\beta$  changes over this temperature range from 50 to 150.

**SIM D 7.111** Using a 3-V power supply, design a version of the circuit of Fig. 7.54 to provide a dc emitter current of 0.5 mA and to allow a  $\pm 1$ -V signal swing at the collector. The BJT has a nominal  $\beta = 100$ . Use standard 5% resistor values (see Appendix J). If the actual BJT used has  $\beta = 50$ , what emitter current is obtained? Also, what is the allowable signal swing at the collector? Repeat for  $\beta = 150$ .

- Using a 3-V power supply, design the feedback bias circuit of Fig. 7.54 to provide  $I_C = 1$  mA and  $V_C = V_{CC}/2$  for  $\beta = 100$ .
- Select standard 5% resistor values, and reevaluate  $V_C$  and  $I_C$  for  $\beta = 100$ .
- Find  $V_C$  and  $I_C$  for  $\beta = \infty$ .
- To improve the situation that obtains when high- $\beta$  transistors are used, we have to arrange for an additional current to flow through  $R_B$ . This can be achieved by connecting a resistor between base and emitter, as shown in Fig. P7.112.

Design this circuit for  $\beta = 100$ . Use a current through  $R_B$  equal to the base current. Now, what values of  $V_C$  and  $I_C$  result with  $\beta = \infty$ ?

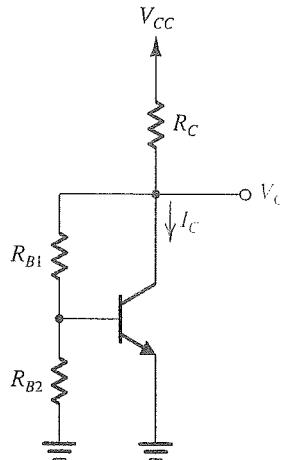


Figure P7.112

**D 7.113** A circuit that can provide a very large voltage gain for a high-resistance load is shown in Fig. P7.113. Find the values of  $I$  and  $R_B$  to bias the BJT at  $I_C = 1$  mA and  $V_C = 1.5$  V. Let  $\beta = 100$ .

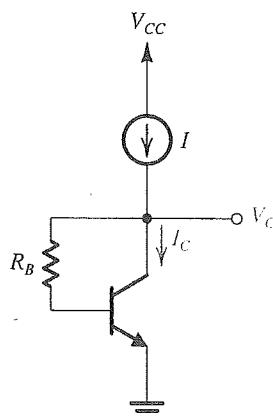


Figure P7.113

**7.114** The circuit in Fig. P7.114 provides a constant current  $I_O$  as long as the circuit to which the collector is

$R_{B2}$   
 $I_C$

connected maintains the BJT in the active mode. Show that

$$I_O = \alpha \frac{V_{CC} [R_2 / (R_1 + R_2)] - V_{BE}}{R_E + (R_1 \parallel R_2) / (\beta + 1)}$$

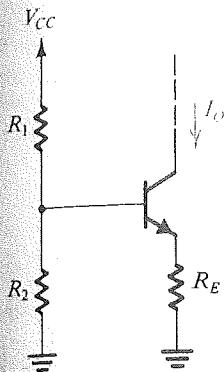


Figure P7.114

**SIM** **D** \*7.115 For the circuit in Fig. P7.115, assuming all transistors to be identical with  $\beta$  infinite, derive an expression for the output current  $I_O$ , and show that by selecting

$$R_1 = R_2$$

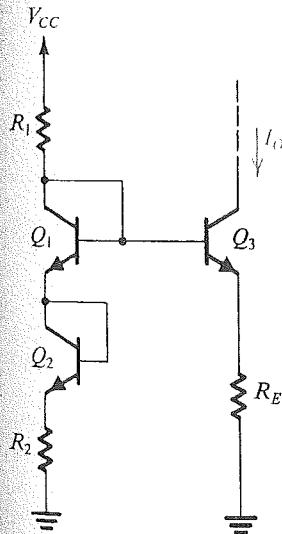


Figure P7.115

and keeping the current in each junction the same, the current  $I_O$  will be

$$I_O = \frac{V_{CC}}{2R_E}$$

which is independent of  $V_{BE}$ . What must the relationship of  $R_E$  to  $R_1$  and  $R_2$  be? For  $V_{CC} = 10$  V and  $V_{BE} = 0.7$  V, design the circuit to obtain an output current of 0.5 mA. What is the lowest voltage that can be applied to the collector of  $Q_3$ ?

**D** 7.116 For the circuit in Fig. P7.116 find the value of  $R$  that will result in  $I_O \approx 0.5$  mA. What is the largest voltage that can be applied to the collector? Assume  $|V_{BE}| = 0.7$  V.

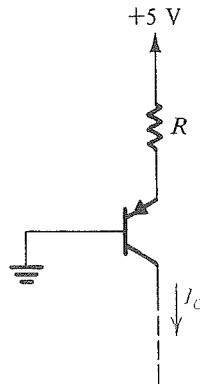


Figure P7.116

### Section 7.5: Discrete-Circuit Amplifiers

7.117 Calculate the overall voltage gain  $G_v$  of a common-source amplifier for which  $g_m = 3$  mA/V,  $r_o = 100$  k $\Omega$ ,  $R_D = 10$  k $\Omega$ , and  $R_G = 10$  M $\Omega$ . The amplifier is fed from a signal source with a Thévenin resistance of 1 M $\Omega$ , and the amplifier output is coupled to a load resistance of 20 k $\Omega$ .

**SIM** 7.118 The NMOS transistor in the CS amplifier shown in Fig. P7.118 has  $V_t = 0.7$  V and  $V_A = 50$  V.

- Neglecting the Early effect, verify that the MOSFET is operating in saturation with  $I_D = 0.5$  mA and  $V_{ov} = 0.3$  V. What must the MOSFET's  $k_n$  be? What is the dc voltage at the drain?
- Find  $R_{in}$  and  $G_v$ .
- If  $v_{sig}$  is a sinusoid with a peak amplitude  $\hat{v}_{sig}$ , find the maximum allowable value of  $\hat{v}_{sig}$  for which the transistor remains in saturation. What is the corresponding amplitude of the output voltage?

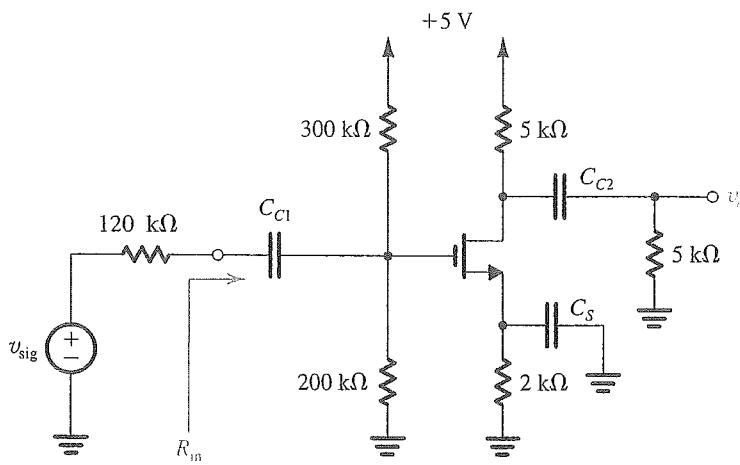


Figure P7.118

- (d) What is the value of resistance  $R_s$  that needs to be inserted in series with capacitor  $C_s$  in order to allow us to double the input signal  $\hat{v}_{sig}$ ? What output voltage now results?

**SIM D \*7.119** The PMOS transistor in the CS amplifier of Fig. P7.119 has  $V_p = -0.7$  V and a very large  $|V_A|$ .

- (a) Select a value for  $R_s$  to bias the transistor at  $I_D = 0.3$  mA and  $|V_{ov}| = 0.3$  V. Assume  $v_{sig}$  to have a zero dc component.
- (b) Select a value for  $R_D$  that results in  $G_v = -10$  V/V.

- (c) Find the largest sinusoid  $\hat{v}_{sig}$  that the amplifier can handle while remaining in the saturation region. What is the corresponding signal at the output?

- (d) If to obtain reasonably linear operation,  $\hat{v}_{sig}$  is limited to 50 mV, what value can  $R_D$  be increased to while maintaining saturation-region operation? What is the new value of  $G_v$ ?

7.120 Figure P7.120 shows a scheme for coupling and amplifying a high-frequency pulse signal. The circuit utilizes

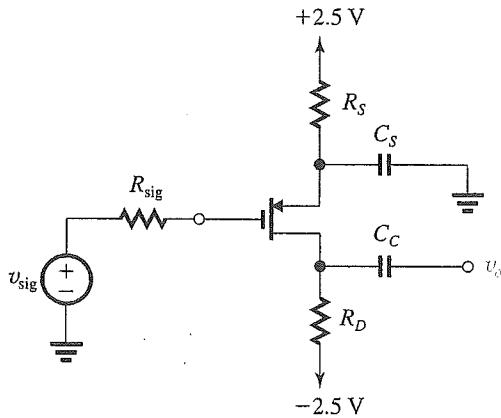


Figure P7.119

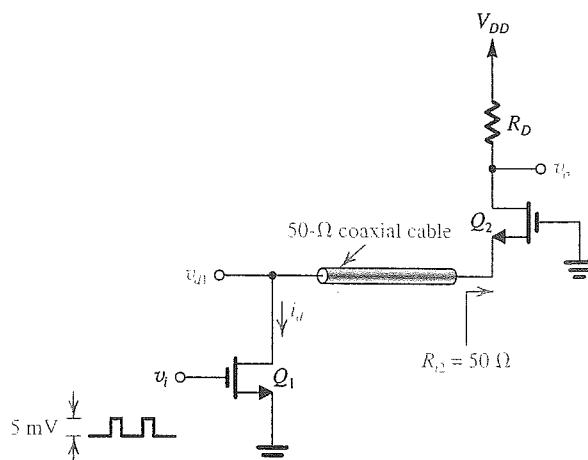


Figure P7.120

two MOSFETs whose bias details are not shown and a  $50\text{-}\Omega$  coaxial cable. Transistor  $Q_1$  operates as a CS amplifier and  $Q_2$  as a CG amplifier. For proper operation, transistor  $Q_2$  is required to present a  $50\text{-}\Omega$  resistance to the cable. This situation is known as "proper termination" of the cable and ensures that there will be no signal reflection coming back on the cable. When the cable is properly terminated, its input resistance is  $50\text{\Omega}$ . What must  $g_{m2}$  be? If  $Q_1$  is biased at the same point as  $Q_2$ , what is the amplitude of the current pulses in the drain of  $Q_1$ ? What is the amplitude of the voltage pulses at the drain of  $Q_1$ ? What value of  $R_D$  is required to provide 1-V pulses at the drain of  $Q_2$ ?

D \*7.121 The MOSFET in the circuit of Fig. P7.121 has  $V_t = 0.8\text{ V}$ ,  $k_u = 5\text{ mA/V}^2$ , and  $V_A = 40\text{ V}$ .

- Find the values of  $R_S$ ,  $R_D$ , and  $R_G$  so that  $I_D = 0.4\text{ mA}$ , the largest possible value for  $R_D$  is used while a maximum signal swing at the drain of  $\pm 0.8\text{ V}$  is possible, and the input resistance at the gate is  $10\text{ M}\Omega$ . Neglect the Early effect.
- Find the values of  $g_m$  and  $r_o$  at the bias point.
- If terminal Z is grounded, terminal X is connected to a signal source having a resistance of  $1\text{ M}\Omega$ , and terminal Y is connected to a load resistance of  $10\text{ k}\Omega$ , find the voltage gain from signal source to load.
- If terminal Y is grounded, find the voltage gain from X to Z with Z open-circuited. What is the output resistance of the source follower?

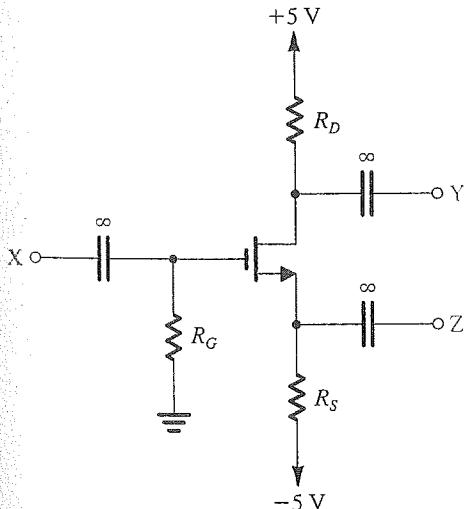
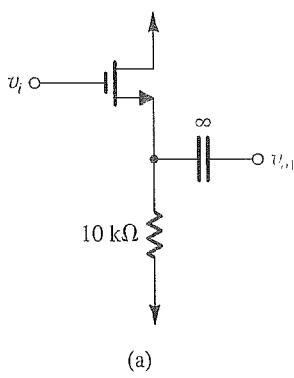


Figure P7.121

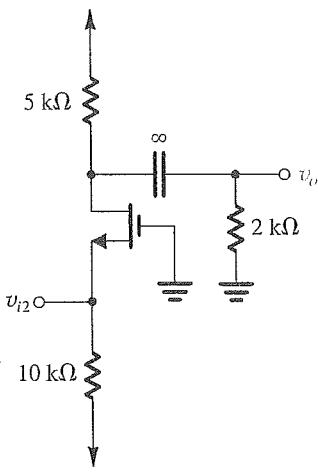
- If terminal X is grounded and terminal Z is connected to a current source delivering a signal current of  $50\text{ }\mu\text{A}$  and having a resistance of  $100\text{ k}\Omega$ , find the voltage signal that can be measured at Y. For simplicity, neglect the effect of  $r_o$ .

#### \*7.122

- The NMOS transistor in the source-follower circuit of Fig. P7.122(a) has  $g_m = 10\text{ mA/V}$  and a large  $r_o$ . Find the open-circuit voltage gain and the output resistance.
- The NMOS transistor in the common-gate amplifier of Fig. P7.122(b) has  $g_m = 10\text{ mA/V}$  and a large  $r_o$ . Find the input resistance and the voltage gain.
- If the output of the source follower in (a) is connected to the input of the common-gate amplifier in (b), use the results of (a) and (b) to obtain the overall voltage gain  $v_o/v_i$ .



(a)



(b)

Figure P7.122

**SIM** = Multisim/PSpice; \* = difficult problem; \*\* = more difficult; \*\*\* = very challenging; D = design problem

**D \*\*7.123** The MOSFET in the amplifier circuit of Fig. P7.123 has  $V_t = 0.6$  V,  $k_n = 5 \text{ mA/V}^2$ , and  $V_A = 60$  V. The signal  $v_{\text{sig}}$  has a zero average.

- It is required to bias the transistor to operate at an overdrive voltage  $V_{ov} = 0.2$  V. What must the dc voltage at the drain be? Calculate the dc drain current  $I_D$  taking into account  $V_A$ . Now, what value must the drain resistance  $R_D$  have?
- Calculate the values of  $g_m$  and  $r_o$  at the bias point established in (a).
- Using the small-signal equivalent circuit of the amplifier, show that the voltage gain is given by

$$\frac{v_o}{v_{\text{sig}}} = - \frac{R_2/R_1}{1 + \frac{1 + R_2/R_1}{g_m(R_D \parallel r_o \parallel R_2)(1 - 1/g_m R_2)}}$$

and find the value of the gain.

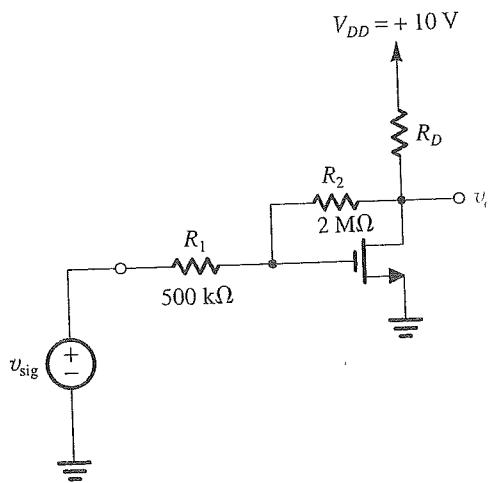


Figure P7.123

P.S. This feedback amplifier and the gain expression should remind you of an op amp utilized in the inverting configuration. We shall study feedback formally in Chapter 11.

**D \*\*7.124** The MOSFET in the amplifier circuit of Fig. P7.124 has  $V_t = 0.6$  V and  $k_n = 5 \text{ mA/V}^2$ . We shall assume that  $V_A$  is sufficiently large so that we can ignore the Early effect. The input signal  $v_{\text{sig}}$  has a zero average.

- It is required to bias the transistor to operate at an overdrive voltage  $V_{ov} = 0.2$  V. What must the dc voltage at the drain be? Calculate the dc drain current  $I_D$ . What value must  $R_D$  have?
- Calculate the value of  $g_m$  at the bias point.
- Use the small-signal equivalent circuit of the amplifier to show that

$$\frac{v_o}{v_{\text{sig}}} = \frac{1 + (R_2/R_1)}{1 + \frac{(1 + R_2/R_1)}{g_m R'_D}}$$

and

$$R_{\text{in}} = \frac{1}{g_m} (1 + g_m R'_D \frac{R_1}{R_1 + R_2})$$

where

$$R'_D = R_D \parallel (R_1 + R_2)$$

- Evaluate  $v_o/v_{\text{sig}}$  and  $R_{\text{in}}$ .

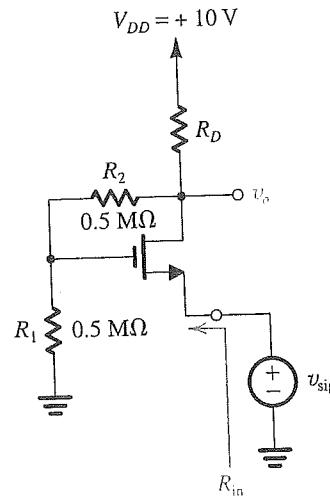


Figure P7.124

P.S. This feedback amplifier circuit and the gain formula should remind you of an op amp connected in the noninverting configuration. We shall study feedback formally in Chapter 11.

**D 7.125** For the common-emitter amplifier shown in Fig. P7.125, let  $V_{CC} = 15$  V,  $R_1 = 27$  k $\Omega$ ,  $R_2 = 15$  k $\Omega$ ,  $R_E = 2.4$  k $\Omega$ , and  $R_L = 2$  k $\Omega$ . The transistor has  $\beta = 100$ . Calculate the dc bias current  $I_C$ . If the amplifier operates between a source for which  $R_{sig} = 2$  k $\Omega$  and a load of 2 k $\Omega$ , replace the transistor with its hybrid- $\pi$  model, and find the values of  $R_{in}$ , and the overall voltage gain  $v_o/v_{sig}$ .

**D 7.126** Using the topology of Fig. P7.125, design an amplifier to operate between a 2-k $\Omega$  source and a 2-k $\Omega$  load with a gain  $v_o/v_{sig}$  of  $-40$  V/V. The power supply available is 15 V. Use an emitter current of approximately 2 mA and a current of about one-tenth of that in the voltage divider that feeds the base, with the dc voltage at the base about one-third of the supply. The transistor available has  $\beta = 100$ . Use standard 5% resistors (see Appendix J).

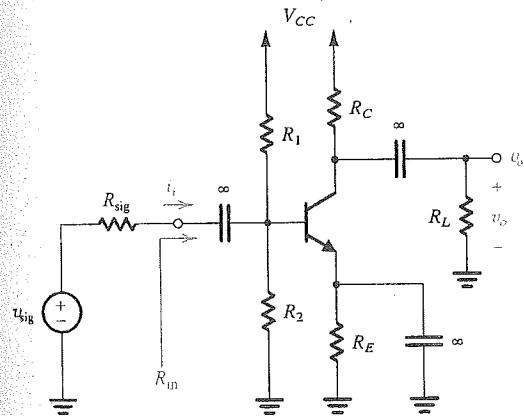


Figure P7.125

**D 7.127** A designer, having examined the situation described in Problem 7.125 and estimating the available gain to be approximately  $-36.3$  V/V, wants to explore the possibility of improvement by reducing the loading

of the source by the amplifier input. As an experiment, the designer varies the resistance levels by a factor of approximately 3:  $R_1$  to 82 k $\Omega$ ,  $R_2$  to 47 k $\Omega$ ,  $R_E$  to 7.2 k $\Omega$ , and  $R_L$  to 12 k $\Omega$  (standard values of 5%-tolerance resistors). With  $V_{CC} = 15$  V,  $R_{sig} = 2$  k $\Omega$ ,  $R_L = 2$  k $\Omega$ , and  $\beta = 100$ , what does the gain become? Comment.

**D 7.128** The CE amplifier circuit of Fig. P7.128 is biased with a constant-current source  $I$ . It is required to design the circuit (i.e., find values for  $I$ ,  $R_B$ , and  $R_C$ ) to meet the following specifications:

- $R_{in} \approx 10$  k $\Omega$ .
- The dc voltage drop across  $R_B$  is approximately 0.2 V.
- The open-circuit voltage gain from base to collector is the maximum possible, consistent with the requirement that the collector voltage never fall by more than approximately 0.4 V below the base voltage with the signal between base and emitter being as high as 5 mV.

Assume that  $v_{sig}$  is a sinusoidal source, the available supply  $V_{CC} = 5$  V, and the transistor has  $\beta = 100$ . Use standard 5% resistance values, and specify the value of  $I$  to one significant digit. What base-to-collector open-circuit voltage gain does your design provide? If  $R_{sig} = R_L = 20$  k $\Omega$ , what is the overall voltage gain?

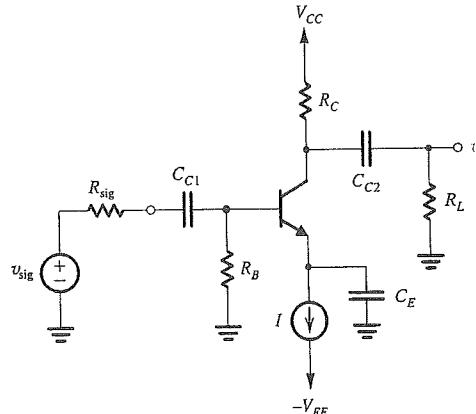


Figure P7.128

## CHAPTER 7 PROBLEMS

**D 7.129** In the circuit of Fig. P7.129,  $v_{sig}$  is a small sine-wave signal with zero average. The transistor  $\beta$  is 100.

- (a) Find the value of  $R_E$  to establish a dc emitter current of about 0.5 mA.

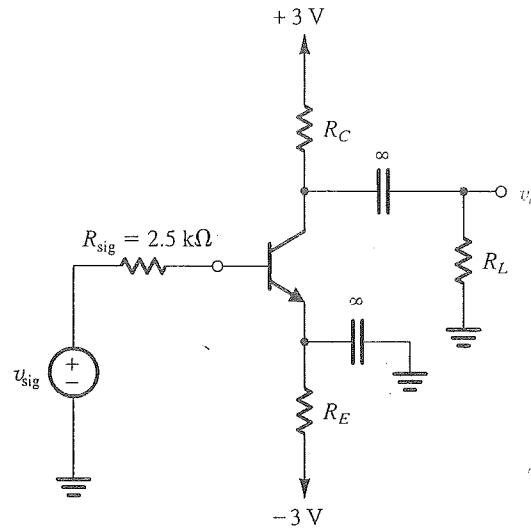


Figure P7.129

- (b) Find  $R_C$  to establish a dc collector voltage of about +0.5 V.

- (c) For  $R_L = 10 \text{ k}\Omega$ , draw the small-signal equivalent circuit of the amplifier and determine its overall voltage gain.

\***7.130** The amplifier of Fig. P7.130 consists of two identical common-emitter amplifiers connected in cascade. Observe that the input resistance of the second stage,  $R_{in2}$ , constitutes the load resistance of the first stage.

- (a) For  $V_{CC} = 15 \text{ V}$ ,  $R_1 = 100 \text{ k}\Omega$ ,  $R_2 = 47 \text{ k}\Omega$ ,  $R_E = 3.9 \text{ k}\Omega$ ,  $R_C = 6.8 \text{ k}\Omega$ , and  $\beta = 100$ , determine the dc collector current and dc collector voltage of each transistor.
- (b) Draw the small-signal equivalent circuit of the entire amplifier and give the values of all its components.
- (c) Find  $R_{in1}$  and  $v_{b1}/v_{sig}$  for  $R_{sig} = 5 \text{ k}\Omega$ .
- (d) Find  $R_{in2}$  and  $v_{b2}/v_{b1}$ .
- (e) For  $R_L = 2 \text{ k}\Omega$ , find  $v_o/v_{b2}$ .
- (f) Find the overall voltage gain  $v_o/v_{sig}$ .

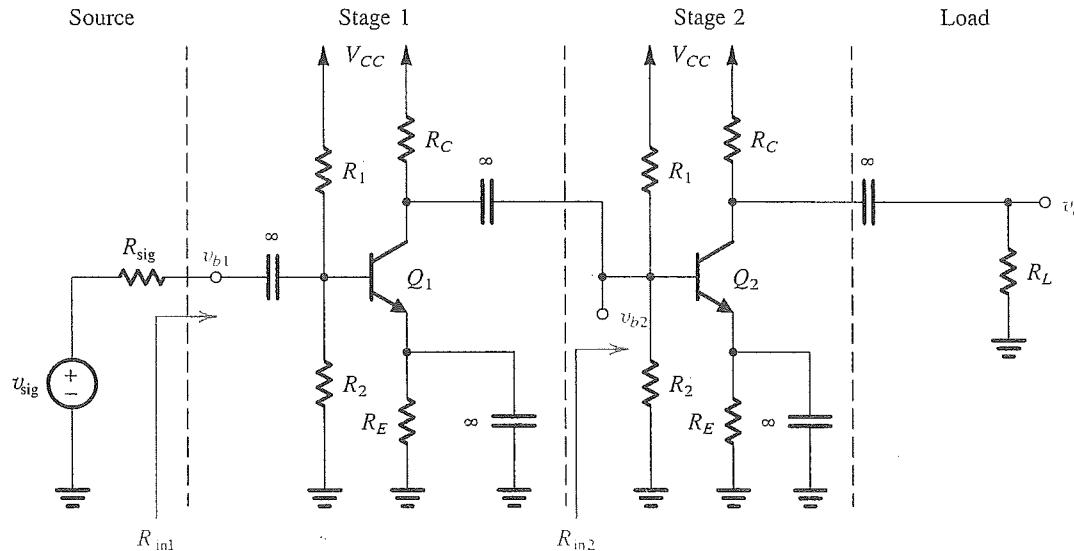


Figure P7.130

7.131 In the circuit of Fig. P7.131, the BJT is biased with a constant-current source, and  $v_{sig}$  is a small sine-wave signal. Find  $R_{in}$  and the gain  $v_o/v_{sig}$ . Assume  $\beta = 100$ . If the amplitude of the signal  $v_{be}$  is to be limited to 5 mV, what is the largest signal at the input? What is the corresponding signal at the output?

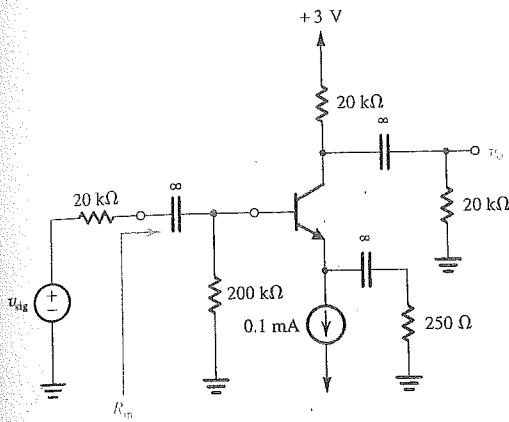


Figure P7.131

\*7.132 The BJT in the circuit of Fig. P7.132 has  $\beta = 100$ .

- Find the dc collector current and the dc voltage at the collector.
- Replacing the transistor by its T model, draw the small-signal equivalent circuit of the amplifier. Analyze the resulting circuit to determine the voltage gain  $v_o/v_i$ .

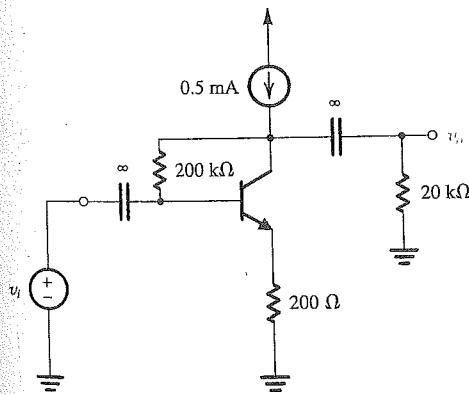


Figure P7.132

7.133 For the circuit in Fig. P7.133, find the input resistance  $R_{in}$  and the voltage gain  $v_o/v_{sig}$ . Assume that the source provides a small signal  $v_{sig}$  and that  $\beta = 100$ .

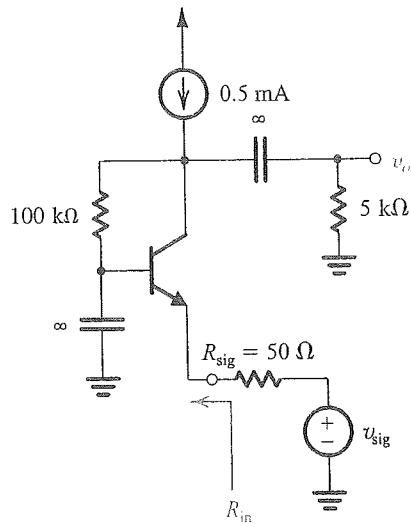


Figure P7.133

7.134 For the emitter-follower circuit shown in Fig. P7.134, the BJT used is specified to have  $\beta$  values in the range of 50 to 200 (a distressing situation for the circuit designer).

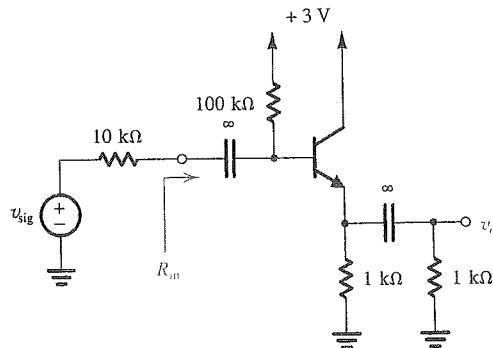


Figure P7.134

**SIM** = Multisim/PSpice; \* = difficult problem; \*\* = more difficult; \*\*\* = very challenging; D = design problem

For the two extreme values of  $\beta$  ( $\beta=50$  and  $\beta=200$ ), find:

- $I_E$ ,  $V_E$ , and  $V_B$
- the input resistance  $R_{in}$
- the voltage gain  $v_o/v_{sig}$

7.135 For the emitter follower in Fig. P7.135, the signal source is directly coupled to the transistor base. If the dc component of  $v_{sig}$  is zero, find the dc emitter current. Assume  $\beta=100$ . Neglecting  $r_o$ , find  $R_{in}$ , the voltage gain  $v_o/v_{sig}$ , the current gain  $i_o/i_i$ , and the output resistance  $R_{out}$ .

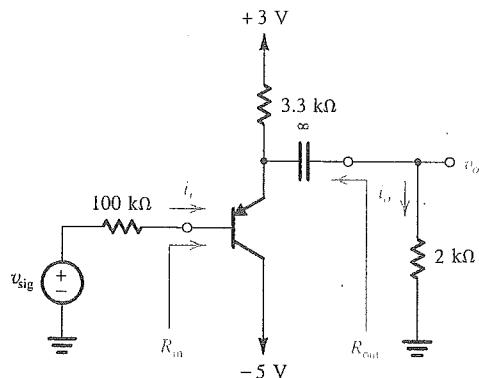


Figure P7.135

\*\*7.136 For the circuit in Fig. P7.136, called a **bootstrapped follower**:

- Find the dc emitter current and  $g_m$ ,  $r_e$ , and  $r_\pi$ . Use  $\beta=100$ .
- Replace the BJT with its T model (neglecting  $r_o$ ), and analyze the circuit to determine the input resistance  $R_{in}$  and the voltage gain  $v_o/v_{sig}$ .
- Repeat (b) for the case when capacitor  $C_B$  is open-circuited. Compare the results with those obtained in (b) to find the advantages of bootstrapping.

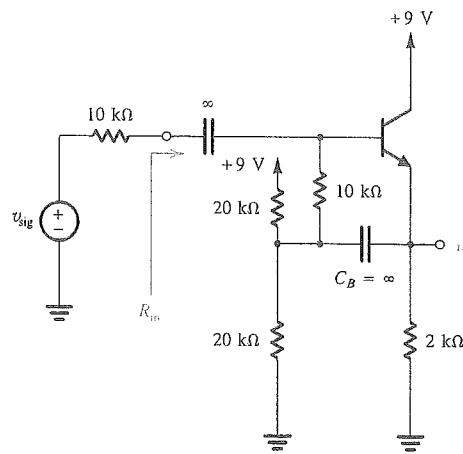


Figure P7.136

\*\*7.137 For the follower circuit in Fig. P7.137, let transistor  $Q_1$  have  $\beta=50$  and transistor  $Q_2$  have  $\beta=100$ , and neglect the effect of  $r_o$ . Use  $V_{BE}=0.7$  V.

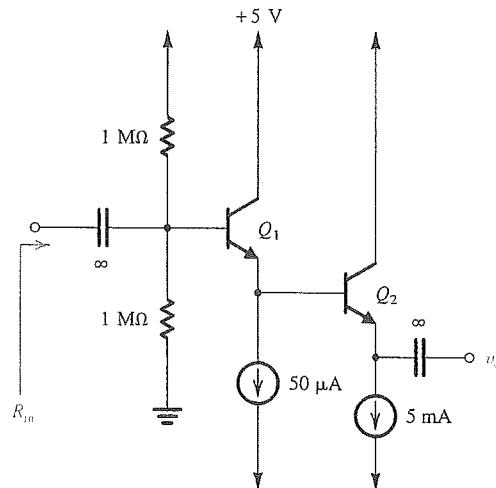


Figure P7.137

- (a) Find the dc emitter currents of  $Q_1$  and  $Q_2$ . Also, find the dc voltages  $V_{B1}$  and  $V_{B2}$ .
- (b) If a load resistance  $R_L = 1 \text{ k}\Omega$  is connected to the output terminal, find the voltage gain from the base to the emitter of  $Q_2$ ,  $v_o/v_{b2}$ , and find the input resistance  $R_{ib2}$  looking into the base of  $Q_2$ . (Hint: Consider  $Q_2$  as an emitter follower fed by a voltage  $v_{b2}$  at its base.)
- (c) Replacing  $Q_2$  with its input resistance  $R_{ib2}$  found in (b), analyze the circuit of emitter follower  $Q_1$  to determine its input resistance  $R_{in}$ , and the gain from its base to its emitter,  $v_{e1}/v_{b1}$ .
- (d) If the circuit is fed with a source having a  $100\text{-k}\Omega$  resistance, find the transmission to the base of  $Q_1$ ,  $v_{b1}/v_{sig}$ .
- (e) Find the overall voltage gain  $v_o/v_{sig}$ .

D 7.138 A CE amplifier has a midband voltage gain of  $|A_M| = 100 \text{ V/V}$ , a lower 3-dB frequency of  $f_L = 100 \text{ Hz}$ , and a higher 3-dB frequency  $f_H = 500 \text{ kHz}$ . In Chapter 10 we will learn that connecting a resistance  $R_e$  in the emitter of the BJT results in lowering  $f_L$  and raising  $f_H$  by the factor  $(1 + g_m R_e)$ . If the BJT is biased at  $I_C = 1 \text{ mA}$ , find  $R_e$  that will result in  $f_H$  at least equal to  $2 \text{ MHz}$ . What will the new values of  $f_L$  and  $A_M$  be?