Computer Simulation Problems

SIM Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

Section 9.1: The MOS Differential Pair

9.1 For an NMOS differential pair with a common-mode voltage V_{CM} applied, as shown in Fig. 9.2, let $V_{DD} = V_{SS} = 1.0$ V, $k_n' = 0.4$ mA/V^2, $(W/L)_{1,2} = 10$, $V_{tn} = 0.4$ V, $I = 0.16$ mA, $R_D = 5$ kΩ, and neglect channel-length modulation.

(a) Find V_{OV} and V_{GS} for each transistor.
(b) For $V_{CM} = 0$, find V_S, I_{D1}, I_{D2}, V_{D1}, and V_{D2}.
(c) Repeat (b) for $V_{CM} = +0.4$ V.
(d) Repeat (b) for $V_{CM} = -0.1$ V.
(e) What is the highest value of V_{CM} for which Q_1 and Q_2 remain in saturation?
(f) If current source I requires a minimum voltage of 0.2 V to operate properly, what is the lowest value allowed for V_S and hence for V_{CM}?

9.2 For the PMOS differential amplifier shown in Fig. P9.2 let $V_{tp} = -0.8$ V and $k_p'W/L = 4$ mA/V^2. Neglect channel-length modulation.

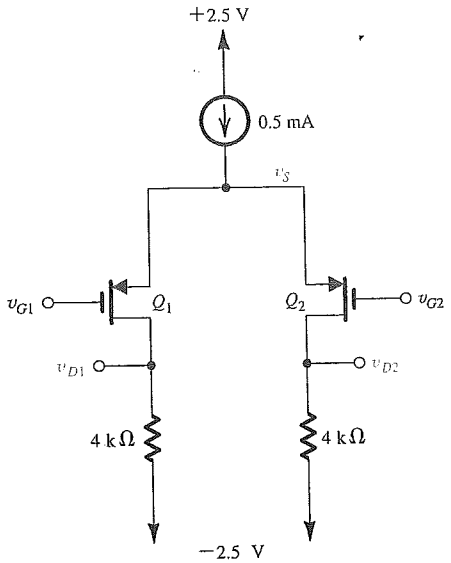

Figure P9.2

(a) For $v_{G1} = v_{G2} = 0$ V, find $|V_{OV}|$ and V_{SG} for each of Q_1 and Q_2. Also find V_S, V_{D1}, and V_{D2}.
(b) If the current source requires a minimum voltage of 0.4 V, find the input common-mode range.

9.3 For the differential amplifier specified in Problem 9.1 let $v_{G2} = 0$ and $v_{G1} = v_{id}$. Find the value of v_{id} that corresponds to each of the following situations:
(a) $i_{D1} = i_{D2} = 0.08$ mA; (b) $i_{D1} = 0.12$ mA and $i_{D2} = 0.04$ mA; (c) $i_{D1} = 0.16$ mA and $i_{D2} = 0$ (Q_2 just cuts off); (d) $i_{D1} = 0.04$ mA and $i_{D2} = 0.12$ mA; (e) $i_{D1} = 0$ mA (Q_1 just cuts off) and $i_{D2} = 0.16$ mA. For each case, find v_S, v_{D1}, v_{D2}, and $(v_{D2} - v_{D1})$.

SIM 9.4 For the differential amplifier specified in Problem 9.2, let $v_{G2} = 0$ and $v_{G1} = v_{id}$. Find the range of v_{id} needed to steer the bias current from one side of the pair to the other. At each end of this range, give the value of the voltage at the common-source terminal and the drain voltages.

9.5 Consider the differential amplifier specified in Problem 9.1 with G_2 grounded and $v_{G1} = v_{id}$. Let v_{id} be adjusted to the value that causes $i_{D1} = 0.09$ mA and $i_{D2} = 0.07$ mA. Find the corresponding values of v_{GS2}, v_S, v_{GS1}, and hence v_{id}. What is the difference output voltage $v_{D2} - v_{D1}$? What is the voltage gain $(v_{D2} - v_{D1})/v_{id}$? What value of v_{id} results in $i_{D1} = 0.07$ mA and $i_{D2} = 0.09$ mA?

D 9.6 Design the circuit in Fig. P9.6 to obtain a dc voltage of +0.1 V at each of the drains of Q_1 and Q_2 when $v_{G1} = v_{G2} = 0$ V. Operate all transistors at $V_{OV} = 0.15$ V.

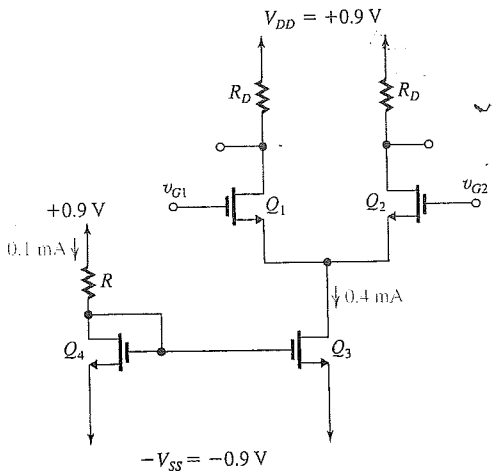

Figure P9.6

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

and assume that for the process technology in which the circuit is fabricated, $V_{tn} = 0.4$ V and $\mu_n C_{ox} = 400\ \mu A/V^2$. Neglect channel-length modulation. Determine the values of R, R_D, and the W/L ratios of Q_1, Q_2, Q_3, and Q_4. What is the input common-mode voltage range for your design?

9.7 The table providing the answers to Exercise 9.3 shows that as the maximum input signal to be applied to the differential pair is increased, linearity is maintained at the same level by operating at a higher V_{OV}. If $|v_{id}|_{max}$ is to be 220 mV, use the data in the table to determine the required V_{OV} and the corresponding values of W/L and g_m.

9.8 Use Eq. (9.23) to show that if the term involving v_{id}^2 is to be kept to a maximum value of k then the maximum possible fractional change in the transistor current is given by

$$\frac{\Delta I_{max}}{I/2} = 2\sqrt{k(1-k)}$$

and the corresponding maximum value of v_{id} is given by

$$v_{idmax} = 2\sqrt{k}V_{OV}$$

Evaluate both expressions for $k = 0.01$, 0.1, and 0.2.

9.9 A MOS differential amplifier biased with a current source $I = 200\ \mu A$ is found to switch currents completely to one side of the pair when a difference signal $v_{id} = 0.3$ V is applied. At what overdrive voltage will each of Q_1 and Q_2 be operating when $v_{id} = 0$? If v_{id} for full current switching is to be 0.5 V, what must the bias current I be changed to?

D 9.10 Design the MOS differential amplifier of Fig. 9.5 to operate at $V_{OV} = 0.25$ V and to provide a transconductance g_m of 1 mA/V. Specify the W/L ratios and the bias current. The technology available provides $V_t = 0.5$ V and $\mu_n C_{ox} = 400\ \mu A/V^2$.

9.11 For the MOS differential pair in Fig. 9.5, specify the value of $v_{id} \equiv v_{G1} - v_{G2}$, in terms of V_{OV}, that

(a) causes i_{D1} to increase by 10% above its equilibrium value of $I/2$.
(b) makes $i_{D1}/i_{D2} = 1.0$; 2.0; 1.1; 1.01; 20.

9.12 An NMOS differential amplifier is operated at a bias current I of 0.2 mA and has a W/L ratio of 32, $\mu_n C_{ox} = 200\ \mu A/V^2$, $V_A = 10$ V, and $R_D = 10\ k\Omega$. Find V_{OV}, g_m, r_o, and A_d.

D 9.13 It is required to design an NMOS differential amplifier to operate with a differential input voltage that can be as high as 0.1 V while keeping the nonlinear term under the square root in Eq. (9.23) to a maximum of 0.04. A transconductance g_m of 2 mA/V is needed and the amplifier is required to provide a differential output signal of 1 V when the input is at its maximum value. Find the required values of V_{OV}, I, R_D, and W/L. Assume that the technology available has $\mu_n C_{ox} = 200\ \mu A/V^2$ and $\lambda = 0$.

D 9.14 Design a MOS differential amplifier to operate from ±1-V power supplies and dissipate no more than 1 mW in the equilibrium state. The differential voltage gain A_d is to be 10 V/V and the output common-mode dc voltage is to be 0.2 V. (*Note*: This is the dc voltage at the drains.) Assume $\mu_n C_{ox} = 400\ \mu A/V^2$ and neglect the Early effect. Specify I, R_D, and W/L.

D 9.15 Design a MOS differential amplifier to operate from ±1-V supplies and dissipate no more than 1 mW in its equilibrium state. Select the value of V_{OV} so that the value of v_{id} that steers the current from one side of the pair to the other is 0.25 V. The differential voltage gain A_d is to be 10 V/V. Assume $k_n' = 400\ \mu A/V^2$ and neglect the Early effect. Specify the required values of I, R_D, and W/L.

9.16 An NMOS differential amplifier employing equal drain resistors, $R_D = 47\ k\Omega$, has a differential gain A_d of 20 V/V.

(a) What is the value of g_m for each of the two transistors?
(b) If each of the two transistors is operating at an overdrive voltage $V_{OV} = 0.2$ V, what must the value of I be?
(c) For $v_{id} = 0$, what is the dc voltage across each R_D?
(d) If v_{id} is 20-mV peak-to-peak sine wave applied in a balanced manner but superimposed on $V_{CM} = 0.5$ V, what is the peak of the sine-wave signal at each drain?
(e) What is the lowest value that V_{DD} must have to ensure saturation-mode operation for Q_1 and Q_2 at all times? Assume $V_t = 0.5$ V.

9.17 A MOS differential amplifier is designed to have a differential gain A_d equal to the voltage gain obtained from a common-source amplifier. Both amplifiers utilize the same values of R_D and supply voltages, and all the transistors have the same W/L ratios. What must the bias current I of the differential pair be relative to the bias current I_D of the CS amplifier? What is the ratio of the power dissipation of the two circuits?

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

Solution

Since the circuit is symmetrical and is fed with v_{id} in a balanced manner, the differential half-circuit will be as shown in Fig. 9.11(b). Observe that because the line of symmetry passes through the middle of R_L, the half-circuit has a resistance $R_L/2$ connected between drain and ground. Also note that the virtual ground appears on the node between the two resistances R_s. As a result, the half-circuit has a source-degeneration resistance R_s.

Now, neglecting r_o of the half-circuit transistor Q_1, we can obtain the gain as the ratio of the total resistance in the drain to the total resistance in the source as

$$\frac{-v_{od}/2}{v_{id}/2} = -\frac{R_D \| (R_L/2)}{1/g_m + R_s}$$

with the result that

$$A_d \equiv \frac{v_{od}}{v_{id}} = \frac{R_D \| (R_L/2)}{1/g_m + R_s} \tag{9.37}$$

EXERCISE

9.4 A MOS differential amplifier is operated at a total current of 0.8 mA, using transistors with a W/L ratio of 100, $\mu_n C_{ox} = 0.2$ mA/V^2, $V_A = 20$ V, and $R_D = 5$ kΩ. Find V_{OV}, g_m, r_o, and A_d.
Ans. 0.2 V; 4 mA/V; 50 kΩ; 18.2 V/V

9.1.5 The Differential Amplifier with Current-Source Loads

To obtain higher gain, the passive resistances R_D can be replaced with current sources, as shown in Fig. 9.12(a). Here the current sources are realized with PMOS transistors Q_3 and Q_4, and V_G is a dc bias voltage that ensures that Q_3 and Q_4 each conducts a current equal to $I/2$. The differential voltage gain A_d can be found from the differential half-circuit shown in Fig. 9.12(b) as

$$A_d \equiv \frac{v_{od}}{v_{id}} = g_{m1}(r_{o1} \| r_{o3})$$

EXERCISE

9.5 The differential amplifier of Fig. 9.12(a) is fabricated in a 0.18-μm CMOS technology for which $\mu_n C_{ox} = 4\mu_p C_{ox} = 400$ μA/V^2, $|V_t| = 0.5$ V, and $|V_A'| = 10$ V/μm. If the bias current $I = 200$ μA and all transistors have a channel length twice the minimum and are operating at $|V_{OV}| = 0.2$ V, find W/L for each of Q_1, Q_2, Q_3, and Q_4, and determine the differential voltage gain A_d.
Ans. $(W/L)_{1,2} = 12.5$; $(W/L)_{3,4} = 50$; $A_d = 18$ V/V

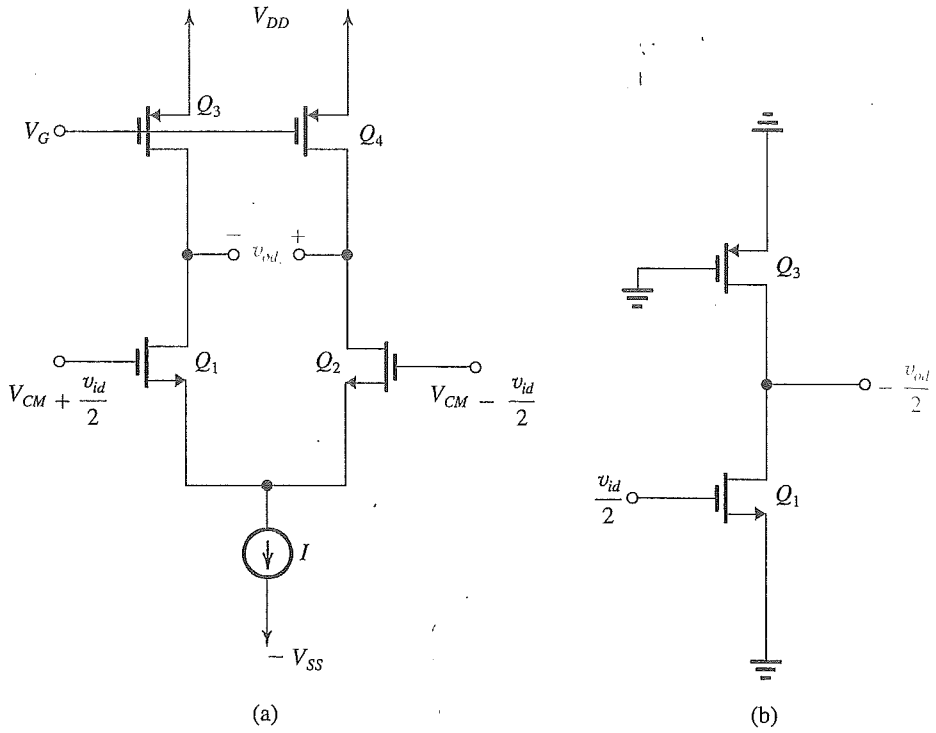

Figure 9.12 (a) Differential amplifier with current-source loads formed by Q_3 and Q_4. (b) Differential half-circuit of the amplifier in (a).

THE LONG-TAILED PAIR:

This idea using vacuum tubes was first documented by B. C. P. Matthews in 1934 in the *Proceedings of the Physical Society*, and was further developed by others in the late 1930s. The topology is simply that of a differential pair, where the term "long-tailed" refers to the biasing current source, which originally used a large-valued (hence long) resistor. Interestingly enough, the first application in measuring biological potentials in an electrically noisy environment continues to be an important one in modern medical instruments that utilize MOS devices.

9.1.6 Cascode Differential Amplifier

The gain of the differential amplifier can be increased by utilizing the cascode configuration studied in Section 8.5. Figure 9.13(a) shows a CMOS differential amplifier with cascoding applied to the amplifying transistors Q_1 and Q_2 via transistors Q_3 and Q_4, and to the current-source transistors Q_7 and Q_8 via transistors Q_5 and Q_6. The differential voltage gain can be found from the differential half-circuit shown in Fig. 9.13(b) as

$$A_d \equiv \frac{v_{od}}{v_{id}} = g_{m1}\left(R_{on} \| R_{op}\right) \tag{9.38}$$

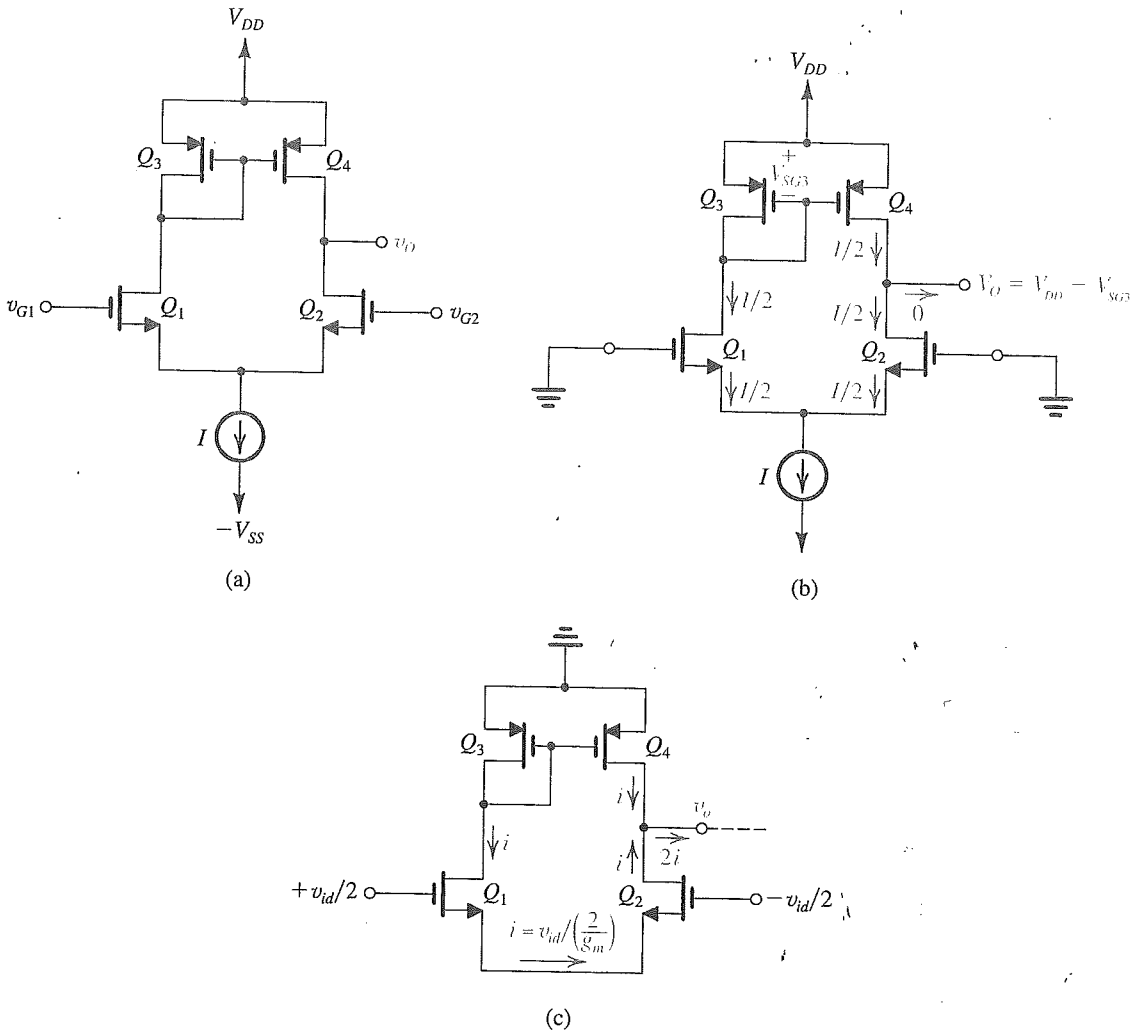

Figure 9.32 **(a)** The current-mirror-loaded MOS differential pair. **(b)** The circuit at equilibrium assuming perfect matching. **(c)** The circuit with a differential input signal applied and neglecting the r_o of all transistors.

fed to the input of the Q_3–Q_4 mirror, which responds by providing a replica in the drain of Q_4. Now, at the output node we have two currents, each equal to i, which sum together to provide an output current $2i$. It is this factor of 2, which is a result of the current-mirror action, that makes it possible to convert the signal to single-ended form (i.e., between the output node and ground) with no loss of gain! If a load resistance is connected to the output node, the current $2i$ flows through it and thus determines the output voltage v_o. In the absence of a load resistance, the output voltage is determined by the output current $2i$ and the output resistance of the circuit, as we shall shortly see.

Before immersing ourselves in detailed analysis of the circuit, it is important to understand the essence of its operation: For dc quantities and common-mode inputs, the current-mirror load produces an output current in the drain of Q_4 that *cancels* the current of Q_2. On the other hand, for differential input signals, the output current of the mirror *adds* to the current of Q_2.

9.5.3 Differential Gain of the Current-Mirror-Loaded MOS Pair

As we learned in Chapter 8, the output resistance r_o of the transistor plays a significant role in the operation of active-loaded amplifiers. Therefore, we shall now take r_o into account and derive an expression for the differential gain v_o/v_{id} of the current-mirror-loaded MOS differential pair. Toward that end, we first observe that the circuit is *not* symmetrical: While the drain of Q_1 sees the small resistance of the diode-connected transistor Q_3 (approximately equal to $1/g_{m3}$), the drain of Q_2 sees the much larger output resistance of Q_4 (r_{o4}). Thus, a virtual ground will *not* develop at the common sources[3] and we cannot use the differential half-circuit technique.

Our approach will be to represent the output of the circuit in Fig. 9.32(c) by the general equivalent circuit shown in Fig. 9.33. Here G_m is the short-circuit transconductance and R_o is the output resistance. In the following, we will show that

$$G_m = g_{m1,2} \tag{9.128}$$

where $g_{m1,2}$ is the transconductance of each of Q_1 and Q_2. We will also show that

$$R_o = r_{o2} \| r_{o4} \tag{9.129}$$

In other words, we shall have two intuitively appealing results: The short-circuit transconductance of the circuit is equal to g_m of each of the two transistors of the differential pair, and the output resistance is the parallel equivalent of the output resistances of Q_2 and Q_4. Thus, the open-circuit differential voltage gain can be found as

$$A_d \equiv \frac{v_o}{v_{id}} = G_m R_o = g_{m1,2}(r_{o2} \| r_{o4}) \tag{9.130}$$

Writing $g_{m1,2}$ simply as g_m, and for the case $r_{o2} = r_{o4} = r_o$,

$$A_d = \frac{1}{2} g_m r_o = \frac{1}{2} A_0 \tag{9.131}$$

where A_0 is the intrinsic gain of the MOS transistor.

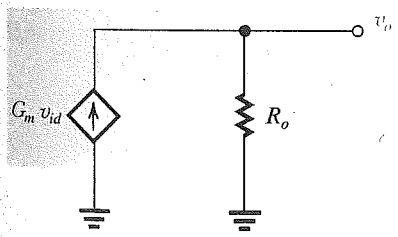

Figure 9.33 Output equivalent circuit of the amplifier in Fig. 9.32(a) for differential input signals.

[3]The qualitative description of circuit operation above implied that a virtual ground develops at the MOSFET sources. That was the case because we were neglecting r_o of all transistors.

EXERCISE

9.17 A current-mirror-loaded MOS differential amplifier of the type shown in Fig. 9.32(a) is specified as follows: $(W/L)_n = 100$, $(W/L)_p = 200$, $\mu_n C_{ox} = 2\mu_p C_{ox} = 0.2$ mA/V^2, $V_{An} = |V_{Ap}| = 20$ V, and $I = 0.8$ mA. Calculate G_m, R_o, and A_d.
Ans. 4 mA/V; 25 kΩ; 100 V/V

Derivation of the Short-Circuit Transconductance, G_m Figure 9.34(a) shows the current-mirror-loaded MOS amplifier with the output terminal short-circuited to ground. Our purpose is to determine the short-circuit transconductance

$$G_m \equiv \frac{i_o}{v_{id}}$$

We note that short-circuiting the output terminal makes the circuit nearly balanced. This is because the drain of Q_1 sees the small resistance of the diode-connected transistor Q_3, and now the drain of Q_2 sees a short circuit. It follows that the voltage at the MOSFET sources will be approximately zero. Now, replacing each of the four transistors with its hybrid-π model and noting that for the diode-connected transistor Q_3, the model reduces to a resistance $(1/g_{m3} \| r_{o3})$, we obtain the equivalent circuit shown in Fig. 9.34(b). The short-circuit output current i_o can be found by writing a node equation at the output and noting that the currents in r_{o2} and r_{o4} are zero; thus

$$i_o = g_{m2}\left(\frac{v_{id}}{2}\right) - g_{m4}\, v_{gs4} \tag{9.132}$$

Next, we note that

$$v_{gs4} = v_{gs3} \tag{9.133}$$

and v_{gs3} can be obtained from a node equation at d_1 as

$$v_{gs3} = -g_{m1}\left(\frac{v_{id}}{2}\right)\left(\frac{1}{g_{m3}} \| r_{o3} \| r_{o1}\right)$$

which for the usual case of $\frac{1}{g_{m3}} \ll r_{o3}, r_{o1}$, reduces to

$$v_{gs3} \simeq -\frac{g_{m1}}{g_{m3}}\left(\frac{v_{id}}{2}\right) \tag{9.134}$$

Combining Eqs. (9.132) to (9.134) and substituting $g_{m3} = g_{m4}$ and $g_{m1} = g_{m2} = g_m$ gives

$$i_o = g_m v_{id}$$

from which G_m is found to be

$$G_m = g_m$$

as expected.

Derivation of the Output Resistance R_o Figure 9.35 shows the circuit[4] for determining the output resistance R_o. Observe that we have set v_{id} to zero, resulting in the ground

[4]Note that rather than replacing each transistor with its small-signal model, we are, for simplicity, using the models implicitly. Thus we have "pulled r_o out" of each transistor and shown it separately so that the drain current becomes $g_m v_{gs}$.

For the simple current mirror utilized in the circuit of Fig. 9.39(a),

$$R_{im} = \frac{1}{g_{m3}} \| r_{o3} \tag{9.154}$$

and

$$R_{om} = r_{o4} \tag{9.155}$$

The current gain A_m can be found as follows

$$A_m i_i = -g_{m4} v_{gs4} = -g_{m4} v_{gs3}$$

but

$$v_{gs3} = -i_i R_{im}$$

Thus

$$A_m = g_{m4} R_{im}$$

Substituting for R_{im} from (9.154) together with using $g_{m4} = g_{m3}$ results in

$$A_m = 1 \Big/ \left(1 + \frac{1}{g_{m3} r_{o3}}\right) \tag{9.156}$$

Finally, substituting in Eq. (9.153) for A_m from (9.156), for G_{mcm} from (9.148), and for R_{om} from (9.155), and noting that $r_{o4} \ll R_{o2}$, $r_{o4} = r_{o3}$, and $g_m r_{o3} \ll 1$, gives for A_{cm} the expression,

$$A_{cm} \simeq -\frac{1}{2 g_{m3} R_{SS}} \tag{9.157}$$

Since R_{SS} is usually large, at least equal to r_o, A_{cm} will be small. The common-mode rejection ratio (CMRR) can now be obtained by utilizing Eqs. (9.130) and (9.157),

$$\text{CMRR} \equiv \frac{|A_d|}{|A_{cm}|} = [g_m (r_{o2} \| r_{o4})][2 g_{m3} R_{SS}] \tag{9.158}$$

which for $r_{o2} = r_{o4} = r_o$ and $g_{m3} = g_m$ simplifies to

$$\text{CMRR} = (g_m r_o)(g_m R_{SS}) \tag{9.159}$$

We observe that to obtain a large CMRR, we select an implementation of the biasing current source I that features a high output resistance. Such circuits include the cascode current source and the Wilson current source studied in Section 8.6.

EXERCISE

9.20 For the current-mirror-loaded MOS differential amplifier specified in Exercise 9.17, let $R_{SS} = 25\ \text{k}\Omega$. Calculate $|A_{cm}|$ and CMRR. Use the results of Exercise 9.17.
Ans. 0.005 V/V; 20,000 or 86 dB