9.111 For the current-mirror-loaded differential pair in Fig. P9.111, find:

(a) differential input resistance, R_{id}
(b) A_d
(c) CMRR

Assume $\beta = 100, |V_{BE}| = 0.7$ V, and $|V_A| = 60$ V.

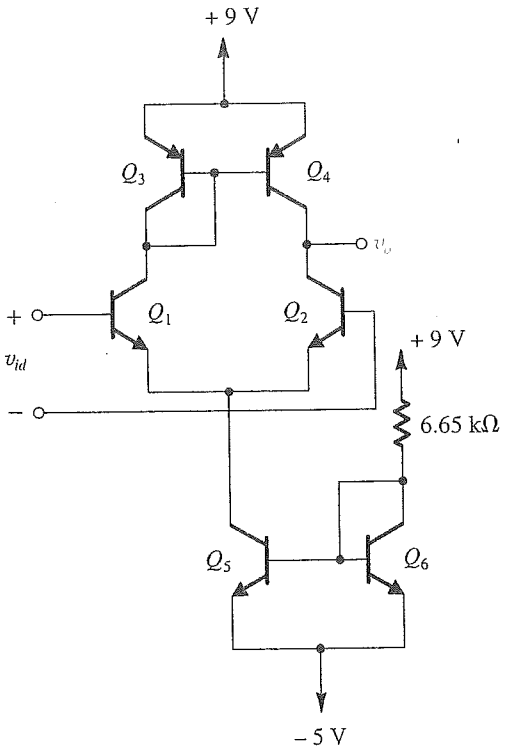

Figure P9.111

9.112 For the current-mirror-loaded differential amplifier in Fig. P9.112, find:

(a) differential input resistance, R_{id}
(b) A_d
(c) CMRR

Assume $\beta = 100, |V_{BE}| = 0.7$ V, $|V_A| = 60$ V, $V_t = 0.7$ V, and $k'(W/L) = 2$ mA/V^2.

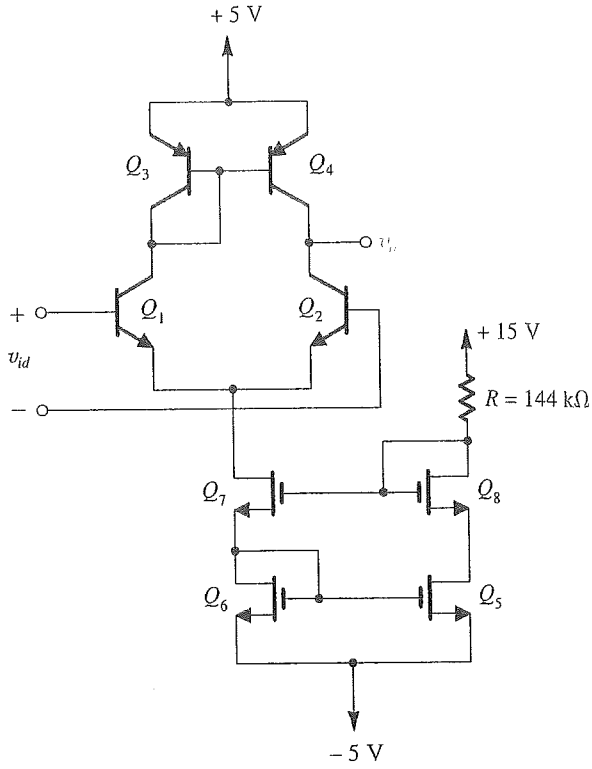

Figure P9.112

Section 9.6: Multistage Amplifiers

9.113 Consider the circuit in Fig. 9.40 with the device geometries (in μm) shown in Table P9.113. Let $I_{REF} = 225$ μA, $|V_t| = 0.75$ V for all devices, $\mu_n C_{ox} = 180$ μA/V^2, $\mu_p C_{ox} = 60$ μA/V^2, $|V_A| = 9$ V for all devices, $V_{DD} = V_{SS} = 1.5$ V. Determine the width of Q_6, W, that will ensure that the op amp will not have a systematic offset voltage. Then, for all devices evaluate I_D, $|V_{OV}|$, $|V_{GS}|$, g_m, and r_o. Provide your results in a table similar to Table 9.1. Also find A_1, A_2, the open-loop voltage gain, the input

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

Table P9.113

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L	30/0.5	30/0.5	10/0.5	10/0.5	60/0.5	W/0.5	60/0.5	60/0.5

common-mode range, and the output voltage range. Neglect the effect of V_A on the bias currents.

D 9.114 The two-stage CMOS op amp in Fig. P9.114 is fabricated in a 0.18-μm technology having $k_n' = 4k_p' = 400\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0.4$ V.

(a) With A and B grounded, perform a dc design that will result in each of Q_1, Q_2, Q_3, and Q_4 conducting a drain current of 100 μA and each of Q_6 and Q_7 a current of 200 μA. Design so that all transistors operate at 0.2-V overdrive voltages. Specify the W/L ratio required for each MOSFET. Present your results in tabular form. What is the dc voltage at the output (ideally)?
(b) Find the input common-mode range.
(c) Find the allowable range of the output voltage.
(d) With $v_A = v_{id}/2$ and $v_B = -v_{id}/2$, find the voltage gain v_o/v_{id}. Assume an Early voltage of 6 V.

D *9.115 In a particular design of the CMOS op amp of Fig. 9.40 the designer wishes to investigate the effects of increasing the W/L ratio of both Q_1 and Q_2 by a factor of 4. Assuming that all other parameters are kept unchanged, refer to Example 9.6 to help you answer the following questions:

(a) Find the resulting change in $|V_{OV}|$ and in g_m of Q_1 and Q_2.
(b) What change results in the voltage gain of the input stage? In the overall voltage gain?
(c) What is the effect on the input offset voltages? (You might wish to refer to Section 9.4).

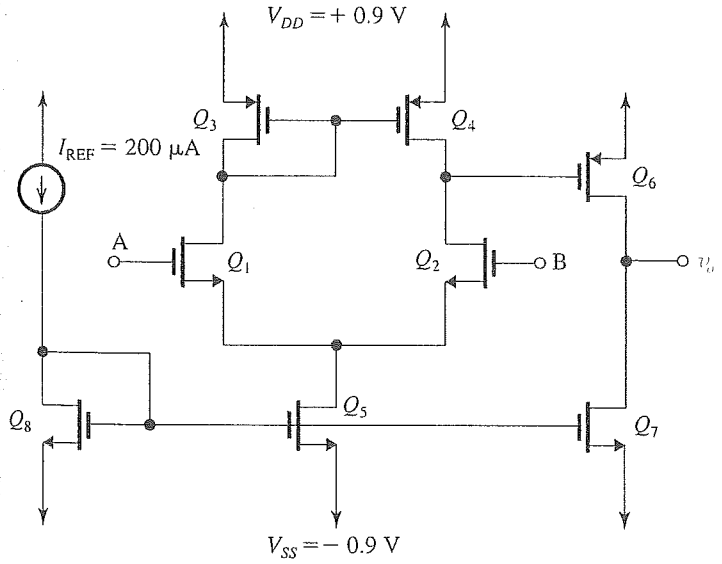

Figure P9.114

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem