Computer Simulations Problems

SIM Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSPice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

Section 5.1: Device Structure and Physical Operation

5.1 MOS technology is used to fabricate a capacitor, utilizing the gate metallization and the substrate as the capacitor electrodes. Find the area required per 1-pF capacitance for oxide thickness ranging from 2 nm to 10 nm. For a square plate capacitor of 10 pF, what dimensions are needed?

5.2 Calculate the total charge stored in the channel of an NMOS transistor having $C_{ox} = 9$ fF/μm^2, $L = 0.36\,\mu$m, and $W = 3.6\,\mu$m, and operated at $V_{OV} = 0.2$ V and $V_{DS} = 0$ V.

5.3 Use dimensional analysis to show that the units of the process transconductance parameter k_n' are A/V^2. What are the dimensions of the MOSFET transconductance parameter k_n?

5.4 An NMOS transistor that is operated with a small v_{DS} is found to exhibit a resistance r_{DS}. By what factor will r_{DS} change in each of the following situations?

(a) V_{OV} is doubled.
(b) The device is replaced with another fabricated in the same technology but with double the width.
(c) The device is replaced with another fabricated in the same technology but with both the width and length doubled.
(d) The device is replaced with another fabricated in a more advanced technology for which the oxide thickness is halved and similarly for W and L (assume μ_n remains unchanged).

D 5.5 An NMOS transistor fabricated in a technology for which $k_n' = 400\,\mu$A/V^2 and $V_t = 0.5$ V is required to operate with a small v_{DS} as a variable resistor ranging in value from 250 Ω to 1 kΩ. Specify the range required for the control voltage V_{GS} and the required transistor width W. It is required to use the smallest possible device, as limited by the minimum channel length of this technology ($L_{min} = 0.18\,\mu$m) and the maximum allowed voltage of 1.8 V.

5.6 Sketch a set of i_D–v_{DS} characteristic curves for an NMOS transistor operating with a small v_{DS} (in the manner shown in Fig. 5.4). Let the MOSFET have $k_n = 5$ mA/V^2 and $V_{tn} = 0.5$ V. Sketch and clearly label the graphs for $V_{GS} = 0.5$, 1.0, 1.5, 2.0, and 2.5 V. Let V_{DS} be in the range 0 to 50 mV. Give the value of r_{DS} obtained for each of the five values of V_{GS}. Although only a sketch, your diagram should be drawn to scale as much as possible.

D 5.7 An n-channel MOS device in a technology for which oxide thickness is 4 nm, minimum channel length is 0.18 μm, $k_n' = 400\,\mu$A/V^2, and $V_t = 0.5$ V operates in the triode region, with small v_{DS} and with the gate–source voltage in the range 0 V to +1.8 V. What device width is needed to ensure that the minimum available resistance is 1 kΩ?

5.8 Consider an NMOS transistor operating in the triode region with an overdrive voltage V_{OV}. Find an expression for the incremental resistance

$$r_{ds} \equiv 1 \Big/ \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{v_{DS}=V_{DS}}$$

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Give the values of r_{ds} in terms of k_n and V_{OV} for $V_{DS} = 0$, $0.2V_{OV}$, $0.5V_{OV}$, $0.8V_{OV}$, and V_{OV}.

5.9 An NMOS transistor with $k_n = 4$ mA/V^2 and $V_t = 0.5$ V is operated with $V_{GS} = 1.0$ V. At what value of V_{DS} does the transistor enter the saturation region? What value of I_D is obtained in saturation?

5.10 Consider a CMOS process for which $L_{min} = 0.25$ μm, $t_{ox} = 6$ nm, $\mu_n = 460$ cm^2/V·s, and $V_t = 0.5$ V.

(a) Find C_{ox} and k_n'.
(b) For an NMOS transistor with $W/L = 20$ μm/0.25 μm, calculate the values of V_{OV}, V_{GS}, and V_{DSmin} needed to operate the transistor in the saturation region with a dc current $I_D = 0.5$ mA.
(c) For the device in (b), find the values of V_{OV} and V_{GS} required to cause the device to operate as a 100-Ω resistor for very small v_{DS}.

5.11 A p-channel MOSFET with a threshold voltage $V_{tp} = -0.7$ V has its source connected to ground.

(a) What should the gate voltage be for the device to operate with an overdrive voltage of $|V_{OV}| = 0.4$ V?
(b) With the gate voltage as in (a), what is the highest voltage allowed at the drain while the device operates in the saturation region?
(c) If the drain current obtained in (b) is 0.5 mA, what would the current be for $V_D = -20$ mV and for $V_D = -2$V?

5.12 With the knowledge that $\mu_p = 0.4\mu_n$, what must be the relative width of n-channel and p-channel devices having equal channel lengths if they are to have equal drain currents when operated in the saturation mode with overdrive voltages of the same magnitude?

5.13 An n-channel device has $k_n' = 100$ μA/V^2, $V_t = 0.7$ V, and $W/L = 20$. The device is to operate as a switch for small v_{DS}, utilizing a control voltage v_{GS} in the range 0 V to 5 V. Find the switch closure resistance, r_{DS}, and closure voltage, V_{DS}, obtained when $v_{GS} = 5$ V and $i_D = 1$ mA. If $\mu_p \simeq 0.4\mu_n$, what must W/L be for a p-channel device that provides the same performance as the n-channel device in this application?

5.14 Consider an n-channel MOSFET with $t_{ox} = 6$ nm, $\mu_n = 460$ cm^2/V·s, $V_t = 0.5$ V, and $W/L = 10$. Find the drain current in the following cases:

(a) $v_{GS} = 2.5$ V and $v_{DS} = 1$ V
(b) $v_{GS} = 2$ V and $v_{DS} = 1.5$ V
(c) $v_{GS} = 2.5$ V and $v_{DS} = 0.2$ V
(d) $v_{GS} = v_{DS} = 2.5$ V

*5.15 This problem illustrates the central point in the electronics revolution that has been in effect for the past four decades: By continually reducing the MOSFET size, we are able to pack more devices on an IC chip. Gordon Moore, co-founder of Intel Corporation, predicted this exponential growth of chip-packing density very early in the history of the development of the integrated circuit in the formulation that has become known as **Moore's law**.

The table on the next page shows four technology generations, each characterized by the minimum possible MOSFET channel length (row 1). In going from one generation to another, both L and t_{ox} are scaled by the same factor. The power supply utilized V_{DD} is also scaled by the same factor, to keep the magnitudes of all electrical fields within the device unchanged. Unfortunately, but for good reasons, V_t cannot be scaled similarly.

Complete the table entries, noting that row 5 asks for the transconductance parameter of an NMOS transistor with $W/L = 10$; row 9 asks for the value of I_D obtained with $V_{GS} = V_{DS} = V_{DD}$; row 10 asks for the power $P = V_{DD}I_D$ dissipated in the circuit. An important quantity is the power density, P/A, asked for in row 11. Finally, you are asked to find the number of transistors that can be placed on an IC chip fabricated in each of the technologies in terms of the number obtained with the 0.5-μm technology (n).

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1	L (μm)	0.5	0.25	0.18	0.13
2	t_{ox} (nm)	10			
3	C_{ox} (fF/μm^2)				
4	k_n' (μA/V^2) ($\mu_n = 500$ cm^2/V · s)				
5	k_n (mA/V^2) For $W/L = 10$				
6	Device area, A (μm^2)				
7	V_{DD} (V)	5			
8	V_t (V)	0.7	0.5	0.4	0.4
9	I_D (mA) For $V_{GS} = V_{DS} = V_{DD}$				
10	P (mW)				
11	P/A (mW/μm^2)				
12	Devices per chip	n			

Section 5.2: Current–Voltage Characteristics

In the following problems, when λ is not specified, assume it is zero.

5.16 Show that when channel-length modulation is neglected (i.e., $\lambda = 0$), plotting i_D/k_n versus v_{DS} for various values of v_{OV}, and plotting i_D/k_n versus v_{OV} for $v_{DS} \geq v_{OV}$, results in universal representation of the i_D–v_{DS} and i_D–v_{GS} characteristics of the NMOS transistor. That is, the resulting graphs are both technology and device independent. Furthermore, these graphs apply equally well to the PMOS transistor by a simple relabeling of variables. (How?) What is the slope at $v_{DS} = 0$ of each of the i_D/k_n versus v_{DS} graphs? For the i_D/k_n versus v_{OV} graph, find the slope at a point $v_{OV} = V_{OV}$.

5.17 An NMOS transistor having $V_t = 0.8$ V is operated in the triode region with v_{DS} small. With $V_{GS} = 1.2$ V, it is found to have a resistance r_{DS} of 1 kΩ. What value of V_{GS} is required to obtain $r_{DS} = 200$ Ω? Find the corresponding resistance values obtained with a device having twice the value of W.

5.18 A particular MOSFET for which $V_m = 0.5$ V and $k_n'(W/L) = 1.6$ mA/V^2 is to be operated in the saturation region. If i_D is to be 50 μA, find the required v_{GS} and the minimum required v_{DS}. Repeat for $i_D = 200$ μA.

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5.19 A particular n-channel MOSFET is measured to have a drain current of 0.4 mA at $V_{GS} = V_{DS} = 1$ V and of 0.1 mA at $V_{GS} = V_{DS} = 0.8$ V. What are the values of k_n and V_t for this device?

D 5.20 For a particular IC-fabrication process, the transconductance parameter $k_n' = 400\ \mu A/V^2$, and $V_t = 0.5$ V. In an application in which $v_{GS} = v_{DS} = V_{supply} = 1.8$ V, a drain current of 2 mA is required of a device of minimum length of 0.18 μm. What value of channel width must the design use?

5.21 An NMOS transistor, operating in the linear-resistance region with $v_{DS} = 50$ mV, is found to conduct 25 μA for $v_{GS} = 1$ V and 50 μA for $v_{GS} = 1.5$ V. What is the apparent value of threshold voltage V_t? If $k_n' = 50\ \mu A/V^2$, what is the device W/L ratio? What current would you expect to flow with $v_{GS} = 2$ V and $v_{DS} = 0.1$ V? If the device is operated at $v_{GS} = 2$ V, at what value of v_{DS} will the drain end of the MOSFET channel just reach pinch-off, and what is the corresponding drain current?

5.22 For an NMOS transistor, for which $V_t = 0.4$ V, operating with v_{GS} in the range of 1.0 V to 1.8 V, what is the largest value of v_{DS} for which the channel remains continuous?

5.23 An NMOS transistor, fabricated with $W = 20$ μm and $L = 1$ μm in a technology for which $k_n' = 100\ \mu A/V^2$ and $V_t = 0.8$ V, is to be operated at very low values of v_{DS} as a linear resistor. For v_{GS} varying from 1.0 V to 4.8 V, what range of resistor values can be obtained? What is the available range if

(a) the device width is halved?
(b) the device length is halved?
(c) both the width and length are halved?

5.24 When the drain and gate of a MOSFET are connected together, a two-terminal device known as a "diode-connected transistor" results. Figure P5.24 shows such devices obtained from MOS transistors of both polarities. Show that

(a) the i–v relationship is given by

$$i = \frac{1}{2}k'\frac{W}{L}(v - |V_t|)^2$$

(b) the incremental resistance r for a device biased to operate at $v = |V_t| + V_{OV}$ is given by

$$r \equiv 1\Big/\left[\frac{\partial i}{\partial v}\right] = 1\Big/\left(k'\frac{W}{L}V_{OV}\right)$$

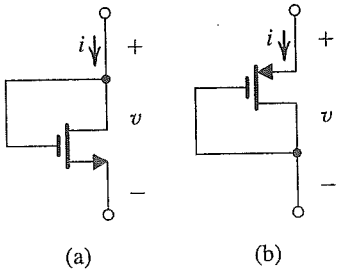

Figure P5.24

5.25 For the circuit in Fig. P5.25, sketch i_D versus v_S for v_S varying from 0 to V_{DD}. Clearly label your sketch.

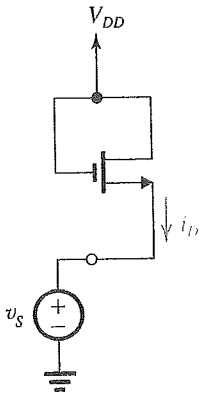

Figure P5.25

5.26 For the circuit in Fig. P5.26, find an expression for v_{DS} in terms of i_D. Sketch and clearly label a graph for v_{DS} versus i_D.

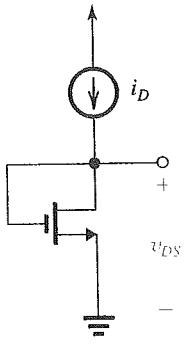

Figure P5.26

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Case	Voltage (V)						Region of operation
	V_S	V_G	V_D	V_{GS}	V_{OV}	V_{DS}	
a	+1.0	+1.0	+2.0				
b	+1.0	+2.5	+2.0				
c	+1.0	+2.5	+1.5				
d	+1.0	+1.5	0				
e	0	+2.5	+1.0				
f	+1.0	+1.0	+1.0				
g	−1.0	0	0				
h	−1.5	0	0				
i	−1.0	0	+1.0				
j	+0.5	+2.0	+0.5				

*5.27 The table above lists 10 different cases labeled (a) to (j) for operating an NMOS transistor with $V_t = 1$ V. In each case the voltages at the source, gate, and drain (relative to the circuit ground) are specified. You are required to complete the table entries. Note that if you encounter a case for which v_{DS} is negative, you should exchange the drain and source before solving the problem. You can do this because the MOSFET is a symmetric device.

5.28 The NMOS transistor in Fig. P5.28 has $V_t = 0.4$ V and $k_n'(W/L) = 1$ mA/V^2. Sketch and clearly label i_D versus v_G with v_G varying in the range 0 to +1.8 V. Give equations for the various portions of the resulting graph.

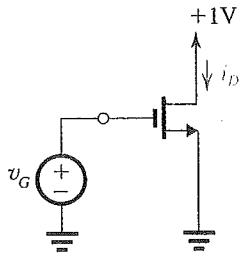

Figure P5.28

5.29 Figure P5.29 shows two NMOS transistors operating in saturation at equal V_{GS} and V_{DS}.

(a) If the two devices are matched except for a maximum possible mismatch in their W/L ratios of 3%, what is the maximum resulting mismatch in the drain currents?

(b) If the two devices are matched except for a maximum possible mismatch in their V_t values of 10 mV, what is the maximum resulting mismatch in the drain currents? Assume that the nominal value of V_t is 0.6 V.

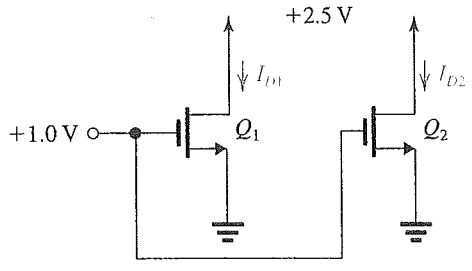

Figure P5.29

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

5.30 For a particular MOSFET operating in the saturation region at a constant v_{GS}, i_D is found to be 0.5 mA for $v_{DS} = 1$ V and 0.52 mA for $v_{DS} = 2$ V. What values of r_o, V_A, and λ correspond?

5.31 A particular MOSFET has $V_A = 20$ V. For operation at 0.1 mA and 1 mA, what are the expected output resistances? In each case, for a change in v_{DS} of 1 V, what percentage change in drain current would you expect?

D 5.32 In a particular IC design in which the standard channel length is 1 μm, an NMOS device with W/L of 10 operating at 200 μA is found to have an output resistance of 100 kΩ, about $\frac{1}{5}$ of that needed. What dimensional change can be made to solve the problem? What is the new device length? The new device width? The new W/L ratio? What is V_A for the standard device in this IC? The new device?

D 5.33 For a particular n-channel MOS technology, in which the minimum channel length is 0.5 μm, the associated value of λ is 0.03 V^{-1}. If a particular device for which L is 1.5 μm operates in saturation at $v_{DS} = 1$ V with a drain current of 100 μA, what does the drain current become if v_{DS} is raised to 5 V? What percentage change does this represent? What can be done to reduce the percentage by a factor of 2?

5.34 An NMOS transistor is fabricated in a 0.5-μm process having $k_n' = 200$ μA/V^2 and $V_A' = 20$ V/μm of channel length. If $L = 1.5$ μm and $W = 15$ μm, find V_A and λ. Find the value of I_D that results when the device is operated with an overdrive voltage of 0.5 V and $V_{DS} = 2$ V. Also, find the value of r_o at this operating point. If V_{DS} is increased by 1 V, what is the corresponding change in I_D?

5.35 If in an NMOS transistor, both W and L are quadrupled and V_{OV} is halved, by what factor does r_o change?

D 5.36 Consider the circuit in Fig. P5.29 with both transistors perfectly matched but with the dc voltage at the drain of Q_1 lowered to +2 V. If the two drain currents are to be matched within 1% (i.e., the maximum difference allowed between the two currents is 1%), what is the minimum required value of V_A? If the technology is specified to have $V_A' = 100$ V/μm, what is the minimum channel length the designer must use?

5.37 Complete the missing entries in the following table, which describes characteristics of suitably biased NMOS transistors:

MOS	1	2	3	4
λ (V^{-1})		0.02		
V_A (V)	20			100
I_D (mA)	0.5		0.1	
r_o (kΩ)		25	100	500

5.38 A PMOS transistor has $k_p'(W/L) = 100$ μA/V^2, $V_t = -1.0$ V, and $\lambda = -0.02$ V^{-1}. The gate is connected to ground and the source to +5 V. Find the drain current for $v_D = +4$ V, +2 V, +1 V, 0 V, and −5 V.

5.39 A p-channel transistor for which $|V_t| = 0.8$ V and $|V_A| = 40$ V operates in saturation with $|v_{GS}| = 3$ V, $|v_{DS}| = 4$ V, and $i_D = 3$ mA. Find corresponding signed values for v_{GS}, v_{SG}, v_{DS}, v_{SD}, V_t, V_A, λ, and $k_p'(W/L)$.

5.40 The table below lists the terminal voltages of a PMOS transistor in six cases, labeled a, b, c, d, e, and f. The transistor has $V_{tp} = -1$ V. Complete the table entries.

	V_S	V_G	V_D	V_{SG}	$\lvert V_{OV}\rvert$	V_{SD}	Region of operation
a	+2	+2	0				
b	+2	+1	0				
c	+2	0	0				
d	+2	0	+1				
e	+2	0	+1.5				
f	+2	0	+2				

= Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

5.41 The PMOS transistor in Fig. P5.41 has $V_{tp} = -0.5$ V. As the gate voltage v_G is varied from +3 V to 0 V, the transistor moves through all of its three possible modes of operation. Specify the values of v_G at which the device changes modes of operation.

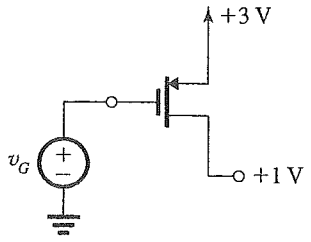

Figure P5.41

*5.42 Various NMOS and PMOS transistors, numbered 1 to 4, are measured in operation, as shown in the table at the bottom of the page. For each transistor, find the values of $\mu C_{ox} W/L$ and V_t that apply and complete the table, with V in volts, I in μA, and $\mu C_{ox} W/L$ in μA/V^2. Assume $\lambda = 0$.

*5.43 All the transistors in the circuits shown in Fig. P5.43 have the same values of $|V_t|$, k', W/L, and λ. Moreover, λ is negligibly small. All operate in saturation at $I_D = I$ and $|V_{GS}| = |V_{DS}| = 1$ V. Find the voltages V_1, V_2, V_3, and V_4. If $|V_t| = 0.5$ V and $I = 0.1$ mA, how large a resistor can be inserted in series with each drain while maintaining saturation? If the current source I requires at least 0.5 V between its terminals to operate properly, what is the largest resistor that can be placed in series with each MOSFET source while ensuring saturated-mode operation of each transistor at $I_D = I$? In the latter limiting situation, what do V_1, V_2, V_3, and V_4 become?

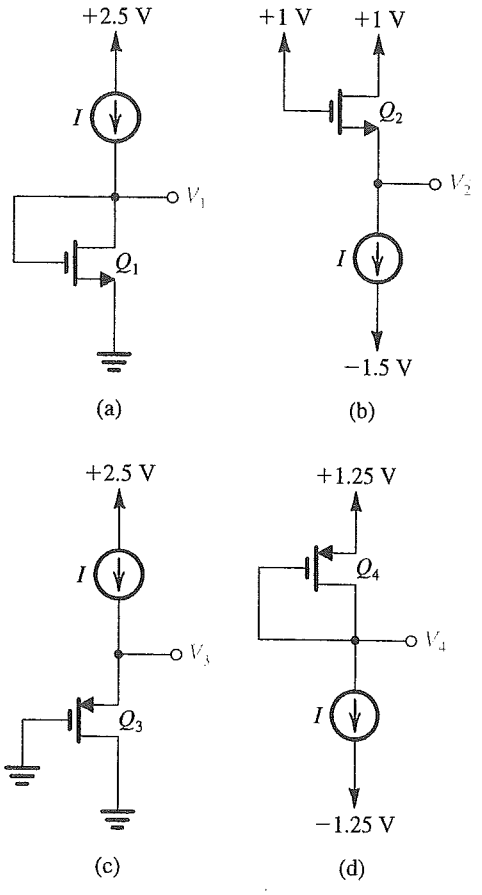

Figure P5.43

Case	Transistor	V_S	V_G	V_D	I_D	Type	Mode	$\mu C_{ox} W/L$	V_t
a	1	0	1	2.5	100				
	1	0	1.5	2.5	400				
b	2	5	3	−4.5	50				
	2	5	2	−0.5	450				
c	3	5	3	4	200				
	3	5	2	0	800				
d	4	−2	0	0	72				
	4	−4	0	−3	270				

Section 5.3: MOSFET Circuits at DC

Note: If λ is not specified, assume it is zero.

D 5.44 Design the circuit of Fig. P5.44 to establish a drain current of 0.1 mA and a drain voltage of +0.3 V. The MOSFET has $V_t = 0.5$ V, $\mu_n C_{ox} = 400\ \mu\text{A/V}^2$, $L = 0.4\ \mu\text{m}$, and $W = 5\ \mu\text{m}$. Specify the required values for R_S and R_D.

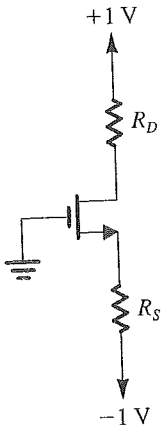

Figure P5.44

5.45 The NMOS transistor in the circuit of Fig. P5.44 has $V_t = 0.4$ V and $k_n = 4\ \text{mA/V}^2$. The voltages at the source and the drain are measured and found to be −0.6 V and +0.2 V, respectively. What current I_D is flowing, and what must the values of R_D and R_S be? What is the largest value for R_D for which I_D remains unchanged from the value found?

D 5.46 For the circuit in Fig. E5.10, assume that Q_1 and Q_2 are matched except for having different widths, W_1 and W_2. Let $V_t = 0.5$ V, $k_n' = 0.4\ \text{mA/V}^2$, $L_1 = L_2 = 0.36\ \mu\text{m}$, $W_1 = 1.44\ \mu\text{m}$, and $\lambda = 0$.

(a) Find the value of R required to establish a current of 50 μA in Q_1.

(b) Find W_2 and R_2 so that Q_2 operates at the edge of saturation with a current of 0.5 mA.

5.47 The transistor in the circuit of Fig. P5.47 has $k_n' = 0.4\ \text{mA/V}^2$, $V_t = 0.4$ V, and $\lambda = 0$. Show that operation at the edge of saturation is obtained when the following condition is satisfied:

$$\left(\frac{W}{L}\right)R_D \simeq 2.5\ \text{k}\Omega$$

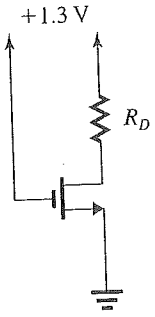

Figure P5.47

D 5.48 It is required to operate the transistor in the circuit of Fig. P5.47 at the edge of saturation with $I_D = 0.1$ mA. If $V_t = 0.4$ V, find the required value of R_D.

D 5.49 The PMOS transistor in the circuit of Fig. P5.49 has $V_t = -0.5$ V, $\mu_p C_{ox} = 100\ \mu\text{A/V}^2$, $L = 0.18\ \mu\text{m}$, and $\lambda = 0$. Find the values required for W and R in order to establish a drain current of 180 μA and a voltage V_D of 1 V.

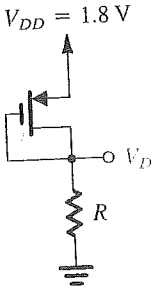

Figure P5.49

D 5.50 The NMOS transistors in the circuit of Fig. P5.50 have $V_t = 0.5$ V, $\mu_n C_{ox} = 250\ \mu\text{A/V}^2$, $\lambda = 0$, and $L_1 = L_2 = 0.25\ \mu\text{m}$. Find the required values of gate width for each of Q_1

and Q_2, and the value of R, to obtain the voltage and current values indicated.

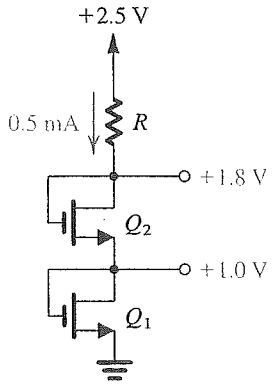

Figure P5.50

D 5.51 The NMOS transistors in the circuit of Fig. P5.51 have $V_t = 0.5$ V, $\mu_n C_{ox} = 90\ \mu\text{A/V}^2$, $\lambda = 0$, and $L_1 = L_2 = L_3 = 0.5\ \mu\text{m}$. Find the required values of gate width for each of Q_1, Q_2, and Q_3 to obtain the voltage and current values indicated.

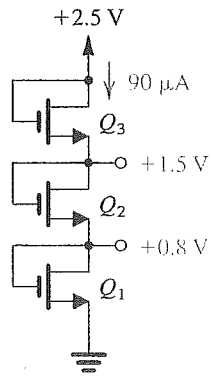

Figure P5.51

5.52 Consider the circuit of Fig. 5.24(a). In Example 5.5 it was found that when $V_t = 1$ V and $k_n'(W/L) = 1\ \text{mA/V}^2$, the drain current is 0.5 mA and the drain voltage is +7 V. If the transistor is replaced with another having $V_t = 1.5$ V with $k_n'(W/L) = 1.5\ \text{mA/V}^2$, find the new values of I_D and V_D. Comment on how tolerant (or intolerant) the circuit is to changes in device parameters.

D 5.53 Using a PMOS transistor with $V_t = -1.5$ V, $k_p'(W/L) = 4\ \text{mA/V}^2$, and $\lambda = 0$, design a circuit that resembles that in Fig. 5.24(a). Using a 10-V supply, design for a gate voltage of +6 V, a drain current of 0.5 mA, and a drain voltage of +5 V. Find the values of R_S and R_D. Also, find the values of the resistances in the voltage divider feeding the gate, assuming a 1-μA current in the divider.

5.54 The MOSFET in Fig. P5.54 has $V_t = 0.4$ V, $k_n' = 500\ \mu\text{A/V}^2$, and $\lambda = 0$. Find the required values of W/L and of R so that when $v_I = V_{DD} = +1.3$ V, $r_{DS} = 50\ \Omega$ and $v_O = 50$ mV.

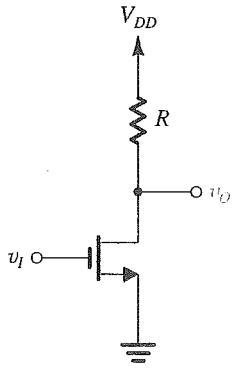

Figure P5.54

5.55 In the circuits shown in Fig. P5.55, transistors are characterized by $|V_t| = 1$ V, $k'W/L = 4\ \text{mA/V}^2$, and $\lambda = 0$.

(a) Find the labeled voltages V_1 through V_7.

(b) In each of the circuits, replace the current source with a resistor. Select the resistor value to yield a current as close to that of the current source as possible, while using resistors specified in the 1% table provided in Appendix J.

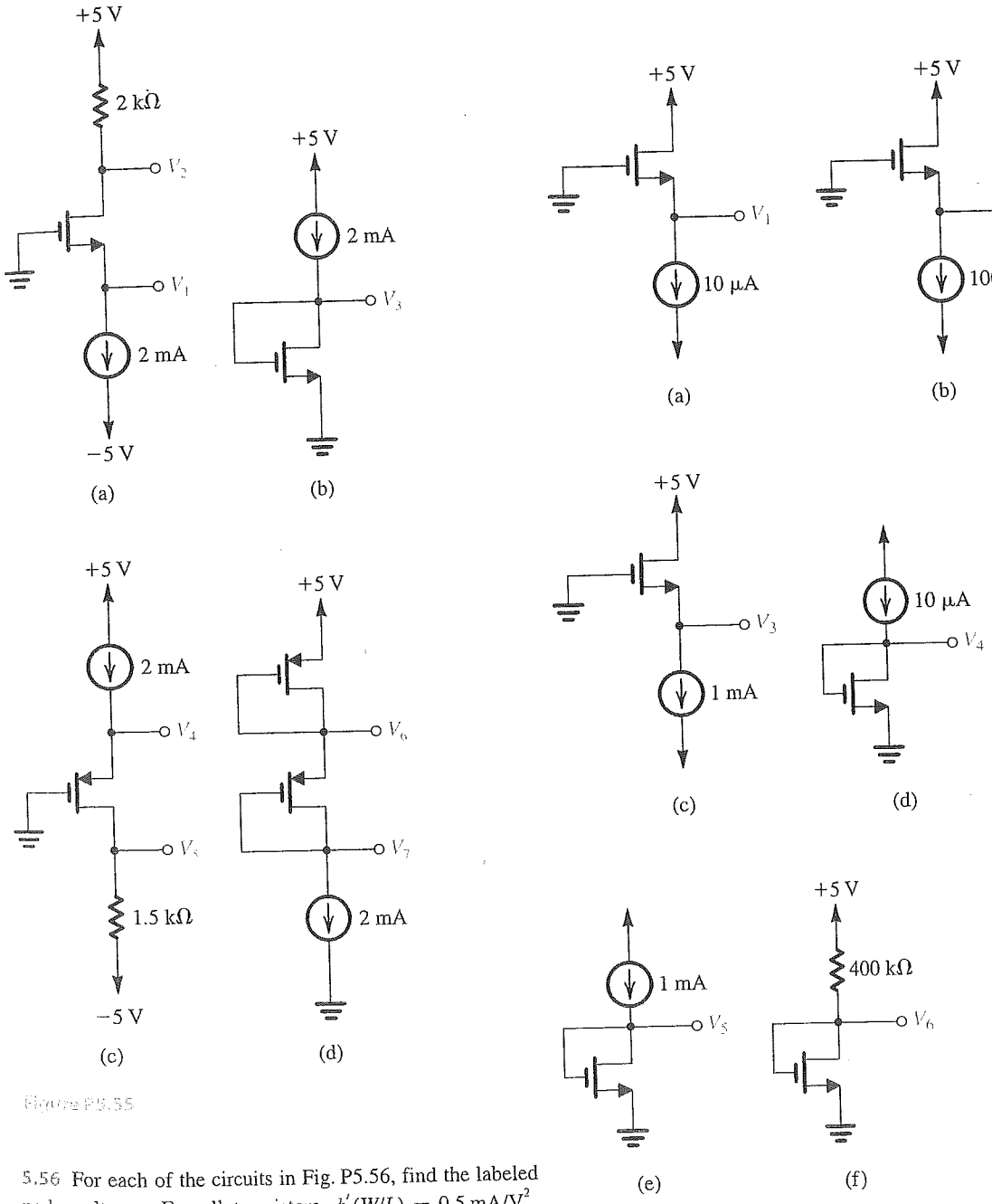

Figure P5.55

5.56 For each of the circuits in Fig. P5.56, find the labeled node voltages. For all transistors, $k_n'(W/L) = 0.5\ \text{mA/V}^2$, $V_t = 0.8$ V, and $\lambda = 0$.

Figure P5.56 *continued*

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

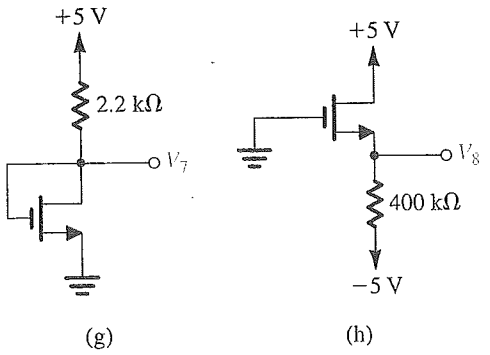

Figure P5.56 *continued*

5.57 For each of the circuits shown in Fig. P5.57, find the labeled node voltages. The NMOS transistors have $V_t = 0.9$ V and $k_n'(W/L) = 1.5$ mA/V^2.

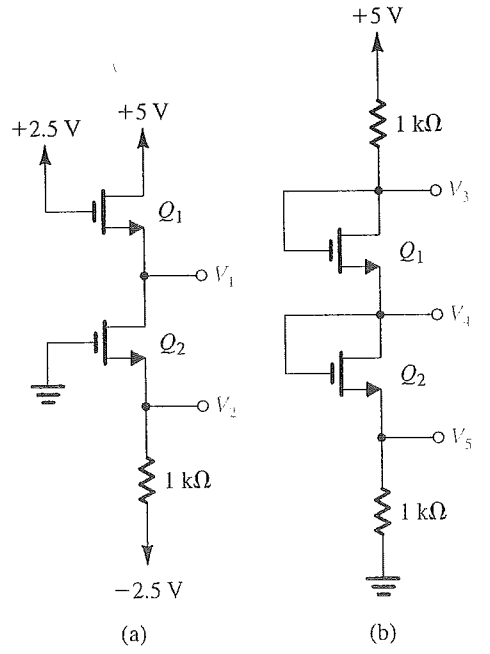

Figure P5.57

*5.58 For the circuit in Fig. P5.58:

(a) Show that for the PMOS transistor to operate in saturation, the following condition must be satisfied:

$$IR \leq |V_{tp}|$$

(b) If the transistor is specified to have $|V_{tp}| = 1$ V and $k_p = 0.2$ mA/V^2, and for $I = 0.1$ mA, find the voltages V_{SD} and V_{SG} for $R = 0$, 10 kΩ, 30 kΩ, and 100 kΩ.

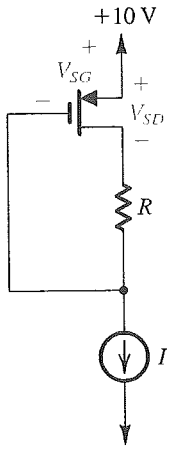

Figure P5.58

5.59 For the circuits in Fig. P5.59, $\mu_n C_{ox} = 3\mu_p C_{ox} = 270\ \mu$A/V^2, $|V_t| = 0.5$ V, $\lambda = 0$, $L = 1\ \mu$m, and $W = 3\ \mu$m, unless otherwise specified. Find the labeled currents and voltages.

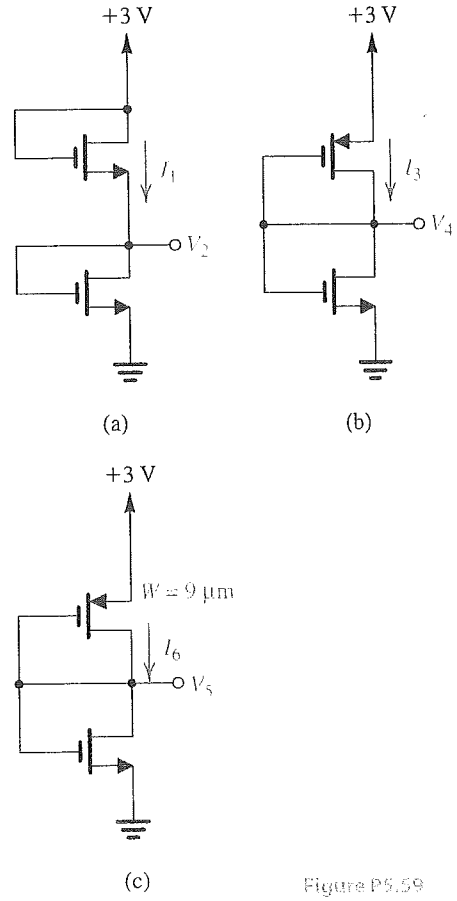

Figure P5.59

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

SIM *5.60 For the devices in the circuit of Fig. P5.60, $|V_t| = 1$ V, $\lambda = 0$, $\mu_n C_{ox} = 50\ \mu\text{A/V}^2$, $L = 1\ \mu\text{m}$, and $W = 10\ \mu\text{m}$. Find V_2 and I_2. How do these values change if Q_3 and Q_4 are made to have $W = 100\ \mu\text{m}$?

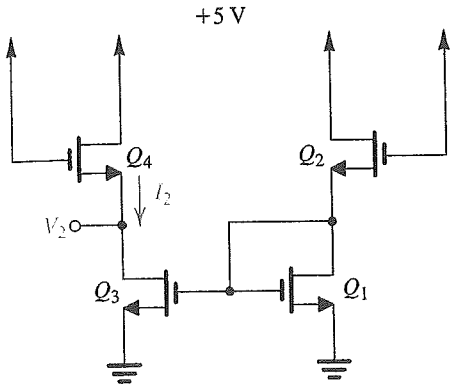

Figure P5.60

5.61 In the circuit of Fig. P5.61, transistors Q_1 and Q_2 have $V_t = 0.7$ V, and the process transconductance parameter $k_n' = 125\ \mu\text{A/V}^2$. Find V_1, V_2, and V_3 for each of the following cases:

(a) $(W/L)_1 = (W/L)_2 = 20$
(b) $(W/L)_1 = 1.5(W/L)_2 = 20$

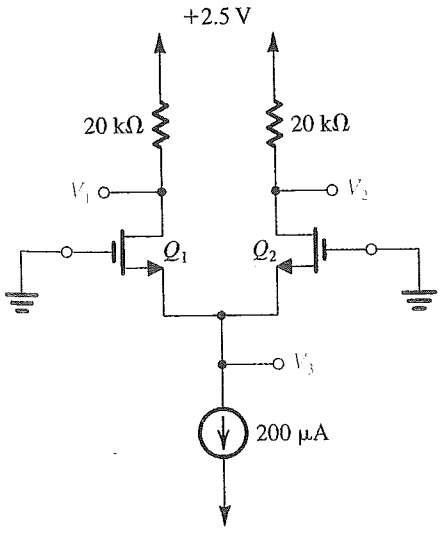

Figure P5.61

Section 5.4: The Body Effect and Other Topics

5.62 In a particular application, an n-channel MOSFET operates with V_{SB} in the range 0 V to 4 V. If V_{t0} is nominally 1.0 V, find the range of V_t that results if $\gamma = 0.5\ \text{V}^{1/2}$ and $2\phi_f = 0.6$ V. If the gate oxide thickness is increased by a factor of 4, what does the threshold voltage become?

5.63 A p-channel transistor operates in saturation with its source voltage 3 V lower than its substrate. For $\gamma = 0.5\ \text{V}^{1/2}$, $2\phi_f = 0.75$ V, and $V_{t0} = -0.7$ V, find V_t.

*5.64 (a) Using the expression for i_D in saturation and neglecting the channel-length modulation effect (i.e., let $\lambda = 0$), derive an expression for the per unit change in i_D per °C $\left[(\partial i_D/i_D)/\partial T\right]$ in terms of the per unit change in k_n' per °C $\left[(\partial k_n'/k_n')/\partial T\right]$, the temperature coefficient of V_t in V/°C $(\partial V_t/\partial T)$, and V_{GS} and V_t.
(b) If V_t decreases by 2 mV for every °C rise in temperature, find the temperature coefficient of k_n' that results in i_D decreasing by 0.2%/°C when the NMOS transistor with $V_t = 1$ V is operated at $V_{GS} = 5$ V.

5.65 A depletion-type n-channel MOSFET with $k_n'W/L = 2\ \text{mA/V}^2$ and $V_t = -3$ V has its source and gate grounded. Find the region of operation and the drain current for $v_D = 0.1$ V, 1 V, 3 V, and 5 V. Neglect the channel-length-modulation effect.

5.66 For a particular depletion-mode NMOS device, $V_t = -2$ V, $k_n'W/L = 200\ \mu\text{A/V}^2$, and $\lambda = 0.02\ \text{V}^{-1}$. When operated at $v_{GS} = 0$, what is the drain current that flows for $v_{DS} = 1$ V, 2 V, 3 V, and 10 V? What does each of these currents become if the device width is doubled with L the same? With L also doubled?

*5.67 Neglecting the channel-length-modulation effect, show that for the depletion-type NMOS transistor of Fig. P5.67, the i–v relationship is given by

$$i = \frac{1}{2}k_n'(W/L)\left(v^2 - 2V_t v\right) \qquad \text{for } v \geq V_t$$

$$i = -\frac{1}{2}k_n'(W/L)V_t^2 \qquad \text{for } v \leq V_t$$

(Recall that V_t is negative.) Sketch the i–v relationship for the case: $V_t = -2$ V and $k_n'(W/L) = 2\ \text{mA/V}^2$.

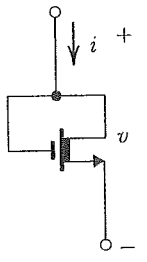

Figure P5.67

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem