

VHDL Assignment #3: Design and Simulation of Digital Circuits

In this lab you will learn how to use CAD tools and VHDL to implement simple digital systems.

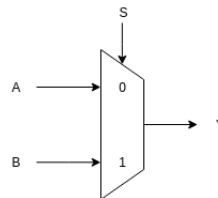
1 Learning Outcomes

After completing this lab you should know how to:

- Synthesize logic functions
- Use CAD tools and VHDL to implement logic functions
- Perform functional simulation

2 VHDL Implementation of a 2-to-1 MUX

A multiplexer is a circuit that selects between several inputs and forwards it to a single output. In general, a 2^n -to-1 MUX has 2^n inputs with n selectors. A schematic diagram of a 2-to-1 multiplexer is given below.



According to the above schematic, the 2-to-1 multiplexer outputs the input signal A when the selector signal S is equal to 0 otherwise it outputs the input signal B . In this lab, you will implement this 2-to-1 multiplexer in VHDL using structural and behavioral styles. In the structural modeling of the 2-to-1 multiplexer in VHDL, the multiplexer is implemented using AND, OR or NOT gates only. More specifically, the structural description of the multiplexer literally realizes its boolean function. Describe the boolean function in VHDL using AND, OR or NOT gates only. Use the following entity declaration for your VHDL description of the 2-to-1 multiplexer:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
entity firstname_lastname_MUX_structural is
    Port (A      : in  std_logic;
          B      : in  std_logic;
          S      : in  std_logic;
          Y      : out std_logic);
end firstname_lastname_MUX_structural;
```

Make sure to replace `firstname_lastname` with your full name. Once completed, you will describe the architecture of the 2-to-1 multiplexer using behavioral style. In the behavioral description, you describe the behavior of your target circuit and the synthesis tool creates a gate-level layout of your design. Use a single VHDL select assignment only and the entity declaration below to implement a behavioral description of the 2-to-1 multiplexer (see the previous VHDL assignment for more details).

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
```

```

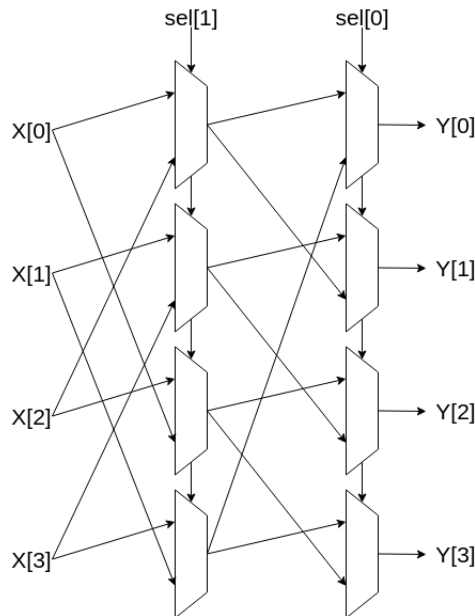
entity firstname_lastname_MUX_behavioral is
  Port (A      : in  std_logic;
        B      : in  std_logic;
        S      : in  std_logic;
        Y      : out std_logic);
end firstname_lastname_MUX_behavioral;

```

Once described both behavioral and structural styles of the 2-to-1 multiplexer in VHDL, you are required to test your circuits. Write a testbench code and perform an exhaustive test for your VHDL descriptions of the 2-to-1 multiplexer.

3 VHDL Implementation of a 4-bit circular barrel shifter

In this part of the lab, you will design a circuit that implements an 4-bit circular barrel shifter. The circular barrel shifter is a circuit that can shift its input by a given number of bits with combinational logic. The 4-bit circular barrel shifter is usually implemented by stacking two layers of 2×1 multiplexers as shown below. All 4 multiplexers in the leftmost layer use `sel(1)` as the selector signal. Similarly, all 4 multiplexers in the rightmost layer use `sel(0)` as the selector signal. Make sure that you familiarize yourself with how the barrel shifter works by calculating its output for several input combinations by hand.



Similar to the first part of the assignment, you will implement the 4-bit barrel shifter in VHDL using both structural and behavioral styles. To obtain a structural description of the 4-bit barrel shifter, you are required to use the structural description of the 2-to-1 multiplexer. Write a structural VHDL description for the 4-bit circular barrel shifter by instantiating the structural description of the 2-to-1 multiplexer 8 times. Use the following entity declaration for your structural VHDL description of the 4-bit circular barrel shifter:

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
entity firstname_lastname_barrel_shifter_structural is
  Port (X      : in  std_logic_vector (3 downto 0);
        sel    : in  std_logic_vector (1 downto 0);
        Y      : out std_logic_vector (3 downto 0));
end firstname_lastname_barrel_shifter_structural;

```

Once completed, you are required to implement the 4-bit circular barrel shifter using the behavioral style. One way to obtain a behavioral description of the 4-bit circular barrel shifter is the use of VHDL select statements.

Write a behavioral VHDL code for the 4-bit circular barrel shifter using a single VHDL select statement only. Use the following entity declaration for your behavioral VHDL description of the 4-bit circular barrel shifter:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
entity firstname_lastname_barrel_shifter_behavioral is
    Port (X          : in  std_logic_vector (3 downto 0);
          sel        : in  std_logic_vector (1 downto 0);
          Y          : out std_logic_vector (3 downto 0));
end firstname_lastname_barrel_shifter_behavioral;
```

Hint: You may want to use the VHDL concatenate operator *ampersand* (&). It can be used to combine two or more signals together. Note that all input signals to the concatenation must be of the same type and the result of the concatenation needs to exactly fit the width of the concatenated input signals.

Once you have your circuit described in VHDL using both structural and behavioral styles, write a testbench code and perform an exhaustive test for your VHDL descriptions of the 4-bit circular barrel shifter.

4 Demo

Instead of submitting a report, you will give a demo to one of the TAs during your scheduled lab session in the week of Feb. 3rd. Example questions are provided below.

5 Questions

1. Explain your VHDL code.
2. Report the number of pins and logic modules used to fit your designs on the FPGA board.

	2-to-1 MUX		4-bit circular barrel shifter	
	Structural	Behavioral	Structural	Behavioral
Logic Utilization (in ALMs)	1/32070(<1%)	1/32070(<1%)	5/32070(<1%)	5/32070(<1%)
Total pins	4/457(<1%)	4/457(<1%)	10/457(2%)	10/457(2%)

3. Show representative simulation plots of the 2-to-1 MUX circuits for all the possible input values.
4. Show representative simulation plots of the 4-bit circular shift register circuits for a given input sequence, e.g., "1011" (X = "1011"), for all the possible shift amounts.