

Aguilar_LE4-2_1



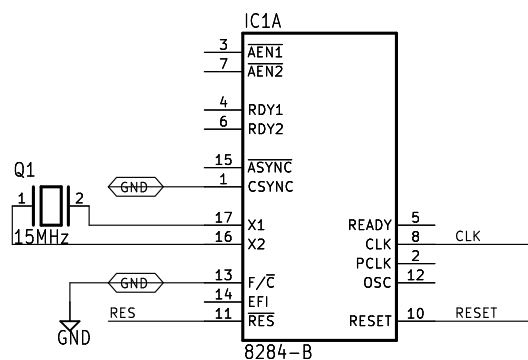
Aguilar_LE4-2_2



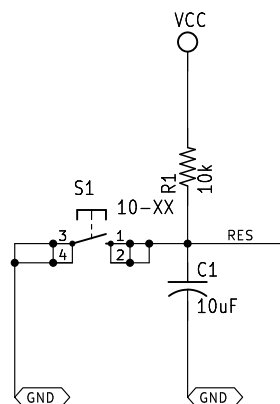
Aguilar_LE4-2_3



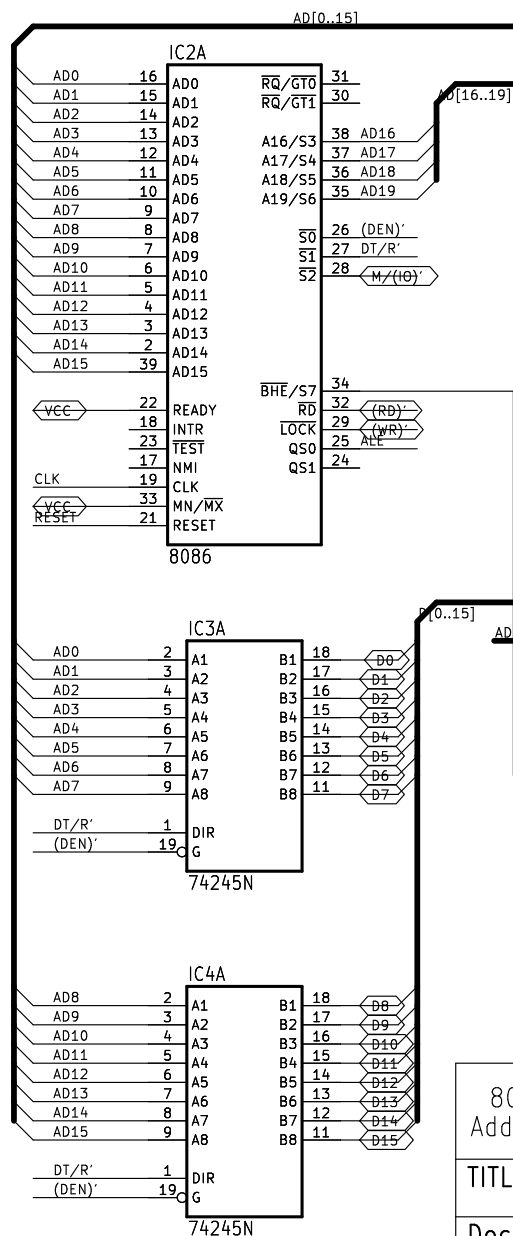
Clock Generator



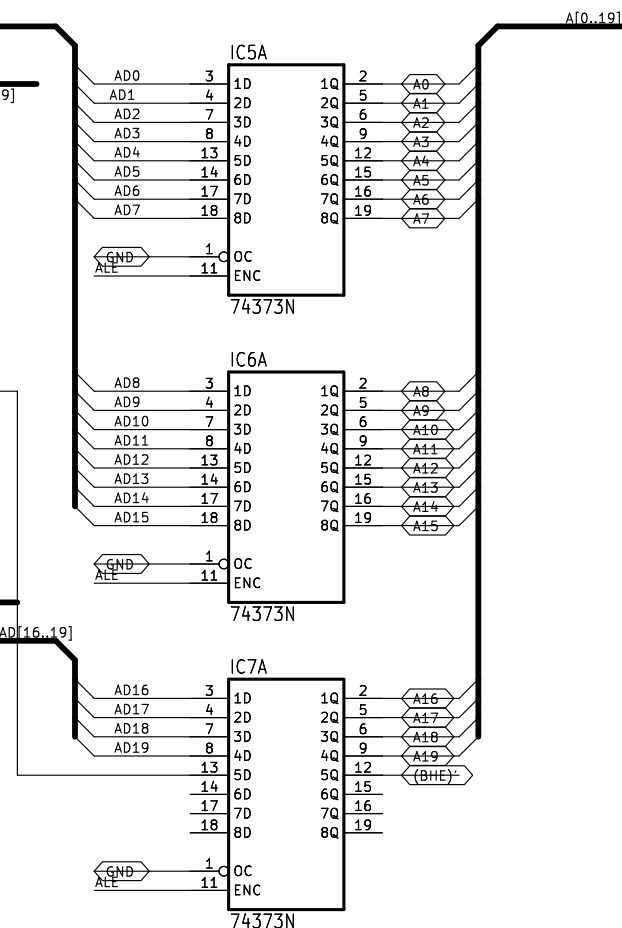
Reset Circuit



Data Bus (to memory & I/O)



Address Bus (to memory & I/O)



8086 with Clock Generator Sean Karl Tyrese G. Aguilar
Address Latch and Data Buffer Designer

TITLE: Aguilar_LE4-2

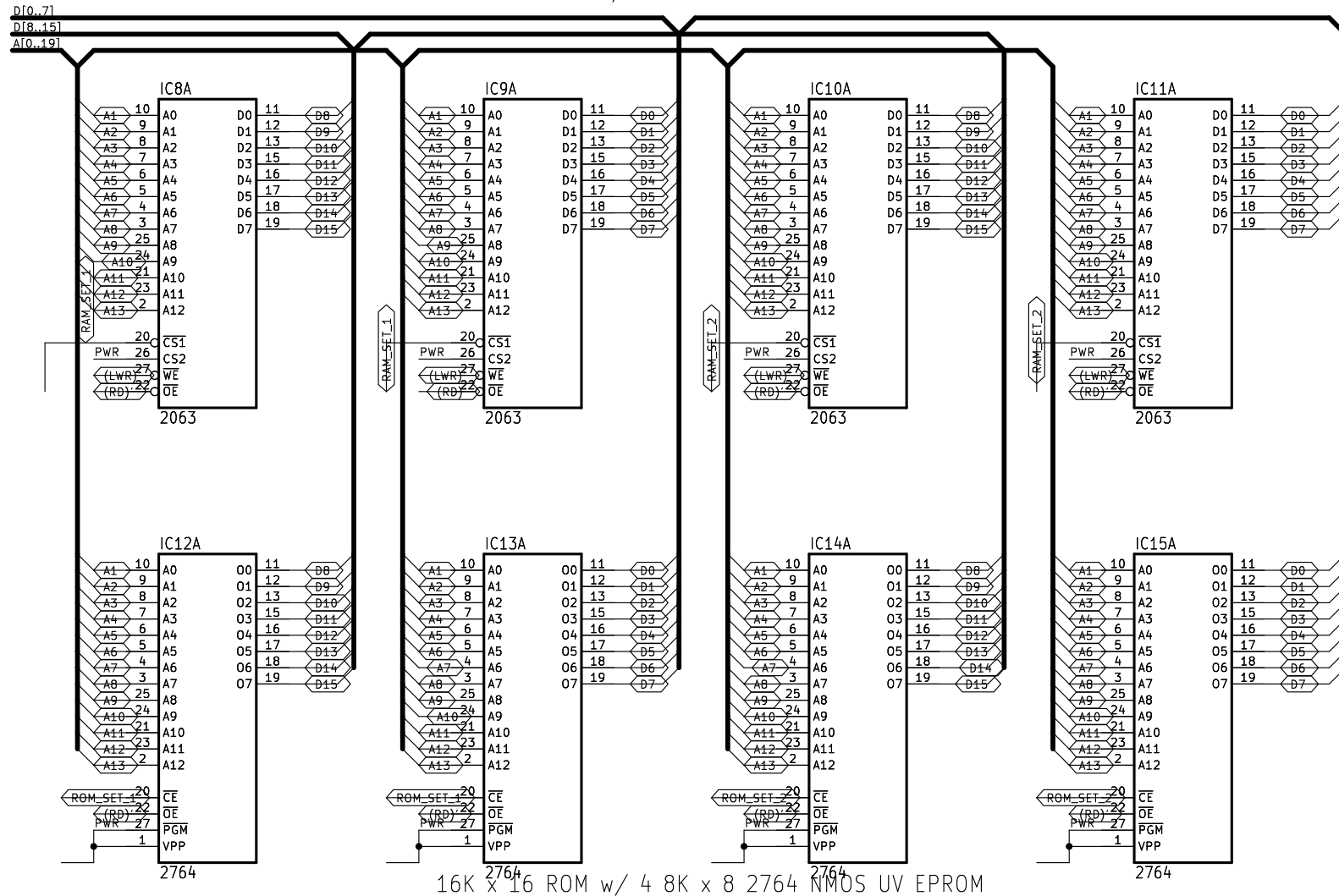
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16K x 16 RAM w/ 4 8K x 8 2063 CMOS SRAM



16K x 16 ROM w/ 4 8K x 8 2764 NMOS UV EPROM



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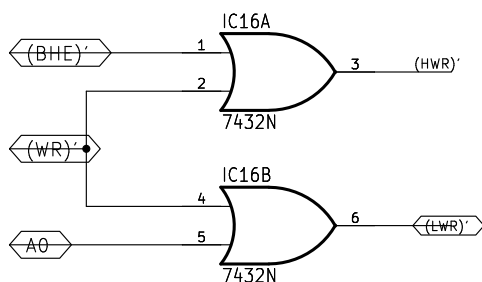
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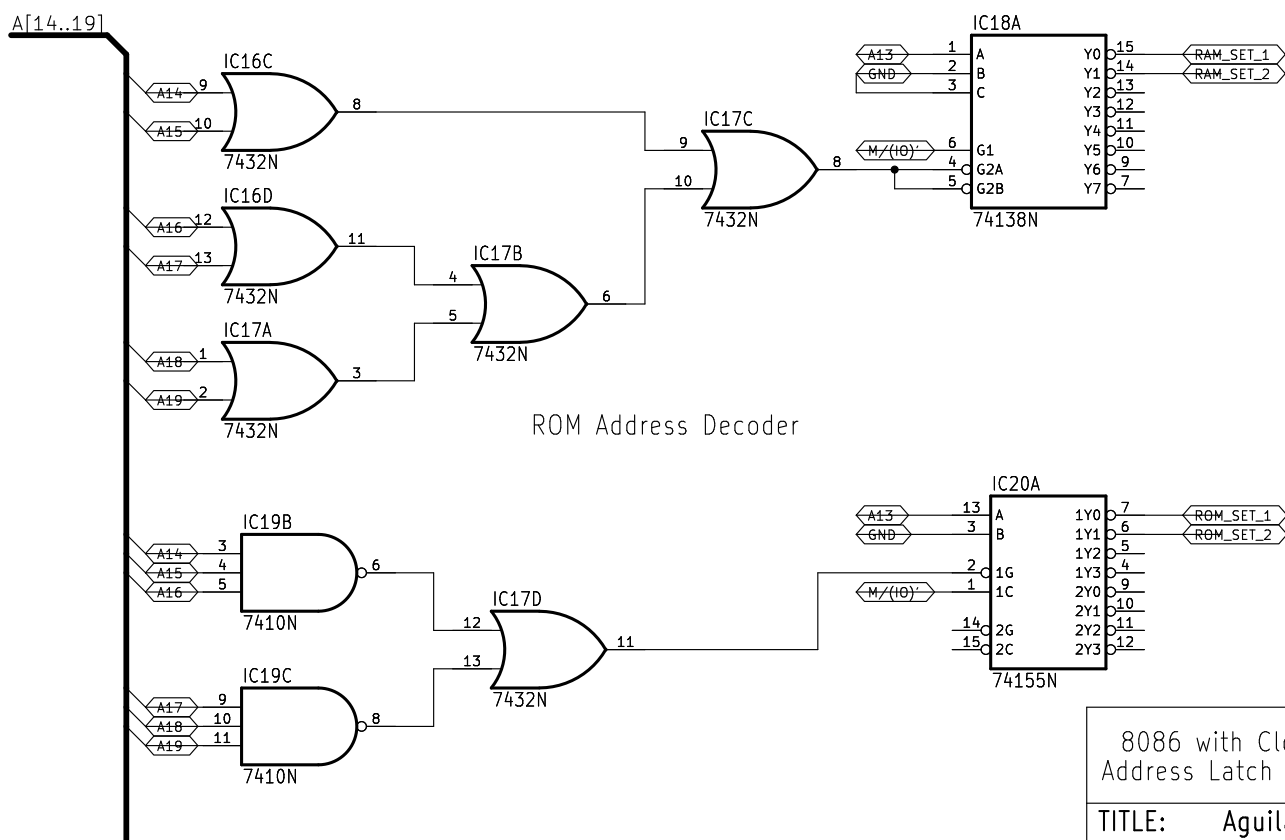
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Bank Select Circuit

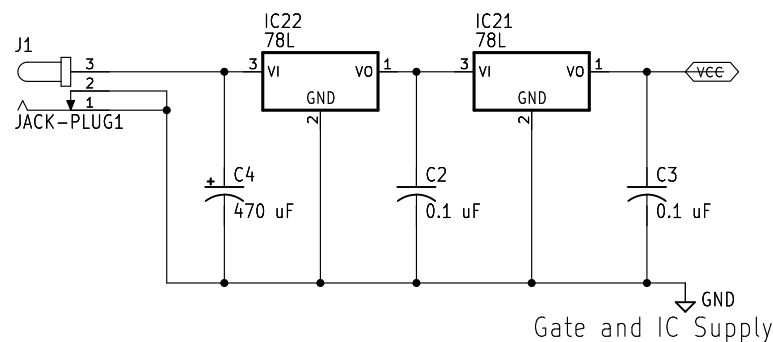


RAM Address Decoder

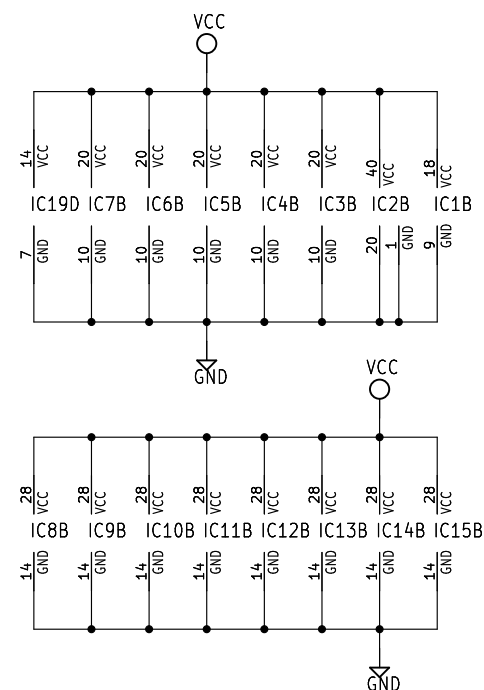


ROM Address Decoder

Power Supply with Regulator



Gate and IC Supply



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Address Latch and Data Buffer Designer

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