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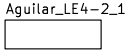

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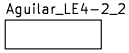

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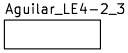
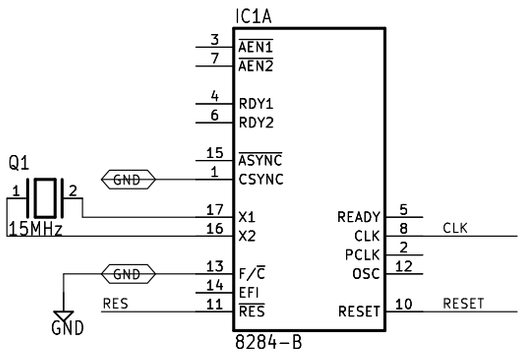
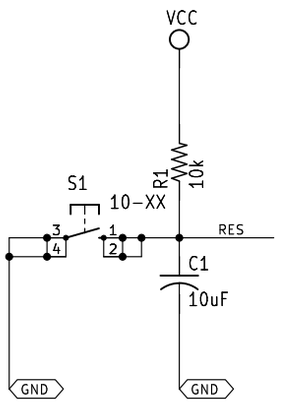


Clock Generator

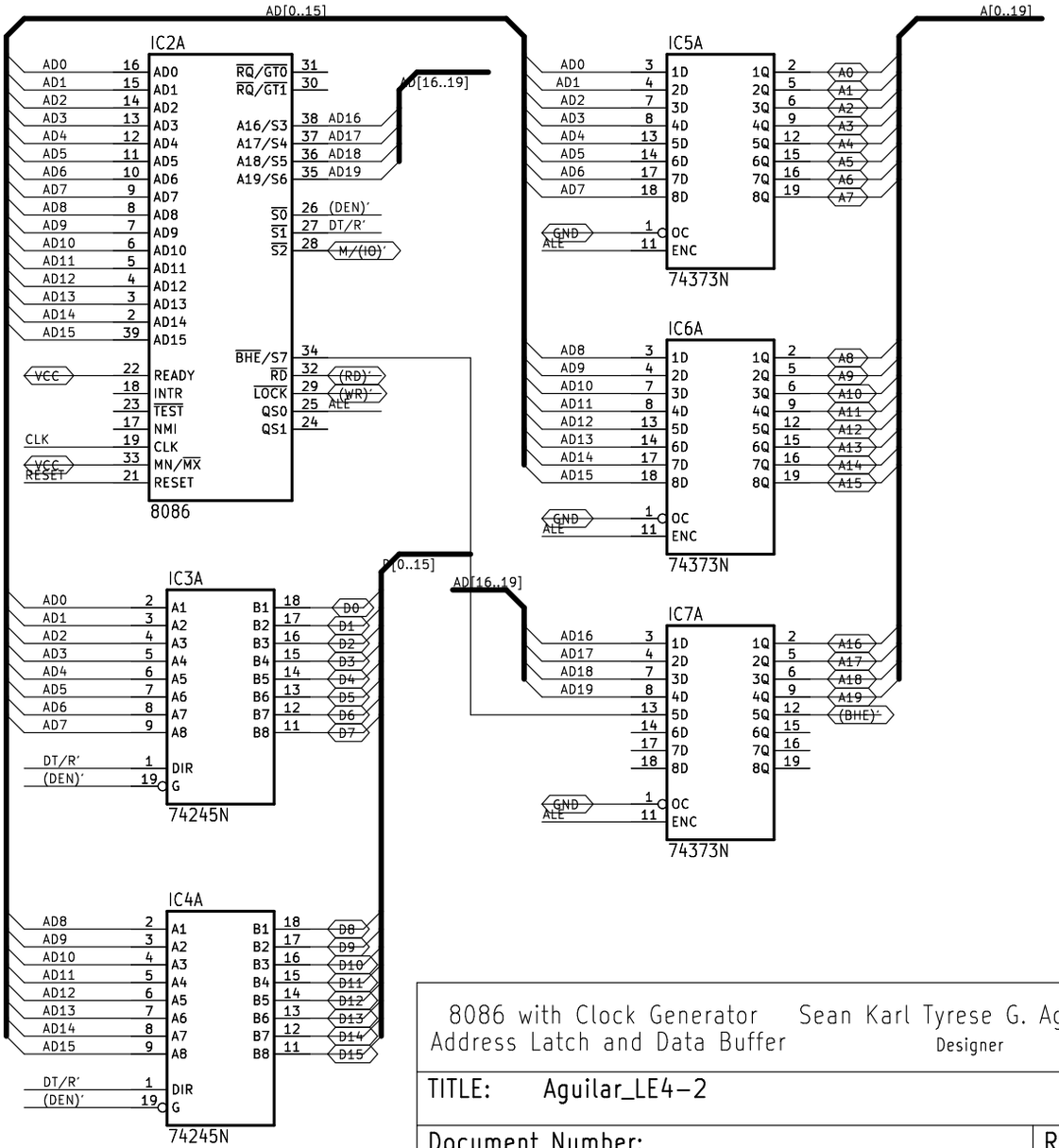


Reset Circuit



Data Bus (to memory & I/O)

Address Bus (to memory & I/O)



8086 with Clock Generator Address Latch and Data Buffer	Sean Karl Tyrese G. Aguilar Designer	
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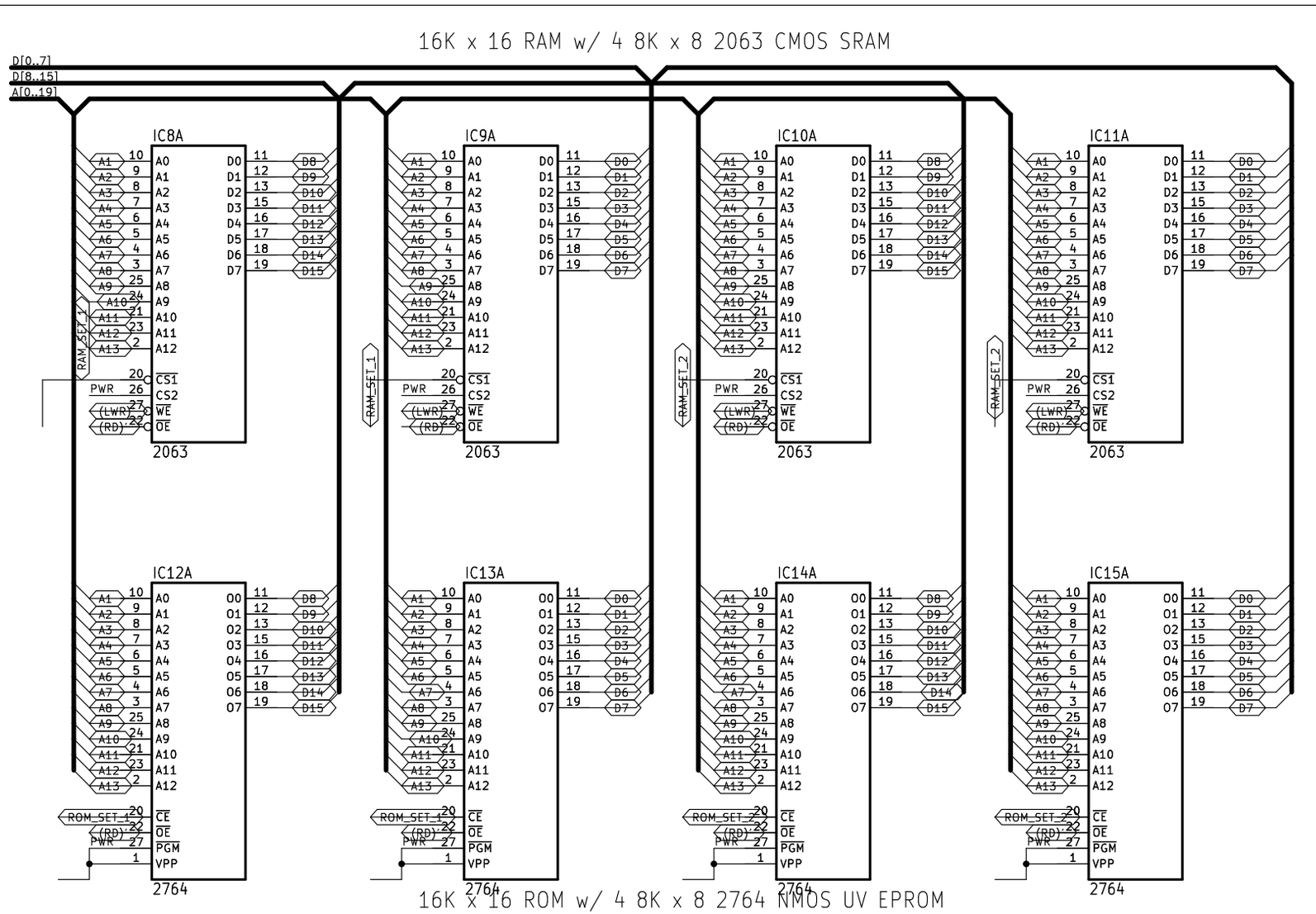
Document Number: CpE 3104 - LE4-2		REV: 1.0
Date: 2024-10-02	Sheet: 1/4	



8086 with Clock Generator Address Latch and Data Buffer	Sean Karl Tyrese G. Aguilar Designer	
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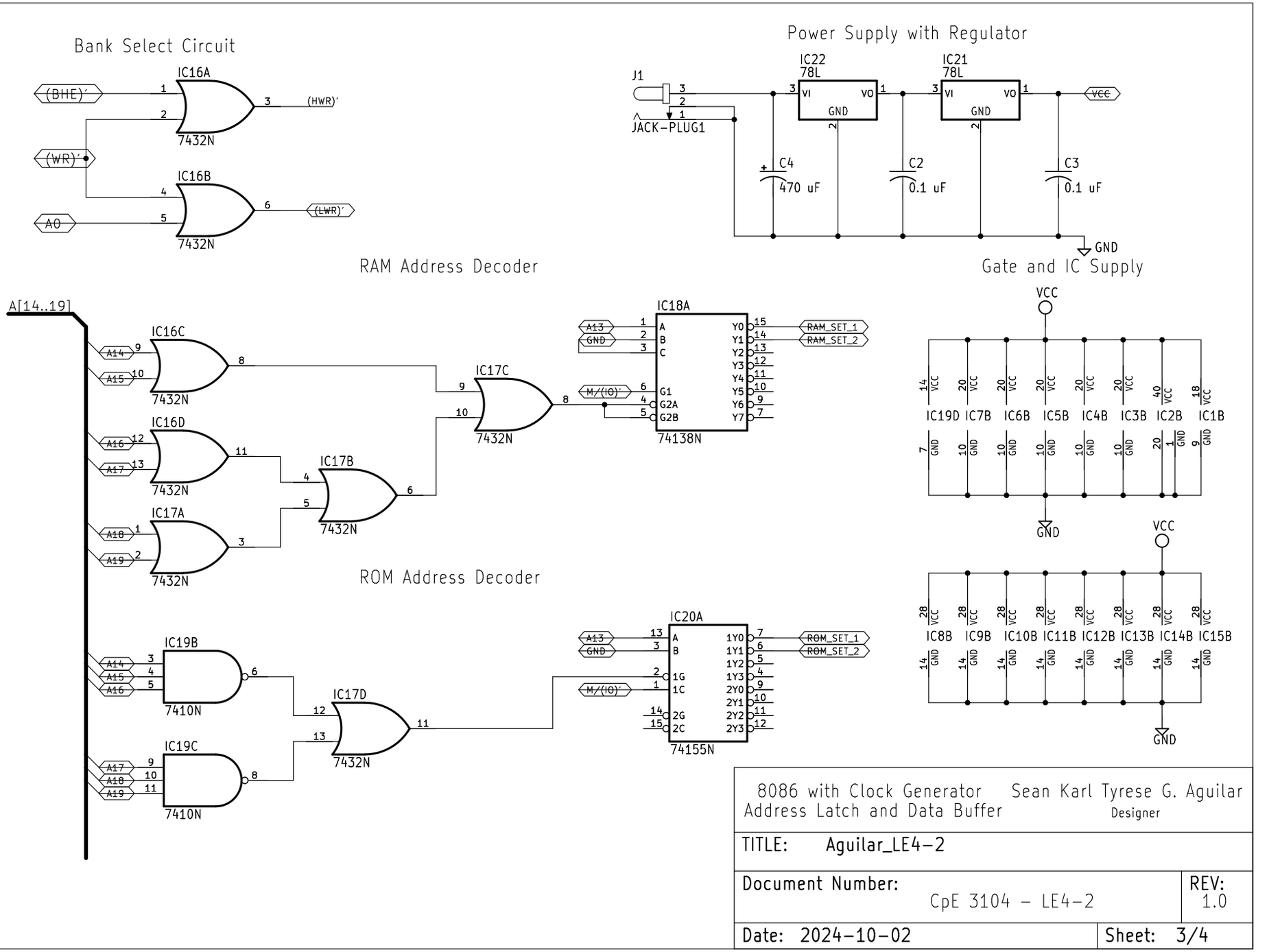
Document Number: CpE 3104 - LE4-2		REV: 1.0
Date: 2024-10-02	Sheet: 2/4	



8086 with Clock Generator Address Latch and Data Buffer

Sean Karl Tyrese G. Aguilar
Designer

TITLE: Aguilar_LE4-2

Document Number: CpE 3104 - LE4-2

REV: 1.0

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