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CS 20 PROJECT 2: Stopwatch and Countdown Timer

This documentation contains the schematics, truth tables, k-maps as well as explanations regarding the schematic design and decisions of the pair. Additional information will be given on the documentation video

The general schematic of the whole circuit is shown below and is composed of the components: buttons (play, pause, reset, increment, and decrement), a mode selector with a bit width of one (1), four (4) 7 segment display, as well as the several subcircuits that composes the clocks, buttons and the circuitry for the LED.

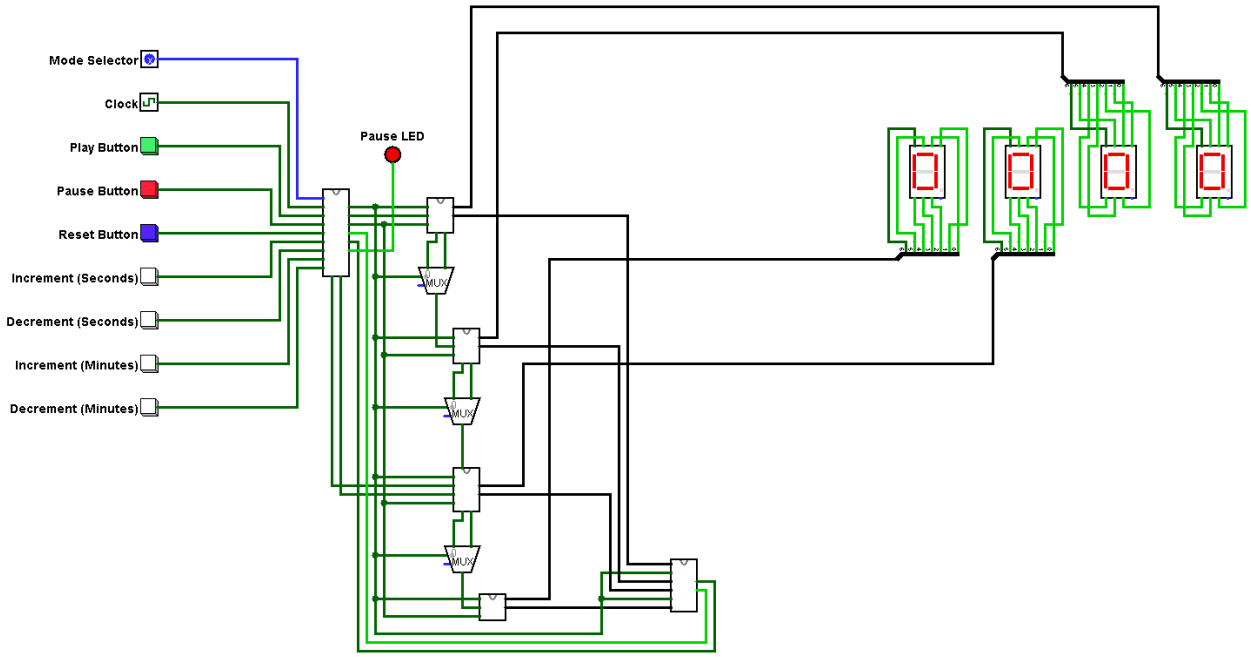

Figure 1. General Schematics of the Project

To show and explain every detail of the schematic, we will be discussing the flow of the circuitry in the general mechanics while explaining in detail the subcircuits we will pass through. Each part will be discussed in detail and its schematic will be shown as well. For us to start discussing, we must first list down all the functions the project has. Listed below are some if not all of the functions found in the project.

- Can automatically count up or count down to 59:59 and 00:00 respectively
- Mode Selector selects whether the circuit will count up or count down
- Play button is used to start the counter
- Pause button is used to stop the counter at its current value
- Reset button is used to reset the counter to 00:00 and pause it at the same time
- Increment button is used to add 1 in decimal value to the preferred time slot (seconds or minutes)
- Decrement button is used to subtract 1 in decimal value to the preferred time slot (seconds or minutes)
- The minutes and seconds component are interconnected with each other and will change each value when reaching the maximum value (for example incrementing the seconds of 00:59 will make the value 01:00)
- The counter will automatically pause/stop when reaching its highest maximum value (59:59 for Stopwatch and 00:00 for Timer).
- Incrementing 59:59 will make the value of the counter be 00:00 while decrementing 00:00 will not yield to any result

If there are any forgotten functions, the pair will be discussing it thoroughly while explaining the specifics of the circuitry.

For the circuitry to work, the user must first select on whether s/he will have to decide on what mode s/he wants to use (stopwatch - 0, timer - 1) as well as the initial value she wants to start with (using the increment and decrement buttons). After deciding the user must press play which will then send a signal to the first sub circuit in the general schematic. Shown below is the schematic/figure for the clock and buttons functions of the circuit.

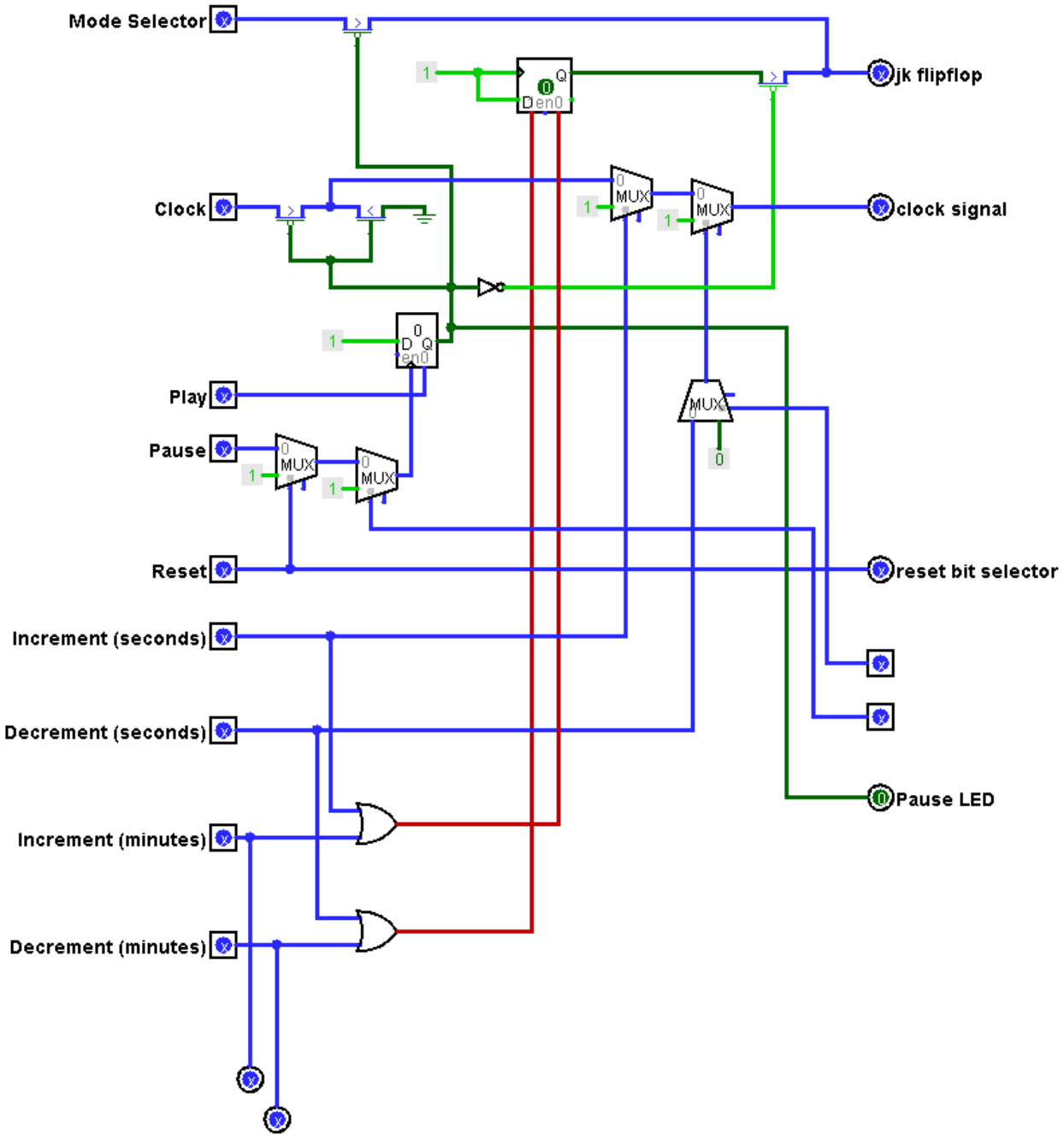

Figure 1.1 Schematics of Clock and Buttons

The sub circuit works by getting the buttons, clock, as well as the mode selector as inputs. By pressing the play button, it resets the signal of the register (positive-edge triggered) and turns it to 0. This signal is connected to the gate of the pmos found in the mode selector which makes it possible for the signal from the mode selector to pass through (since a signal of 1 in the gate of pmos blocks the flow). The pause button simply does it the other way. By connecting the signal

of the pause button to the clock of the register it sends out a tick in the register which then sends out the signal Q to the gate of the cmos thus blocking the flow and stopping the counter. This signal Q is also connected to an output pin which will be used for the Pause LED in the main circuit. The 1st multiplexer found in the pause connection serves the purpose such that when reset is pressed, sends out a signal to the pause button as well so that the value resets and pauses at the same time. The 2nd multiplexer will be further discussed later. The reset button is connected to the different flip-flops found in the 4 subcircuits to be shown later. What it basically does is that it resets all the values of flip flops into 0 so that the shown value in the LED will all be 0.

Next, the increment and decrement buttons (seconds) are each connected to a multiplexer. For the increment button (seconds), it serves as the select bit of a multiplexer (3rd) such that when the counter is paused, if the button is pressed, a constant 1 would still flow through the clock wiring. The output of this multiplexer is then connected to another multiplexer (5th). The decrement button (seconds) together with a constant 0, is connected to a multiplexer (4th) that has an input pin for the select bit which will be discussed later. The output of this multiplexer is connected as the select bit of the 5th multiplexer. The mechanism of the 5th multiplexer is the same as the 3rd one such that if the counter is paused, when the decrement button is pressed there would still be a constant 1 that would flow through the connection. For now, both the increment and decrement buttons (minutes) are connected to output pins that would be discussed later.

Now, notice that the signal from the increment (seconds) and increment (minutes) buttons are both inputs to an OR gate. The output of this OR gate is then connected to the clear of a D flip-flop (positive-edge triggered). The same goes for the decrement (seconds) and decrement (minutes) buttons. Both are inputs to an OR gate and the output is then connected to the preset of the same D-flip flop. The D flip-flop has a constant 1 for its clock and input D. This serves as the mode selector when the counter is paused and the increment and decrement buttons are being used. Notice that the output of this flip-flop Q is then connected to a pmos so that when the play button is pressed, the connection from this flip flop gets blocked. This is the reason why there is a NOT gate connected to the signal Q from the register earlier.

The next few subcircuits contain the connection of the stopwatch/timer. For this, the pair used JK flip flops to implement a moore circuit. A moore circuit is needed for the counter because it would determine the next states depending on the mode selected. Since the highest value needed for the counter is 9 which is made up of four bits (1001). The pair used four JK flip flops with the outputs (Q3, Q2, Q1, Q0). The truth table and k-maps are shown below:

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Mode (M)	Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+	J_3	K_3	J_2	K_2
0	0	0	0	0	0	0	0	1	0	x	0	x
0	0	0	0	1	0	0	1	0	0	x	0	x
0	0	0	1	0	0	0	1	1	0	x	0	x
0	0	0	1	1	0	1	0	0	0	x	1	x
0	0	1	0	0	0	1	0	1	0	x	x	0
0	0	1	0	1	0	1	1	0	0	x	x	0
0	0	1	1	0	0	1	1	1	0	x	x	0
0	0	1	1	1	1	0	0	0	1	x	x	1
0	1	0	0	0	1	0	0	1	x	0	0	x
0	1	0	0	1	1	0	1	0	x	0	0	x
0	1	0	1	0	1	0	1	1	x	0	0	x
0	1	0	1	1	1	1	0	0	x	0	1	x
0	1	1	0	0	1	1	0	1	x	0	x	0
0	1	1	0	1	1	1	1	0	x	0	x	0
0	1	1	1	0	1	1	1	1	x	0	x	0
0	1	1	1	1	0	0	0	0	x	1	x	1
1	0	0	0	0	1	1	1	1	1	x	1	x
1	1	1	1	1	1	1	1	0	x	0	x	0
1	1	1	1	0	1	1	0	1	x	0	x	0
1	1	1	0	1	1	1	0	0	x	0	x	0
1	1	1	0	0	1	0	1	1	x	0	x	1
1	1	0	1	1	1	0	1	0	x	0	0	x
1	1	0	1	0	1	0	0	1	x	0	0	x
1	1	0	0	1	1	0	0	0	x	0	0	x
1	1	0	0	0	0	1	1	1	x	1	1	x
1	0	1	1	0	1	1	0	0	x	x	0	0
1	0	1	1	1	1	1	0	1	x	x	0	0
1	0	1	0	0	1	0	1	0	x	x	0	0
1	0	1	0	1	1	0	0	0	x	x	0	0
1	0	0	1	0	1	0	0	1	x	x	0	1
1	0	0	1	1	1	0	0	0	x	0	0	x
1	0	0	0	0	1	1	1	1	x	1	1	x
1	0	0	0	1	1	1	1	0	x	0	x	0

Table 1.1

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Mode (M)	Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+	J_1	K_1	J_0	K_0
0	0	0	0	0	0	0	0	1	0	x	1	x
0	0	0	0	1	0	0	1	0	1	x	x	1
0	0	0	1	0	0	0	1	1	x	0	1	x
0	0	0	1	1	0	1	0	0	x	1	x	1
0	0	1	0	0	0	1	0	1	0	x	1	x
0	0	1	0	1	0	1	1	0	1	x	x	1
0	0	1	1	0	0	1	1	1	x	0	1	x
0	0	1	1	1	1	0	0	0	x	1	x	1
0	1	0	0	0	1	0	0	1	0	x	1	x
0	1	0	0	1	1	0	1	0	1	x	x	1
0	1	0	1	0	1	0	1	1	x	0	1	x
0	1	0	1	1	1	1	0	0	x	1	x	1
0	1	1	0	0	1	1	0	1	0	x	1	x
0	1	1	0	1	1	1	1	0	1	x	x	1
0	1	1	1	0	1	1	1	1	x	0	1	x
0	1	1	1	1	0	0	0	0	x	1	x	1
1	0	0	0	0	1	1	1	1	1	x	1	x
1	1	1	1	1	1	1	1	0	x	0	x	1
1	1	1	0	1	1	1	0	1	x	1	1	x
1	1	0	1	1	1	1	0	0	0	x	x	1
1	1	0	0	1	0	1	1	1	x	1	1	x
1	0	1	1	1	0	1	0	x	0	x	1	
1	0	1	0	1	0	0	1	x	1	1	x	
1	0	0	1	1	0	0	0	0	x	x	1	
1	0	0	0	0	1	1	1	1	x	1	x	
1	0	1	1	1	0	1	1	0	x	0	x	1
1	0	1	1	0	1	0	1	x	1	1	x	
1	0	1	0	1	0	1	0	0	0	x	x	1
1	0	1	0	0	0	0	1	1	1	x	1	x
1	0	0	1	1	0	0	1	0	x	0	x	1
1	0	0	1	0	0	0	0	1	x	1	1	x
1	0	0	0	1	0	0	0	0	0	x	x	1

Table 1.2

		Q2 Q1 Q0							
		000	001	011	010	110	111	101	100
M Q3	00	0	0	0	0	0	1	0	0
	01	X	X	X	X	X	X	X	X
	11	X	X	X	X	X	X	X	X
	10	1	0	0	0	0	0	0	0
Minimum SOP: M'Q2Q1Q0 + MQ2'Q1'Q0'									

K-map for J3

		Q2 Q1 Q0							
		000	001	011	010	110	111	101	100
M Q3	00	X	X	X	X	X	X	X	X
	01	0	0	0	0	0	1	0	0
	11	1	0	0	0	0	0	0	0
	10	X	X	X	X	X	X	X	X
Minimum SOP: M'Q2Q1Q0 + MQ2'Q1'Q0'									

K-map for K3

		Q2 Q1 Q0							
		000	001	011	010	110	111	101	100
M Q3	00	0	0	1	0	X	X	X	X
	01	0	0	1	0	X	X	X	X
	11	1	0	0	0	X	X	X	X
	10	1	0	0	0	X	X	X	X
Minimum SOP: M'Q1Q0 + MQ1'Q0'									

K-map for J2

	Q2 Q1 Q0							
M Q3	000	001	011	010	110	111	101	100
00	X	X	X	X	0	1	0	0
01	X	X	X	X	0	1	0	0
11	X	X	X	X	0	0	0	1
10	X	X	X	X	0	0	0	1
Minimum SOP: M'Q1Q0 + MQ1'Q0'								

K-map for K2

	Q2 Q1 Q0							
M Q3	000	001	011	010	110	111	101	100
00	0	1	X	X	X	X	1	0
01	0	1	X	X	X	X	1	0
11	1	0	X	X	X	X	0	1
10	1	0	X	X	X	X	0	1
Minimum SOP: M'Q0 + MQ0'								

K-map for J1

	Q2 Q1 Q0							
M Q3	000	001	011	010	110	111	101	100
00	X	X	1	0	0	1	X	X
01	X	X	1	0	0	1	X	X
11	X	X	0	1	1	0	X	X
10	X	X	0	1	1	0	X	X
Minimum SOP: M'Q0 + MQ0'								

K-map for K1

		Q2 Q1 Q0							
		000	001	011	010	110	111	101	100
M Q3	00	1	X	X	1	1	X	X	1
	01	1	X	X	1	1	X	X	1
	11	1	X	X	1	1	X	X	1
	10	1	X	X	1	1	X	X	1
Minimum SOP: 1									

K-map for J0

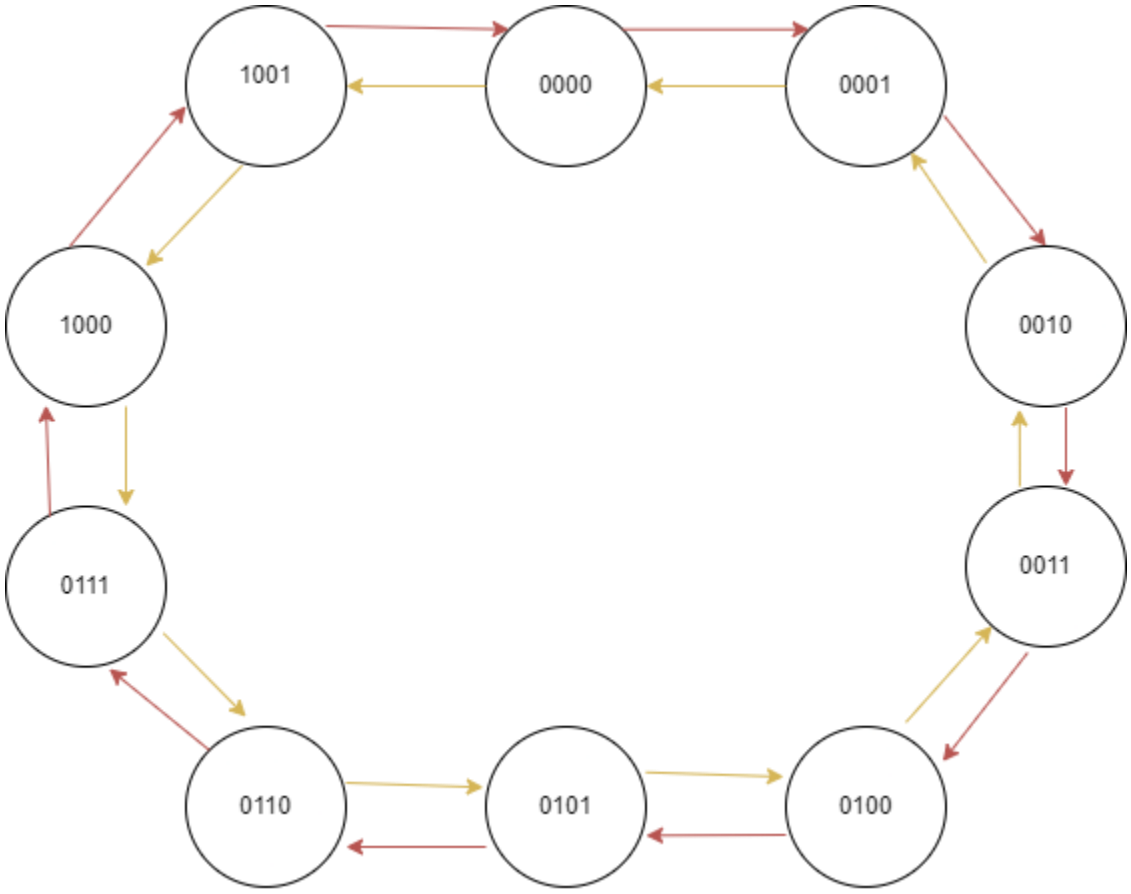
		Q2 Q1 Q0							
		000	001	011	010	110	111	101	100
M Q3	00	X	1	1	X	X	1	1	X
	01	X	1	1	X	X	1	1	X
	11	X	1	1	X	X	1	1	X
	10	X	1	1	X	X	1	1	X
Minimum SOP: 1									

K-map for K0

The moore circuit created from the truth table and k-maps accommodates up to the value of 16 (1111). However, the counter only needs up to the value of 9 (1001) for the right digit and 6 (0110) for the left digit. The pair made use of the reset functionality of the counter to account for this situation which will be explained later. Thus, shown below are the different state diagrams:

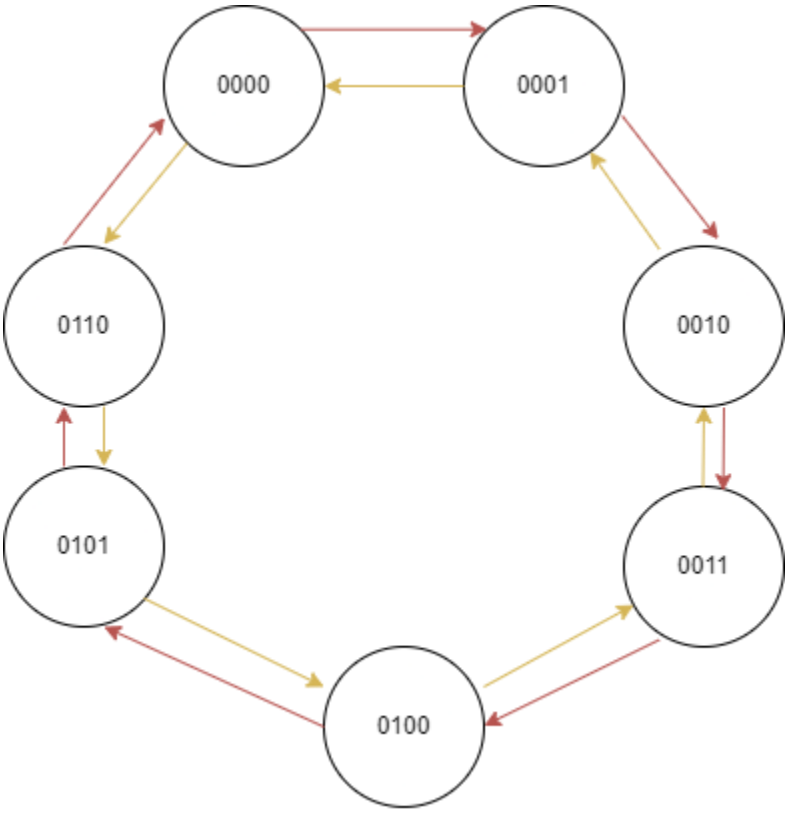
Note: 4-bit format: Q3,Q2,Q1,Q0

a.) Right Digit of Seconds and Minutes (Red:Stopwatch, Yellow: Timer)



State Diagram 1 Right LED of Seconds and Minutes

b.) Left Digit of Seconds and Minutes (Red:Stopwatch, Yellow: Timer)



State Diagram 2 Left LED of Seconds and Minutes

After creating the truth table as well as the state diagrams, the pair proceeded onto creating the circuit in logisim. In total there are 4 different circuits created with this help. Every circuit corresponds to the output of one LED in the general schematic shown in figure 1. The specifics and the schematics of each design is shown below.

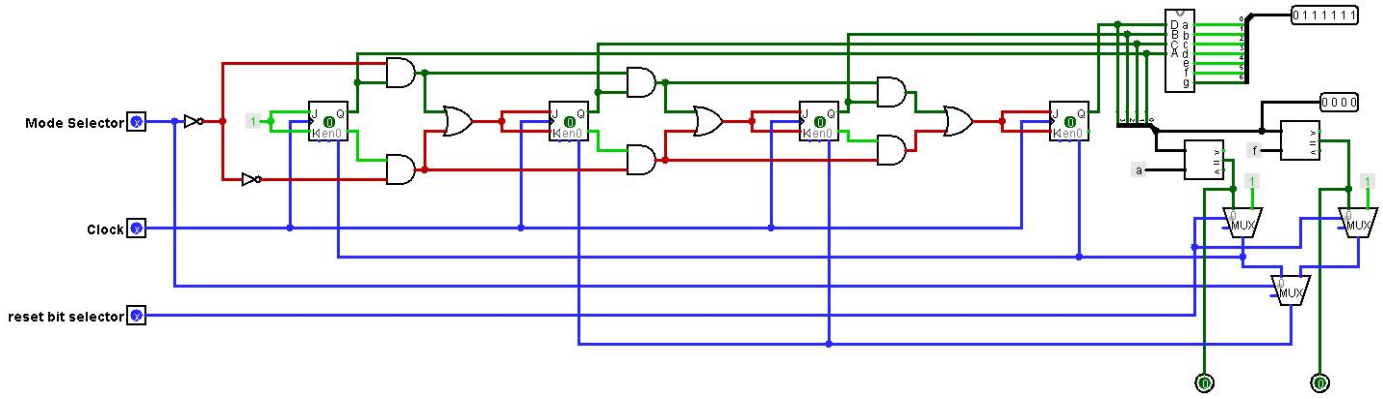


Figure 1.2 Schematics of Right LED (Seconds)

Figure 1.2 is the second place the clock and the button signal will go to. This is the circuitry which determines the value of the rightmost LED of the seconds component (first digit). This works by following the truth table and k-maps determined by the pair. It takes in the input of the clock signal for continuous changing of states (for counting) as well as the mode selector which determines whether it will count up or down. The pair then connected the outputs in a 7 segment display driver for easy conversion of the values into seven outputs for the 7-Segment Display. The pair also needed to connect this to the other LEDs such that when it reaches 9 or 0 (9 for stopwatch, 0 for timer), it will increment or decrement the value of the LED next to it (from 09 to 10 and 10 to 09). To do this the pair took the values created from the JK flip flop and implemented 2 comparators which are used for each mode (stopwatch and timer). The first comparator is used to determine whether the value is equal to 9. When it detects that it is equal to 9 it sends out a signal to the JK flip flops and resets the value so that it goes back to 0. The same concept is used for the timer such that when it detects the value to be 0 it sends out a signal only to the JK flip flops in the middle so that the value becomes 1001 or 9 in decimal. To do this, the pair decided to use multiplexers to divide the reset signal such that when in the mode of stopwatch it resets everything and when in the mode of timer it only resets the two middle flip flops. We also connected the reset bit selector to the first two multiplexers so that when the reset button is pressed, it will automatically reset the value of the flip flops.

To connect the value of the different LEDs together, the pair used a multiplexer to combine the two signals used in the stopwatch/timer and used it as the clock for the next flip flops so that only when it is detected to be 9 or 0 (9 for stopwatch, 0 for timer) will the second set of flip flops work.

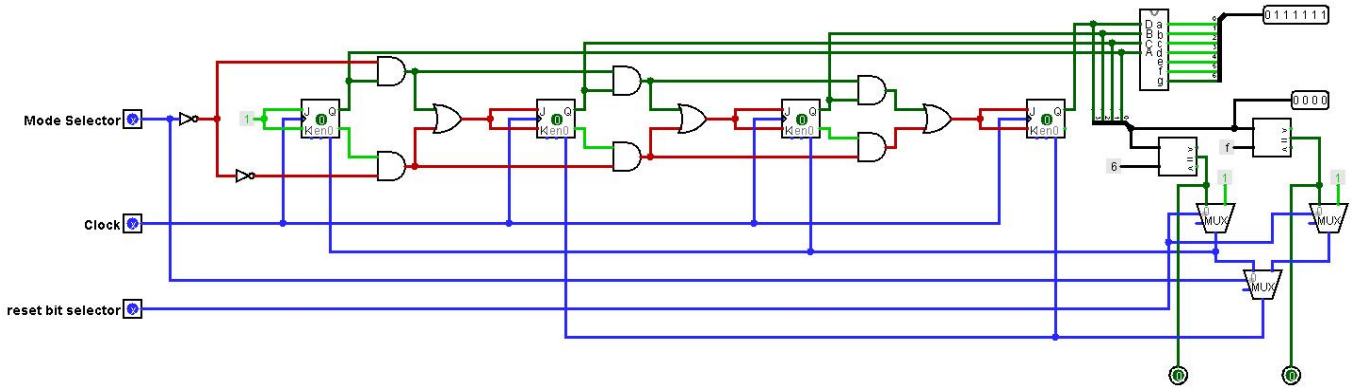


Figure 1.3 Schematics of Left LED (Seconds)

Figure 1.3 works the same way figure 1.2 works but it takes in the output from figure 1.2 as its clock so that it only increment/decrements when the maximum value for the right LED is reached. The detected values however are different since the maximum value for the two LEDs together is 59 so instead of sending out a reset signal when the value is 9, the pair made it so that it works when it detects the value of 5 instead.

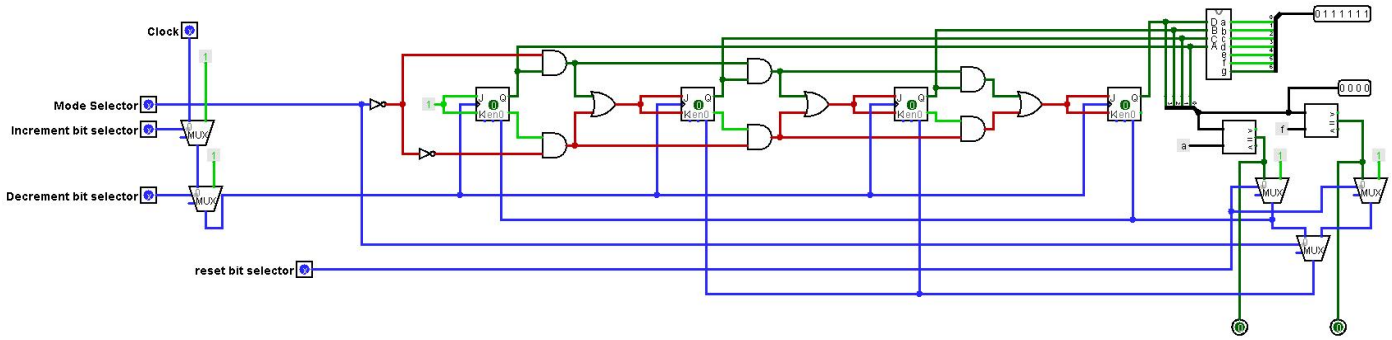


Figure 1.4 Schematics of Right LED (Minutes)

Figure 1.4 works the same as the Right LED of the seconds component but has the added feature of increment and decrement. This works the same way as discussed in the increment/decrement button for the seconds component such that when the button is pressed it sends out a signal of 1 for the clock so that the states of the flip flops changes thus changing the value. This is connected only to this part of the LED so that when the button is pressed, it only changes the values of the minutes LED.

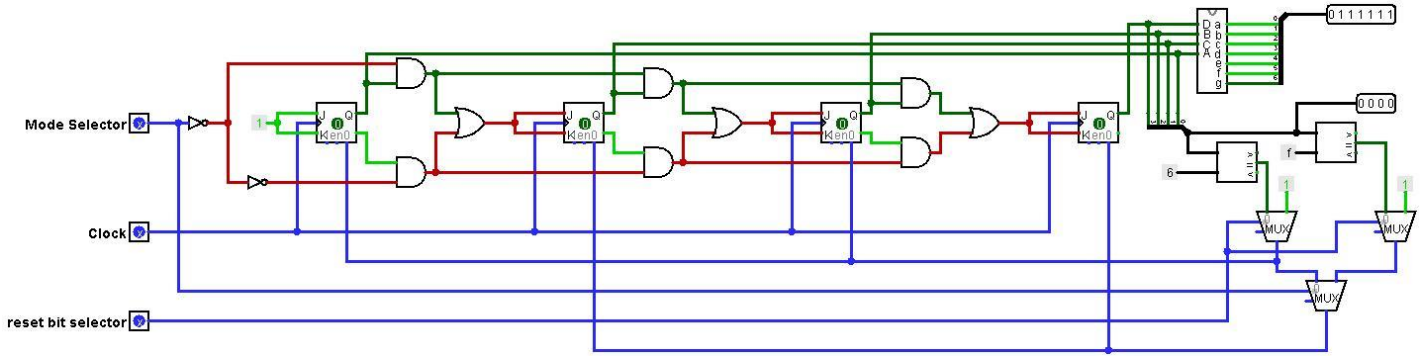
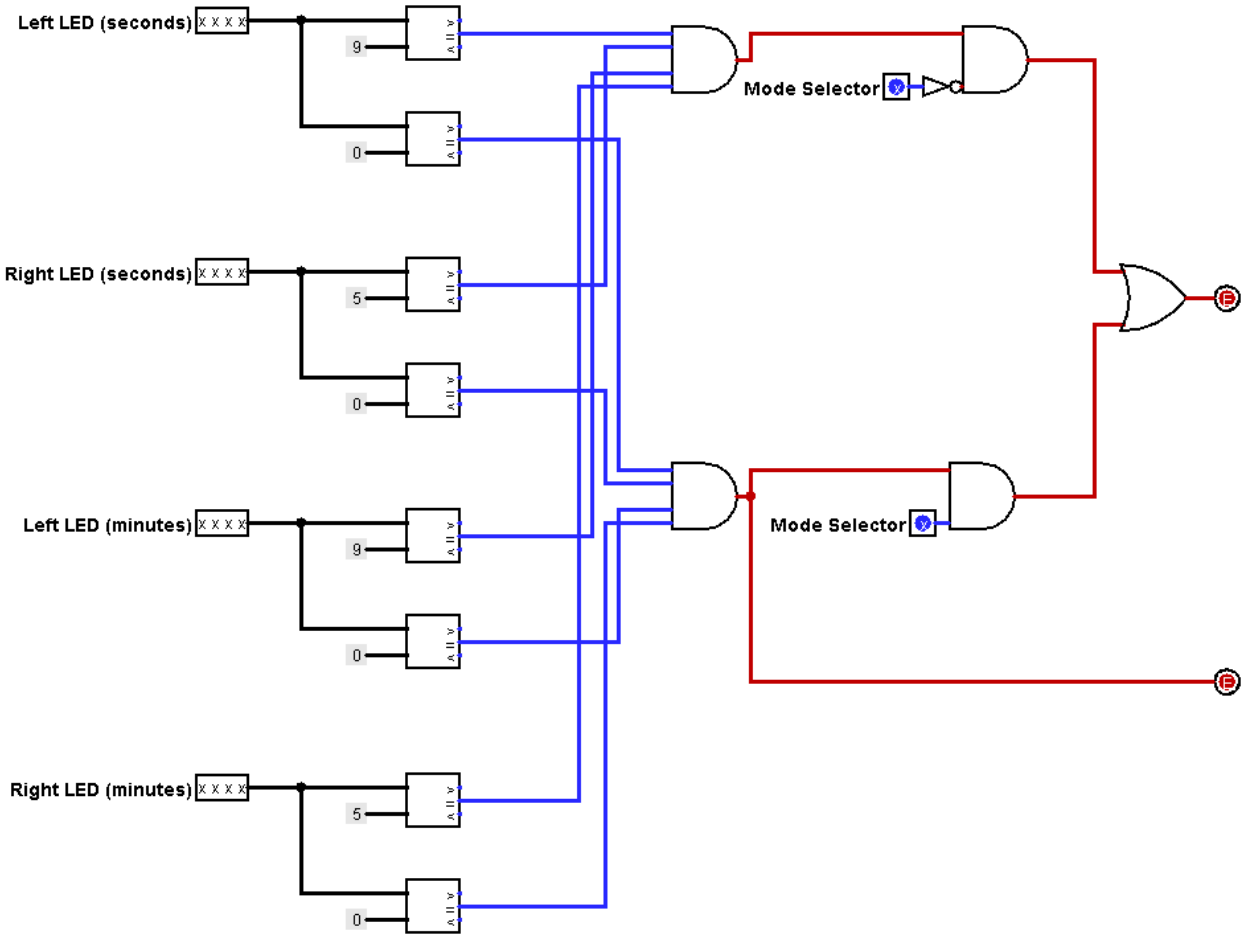


Figure 1.5 Schematics of Left LED (Minutes)

Figure 1.5 works the same way as figure 1.3. The only difference is that it no longer sends out a signal for the next LED since this is the last LED.

The last subcircuit labeled as “Automatic Pause” monitors the counter so that it automatically pauses when the stopwatch reaches 59:59 or the timer reaches 00:00. It also doesn’t allow the decrement button (seconds) to be functional when the timer is at 00:00. This subcircuit is shown below:



The subcircuit takes the 4-bit outputs of the four JK flip-flops for each of the LEDs. The pair used two comparators for each input. The first set of comparators (above) tests if the Left LEDs (seconds and minutes) are equal to 9 and if the Right LEDs (seconds and minutes) are equal to 5. Notice that the equal pins of the first comparators are connected to a 4-input AND gate. Thus, the output of this AND Gate is 1 if the counter is at 59:59. The output of this AND gate is then connected to another AND Gate (2-input) with the mode selector being the other input. The mode selector is first connected to a NOT gate so that the output of the AND gate is 1 if the counter is at 59:59 and 0 as the mode selector. The second set of comparators (below) tests if all the LEDs are equal to zero. These are also connected to a separate 4-input AND gate. Thus, the output of this AND gate would be 1 if the counter is at 00:00. This output is then connected as an input to another AND gate (2-input) with the other input being the mode selector. The output of

this AND gate is 1 if the counter is at 00:00 and if the mode selector is at 1 (timer). Then, the output of this and the output of the first AND gate is connected to an OR gate. The output of the OR gate is then attached to the second multiplexer in the pause connection mentioned earlier (clocks and buttons subcircuit). This would make the counter pause when it is either at 59:59 (with 0 as the mode selector) or when it is at 00:00 (with 1 as the mode selector).

This subcircuit also has another output pin which is connected to the output of the AND gate that checks whether all the LEDs are equal to zero. This serves as the select bit of the 4th multiplexer discussed earlier (clocks and buttons subcircuit). When the counter is at 00:00, the output of the AND gate is 1 and thus the select bit of the 4th multiplexer is also 1. Thus, a constant 0 is the output of this multiplexer making the decrement button (seconds) not functional when the counter is at 00:00.

CONTRIBUTIONS:

General Decisions for the Project: Felix Bueno IV & James Adrian Perez

Creation of Circuitry and Addressing its Issues: Felix Bueno IV & James Adrian Perez

Truth tables and K-map (unannotated): Felix Bueno IV

K-maps (annotated): James Adrian Perez

Documentation: Felix Bueno IV & James Adrian Perez

Documentation Video: Felix Bueno IV & James Adrian Perez

Editing: James Adrian Perez

There were no specific assignments in the creation of the circuits since the pair did most of the circuitry while in a discord call. Both persons contributed ideas and parts in the circuitry to address the issues and problems it had.

Link for Google Drive containing the Documentation Video:

https://drive.google.com/drive/folders/1fBwDwm6WnwdlGkYpIoms6sLOlu3r27V6?usp=sharing