Standard Cells

Open Source Tools

- graywolf
- qrouter
- several FPGA routers

graywolf

- Originates in Academia: TimberWolf
- Simulated annealing
  - Meta heuristic that is useful not only for placement
- Inline syscalls
  - This is just a bad idea

qrouter

- Started in 2011 by Tim Edwards
- Widely used for FPGA
  - Not ready for silicon
- Sequential routing
  - Parallelism not in scope
- Difficult to prove formal correctness
  - Prove that C implementation of Rip-up and Re-route is correct

Productive Tools

- Different tool sets like BonnRoute, Cadence, alliance, etc
- Similar capabilities with respect to silicon
- Just throw man-power at VLSI — what is automation?

State of the Art

- Place components for a large chip
- Route wires roughly along a chessboard for a large chip
- Route detailed tracks and vias for a large chip
- Formal correctness: Rip-up and Re-route
- Formal style: Sequential/Imperative code

Proposed

- Decomposition for a large chip
- Place components and route for small chips in parallel
- Place abstract gates and route recursively
- Formal correctness: Reduction from SMT
- Formal style: Parallel/Functional code

Divide and Conquer

- Academia + Industry:
  - Placement and Routing are different problems
  - All components map to the same problem
- LibreSilicon:
  - Placement and Routing are the same problem
  - Different components map to different problems

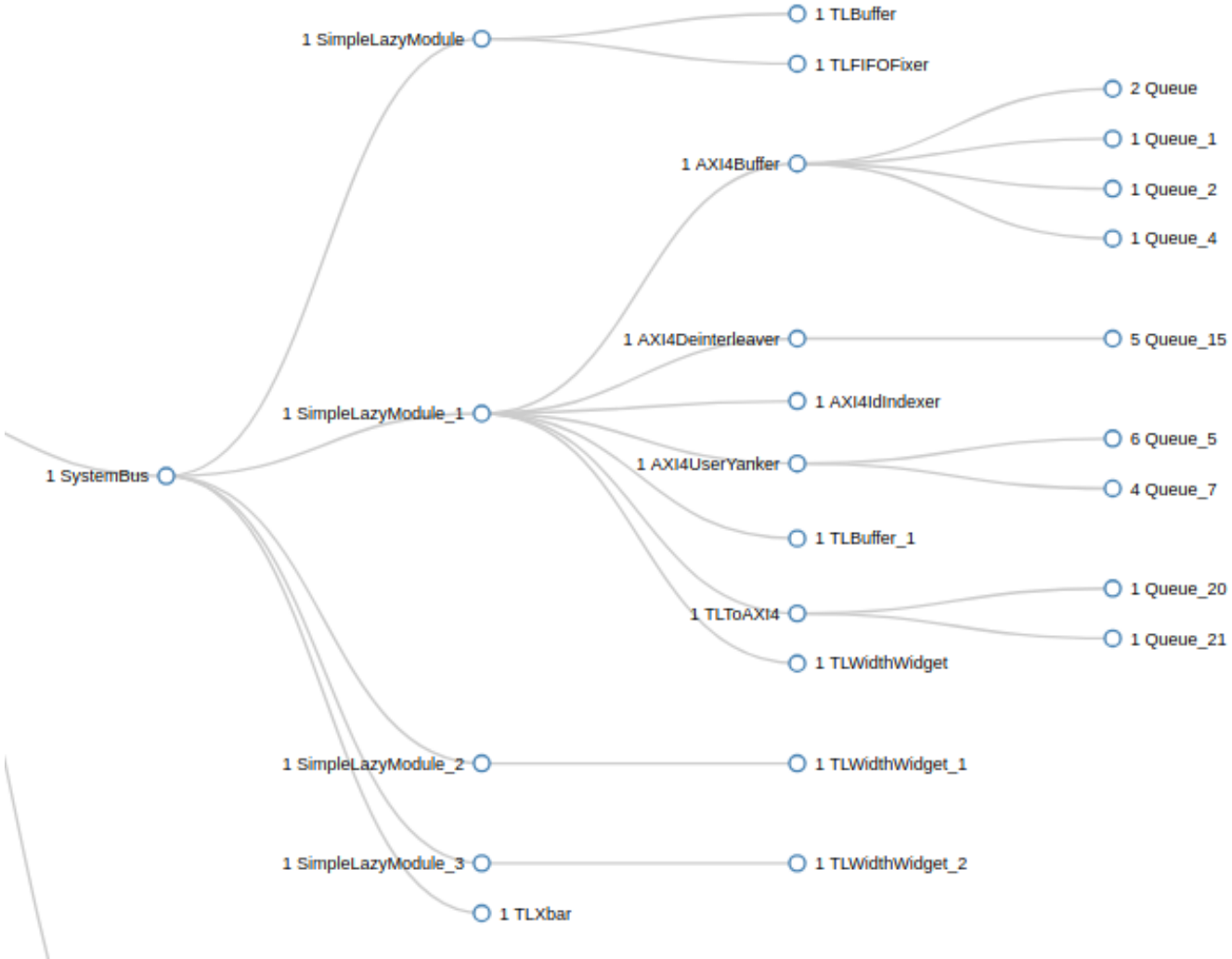
Parallelism

- BonnRoute: concurrency + shared memory model
- qrouter: none
- lsc: map + reduce

Subcell hierarchies

- Explicit subcell hierarchies through high modularization
- Implicit subcell hierarchies through exlining
- Preserve hierarchy in compiler interfaces

High modularization



Exlining

- Proof of concept: picorv

SMT2

- Reduction of a *very* common problem and witty problem to SMT

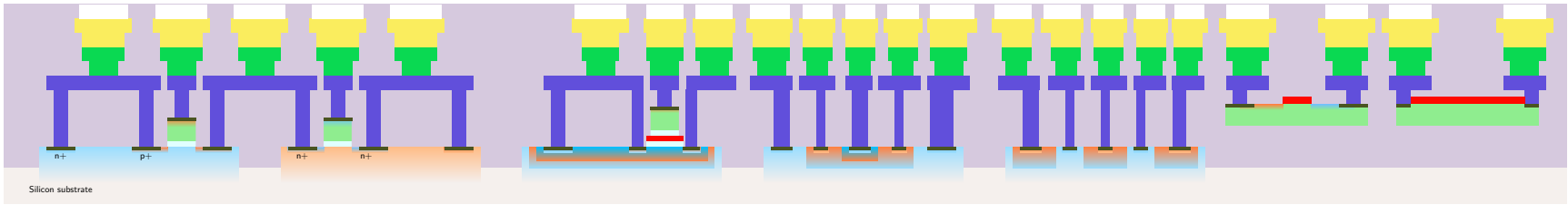
SMT2

- Show routing related problem in integer programming

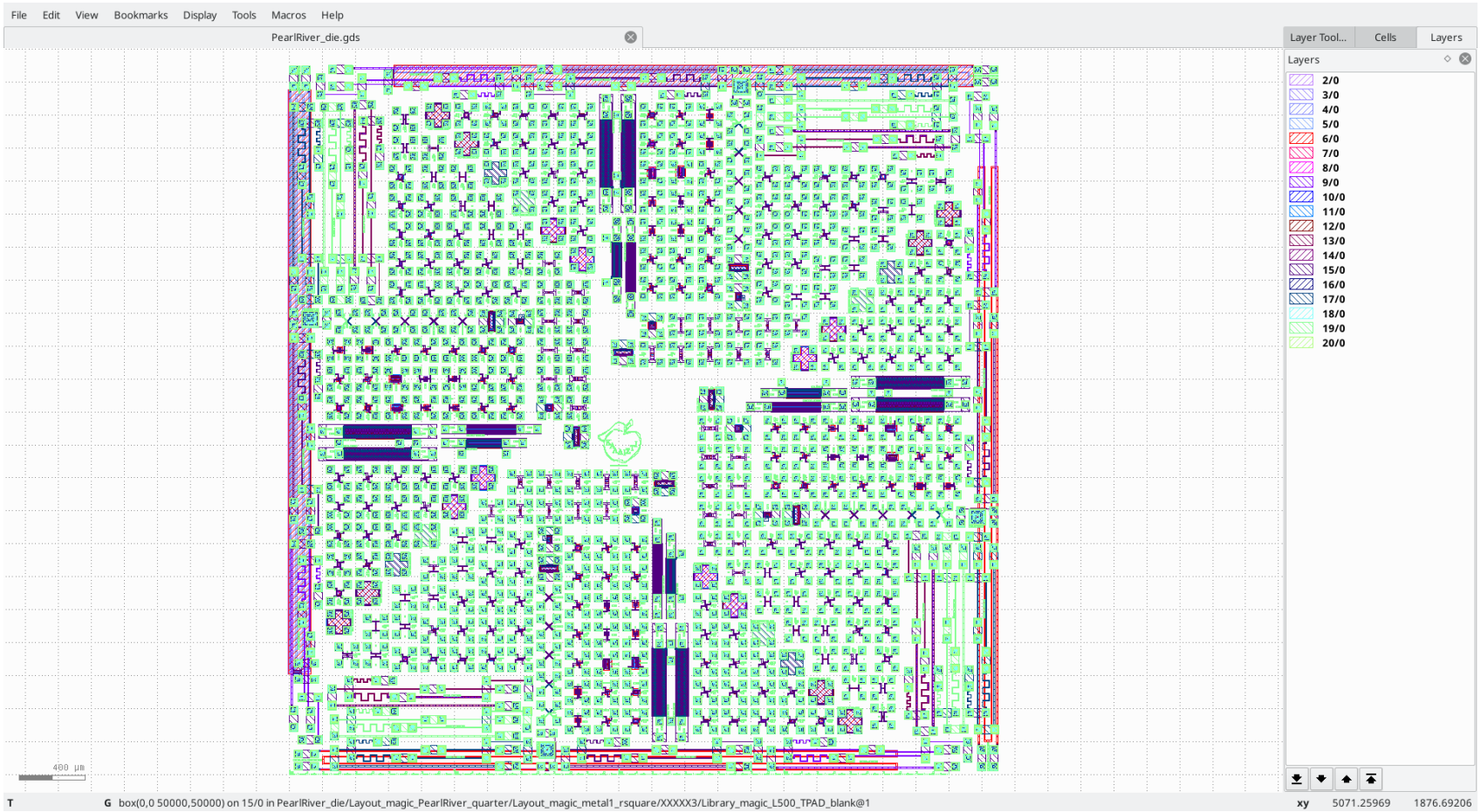
Features

- MOSFETs
- LDMOSFETs (High voltage)
- BJTs
- Zener polysilicon diodes
- SONOS flash cells
- Polysilicon resistors
- Metal caps

Cross section



PearlRiver (珠江芯片一号)

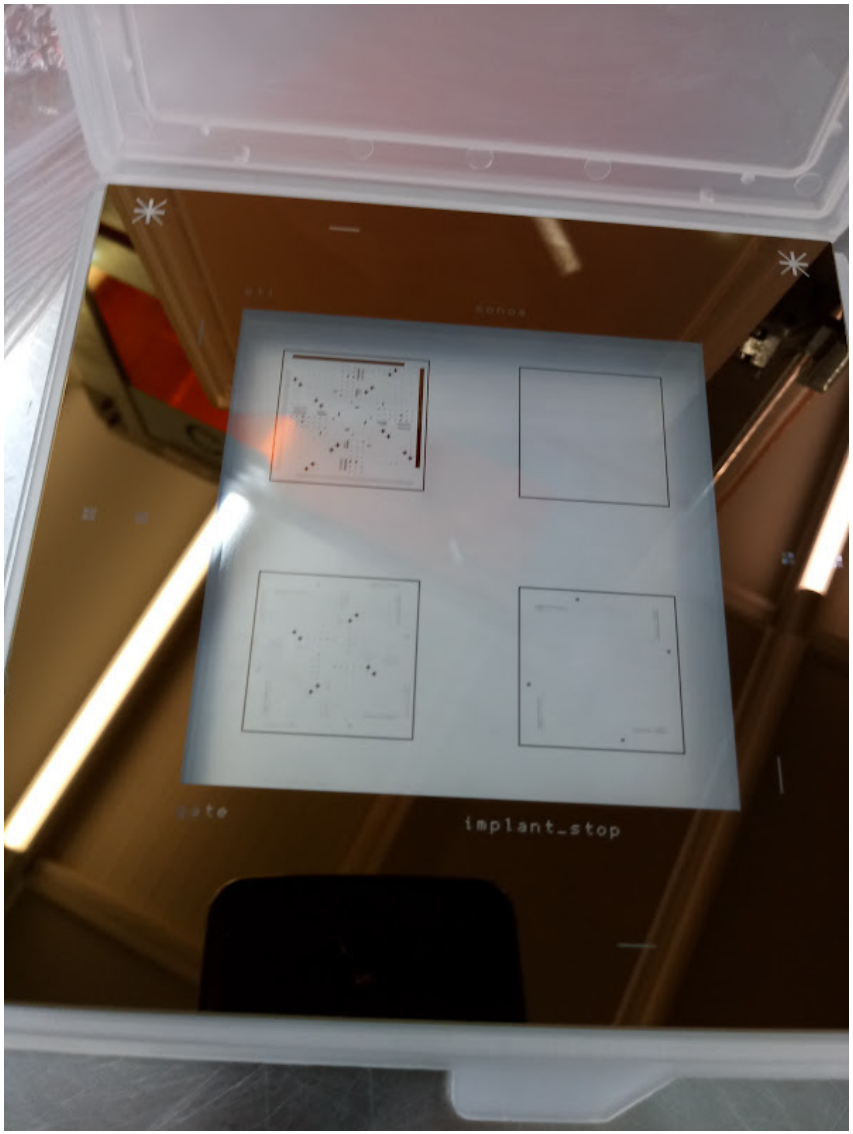


PearlRiver (珠江芯片一号)

Fulfills following functions:

- Debugging
- Calibration of new equipment to LibreSilicon
- Research of new features
- Syncing process features between fabs

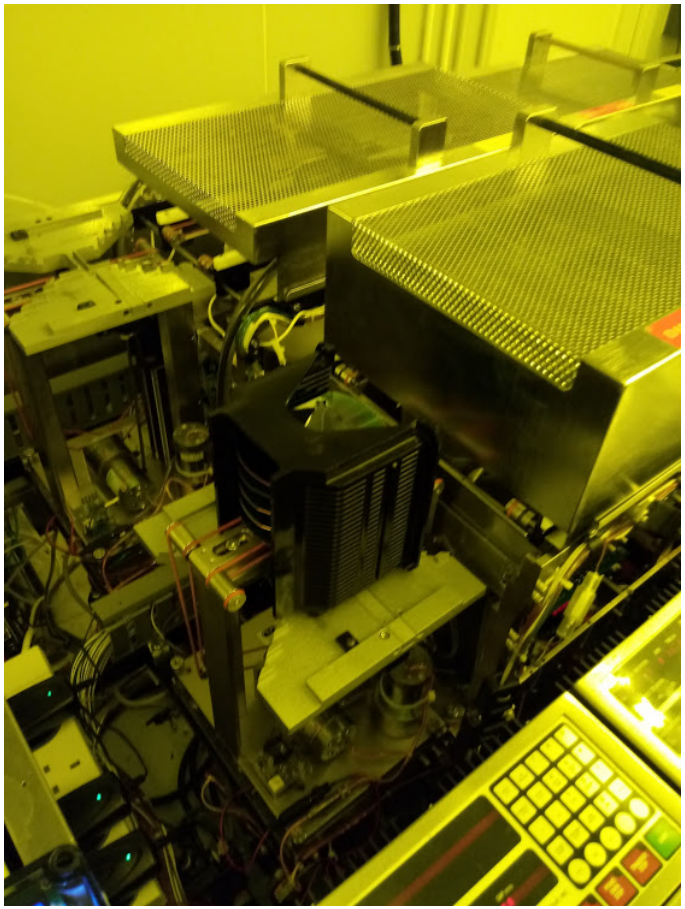
Photomask



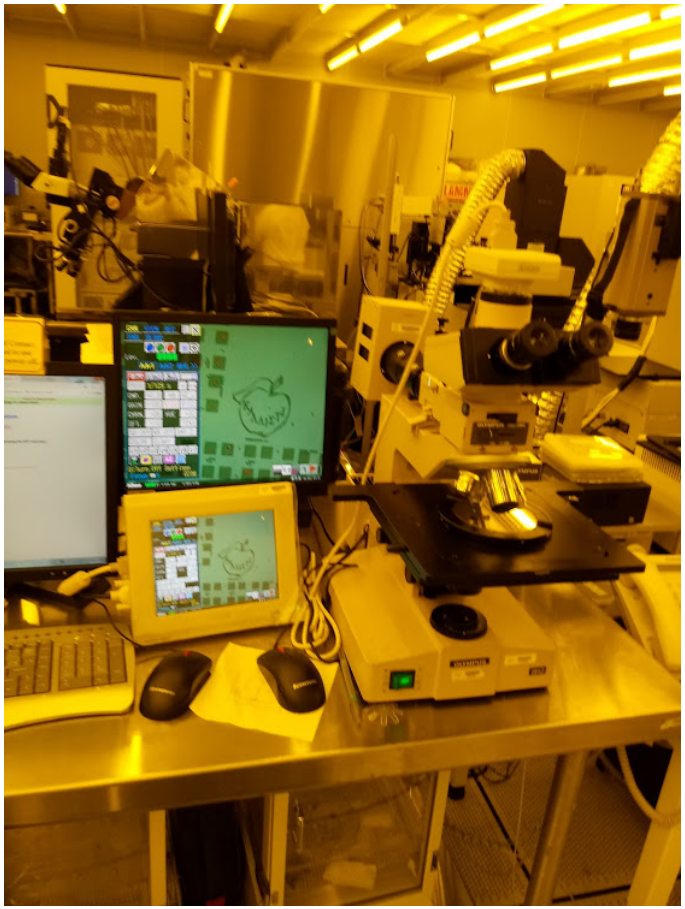
Photomask

- Is stepper/aligner brand specific
- ASML stepper masks contain 4 layers each
- The NFF stepper has a reduction value of 5:1
- A 5 micron gate on the mask is 1 micron on the wafer

Photo resist



After exposure



Alignment