Tools

- graywolf origins in timberwolf

- graywolf simulated annealing

- graywolf inline syscalls

- qrouter purpose and scope

- qrouter sequential routing

- qrouter formal correctness, esp libresilicon tech

Tools

- different tool sets like cadence, alliance, etc

- similar capabilities with respect to silicon

- open source tools are insufficient, except yosys

State of the Art

- Place components for a large chip

- Route wires roughly along a chessboard for a large chip

- Route detailed tracks and vias for a large chip

- Formal correctness: Rip-up and Re-route

- Formal style: Sequential/Imperative code

Proposed

- Decomposition for a large chip

- Place components and route for small chips in parallel

- Place abstract gates and route recursively

- Formal correctness: Reduction from SMT

- Formal style: Parallel/Functional code

Subcell hierarchies

- Explicit subcell hierarchies through high modularization

- Implicit subcell hierarchies through exlining

- Preserve hierarchy in compiler interfaces

High modularization

- Example of a *very* modular chip

Exlining

- Proof of concept: picorv

SMT2

- Reduction of a *very* common problem and witty problem to SMT

SMT2

- Show routing related problem in integer programming