Standard Cells

Open Source Tools

- graywolf origins in timberwolf
- graywolf simulated annealing
- graywolf inline syscalls
- qrouter purpose and scope
- qrouter sequential routing
- qrouter formal correctness, esp libresilicon tech

graywolf

- Originates in Academia: TimberWolf
- Simulated annealing
- Inline syscalls

Productive Tools

- Different tool sets like BonnRoute, Cadence, alliance, etc
- Similar capabilities with respect to silicon
- Just throw man power at large chips - what is automation?

State of the Art

- Place components for a large chip
- Route wires roughly along a chessboard for a large chip
- Route detailed tracks and vias for a large chip
- Formal correctness: Rip-up and Re-route
- Formal style: Sequential/Imperative code

Proposed

- Decomposition for a large chip
- Place components and route for small chips in parallel
- Place abstract gates and route recursively
- Formal correctness: Reduction from SMT
- Formal style: Parallel/Functional code

Divide and Conquer

- Academia + Industry:
  - Placement and Routing are different problems
  - All components map to the same problem
- LibreSilicon:
  - Placement and Routing are the same problem
  - Different components map to different problems

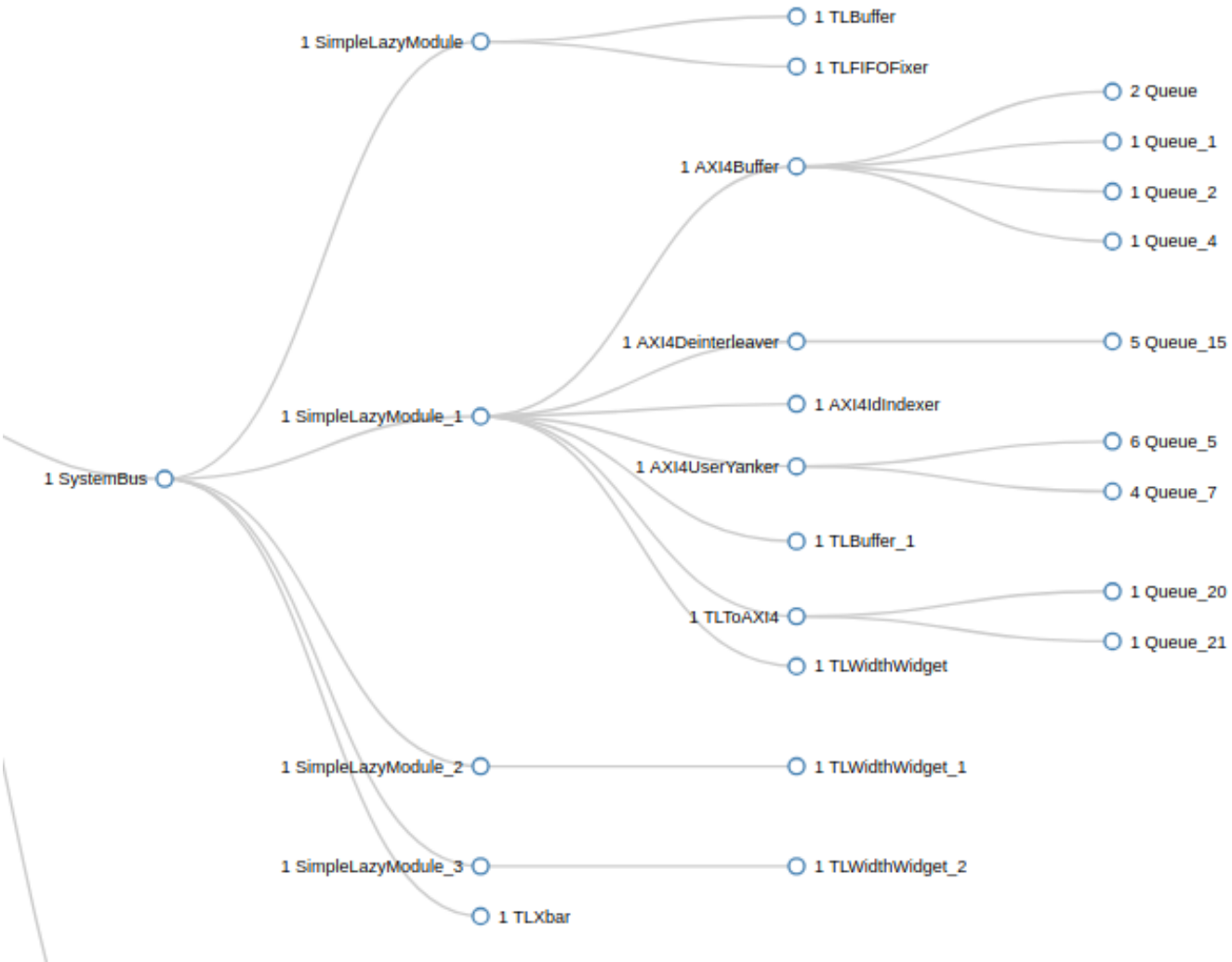
Parallelism

- QRouter: None
- BonnRoute: Concurrency + Shared memory model
- LSC: map + reduce

Subcell hierarchies

- Explicit subcell hierarchies through high modularization
- Implicit subcell hierarchies through exlining
- Preserve hierarchy in compiler interfaces

High modularization



Exlining

- Proof of concept: picorv

SMT2

- Reduction of a *very* common problem and witty problem to SMT

SMT2

- Show routing related problem in integer programming