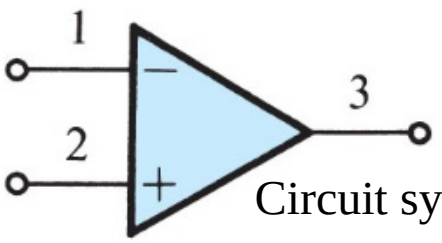
CHAPTER 2

Operational Amplifiers

Lecture 3 (Fall 2019)

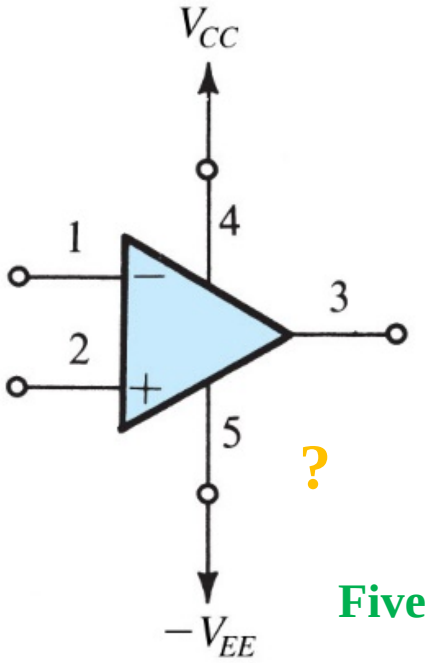
The ideal Op Amp (operational amplifier)



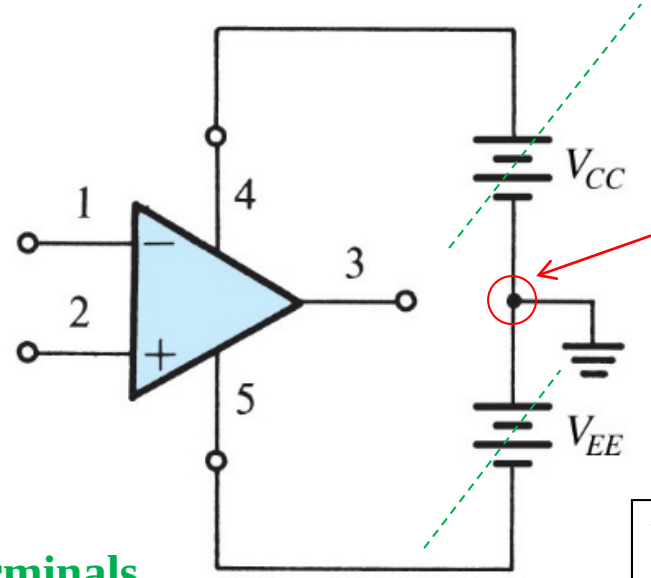
Circuit symbol

Basic components are: electronic vacuum tubes (before 60s) and discrete transistors and resistors (up to now).
The first **IC op amp** was produced in the mid-60s.

One can do almost anything with op amps!!!



(a)



(b)

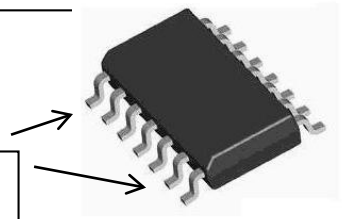
Five terminals

The reference grounding point in op-amp based circuits.

No terminal of the op-amp package is physically connected to ground.

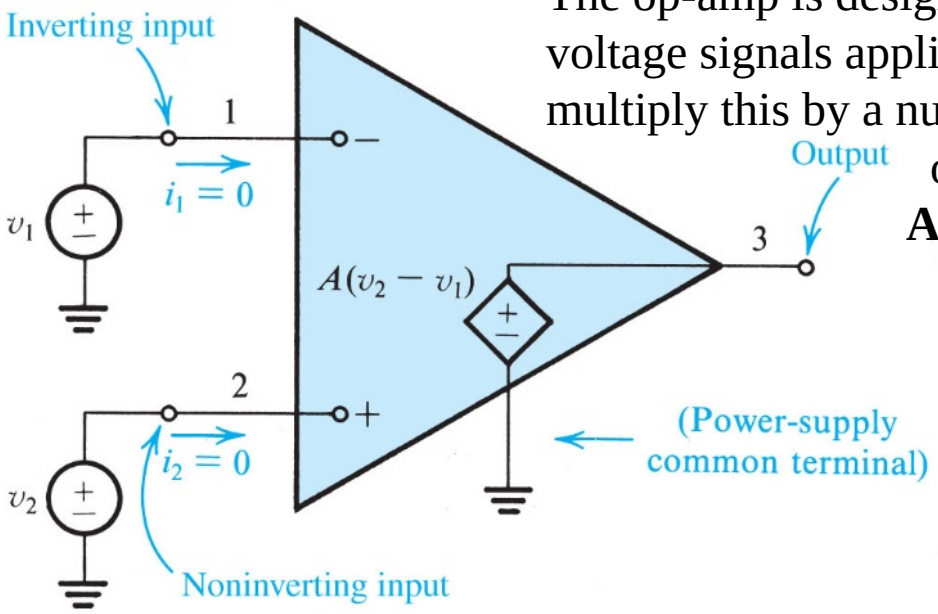
What is the minimum number of terminals required on an IC package containing 4 op amps?

The op amp shown connected to dc power supplies.



Quad op-amp terminals

Function and characteristics of the ideal op-amps.



Equivalent circuit of the ideal op amp.

The op-amp is designed to sense the **difference** between the voltage signals applied at its two input terminals ($v_2 - v_1$), multiply this by a number A, and cause the $A(v_2 - v_1)$ voltage at output terminal 3, $v_3 = A(v_2 - v_1)$.

All $v_{1,2,3}$ are between terminal and ground!

1. Input current = 0 (ideal op-amp).

2. Output voltage is always $v_3 = A(v_2 - v_1)$ independent on the current drawn into a load impedance.

3. If $v_2 = v_1 \Rightarrow v_3 = 0$, an ideal op amp has zero common-mode gain. This is a differential-input, single-ended-output amplifier.

4. "A" is called the **differential gain**. Another name of A is the **open-loop gain**.

Table 2.1 Characteristics of the Ideal Op Amp

1. Infinite input impedance
2. Zero output impedance
3. Zero common-mode gain or, equivalently, infinite common-mode rejection
4. Infinite open-loop gain A ← Op amps are not used along
5. Infinite bandwidth

Differential and common-mode signals

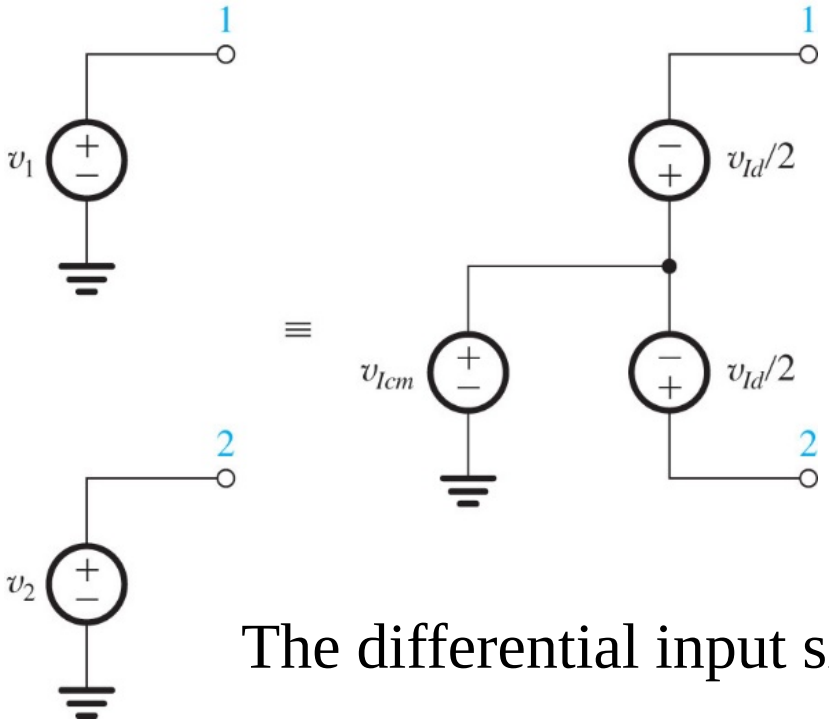


Figure 2.4 Representation of the signal sources v_1 and v_2 in terms of their differential and common-mode components.

The differential input signal is $v_{1d} = (v_2 - v_1)$ (2.1)

The common-mode input signal is $v_{1cm} = 0.5 \times (v_2 + v_1)$ (2.2)

From (2.1) and (2.2):

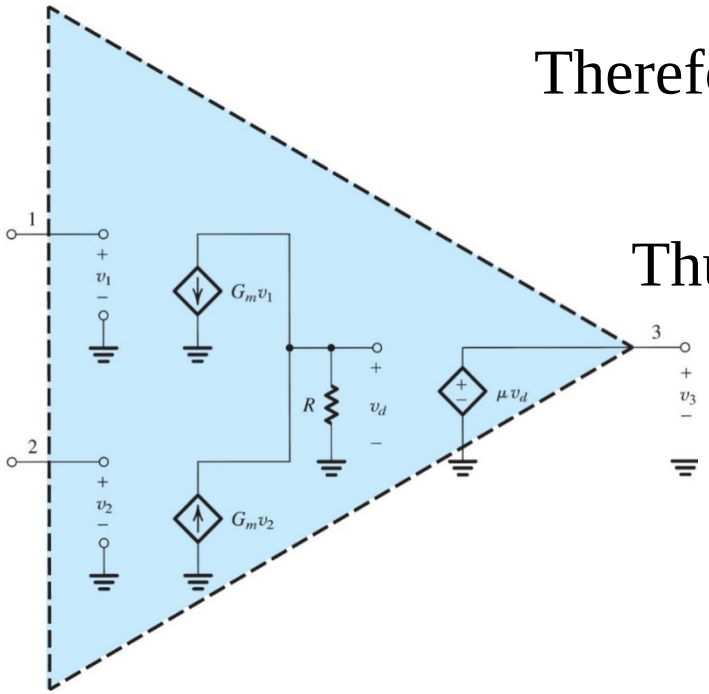
$v_1 = v_{1cm} - v_{1d}/2$ (2.3) and $v_2 = v_{1cm} + v_{1d}/2$ (2.4)

Exercise 2.3. The internal circuit of a particular op amp can be modeled by this circuit. Express v_3 as a function of v_2 and v_1. For the case G_m = 10 mA/V, R = 10 kΩ, and μ = 100, find the value of the open-loop gain A (in decibels).

Solution: From figure: $v_3 = \mu v_d$ and

$$v_d = (G_m v_2 - G_m v_1)R = G_m R\,(v_2 - v_1)$$

Therefore: $v_3 = \mu\, G_m R\,(v_2 - v_1) = A\,(v_2 - v_1)$



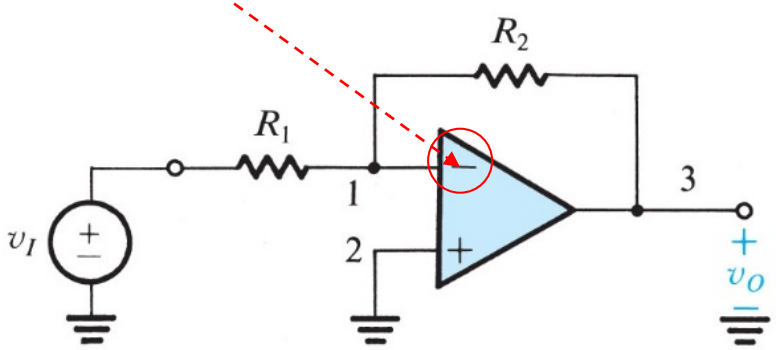
Thus, the open-loop of the op amp is

$$A = \mu\, G_m R = 100 \times 10 \times 10^{-3} \times 10 \times 10^{3}$$

$$= 10^4 \text{ V/V or } 80 \text{ dB}$$

The op amps are not used along.

The inverting closed-loop configuration.



If R_2 is connected between terminals 3 and 1, it applies **negative feedback**.

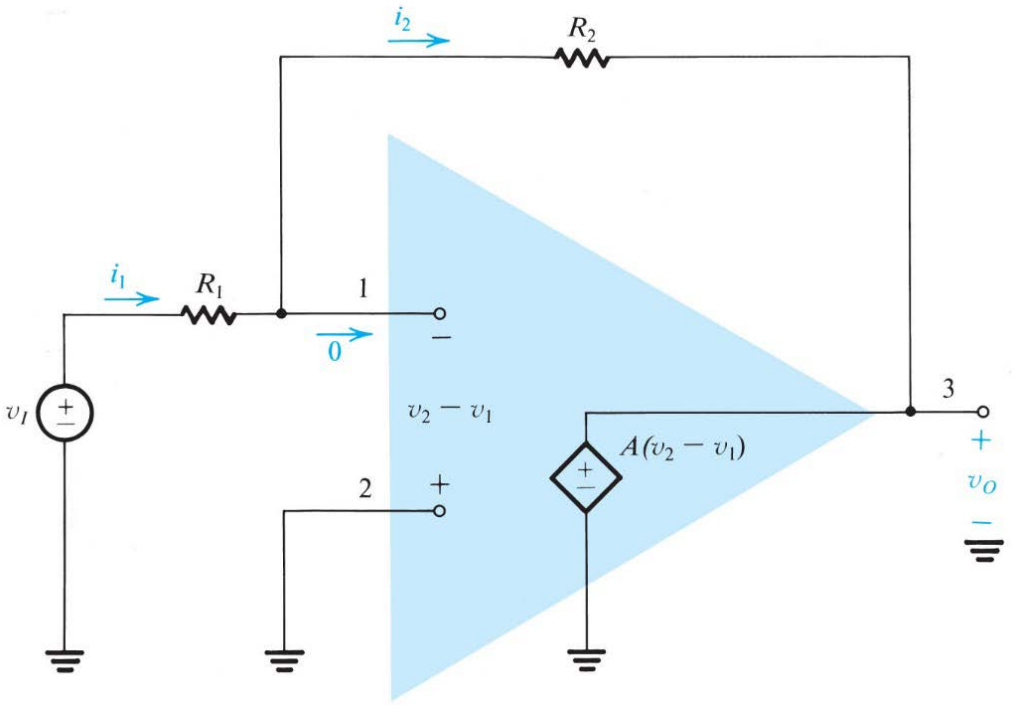
If R_2 is connected between terminals 3 and 2, it applies **positive feedback**.

We say that R_2 *closes the loop* around op amp.

Note that terminal 2 is grounded.

The closed-loop gain G is defined as $G \equiv \frac{v_0}{v_I}$, note $v_I \neq v_1$!!!

The closed-loop gain



The closed-loop gain G is defined as

$$G \equiv \frac{v_0}{v_I}, \text{ note } v_I \neq v_1 !!!$$

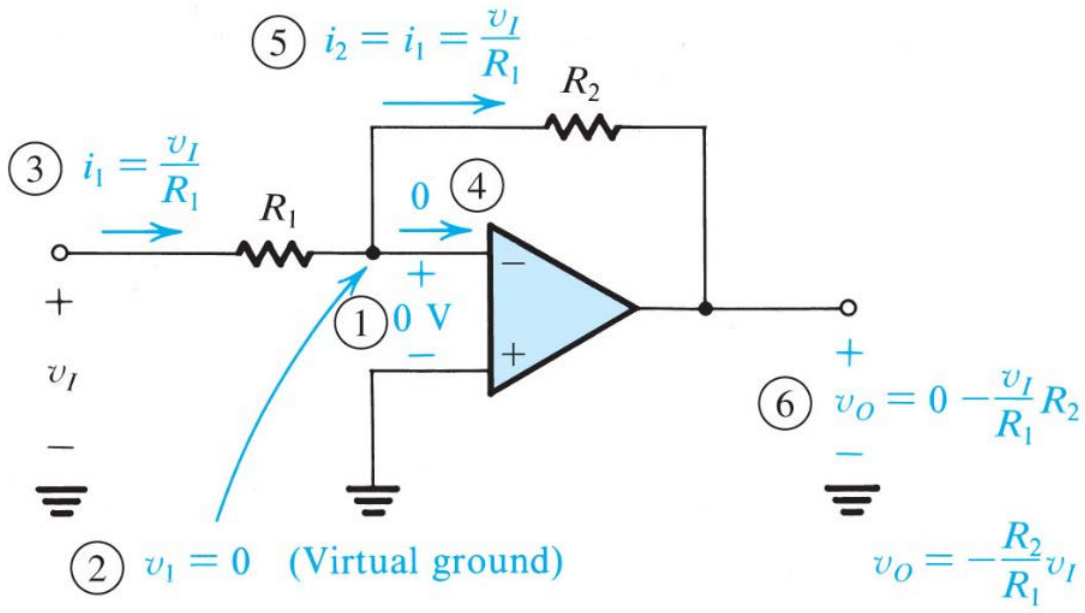
The open-loop gain A is very large (ideally infinite)! But v_0 is finite!

We know: $v_0 = A(v_2 - v_1)$ => $v_2 - v_1 = (v_0 / A) = 0$ *and* $v_2 = v_1$.

Thus we speak of a "**virtual short circuit**" existing between the input terminals!

Terminal 2 is connected to ground; thus $v_2 = 0$ and $v_1 = 0$ (**virtual ground**!)

Analysis of the inverting configuration. The circled numbers indicate the order of the analysis steps.



The closed-loop gain $G \equiv \dfrac{v_0}{v_I} = -\dfrac{R_2}{R_1}$!!! The closed-loop gain is (ideally) independent of the op-amp gain! It is much smaller than A but it is stable and predictable!

G is negative (means **inverting configuration**) => Example: if $(R_2 / R_1) = 10$

If v_I a sine-wave signal of 1 V peak-to-peak, then the v_0 will be a sine wave of 10 V peak-to-peak and phase-shifted 180° with respect to the v_I.

Effect of finite open-loop gain

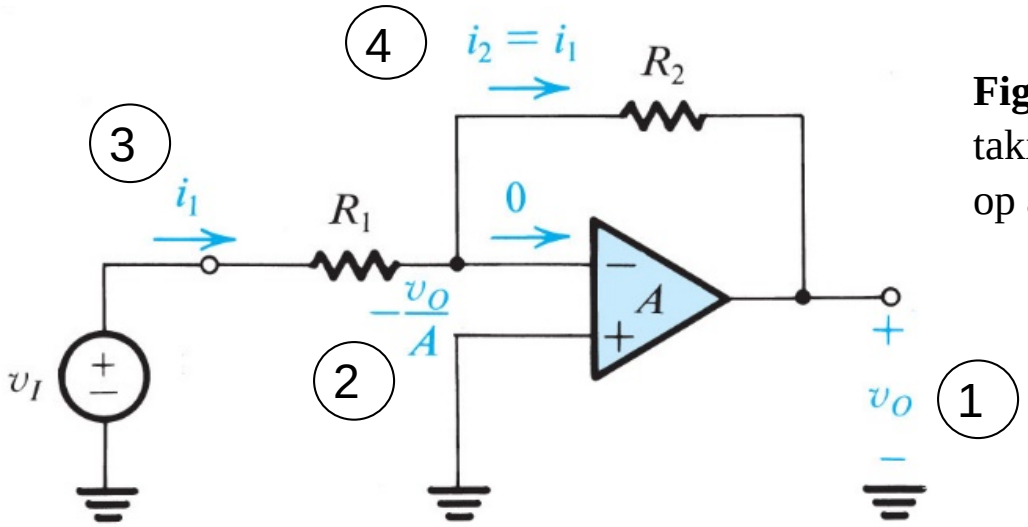


Figure 2.7 Analysis of the inverting configuration taking into account the finite open-loop gain of the op amp.

2 The voltage between two input terminals

3 $$i_1 = \frac{v_I - (-v_0 / A)}{R_1} = \frac{v_I + v_0 / A}{R_1}$$

5 $$i_1 = i_2 = \frac{(-v_0 / A) - v_0}{R_2} \Rightarrow v_0 = -\frac{v_0}{A} - (\frac{v_I + v_0 / A}{R_1})R_2$$

6 $$G \equiv \frac{v_0}{v_I} = -\frac{R_2 / R_1}{1 + (1 + R_2 / R_1)/ A} \qquad (2.5)$$

7 To minimize the dependence of G on the value of A, we should make $1 + \frac{R_2}{R_1} << A$

Read at home Section 2.2.3 (Input and output resistances) and solve yourself Example 2.2

Example 2.2. Assuming the op amp to be ideal, derive an expression for the closed-loop gain.

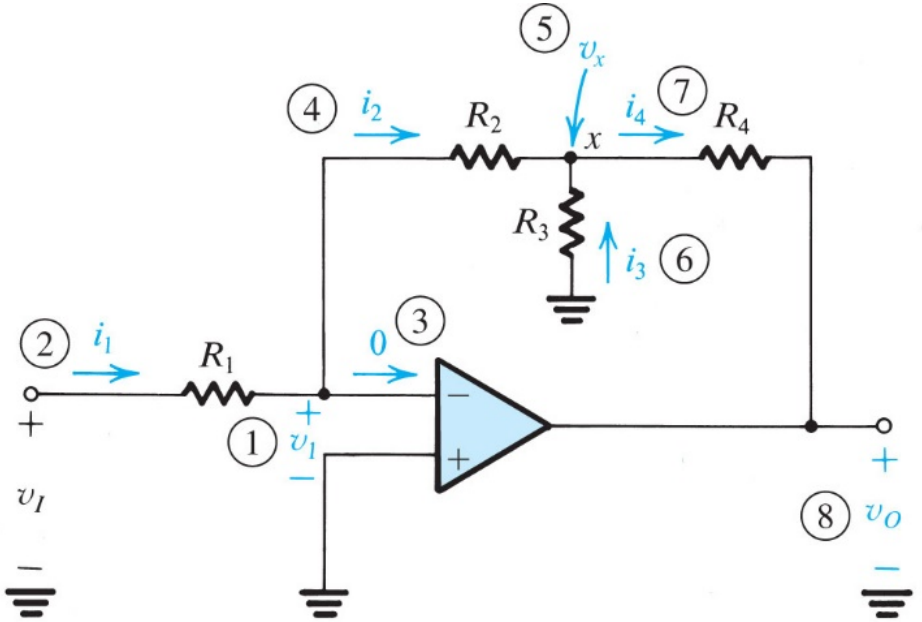


Figure 2.8 Circuit for Example 2.2. The circled numbers indicate the sequence of the steps in the analysis.

$$\frac{v_0}{v_I} = -\frac{R_2}{R_1}\left(1+\frac{R_4}{R_2}+\frac{R_4}{R_3}\right)$$

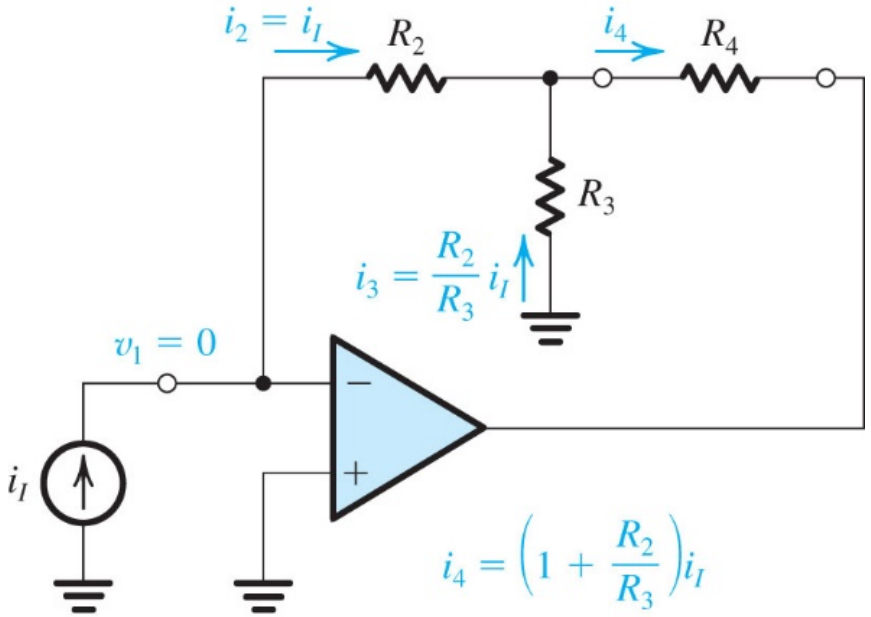


Figure 2.9 A current amplifier based on the circuit of Fig. 2.8. The amplifier delivers its output current to R_4. It has a current gain of $(1+R_2/R_3)$, a zero input resistance, and an infinite output resistance. The load (R_4), however, must be floating (i.e., neither of its two terminals can be connected to ground).

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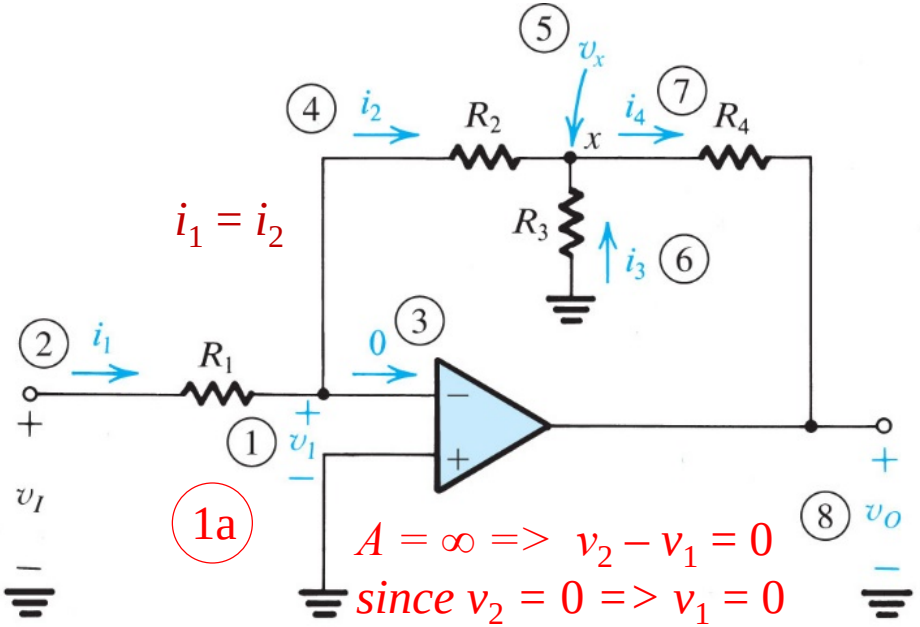

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$$\frac{v_0}{v_I} = -\frac{R_2}{R_1}\left(1 + \frac{R_4}{R_2} + \frac{R_4}{R_3}\right)$$

9 Observe, R_2 and R_3 are in effect in parallel (due to virtual ground).

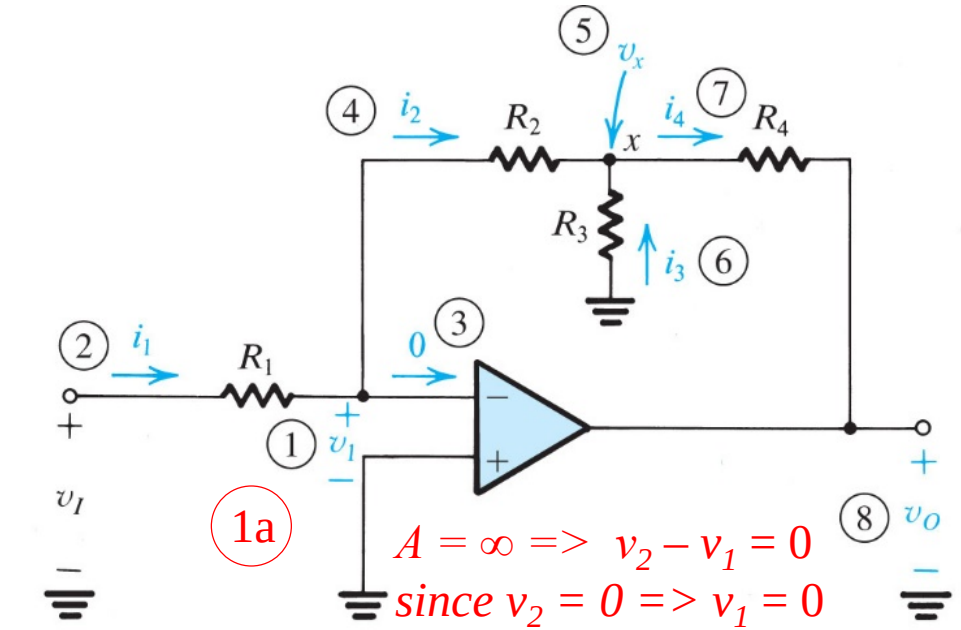
10 Assume $R_2 = k \times R_3$ ($k > 1$). While $i_1 = i_2$, $i_3 = k \times i_1$ and $i_4 = (k + 1) \times i_1$

11 Notice the current through R_4 is independent of the value of R_4.

Thus, a large v_0 can be developed without using a large value of R_4.

The circuit can be used as a current amplifier (next slide).

Example 2.2. Assuming the op amp to be ideal, derive an expression for the closed-loop gain.



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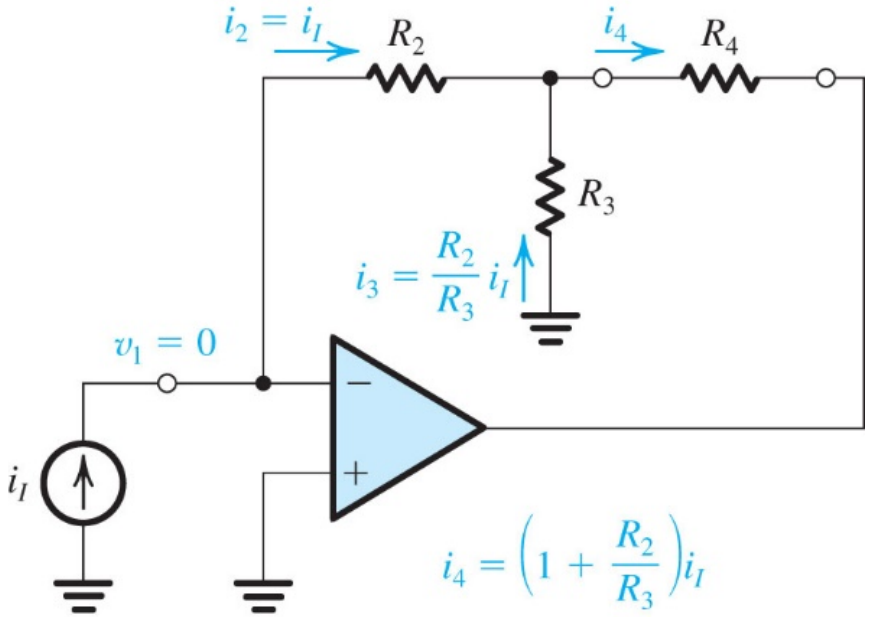

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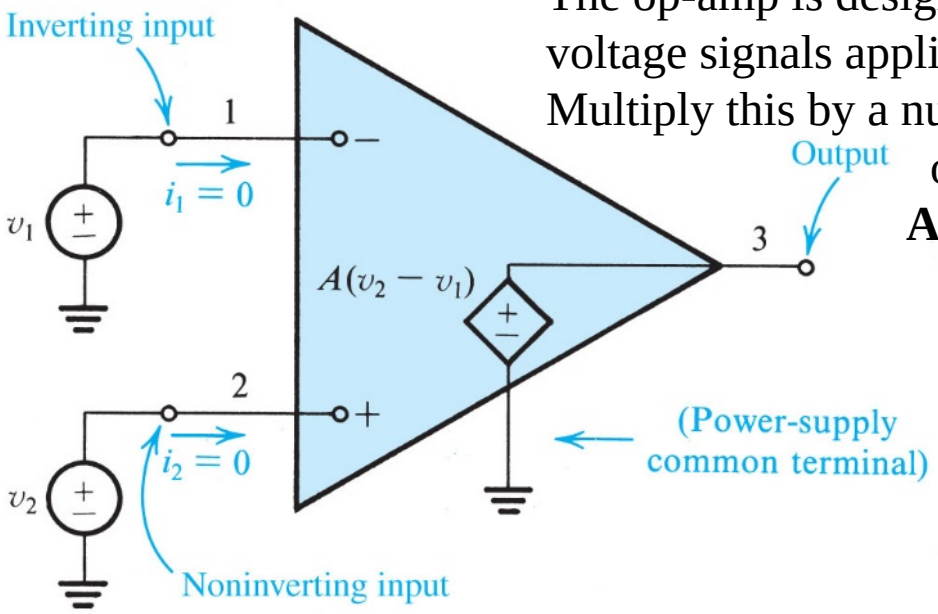

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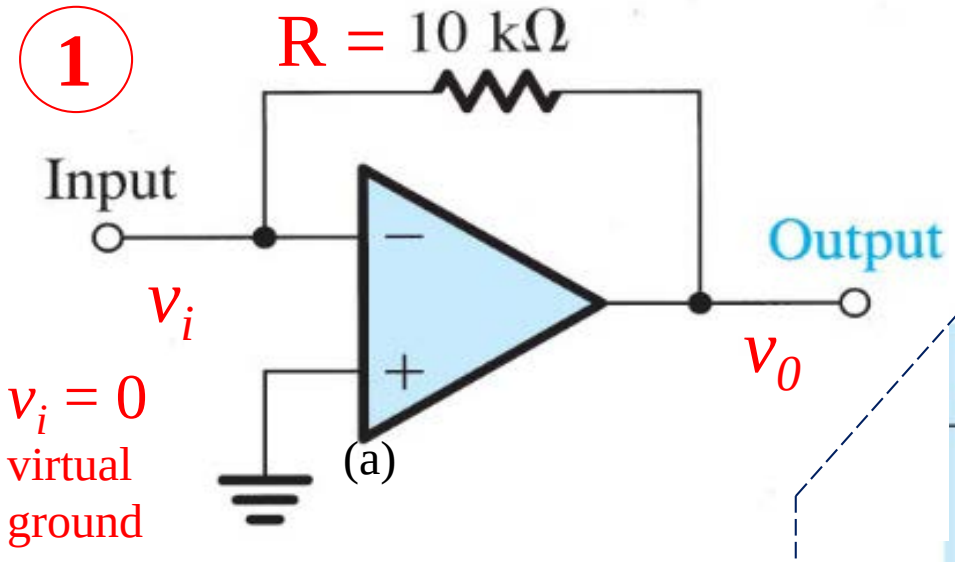
Exercise 2.5. The circuit shown in Fig. (a) can be used to implement a **transresistance** amplifier. Find the value of the input resistance R_i, the transresistance R_m, and the output resistance R_0.

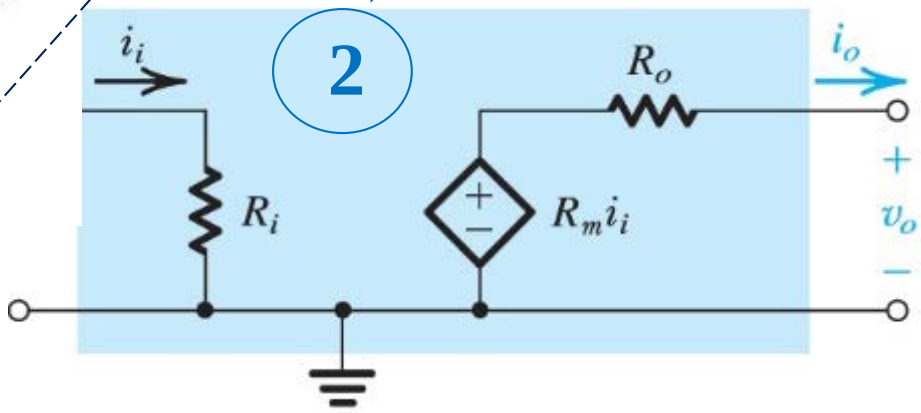


$$R_i = \frac{v_i}{i_i} = \frac{0}{i_i} = 0\,\Omega$$

if $v_i = 0$, i_i must flow through $R = 10\ \text{k}\Omega$

From Table 1.1

Ideal transresistance op amp $R_0 = 0\ \Omega$

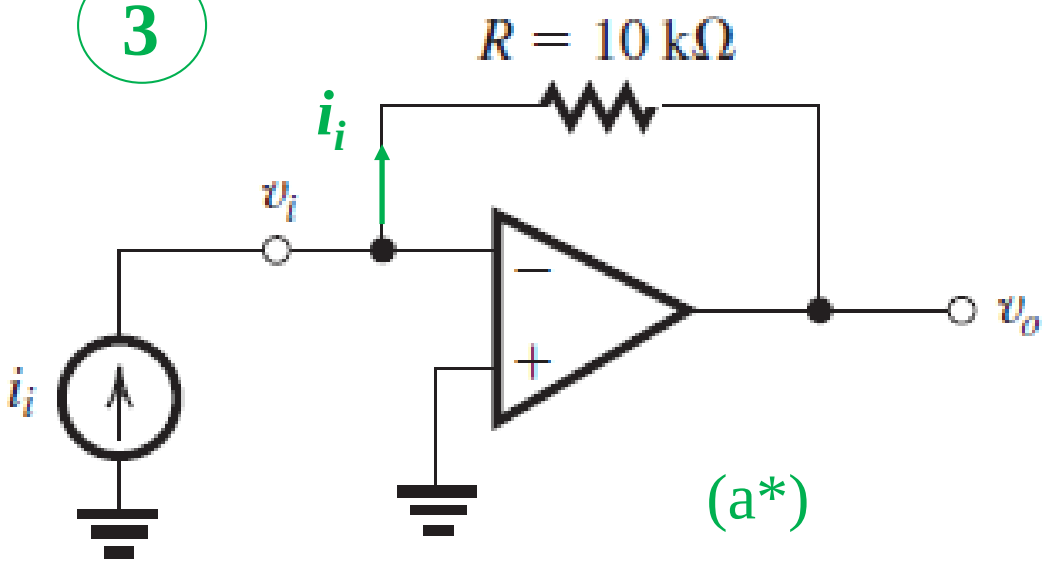


$$i_0 = 0, \text{ thus } v_0 = R_m i_i$$

$$\Rightarrow R_m = v_0 / i_i \quad (1)$$

Exercise 2.5. (continued)

3



(a*)

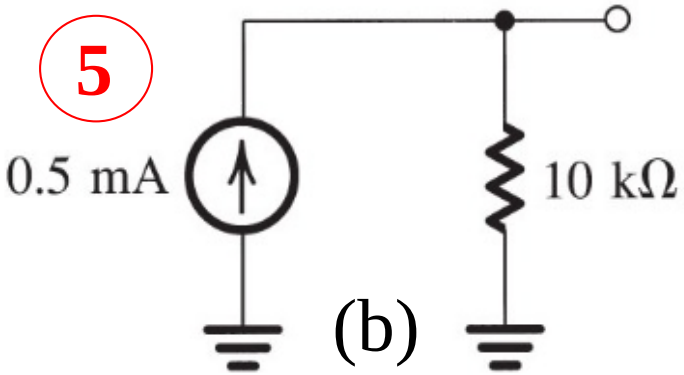
$$\text{from } (a^*)\quad i_i = \frac{v_i - v_0}{R} = \frac{0 - v_0}{R} \Rightarrow v_0 = -i_i R \quad (2)$$

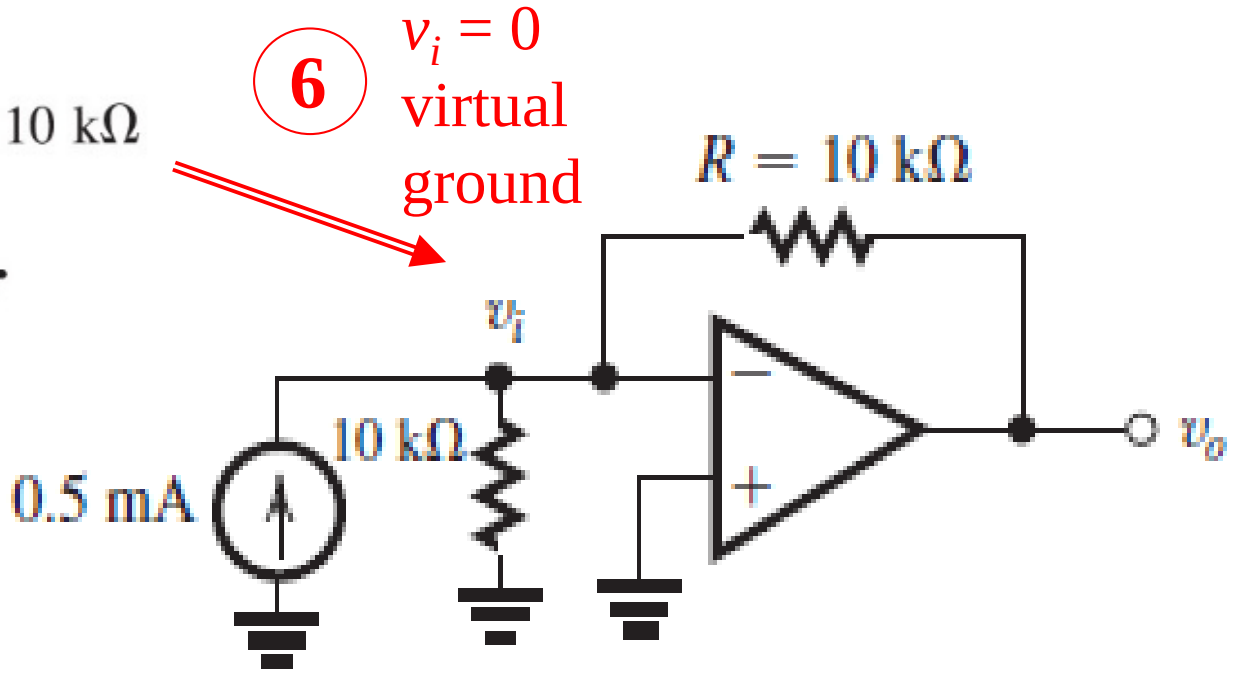
4

$$(2) \rightarrow (1) \Rightarrow R_m = \frac{-R \times i_i}{i_i} = -R = -10\,k\Omega$$

Exercise 2.5 (continued)

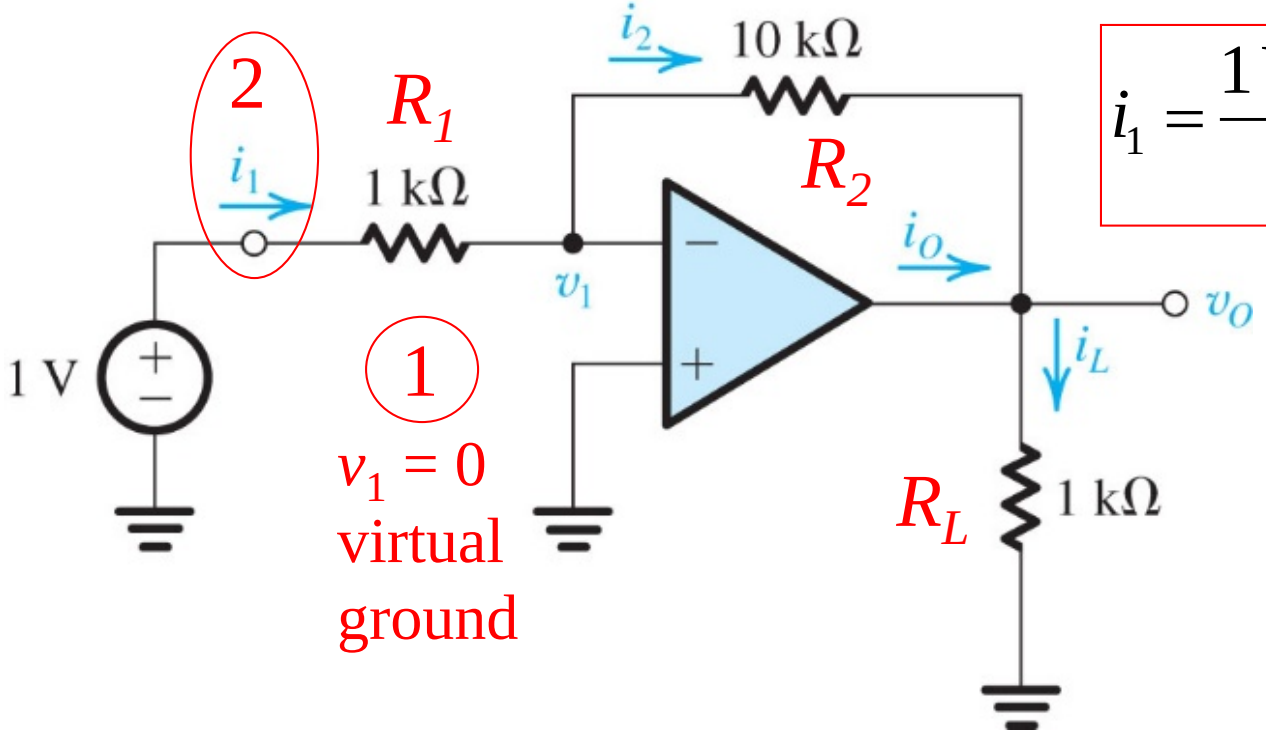
If the signal source shown in Fig. (b) is connected to the input of the transresistance amplifier, find the amplifier output voltage.





$$\text{Thus, } v_0 = v_i - Ri_i = 0 - 10\times10^3\times0.5\times10^{-3} = -5\,V$$

Exercise 2.6. For this circuit determine the values of $v_1, i_1, i_2, v_0, i_L, and\ i_0$. Also determine the voltage gain v_0 / v_I, current gain i_L / i_I, and power gain P_0 / P_I.



$$i_1 = \frac{1\,\mathrm{V} - v_1}{R_1} = \frac{1-0}{1\,k\Omega} = 1\,mA$$

Assuming an ideal op amp, $i_2 = i_1 = 1$ mA

Exercise 2.6. (Continued)

$$v_O = v_1 - i_2 R_2 = 0 - 1\ \text{mA} \times 10\ \text{k}\Omega = -10\ \text{V}$$

$$i_L = \frac{v_o}{R_L} = \frac{-10\ \text{V}}{1\ \text{k}\Omega} = -10\ \text{mA}$$

$$i_O = i_L - i_2 = -10\ \text{mA} - 1\ \text{mA} = -11\ \text{mA}$$

$$\text{Voltage gain} = \frac{v_O}{1\ \text{V}} = \frac{-10\ \text{V}}{1\ \text{V}} = -10\ \text{V/V}$$

20 dB

$$\text{Current gain} = \frac{i_L}{i_1} = \frac{-10\ \text{mA}}{1\ \text{mA}} = -10\ \text{A/A}$$

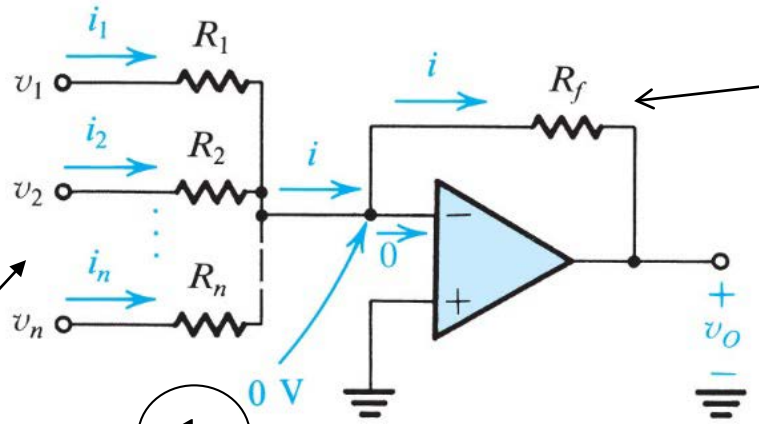
20 dB

Power gain

$$\frac{P_L}{P_i} = \frac{-10(-10\ \text{mA})}{1\ \text{V} \times 1\ \text{mA}} = 100\ \text{W/W or } 20\ \text{dB}$$

A weighted summer.

There are *n* input signals each applied to a corresponding resistor, which is connected to the inverting terminal of the op amp.



negative feedback

1

2 Ohm's law : $i_k = \dfrac{v_k}{R_k}$ (1)

3 KCL : $i = \sum_{k=1}^{n} i_k$ (2)

4 Ohm's law

$$v_0 = 0 - iR_f \quad (3)$$

Combine (1), (2), and (3):

5

$$v_0 = -\sum_{k=1}^{n} \frac{R_f}{R_k} v_k \quad (2.7)$$

$$v_O = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \cdots + \frac{R_f}{R_n}v_n\right)$$

The output voltage is a weighted sum of the input signals (**weighted amplifier**).

At home derive the formula (2.8) for the circuit in Fig. 2.11 yourself.

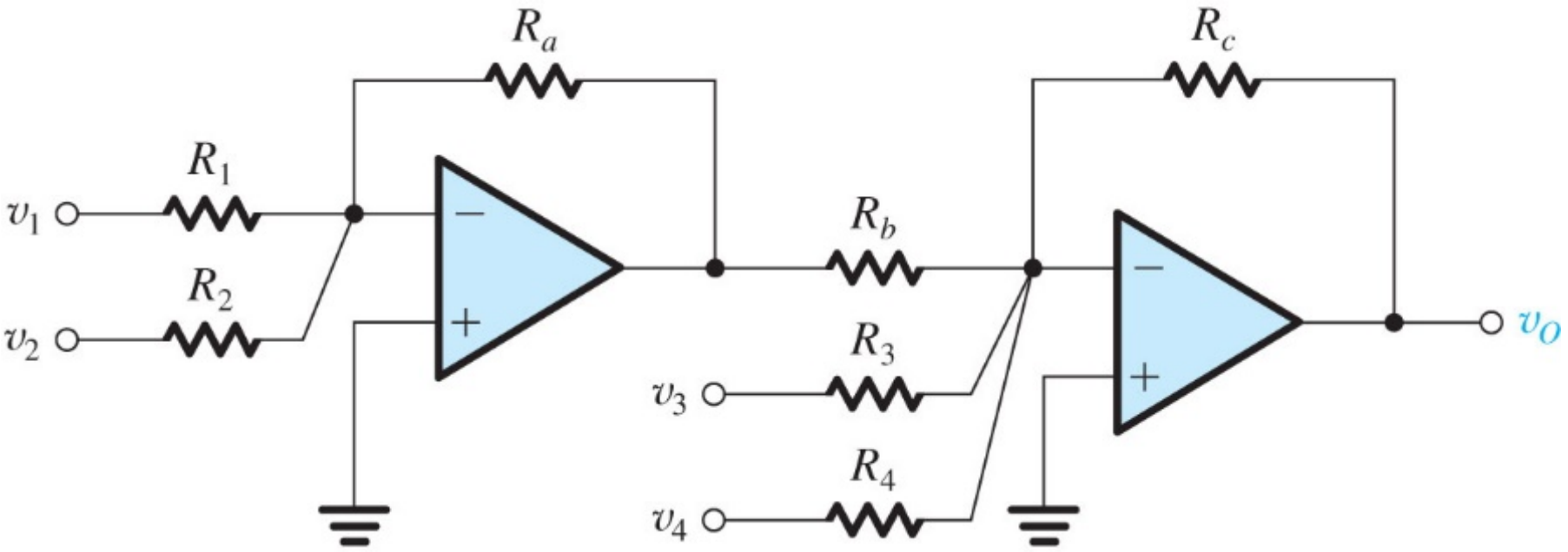
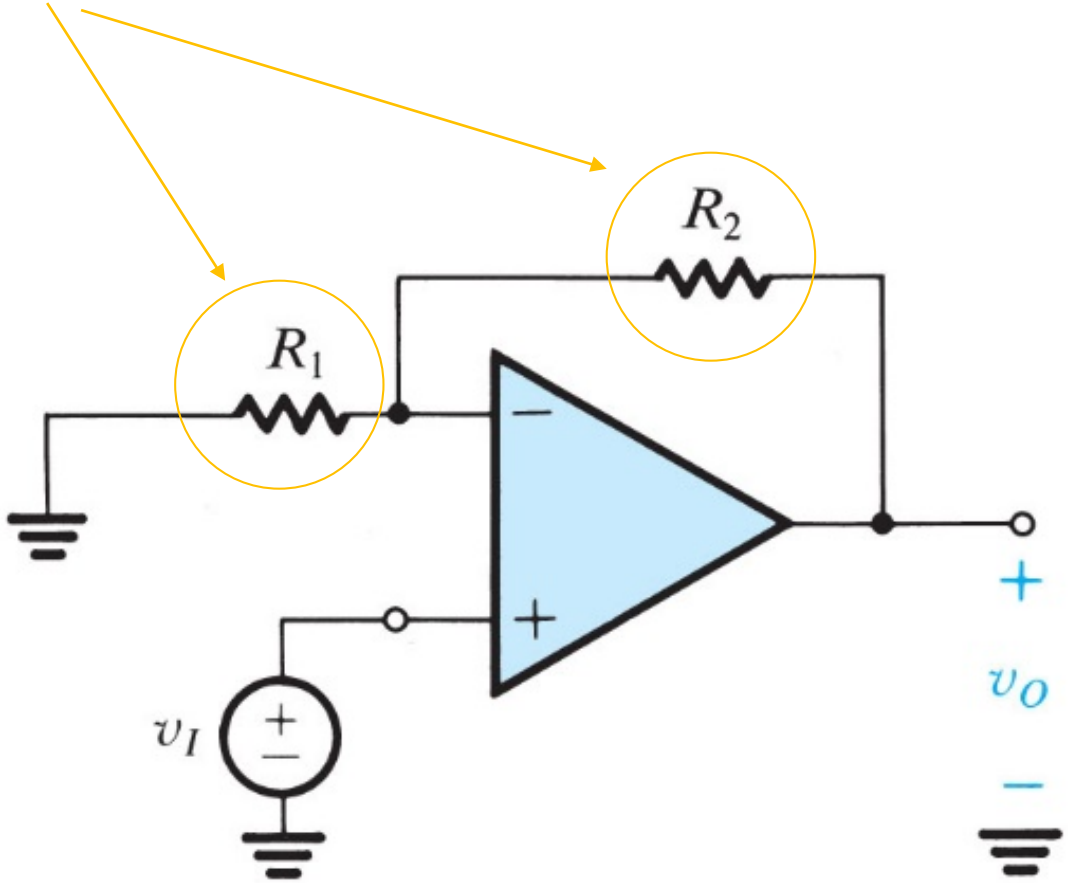


Figure 2.11 A weighted summer capable of implementing summing coefficients of both signs.

The noninverting configuration.

This **negative feedback** has the name **degenerative feedback**



The noninverting configuration (cont.)

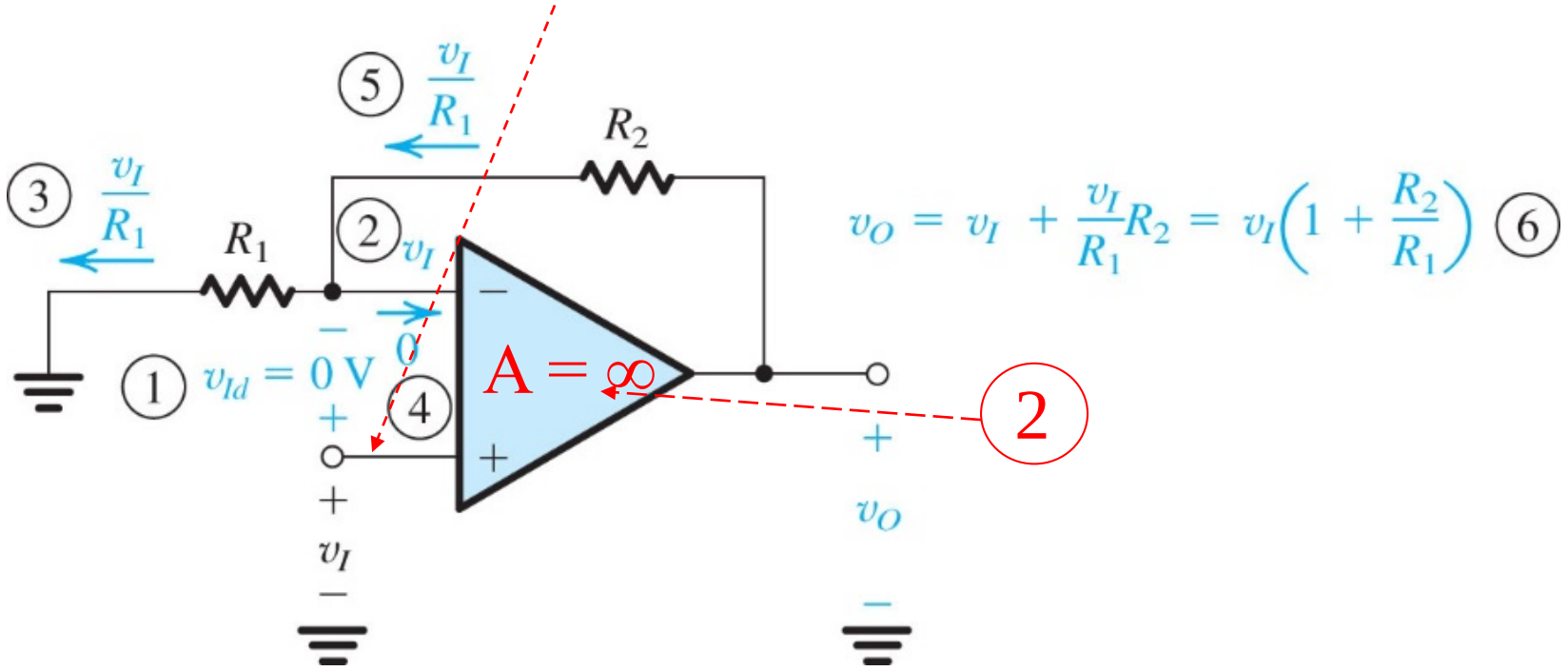
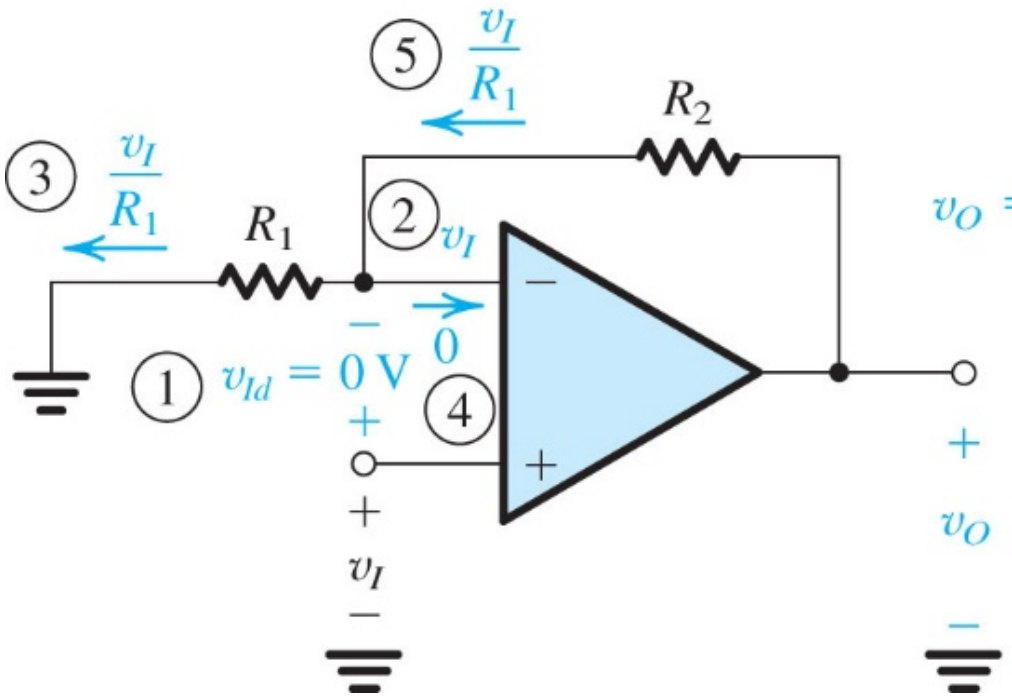


Figure 2.13 Analysis of the noninverting circuit. The sequence of the steps in the analysis is indicated by the circled numbers. **Assume that the op-amp is ideal!**

1 Because $A = \infty$, the difference input signal is $v_{Id} = \frac{v_0}{A} = 0$

The noninverting configuration.

Input impedance of op-amp $Z_{in} = \infty$, by definition.



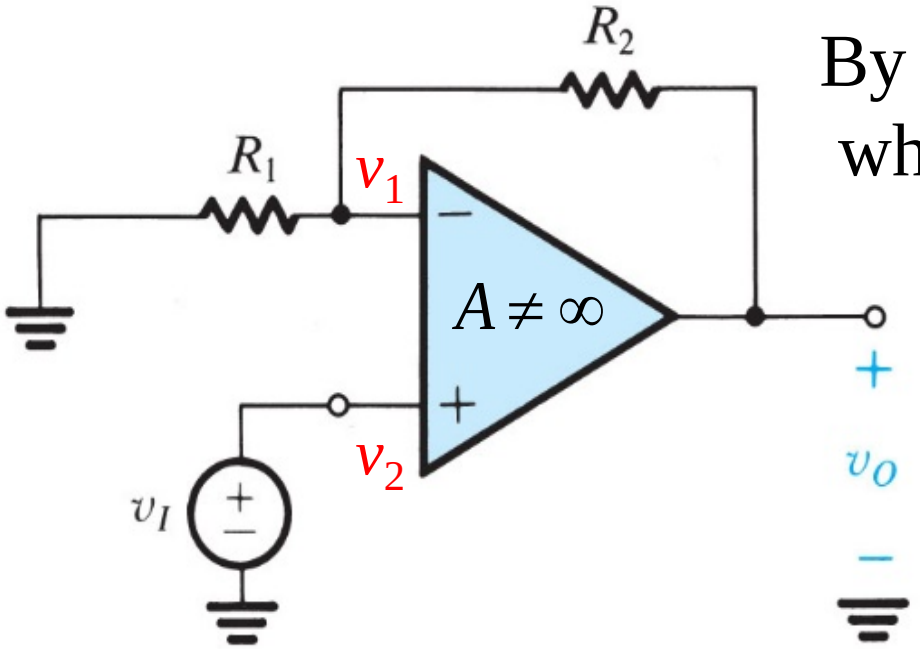
$$v_O = v_I + \frac{v_I}{R_1}R_2 = v_I\left(1 + \frac{R_2}{R_1}\right) \quad (6)$$

The output voltage is the sum of voltages across R_1 and R_2 .

$$\frac{v_0}{v_I} = 1 + \frac{R_2}{R_1}$$

$$\text{Closed-loop gain is } A_v = 1 + \frac{R_{2-\textit{feedback resistor}}}{R_1}$$

Effect of finite open-loop gain, $A \neq \infty$, *but* $Z_{in} = \infty$!!!



By definition: $v_0 = A(v_2 - v_1)$, (1)
where $v_2 = v_I$ (2) and

$$v_1 = v_0 \frac{R_1}{R_2 + R_1} \quad (3)$$

$$\text{Closed-loop gain } G \equiv \frac{v_0}{v_I} \quad (4)$$

Substitute (1), (2), and (3) into (4) =>

$$G = \frac{A\left(v_I - v_0 \dfrac{R_1}{R_1 + R_2}\right)}{v_I} = A\left(1 - \frac{v_0}{v_I}\frac{R_1}{R_1 + R_2}\right)$$

$$= A - AG\frac{R_1}{R_1 + R_2} = \frac{AR_1 + AR_2 - AGR_1}{R_1 + R_2}$$

Effect of finite open-loop gain (cont.)

Rearrange, $G(R_1 + R_2 + AR_1) = A(R_1 + R_2) \Rightarrow G = \dfrac{A(R_1 + R_2)}{(R_1 + R_2 + AR_1)}$

Let's divide nominator and denominator by AR_1 for convenience:

$$G = \frac{A(R_1 + R_2)}{(R_1 + R_2 + AR_1)} = \frac{1 + \dfrac{R_2}{R_1}}{\dfrac{R_1 + R_2}{AR_1} + 1} = \frac{1 + R_2 / R_1}{1 + \dfrac{1 + R_2 / R_1}{A}} \quad (2.11)$$

Summary: G is always positive and ≥ 1

G = 1 => voltage follower

Output resistance is 0, as for inverting amplifier

Effect of finite open-loop gain (cont.)

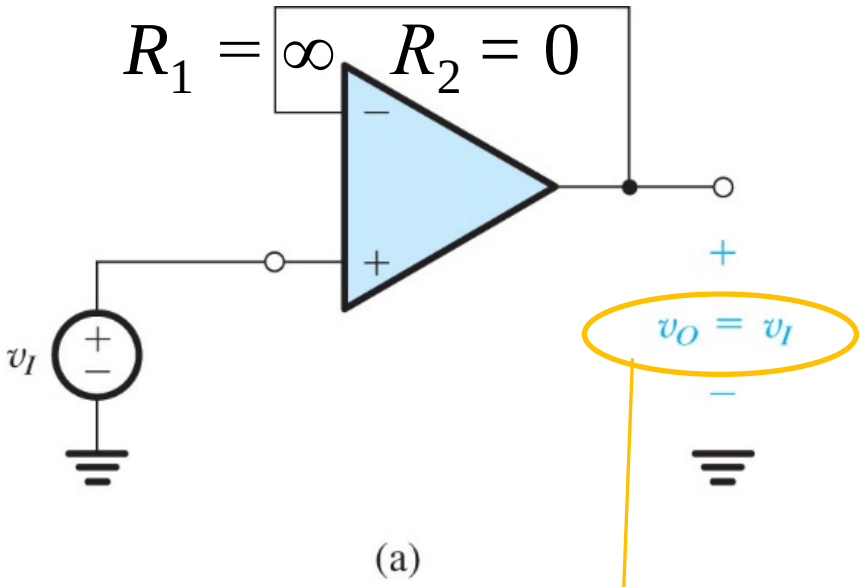
$$G \Rightarrow \text{reduces to the ideal value } 1+\frac{R_2}{R_1}$$

$$\text{for } A=\infty \text{ when } A >> 1+\frac{R_2}{R_1}$$

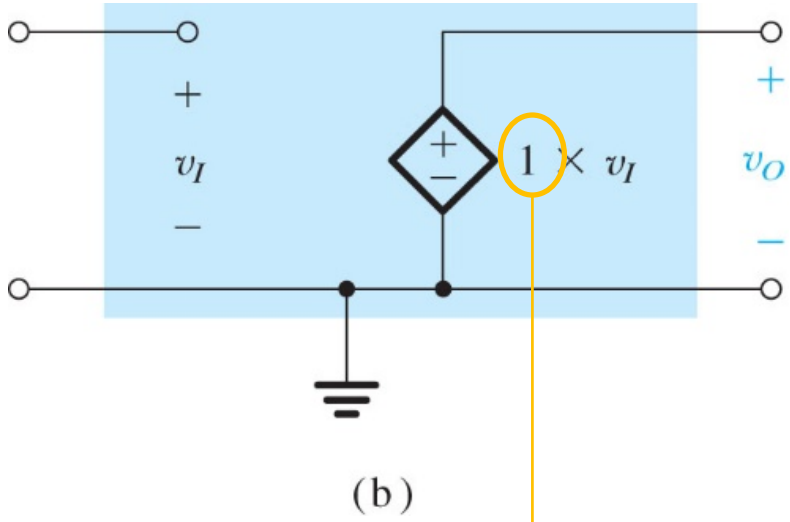
The percentage error in G resulting from the finite op-amp gain A can be determine as

$$\text{Percent gain error} = -\frac{1+\left(R_2/R_1\right)}{A+1+\left(R_2/R_1\right)}\times 100 \quad (2.12)$$

The unity-gain buffer or follower amplifier.

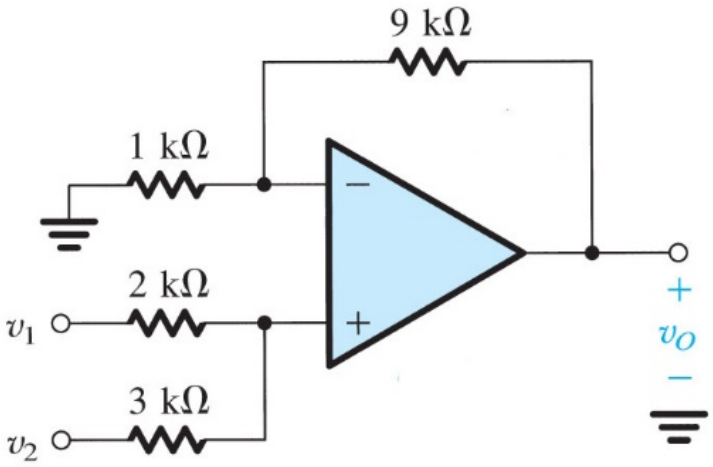


(b) Its equivalent circuit model.



The circuit has 100% negative feedback – the unity-gain amplifier. Buffer amplifier is used to connect a source with a high impedance to a low-impedance load.

Exercise 2.9. Use the **superposition principle** to find the output voltage of the circuit shown in Figure.



How does this approach work? (Board)

$$\text{Turn off } v_2 \Rightarrow v_+ = (\text{voltage divider}) = v_1 \frac{3}{2+3} = 0.6v_1$$

$$\text{Turn off } v_1 \Rightarrow v_+ = (\text{voltage divider}) = v_2 \frac{2}{2+3} = 0.4v_2$$

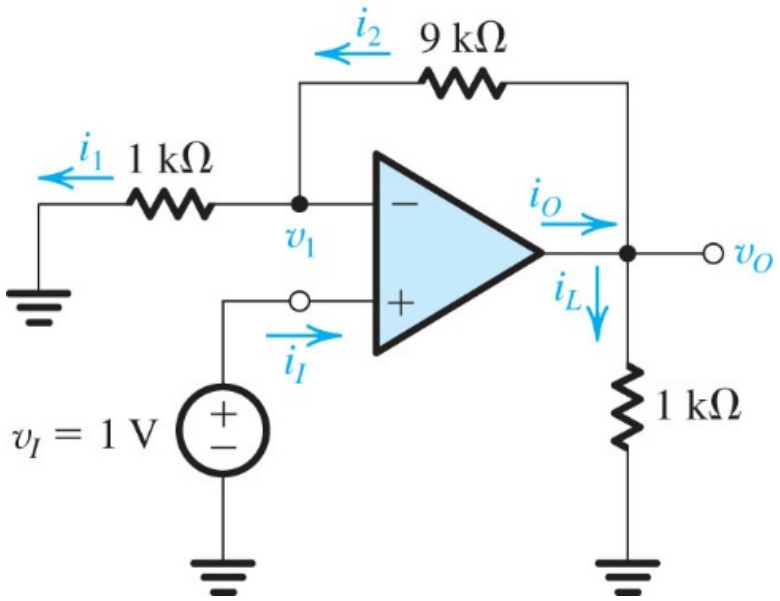
Closed-loop gain?

$$G = \frac{1+\frac{9}{1}}{1+\frac{1+\frac{9}{1}}{A}} = \frac{10}{1+\frac{10}{A}} = (\text{ideal amplifier} \rightarrow A = \infty) = 10$$

$$v_0(\text{due to } v_1) = 0.6v_1 \text{ and } v_0(\text{due to } v_2) = 0.4v_2$$

$$\text{Thus, total } v_0 = 0.6v_1 + 0.4v_2$$

Exercise 2.13. For this circuit find the values of i_I, v_1, i_1, i_2, v_0, i_L, *and* i_0. Also find the voltage gain v_0/v_I, the current gain i_L/i_I, and the power gain P_L/P_I. *(Ideal amplifier)*



$$i_I = 0 \text{ A}, v_1 = v_I = 1 \text{ V}$$

$$i_1 = \frac{v_1}{1 \text{ k}\Omega} = \frac{1 \text{ V}}{1 \text{ k}\Omega} = 1 \text{ mA}$$

$$i_2 = i_1 = 1 \text{ mA}$$

$$v_O = v_1 + i_2 \times 9 \text{ k}\Omega = 1 + 1 \times 9 = 10 \text{ V}$$

$$i_L = \frac{v_O}{1 \text{ k}\Omega} = \frac{10 \text{ V}}{1 \text{ k}\Omega} = 10 \text{ mA}$$

$$i_O = i_L + i_2 = 11 \text{ mA}$$

$$\frac{v_0}{v_I} = \frac{10}{1} = 10\frac{V}{V} \text{ or } 20 \text{ dB}$$

$$\frac{i_L}{i_I} = \frac{10 \text{ mA}}{0} = \infty$$

$$\frac{P_L}{P_I} = \frac{v_O \times i_L}{v_I \times i_I} = \frac{10 \times 10}{1 \times 0} = \infty$$

CHAPTER 2

Operational Amplifiers

Lecture 4

Fall 2019

Difference (or Differential) Amplifiers (1)

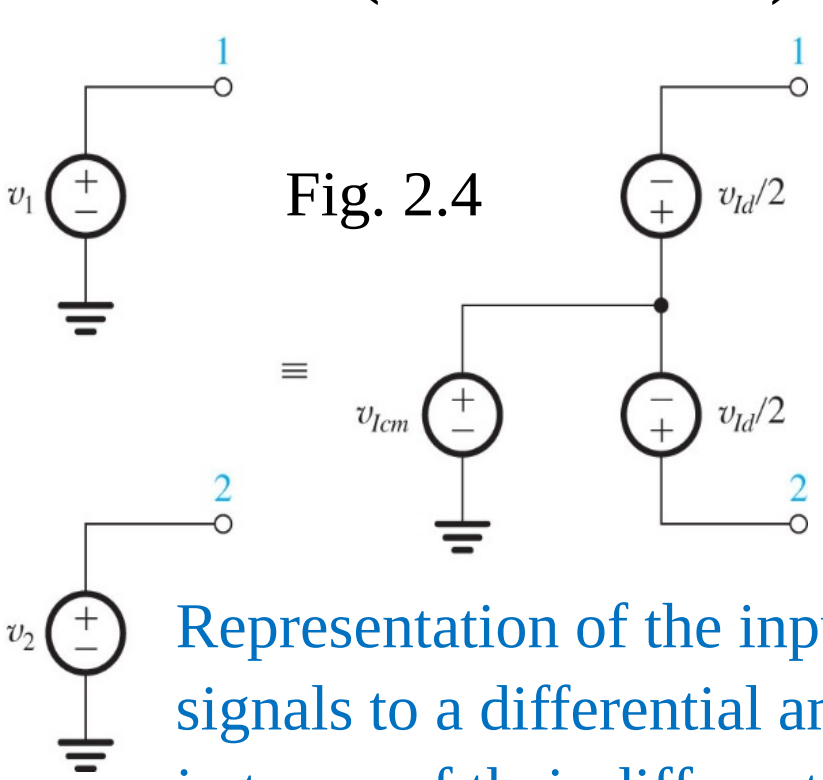


Fig. 2.4

Representation of the input signals to a differential amplifier in terms of their differential and common-mode components.

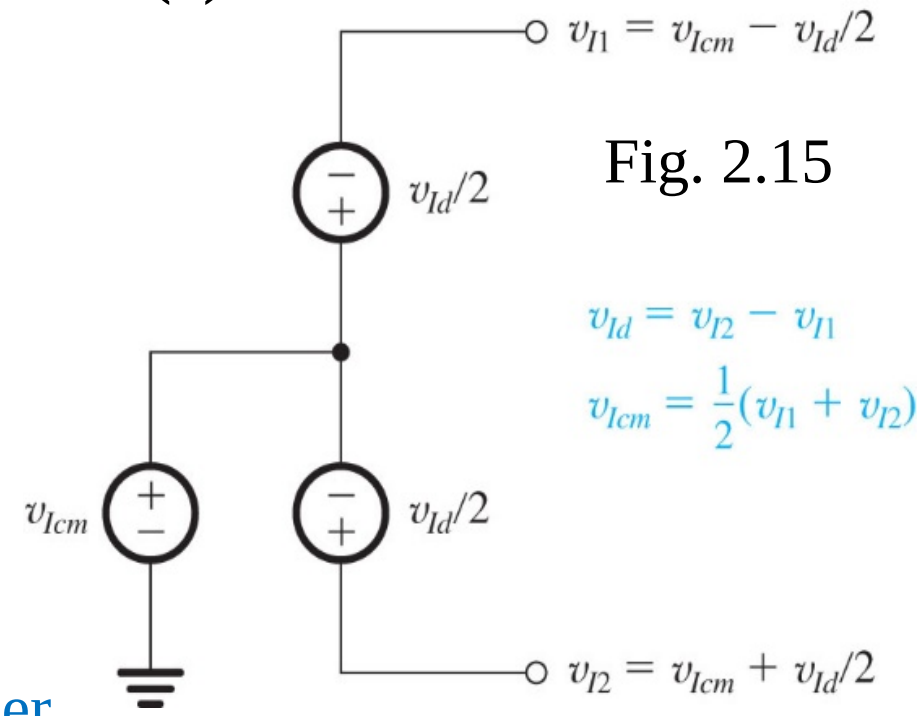


Fig. 2.15

$$v_{Id} = v_{I2} - v_{I1}$$

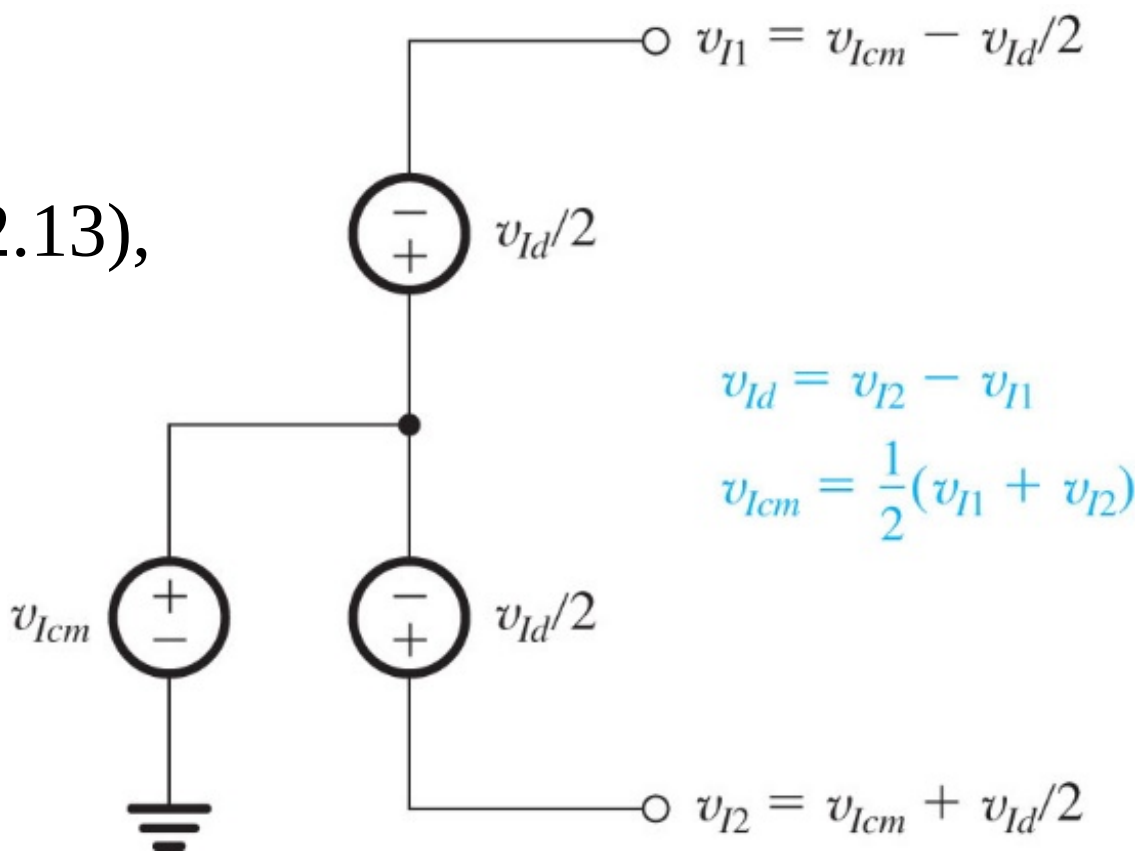
$$v_{Icm} = \frac{1}{2}(v_{I1} + v_{I2})$$

Although ideally the difference amplifier will amplify only the differential signal and reject completely the common-mode input signal, practical circuits will have an output voltage shown on the next slide!

Difference (or Differential) Amplifiers (1a)

$$v_0 = A_d v_{Id} + A_{cm} v_{Icm} \quad (2.13),$$

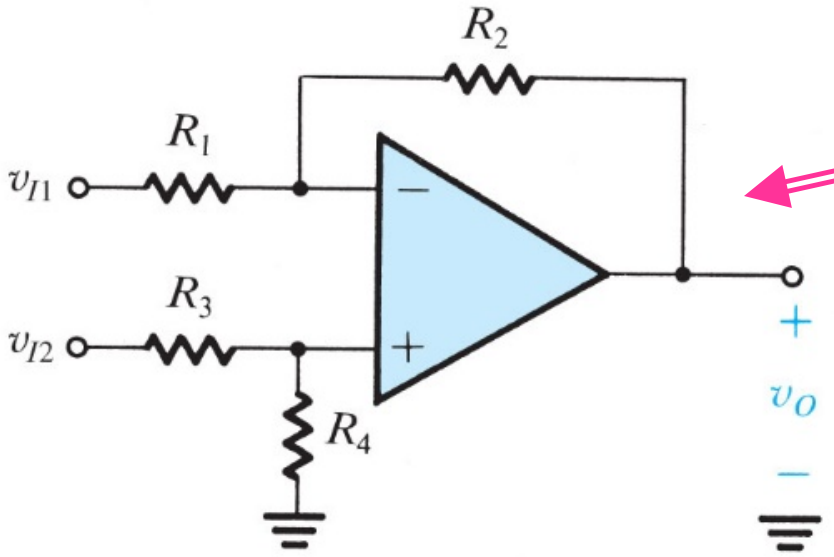
where A_{cm} ideally $= 0$



The efficacy of a differential amplifier is usually qualified by the common-mode rejection ratio

$$CMRR = 20 \lg \frac{|A_d|}{|A_{cm}|} \quad (2.14)$$

A difference amplifier (2)



Combining the inverting and noninverting configurations (Fig) yields the difference between two input signals. In order to reject common-mode signals we have to make the two gain magnitudes equal!

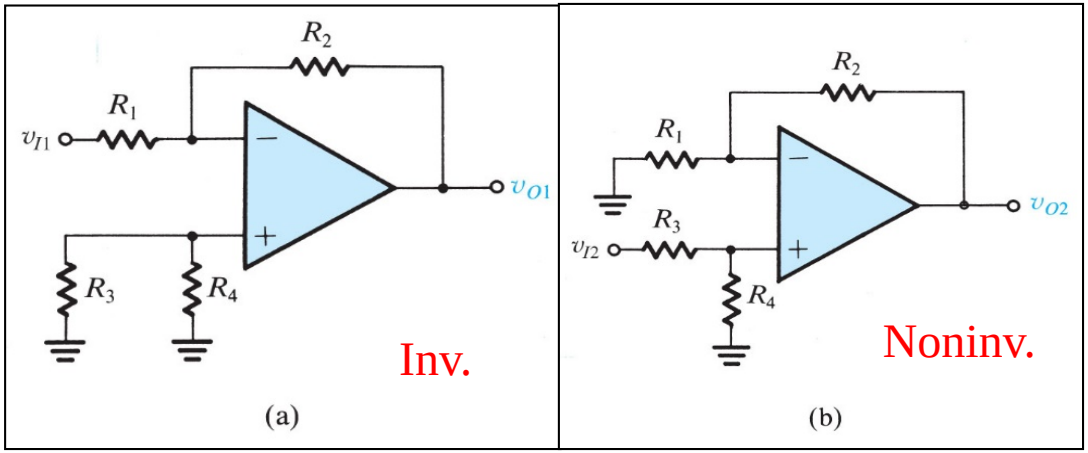
This condition can be reached when $\frac{R_4}{R_3} = \frac{R_2}{R_1}$ (2.15)

Use superposition to the analysis to determine v_0 in terms of v_{I1} and v_{I2} (shown on the next slide).

A difference amplifier (2a)

(a) R_3 and R_4 do not affect the gain:

$$v_{01} = -\frac{R_2}{R_1} v_{I1}$$



(b) Noninverting amplifier with an additional voltage divider, made up of R_3 and R_4, connected to the v_{I2}.

$$v_{02} = v_{I2} \frac{R_4}{R_3 + R_4} \left(1 + \frac{R_2}{R_1}\right) = (\text{using } 2.15) = \frac{R_2}{R_1} v_{I2}$$

$$\Rightarrow v_0 = v_{01} + v_{02} = \frac{R_2}{R_1}\left(v_{I2} - v_{I1}\right) = \frac{R_2}{R_1} v_{Id} \quad (2.16)$$

Thus, the circuit acts as a difference amplifier with a differential gain:

$$A_d = \frac{R_2}{R_1} (2.17)$$

A difference amplifier (3)

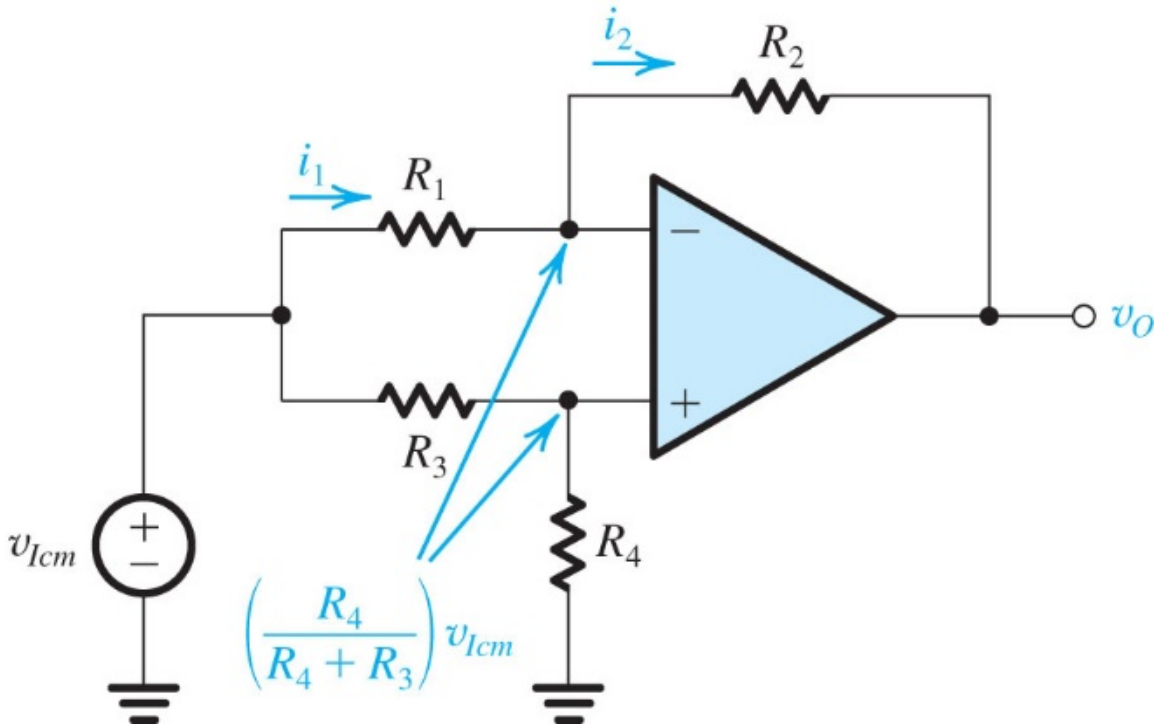


Figure 2.18. Analysis to determine a common-mode gain,

$$A_{cm} \equiv v_0 / v_{Icm} .$$

$$A_{cm} \equiv \frac{v_0}{v_{Icm}} = \frac{R_4}{R_3 + R_4}\left(1 - \frac{R_2}{R_1}\frac{R_3}{R_4}\right) \qquad (2.19)$$

A difference amplifier (3a)

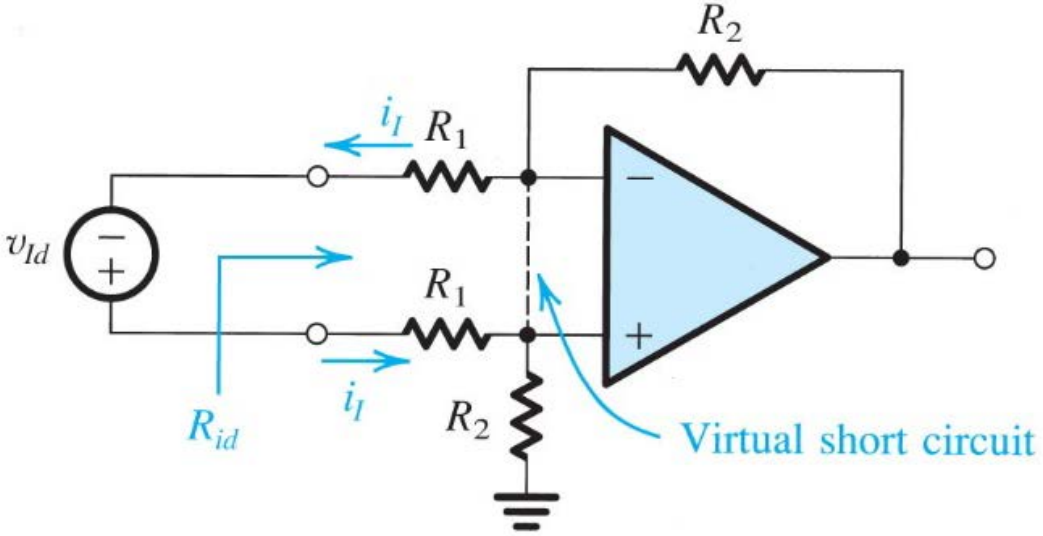


Fig. 2.19 The input resistance, R_{id}, of the difference amplifier for the case $R_3 = R_1$ and $R_4 = R_2$.

$$R_{id} \equiv \frac{v_{Id}}{i_I} = \left(\text{from a loop equation}\right) = \frac{R_1 i_I + 0 + R_1 i_I}{i_I} = 2R_1$$

If a large differential gain R_2 / R_1 is required, then R_1 must be small, thus R_{id} will be small (this is a drawback of this circuit). It is not easy to vary the differential gain (second drawback). Instrumentation amplifier is needed.

Instrumentation amplifier

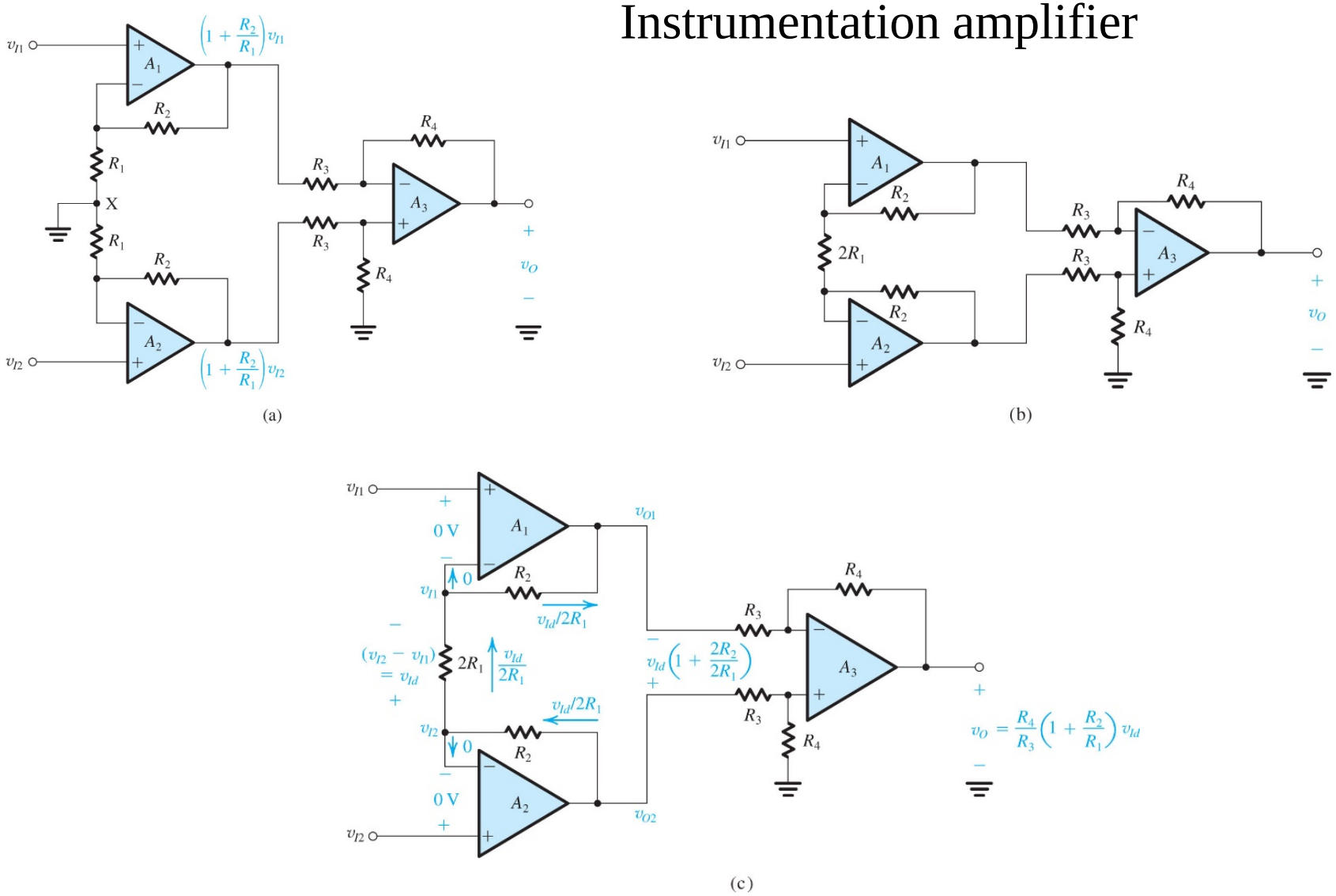
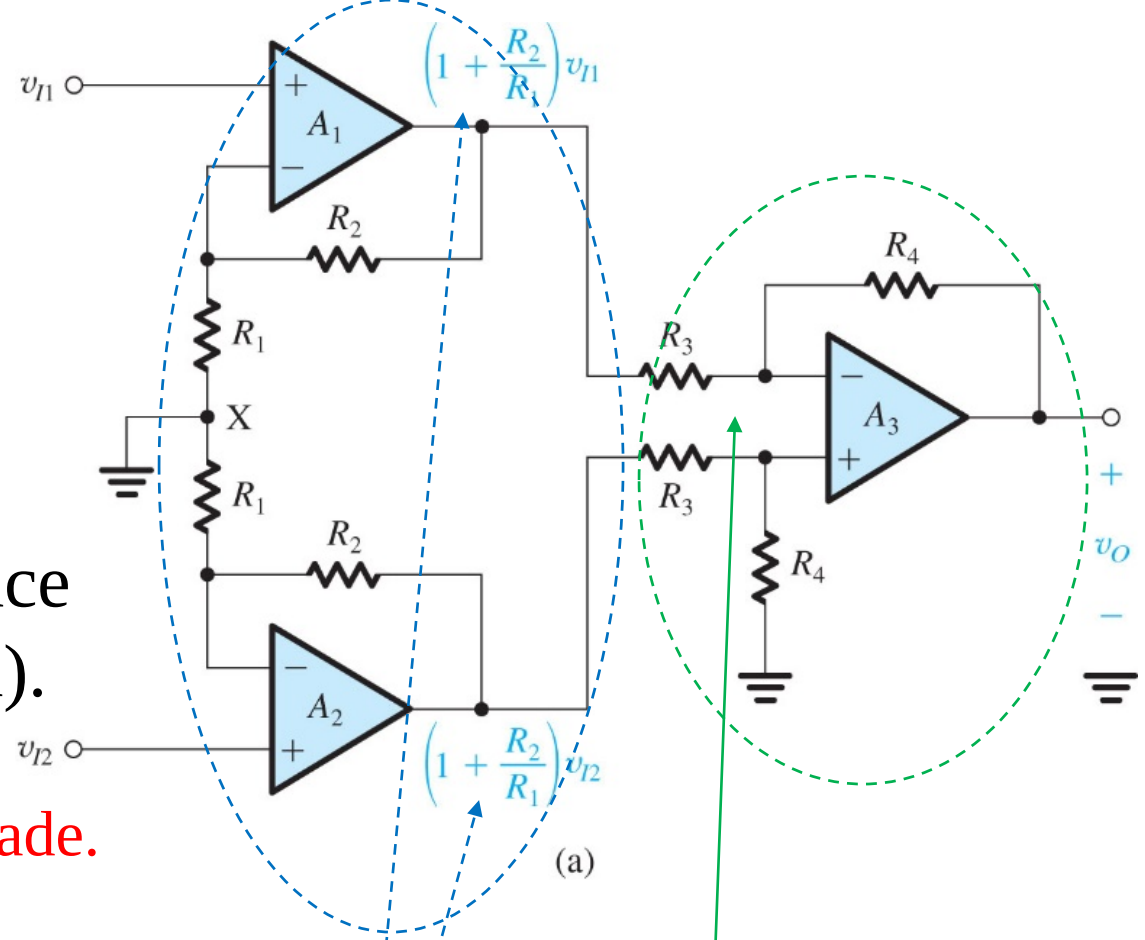


Figure 2.20 A popular circuit for an instrumentation amplifier. **(a)** Initial approach to the circuit. **(b)** The circuit in **(a)** with the connection between node X and ground removed and the two resistors R_1 and R_1 lumped together. This simple wiring change dramatically improves performance. **(c)** Analysis of the circuit in **(b)** assuming ideal op amps.

Instrumentation amplifier (1)

Use the followers with gain (not unity-gain) to buffer the two input terminals of the difference amplifier as shown in (a).



There are two stages in cascade.

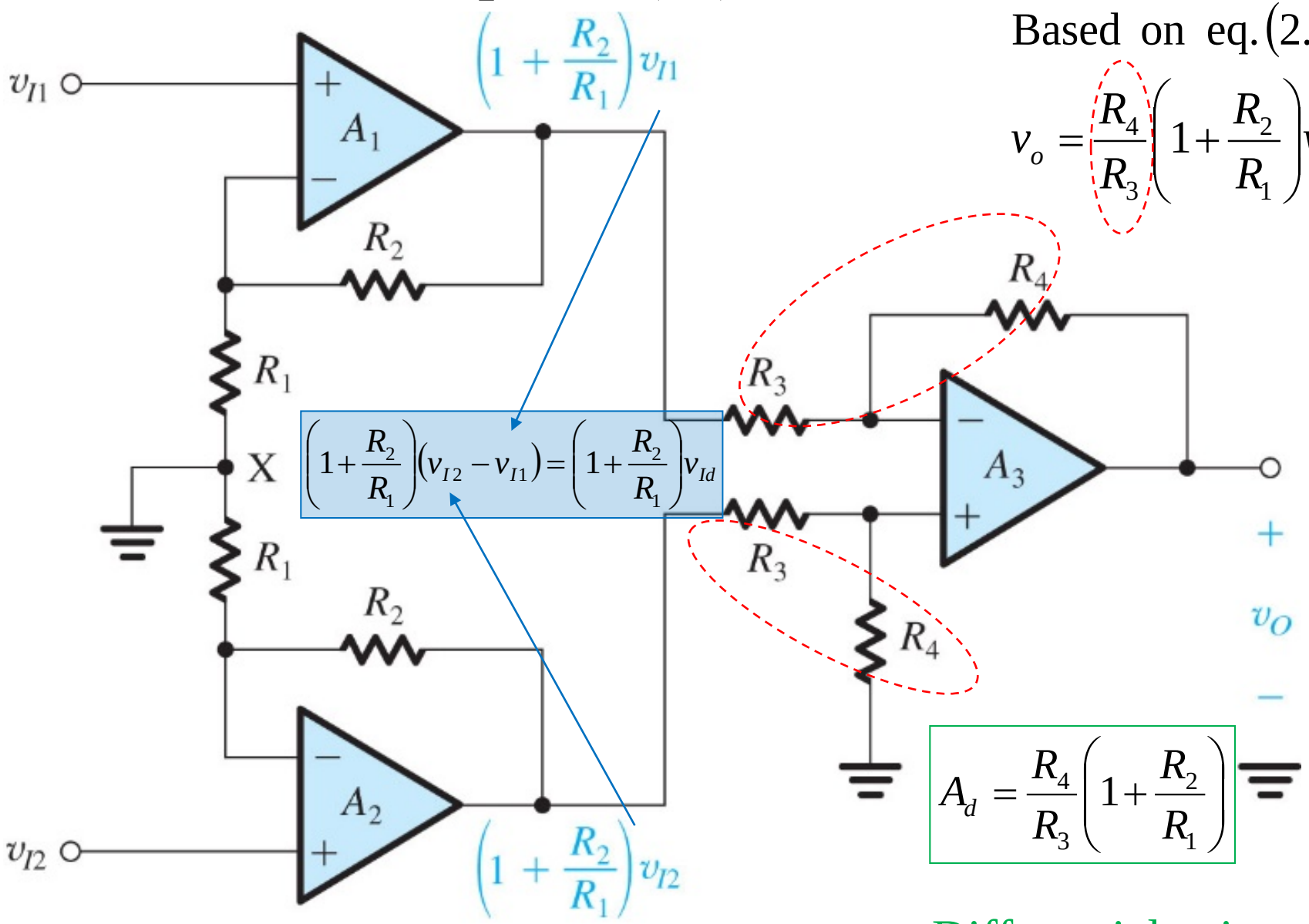
The first stage is formed by op amps A_1 and A_2 and their resistors R_2 and R_1. Each has a closed loop gain $(1 + R_2/R_1)$ {see corresponding v_0}.

The second stage (difference amplifier) operates on the difference signal

Instrumentation amplifier (1a)

Based on eq.(2.16)

$$v_o = \frac{R_4}{R_3}\left(1+\frac{R_2}{R_1}\right)v_{Id}$$



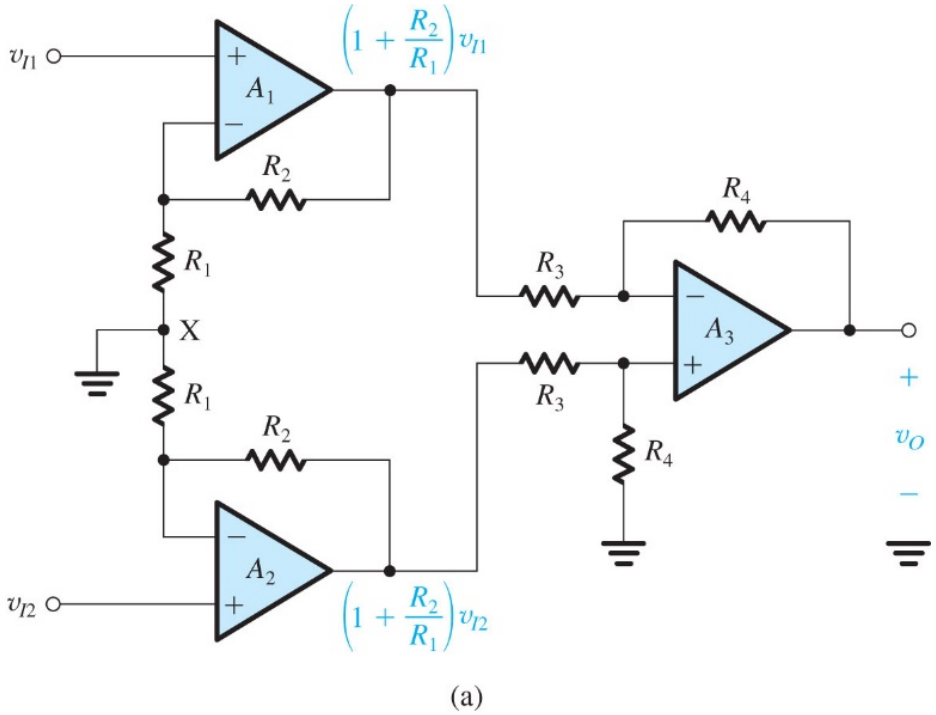
$$A_d = \frac{R_4}{R_3}\left(1+\frac{R_2}{R_1}\right)$$

Differential gain

(a)

Instrumentation amplifier (1b)

Summary for the circuit in Fig. 2.20(a)



(a)

Advantages: very high input resistance and high differential gain; signal paths are symmetric!

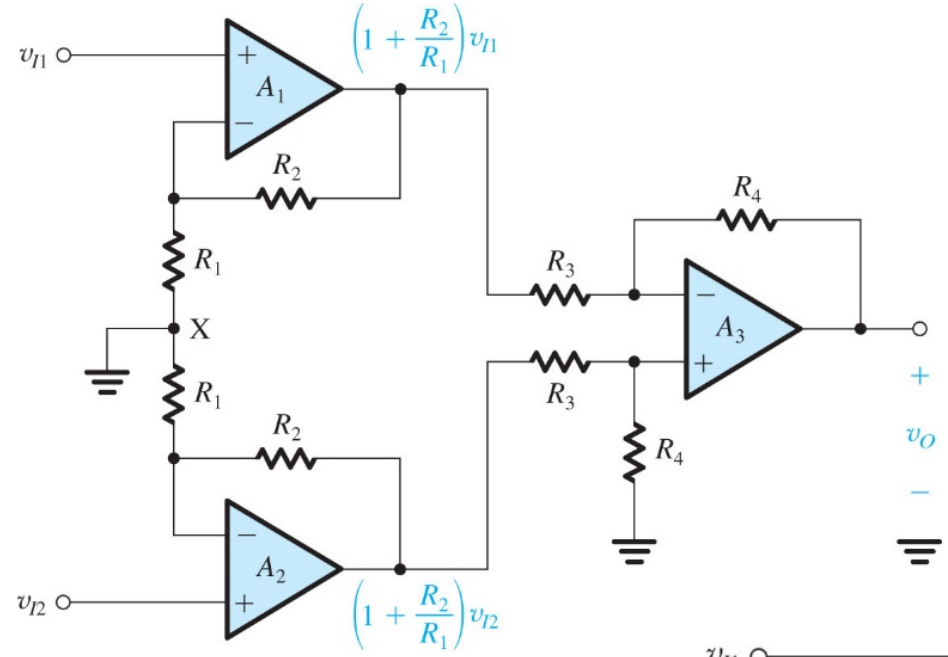
Disadvantages:

1) the v_{Icm} is amplified in the first stage too much (saturation, poor CMRR)

2) A_1 and A_2 op amps must be perfectly matched (faked signal may appear and amplified in the second stage.

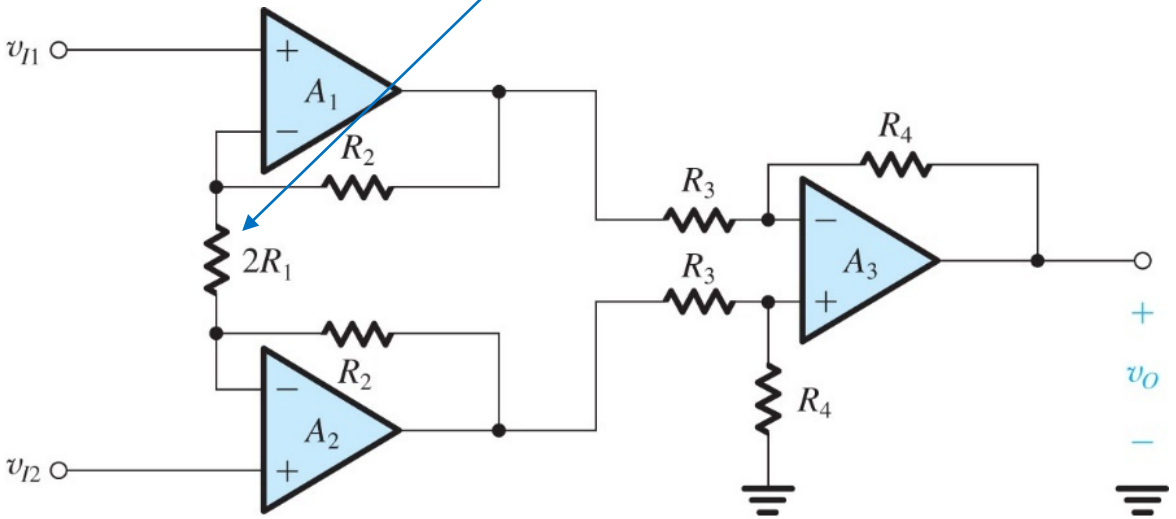
3) To vary A_d, two resistors (two R_1 or two R_2) must be varied simultaneously.

Instrumentation amplifier (2)



(a)

The circuit with the connection between node X and ground removed and the two resistors R_1 and R_1 lumped together.



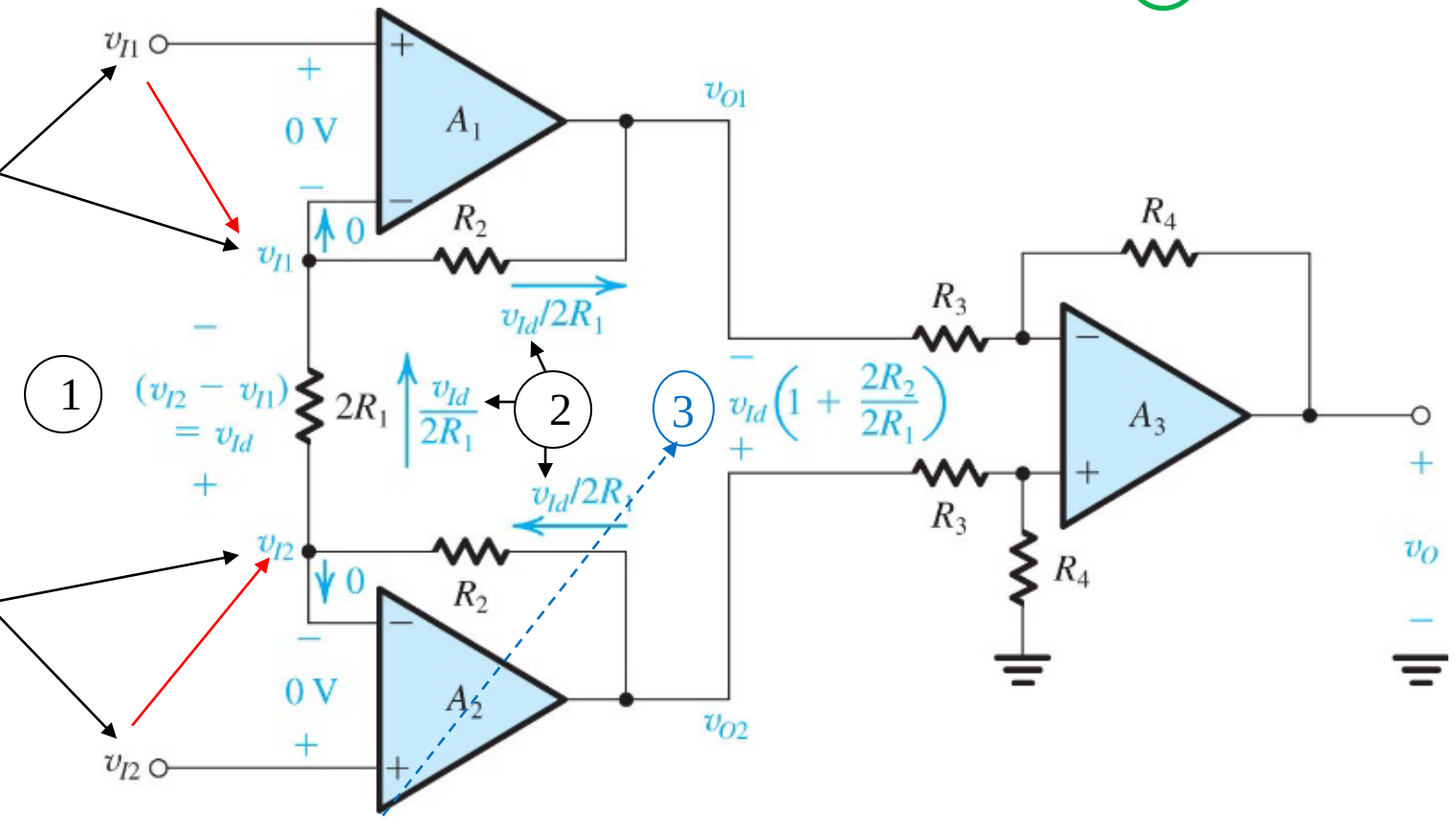
(b)

This simple wiring change solves all three issues of the ciruit in Fig. 2.20(a)

Instrumentation amplifier (2a)

Let's analyze assuming ideal op amps: start with (1)

appear due to virtual short circuits at the inputs of A_1 and A_2



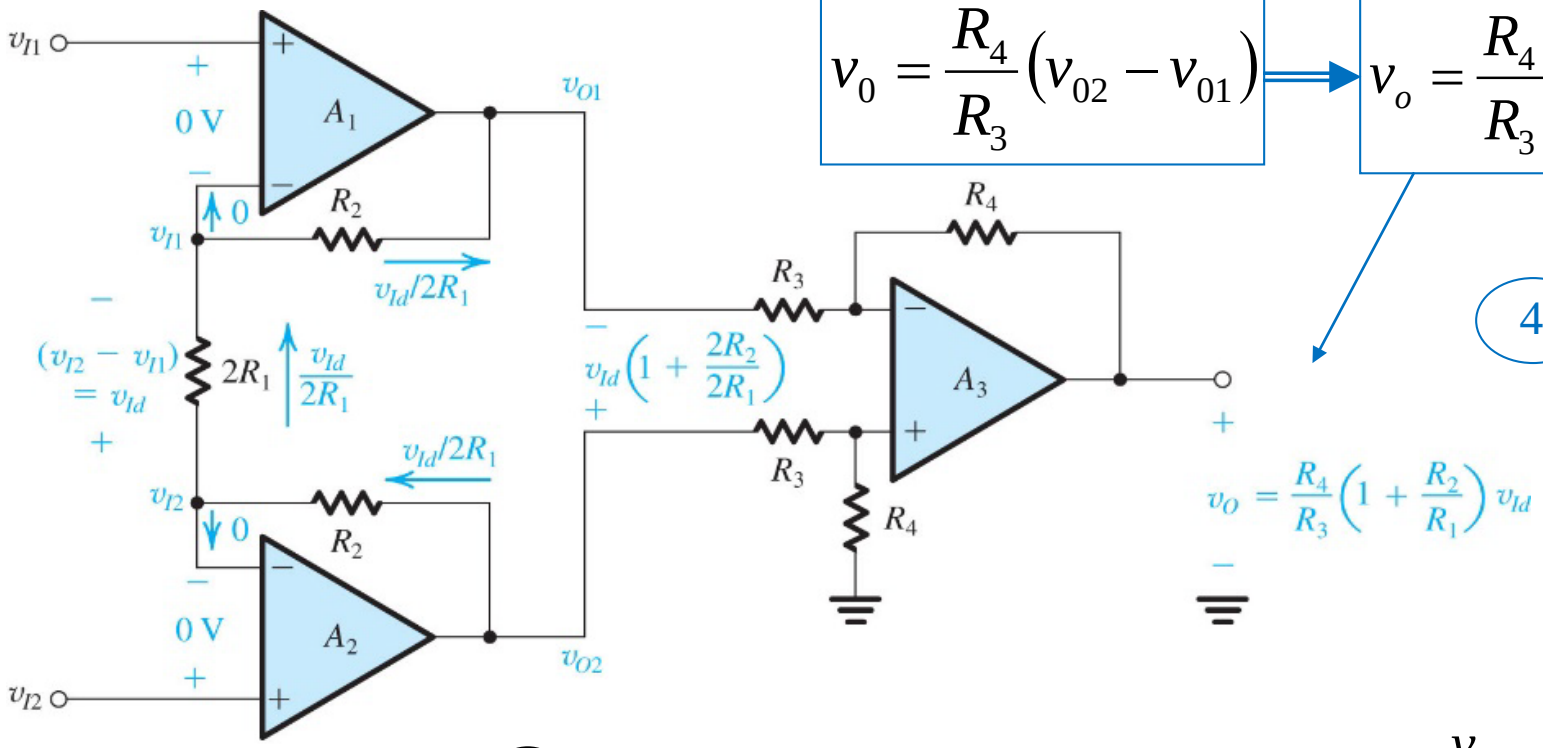
(3)

$$v_{02} - v_{01} = \left(v_{I2} + \frac{v_{Id}}{2R_1}R_2\right) - \left(v_{I1} - \frac{v_{Id}}{2R_1}R_2\right) = v_{Id}\left(1 + \frac{2R_2}{2R_1}\right)$$

Instrumentation amplifier (2b)

$$v_0 = \frac{R_4}{R_3}(v_{02} - v_{01}) \Rightarrow v_o = \frac{R_4}{R_3}\left(1 + \frac{R_2}{R_1}\right)v_{Id}$$

Based on eq.(2.16)



4

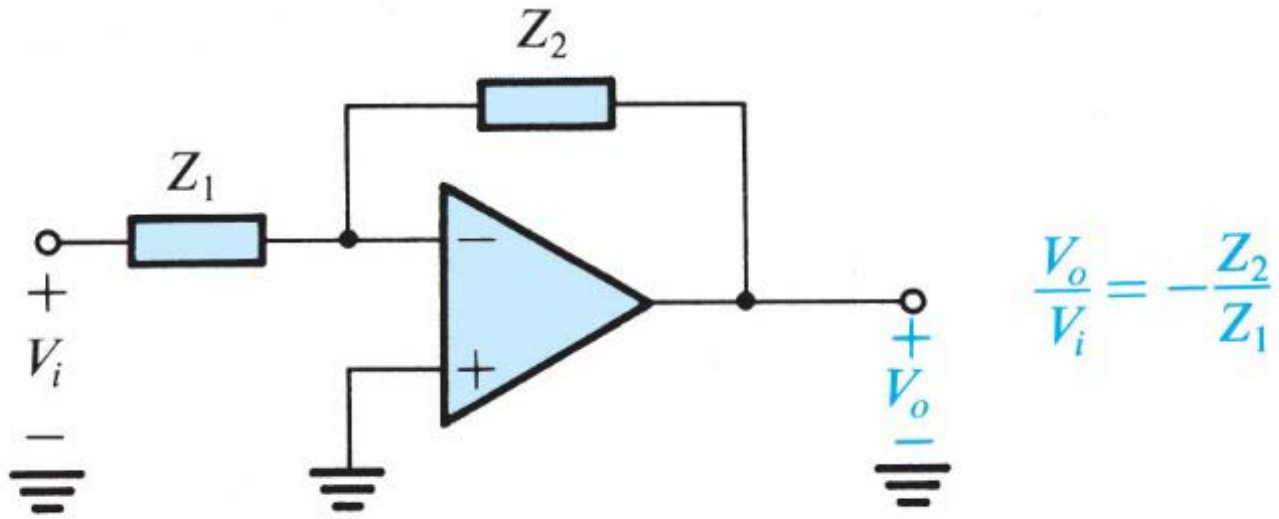
5 Overall differential voltage gain $A_d \equiv \dfrac{v_0}{v_{Id}} = \dfrac{R_4}{R_3}\left(1 + \dfrac{R_2}{R_1}\right)$

5 If two input terminals are connected together to v_{Icm} there is no current through $2R_1$, thus there is no current through R_2, and v_{Icm} is not amplified by the first stage as well as by second stage.

Varied one resistor, $2R_1$, changes the gain.

Integrators and Differentiators (1)

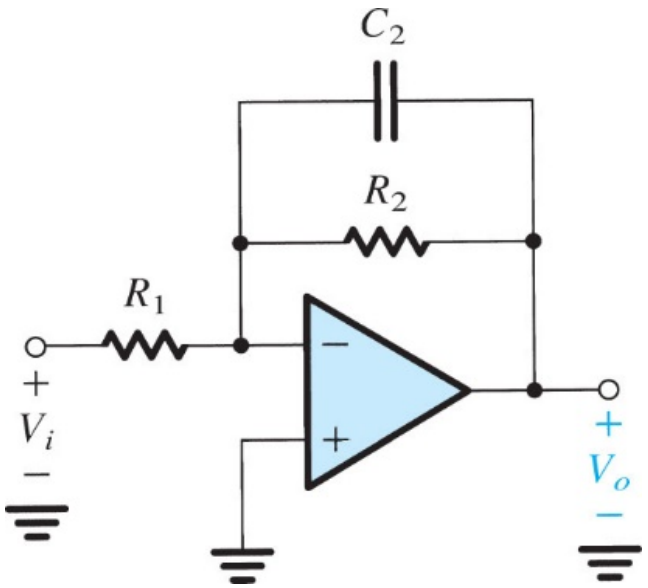
The ***inverting configuration*** with general impedances in the feedback and the feed-in paths.



The closed-loop transfer function is

$$\frac{V_0(j\omega)}{V_i(j\omega)} = \frac{V_0(s)}{V_i(s)} = -\frac{Z_2(s)}{Z_1(s)} \qquad (2.24)$$

Integrators and Differentiators (2)



Example 2.4. Derive the transfer function

$$\frac{V_0(s)}{V_i(s)} = -\frac{Z_2(s) = \left(R_2 \left\| \frac{1}{sC_2} \right. \right.}{Z_1(s) = R_1}$$

$$= -\frac{1}{R_1\{Y_2(s) = [(1/R_2) + sC_2]\}}$$

$$= -\frac{1}{\frac{R_1}{R_2} + sC_2R_1} = \frac{-(R_2/R_1)}{1 + sC_2R_2}$$

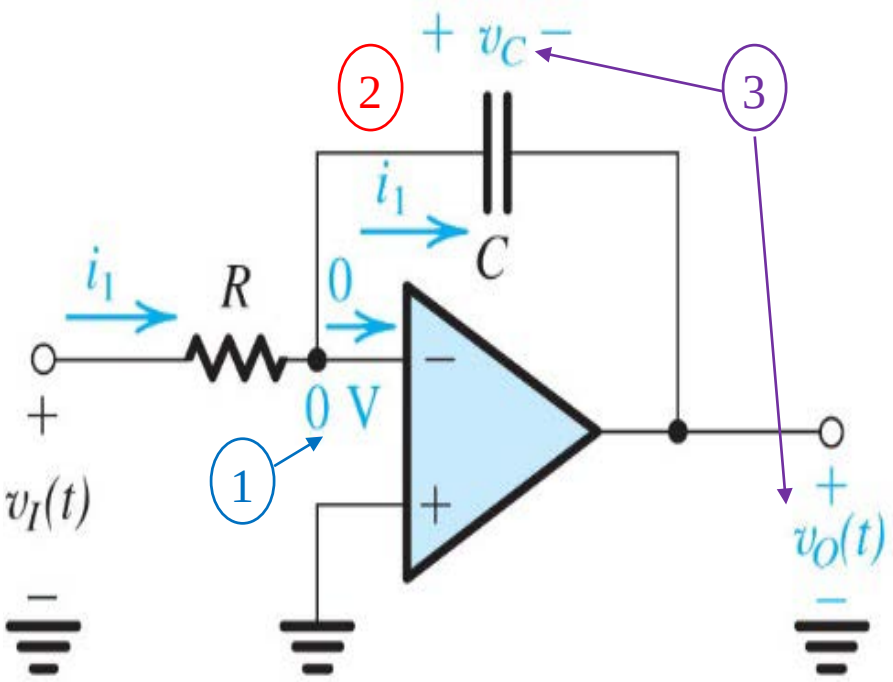
$$\left(\text{low - pass STC network}\right)$$

for which the dc gain $K = -\dfrac{R_2}{R_1}$

and $\omega_0 = \dfrac{1}{C_2R_2}$ is 3-dB frequency

Why only R_2 seen by C_2 ?

The inverting integrator (1)



The Miller or inverting integrator

Time domain analysis:

1) virtual ground => $i_1(t) = v_I(t)/R$;
2) charge capacitor by time-varying $i_1(t) = v_I(t)/R$;
3) if the initial voltage on C ($t = 0$) is V_C, then

3

$$v_C(t) = V_C + \frac{1}{C}\int_0^t i_1(t)dt$$

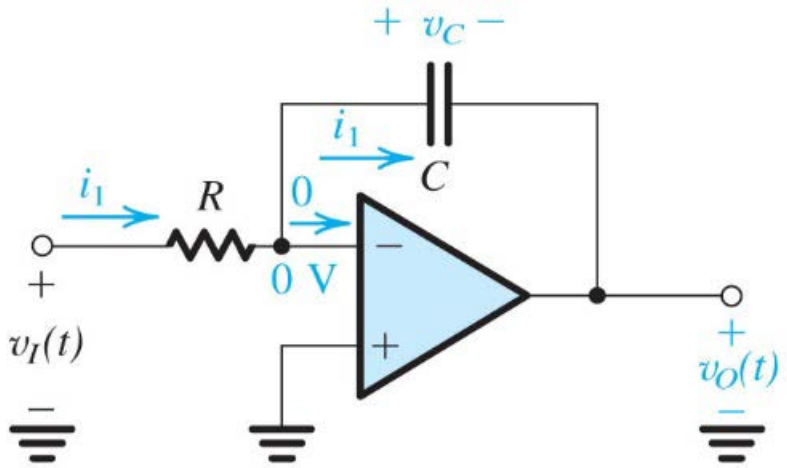
$$= V_C + \frac{1}{C}\int_0^t \frac{v_I(t)}{R}dt$$

4 Using a virtual ground => $v_0(t) = -v_C(t)$

$$\text{Thus, } v_0(t) = -\frac{1}{CR}\int_0^t v_I(t)dt - V_C \quad (2.25)$$

CR is the integrator time constant

The inverting integrator (1a)

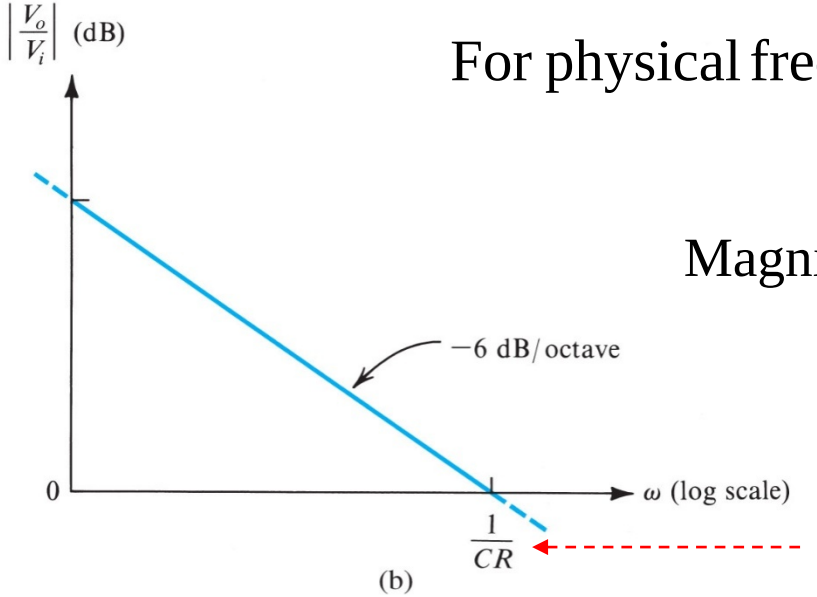


The Miller or inverting integrator

Frequency domain analysis:

$Z_1(s) = R$ and $Z_2(s) = 1/sC$ => (2.24)

The transfer function is $\frac{V_0(s)}{V_i(s)} = -\frac{1}{sCR}$ (2.26)



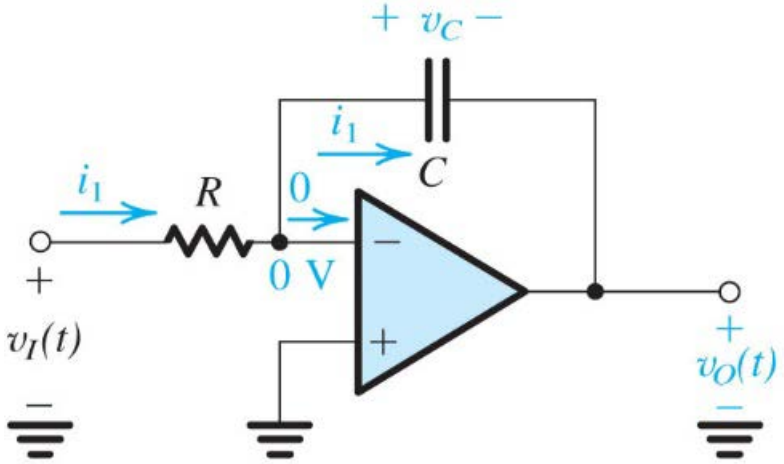
Frequency response of the integrator. Bode plot.

For physical frequencies $\frac{V_0(j\omega)}{V_i(j\omega)} = -\frac{1}{j\omega CR}$ (2.27)

Magnitude is $\left|\frac{V_0}{V_i}\right| = \frac{1}{\omega CR}$ and phase is $\phi = +90^0$

At integrator frequency $\omega = (CR)^{-1}$ $\left|\frac{V_0}{V_i}\right| = 1$

The inverting integrator (2)

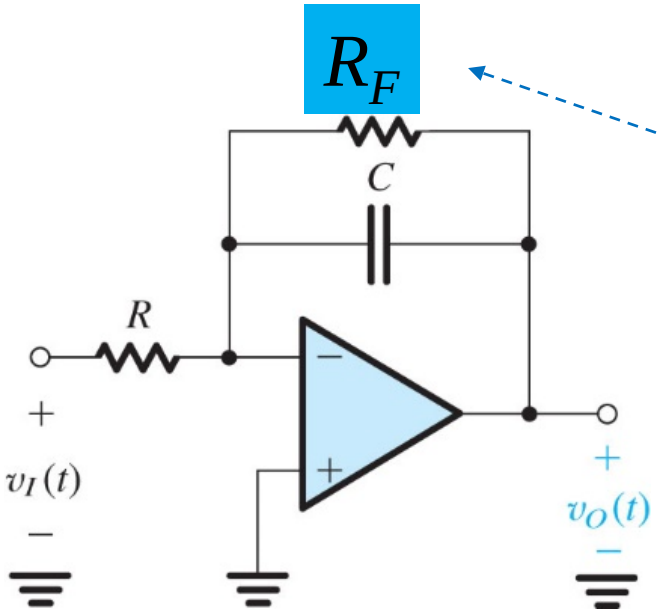


Frequency response – STC low-pass network.

The magnitude of the transfer function is infinite (∞) at $\omega = 0$.

At *dc* there is no negative feedback! Theoretically, any tiny *dc* component => an infinite output. In practice the amplifier saturates at a voltage close to the op-amp positive or negative power supply depending on polarity of the input *dc* signal.

The inverting integrator (2a)



Alleviate *dc* problem

The Miller integrator with a large resistance R_F connected in parallel with C in order to provide negative feedback and hence finite gain at dc.

The gain at dc is $-(R_F / R)$, not infinite!

The lower the value of R_F, the less ideal integrator is.

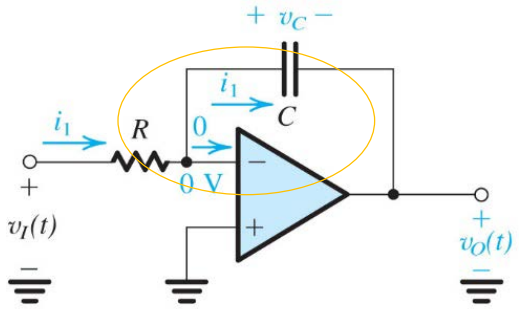
The integrator transfer function becomes:

$$\frac{V_0(s)}{V_i(s)} = -\frac{R_F / R}{1 + sCR_F} \quad \text{not} \quad -\frac{1}{sCR}$$

The integrator pole moves from its ideal location at ω = 0

The effect of R_F is discussed in Example 2.5

Example 2.5 Find the output produces by a Miller integrator in response to an input in Fig. (a)



The Miller integrator without a large resistance R_F connected in parallel with C in order to provide negative feedback and hence finite gain at dc.

R = 10 kΩ, R_F = 1 MΩ and C = 10 nF.

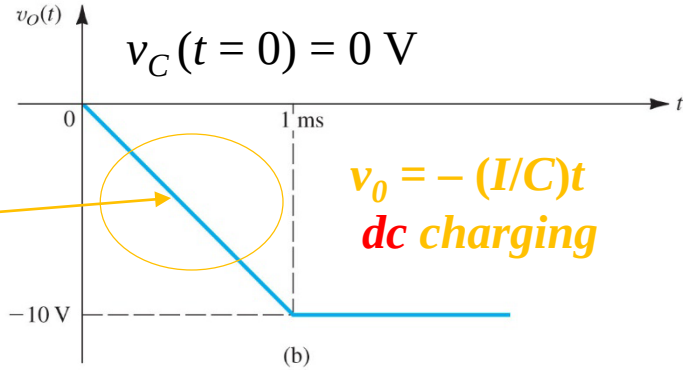
Saturates at ± 13 V

$i_1(t) = v_I(t)/R$ (charges capacitor)
= 1 V/10 kΩ = 0.1 mA = I (dc)

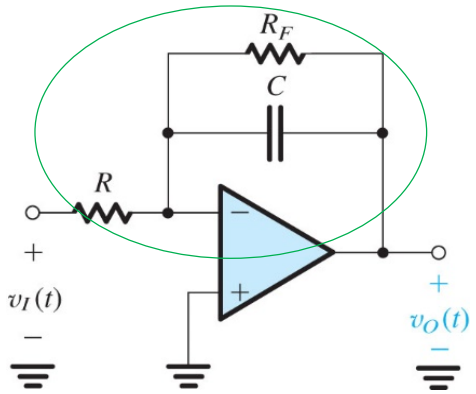
$$v_0(t) = -\frac{1}{CR}\int_0^t v_I(t)dt - V_C \quad (2.25)$$

$$= (V_C = 0\,\text{V}, v_I = 1\,\text{V}, \text{ and } 0 \le t \le 1\,\text{ms})$$

$$= -10 \times t\,(\text{Volt}),\ \tau = C \times R = 0.1\,\text{ms}$$



Example 2.5 Find the output produces by a Miller integrator in response to an input in Fig. (a)



The Miller integrator with a large resistance R_F connected in parallel with C in order to provide negative feedback and hence finite gain at dc.

The 1-V input pulse produces the same *dc* I = 0.1 mA, which is supplied to an STC network $R_F \| C$ ($\tau = R_F C$ = 10 ms)

$$\frac{V_0(s)}{V_i(s)} = -\frac{R_F/R}{1+sCR_F} \Rightarrow \text{dc gain} = -\frac{R_F}{R} = -100\,\frac{\text{V}}{\text{V}}$$

$$v_0(t) = -\frac{1}{R_F C}\int_0^t v_I(t)dt = -100\left(1-e^{-t/10}\right),\ 0 \le t \le 1\,\text{ms}$$

$$v_0(t = 1\,\text{ms}) = -100\left(1-e^{-1/10}\right) \approx -9.52\ \text{V}$$