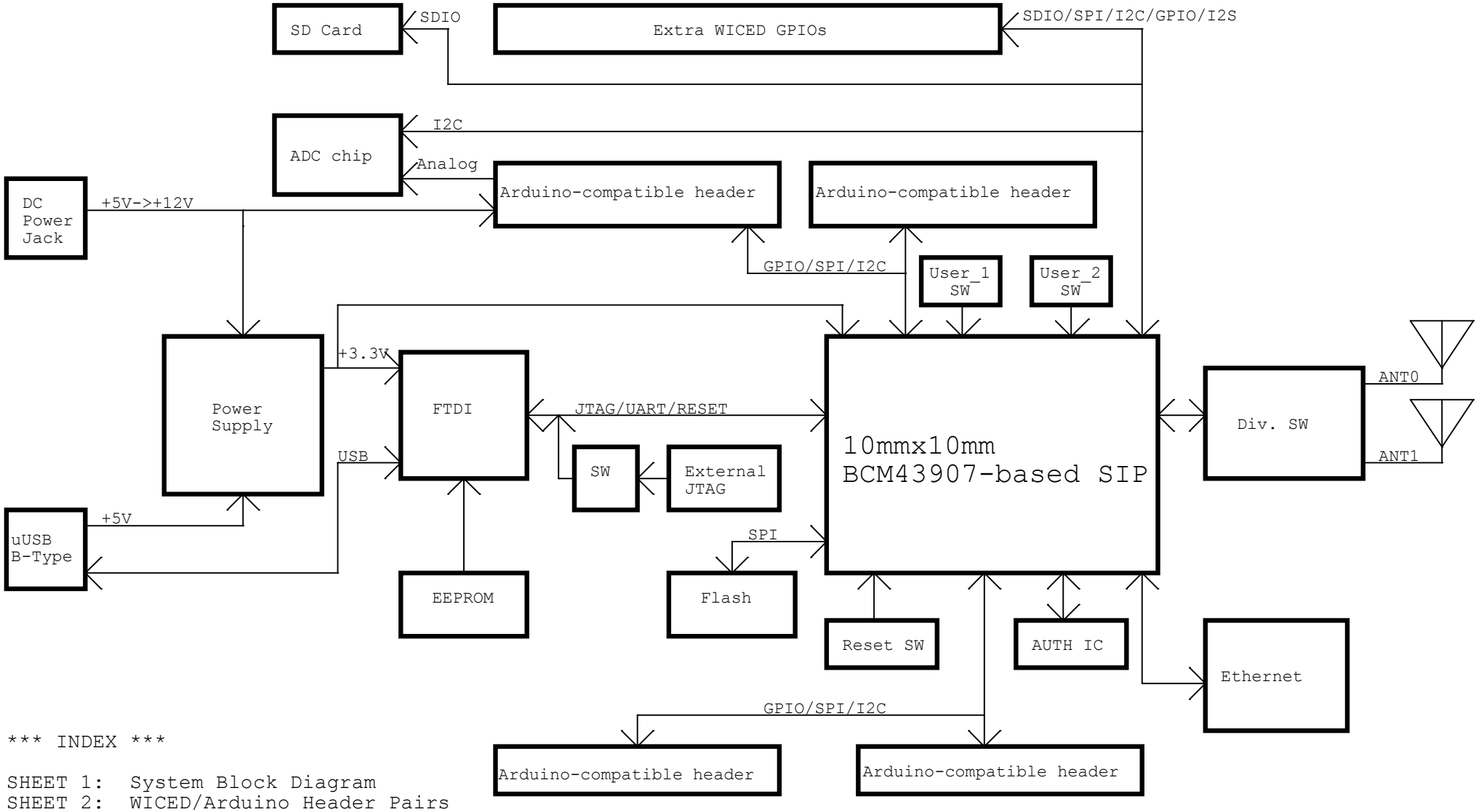
# CYW943907AEVAL1F

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## SYSTEM BLOCK DIAGRAM

| | | | | |
|---|---|---|---|---|
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| Title: CYW943907AEVAL1F | | | | |
| Size: A | Document Number: 630-60379-01 | Designer | Deval Dave | Rev: 1.0 |
| Date: Friday, May 26, 2017 | | Sheet 1 of 10 | | |

| BCM43907-based SiP Pin Name | WICED header net name |
|---|---|
| PWM_3 | PWM_3 |
| PWM_4 | PWM_4 |
| PWM_5 | PWM_5 |
| I2S0_MCK | I2S0_MCK |
| I2S0_SD_OUT | I2S0_SD_OUT |
| I2S0_SCK_BLCK | I2S0_SCK_BLCK |
| I2S0_WS_LRCLK | I2S0_WS_LRCLK |
| GND | GND |
| SPI_1_CLK | SPI_1_CLK |
| I2S1_SD_OUT | I2S1_SD_OUT |
| SPI_1_MISO | SPI_1_MISO |
| SPI_0_CLK | SPI_0_CLK |
| SPI_1_MOSI | SPI_1_MOSI |
| SPI_0_MOSI | SPI_0_MOSI |
| SPI_1_CS | SPI_1_CS |
| SPI_0_CS | SPI_0_CS |
| SPI_0_MISO | SPI_0_MISO |
| UART0_RXD_IN | UART0_RXD_IN |
| GND | GND |
| UART0_TXD_OUT | UART0_TXD_OUT |
| USB2_HOST_DEV_SEL | USB2_HOST_DEV_SEL |
| UART0_CTS_IN | UART0_CTS_IN |
| I2C_0_SCL | I2C_0_SCL |
| UART0_RTS_OUT | UART0_RTS_OUT |
| I2C_0_SDA | I2C_0_SDA |
| I2S1_MCK | I2S1_MCK |
| I2S1_WS_LRCLK | I2S1_WS_LRCLK |
| GND | GND |
| I2S1_SCK_BCLK | I2S1_SCK_BCLK |
| SDIO_DATA1 | SDIO_DATA_1 |
| SDIO_DATA0 | SDIO_DATA_0 |
| SDIO_CLK | SDIO_CLK |
| SDIO_CMD | SDIO_CMD |
| SDIO_DATA3 | SDIO_DATA_3 |
| SDIO_DATA2 | SDIO_DATA_2 |
| RF_SW_CTRL_6_UART1_RX_IN | RF_SW_CTRL_6_UART1_RXD |
| RF_SW_CTRL_7_RSRC_INIT_MODE_UART1_TX_OUT | UART1_TXD |
| RF_SW_CTRL_8_UART2_RX | RF_SW_CTRL_8_UART2_RXD |
| RF_SW_CTRL_9_HIB_LPO_SEL_UART2_TX | UART2_TXD |
| HIB_WAKE | HIB_WAKE |
| HIB_LPO_SEL | HIB_LPO_SEL |
| HIB_REG_ON_IN | HIB_REG_ON_IN |
| USB2_DN | USB2_DN |
| USB2_DP | USB2_DP |

| BCM43907-based SiP Pin Name | BCM43907-based SiP Pin Function | Bootstrap option | Arduino header net name | Arduino functions |
|---|---|---|---|---|
| GPIO_0 | UART0_RX | | ARD_GPIO0 | UART_RX |
| GPIO_1_GSPI_MODE | UART0_TX | GSPI MODE | ARD_GPIO1 | UART_TX |
| GPIO_13_SDIO_MODE | GPIO_13 | SDIO MOD | ARD_GPIO2 | GPIO |
| GPIO_7_WCPU_BOOT_MODE | PWM5 | WLAN BOOT | ARD_GPIO3 | PWM |
| GPIO_14 | GPIO_14 | | ARD_GPIO4 | GPIO |
| GPIO_16 | PWM2 | | ARD_GPIO5 | PWM |
| GPIO_15 | PWM3 | | ARD_GPIO6 | PWM |
| I2S0_SD_IN | GPIO_26 | | ARD_GPIO7 | GPIO |
| N/A(uses external ADC chip) | ADC | | ARD_AD0 | AD0 |
| N/A(uses external ADC chip) | ADC | | ARD_AD1 | AD1 |
| N/A(uses external ADC chip) | ADC | | ARD_AD2 | AD2 |
| N/A(uses external ADC chip) | ADC | | ARD_AD3 | AD3 |
| N/A(uses external ADC chip) | ADC | | ARD_AD4_SDA | AD4, SDA |
| N/A(uses external ADC chip) | ADC | | ARD_AD5_SCL | AD5, SCL |
| I2S1_SD_IN | GPIO_29 | | ARD_GPIO8 | GPIO |
| PWM_4 | PWM4 | | ARD_GPIO9 | PWM |
| GPIO_11_ACPU_BOOT_MODE | SPI1_CS, PWM1 | APPS BOOT | ARD_SS | PWM, SPI_CS |
| GPIO_10 | SPI1_MOSI, PWM0 | | ARD_MOSI | PWM, SPI_MOSI |
| GPIO_12 | SPI1_MISO | | ARD_MISO | SPI_MISO |
| GPIO_9_USB_SEL | SPI1_CLK | | ARD_SCK | SPI_SCK |
| GND | GND | | GND | GND |
| N/A (supplied off eval board) | N/A (supplied off eval board) | | ARD_AREF | POWER |
| I2C_1_SDA | I2C_SDA | | ARD_AD4_SDA | AD4, SDA |
| I2C_1_SCL | I2C_SCL | | ARD_AD5_SCL | AD5, SCL |
| NC | NC | | ARD_NC | NC |
| N/A (supplied off eval board) | N/A (supplied off eval board) | | ARD_IOREF | POWER |
| RESET_L | RESET | | ARD_RESET | RESET |
| N/A (supplied off eval board) | N/A (supplied off eval board) | | +3V3 | POWER |
| N/A (supplied off eval board) | N/A (supplied off eval board) | | NC | POWER |
| GND | GND | | GND | GND |
| GND | GND | | GND | GND |
| N/A (supplied off eval board) | N/A (supplied off eval board) | | VIN_EXT | POWER |

| BCM43907-based SiP Pin Name | On Board Debug Interface |
|---|---|
| GPIO2_JTAG_TCK | GPIO2_JTAG_TCK |
| GPIO3_JTAG_TMS | GPIO3_JTAG_TMS |
| GPIO4_JTAG_TDI | GPIO4_JTAG_TDI |
| GPIO5_JTAG_TDO | GPIO5_JTAG_TDO |
| GPIO6_JTAG_TRST_N | GPIO6_JTAG_TRST_N |
| RF_SW_CTRL_7_RSRC_INIT_MODE_UART1_TX_OUT | UART1_TXD |
| RF_SW_CTRL_6_UART1_RX_IN | RF_SW_CTRL_6_UART1_RXD |

# WICED / ARDUINO HEADER PAIRS

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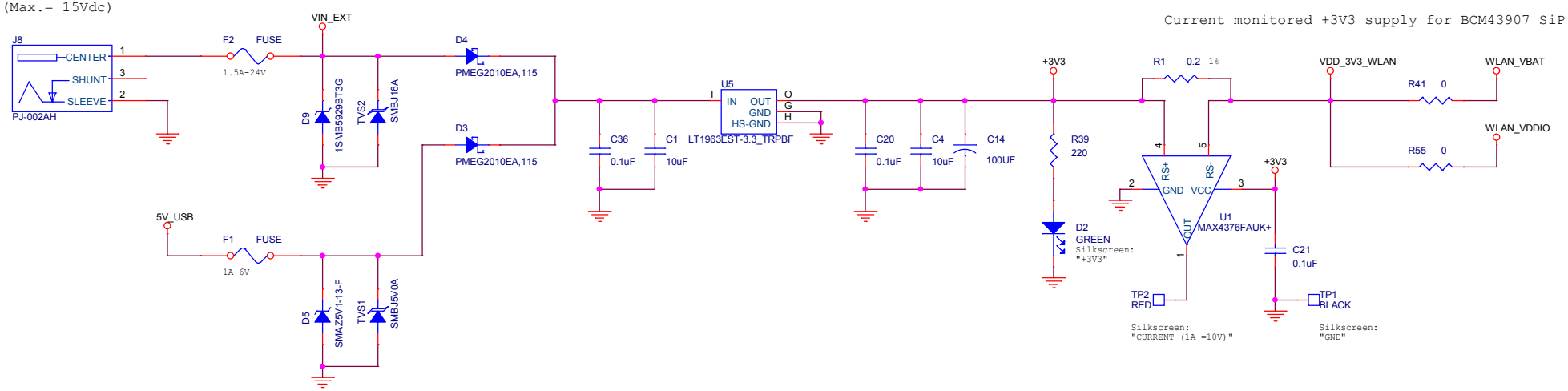
2.1mm DC Jack (centre pin positive)
Typ.= 5Vdc to 12Vdc
(Min.= 4.5Vdc)
(Max.= 15Vdc)

Current monitored +3V3 supply for BCM43907 SiP




**POWER**

| | | |
|---|---|---|
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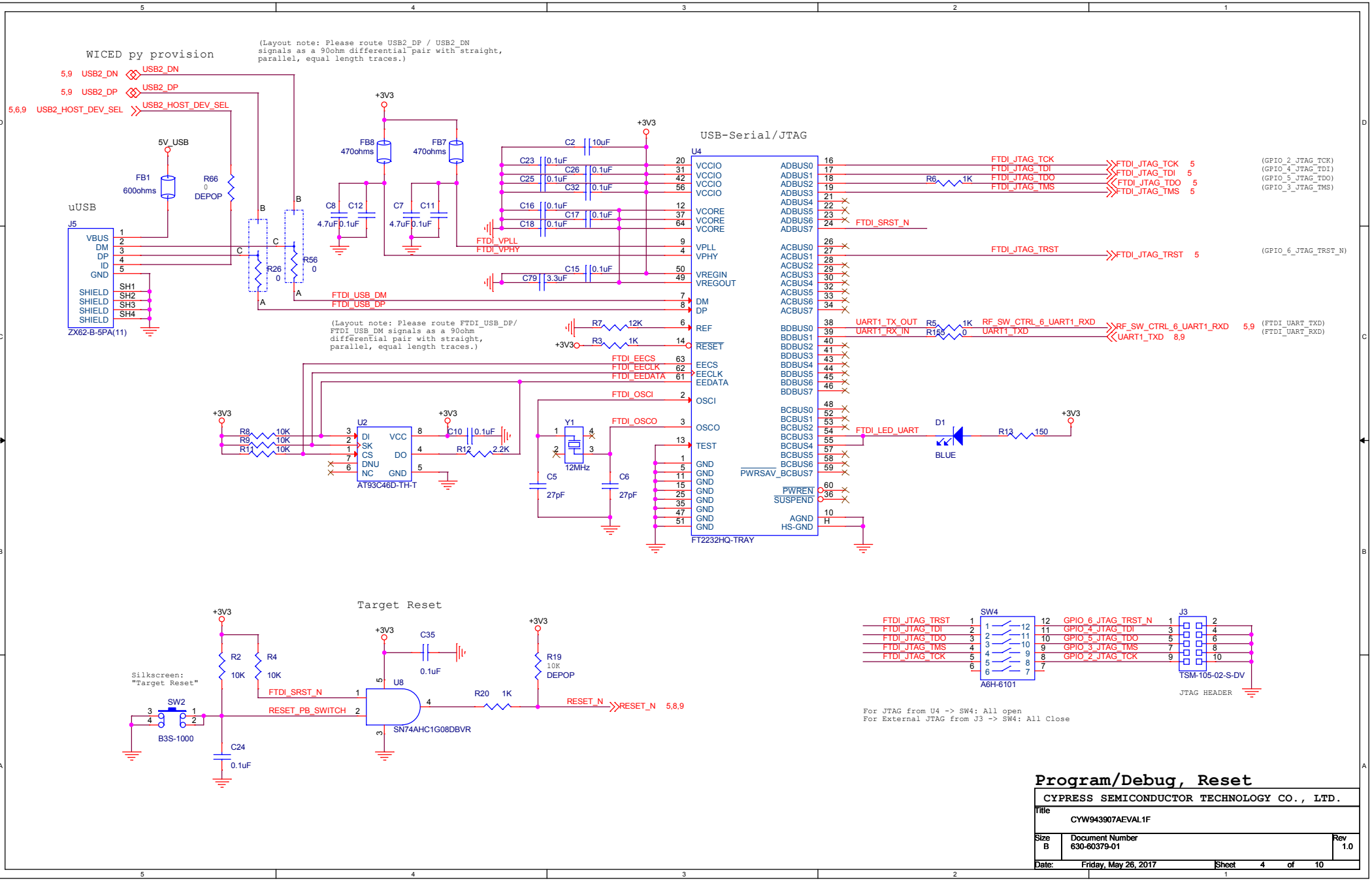
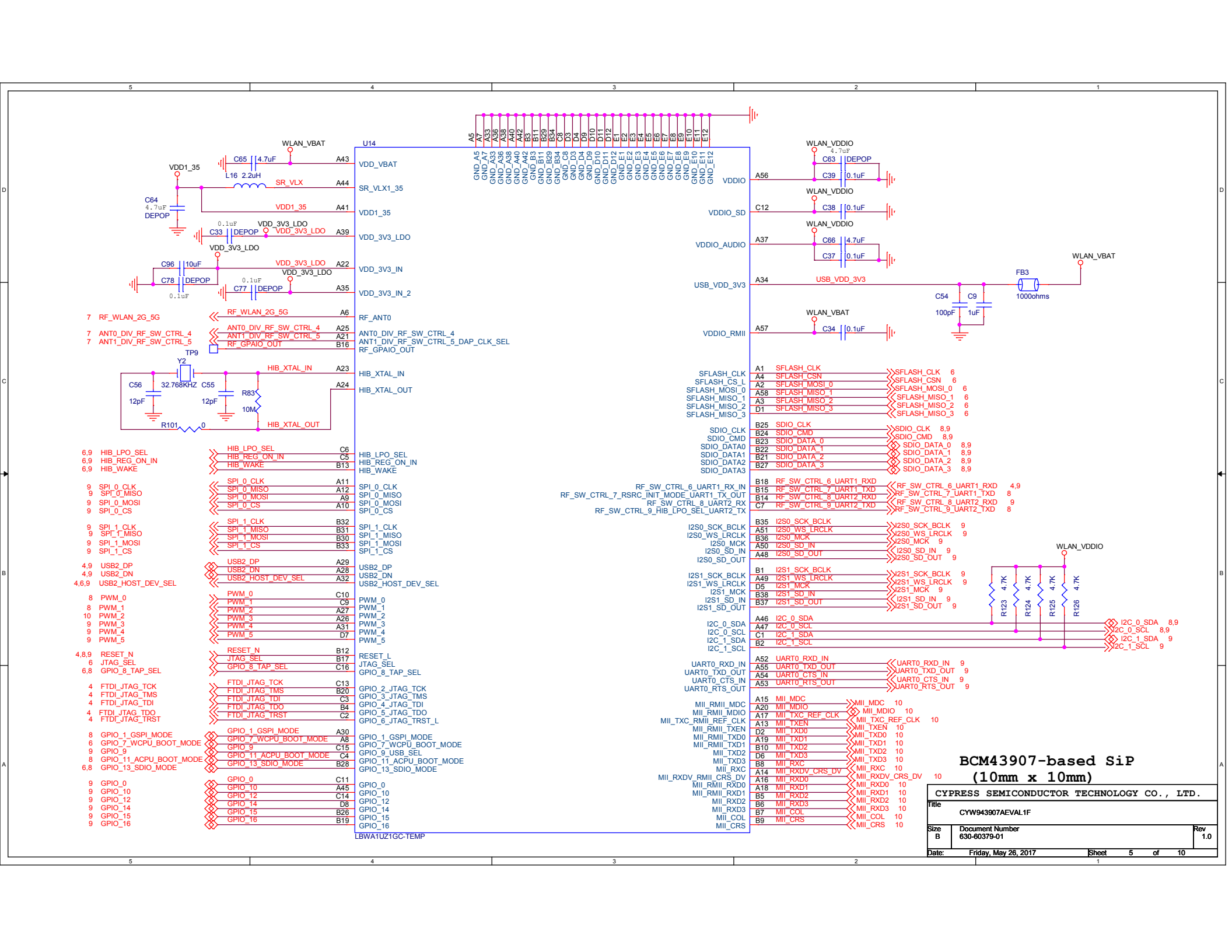

WICED py provision
(Layout note: Please route USB2_DP / USB2_DN signals as a 90ohm differential pair with straight, parallel, equal length traces.)
USB-Serial/JTAG
uUSB
ZX62-B-5PA(11)
FT2232HQ-TRAY
AT93C46D-TH-T
12MHz
BLUE
(Layout note: Please route FTDI_USB_DP/ FTDI_USB_DM signals as a 90ohm differential pair with straight, parallel, equal length traces.)
Target Reset
Silkscreen: "Target Reset"
B3S-1000
SN74AHC1G08DBVR
A6H-6101
TSM-105-02-S-DV
JTAG HEADER
For JTAG from U4 -> SW4: All open
For External JTAG from J3 -> SW4: All Close
Program/Debug, Reset
CYPRESS SEMICONDUCTOR TECHNOLOGY CO., LTD.
CYW943907AEVAL1F
630-60379-01
Friday, May 26, 2017


U14
WLAN_VBAT
VDD1_35
C65 4.7uF
L16 2.2uH
C64 4.7uF DEPOP
C33 0.1uF DEPOP
VDD_3V3_LDO
C96 10uF
C78 DEPOP
C77 0.1uF DEPOP
VDD_VBAT
SR_VLX
VDD1_35
VDD_3V3_LDO
VDD_3V3_IN
VDD_3V3_IN_2
RF_WLAN_2G_5G
ANT0_DIV_RF_SW_CTRL_4
ANT1_DIV_RF_SW_CTRL_5
RF_GPAIO_OUT
TP9
Y2
C56 12pF
32.768KHZ
C55 12pF
R83 10M
R101 0
HIB_XTAL_IN
HIB_XTAL_OUT
RF_ANT0
ANT0_DIV_RF_SW_CTRL_4
ANT1_DIV_RF_SW_CTRL_5_DAP_CLK_SEL
RF_GPAIO_OUT
HIB_XTAL_IN
HIB_XTAL_OUT
HIB_LPO_SEL
HIB_REG_ON_IN
HIB_WAKE
SPI_0_CLK
SPI_0_MISO
SPI_0_MOSI
SPI_0_CS
SPI_1_CLK
SPI_1_MISO
SPI_1_MOSI
SPI_1_CS
USB2_DP
USB2_DN
USB2_HOST_DEV_SEL
PWM_0
PWM_1
PWM_2
PWM_3
PWM_4
PWM_5
RESET_N
JTAG_SEL
GPIO_8_TAP_SEL
FTDI_JTAG_TCK
FTDI_JTAG_TMS
FTDI_JTAG_TDI
FTDI_JTAG_TDO
FTDI_JTAG_TRST
GPIO_1_GSPI_MODE
GPIO_7_WCPU_BOOT_MODE
GPIO_9
GPIO_11_ACPU_BOOT_MODE
GPIO_13_SDIO_MODE
GPIO_0
GPIO_10
GPIO_12
GPIO_14
GPIO_15
GPIO_16
GPIO_2_JTAG_TCK
GPIO_3_JTAG_TMS
GPIO_4_JTAG_TDI
GPIO_5_JTAG_TDO
GPIO_6_JTAG_TRST_L
GPIO_9_USB_SEL
GPIO_11_ACPU_BOOT_MODE
GPIO_13_SDIO_MODE
LBWA1UZ1GC-TEMP
GND_A5 GND_A7 GND_A33 GND_A36 GND_A38 GND_A40 GND_A42 GND_B3 GND_B11 GND_B29 GND_B34 GND_C8 GND_D3 GND_D4 GND_D9 GND_D10 GND_D11 GND_D12 GND_E1 GND_E2 GND_E3 GND_E4 GND_E5 GND_E6 GND_E7 GND_E8 GND_E9 GND_E10 GND_E11 GND_E12
VDDIO
VDDIO_SD
VDDIO_AUDIO
USB_VDD_3V3
VDDIO_RMII
WLAN_VDDIO
C63 DEPOP
C39 0.1uF
C12
C38 0.1uF
C66 4.7uF
C37 0.1uF
FB3 1000ohms
C54 100pF
C9 1uF
C34 0.1uF
WLAN_VBAT
USB_VDD_3V3
SFLASH_CLK
SFLASH_CS_L
SFLASH_MOSI_0
SFLASH_MISO_1
SFLASH_MISO_2
SFLASH_MISO_3
SDIO_CLK
SDIO_CMD
SDIO_DATA0
SDIO_DATA1
SDIO_DATA2
SDIO_DATA3
RF_SW_CTRL_6_UART1_RX_IN
RF_SW_CTRL_7_RSRC_INIT_MODE_UART1_TX_OUT
RF_SW_CTRL_8_UART2_RX
RF_SW_CTRL_9_HIB_LPO_SEL_UART2_TX
I2S0_SCK_BCLK
I2S0_WS_LRCLK
I2S0_MCK
I2S0_SD_IN
I2S0_SD_OUT
I2S1_SCK_BCLK
I2S1_WS_LRCLK
I2S1_MCK
I2S1_SD_IN
I2S1_SD_OUT
I2C_0_SDA
I2C_0_SCL
I2C_1_SDA
I2C_1_SCL
UART0_RXD_IN
UART0_TXD_OUT
UART0_CTS_IN
UART0_RTS_OUT
MII_RMII_MDC
MII_RMII_MDIO
MII_TXC_RMII_REF_CLK
MII_RMII_TXEN
MII_RMII_TXD0
MII_RMII_TXD1
MII_TXD2
MII_TXD3
MII_RXC
MII_RXDV_RMII_CRS_DV
MII_RMII_RXD0
MII_RMII_RXD1
MII_RXD2
MII_RXD3
MII_COL
MII_CRS
R123 4.7K
R124 4.7K
R125 4.7K
R126 4.7K
BCM43907-based SiP
(10mm x 10mm)
CYPRESS SEMICONDUCTOR TECHNOLOGY CO., LTD.
Title
CYW943907AEVAL1F
Size B
Document Number 630-60379-01
Rev 1.0
Date: Friday, May 26, 2017
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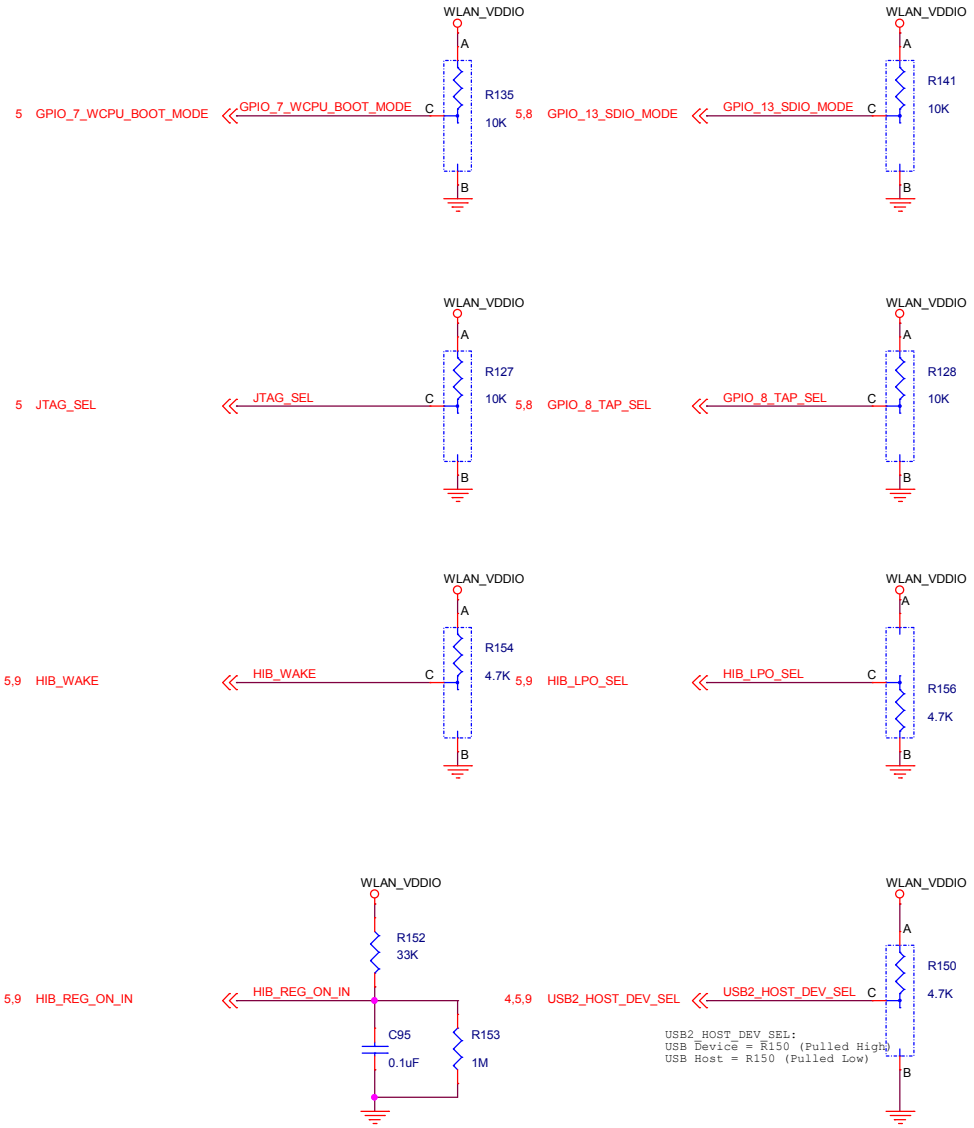
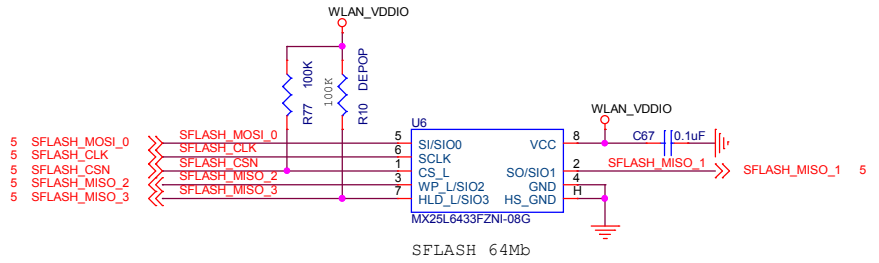



| Pin | Strap Function | Strap Pull | |
|---|---|---|---|
| | | Chip Default | Board Default |
| GPIO_1 | gSPI Mode | 0 | 0 |
| GPIO_7 | WCPU Boot Mode :<br>0 = TCROM Boot<br>1 = TCMSRAM Boot | 0 | 1<br>R135 = 10K to WLAN_VDDIO |
| GPIO_11 | ACPU Boot Mode :<br>0 = SOCROM Boot<br>1 = SOCSRAM Boot | 0 | 0 |
| GPIO_13 | SDIO Mode :<br>0 = SDIO Device<br>1 = SDIO Host | 0 | 1<br>R141= 10K to WLAN_VDDIO |
| GPIO_15 | (Note: GPIO_15 is not a strap option for B0 IC) | 0 | 0 |
| RF_SW_CTRL_5 | Host DAP Clock Sel | 0 | 0 |
| RF_SW_CTRL_7 | Host RSRC Init | 0 | 0 |
| RF_SW_CTRL_9 | LPO Sel:<br>0 = LPO from HIB<br>1 = Internal 32KHz LPO | 0 | 0 |

Note: There is no bootstrapping provision for GPIO_1, GPIO_11, GPIO_15, RF_SW_CTRL_5, RF_SW_CTRL_7, and RF_SW_CTRL_9 on this board.




# Bootstraps, Flash

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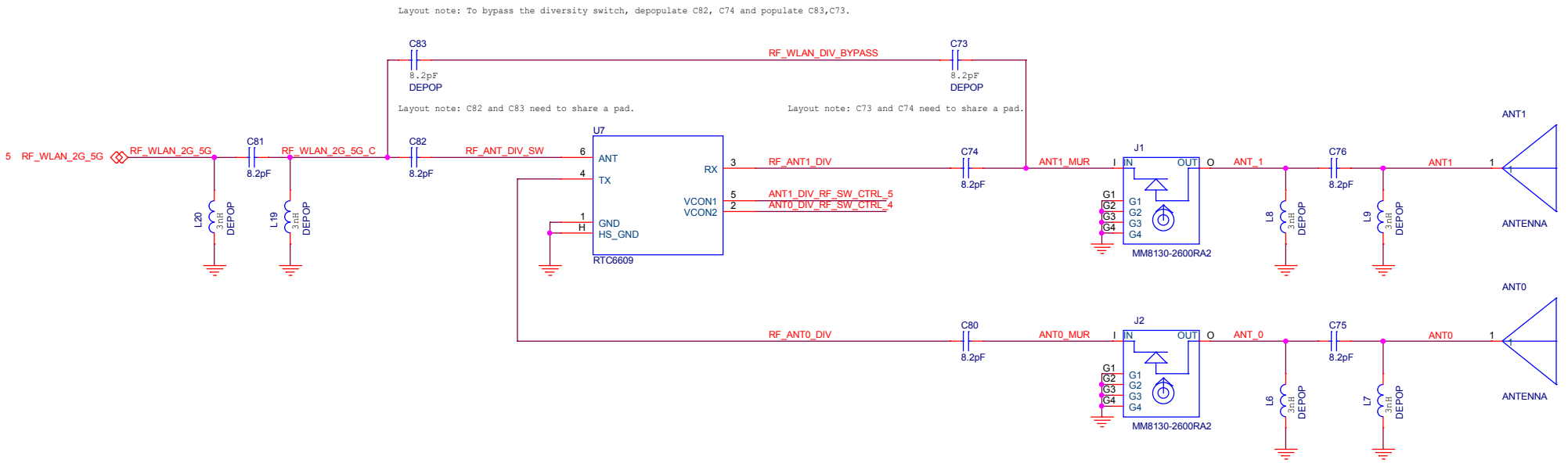


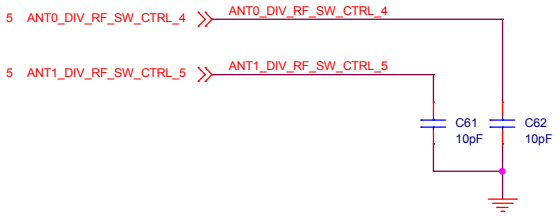


## U7 SPDT Is Optional Diversity Switch

| U7 SPDT WLAN Antenna Diversity Switch Control Table | | |
|---|---|---|
| MODE OF OPERATION<br>Ant Diversity | ANT0_DIV_RF_SW_CTRL_4<br>SPDT(U7 Pin2) | ANT1_DIV_RF_SW_CTRL_5<br>SPDT(U7 Pin5) |
| WLAN Ant0 | 1 | 0 |
| WLAN Ant1 | 0 | 1 |

ALL OTHER STATES UNDEFINED.

**RF**

CYPRESS SEMICONDUCTOR TECHNOLOGY CO., LTD.

| | | |
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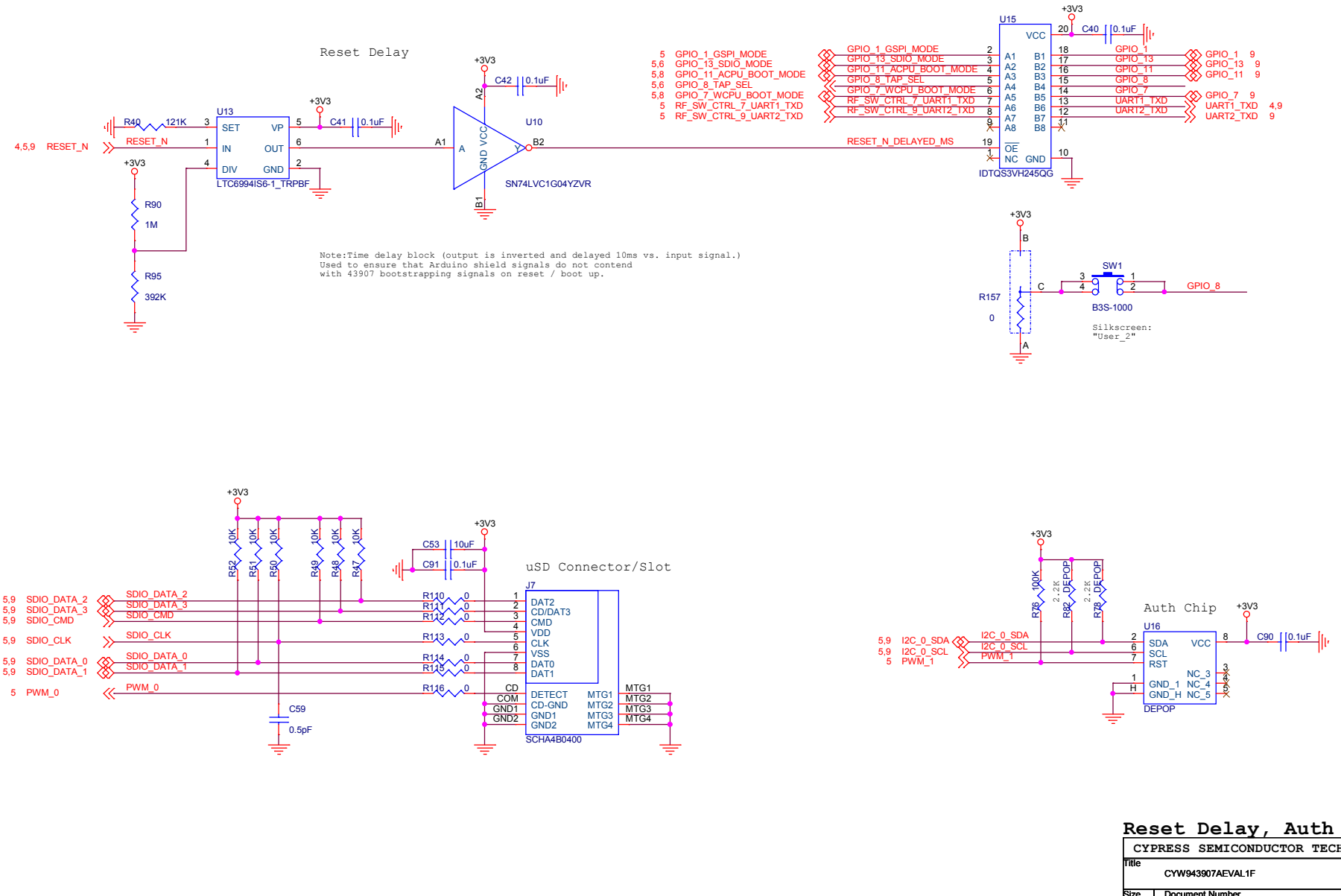


# Reset Delay, Auth IC, uSD

| | | |
|---|---|---|
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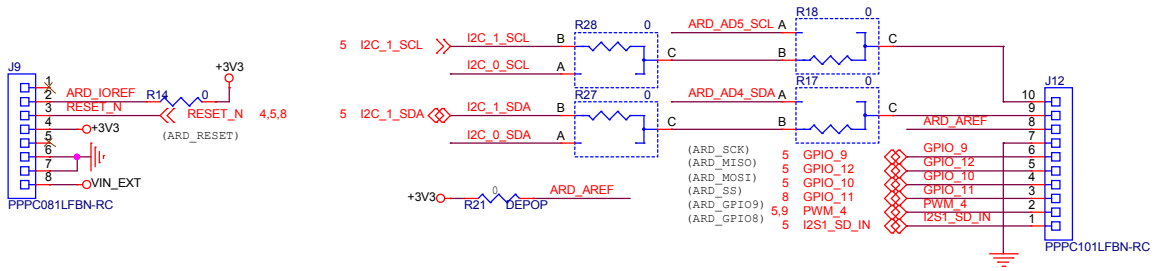
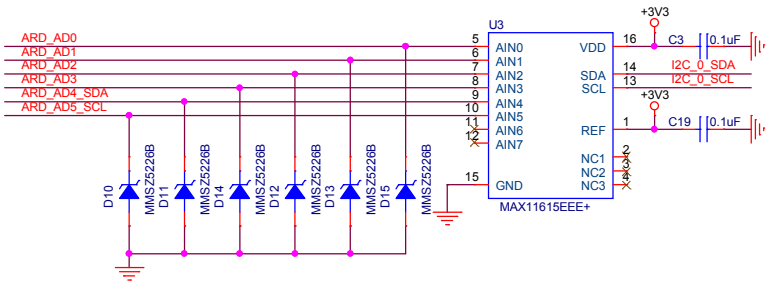
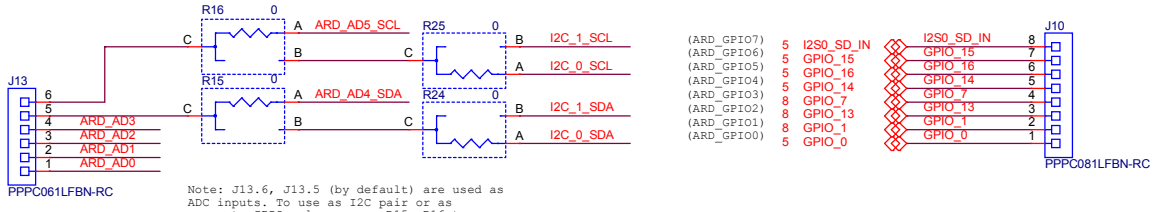
## Arduino-compatible Headers (+3V3 I/O only)

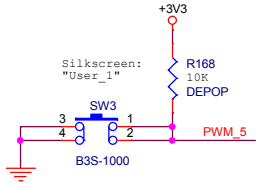


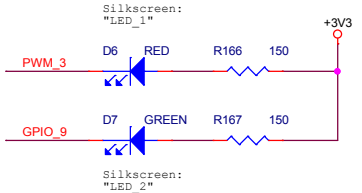

## External ADC




Note: J13.6, J13.5 (by default) are used as ADC inputs. To use as I2C pair or as separate GPIOs please move R15, R16 to position B-C.




Place acrylic feet at the corners (or as close to) of the board on the bottom layer.
Make sure they to not overlap the edge of the board.

F3

| NON PCB MOUNT PART |
|---|
| RUBBER,FEET,9.5X3.8mm,ACRYLIC TRANSPARENT |

SJ5306

F4

| NON PCB MOUNT PART |
|---|
| RUBBER,FEET,9.5X3.8mm,ACRYLIC TRANSPARENT |

SJ5306

F5

| NON PCB MOUNT PART |
|---|
| RUBBER,FEET,9.5X3.8mm,ACRYLIC TRANSPARENT |

SJ5306

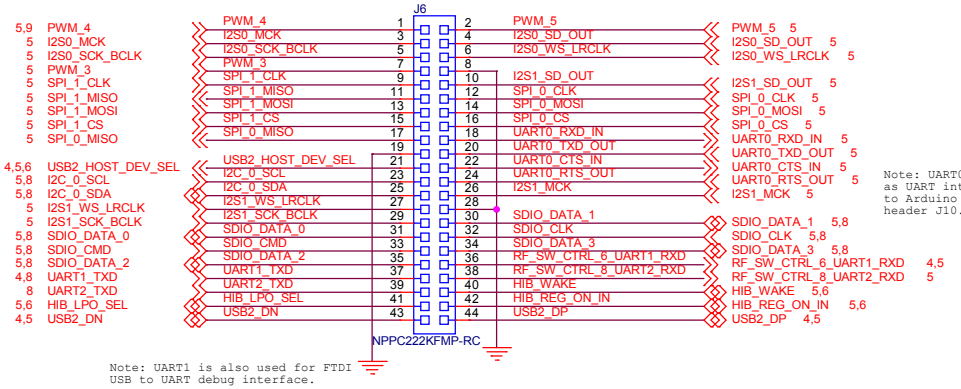
F6

| NON PCB MOUNT PART |
|---|
| RUBBER,FEET,9.5X3.8mm,ACRYLIC TRANSPARENT |

SJ5306

## WICED Header (+3V3 I/O only)

Silkscreen:
"WICED HEADER (+3V3 ONLY)"




Note: UART1 is also used for FTDI USB to UART debug interface.

Note: UART0 Tx/Rx may also be used as UART interface to Arduino shields via Arduino header J10.1, J10.2

ZJ1

| NON PCB MOUNT PART |
|---|
| CBL,USB-A/MICROUSB-B,M/M,2ft,4/5P DATA CABLE,BROADPEBBLE |

99-110080-0001

# WICED/Arduino Headers, ADC

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| | | |
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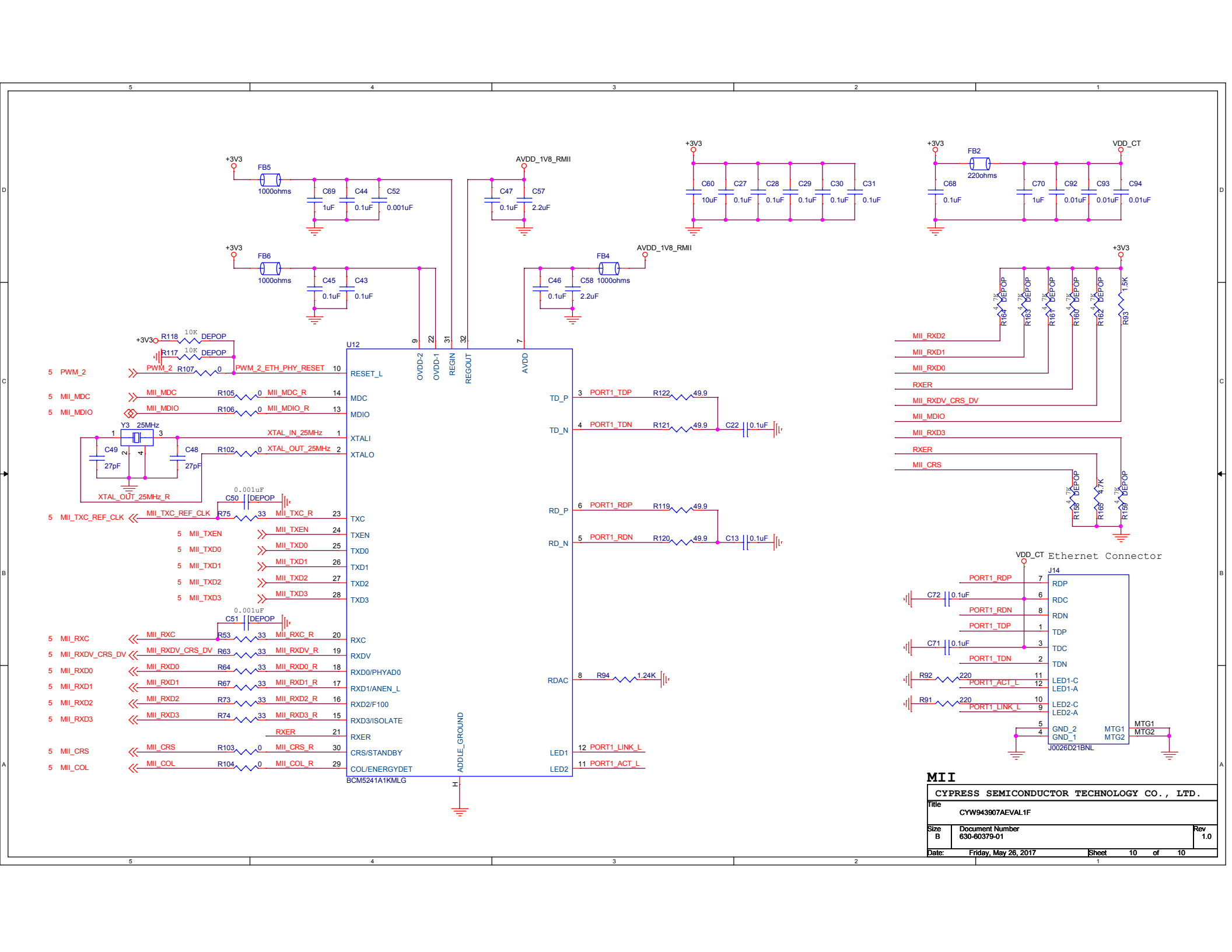


# MII

| | | |
|---|---|---|
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