Hydra rev0 SPI register definition:

Register Address		msb 7	6	5	4	3	2	1	lsb 0	comments
0	0	manufacturer ID (8 bits)								read-only
	1	product ID (8 bits)								read-only
1	0	*reserved*		ringosc_freq_sel		power-on status				lower 4 bits read-only
2	0	DAC0_value[7:0]								
	1	*reserved*			enable_ DAC0	DAC0_value[11:8]				
	2	DAC1_value[7:0]								
	3	*reserved*			enable_ DAC1	DAC1_value[11:8]				
3	0	ADC0_value[7:0]								read-only
	1	ADC0_input_select				ADC0_value[11:8]				lower 4 bits read-only
	2	*reserved*				ADC0_vref_select		run_ ADC0	enable_ ADC0	
	3	ADC1_value[7:0]								read-only
	4	ADC1_input_select				ADC1_value[11:8]				lower 4 bits read-only
	5	*reserved*				ADC1_vref_select		run_ ADC1	enable_ ADC1	
4	0	bandgap_trim				Vref0_value			enable_ Vref0	
	1	*reserved*				Vref1_value			enable_ Vref1	
5	0	*reserved*				LDO0_value			enable_ LDO0	
	1	*reserved*				LDO1_value			enable_ LDO1	
6	0	*reserved*				Iref0_value			enable_ Iref0	
	1	*reserved*				Iref1_value			enable_ Iref1	

SPI protocol definition

All input is in groups of 8 bits. Each byte is input msb first.

CSB pin must be low to enable an SPI transmission. Data are clocked by pin SCK, with data valid on the rising edge of SCK. Output data are received on the SDO line. SDO is held high-impedance when CSB is high. SDO outputs become active on the falling edge of SCK. SPI definition allows this to be changed to SDO active on the rising edge of SCK by applying a command word to the SPI (see below).

After CSB is set low, the SPI is always in the "idle" state, awaiting a new command.

The first byte of a command always comprises 4 bits of a command word in the lower four bits. The upper four bits are command-dependent.

Depending on the command word, the command byte may be followed by one byte, two bytes, a number of bytes equal to the size in bytes of the addressed register, or (in streaming modes) an arbitrary number of bytes.

All commands except streaming modes (read, write, and read/write) end after a predetermined number of bytes. Streaming modes end only after the end of the address space has been reached, or the CSB pin is pulled high.

The address space is divided into registers and bytes. Registers are numbered 0 to 15 and are addressed by the upper four bits of commands that require a register address, Each register defines an arbitrarily large number of bytes, which are numbered from zero up, and are accessed in series from position zero. Commands that specify only a register value will read to, or write from, the entire register beginning at the first byte and continuing to the last defined byte. After the last defined byte has been read or written, the SPI returns to the idle state.

For all read, write, and read/write commands, the address auto-increments by one for each byte read or written (i.e., every 8 SCK cycles). In streaming modes, the address space is continuous, with the first byte of each register occupying the address following the last byte of the previous register.

For streaming mode commands, an additional byte is sent after the command/register byte, specifying a byte offset position in the register at which to begin reading and/or writing data. If this byte is value 255 (all ones), then it is followed by an additional byte, and the starting byte offset address is the addition of both values.

The 4-bit command words defined by the protocol are as follows:

Table 1: Command words

0000	No operation
0001	Write
0010	Read
0011	Simultaneous Read/Write
0100	Device reset
0101	Write, 12-bit address
0110	Read, 12-bit address
0111	Simultaneous Read/Write, 12-bit address
1000	Query register length
1001	Address offset Read/Write
1010	Device program (if applicable)
1011	Device standby (if implemented)
1100	SPI protocol flags
1101	*Reserved*
1110	*Reserved*
1111	Extended command protocol (device-dependent)

Description of SPI commands

No operation:	XX000000	Address field is ignored. Command is one byte only. SPI returns to idle. Upper two bits are always ignored.
SDO timing:	00ss0000	Defines signal timing for SDO. If ss = 01, then SDO is valid on SCK falling edge (default). If ss = 10, then SDO is valid on SCK rising edge. Behavior remains in effect until a power-cycle or another SDO timing command.
Write:	AAAA0001 dddddddd dddddddd ⋮ dddddddd	Address is 4 bits and defines a major address. Data are passed in the following bytes, up to the defined length of the register. Register lengths are device-dependent. At the end of data, the SPI returns to idle.
Read:	AAAA0010 XXXXXXXX XXXXXXXX ⋮ XXXXXXXX	Address is 4 bits and defines a major address. Data on SDI following the address/command byte are ignored. For each 8 bits clocked through SCK, register data are returned in SDO, up to the defined length of the register. Register lengths are device-dependent. At the end of data, the SPI returns to idle.
Simultaneous Read/Write:	AAAA0011 dddddddd dddddddd ⋮ dddddddd	Combines the read and write functions. Existing register data are output to SDO, while new data are read by the slave from SDI and applied to the register.
Device reset:	00000100	The implementation of a hard reset is device-dependent, but generally will force the device to the initial power-up state.
Special reset:	pppp0100	The device may define device-dependent specific reset states pppp = 1 to 14
Write, 12-bit address:	AAAA0101 aaaaaaaa dddddddd dddddddd ⋮ dddddddd	This mode of addressing accesses registers by byte. The major address is given by AAAA and corresponds to the same major address used by the standard Read/Write commands. The minor address aaaaaaaa gives a byte offset from the beginning of register AAAA and may be used to write to a portion of a register. The write does not terminate at the end of the register, but continues into the following register address. Transmission is terminated by raising the CSB pin, or at the end of all defined register data. If aaaaaaaa is 255, then an additional byte follows containing further address data, and the sum of the address bytes indicates the starting offset position. Read, 12-bit address and Read/Write, 12-bit address operate equivalently to their 4-bit address counterparts as does the Write, 12-bit address command.
Query register length:	AAAA1000 XXXXXXXX (XXXXXXXX) ⋮	Query the length of the register (number of bytes) at major address AAAA. This byte is followed by one byte of output on SDO. The value on SDI following the command/register byte is ignored. A return value of 00000000 indicates that the register does not exist. If the register contains more than 254 bytes, then the value 11111111 is returned, and there will be an additional byte following. At the end of the transmission, the sum of the returned bytes is the register byte length.
Address offset read/write:	AAAA1001 BBBBxxxx dddddddd dddddddd ⋮ dddddddd	This optional command (which may or may not be implemented by the device) operates like the standard simultaneous Read/Write command. However, it takes an additional input byte defining register BBBB. Values written to the device will be applied to register AAAA, while values read from the device will be read from register BBBB. If register AAAA is longer than register BBBB, then values past the end of BBBB are read as zero. If register BBBB is longer than register AAAA, then values past the end of register AAAA are ignored. If BBBB is equal to AAAA, then an additional byte aaaaaaaa specifies a byte offset within the same register. Like the other commands specifying a byte address, a value of 255 indicates an additional address offset byte following.
Device program:	pppp1010	If a device has non-volatile memory storage, then this command is a request to program the device memory. The device may implement additional commands in field pppp
Device standby:	00001011	This command puts the device into standby mode, in which all onboard functions are powered down and only the SPI remains active.
Device active:	11111011	This command restores the active state of a device that has been placed into standby.
Device power modes:	pppp1011	The device may optionally define device-dependent power states 1 to 14.
SPI protocol flags:	00001100	The device returns two bytes indicating which of the commands 0 through 15 are implemented by the device. Each bit is set to 1 if the corresponding SPI protocol 4-bit command is implemented, 0 if it is not. The first byte returned corresponds to commands 0 to 7; the second byte, commands 8 to 15.
Command protocol flags:	cccc1100	For specific 4-bit command cccc, the device returns two bytes indicating which of the sub-commands 0 through 15 are implemented by the device. For example, "01001100" requests the list of special resets implemented by the device. If the device returns "00000011, 00000000", then two reset commands are implemented, command "00000100" (device reset), and "00010100" (special reset, device-dependent).
Extended command protocol:	pppp1111	A device may arbitrarily extend the SPI protocol by defining additional commands in the field pppp of command 1111. The number of bytes following the command is device-dependent.

Hydra block diagram