1. Description

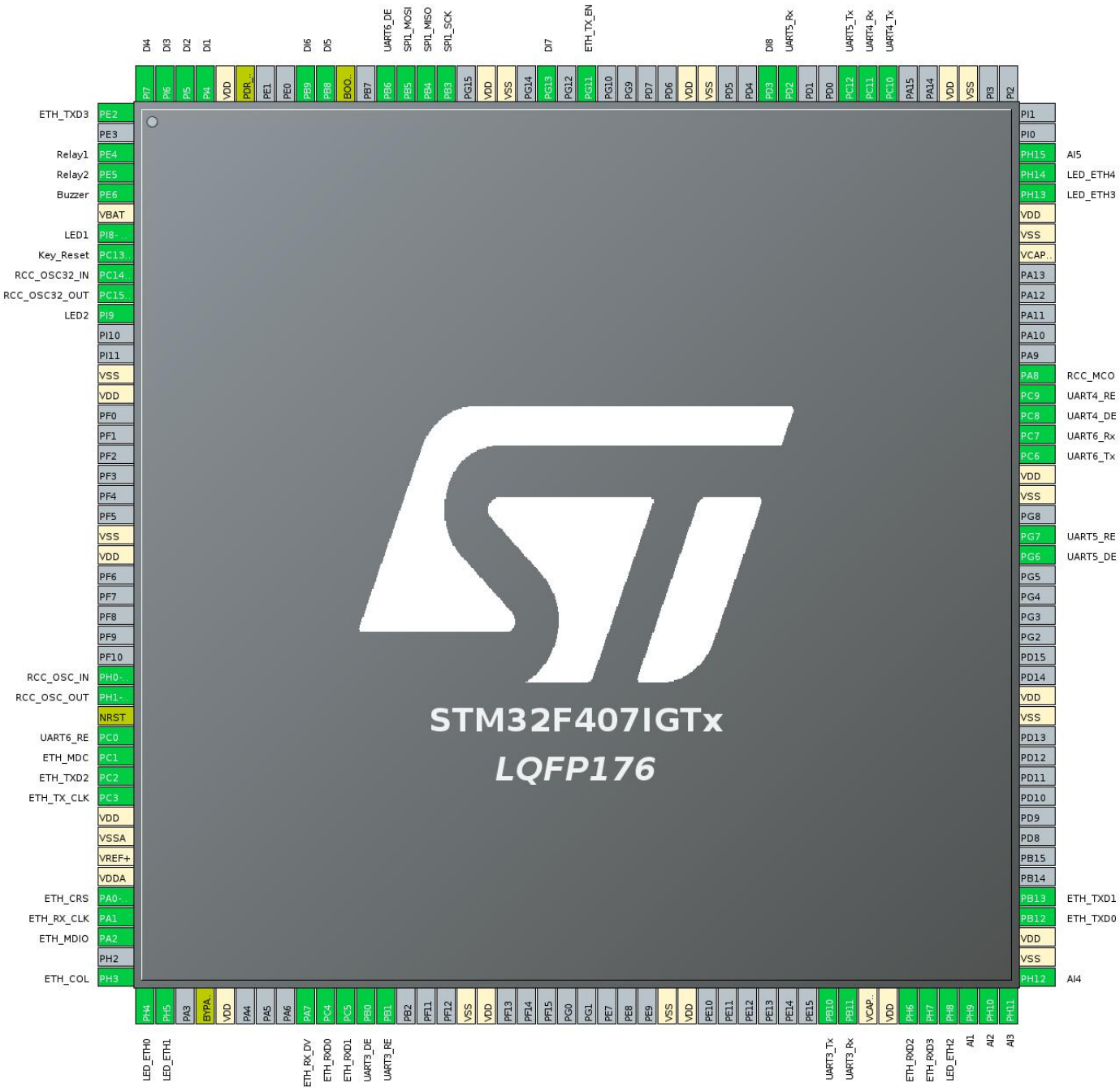
1.1. Project

Project Name	iota2_hub
Board Name	custom
Generated with:	STM32CubeMX 5.3.0
Date	09/20/2019

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407IGTx
MCU Package	LQFP176
MCU Pin number	176

2. Pinout Configuration



3. Pins Configuration

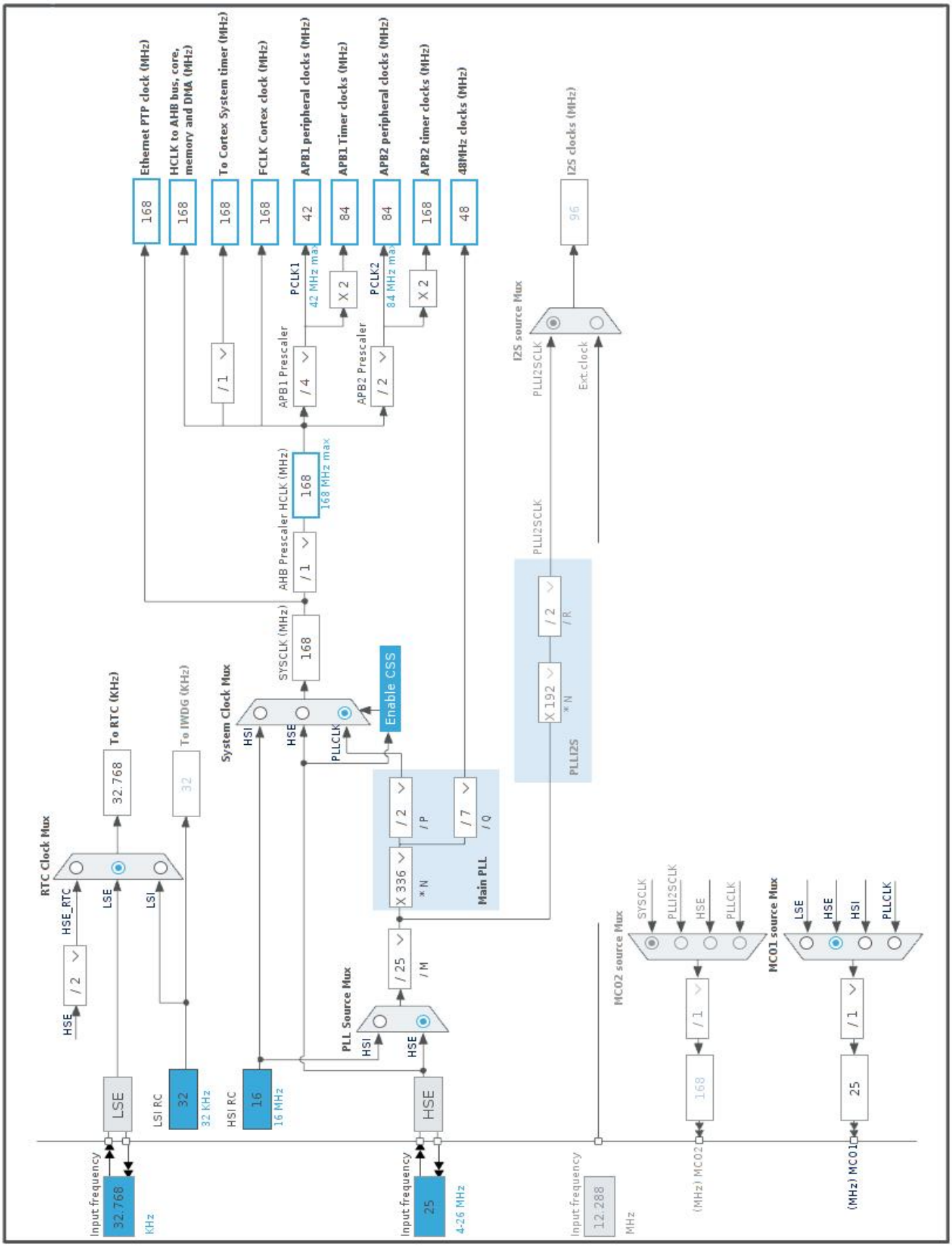
Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	ETH_TXD3	ETH_TXD3
3	PE4 *	I/O	GPIO_Output	Relay1
4	PE5 *	I/O	GPIO_Output	Relay2
5	PE6 *	I/O	GPIO_Output	Buzzer
6	VBAT	Power		
7	PI8- ANTI TAMP2 *	I/O	GPIO_Output	LED1
8	PC13-ANTI_TAMP *	I/O	GPIO_Input	Key_Reset
9	PC14-OSC32_IN	I/O	RCC_OSC32_IN	RCC_OSC32_IN
10	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	RCC_OSC32_OUT
11	PI9 *	I/O	GPIO_Output	LED2
14	VSS	Power		
15	VDD	Power		
22	VSS	Power		
23	VDD	Power		
29	PH0-OSC_IN	I/O	RCC_OSC_IN	RCC_OSC_IN
30	PH1-OSC_OUT	I/O	RCC_OSC_OUT	RCC_OSC_OUT
31	NRST	Reset		
32	PC0 *	I/O	GPIO_Output	UART6_RE
33	PC1	I/O	ETH_MDC	ETH_MDC
34	PC2	I/O	ETH_TXD2	ETH_TXD2
35	PC3	I/O	ETH_TX_CLK	ETH_TX_CLK
36	VDD	Power		
37	VSSA	Power		
38	VREF+	Power		
39	VDDA	Power		
40	PA0-WKUP	I/O	ETH_CRS	ETH_CRS
41	PA1	I/O	ETH_RX_CLK	ETH_RX_CLK
42	PA2	I/O	ETH_MDIO	ETH_MDIO
44	PH3	I/O	ETH_COL	ETH_COL
45	PH4 *	I/O	GPIO_Output	LED_ETH0
46	PH5 *	I/O	GPIO_Output	LED_ETH1
48	BYPASS_REG	Reset		
49	VDD	Power		
53	PA7	I/O	ETH_RX_DV	ETH_RX_DV
54	PC4	I/O	ETH_RXD0	ETH_RXD0
55	PC5	I/O	ETH_RXD1	ETH_RXD1

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
56	PB0 *	I/O	GPIO_Output	UART3_DE
57	PB1 *	I/O	GPIO_Output	UART3_RE
61	VSS	Power		
62	VDD	Power		
71	VSS	Power		
72	VDD	Power		
79	PB10	I/O	USART3_TX	UART3_Tx
80	PB11	I/O	USART3_RX	UART3_Rx
81	VCAP_1	Power		
82	VDD	Power		
83	PH6	I/O	ETH_RXD2	ETH_RXD2
84	PH7	I/O	ETH_RXD3	ETH_RXD3
85	PH8 *	I/O	GPIO_Output	LED_ETH2
86	PH9 *	I/O	GPIO_Analog	AI1
87	PH10 *	I/O	GPIO_Analog	AI2
88	PH11 *	I/O	GPIO_Analog	AI3
89	PH12 *	I/O	GPIO_Analog	AI4
90	VSS	Power		
91	VDD	Power		
92	PB12	I/O	ETH_TXD0	ETH_TXD0
93	PB13	I/O	ETH_TXD1	ETH_TXD1
102	VSS	Power		
103	VDD	Power		
110	PG6 *	I/O	GPIO_Output	UART5_DE
111	PG7 *	I/O	GPIO_Output	UART5_RE
113	VSS	Power		
114	VDD	Power		
115	PC6	I/O	USART6_TX	UART6_Tx
116	PC7	I/O	USART6_RX	UART6_Rx
117	PC8 *	I/O	GPIO_Output	UART4_DE
118	PC9 *	I/O	GPIO_Output	UART4_RE
119	PA8	I/O	RCC_MCO_1	RCC_MCO
125	VCAP_2	Power		
126	VSS	Power		
127	VDD	Power		
128	PH13 *	I/O	GPIO_Output	LED_ETH3
129	PH14 *	I/O	GPIO_Output	LED_ETH4
130	PH15 *	I/O	GPIO_Analog	AI5
135	VSS	Power		

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
136	VDD	Power		
139	PC10	I/O	UART4_TX	UART4_Tx
140	PC11	I/O	UART4_RX	UART4_Rx
141	PC12	I/O	UART5_TX	UART5_Tx
144	PD2	I/O	UART5_RX	UART5_Rx
145	PD3 *	I/O	GPIO_Output	DI8
148	VSS	Power		
149	VDD	Power		
154	PG11	I/O	ETH_TX_EN	ETH_TX_EN
156	PG13 *	I/O	GPIO_Output	DI7
158	VSS	Power		
159	VDD	Power		
161	PB3	I/O	SPI1_SCK	SPI1_SCK
162	PB4	I/O	SPI1_MISO	SPI1_MISO
163	PB5	I/O	SPI1_MOSI	SPI1_MOSI
164	PB6 *	I/O	GPIO_Output	UART6_DE
166	BOOT0	Boot		
167	PB8 *	I/O	GPIO_Output	DI5
168	PB9 *	I/O	GPIO_Output	DI6
171	PDR_ON	Reset		
172	VDD	Power		
173	PI4 *	I/O	GPIO_Output	DI1
174	PI5 *	I/O	GPIO_Output	DI2
175	PI6 *	I/O	GPIO_Output	DI3
176	PI7 *	I/O	GPIO_Output	DI4

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	iota2_hub
Project Folder	/home/naval/HUB_CLONED/naval/iota2-hub/tools/mcu_configuration
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F4 V1.24.1

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407IGTx
Datasheet	022152_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. CRC

mode: Activated

7.2. ETH

Mode: MII

7.2.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	1

Ethernet Basic Configuration:

Rx Mode	Polling Mode
TX IP Header Checksum Computation	By hardware

7.2.2. Advanced Parameters:

External PHY Configuration:

PHY	DP83848_PHY_ADDRESS
PHY Address Value	1
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***

Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x1F ***
MII Interrupt Control Register	**0x11 ***
MII Interrupt Status and Misc. Control Register	**0x12 ***
PHY Link mask	**0x0001 ***
PHY Speed mask	**0x0004 ***
PHY Duplex mask	**0x0010 ***
PHY Enable interrupts	**0x0002 ***
PHY Enable output interrupt events	**0x0001 ***
Enable Interrupt on change of link status	**0x0020 ***
PHY link status interrupt mask	**0x2000 ***

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator
Low Speed Clock (LSE) : Crystal/Ceramic Resonator
mode: Master Clock Output 1

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

7.4. RNG

mode: Activated

7.5. RTC

mode: Activate Clock Source

7.5.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

7.6. SPI1

Mode: Full-Duplex Master

7.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**42.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.7. SYS

Timebase Source: SysTick

7.8. UART4

Mode: Asynchronous

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.9. UART5

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.10. USART3

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.11. USART6

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.12. FREERTOS

Interface: CMSIS_V1

7.12.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.0.1
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	**5 ***
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	**Disabled ***
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	**Enabled ***

QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

7.12.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled

xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ETH	PE2	ETH_TXD3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_TXD3
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_MDC
	PC2	ETH_TXD2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_TXD2
	PC3	ETH_TX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_TX_CLK
	PA0-WKUP	ETH_CRS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_CRS
	PA1	ETH_RX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_RX_CLK
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_MDIO
	PH3	ETH_COL	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_COL
	PA7	ETH_RX_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_RX_DV
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_RXD0
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_RXD1
	PH6	ETH_RXD2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_RXD2
	PH7	ETH_RXD3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_RXD3
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_TXD0
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_TXD1
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_TX_EN
RCC	PC14-	RCC_OSC32_IN	n/a	n/a	n/a	RCC_OSC32_IN

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	OSC32_IN					
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	RCC_OSC32_OUT
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	RCC_OSC_IN
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	RCC_OSC_OUT
	PA8	RCC_MCO_1	Alternate Function Push Pull	No pull-up and no pull-down	Low	RCC_MCO
SPI1	PB3	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI1_SCK
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI1_MISO
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI1_MOSI
UART4	PC10	UART4_TX	Alternate Function Push Pull	Pull-up	**Very High ***	UART4_Tx
	PC11	UART4_RX	Alternate Function Push Pull	Pull-up	**Very High ***	UART4_Rx
UART5	PC12	UART5_TX	Alternate Function Push Pull	Pull-up	**Very High ***	UART5_Tx
	PD2	UART5_RX	Alternate Function Push Pull	Pull-up	**Very High ***	UART5_Rx
USART3	PB10	USART3_TX	Alternate Function Push Pull	Pull-up	**Very High ***	UART3_Tx
	PB11	USART3_RX	Alternate Function Push Pull	Pull-up	**Very High ***	UART3_Rx
USART6	PC6	USART6_TX	Alternate Function Push Pull	Pull-up	**Very High ***	UART6_Tx
	PC7	USART6_RX	Alternate Function Push Pull	Pull-up	**Very High ***	UART6_Rx
GPIO	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay1
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay2
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Buzzer
	PI8- ANTI TAMP2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PC13-ANTI_TAMP	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Key_Reset
	PI9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UART6_RE
	PH4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_ETH0
	PH5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_ETH1
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UART3_DE
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UART3_RE
	PH8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_ETH2
	PH9	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	AI1
	PH10	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	AI2
	PH11	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	AI3
	PH12	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	AI4
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UART5_DE
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UART5_RE
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UART4_DE
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UART4_RE
	PH13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_ETH3
	PH14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_ETH4
	PH15	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	AI5
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DI8
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DI7
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UART6_DE
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DI5
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DI6
	PI4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DI1
	PI5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DI2
	PI6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DI3
	PI7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DI4

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_RX	DMA2_Stream2	Peripheral To Memory	Low
SPI1_TX	DMA2_Stream3	Memory To Peripheral	Low

SPI1_RX: DMA2_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI1_TX: DMA2_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
UART4 global interrupt	true	5	0
DMA2 stream2 global interrupt	true	5	0
DMA2 stream3 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
SPI1 global interrupt	unused		
USART3 global interrupt	unused		
UART5 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
USART6 global interrupt	unused		
HASH and RNG global interrupts	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report