

1 2 3 4 5 6 7 8

A A

# AD7190

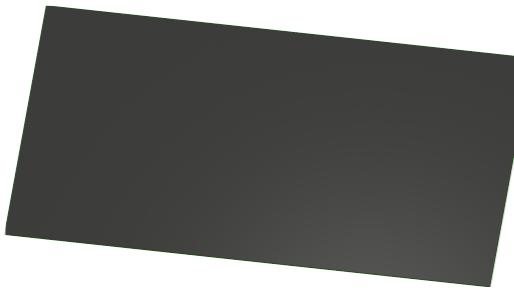
## Variant: DRAFT

2026-02-24

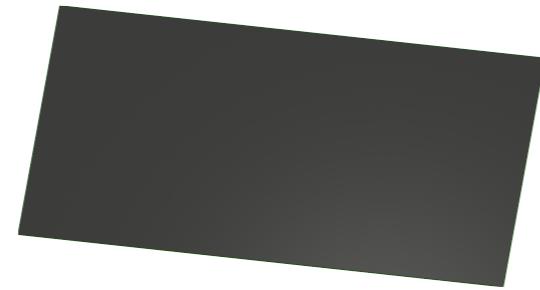
## Rev + (Unreleased)

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### TOP VIEW



### BOTTOM VIEW



### NOTES

Comment

Not fitted components are marked as

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There shouldn't be any mistakes. Contact the engineer if you find any.

RELEASED - A board with this schematic has been sent to production.

Date: 24-Feb-2026

### DESIGN CONSIDERATIONS

DESIGN NOTE:  
Example text for informational design notes.

DESIGN NOTE:  
Example text for debug notes.

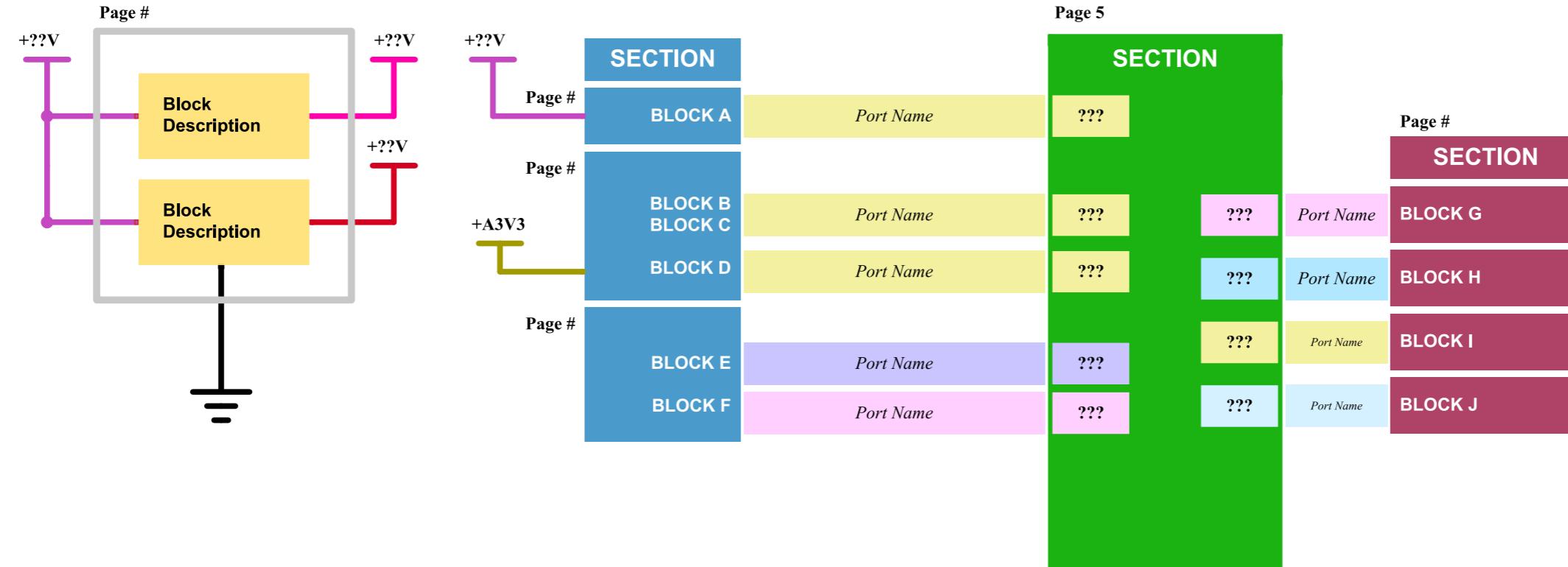
DESIGN NOTE:  
Example text for cautionary design notes.

DESIGN NOTE:  
Example text for critical design notes.

LAYOUT NOTE:  
Example text for critical layout guidelines.

	Comments:	Company: <b>OPEN_TRUST_LAB</b>	Variant: <b>DRAFT</b>	Git Hash: <b>f2c7d09</b>
	Board Name: <b>AD7190</b>	Project Name: <b>OPEN_WEIGHT</b>		
	Sheet Title: File Name: <b>Cellule_de_force_V2.kicad_sch</b>	Designer: <b>SIEBERT DIMITRY</b>	Date: <b>2025-01-12</b>	Revision: <b>+ (Unreleased)</b>
	Sheet Path: <b>/</b>	Reviewer:	Size: <b>A3</b>	Sheet: <b>1 of 10</b>

# [2] Block Diagram

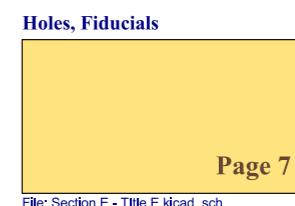
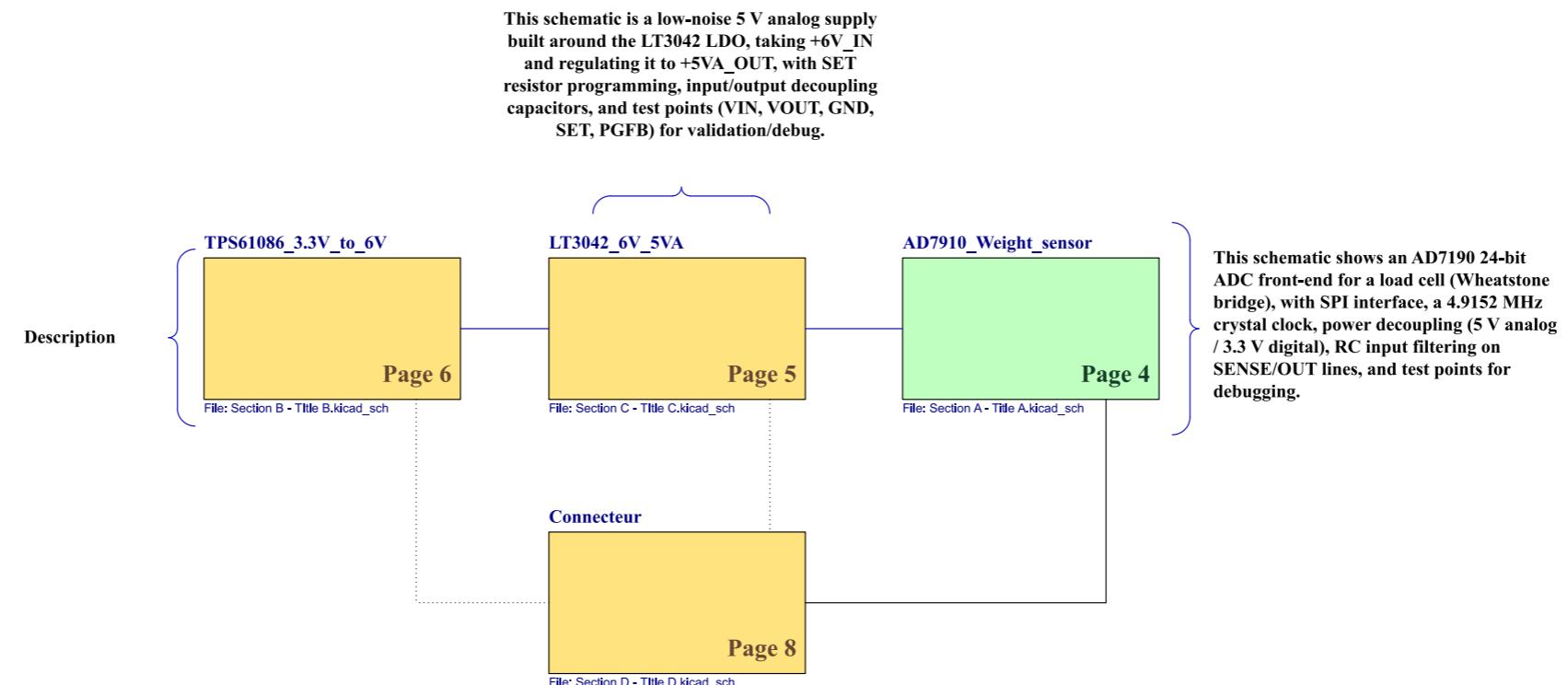


## Target specifications:

<b>Input voltage:</b>	<b>?? - ?? V</b>
<b>Spec 2</b>	<b>??</b>
<b>Spec 3</b>	<b>??</b>
<b>Spec 4</b>	<b>??</b>

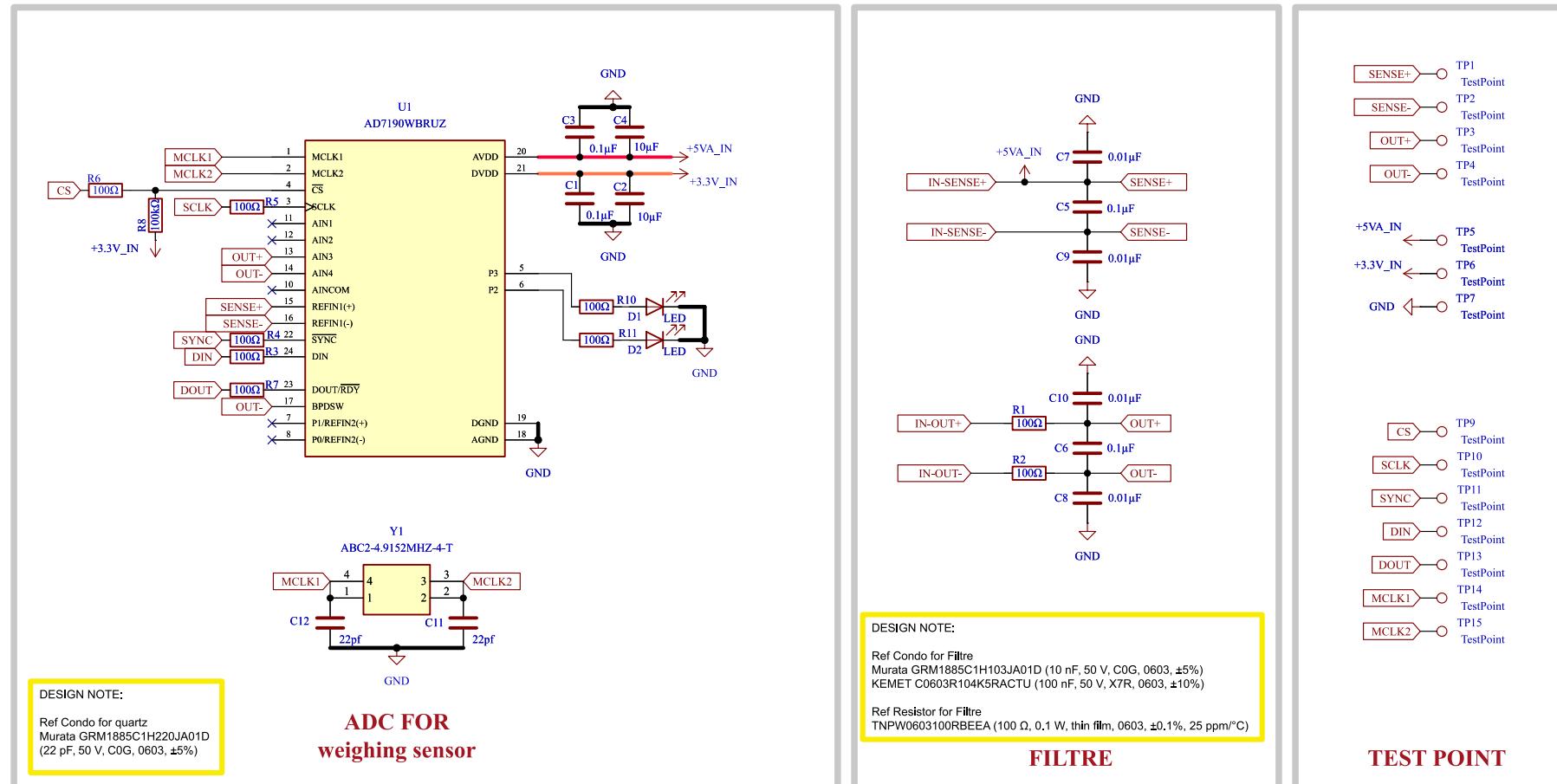
	<b>Comments:</b>	<b>Company:</b>	<b>Variant:</b>	
		<b>OPEN_TRUST_LAB</b>	<b>DRAFT</b>	f2c7d09
	<b>Board Name:</b>	<b>AD7190</b>	<b>Project Name:</b>	<b>OPEN_WEIGHT</b>
	<b>Sheet Title:</b>	<b>File Name:</b>	<b>Designer:</b>	<b>Date:</b>
	Block Diagram	Block Diagram.kicad_sch	SIEBERT DIMITRY	2025-01-12 + (Unreleased)
	<b>Sheet Path:</b>	<b>Reviewer:</b>		<b>Revision:</b>
	/Block Diagram/			
	<b>Size:</b>	<b>Sheet:</b>		
	<b>A3</b>	<b>2 of 10</b>		

# [3] Project Architecture



Comments:	Company: <b>OPEN_TRUST_LAB</b>	Variant: <b>DRAFT</b>	Git Hash: <b>f2c7d09</b>
	Board Name: <b>AD7910</b>	Project Name: <b>OPEN_WEIGHT</b>	
Sheet Title: Project Architecture	File Name: Project Architecture.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 + (Unreleased)
Sheet Path: /Project Architecture/	Reviewer:	Size: <b>A3</b>	Sheet: <b>3 of 10</b>

# [4] Sheet Title A



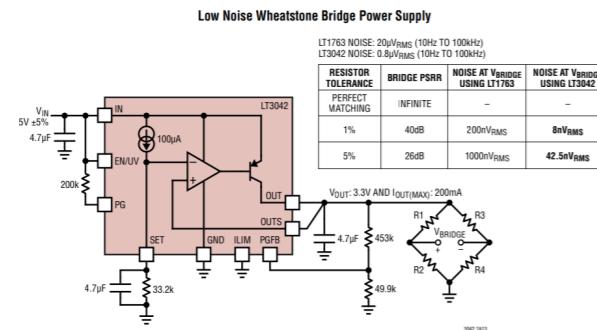
**About**

The AD7190 is a low noise, complete analog front end for high precision measurement applications. It contains a low noise, 24-bit sigma-delta ( $\Sigma\Delta$ ) analog-to-digital converter (ADC). The on-chip low noise gain stage means that signals of small amplitude can be interfaced directly to the ADC. The device can be configured to have two differential inputs or four pseudo differential inputs. The on-chip channel sequencer allows several channels to be enabled, and the AD7190 sequentially converts on each enabled channel. This simplifies communication with the part. The on-chip 4.92 MHz clock can be used as the clock source to the ADC or, alternatively, an external clock or crystal can be used. The output data rate from the part can be varied from 4.7 Hz to 4.8 kHz. The device has two digital filter options. The choice of filter affects the rms noise/noise-free resolution at the programmed output data rate, the settling time, and the 50 Hz/60 Hz rejection.

Comments: AN5346 STM32G474 Datasheet p.81 J. Pieper ADC investigation	Company: <b>OPEN_TRUST_LAB</b>	Variant: DRAFT	Git Hash: f2c7d09
Board Name: <b>AD7190</b>	Project Name: <b>OPEN_WEIGHT</b>		
Sheet Title: Sheet Title A	File Name: Section A - Title A.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12
Sheet Path: /Project Architecture/AD7910_Weight_sensor/	Reviewer:	Size: <b>A4</b>	Revision: + (Unreleased)

# [5] Sheet Title B

## TYPICAL APPLICATIONS



IN (pins 1-2) : entrée d'alimentation du LT3042 (6V), à découpler avec CIN.  
 EN/UV (pin 3) : active/désactive le régulateur et permet un seuil UVLO (souvent relié à IN pour "toujours ON").  
 PG (pin 4) : sortie Power-Good open-collector (nécessite une résistance pull-up).  
 ILIM (pin 5) : programmation/monitoring de la limite de courant (souvent à GND si non utilisé).  
 PGFB (pin 6) : entrée qui fixe le seuil de Power-Good via un pont diviseur depuis VOUT.  
 SET (pin 7) : règle la tension de sortie via RSET (et CSET réduit le bruit/soft-start).  
 GND (pin 8) : masse de référence du circuit.  
 OUTS (pin 9) : sense Kelvin de la sortie (à relier au + de COUT / point de charge).  
 OUT (pin 10) : sortie régulée (5V), à découpler avec COUT.  
 EPAD (pad exposé) : masse + dissipation thermique (à souder sur plan GND).

### DESIGN NOTE:

Ref Condo for SET PIN (important pour les vibrations P16)  
 KYOCERA AVX TAJA225K016RNJ (2.2 μF, 16 VDC,  
 condensateur tantalum solide SMD moulé, 1206 / 3216 (A case),  
 ±10%, ESR 6.5 Ω).

$$V_{OUT} = I_{SET} \times R_{SET}$$

$$I_{SET} \approx 100 \mu A$$

Donc :  
 $R_{SET} = V_{OUT} / I_{SET}$   
 $R_{SET} = 5.0 \text{ V} / 100 \mu A = 50 \text{ k}\Omega$   
 (= valeur standard recommandée : 49.9 kΩ)

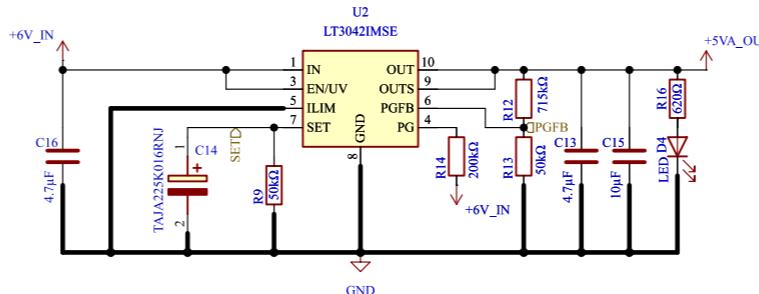
$$V_{OUT(PG\_THRESHOLD)} = 0.3 \text{ V} \times (1 + RPG2/RPG1)$$

$$PGFB\_THRESHOLD = 0.3 \text{ V}$$

Donc :  
 $RPG2 = RPG1 \times (V_{OUT(PG)} / 0.3 \text{ V} - 1)$

Exemple (PG OK ~4.8 V) :  
 Choix RPG1 = 49.9 kΩ  
 $RPG2 = 49.9 \text{ k}\Omega \times (4.8 / 0.3 - 1) = 748.5 \text{ k}\Omega$   
 (= valeur standard recommandée : 750 kΩ)

## Design guide line

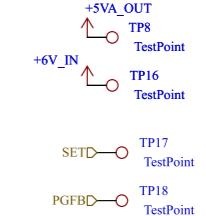


## Convertisseur 5VA

### About

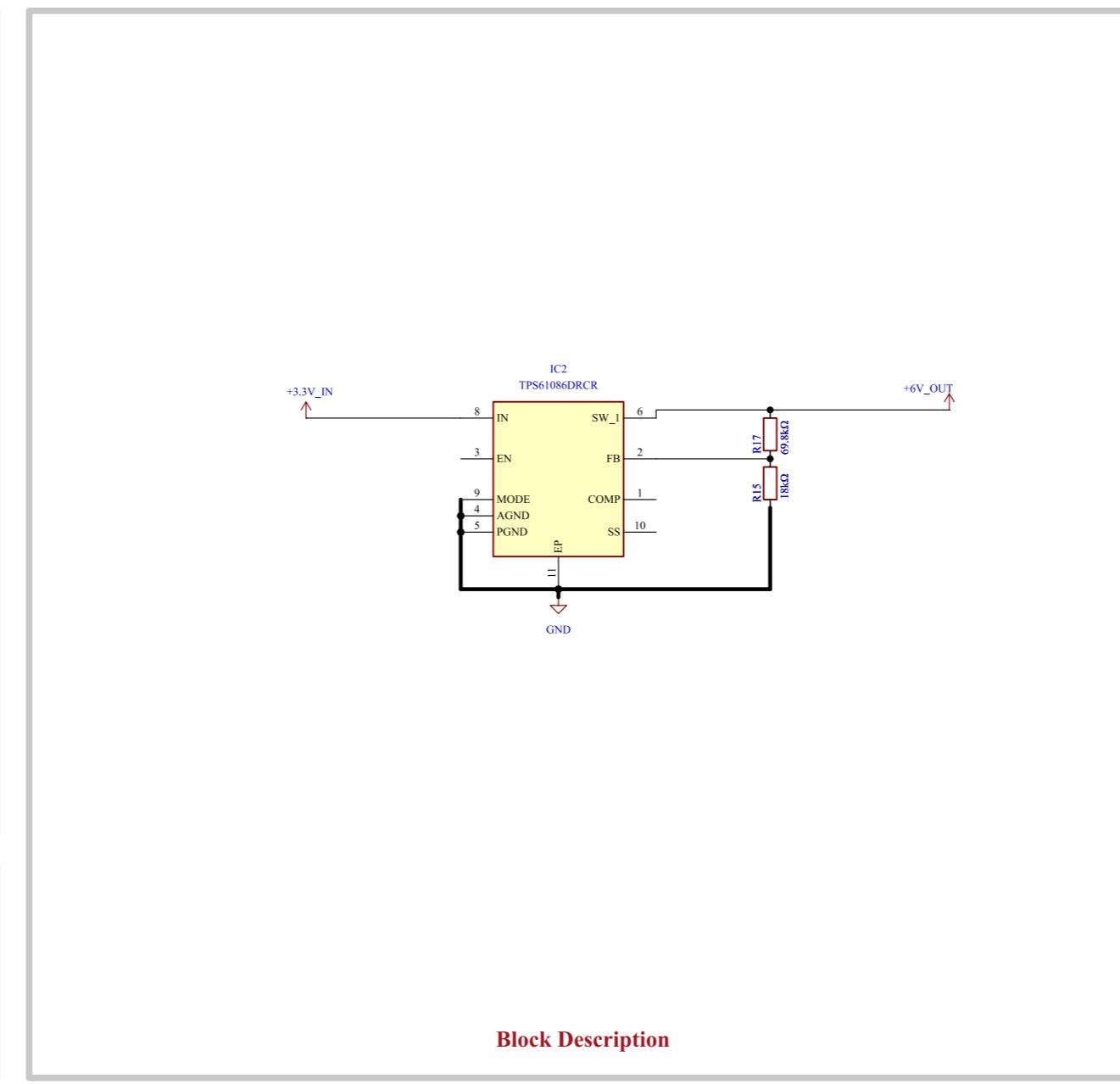
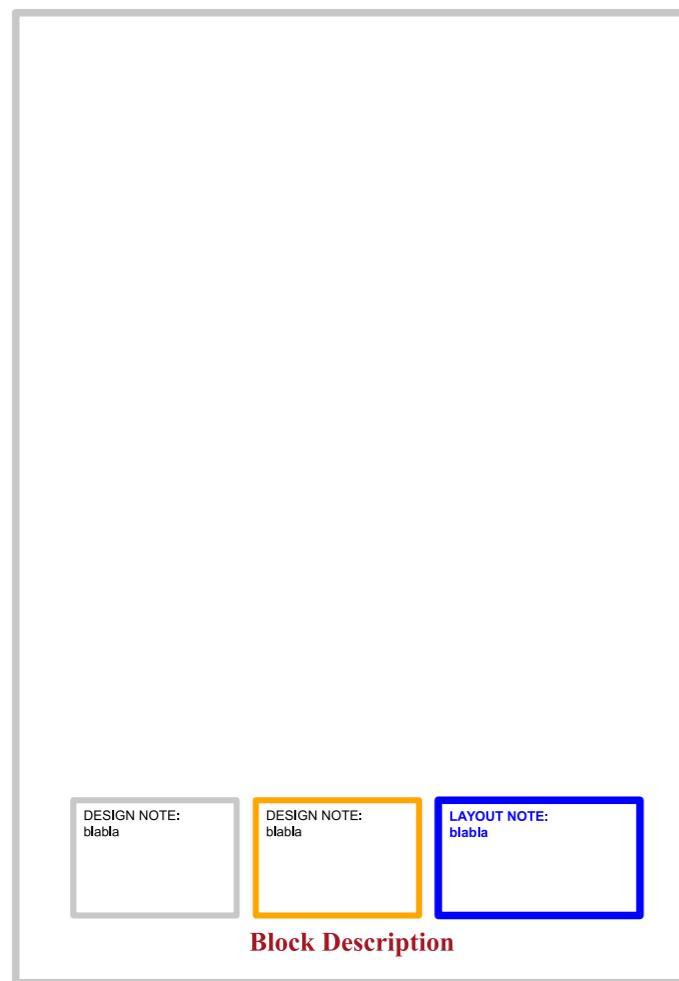
The LT®3042 is a high performance low dropout linear regulator featuring LTC's ultralow noise and ultrahigh PSRR architecture for powering noise sensitive RF applications. Designed as a precision current reference followed by a high performance voltage buffer, the LT3042 can be easily paralleled to further reduce noise, increase output current and spread heat on the PCB. The device supplies 200mA at a typical 350mV dropout voltage. Operating quiescent current is nominally 2mA and drops to <<1μA in shutdown. The LT3042's wide output voltage range (0V to 15V) while maintaining unitygain operation provides virtually constant output noise, PSRR, bandwidth and load regulation, independent of the programmed output voltage. Additionally, the regulator features programmable current limit, fast start-up capability and programmable power good to indicate output voltage regulation. The LT3042 is stable with a minimum 4.7μF ceramic output capacitor. Built-in protection includes reverse battery protection, reverse current protection, internal current limit with foldback and thermal limit with hysteresis. The LT3042 is available in thermally enhanced 10-Lead MSOP and 3mm × 3mm DFN package.

## TEST POINT



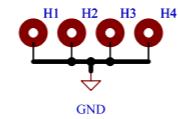
Comments: References: Flexible I/O worked examples Flexible I/O source configuration	Company: <b>OPEN_TRUST_LAB</b>	Variant: DRAFT	Git Hash: f2c7d09
Board Name: <b>AD7190</b>	Project Name: <b>OPEN_WEIGHT</b>		
Sheet Title: Sheet Title B	File Name: Section C - Title C.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 Revision: + (Unreleased)
Sheet Path: /Project Architecture/LT3042_6V_5VA/	Reviewer:	Size: <b>A3</b>	Sheet: <b>5 of 10</b>

# [6] Sheet Title B



Comments: References: Flexible I/O worked examples Flexible I/O source configuration	Company: <b>OPEN_TRUST_LAB</b>	Variant: DRAFT	Git Hash: f2c7d09
	Board Name: <b>AD7190</b>	Project Name: <b>OPEN_WEIGHT</b>	
Sheet Title: Sheet Title B	File Name: Section B - Title B.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 Revision: + (Unreleased)
Sheet Path: /Project Architecture/TPS61086_3.3V_to_6V/	Reviewer:	Size: <b>A3</b>	Sheet: <b>6 of 10</b>

# [7] Sheet Title B



FID1  
Fiducial  
FID2  
Fiducial  
FID3  
Fiducial

**Block Description**

DESIGN NOTE:  
blabla

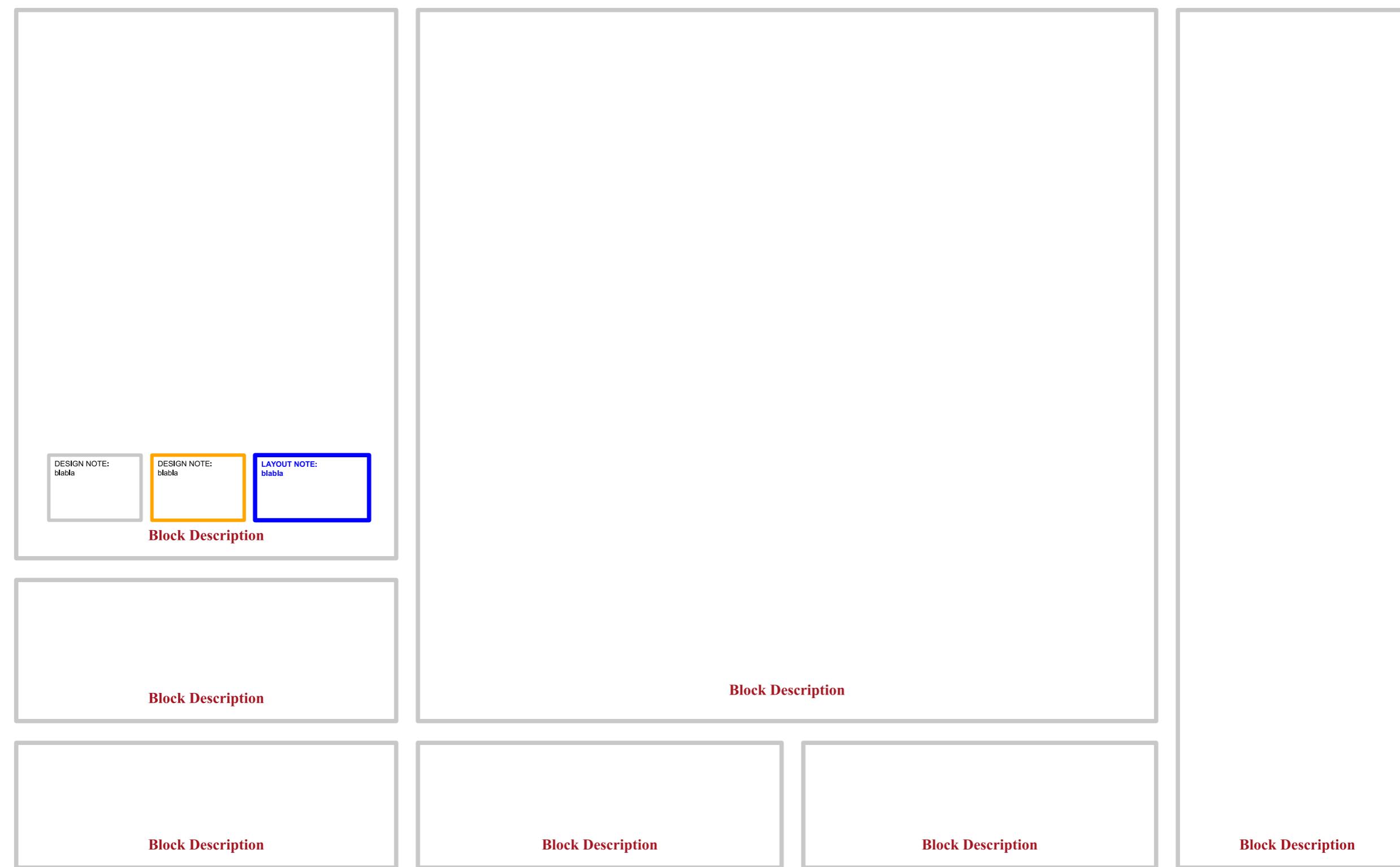
DESIGN NOTE:  
blabla

LAYOUT NOTE:  
blabla

**Block Description**

	Comments: References: Flexible I/O worked examples Flexible I/O source configuration	Company: <b>OPEN_TRUST_LAB</b>	Variant: DRAFT	Git Hash: f2c7d09
	Board Name: <b>AD7190</b>	Project Name: <b>OPEN_WEIGHT</b>		
	Sheet Title: Sheet Title B	File Name: Section E - Title E.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 Revision: + (Unreleased)
	Sheet Path: /Project Architecture/Holes, Fiducials/		Reviewer:	Size: <b>A3</b> Sheet: <b>7 of 10</b>

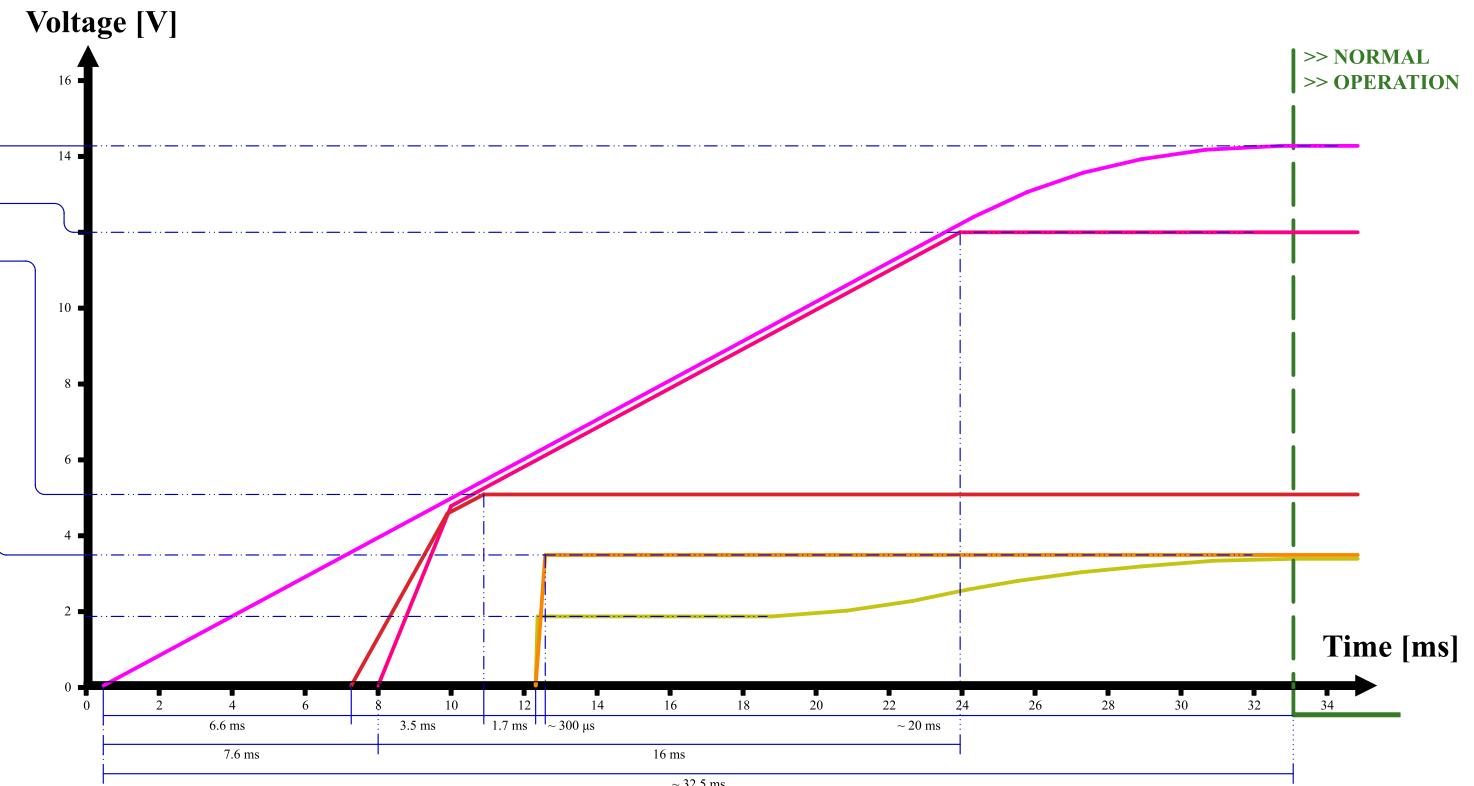
# [8] Sheet Title B



	Comments: References: Flexible I/O worked examples Flexible I/O source configuration	Company: <b>OPEN_TRUST_LAB</b>	Variant: DRAFT	Git Hash: f2c7d09
	Board Name: <b>AD7190</b>	Project Name: <b>OPEN_WEIGHT</b>		
	Sheet Title: Sheet Title B	File Name: Section D - Title D.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 Revision: + (Unreleased)
	Sheet Path: /Project Architecture/Connecteur/	Reviewer:	Size: <b>A3</b>	Sheet: <b>8 of 10</b>

# [9] Power - Sequencing

NAME	SOURCE	LEVEL
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%



			Comments:	Company:	Variant:	Git Hash:	
				OPEN_TRUST_LAB	DRAFT	f2c7d09	
			Board Name:	Project Name:			
			AD7190	OPEN_WEIGHT			
Sheet Title:		File Name:	Designer:	Date:	Revision:		
Power - Sequencing		Power - Sequencing.kicad_sch	SIEBERT DIMITRY	2025-01-12	+ (Unreleased)		
Sheet Path:		Reviewer:		Size:	Sheet:		
/Power - Sequencing/		A4		9	of 10		

# [10] Revision History

A					A
B					B
C					C
D					D

		Comments:	Company: <b>OPEN_TRUST_LAB</b>	Variant: DRAFT	Git Hash: f2c7d09
			Board Name: <b>AD7190</b>	Project Name: <b>OPEN_WEIGHT</b>	
		Sheet Title: Revision History	File Name: Revision History.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 Revision: + (Unreleased)
		Sheet Path: <a href="#">/Revision History/</a>		Reviewer:	Size: <b>A4</b> Sheet: <b>10 of 10</b>