

1 2 3 4 5 6 7 8

AD7190

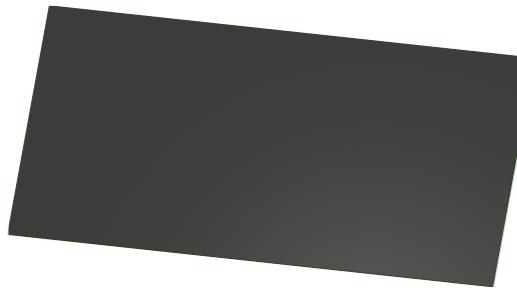
Variant: DRAFT

2026-02-25

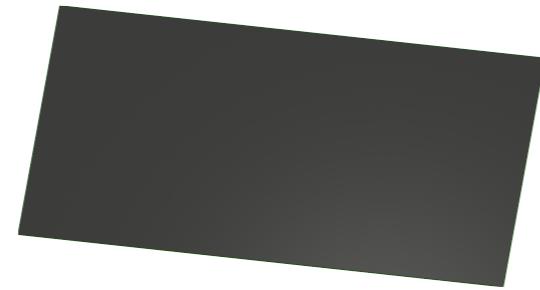
Rev + (Unreleased)

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TOP VIEW



BOTTOM VIEW



NOTES

Comment

Not fitted components are marked as

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There shouldn't be any mistakes. Contact the engineer if you find any.

RELEASED - A board with this schematic has been sent to production.

Date: 25-Feb-2026

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for debug notes.

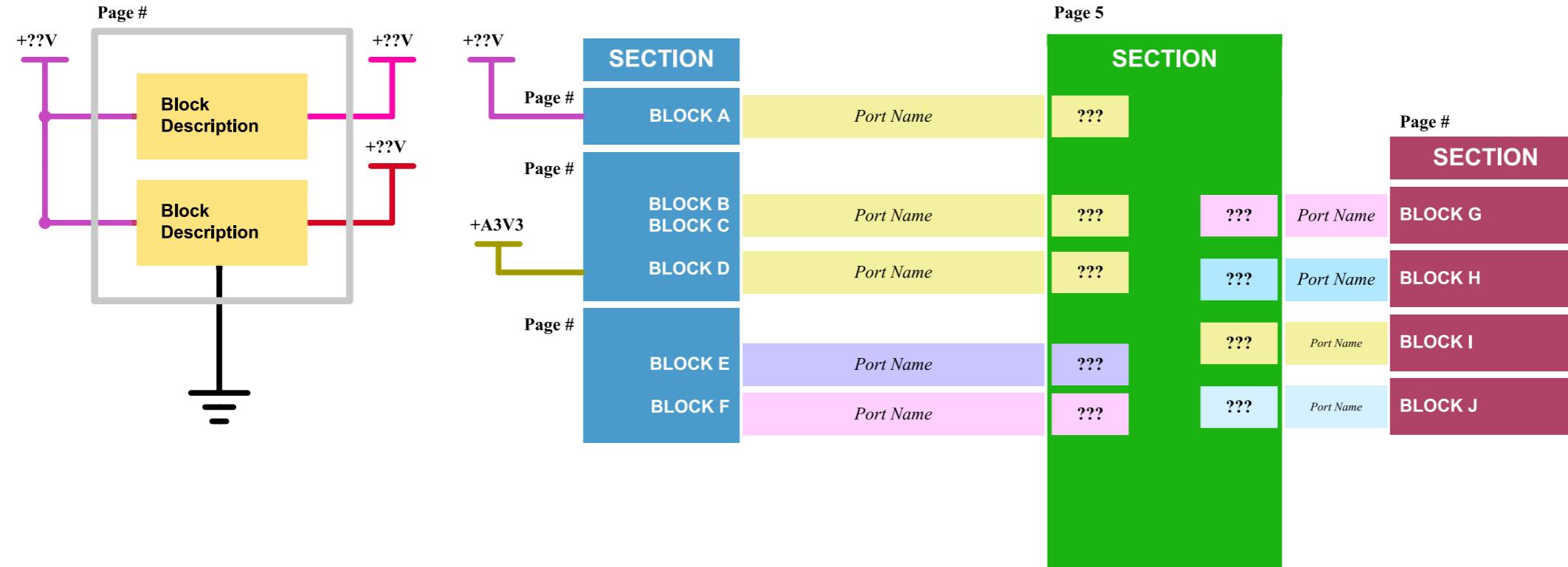
DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

	Comments:	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
	Board Name: AD7190	Project Name: OPEN_WEIGHT		
	Sheet Title: File Name: Cellule_de_force_V2.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12	Revision: + (Unreleased)
	Sheet Path: /	Reviewer:	Size: A3	Sheet: 1 of 10

[2] Block Diagram

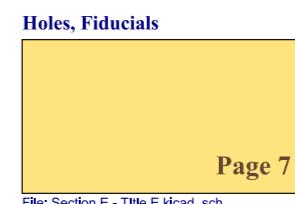
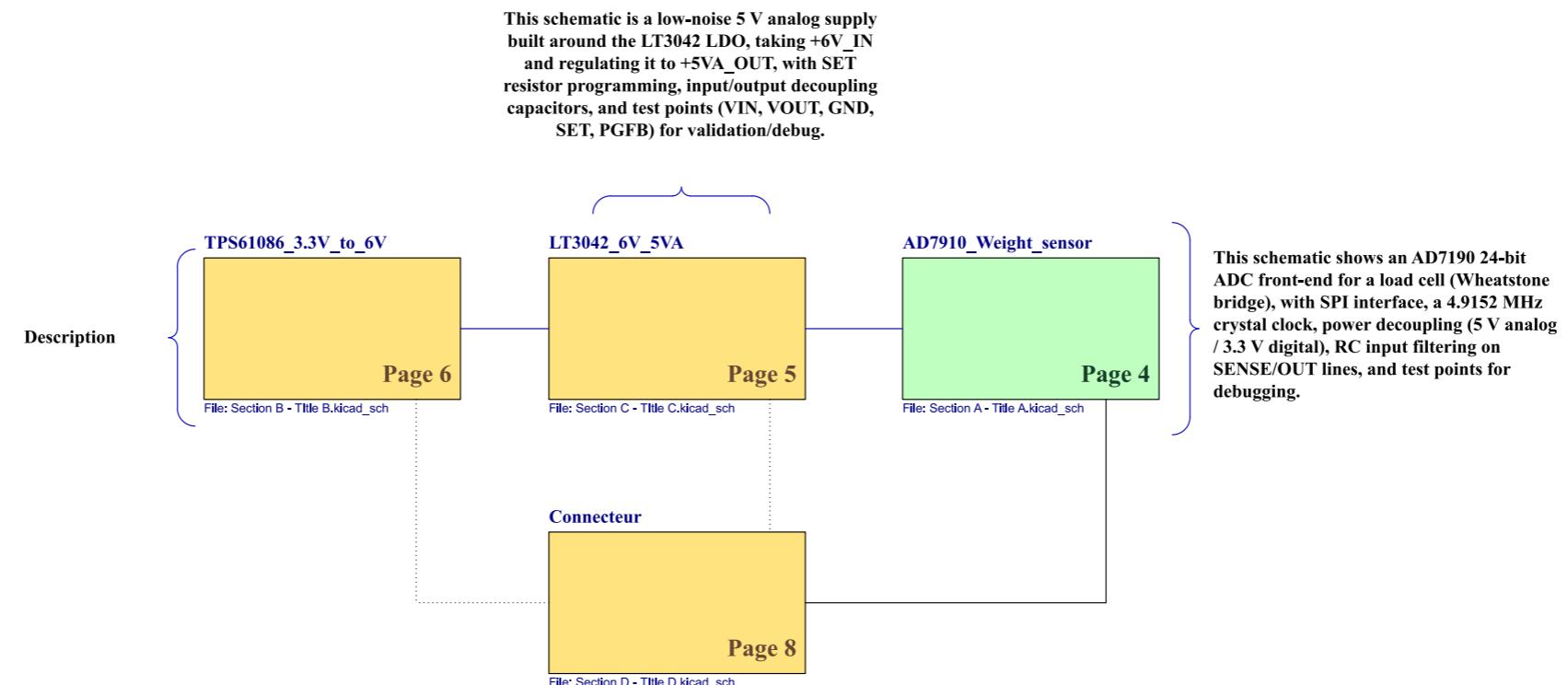


Target specifications:

Input voltage:	?? - ?? V
Spec 2	??
Spec 3	??
Spec 4	??

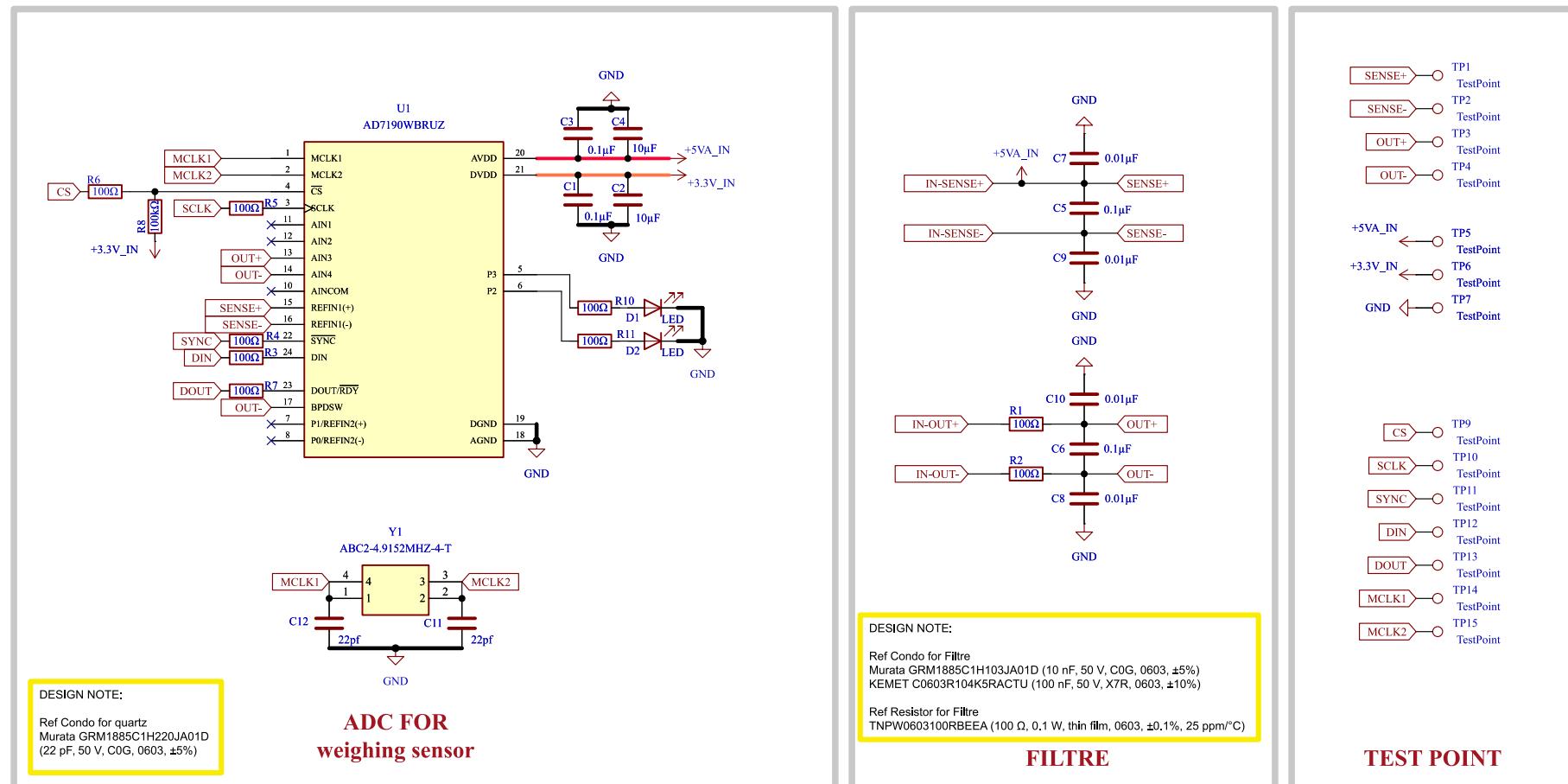
	Comments:	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
		Board Name: AD7190	Project Name: OPEN_WEIGHT	
	Sheet Title: Block Diagram	File Name: Block Diagram.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 + (Unreleased)
	Sheet Path: /Block Diagram/		Reviewer:	Size: A3 Sheet: 2 of 10

[3] Project Architecture



Comments:	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
	Board Name: AD7910	Project Name: OPEN_WEIGHT	
Sheet Title: Project Architecture	File Name: Project Architecture.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 + (Unreleased)
Sheet Path: /Project Architecture/	Reviewer:	Size: A3	Sheet: 3 of 10

[4] Sheet Title A

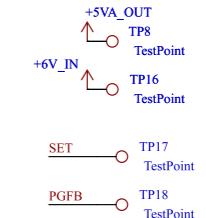
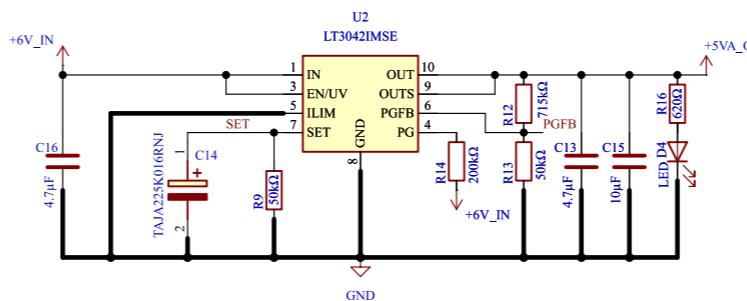
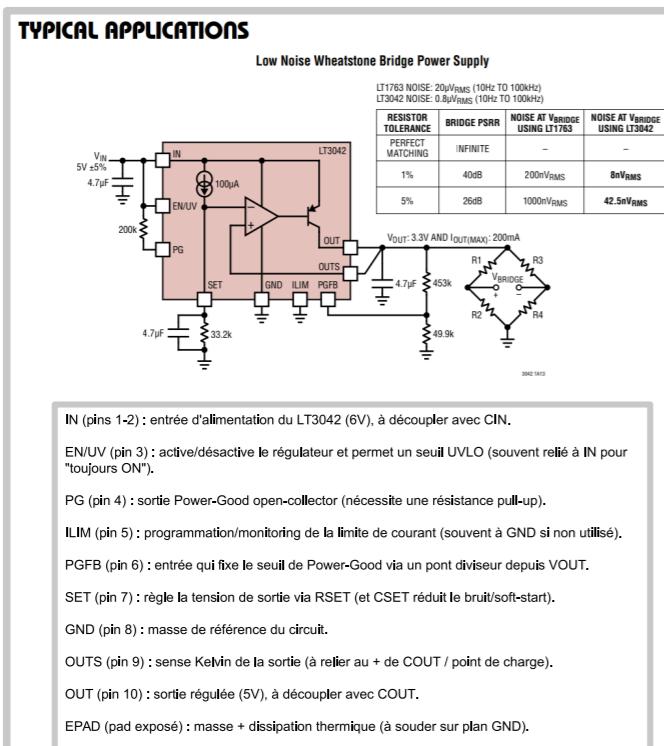


About

The AD7190 is a low noise, complete analog front end for high precision measurement applications. It contains a low noise, 24-bit sigma-delta ($\Sigma\Delta$) analog-to-digital converter (ADC). The on-chip low noise gain stage means that signals of small amplitude can be interfaced directly to the ADC. The device can be configured to have two differential inputs or four pseudo differential inputs. The on-chip channel sequencer allows several channels to be enabled, and the AD7190 sequentially converts on each enabled channel. This simplifies communication with the part. The on-chip 4.92 MHz clock can be used as the clock source to the ADC or, alternatively, an external clock or crystal can be used. The output data rate from the part can be varied from 4.7 Hz to 4.8 kHz. The device has two digital filter options. The choice of filter affects the rms noise/noise-free resolution at the programmed output data rate, the settling time, and the 50 Hz/60 Hz rejection.

Comments: AN5346 STM32G474 Datasheet p.81 J. Pieper ADC investigation	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
Board Name: AD7190	Project Name: OPEN_WEIGHT		
Sheet Title: Sheet Title A	File Name: Section A - Title A.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12
Sheet Path: /Project Architecture/AD7910_Weight_sensor/	Reviewer:	Size: A4	Revision: + (Unreleased)

[5] Sheet Title B



DESIGN NOTE:
Ref Condo for SET PIN (important pour les vibrations P16)
KYOCERA AVX TAJA225K016RNJ (2.2 µF, 16 VDC,
condensateur tantalique solide SMD moulé, 1206 / 3216 (A case
+10% ESR 6.5 Ω).

$$V_{OUT} \approx I_{SET} \times R_{SET}$$

Donc :
 $RSET \approx VOUT / ISET$
 $RSET \approx 5.0 \text{ V} / 100 \mu\text{A} = 50 \text{ k}\Omega$
 $(\Rightarrow \text{valeur standard recommandée : } 49.9 \text{ k}\Omega)$

$$V_{OUT(PG_THRESHOLD)} \approx 0.3 \text{ V} \times (1 + RPG2/RPG1)$$

$$PGFB_THRESHOLD \approx 0.3 \text{ V}$$

Donc :
 $RPG2 \approx RPG1 \times (VOUT(PG)/0.3 V - 1)$

Exemple (PG OK à ~4.8 V) :
 Choix RPG1 = 49.9 kΩ
 $RPG2 \approx 49.9 \text{ k}\Omega \times (4.8/0.3 - 1) \approx 748.5 \text{ k}\Omega$
 (=> valeur standard recommandée : 750 kΩ)

Design guide line

Convertisseur 5VA

About

The LT®3042 is a high performance low dropout linear regulator featuring LTC's ultralow noise and ultrahigh PSRR architecture for powering noise sensitive RF applications. Designed as a precision current reference followed by a high performance voltage buffer, the LT3042 can be easily paralleled to further reduce noise, increase output current and spread heat on the PCB. The device supplies 200mA at a typical 350mV dropout voltage. Operating quiescent current is nominally 2mA and drops to <<1µA in shutdown. The LT3042's wide output voltage range (0V to 15V) while maintaining unitygain operation provides virtually constant output noise, PSRR, bandwidth and load regulation, independent of the programmed output voltage. Additionally, the regulator features programmable current limit, fast start-up capability and programmable power good to indicate output voltage regulation. The LT3042 is stable with a minimum 4.7µF ceramic output capacitor. Built-in protection includes reverse battery protection, reverse current protection, internal current limit with foldback and thermal limit with hysteresis. The LT3042 is available in thermally enhanced 10-Lead MSOP and 3mm × 3mm DFN package.

TEST POINT

	Comments: References: Flexible I/O worked examples Flexible I/O source configuration	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
		Board Name: AD7190	Project Name: OPEN_WEIGHT	
	Sheet Title: Sheet Title B	File Name: Section C - Title C.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 + (Unreleased)
	Sheet Path: /Project Architecture/LT3042_6V_5VA/		Reviewer:	Size: A3 5 of 10

[6] Sheet Title B

A

COMP (pin 1) : broche de compensation de l'ampli d'erreur ; y connecter le réseau Rcomp + Ccomp vers AGND pour stabiliser la boucle (ne pas la router près de SW).

FB (pin 2) : entrée feedback ; à relier au pont diviseur R1/R2 depuis VOUT (après la diode) pour régler la tension de sortie (ex. 6 V).

EN (pin 3) : enable / shutdown ; niveau haut = actif, bas = arrêt. Souvent relié à IN pour "toujours ON", ou piloté par un GPIO.

AGND (pin 4) : masse analogique (référence des signaux sensibles : FB/COMP/SS/MODE). A garder "propre" et relier au plan GND de façon matrisée.

PGND (pin 5) : masse puissance (retour des courants de commutation). À relier au plan GND avec une zone cuivre courte/large et proche des capas de puissance.

SW (pins 6-7) : noeud switch (commutation) ; à connecter à L et à la diode Schottky. C'est le noeud le plus bruyant → piste courte, boucle minimale, éloignée de FB/COMP.

IN (pin 8) : entrée d'alimentation (2.3-6 V) ; à découpler au plus près avec Cby ~1 µF + Cin (ex. 10 µF) vers GND.

MODE (pin 9) : sélection du mode : MODE = High → Forced PWM (fréquence plus stable, mieux pour le bruit), MODE = Low → PFM (meilleur rendement à faible charge).

SS (pin 10) : soft-start ; mettre un condensateur (Css) pour limiter l'inrush au démarrage. Ouvert = pas de soft-start.

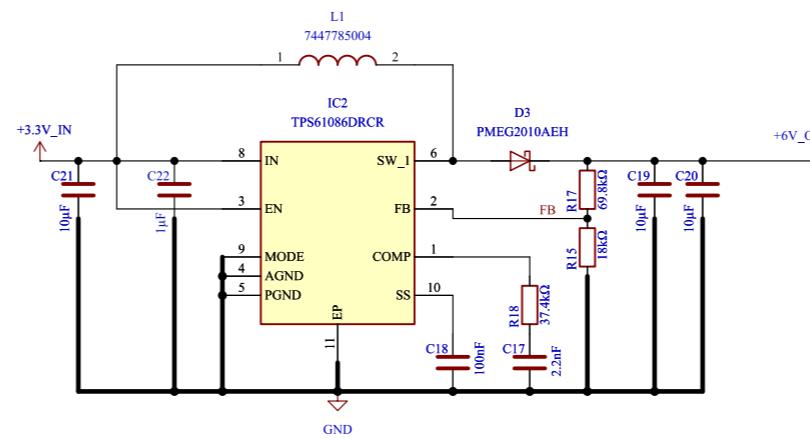
B

C

D

E

F



FB → TP19
+6V_OUT → TP20
+3.3V_IN → TP21

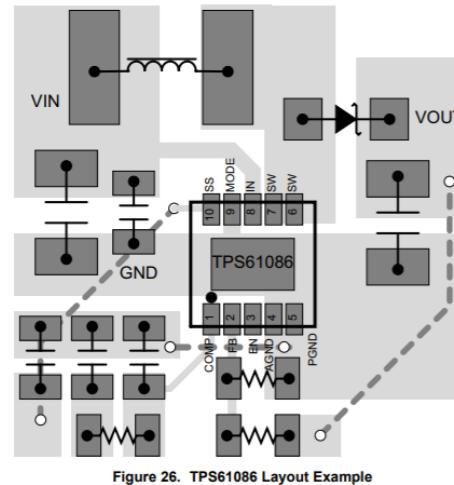


Figure 26. TPS61086 Layout Example

Block Description

Block Description

About

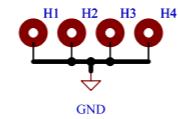
The TPS61086 device is a high-frequency, high-efficiency DC-to-DC converter with an integrated 2.0-A, 0.13-Ω power switch capable of providing an output voltage up to 18.5 V. The implemented boost converter is based on a fixed frequency of 1.2-MHz, pulse-width-modulation (PWM) controller that allows the use of small external inductors and capacitors and provides fast transient response.

At light-load, the device can operate in Power Save Mode with pulse-frequency-modulation (PFM) to improve the efficiency while keeping a low-output voltage ripple. For very noise-sensitive applications, the device can be forced to PWM Mode operation over the entire load range by pulling the MODE pin high. The external compensation allows optimizing the application for specific conditions. A capacitor connected to the soft-start pin minimizes inrush current at start-up.

Block Description

Comments: References: Flexible I/O worked examples Flexible I/O source configuration	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
Board Name: AD7190	Project Name: OPEN_WEIGHT		
Sheet Title: Sheet Title B	File Name: Section B - Title B.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 Revision: + (Unreleased)
Sheet Path: /Project Architecture/TPS61086_3.3V_to_6V/	Reviewer:	Size: A3	Sheet: 6 of 10

[7] Sheet Title B



FID1
Fiducial
FID2
Fiducial
FID3
Fiducial

Block Description

DESIGN NOTE:
blabla

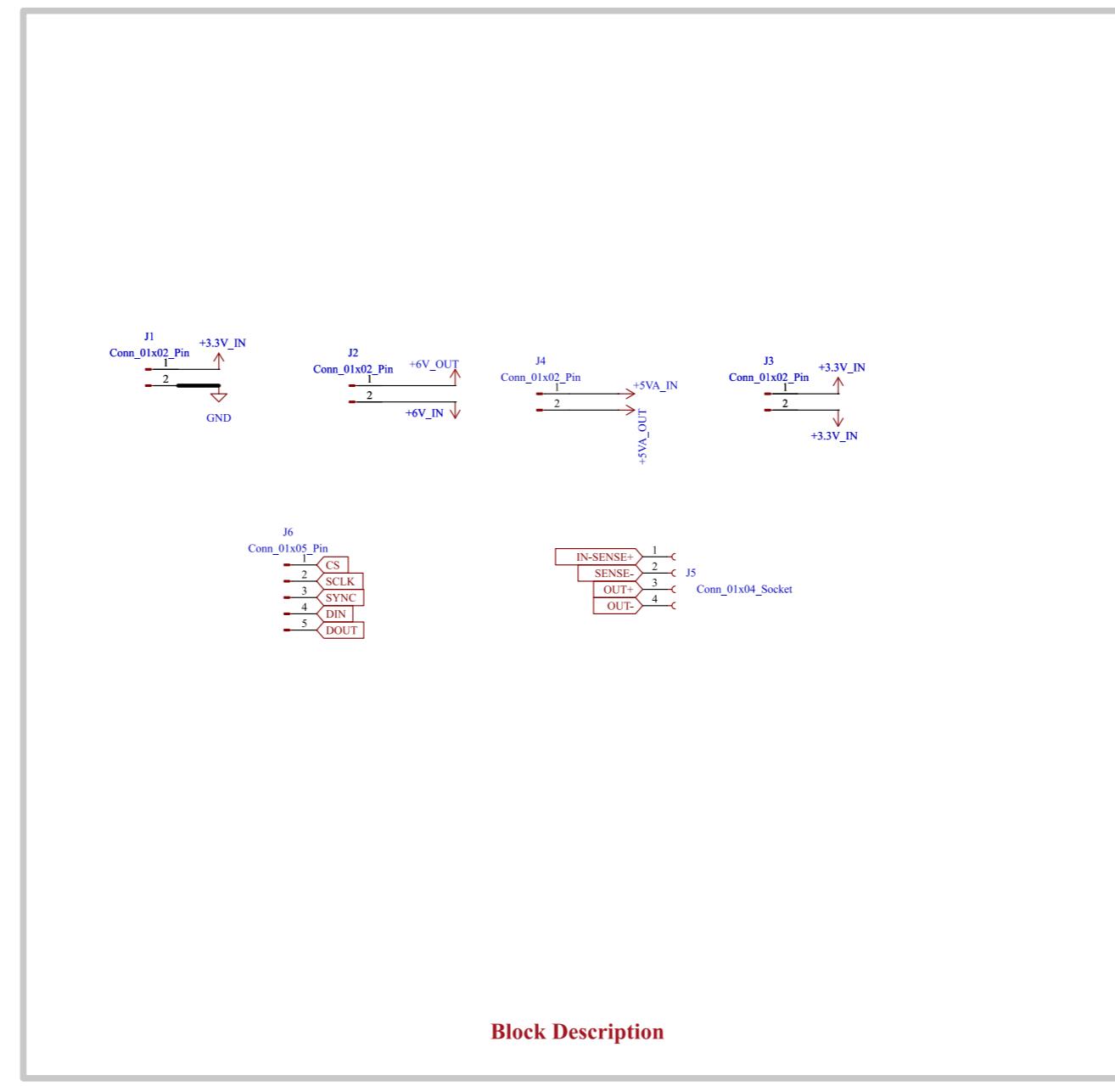
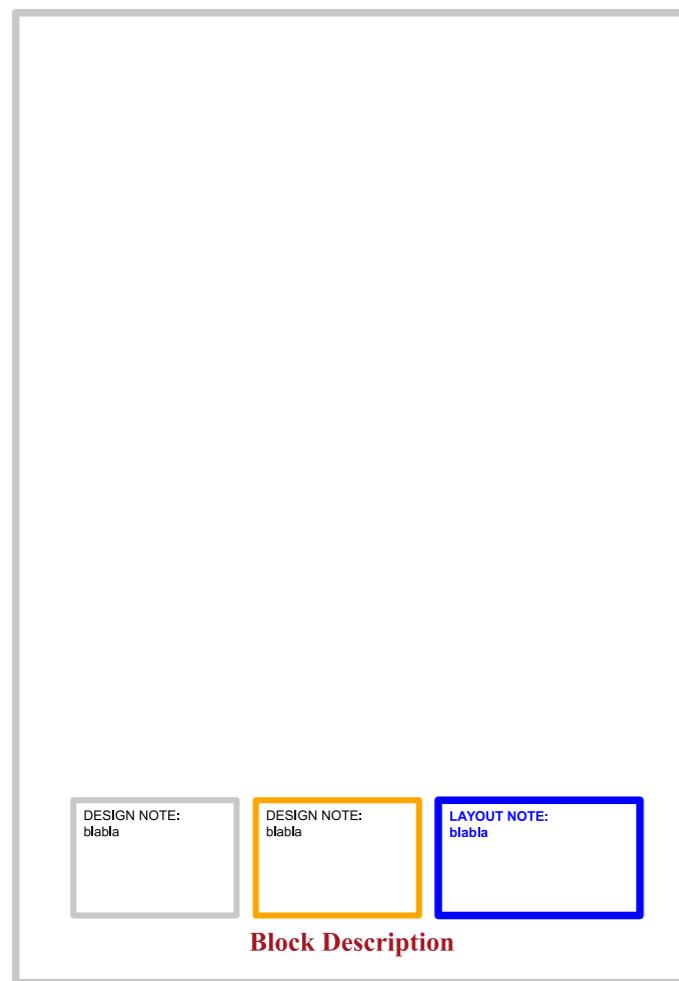
DESIGN NOTE:
blabla

LAYOUT NOTE:
blabla

Block Description

	Comments: References: Flexible I/O worked examples Flexible I/O source configuration	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
	Board Name: AD7190	Project Name: OPEN_WEIGHT		
	Sheet Title: Sheet Title B	File Name: Section E - Title E.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 Revision: + (Unreleased)
	Sheet Path: /Project Architecture/Holes, Fiducials/		Reviewer:	Size: A3 Sheet: 7 of 10

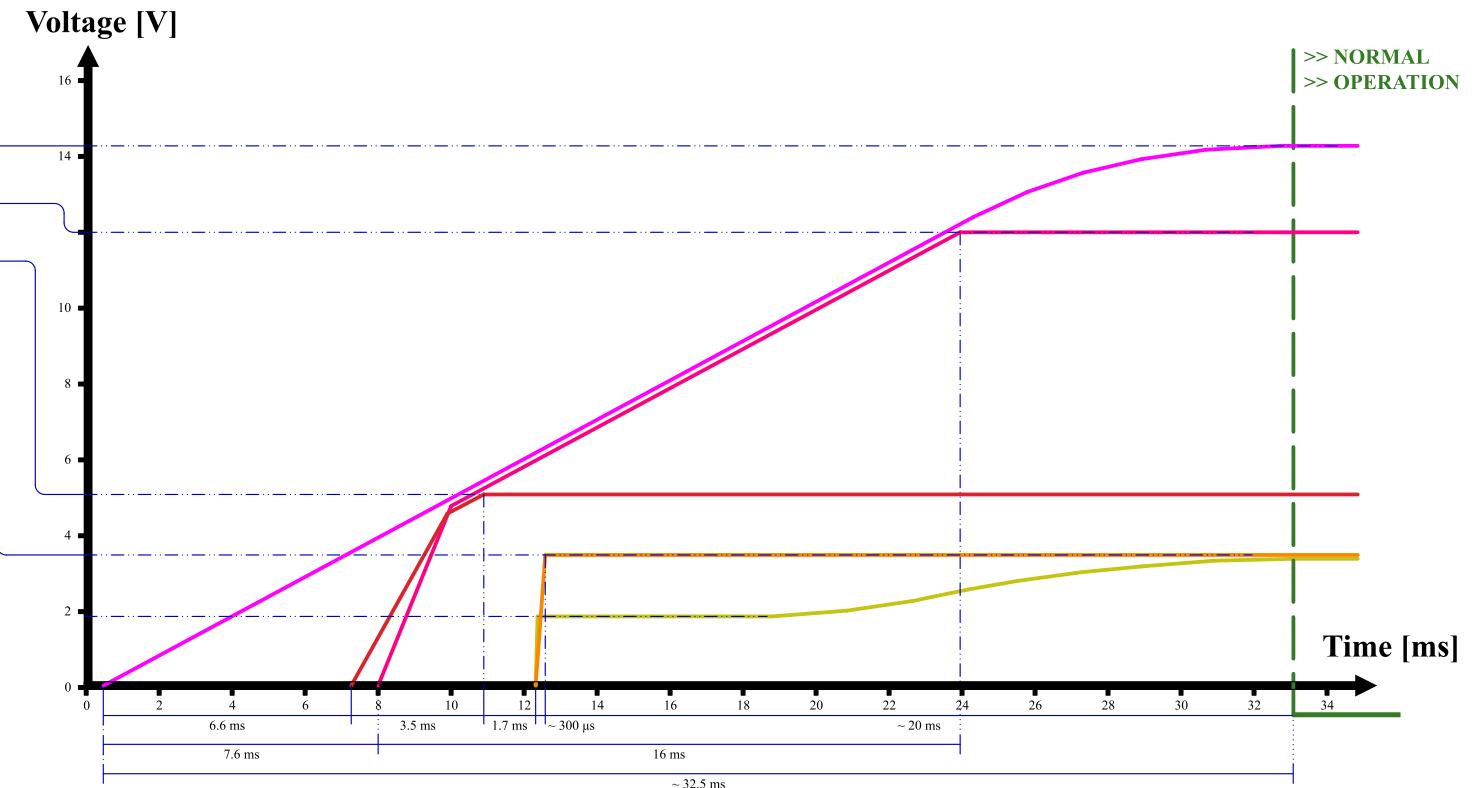
[8] Sheet Title B



Comments: References: Flexible I/O worked examples Flexible I/O source configuration	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
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Sheet Title: Sheet Title B	File Name: Section D - Title D.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 + (Unreleased)
Sheet Path: /Project Architecture/Connecteur/	Reviewer:	Size: A3	Sheet: 8 of 10

[9] Power - Sequencing

NAME	SOURCE	LEVEL
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%



			Comments:	Company:	Variant:	Git Hash:	
				OPEN_TRUST_LAB	DRAFT	f2c7d09	
			Board Name:	Project Name:			
			AD7190	OPEN_WEIGHT			
Sheet Title:		File Name:	Designer:	Date:	Revision:		
Power - Sequencing		Power - Sequencing.kicad_sch	SIEBERT DIMITRY	2025-01-12	+ (Unreleased)		
Sheet Path:		Reviewer:		Size:	Sheet:		
/Power - Sequencing/		A4		9	of 10		

[10] Revision History

A					A
B					B
C					C
D					D

		Comments:	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
			Board Name: AD7190	Project Name: OPEN_WEIGHT	
		Sheet Title: Revision History	File Name: Revision History.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 Revision: + (Unreleased)
		Sheet Path: /Revision History/		Reviewer:	Size: A4 Sheet: 10 of 10