

1 2 3 4 5 6 7 8

A A

# AD7190

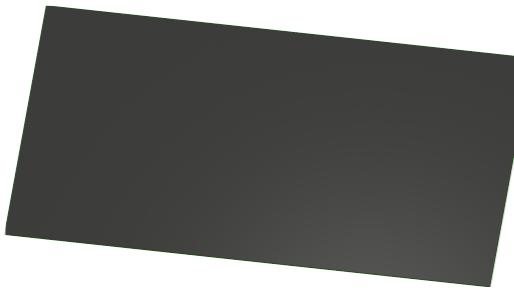
## Variant: DRAFT

2026-02-25

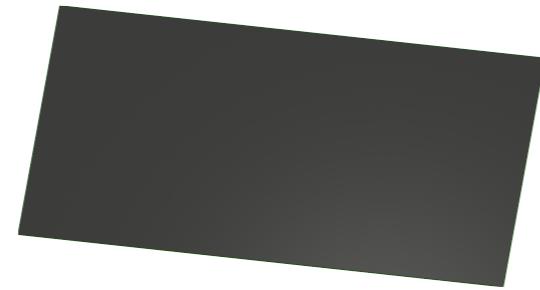
## Rev + (Unreleased)

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### TOP VIEW



### BOTTOM VIEW



### NOTES

Comment

Not fitted components are marked as

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There shouldn't be any mistakes. Contact the engineer if you find any.

RELEASED - A board with this schematic has been sent to production.

Date: 25-Feb-2026

### DESIGN CONSIDERATIONS

DESIGN NOTE:  
Example text for informational design notes.

DESIGN NOTE:  
Example text for debug notes.

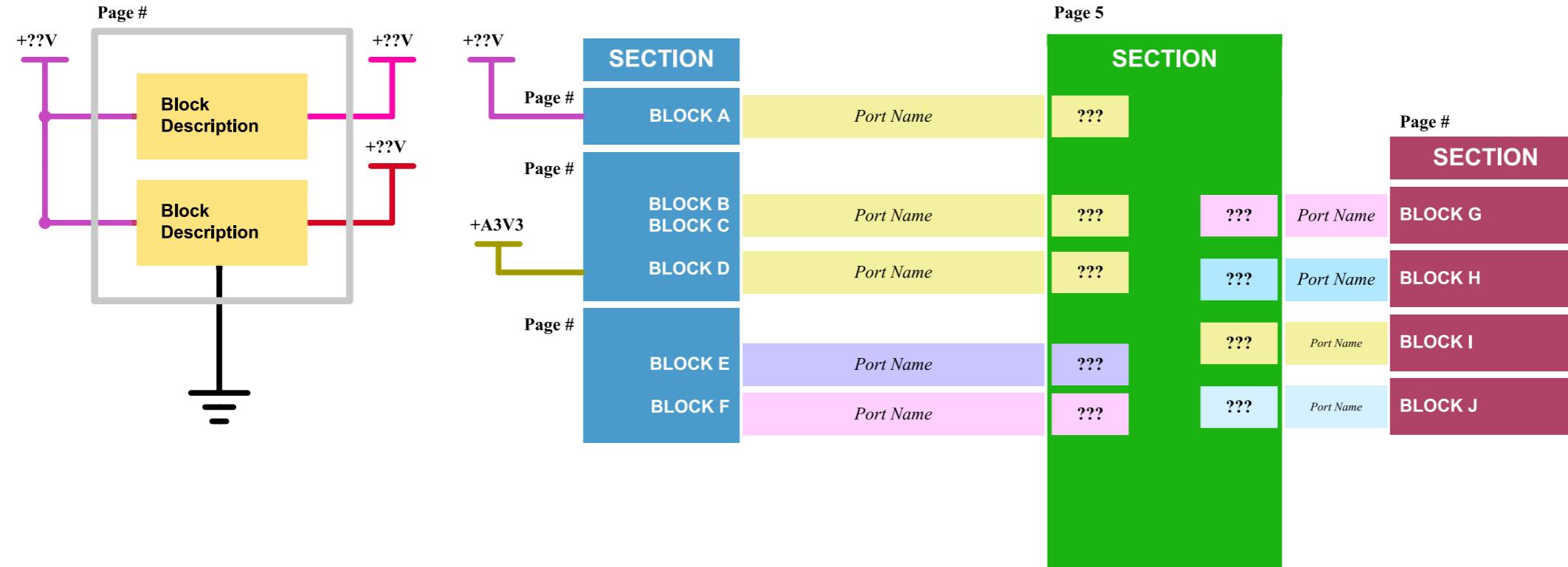
DESIGN NOTE:  
Example text for cautionary design notes.

DESIGN NOTE:  
Example text for critical design notes.

LAYOUT NOTE:  
Example text for critical layout guidelines.

|  |  |                                     |                            |                                    |
|--|--|-------------------------------------|----------------------------|------------------------------------|
|  | Comments:  | Company:<br><b>OPEN_TRUST_LAB</b>   | Variant:<br><b>DRAFT</b>   | Git Hash:<br><b>f2c7d09</b>        |
|  | Board Name:<br><b>AD7190</b>                                       | Project Name:<br><b>OPEN_WEIGHT</b> |                            |                                    |
|  | Sheet Title:<br>File Name:<br><b>Cellule_de_force_V2.kicad_sch</b> | Designer:<br><b>SIEBERT DIMITRY</b> | Date:<br><b>2025-01-12</b> | Revision:<br><b>+ (Unreleased)</b> |
|  | Sheet Path:<br><b>/</b>  | Reviewer:                           | Size:<br><b>A3</b>         | Sheet:<br><b>1 of 10</b>           |

# [2] Block Diagram



## Target specifications:

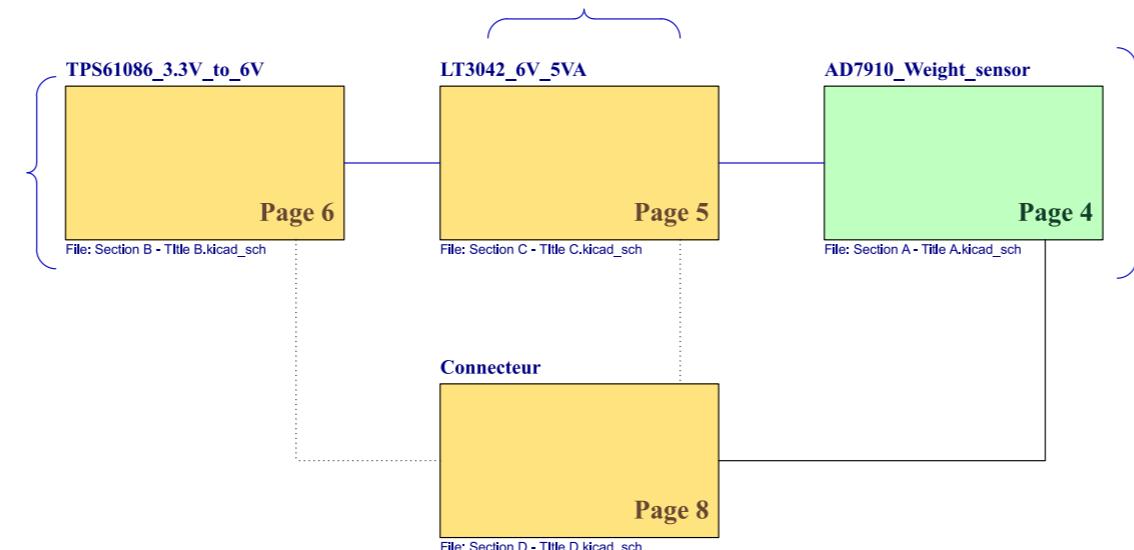
|                       |                  |
|-----------------------|------------------|
| <b>Input voltage:</b> | <b>?? - ?? V</b> |
| <b>Spec 2</b>         | <b>??</b>        |
| <b>Spec 3</b>         | <b>??</b>        |
| <b>Spec 4</b>         | <b>??</b>        |

|  |                     |                         |                      |                              |
|--|---------------------|-------------------------|----------------------|------------------------------|
|  | <b>Comments:</b>    | <b>Company:</b>         | <b>Variant:</b>      |                              |
|  |                     | <b>OPEN_TRUST_LAB</b>   | <b>DRAFT</b>         | f2c7d09                      |
|  | <b>Board Name:</b>  | <b>AD7190</b>           | <b>Project Name:</b> | <b>OPEN_WEIGHT</b>           |
|  |                     |                         |                      |                              |
|  | <b>Sheet Title:</b> | <b>File Name:</b>       | <b>Designer:</b>     | <b>Date:</b>                 |
|  | Block Diagram       | Block Diagram.kicad_sch | SIEBERT DIMITRY      | 2025-01-12<br>+ (Unreleased) |
|  | <b>Sheet Path:</b>  | <b>Reviewer:</b>        |                      | <b>Revision:</b>             |
|  | /Block Diagram/     |                         |                      |                              |
|  | <b>Size:</b>        | <b>Sheet:</b>           |                      |                              |
|  | <b>A3</b>           | <b>2 of 10</b>          |                      |                              |

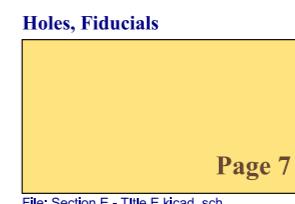
# [3] Project Architecture

This schematic is a low-noise 5 V analog supply built around the LT3042 LDO, taking +6V\_IN and regulating it to +5VA\_OUT, with SET resistor programming, input/output decoupling capacitors, and test points (VIN, VOUT, GND, SET, PGFB) for validation/debug.

This schematic is a TPS61086-based 3.3 V → 6 V boost supply with inductor/Schottky power stage, feedback divider for VOUT, decoupling + soft-start/compensation, and test points (+3.3V\_IN, +6V\_OUT, FB, GND).



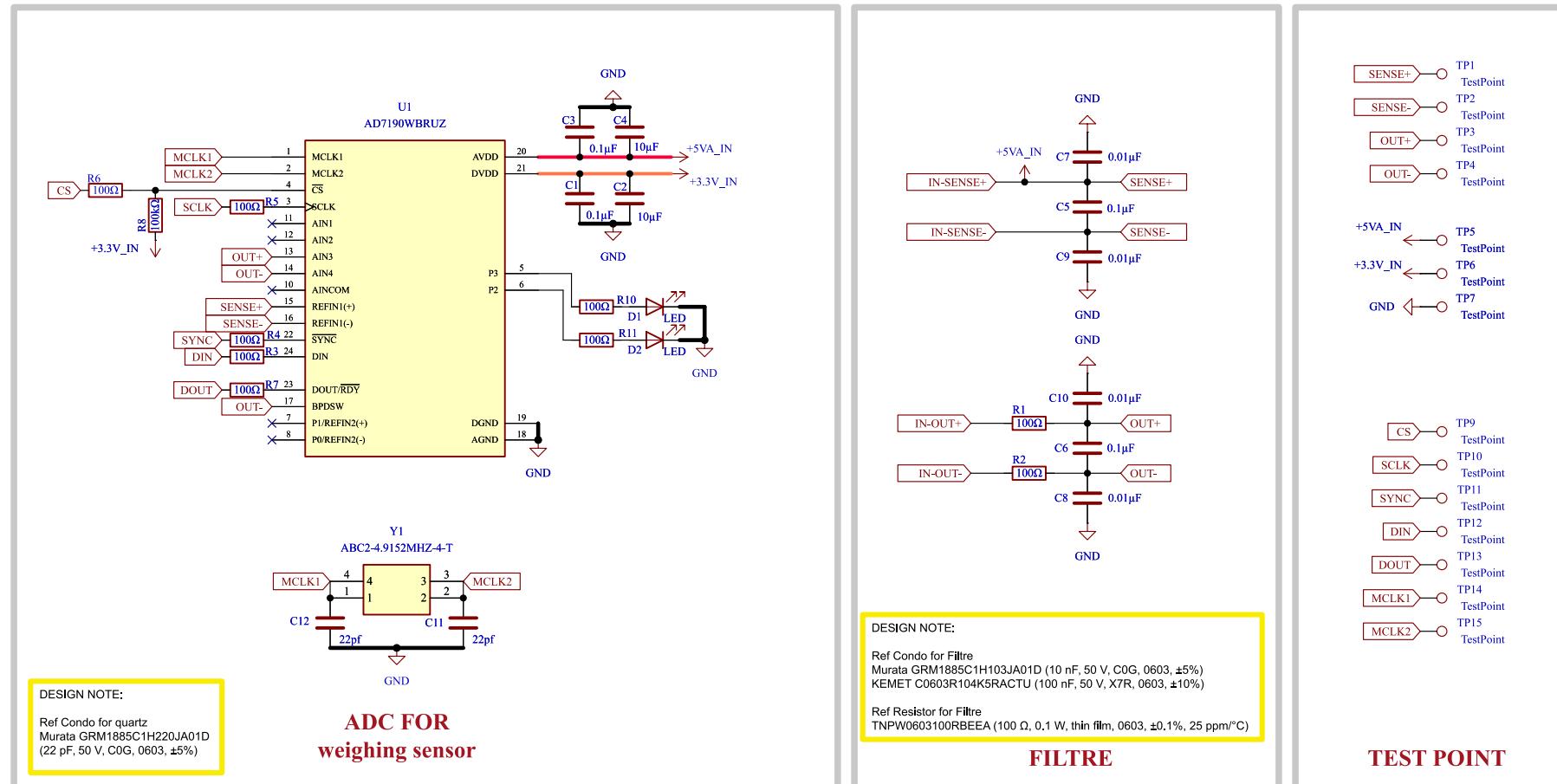
This schematic shows an AD7190 24-bit ADC front-end for a load cell (Wheatstone bridge), with SPI interface, a 4.9152 MHz crystal clock, power decoupling (5 V analog / 3.3 V digital), RC input filtering on SENSE/OUT lines, and test points for debugging.



File: Section E - Title E.kicad\_sch

|                                       |  |                                     |                                       |
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|                                       | Board Name:<br><b>AD7190</b>                 | Project Name:<br><b>OPEN_WEIGHT</b> |                                       |
| Sheet Title:<br>Project Architecture  | File Name:<br>Project Architecture.kicad_sch | Designer:<br>SIEBERT DIMITRY        | Date:<br>2025-01-12<br>+ (Unreleased) |
| Sheet Path:<br>/Project Architecture/ | Reviewer:                                    | Size:<br><b>A3</b>                  | Sheet:<br><b>3 of 10</b>              |

# [4] AD7910\_Weight\_sensor

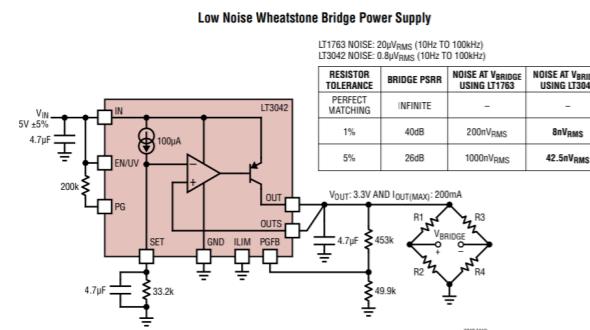


| About  |  |
|--|--|
| <p>The AD7190 is a low noise, complete analog front end for high precision measurement applications. It contains a low noise, 24-bit sigma-delta (<math>\Sigma\Delta</math>) analog-to-digital converter (ADC). The on-chip low noise gain stage means that signals of small amplitude can be interfaced directly to the ADC. The device can be configured to have two differential inputs or four pseudo differential inputs. The on-chip channel sequencer allows several channels to be enabled, and the AD7190 sequentially converts on each enabled channel. This simplifies communication with the part. The on-chip 4.92 MHz clock can be used as the clock source to the ADC or, alternatively, an external clock or crystal can be used. The output data rate from the part can be varied from 4.7 Hz to 4.8 kHz. The device has two digital filter options. The choice of filter affects the rms noise/noise-free resolution at the programmed output data rate, the settling time, and the 50 Hz/60 Hz rejection.</p> |  |

|  |   |                              |                                     |
|--|---|------------------------------|-------------------------------------|
| Comments:<br>AN5346<br>STM32G474 Datasheet p.81<br>J. Pieper ADC investigation | Company:<br><b>OPEN_TRUST_LAB</b>           | Variant:<br>DRAFT            | Git Hash:<br>f2c7d09                |
| Board Name:<br><b>AD7190</b>   |   |                              | Project Name:<br><b>OPEN_WEIGHT</b> |
| Sheet Title:<br>Sheet Title A  | File Name:<br>Section A - Title A.kicad_sch | Designer:<br>SIEBERT DIMITRY | Date:<br>2025-01-12                 |
| Sheet Path:<br>/Project Architecture/AD7910_Weight_sensor/                     | Reviewer:                                   | Size:<br><b>A4</b>           | Revision:<br>+ (Unreleased)         |

# [5] LT3042\_6V\_5VA

## TYPICAL APPLICATIONS



IN (pins 1-2) : entrée d'alimentation du LT3042 (6V), à découpler avec CIN.  
EN/UV (pin 3) : active/désactive le régulateur et permet un seuil UVLO (souvent relié à IN pour "toujours ON").  
PG (pin 4) : sortie Power-Good open-collector (nécessite une résistance pull-up).  
ILIM (pin 5) : programmation/monitoring de la limite de courant (souvent à GND si non utilisé).  
PGFB (pin 6) : entrée qui fixe le seuil de Power-Good via un pont diviseur depuis VOUT.  
SET (pin 7) : règle la tension de sortie via RSET (et CSET réduit le bruit/soft-start).  
GND (pin 8) : masse de référence du circuit.  
OUTS (pin 9) : sense Kelvin de la sortie (à relier au + de COUT / point de charge).  
OUT (pin 10) : sortie régulée (5V), à découpler avec COUT.  
EPAD (pad exposé) : masse + dissipation thermique (à souder sur plan GND).

### DESIGN NOTE:

Ref Condo for SET PIN (important pour les vibrations P16)  
KYOCERA AVX TAJA225K016RNJ (2.2 μF, 16 VDC,  
condensateur tantalé solide SMD moulé, 1206 / 3216 (A case),  
±10%, ESR 6.5 Ω).

$$V_{OUT} = I_{SET} \times R_{SET}$$

$$I_{SET} \approx 100 \mu A$$

Donc :  
R<sub>SET</sub> = V<sub>OUT</sub> / I<sub>SET</sub>  
R<sub>SET</sub> = 5.0 V / 100 μA = 50 kΩ  
(=> valeur standard recommandée : 49.9 kΩ)

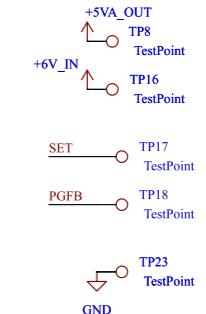
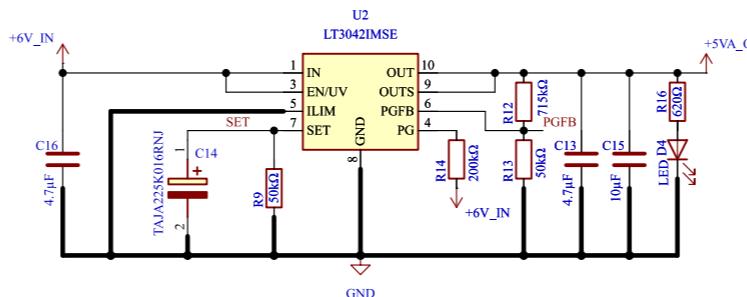
$$V_{OUT(PG\_THRESHOLD)} = 0.3 V \times (1 + RPG2/RPG1)$$

$$PGFB\_THRESHOLD = 0.3 V$$

Donc :  
RPG2 = RPG1 × (V<sub>OUT(PG)</sub>/0.3 V - 1)

Exemple (PG OK ~4.8 V) :  
Choix RPG1 = 49.9 kΩ  
RPG2 = 49.9 kΩ × (4.8/0.3 - 1) = 748.5 kΩ  
(=> valeur standard recommandée : 750 kΩ)

## Design guide line



## Convertisseur 5VA

### About

The LT®3042 is a high performance low dropout linear regulator featuring LTC's ultralow noise and ultrahigh PSRR architecture for powering noise sensitive RF applications. Designed as a precision current reference followed by a high performance voltage buffer, the LT3042 can be easily paralleled to further reduce noise, increase output current and spread heat on the PCB. The device supplies 200mA at a typical 350mV dropout voltage. Operating quiescent current is nominally 2mA and drops to <<1μA in shutdown. The LT3042's wide output voltage range (0V to 15V) while maintaining unitygain operation provides virtually constant output noise, PSRR, bandwidth and load regulation, independent of the programmed output voltage. Additionally, the regulator features programmable current limit, fast start-up capability and programmable power good to indicate output voltage regulation. The LT3042 is stable with a minimum 4.7μF ceramic output capacitor. Built-in protection includes reverse battery protection, reverse current protection, internal current limit with foldback and thermal limit with hysteresis. The LT3042 is available in thermally enhanced 10-Lead MSOP and 3mm × 3mm DFN package.

## TEST POINT

|   |   |                              |  |
|---|---|------------------------------|--|
| Comments:<br>References:<br>Flexible I/O worked examples<br>Flexible I/O source configuration | Company:<br><b>OPEN_TRUST_LAB</b>           | Variant:<br>DRAFT            | Git Hash:<br>f2c7d09                               |
| Board Name:<br><b>AD7190</b>  | Project Name:<br><b>OPEN_WEIGHT</b>         |                              |  |
| Sheet Title:<br>Sheet Title B   | File Name:<br>Section C - Title C.kicad_sch | Designer:<br>SIEBERT DIMITRY | Date:<br>2025-01-12<br>Revision:<br>+ (Unreleased) |
| Sheet Path:<br>/Project Architecture/LT3042_6V_5VA/   | Reviewer:                                   | Size:<br><b>A3</b>           | Sheet:<br><b>5 of 10</b>                           |

# [6] TPS61086\_3.3V\_to\_6V

A

COMP (pin 1) : broche de compensation de l'ampli d'erreur ; y connecter le réseau Rcomp + Ccomp vers AGND pour stabiliser la boucle (ne pas la router près de SW).

FB (pin 2) : entrée feedback ; à relier au pont diviseur R1/R2 depuis VOUT (après la diode) pour régler la tension de sortie (ex. 6 V).

EN (pin 3) : enable / shutdown ; niveau haut = actif, bas = arrêt. Souvent relié à IN pour "toujours ON", ou piloté par un GPIO.

AGND (pin 4) : masse analogique (référence des signaux sensibles : FB/COMP/SS/MODE). A garder "propre" et relier au plan GND de façon matrisée.

PGND (pin 5) : masse puissance (retour des courants de commutation). À relier au plan GND avec une zone cuivre courte/large et proche des capas de puissance.

SW (pins 6-7) : noeud switch (commutation) ; à connecter à L et à la diode Schottky. C'est le noeud le plus bruyant → piste courte, boucle minimale, éloignée de FB/COMP.

IN (pin 8) : entrée d'alimentation (2.3-6 V) ; à découpler au plus près avec Cby ~1 µF + Cin (ex. 10 µF) vers GND.

MODE (pin 9) : sélection du mode : MODE = High → Forced PWM (fréquence plus stable, mieux pour le bruit), MODE = Low → PFM (meilleur rendement à faible charge).

SS (pin 10) : soft-start ; mettre un condensateur (Css) pour limiter l'inrush au démarrage. Ouvert = pas de soft-start.

B

C

D

E

F

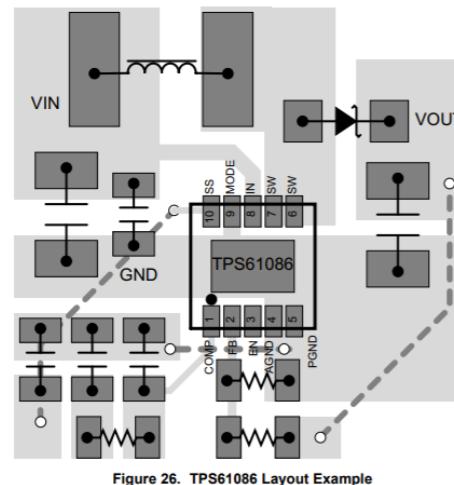
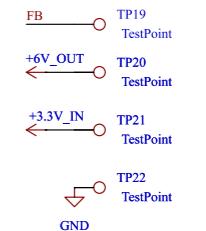
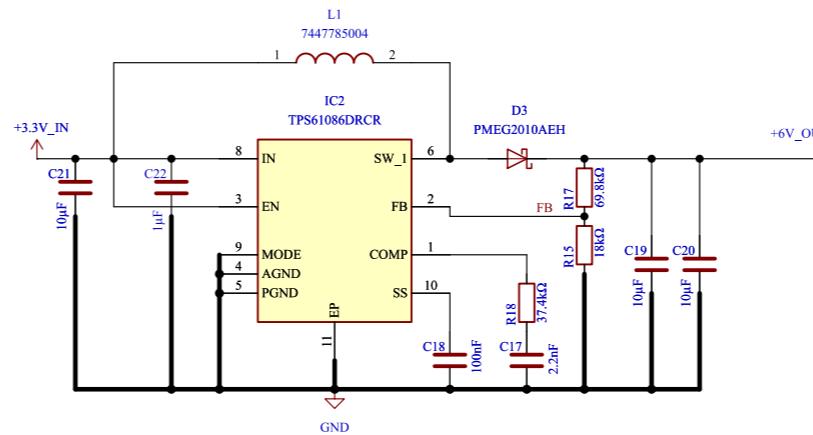


Figure 26. TPS61086 Layout Example

## Block Description

### Block Description

#### About

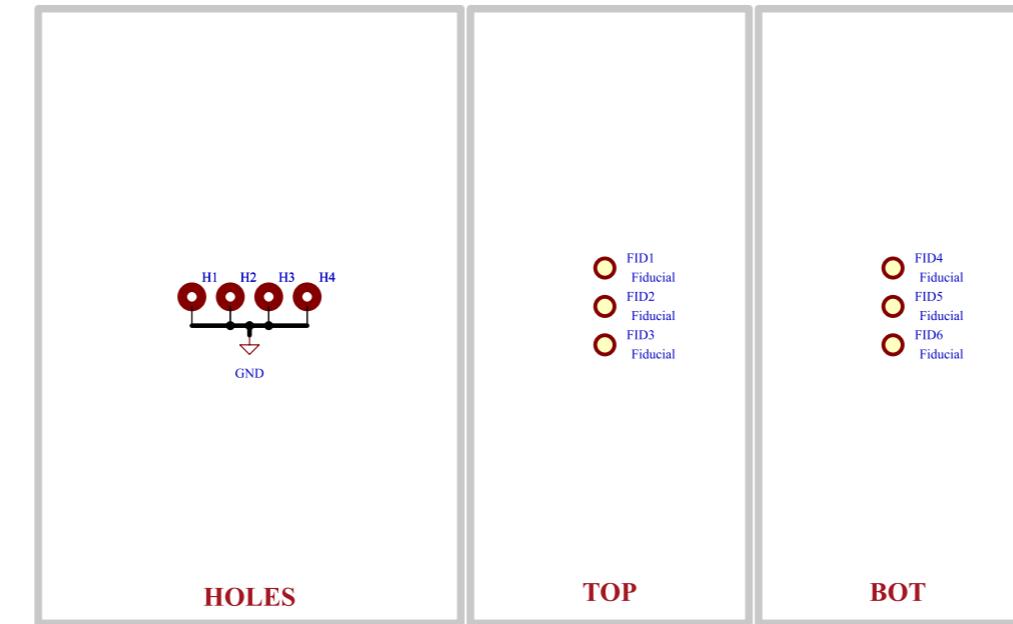
The TPS61086 device is a high-frequency, high-efficiency DC-to-DC converter with an integrated 2.0-A, 0.13-Ω power switch capable of providing an output voltage up to 18.5 V. The implemented boost converter is based on a fixed frequency of 1.2-MHz, pulse-width-modulation (PWM) controller that allows the use of small external inductors and capacitors and provides fast transient response.

At light-load, the device can operate in Power Save Mode with pulse-frequency-modulation (PFM) to improve the efficiency while keeping a low-output voltage ripple. For very noise-sensitive applications, the device can be forced to PWM Mode operation over the entire load range by pulling the MODE pin high. The external compensation allows optimizing the application for specific conditions. A capacitor connected to the soft-start pin minimizes inrush current at start-up.

## Block Description

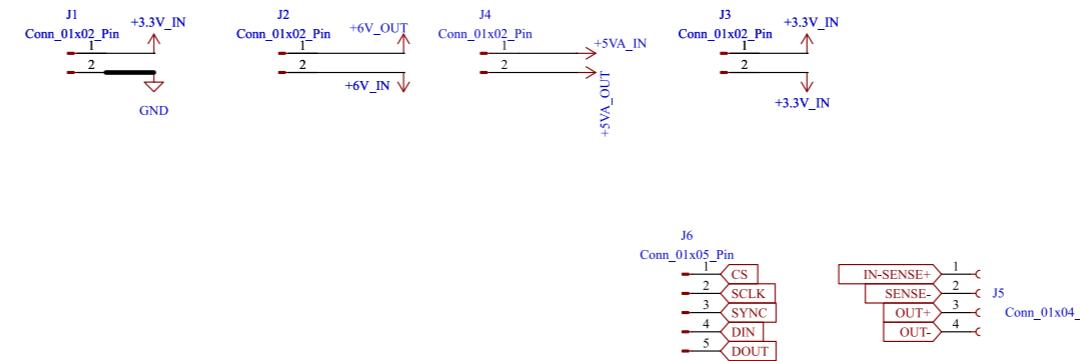
|   |   |                              |  |
|---|---|------------------------------|--|
| Comments:<br>References:<br>Flexible I/O worked examples<br>Flexible I/O source configuration | Company:<br><b>OPEN_TRUST_LAB</b>           | Variant:<br>DRAFT            | Git Hash:<br>f2c7d09                               |
| Board Name:<br><b>AD7190</b>  | Project Name:<br><b>OPEN_WEIGHT</b>         |                              |  |
| Sheet Title:<br>Sheet Title B   | File Name:<br>Section B - Title B.kicad_sch | Designer:<br>SIEBERT DIMITRY | Date:<br>2025-01-12<br>Revision:<br>+ (Unreleased) |
| Sheet Path:<br>/Project Architecture/TPS61086_3.3V_to_6V/                                     | Reviewer:                                   | Size:<br><b>A3</b>           | Sheet:<br><b>6 of 10</b>                           |

# [7]Holes, Fiducials



|  |   |   |                                     |  |
|--|---|---|-------------------------------------|--|
|  | Comments:<br>References:<br>Flexible I/O worked examples<br>Flexible I/O source configuration | Company:<br><b>OPEN_TRUST_LAB</b>           | Variant:<br>DRAFT                   | Git Hash:<br>f2c7d09                               |
|  | Board Name:<br><b>AD7190</b>  |   | Project Name:<br><b>OPEN_WEIGHT</b> |  |
|  | Sheet Title:<br>Sheet Title B   | File Name:<br>Section E - Title E.kicad_sch | Designer:<br>SIEBERT DIMITRY        | Date:<br>2025-01-12<br>Revision:<br>+ (Unreleased) |
|  | Sheet Path:<br>/Project Architecture/Holes, Fiducials/  |   | Reviewer:                           | Size:<br><b>A3</b><br>Sheet:<br><b>7 of 10</b>     |

# [8] Connecteur



DESIGN NOTE:  
blabla

DESIGN NOTE:  
blabla

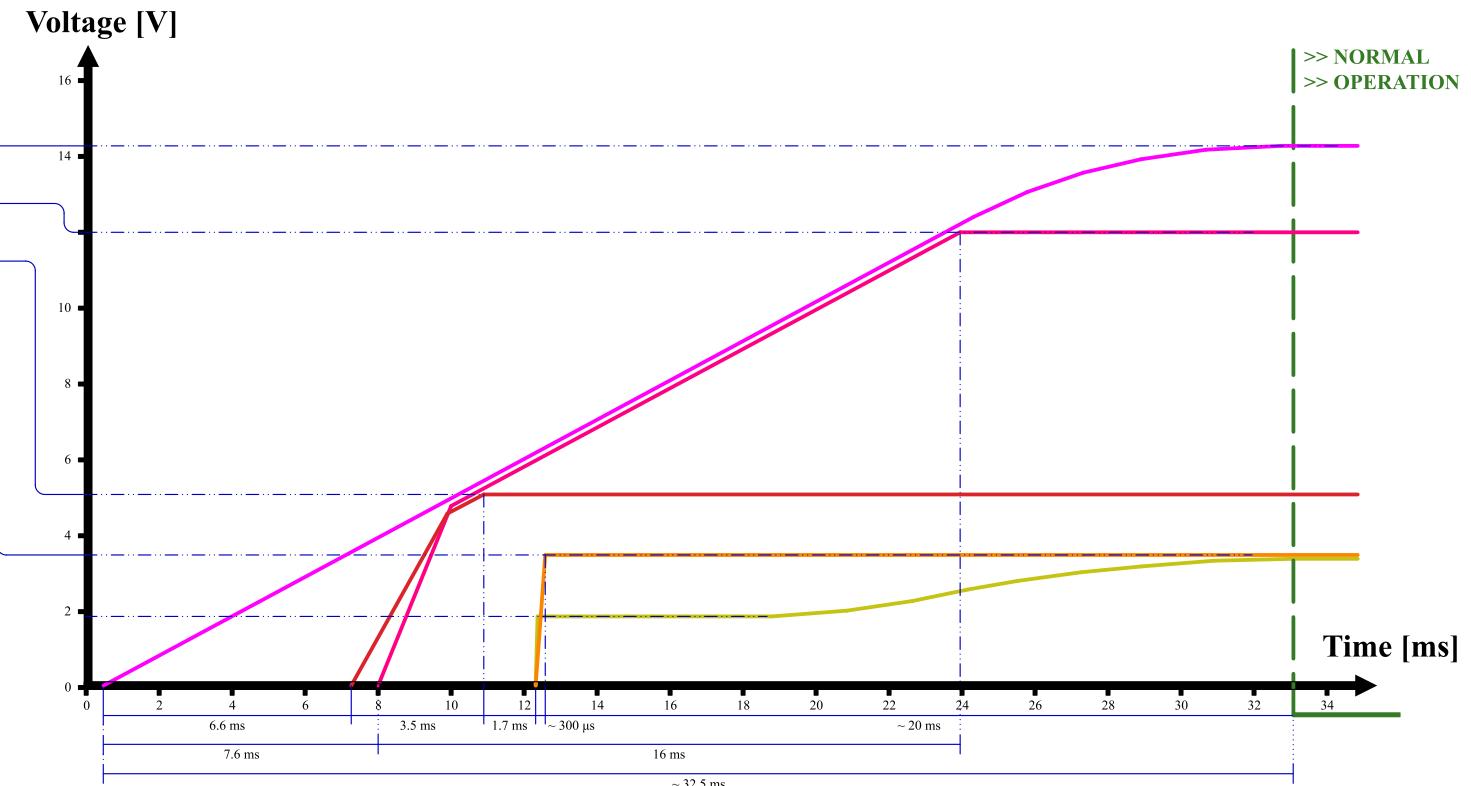
LAYOUT NOTE:  
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**Block Description**

|   |   |                                     |                                       |
|---|---|-------------------------------------|---------------------------------------|
| Comments:<br>References:<br>Flexible I/O worked examples<br>Flexible I/O source configuration | Company:<br><b>OPEN_TRUST_LAB</b>           | Variant:<br>DRAFT                   | Git Hash:<br>f2c7d09                  |
|   | Board Name:<br><b>AD7190</b>                | Project Name:<br><b>OPEN_WEIGHT</b> |                                       |
| Sheet Title:<br>Sheet Title B   | File Name:<br>Section D - Title D.kicad_sch | Designer:<br>SIEBERT DIMITRY        | Date:<br>2025-01-12<br>+ (Unreleased) |
| Sheet Path:<br>/Project Architecture/Connecteur/  | Reviewer:                                   | Size:<br><b>A3</b>                  | Sheet:<br><b>8 of 10</b>              |

# [9] Power - Sequencing

| NAME | SOURCE | LEVEL       |
|------|--------|-------------|
| +V?? | ??     | ? - ? ± ??% |
| +V?? | ??     | ? - ? ± ??% |
| +V?? | ??     | ? - ? ± ??% |
| +V?? | ??     | ? - ? ± ??% |
| +V?? | ??     | ? - ? ± ??% |



|                      |  |  |              |                              |                 |                           |  |  |
|----------------------|--|--|--------------|------------------------------|-----------------|---------------------------|--|--|
|                      |  |  | Comments:    | Company:                     | Variant:        | Git Hash:                 |  |  |
|                      |  |  |              | OPEN_TRUST_LAB               | DRAFT           | f2c7d09                   |  |  |
|                      |  |  | Board Name:  | AD7190                       | Project Name:   | OPEN_WEIGHT               |  |  |
|                      |  |  | Sheet Title: | File Name:                   | Date:           | Revision:                 |  |  |
| Power - Sequencing   |  |  |              | Power - Sequencing.kicad_sch | SIEBERT DIMITRY | 2025-01-12 + (Unreleased) |  |  |
| Sheet Path:          |  |  |              | Reviewer:                    | Size:           | Sheet:                    |  |  |
| /Power - Sequencing/ |  |  |              |                              | A4              | 9 of 10                   |  |  |

# [10] Revision History

|   |  |  |  |  |   |
|---|--|--|--|--|---|
| A |  |  |  |  | A |
| B |  |  |  |  | B |
| C |  |  |  |  | C |
| D |  |  |  |  | D |
|   |  |  |  |  |   |

|  |  |   |  |                                     |  |
|--|--|---|--|-------------------------------------|--|
|  |  | Comments:   | Company:<br><b>OPEN_TRUST_LAB</b>        | Variant:<br>DRAFT                   | Git Hash:<br>f2c7d09                               |
|  |  |   | Board Name:<br><b>AD7190</b>             | Project Name:<br><b>OPEN_WEIGHT</b> |  |
|  |  | Sheet Title:<br>Revision History                  | File Name:<br>Revision History.kicad_sch | Designer:<br>SIEBERT DIMITRY        | Date:<br>2025-01-12<br>Revision:<br>+ (Unreleased) |
|  |  | Sheet Path:<br><a href="#">/Revision History/</a> |  | Reviewer:                           | Size:<br><b>A4</b><br>Sheet:<br><b>10 of 10</b>    |