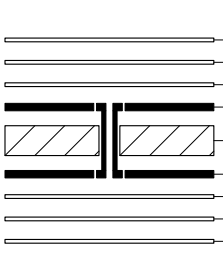
AD7190 Fabrication Document

Layer Stack Legend



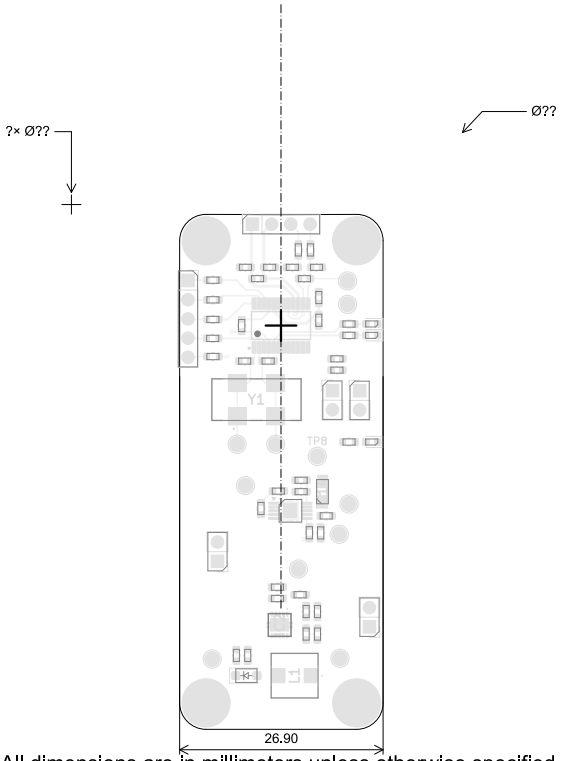
Material	Layer	Thickness	Dielectric	Type	Gerber
	F.Paste			Paste Mask	
	F.Silkscreen		Direct Printing	Legend	GBR
	F.Mask	0.02mm	Solder Resist	Solder Mask	GBR
Copper	**L1 (Sig, PWR)**	**0.07mm (2.00oz)**		**Signal**	**GBR**
Core		1.48mm	FR4_7628	Dielectric	
Copper	**L6 (Sig, PWR)**	**0.07mm (2.00oz)**		**Signal**	**GBR**
	B.Mask	0.02mm	Solder Resist	Solder Mask	GBR
	B.Silkscreen		Direct Printing	Legend	GBR
	B.Paste			Paste Mask	

Total thickness: 1.66mm
Note: external layer thicknesses are specified after plating

Impedance Table

Transmission Line	Impedance [ohms]	Tolerance [ohms]	Layer	Trace Width [mm]	Gap [mm]	Ref. Layers
Edge-Coupled Coated Microstrip	100	±10 %	L1	0.2032	0.28	L2

Top Fabrication (Scale 1:1)



All dimensions are in millimeters unless otherwise specified.

FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

1) FABRICATE PER IPC-6012A CLASS 2.

2) OUTLINE DEFINED IN SEPARATE GERBER FILE WITH "Edge_Cuts.GBR" SUFFIX.

   DIMENSIONS OF CIRCUMSIZED RECTANGLE SHOWN ON THIS DRAWING FOR REFERENCE ONLY.

3) SEE SEPARATE DRILL FILES WITH ".DRL" SUFFIX FOR HOLE LOCATIONS.

   SELECTED HOLE LOCATIONS SHOWN ON THIS DRAWING FOR REFERENCE ONLY.

4) SURFACE FINISH: IMMERSION GOLD

5) SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR BLACK.

6) SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING YELLOW NON-CONDUCTIVE EPOXY INK.

7) ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.

8) VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING

9) PCB MATERIAL REQUIREMENTS:

   A. FLAMMABILITY RATING MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.
   B. Tg 170 C OR EQUIVALENT.
   C. EQUIVALENT MATERIAL SHALL BE RoHS COMPLIANT, HALOGEN FREE AND APPROVED BY OPEN_TRUST_LAB.

10) DESIGN GEOMETRY MINIMUM FEATURE SIZES:

BOARD SIZE	26.901 × 68.100 mm
BOARD THICKNESS	1.660 mm
TRACE WIDTH	0.200 mm
TRACE TO TRACE	0.200 mm
MIN. HOLE (PTH)	0.200 mm
MIN. HOLE (NPTH)	N/A mm
ANNULAR RING	0.150 mm
COPPER TO HOLE	0.254 mm
COPPER TO EDGE	0.250 mm
HOLE TO HOLE	0.254 mm

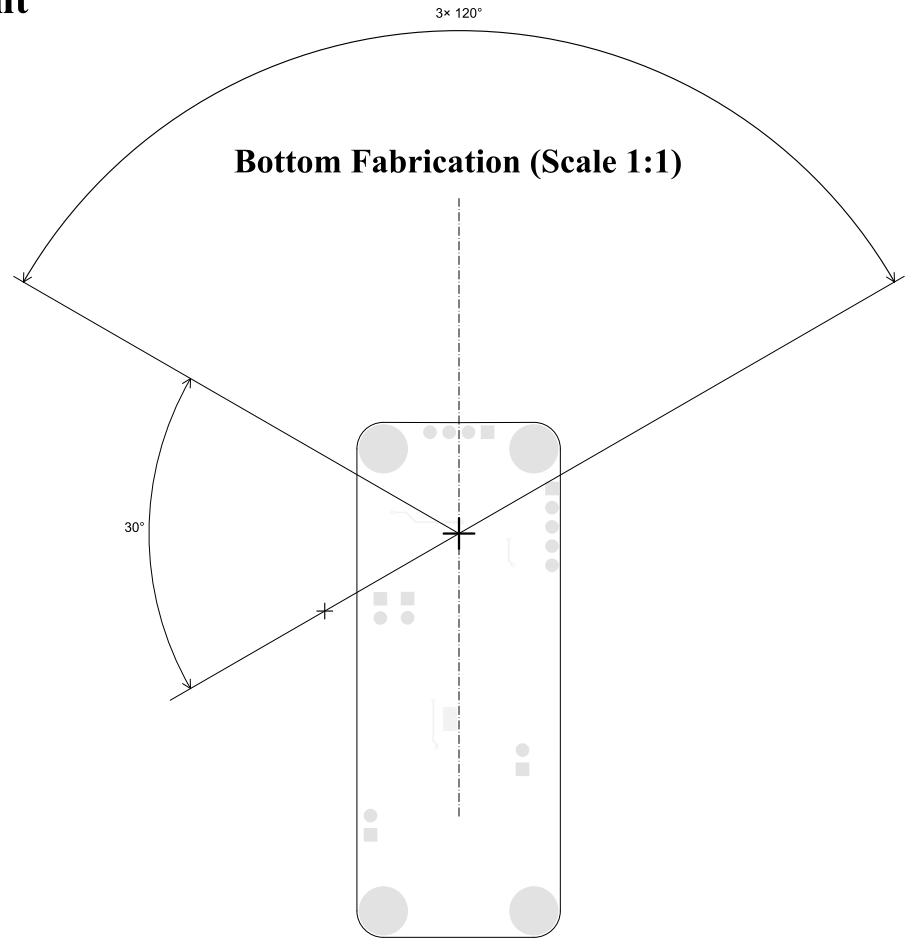
11) REFER TO IMPEDANCE TABLE FOR IMPEDANCE CONTROL REQUIREMENTS.

12) CONFIRM SPACE WIDTHS AND SPACINGS.

Comments:	Company: OPEN_TRUST_LAB		Variant: PRELIMINARY	Git Hash: 0bfb00e
	Board Name: AD7190		Project Name: OPEN_WEIGHT	
Sheet Title: Top Fabrication (Scale 1:1)	File Name: Cellule_de_force_V2.kicad_pcb	Designer: SIEBERT DIMITRY	Date: 2024-04-13	Revision: + (Unreleased)
Sheet Path:		Reviewer:	Size: A4	Sheet: 1 of 7

AD7190 Fabrication Document

Bottom Fabrication (Scale 1:1)



All dimensions are in millimeters unless otherwise specified.

	Comments:	Company: OPEN_TRUST_LAB		Variant: PRELIMINARY	Git Hash: 0bfb00e
		Board Name: AD7190		Project Name: OPEN_WEIGHT	
	Sheet Title: Bottom Fabrication (Scale 1:1)	File Name: Cellule_de_force_V2.kicad_pcb	Designer: SIEBERT DIMITRY	Date: 2024-04-13	Revision: + (Unreleased)
	Sheet Path:		Reviewer:	Size: A4	Sheet: 2 of 7

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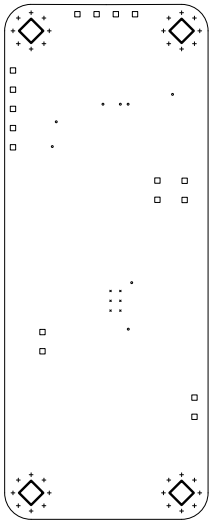
Drill Table

Symbol	Count	Hole Size	Plated	Hole Shape	Drill Layer Pair	Hole Type
×	6	0.20mm (7.87mils)	PTH	Round	L1 (Sig, PWR) - L6 (Sig, PWR)	Pad
○	8	0.25mm (9.84mils)	PTH	Round	L1 (Sig, PWR) - L6 (Sig, PWR)	Via
+	32	0.50mm (19.69mils)	PTH	Round	L1 (Sig, PWR) - L6 (Sig, PWR)	Pad
□	17	1.00mm (39.37mils)	PTH	Round	L1 (Sig, PWR) - L6 (Sig, PWR)	Pad
◇	4	3.20mm (125.98mils)	PTH	Round	L1 (Sig, PWR) - L6 (Sig, PWR)	Pad
	Total 67					

Drill Drawing L1 - L2 (Scale 1:1)



	Comments:	Company: OPEN_TRUST_LAB		Variant: PRELIMINARY	Git Hash: 0bfb00e
		Board Name: AD7190		Project Name: OPEN_WEIGHT	
	Sheet Title: Drill Drawing (L1 - L2)	File Name: Cellule_de_force_V2.kicad_pcb	Designer: SIEBERT DIMITRY	Date: 2024-04-13	Revision: + (Unreleased)
	Sheet Path:		Reviewer:	Size: A4	Sheet: 3 of 7

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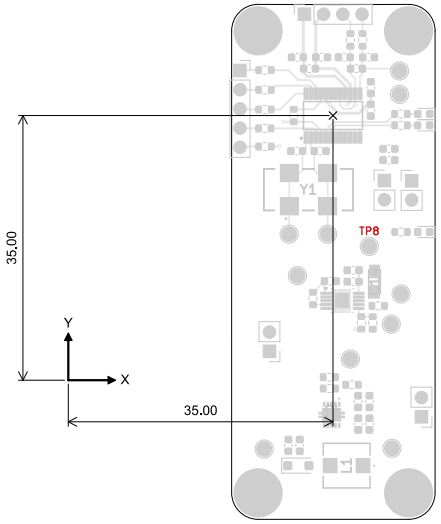
Top Test Points (Scale 1:1)

Ref.	Net	X [mm]	Y [mm]
TP1		-64.00	106.00
TP2		-64.00	106.00
TP3	OUT+	93.30	21.90
TP4	OUT-	93.30	18.80
TP5		-64.00	106.00
TP6	+3.3V_IN	92.30	-28.00
TP7		-64.00	106.00
TP8	+5VA_OUT	89.30	-1.30
TP14	MCLK1	78.70	0.30
TP15	MCLK2	83.80	0.30
TP16	+6V_IN	79.80	-5.17
TP17	SET	93.50	-7.60
TP18	PGFB	92.20	-11.60
TP19	FB	86.80	-16.20
TP20	+6V_OUT	75.40	-28.10
TP21		-64.00	106.00
TP22		-64.00	106.00
TP23		-64.00	106.00

Ref.	Net	X [mm]	Y [mm]



All dimensions are in millimeters unless otherwise specified.

	Comments:	Company: OPEN_TRUST_LAB		Variant: PRELIMINARY	Git Hash: 0bfb00e
		Board Name: AD7190		Project Name: OPEN_WEIGHT	
	Sheet Title: Top Test Points (Scale 1:1)	File Name: Cellule_de_force_V2.kicad_pcb	Designer: SIEBERT DIMITRY	Date: 2024-04-13	Revision: + (Unreleased)
	Sheet Path:		Reviewer:	Size: A4	Sheet: 4 of 7

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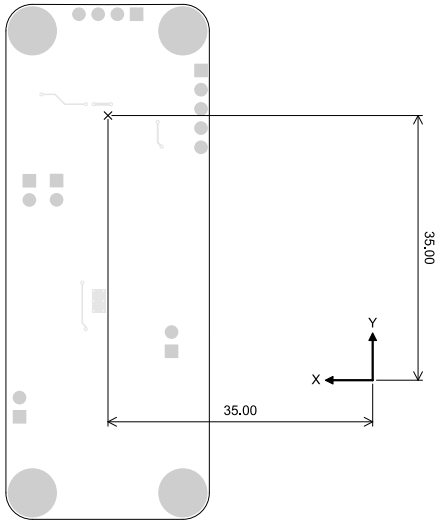
Bottom Test Points (Scale 1:1)

Ref.	Net	X [mm]	Y [mm]



All dimensions are in millimeters unless otherwise specified.

	Comments:	Company: OPEN_TRUST_LAB		Variant: PRELIMINARY	Git Hash: 0bfb00e
		Board Name: AD7190		Project Name: OPEN_WEIGHT	
	Sheet Title: Bottom Test Points (Scale 1:1)	File Name: Cellule_de_force_V2.kicad_pcb	Designer: SIEBERT DIMITRY	Date: 2024-04-13	Revision: + (Unreleased)
	Sheet Path:		Reviewer:	Size: A4	Sheet: 5 of 7

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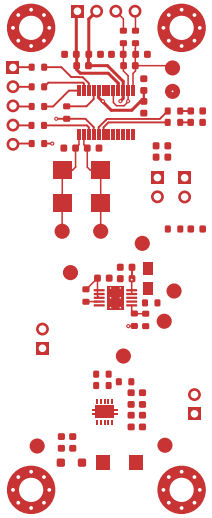
L1 (Sig, PWR) (Scale 1:1)



	Comments:	Company: OPEN_TRUST_LAB		Variant: PRELIMINARY	Git Hash: 0bfb00e
		Board Name: AD7190		Project Name: OPEN_WEIGHT	
	Sheet Title: L1 (Sig, PWR) (Scale 1:1)	File Name: Cellule_de_force_V2.kicad_pcb	Designer: SIEBERT DIMITRY	Date: 2024-04-13	Revision: + (Unreleased)
	Sheet Path:		Reviewer:	Size: A4	Sheet: 6 of 7

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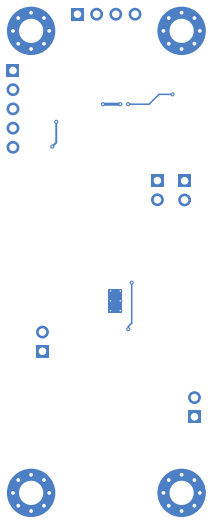
L6 (Sig, PWR) (Scale 1:1)



	Comments:	Company: OPEN_TRUST_LAB		Variant: PRELIMINARY	Git Hash: 0bfb00e
		Board Name: AD7190		Project Name: OPEN_WEIGHT	
	Sheet Title: L6 (Sig, PWR) (Scale 1:1)	File Name: Cellule_de_force_V2.kicad_pcb	Designer: SIEBERT DIMITRY	Date: 2024-04-13	Revision: + (Unreleased)
	Sheet Path:		Reviewer:	Size: A4	Sheet: 7 of 7