

1 2 3 4 5 6 7 8

A A

AD7190

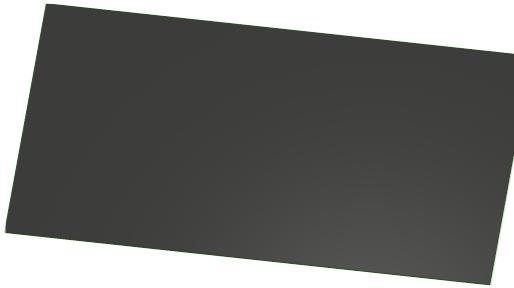
Variant: DRAFT

2026-02-24

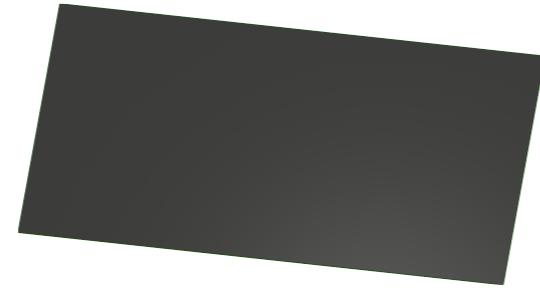
Rev + (Unreleased)

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TOP VIEW



BOTTOM VIEW



NOTES

Comment

Not fitted components are marked as

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There shouldn't be any mistakes. Contact the engineer if you find any.

RELEASED - A board with this schematic has been sent to production.

Date: 24-Feb-2026

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for debug notes.

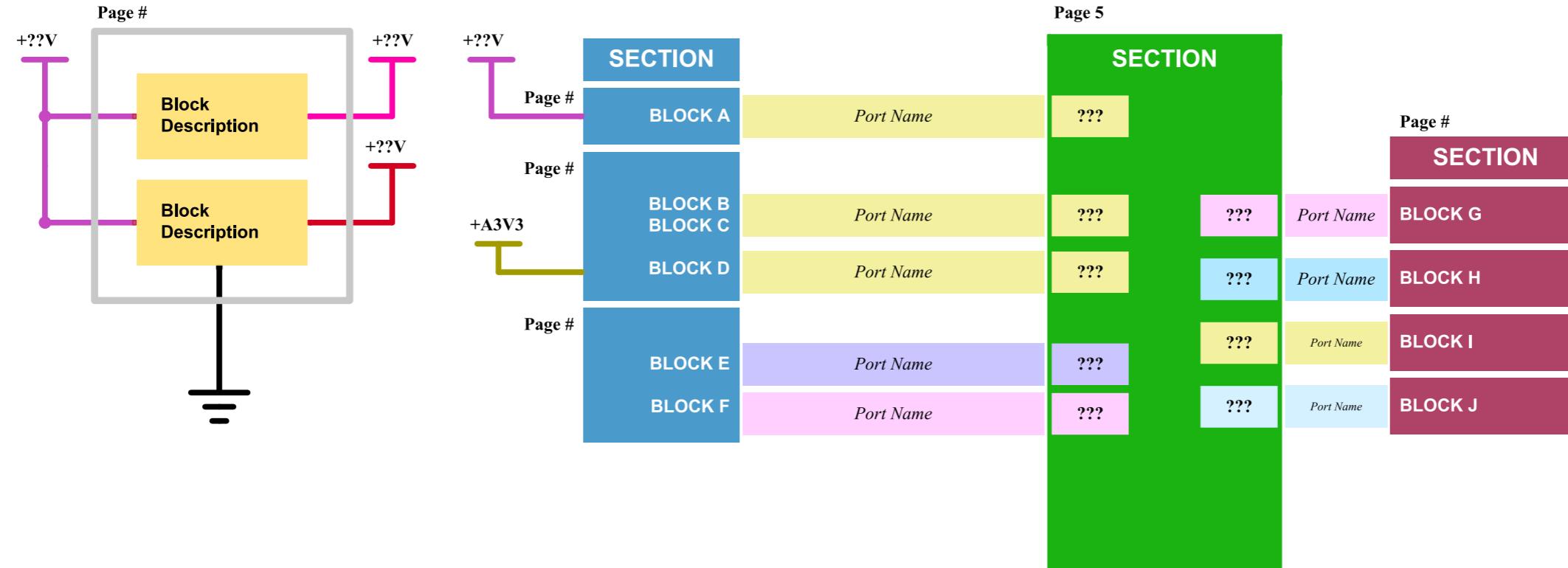
DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

	Comments:	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
	Board Name: AD7190	Project Name: OPEN_WEIGHT		
	Sheet Title: File Name: Cellule_de_force_V2.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12	Revision: + (Unreleased)
	Sheet Path: /	Reviewer:	Size: A3	Sheet: 1 of 10

[2] Block Diagram

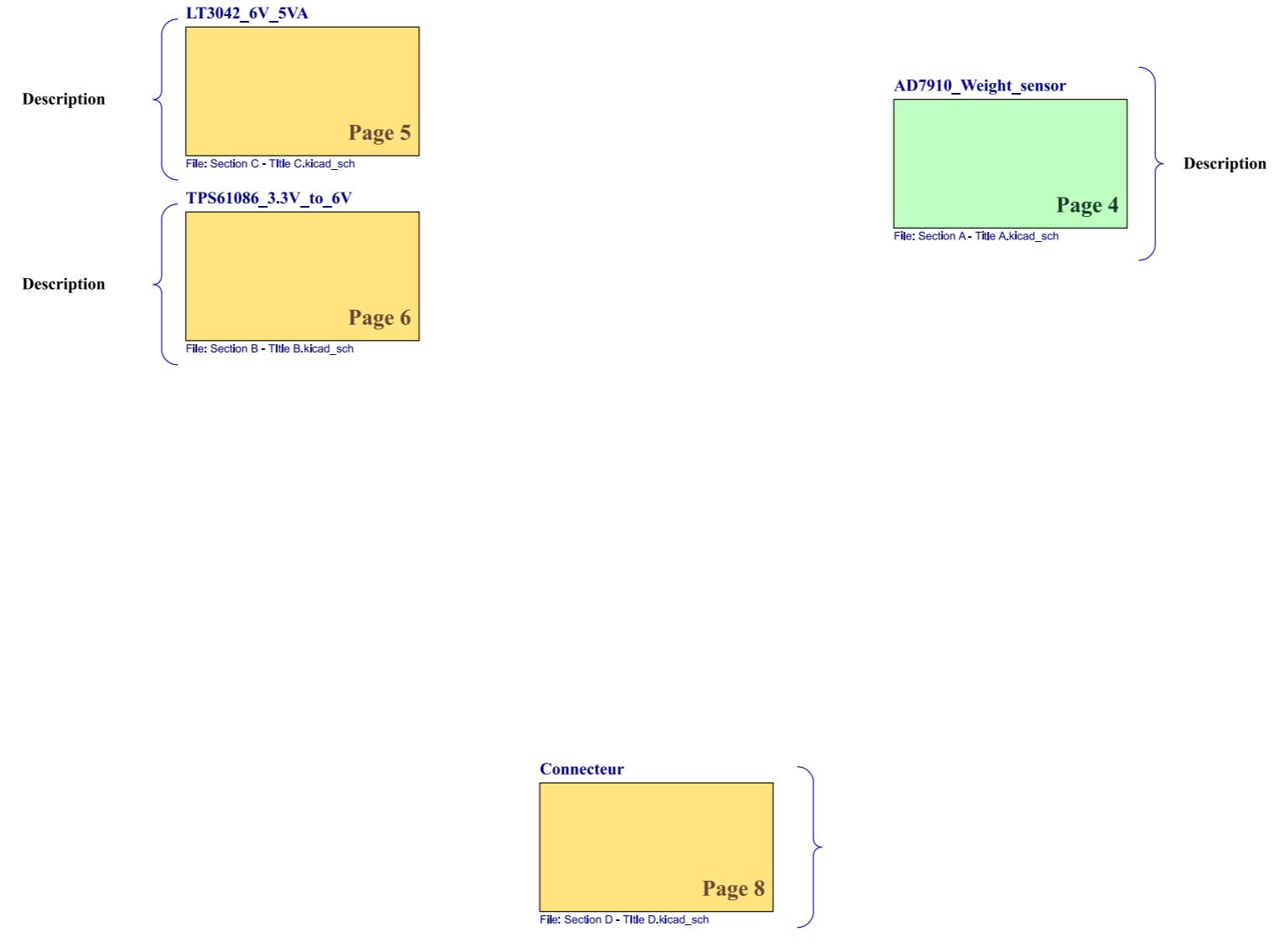


Target specifications:

Input voltage:	?? - ?? V
Spec 2	??
Spec 3	??
Spec 4	??

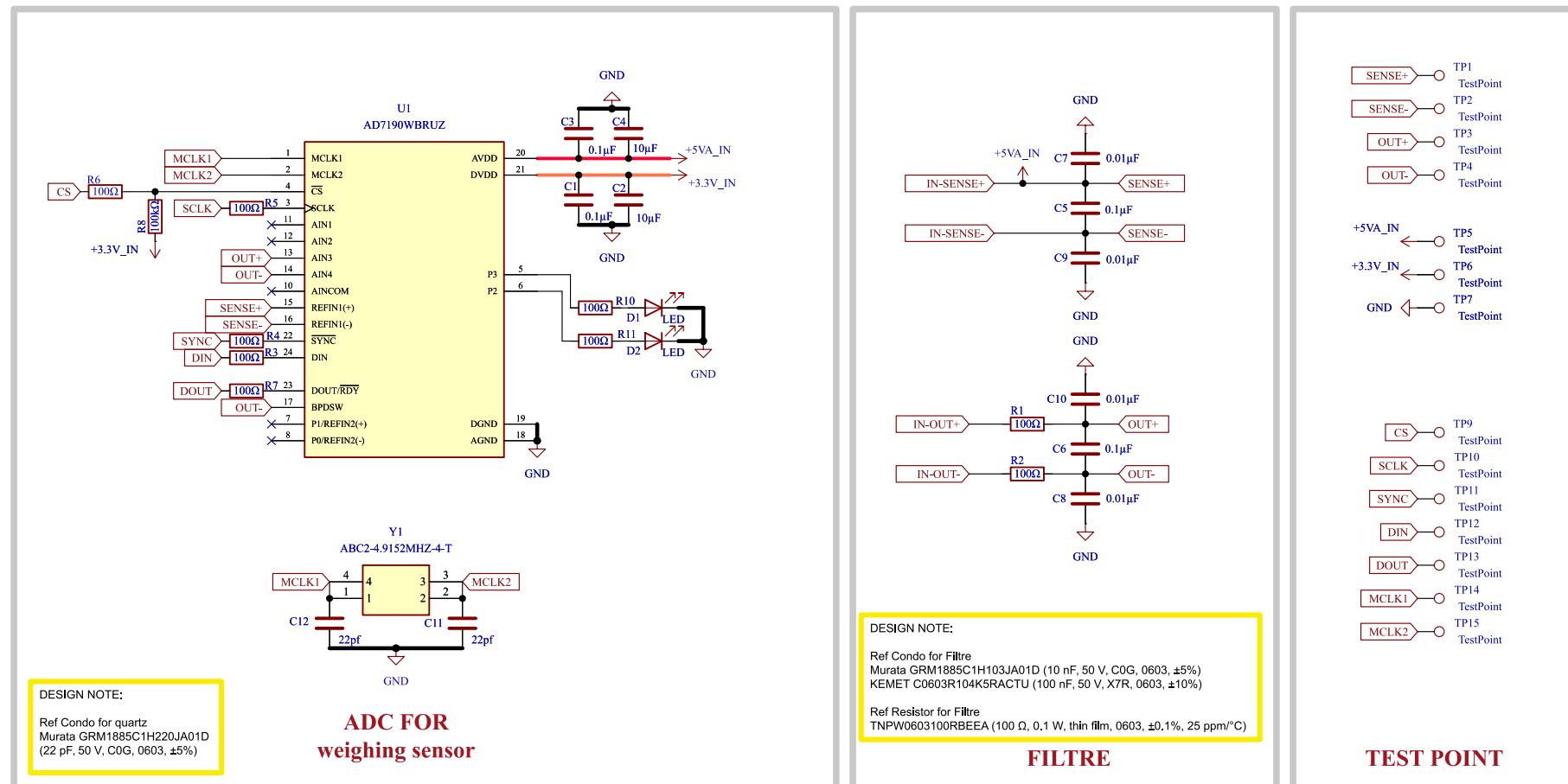
	Comments:	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
		Board Name: AD7190	Project Name: OPEN_WEIGHT	
	Sheet Title: Block Diagram	File Name: Block Diagram.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 + (Unreleased)
	Sheet Path: /Block Diagram/		Reviewer:	Size: A3 Sheet: 2 of 10

[3] Project Architecture



	Comments:	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
	Board Name: AD7190		Project Name: OPEN_WEIGHT	
	Sheet Title: Project Architecture	File Name: Project Architecture.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 + (Unreleased)
	Sheet Path: /Project Architecture/		Reviewer:	Size: A3 Sheet: 3 of 10

[4] Sheet Title A



About

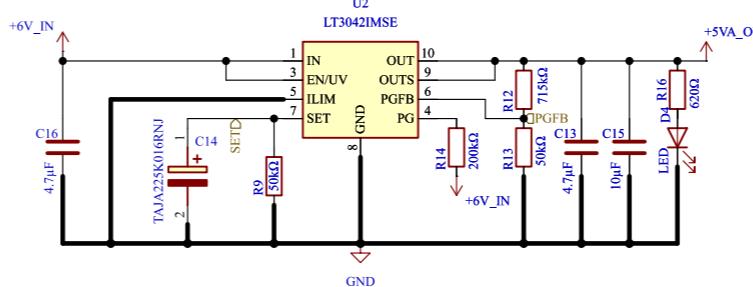
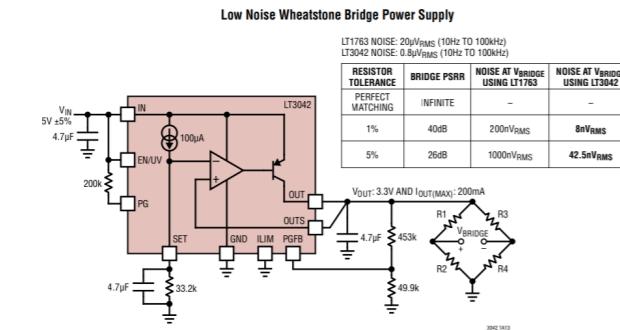
The AD7190 is a low noise, complete analog front end for high precision measurement applications. It contains a low noise, 24-bit sigma-delta ($\Sigma\Delta$) analog-to-digital converter (ADC). The on-chip low noise gain stage means that signals of small amplitude can be interfaced directly to the ADC. The device can be configured to have two differential inputs or four pseudo differential inputs. The on-chip channel sequencer allows several channels to be enabled, and the AD7190 sequentially converts on each enabled channel. This simplifies communication with the part. The on-chip 4.92 MHz clock can be used as the clock source to the ADC or, alternatively, an external clock or crystal can be used. The output data rate from the part can be varied from 4.7 Hz to 4.8 kHz. The device has two digital filter options. The choice of filter affects the rms noise/noise-free resolution at the programmed output data rate, the settling time, and the 50 Hz/60 Hz rejection.

Comments: AN5346 STM32G474 Datasheet p.81 J. Pieper ADC investigation	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
Board Name: AD7190	Project Name: OPEN_WEIGHT		
Sheet Title: Sheet Title A	File Name: Section A - Title A.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12
Sheet Path: /Project Architecture/AD7910_Weight_sensor/	Reviewer:	Size: A4	Revision: + (Unreleased)

[5] Sheet Title B

A
IN (pins 1-2) : entrée d'alimentation du LT3042 (6V), à découpler avec CIN.
EN/UV (pin 3) : active/désactive le régulateur et permet un seuil UVLO (souvent relié à IN pour "toujours ON").
PG (pin 4) : sortie Power-Good open-collector (nécessite une résistance pull-up).
ILIM (pin 5) : programmation/monitoring de la limite de courant (souvent à GND si non utilisé).
PGFB (pin 6) : entrée qui fixe le seuil de Power-Good via un pont diviseur depuis VOUT.
SET (pin 7) : règle la tension de sortie via RSET (et CSET réduit le bruit/soft-start).
GND (pin 8) : masse de référence du circuit.
OUTS (pin 9) : sense Kelvin de la sortie (à relier au + de COUT / point de charge).
OUT (pin 10) : sortie régulée (5V), à découpler avec COUT.
EPAD (pad exposé) : masse + dissipation thermique (à souder sur plan GND).

TYPICAL APPLICATIONS



D
DESIGN NOTE:
Ref Condo for SET PIN (important pour les vibrations P16)
KYOCERA AVX TAJA225K016RNJ (2.2 µF, 16 VDC,
condensateur tantalique solide SMD moulé, 1206 / 3216 (A case),
±10%, ESR 6.5 Ω).

V_{OUT} = I_{SET} × R_{SET}
I_{SET} ≈ 100 µA

Donc :
R_{SET} = V_{OUT} / I_{SET}
R_{SET} = 5.0 V / 100 µA = 50 kΩ
(=> valeur standard recommandée : 49.9 kΩ)

V_{OUT(PG_THRESHOLD)} = 0.3 V × (1 + RPG2/RPG1)
PGFB_THRESHOLD = 0.3 V

Donc :
RPG2 = RPG1 × (V_{OUT(PG)}/0.3 V - 1)

Exemple (PG OK à ~4.8 V) :
Choix RPG1 = 49.9 kΩ
RPG2 = 49.9 kΩ × (4.8/0.3 - 1) = 748.5 kΩ
(=> valeur standard recommandée : 750 kΩ)

Design guide line

Block Description

Convertisseur 5VA

Block Description

TEST POINT

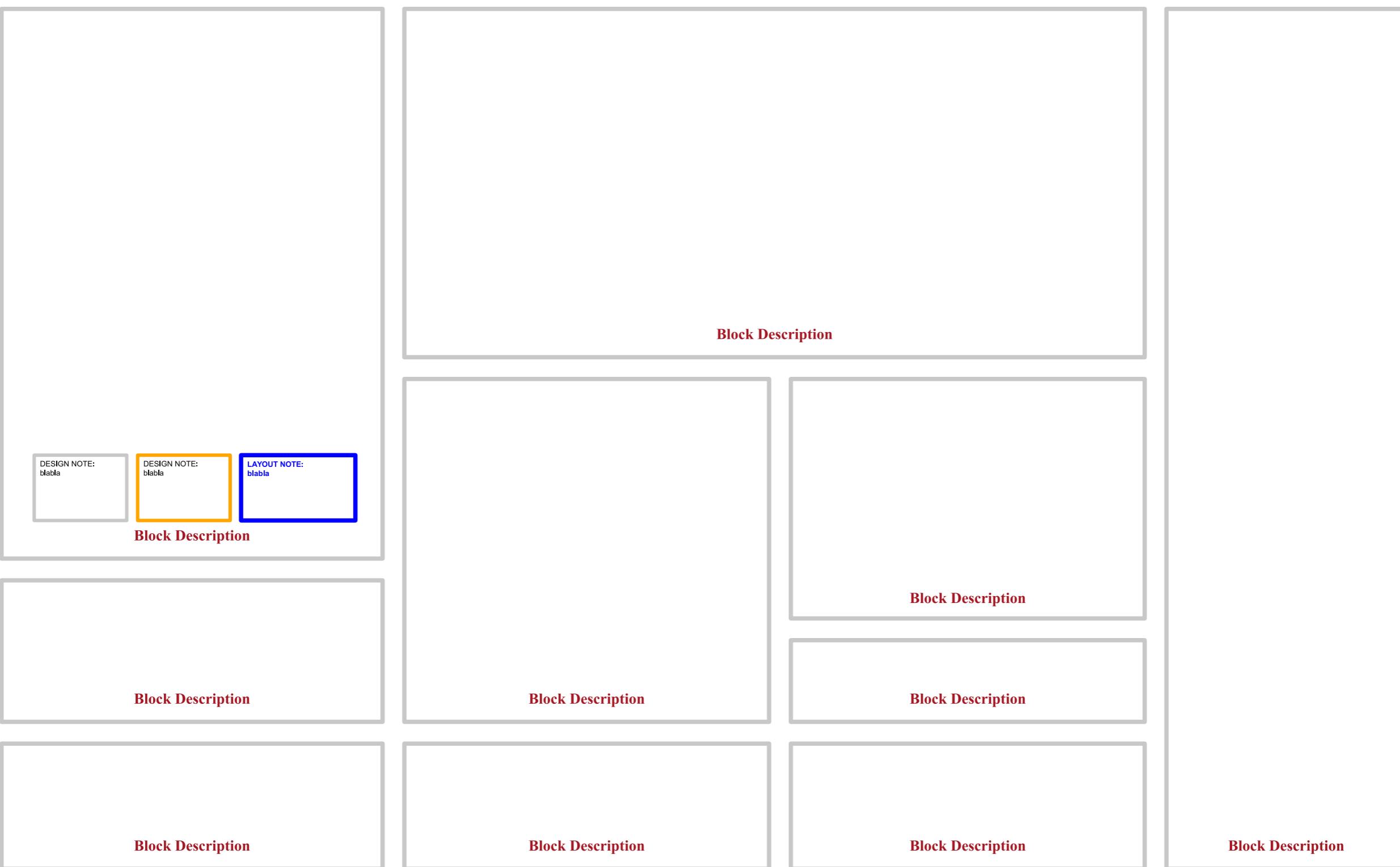
Comments: References: Flexible I/O worked examples Flexible I/O source configuration	Company: OPEN_TRUST_LAB	Variant: DRAFT	
		Board Name: AD7190	Project Name: OPEN_WEIGHT
Sheet Title: Sheet Title B	File Name: Section C - Title C.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 Revision: + (Unreleased)
Sheet Path: /Project Architecture/LT3042_6V_5VA/	Reviewer:	Size: A3	Sheet: 5 of 10

[6] Sheet Title B



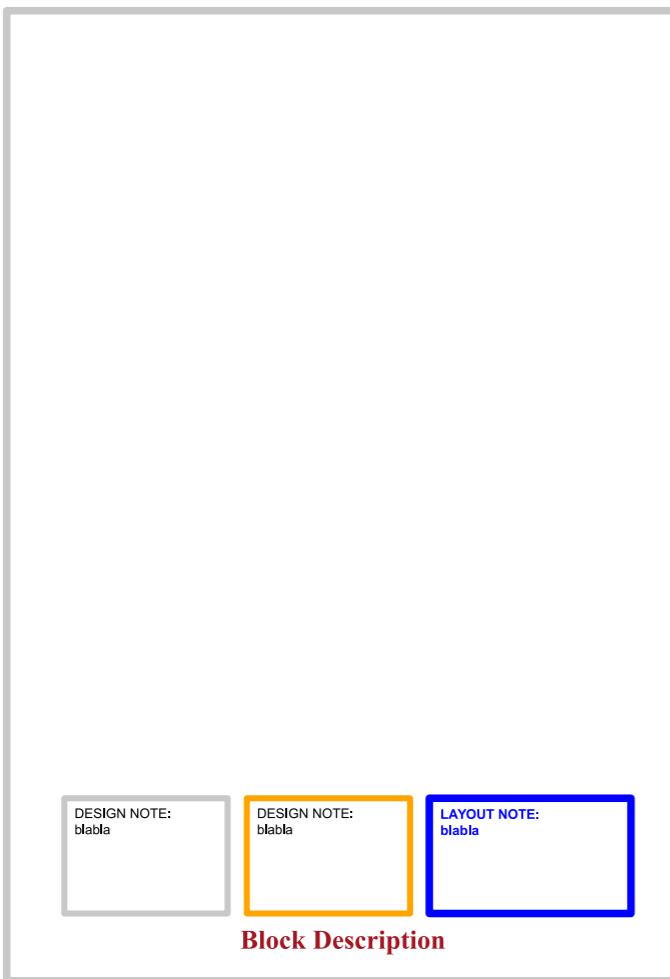
	Comments: References: Flexible I/O worked examples Flexible I/O source configuration	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
	Board Name: AD7190		Project Name: OPEN_WEIGHT	
	Sheet Title: Sheet Title B	File Name: Section B - Title B.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 Revision: + (Unreleased)
	Sheet Path: /Project Architecture/TPS61086_3.3V_to_6V/		Reviewer:	Size: A3 Sheet: 6 of 10

[7] Sheet Title B



	Comments: References: Flexible I/O worked examples Flexible I/O source configuration	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
	Board Name: AD7190		Project Name: OPEN_WEIGHT	
	Sheet Title: Sheet Title B	File Name: Section E - Title E.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 Revision: + (Unreleased)
	Sheet Path: /Project Architecture/Holes, Fiducials/		Reviewer:	Size: A3 Sheet: 7 of 10

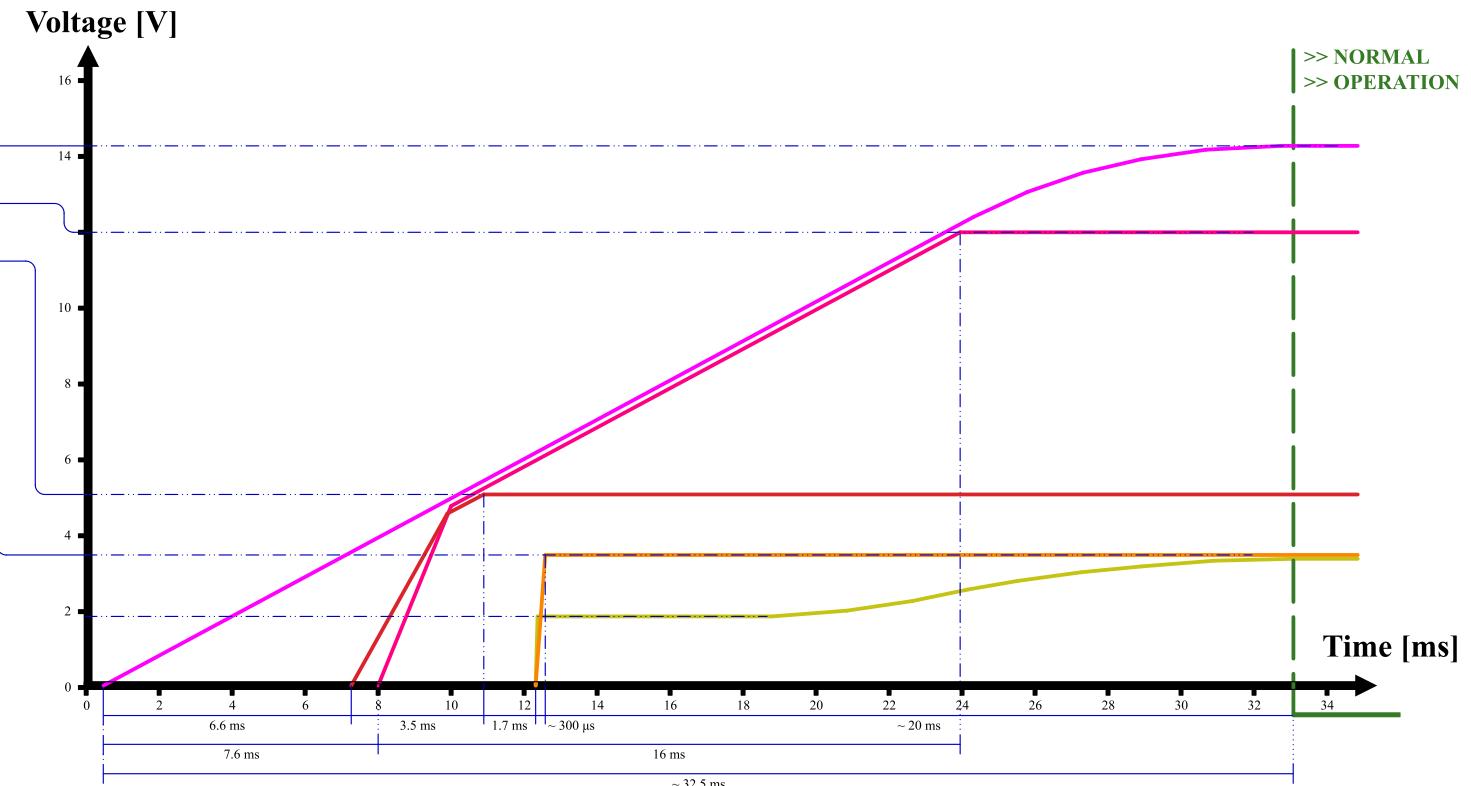
[8] Sheet Title B



	Comments: References: Flexible I/O worked examples Flexible I/O source configuration	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
	Board Name: AD7190		Project Name: OPEN_WEIGHT	
	Sheet Title: Sheet Title B	File Name: Section D - Title D.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 Revision: + (Unreleased)
	Sheet Path: /Project Architecture/Connecteur/		Reviewer:	Size: A3 Sheet: 8 of 10

[9] Power - Sequencing

NAME	SOURCE	LEVEL
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%



			Comments:	Company:	Variant:	Git Hash:	
				OPEN_TRUST_LAB	DRAFT	f2c7d09	
			Board Name:	Project Name:			
			AD7190	OPEN_WEIGHT			
Sheet Title:		File Name:	Designer:	Date:	Revision:		
Power - Sequencing		Power - Sequencing.kicad_sch	SIEBERT DIMITRY	2025-01-12	+ (Unreleased)		
Sheet Path:		Reviewer:		Size:	Sheet:		
/Power - Sequencing/		A4		9	of 10		

[10] Revision History

A					A
B					B
C					C
D					D

		Comments:	Company: OPEN_TRUST_LAB	Variant: DRAFT	Git Hash: f2c7d09
			Board Name: AD7190	Project Name: OPEN_WEIGHT	
		Sheet Title: Revision History	File Name: Revision History.kicad_sch	Designer: SIEBERT DIMITRY	Date: 2025-01-12 Revision: + (Unreleased)
		Sheet Path: /Revision History/		Reviewer:	Size: A4 Sheet: 10 of 10