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Distortion Cancellation in Time-Interleaved ADCs

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Distortion Cancellation in Time-Interleaved ADCs

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Summary
Time-Interleaved Analog to Digital Converters (TI ADC) consist of several individual sub-converters operating at a lower sampling rate, working in parallel, and in a circular loop. Thereby, they are increasing the sampling rate without compromising on the resolution during conversion, at high sampling rates. The latter is the main requirement in the area of radio frequency sampling. However, they suffer from mismatches caused by the different characteristics in each sub-converter and the TI structure. The TI ADC's output contains a lot of harmonics and spurious tones due to the non-linearities mismatch between the sub-converters. Therefore, previously frequency planning was performed to avoid the input signal from coinciding with these harmonic bins. More importance has been given to digital calibration in recent years where algorithms are developed and implemented outside ADC in a Digital signal processor (DSP), whereas the compensation is done in real time. In this work, we model the distortions and the harmonics present in the TI ADC output. A post-correction block is developed for the cancellation of the characterized harmonics. The suggested method is tested on the TI ADC working at radio frequencies, but is valid also for other types of ADCs such as pipeline ADCs and sigma-delta ADCs.
Nyckelord
Time-Interleaved ADC, Post correction, Blind calibration, Harmonics cancellation, Mismatch analysis, Linearisation

ABSTRACT

Time-Interleaved Analog to Digital Converters (TI ADC) consist of several individual sub-converters operating at a lower sampling rate, working in parallel, and in a circular loop. Thereby, they are increasing the sampling rate without compromising on the resolution during conversion, at high sampling rates. The latter is the main requirement in the area of radio frequency sampling. However, they suffer from mismatches caused by the different characteristics in each sub-converter and the TI structure.

The output of the TI ADC under consideration contains a lot of harmonics and spurious tones due to the non-linearities mismatch between the sub-converters. Therefore, previously extensive frequency planning was performed to avoid the input signal from coinciding with these harmonic bins. More importance has been given to digital calibration in recent years where algorithms are developed and implemented outside ADC in a Digital signal processor (DSP), whereas the compensation is done in real time.

In this work, we model the distortions and the harmonics present in the TI ADC output to get a clear understanding of the TI ADC. A post-correction block is developed for the cancellation of the characterized harmonics. The suggested method is tested on the TI ADCs working at radio frequencies, but is valid also for other types of ADCs, such as pipeline ADCs and sigma-delta ADCs.

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LIST OF ABBREVIATIONS

Abbreviation	Meaning
F_{samp}	Sampling frequency of the TI ADC
B_w	Signal bandwidth
F_i	Input signal frequency
F_a	Frequency of the aliased signal
B	Number of bits (resolution of conversion)
N	Number of sub-converters in the TI ADC
$x(t)$	Continuous input signal to the TI ADC
T_s	Sampling period of the individual sub-converters in the TI ADC
F_s	Sampling frequency of the individual sub-converters in the TI ADC
M	Number of samples considered in the time domain
n	Nyquist Zone
w_k	Normalized angular frequency
$A1, A2$	Amplitudes of the sinusoidal signals used for the model simulation
$\alpha_1, \alpha_2, \alpha_3,$	Gain mismatches of the last three sub-converters respectively
o_1, o_2, o_3	Offset mismatches of the last three sub-converters respectively
$\Delta t_1, \Delta t_2, \Delta t_3$	Skew mismatches of the last three sub-converters respectively

LIST OF ACRONYMS

Acronym	Meaning	Description	Context
ADC	Analog to Digital Converter	A device used to convert an analog signal to a digital signal.	In Chapter 2
DFT	Discrete Fourier Transform	It is a transform that deals with finite discrete time signal and a discrete number of frequencies.	In Chapter 3,4
DSP	Digital Signal Processing	It is a field in signal processing where digital signals are used to perform manipulations such as filtering, compressing, etc. of an analog signal.	In Chapter 1
FPGA	Field programmable gate array	It is an integrated circuit which could be configured by the user after it is manufactured.	In Chapter 1, 6
GSps	Giga Samples per second	It is bit rate and depicts as to how many bits are processed per unit time. In this case 10^9 bits are processed per second.	In Chapter 2
ISY	An Institution in the University of Linköping	One of the departments at Linköping institute of technology. Department of electrical engineering in English.	Front page
kSps	Kilo samples per second	It is bit rate and in this case 10^3 bits are processed per second.	In Chapter 2
LSB	Least Significant Bit	It represents the unit's value in the binary integer format and determines if a number is odd or even.	In Chapter 2
MUX	Multiplexer	It is a device allowing one or more low-speed analog or digital input signals to be selected, combined and transmitted at a higher speed on a single shared medium or within a single shared device.	In the TI ADC. Figure 2.4.1, Figure 3.1.1
MSps	Mega Samples per second	It is bit rate and in this case 10^6 bits are processed per second.	In Chapter 2

SAR	Successive Approximation Register	Sub class of ADCs, that performs the conversion by performing binary search through all possible quantization levels before converging to the digital output for each conversion.	In Chapter 2
SFDR	Spurious-Free Dynamic Range	It is defined as the ratio between the fundamental tone and the highest spurious tone powers. Detailed information could be found in Subsection 2.5.4.	In Chapter 4, 5
SNDR	Signal-to-Noise-and-Distortion Ratio	It is a quantity that measures the ratio between the power of the signal and the sum of the quantization noise, distortion noise and the additive random noise powers. Detailed information could be found in Subsection 2.5.3.	In Chapter 4, 5
TI ADC	Time-Interleaved Analog to Digital Converter	Sub class of ADCs.	Through out the thesis
THD	Total Harmonic Distortion	In this context it is a measure of non-linear distortion introduced by an ADC. Detailed information could be found in Subsection 2.5.5.	In Chapter 4, 5

Since it was meant to be

1 INTRODUCTION

1.1 Analog-to-digital conversion

Modern-day communication systems process the information, carried by the signals, digitally. This is because of the versatility of digital circuits over their analog counterparts, and some of the examples are:

- Digital circuits are more robust to noise since the effects of electromagnetic interference are minimal.
- Digital signals typically use less bandwidth. The amount of data carried by a digital signal is increased by optimisation algorithms.
- The information processed digitally are more secure since they are encrypted.
- Digital designs are cheaper to implement since they can adapt to different silicon technologies (silicon wafer length).

Although the digital circuits have the above-mentioned advantages, the analog circuits cannot be eliminated, because of the relevance of analog signals in the real world, especially in applications where the signals are processed at higher frequencies. Nevertheless, the input signals have to be converted from analog to digital format (binary representation, i.e. 0's and 1's), before being processed digitally.

The conversion of signals from analog to digital domain is performed by an Analog to Digital Converter (ADC). The processes in this device include sampling and quantizing the input signal, which leads to information loss due to the limited resolution of the converter, thereby making it the bottleneck of any modern-day communication system.

There have been many breakthroughs made in the field of ADCs to increase its performance operating at nominal sampling rates ranging over few hundred Mega samples per second (MSps). But, today's trend is to reduce the analog circuitry, thereby moving the A-D conversion to the front end in the receivers. This increases the performance requirements on an ADC. For example, if an incoming signal has a signal bandwidth B_w of around 1 gigahertz (GHz), then according to Nyquist criterion, it could be reconstructed from its samples without any information loss (in terms of the frequency content), if it is sampled at a frequency greater than twice its bandwidth. This means that the ADC should have a sampling rate of 2 Giga samples per second (GSps) along with a good resolution to preserve the integrity of the incoming signal.

1.2 Objective of the master thesis

The main objective of this master thesis work is to develop a digital post-correction technique for the mitigation of spurious tones, which are mainly caused by the nonlinearities for a Time-Interleaved ADC (TI ADC). We shall be considering the aspect of harmonic suppression by developing a calibration scheme for the low order harmonics, which covers the cases of both even and odd harmonic tones respectively. This method could be extended to any order of harmonics without a loss in generality.

The focus in this work is mainly given to the harmonic suppression, since the TI ADC under consideration has an in chip calibration (different types of calibration techniques shall be explained later in Subsection 2.4.5) implemented by the manufacturer, and this does a good job in the suppression of spurious tones arising from the gain, offset, and skew mismatches present between the individual sub-converters respectively. However, the previously implemented in chip calibration technique cannot suppress the harmonics arising from each individual sub-converter. Therefore, in this work, we shall create an analytical model of TI ADC in frequency domain, that shall establish a framework, which facilitates us to develop a post-correction block, that is capable of suppressing the harmonics (up to any order), which are originating from the individual sub-converters in the TI ADC architecture. This post-correction block shall treat the output sequence of the TI ADC under consideration without the need to know as to which individual sub-converter in the TI ADC architecture has contributed to which part of the output sample. The proposed post-correction block is not limited to TI ADC alone, and is totally valid for other ADC architectures such as sigma-delta ADCs and pipeline ADCs.

Also, we shall develop a four channel TI ADC model in the time domain, to be able to simulate the effects of mismatches. This shall provide a good framework to propose calibration techniques in the future, such that the effects of mismatches can be mitigated even further.

1.3 Tools

In this work, we shall not consider the implementation of the proposed post-correction block, on an ASIC. Therefore, we shall only be using software tools in this work. The tools used in this work are as follows:

- **MATLAB:** For developing all the models, including the proposed post-correction block for the mitigation of harmonics, the TI ADC models in order to simulate the mismatch effects, etc. and to measure the improvements in the TI ADC's performance post calibration.
- **Data capture software:** This is a stand-alone software provided by Texas Instruments to capture the output data from the TI ADC under consideration.

Also, the complete test-bed setup used in this work shall be explained in detail in Subsection 4.2.2.

1.4 Research limitations

In this thesis work, we shall begin at a theoretical level by developing an analytical proof, which provides the basis for the proposed post-correction block. Since we shall be focussing on developing a system level model of the post-correction block, the implementation will not be considered in this work. The proposed solutions will have to be implemented on an FPGA and plugged on a real TI ADC which requires an efficient implementation in order to save area and power consumption along with having high compensation performance. This is really important since having a robust correction technique is impractical if it comes at a computational cost that is not acceptable by the industrial standards. These shall be considered as future work and more information about future work could be found in Chapter 6.

1.5 Outline of the master thesis

In Chapter 2, we present the background theory required for analog to digital conversion. After a brief review of various single die ADC architectures, a new architecture known as the TI ADC shall be studied, since it serves the purpose when it comes to applications where RF sampling is involved (RF receivers). Here, the working principle of the TI ADC shall be discussed, along with its drawbacks. A short literature survey would be done to get a better understanding of the TI ADC model, which facilitates us while modelling its mismatches and non-linearities.

In Chapter 3, we shall present an analytical representation of the total converter's (TI ADC's) output in terms of its sub- converter's output in the frequency domain. This step is crucial while performing the analysis of individual sub- converter's effect on the

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harmonics. Also, we shall concentrate on the analysis of gain, timing and offset mismatches, that is, the way they affect the output of the TI ADC, by studying a time domain model in MATLAB. Also, the frequency calculation of the spurious tones resulting from these mismatches is presented based on the simulations performed on the time domain model. This is a preliminary step, which gives a good understanding of the mismatches before we start to propose any compensation technique in the future. Along with this, we shall model the non-linearity of the device and characterize the dynamic non-linear phase distortion for the first order harmonics, which is a preliminary step while designing the post-correction block for the harmonic suppression.

In Chapter 4, we propose a post-correction technique for the compensation of non-linearities (first order harmonics), that treats the raw data coming from the TI ADC (without the knowledge of the sub-converter it is coming from) and is capable of dynamically suppressing the harmonics.

In Chapter 5, we discuss the results from the previous chapter in order to validate whether the proposed post-correction block is fully functional. We also review the methods and whether the proposed post-correction block is reliable.

Finally, in Chapter 6, conclusions and some guidelines for future work is presented.

2 THEORY

2.1 Introduction

In this chapter, the background theory required for this work shall be presented. At first, the reader shall be introduced to the basic theoretical concepts, pertaining to the analog to digital conversion. Later on, different ADC architectures are studied briefly and conclusions are drawn on how these architectures are not really apt for any modern-day communication system where RF sampling is employed often. Therefore, a more suitable architecture of an ADC known as the TI ADC, which is capable of working at higher frequencies is studied, to explore its possibilities and limitations. Also, the reader shall be introduced to the basic performance parameters, which shall be helpful while presenting the results in Section 4.4.

2.2 Sampling process

There are two types of sampling processes, which could be performed before quantization, namely:

- Oversampling.
- Subsampling.

These sampling processes are explained in detail in Subsections 2.2.1 and 2.2.2, along with their advantages and disadvantages. In general, sampling is a process of reducing a continuous time signal to a discrete time signal

2.2.1 Oversampling

According to the Nyquist-Shannon sampling theorem [1], an incoming signal must be sampled at a rate higher than twice its maximum frequency component for an explicit representation of the signal in the first Nyquist zone which ranges from 0 to $F_{\text{samp}}/2$, where F_{samp} is the sampling frequency. This process is known as oversampling. For simplicity, we could represent $F_{\text{samp}}/2 = F_N$, where F_N is known as the Nyquist frequency.

The advantages of oversampling are that it provides good processing gain, reduction in noise and a great flexibility while performing frequency planning calculations in ADCs. It also has many disadvantages. To name a few, it puts a lot of requirements on the design and the circuitry of an ADC. Therefore, it consumes more power and requires higher data rate for the capture unit which is usually implemented on Field Programmable Gate Array (FPGA). This process is illustrated in Figure 2.2.1, where the frequency of the incoming signal F_i is present in the first Nyquist zone.

2.2.2 Subsampling

If the incoming signal is sampled at a rate, lower than twice its maximum frequency component, then it is known as subsampling. For example, in Figure 2.2.2, it could be seen that the frequency of the input signal is present in the second Nyquist zone which ranges between F_N to F_{samp} . Also, it is clearly evident that $2F_i > F_{\text{samp}}$ where F_i is the frequency of the input signal. This creates an aliased signal at frequency F_a whose frequency could be defined as follows:

$$F_a = F_N - (F_i - F_N) . \quad (2.1)$$

The process of subsampling overcomes all the disadvantages posed by oversampling. Another major advantage is that this performs the job of a mixer (which is used to down convert the incoming signal in the analog domain). This reduces the number of components required in the analog domain and the signal could be directly processed by the data capture unit, which shall usually be operating at a lower frequency comparatively.

Distortion Cancellation in Time-Interleaved ADCs

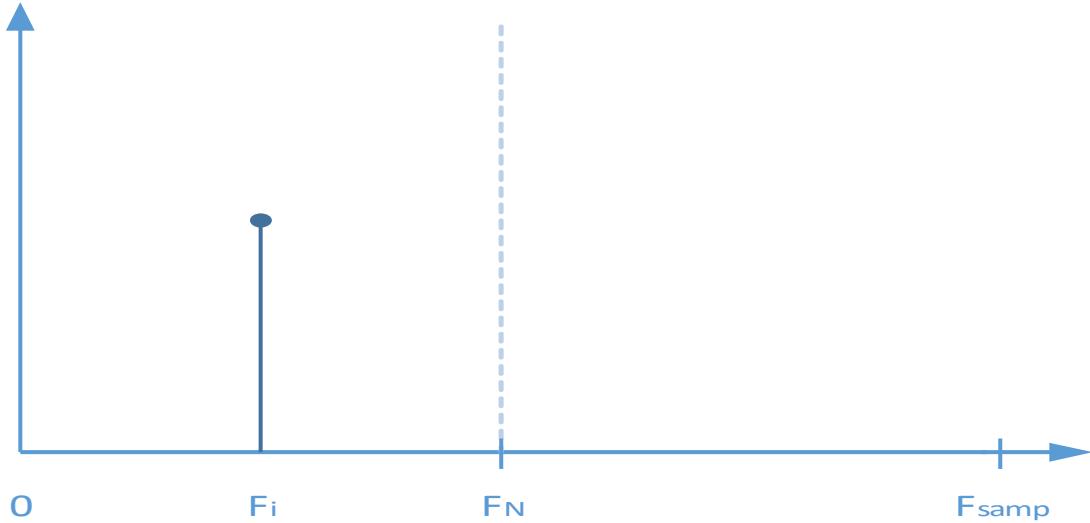


Figure 2.2.1: Oversampling illustration. Here F_i is the frequency of the incoming signal. F_{samp} is the sampling frequency of the ADC. The region from 0 to F_N is termed as the first Nyquist zone.

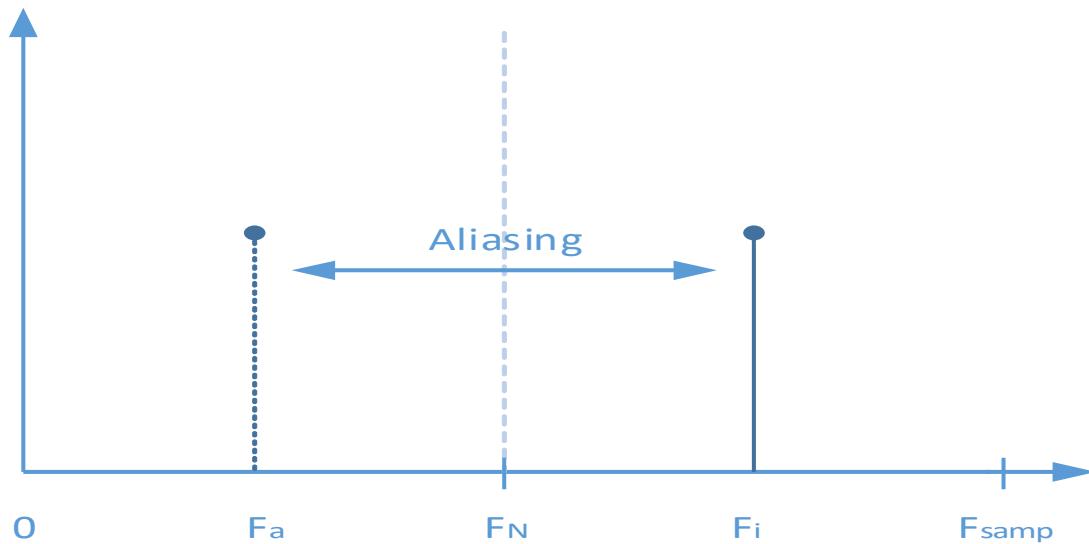


Figure 2.2.2: Subsampling illustration. Here F_i is the frequency of the incoming signal. F_{samp} is the sampling frequency of the ADC. F_a is the aliased signal. The region from F_N to F_{samp} is termed as the second Nyquist zone.

2.3 ADC architectures

Some of the popular analog to digital converter architectures are presented in this section which shall be reviewed briefly, in order to present their uses and limitations.

2.3.1 Flash converters

Flash converters typically consist of a resistance ladder structure along with a comparator at each stage in the ladder structure, which compares the input voltage with the reference voltages. The output from these comparators will be fed into a digital encoder, thereby converting the input voltage into a binary value. Even though this architecture is known to have high sampling rates ranging from few 100 MSps to few GSps, the chip area increases exponentially to the resolution of ADC. It would require 2^B resistors and comparators to convert the analog signal to B bits of binary data. Therefore, the resolution of such architecture is impractical to exceed beyond 7-8 bits [2].

2.3.2 SAR converters

Successive-approximation-register (SAR) ADC works on a similar logic to that of flash ADC, except for the fact that it uses only one comparator. It uses binary search method. First, the incoming signal is sampled and compared to the mid reference voltage and depending upon the result obtained, it performs the comparison again with the lower or upper half of the ladder. This goes on until B possible quantizations before converging to the digital output for each iteration of conversion. Typically they have lower sampling rates ranging from few hundred Kilo samples per second (kSps) to few hundred MSps with an effective resolution of up to ten bits [2]. It is most suited for data acquisition applications.

2.3.3 Pipeline ADCs

Pipeline ADCs typically consists of consecutive stages of a low-resolution ADCs (typically flash ADCs). Considering that a pipeline ADC has S stages, the analog input is sampled and quantized in the first stage. The output of this stage is entered into a DAC (Digital to Analog Converter) whose output is subtracted from the input signal and the resultant signal is amplified and then passed on to the next stage. This goes on until S stages. The quantized bits from each stage make up the digital output. The Pipeline ADC has medium latency due to increased number stages to obtain the final output. Typically, these are well suited for telecommunications since they have good sampling rates ranging from few tens of MSps to few hundred MSps with a good resolution [2].

2.3.4 Sigma-Delta converters

A Sigma-Delta ADC consists of a sigma-delta modulator. Here the analog input signal is sampled multiple times (also known as oversampling) and its value is compared to its previous sampling instant's value. This process produces series of binary data that somewhat represents the derivative of the input signal. By passing this through a digital integrator, the digital code is obtained. They typically have a very good resolution of up to 20 bits but at lower sampling rates [2]. It is most suited for bio-medical applications.

2.3.5 Remarks

We briefly discussed as to why various popular ADC architectures are not suitable for the current industrial standards when it comes to applications, which requires RF sampling. Therefore, in the upcoming section, a new architecture is studied which allows RF sampling without a drastic loss in the resolution of Analog to digital conversion.

2.4 Time-Interleaved ADC

After a brief review of various re-known architectures of ADC, the readers shall be introduced to the concept of Time-Interleaved ADC, its working and its limitations with respect to the mismatches between the individual sub-converters in the TI ADC.

2.4.1 Introduction

In modern-day communication systems, there is always a need to perform the A-D conversion at a higher sampling rate along with a good resolution to preserve the integrity of the incoming signal. But, in Section 2.3, it was seen that several popular ADC architectures either achieved higher sampling rates, but compromised on the resolution of conversion and vice versa. Therefore, to achieve a good resolution of A-D conversion at a higher sampling rates a new architecture was proposed in 1980 [3], known as the Time-Interleaved ADC (TI ADC).

2.4.2 Time-Interleaved ADC principle

A TI ADC consists of several individual ADCs (sub-convertisers) of similar architecture, working in parallel in order to increase the sampling rate. A typical TI ADC is shown in Figure 2.4.1.

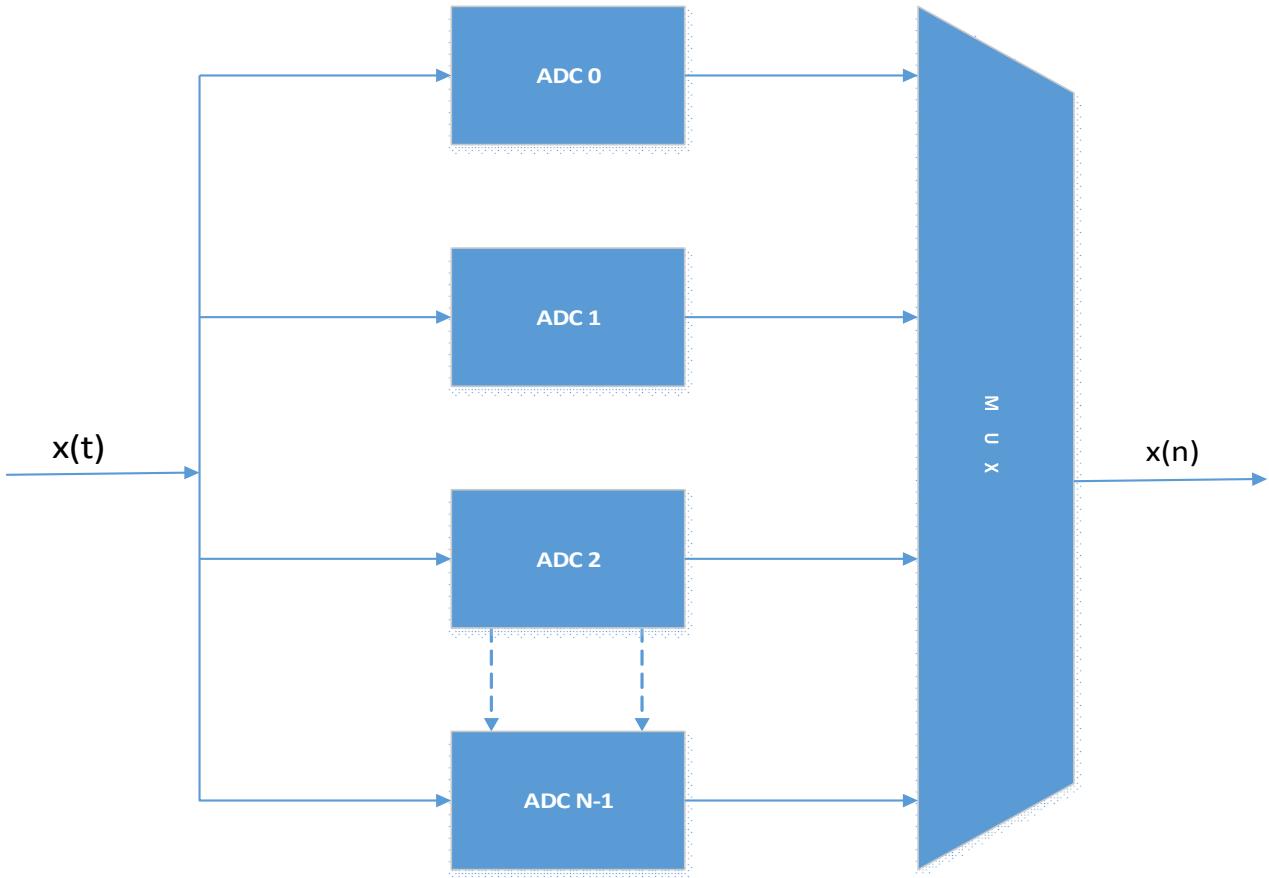


Figure 2.4.1: Time-Interleaved ADC (TI ADC) working principle. Here ADC 0 to ADC N-1 are the individual sub-convertisers.

In Figure 2.4.1, it is seen that the Time-Interleaved ADC consists of N individual sub-convertisers which sample the input signal $x(t)$ in a sequential loop. So, for instance, if T_s is the sampling period of all the N individual sub-convertisers, then the sampling period of the TI ADC is given by T_s/N . Similarly, if F_s is the sampling frequency of all the N individual sub-convertisers, then the sampling rate of the TI ADC is given by NF_s . This architecture enables us to achieve higher sampling rates, which is not possible by a single converter core. Also, it is theoretically possible to achieve arbitrary sampling frequency by interleaving as many cores.

2.4.3 TI ADC mismatches

Although the TI ADC has many advantages, it suffers from the setbacks caused by the mismatches between the individual sub-converters in the Time-Interleaved architecture [4]. In reality, due to the fabrication process, the sub-converters have slightly different characteristics, which results in the mismatches. These mismatches could be classified as follows:

- **Offset mismatch** - the sub-converters in the TI ADC have different offset values, which should ideally be zero.
- **Gain mismatch** - the sub-converters in the TI ADC have different gain values which should ideally be one.
- **Timing skew mismatch** - the sub-converters in the TI ADC sample the incoming signal with a small error at the sampling instant.
- **Non-linear mismatches** - the sub-converters in the TI ADC have different non-linear quantization transfer functions.

These differences affect the output of the total converter (TI ADC) by introducing mismatch aliasing noise and spurious tones, along with harmonics which reduce the performance of the TI ADC.

2.4.4 Literature survey

The mismatch analysis was previously shown in [5], where the authors consider only offset and gain mismatches and they show the effects on the SNDR of the ADC using probability distribution of gain and offsets.

In [6] and [7], the author presents the frequency effects of non-uniform sampling for a sine input signal. In [8], the author presents on how non-uniform sampling affects the reconstruction of the signal while using DAC.

The non-linearity mismatch was first dealt in [9]. Here, the author demonstrates that the Integral Non-linearity (INL) and the Differential Non-linearity (DNL) of the TI ADC are smaller than that of its individual sub-converters' INL and DNL. In [10], the author demonstrates the effects of non-linearity mismatch using the experimental results.

The major development in TI ADC modelling occurs with the use of Hybrid-Filter-Banks (HFB) as a framework. In [11], [12], and [13] the author uses the HFB framework to derive the output frequency spectrum of the TI ADC in the presence of gain, offset, and skew mismatches, for a sinusoidal input signal.

In [14], the author extends the model to Non-Linear HFB, in order to deal with the non-linearity mismatches.

2.4.5 Calibration techniques

To overcome the effects caused by the mismatches in the TI ADC, there has to be a calibration technique implemented, which rectifies the errors. There are different types of calibration techniques depending on the way they are implemented, namely:

- **In-Chip calibration** - In-Chip calibration is a method which includes internal hardware changes or some kind of tuning to be performed internally at each sub-converter level and usually considering the first sub-converter as a reference. This is implemented through an in-chip background calibration.
- **Off-Chip calibration** - With the advancement in the digital circuits as mentioned previously in Section 1.1, the main idea is to find a way to rectify the ADC output without modifying the internal circuitry or perform a calibration phase. Off-Chip calibration is implemented usually on a DSP outside the ADC during the normal operation, and the calibration is performed without the knowledge of the input signal. This is an effective way of implementation, since it is cheaper and could be implemented on any type of ADCs.

In this work, it is intended that we propose an off-chip calibration technique, to compensate for the effects of harmonics. Although depending on the hardware requirements, post-implementation phase, it shall be decided whether it could be implemented in chip or off chip.

2.5 ADC performance measurements

This section is intended for the reader to get familiarized with the figure of merits (FOM) used to measure the performance of the TI ADC under consideration.

2.5.1 ADC signal model

The discrete output signal of an ADC $z(n)$ could be defined as follows:

$$z(n) = x(n) + er_q(n) + er_d(n) + er_a(n), \quad (2.2)$$

where $x(n)$ represents the sampled input signal, $er_q(n)$ represents the quantization noise which occurs due to the uncertainty arising in the quantization process, $er_d(n)$ represents the distortion noise which is usually generated by the non-linearities and in the case of TI ADCs, the mismatches between the individual converters also contributes to the distortion noise, $er_a(n)$ represents an additive random noise, which

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comprises of thermal noise (generated in all internal analog components in an ADC) and sampling jitter (generated when a non-ideal clock is driving a non-ideal ADC).

The average power of the signal part could be expressed as follows:

$$\overline{P_x} = \frac{1}{N} \sum_{n=0}^{N-1} x^2(n), \quad (2.3)$$

where N corresponds to the number of samples considered.

Similarly, we could define the quantization noise power denoted as $\overline{P_q}$, the distortion noise power denoted as $\overline{P_d}$ and the additive random noise power denoted as $\overline{P_a}$.

The quantization noise is generally modelled as an uncorrelated zero mean uniform random process, which implies that the quantization noise is uniformly distributed in the interval as defined below:

$$\overline{P_d} \in \left[-\frac{\Delta q}{2}, \frac{\Delta q}{2} \right]. \quad (2.4)$$

Δq is defined as the minimum discrete step size in the ADC (value of one LSB), which is defined as follows:

$$\Delta q = \frac{V_{pp}}{2^B}, \quad (2.5)$$

where V_{pp} is the full-scale range (FSR) of the ADC, given in volts, and B corresponds to the number of quantization bits. It is illustrated in Figure 2.5.1.

The probability density function of $er_q(n)$, could be expressed as follows:

$$P_q(x) = \frac{1}{\Delta q}, \quad (2.6)$$

$$P_q(x) = \frac{2^B}{V_{pp}}, \quad (2.7)$$

where x could vary from -2^{-B} to 2^{-B} .

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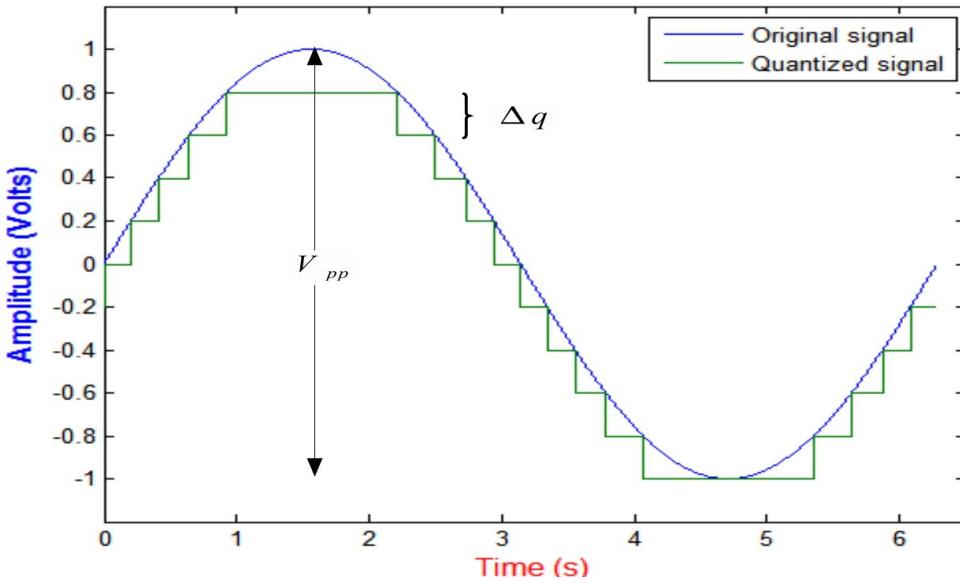


Figure 2.5.1: A quantized sinusoidal wave along with its analog representation. V_{pp} is the full-scale range and Δq (delta q) is the minimum quantization step.

Also, the average power of a random process corresponds to its variance. Therefore, the quantization noise power is given by:

$$\overline{P}_q = \int_{-\frac{\Delta q}{2}}^{\frac{\Delta q}{2}} x^2 P_q(x) dx , \quad (2.8)$$

$$\overline{P}_q = \frac{1}{\Delta q} \int_{-\frac{\Delta q}{2}}^{\frac{\Delta q}{2}} x^2 dx , \quad (2.9)$$

$$\overline{P}_q = \frac{2^B}{V_{pp}} \left[\frac{x^3}{3} \right]_{-\frac{\Delta q}{2}}^{\frac{\Delta q}{2}} , \quad (2.10)$$

$$\overline{P}_q = \frac{(\Delta q)^2}{12} , \quad (2.11)$$

$$\overline{P}_q = \frac{(V_{pp})^2 2^{-2B}}{12} , \quad (2.12)$$

where V_{pp} is the full-scale range (peak to peak voltage) and B corresponds to the number of quantization bits.

2.5.2 Signal-to-Quantization-Noise Ratio (SNQR)

As the name suggests, SNQR is a measure of the power ratio between the signal and the quantization noise. It is defined as follows:

$$SNQR = 10\log \frac{\overline{P_x}}{\overline{P_q}} . \quad (2.13)$$

Considering the case, where the input signal is a full-scale sinusoidal wave, the signal power $\overline{P_x}$ of $x(n)$ is equal to $\frac{V_{pp}^2}{8}$ and the above equation could be re-written as follows:

$$SNQR = 10\log \frac{12}{2^{-2B}8} , \quad (2.14)$$

$$SNQR = 10\log(1.5) + 20\log(2)B , \quad (2.15)$$

$$SNQR \approx 6.02B + 1.76 . \quad (2.16)$$

In (2.16), B stands for the number of quantization bits. Also, SNQR is expressed in dB.

2.5.3 Signal-to-Noise Ratio (SNR)

The Signal-to-Noise ratio (also expressed in dB) is a quantity, that measures the ratio between the power of the signal and the noise power. Therefore, it could be defined as follows:

$$SNDR = 10\log \frac{\overline{P_x}}{\overline{P_q} + \overline{P_d} + \overline{P_a}} , \quad (2.17)$$

where $\overline{P_q}$ is the quantization noise power, $\overline{P_d}$ is the distortion noise power, and $\overline{P_a}$ is the additive random noise power.

2.5.4 Spurious-Free Dynamic Range (SFDR)

For a sinusoidal input signal, the SFDR (expressed in dB) is given by the ratio between the fundamental tone and the highest spurious tone power. Therefore, it could be expressed as follows:

$$SFDR = 10 \log \frac{\overline{P}_x}{\max(\overline{P}_q, \overline{P}_d, \overline{P}_a)} . \quad (2.18)$$

It could be easily measured by calculating the DFT of the ADC output. This is illustrated in Figure 2.5.2.

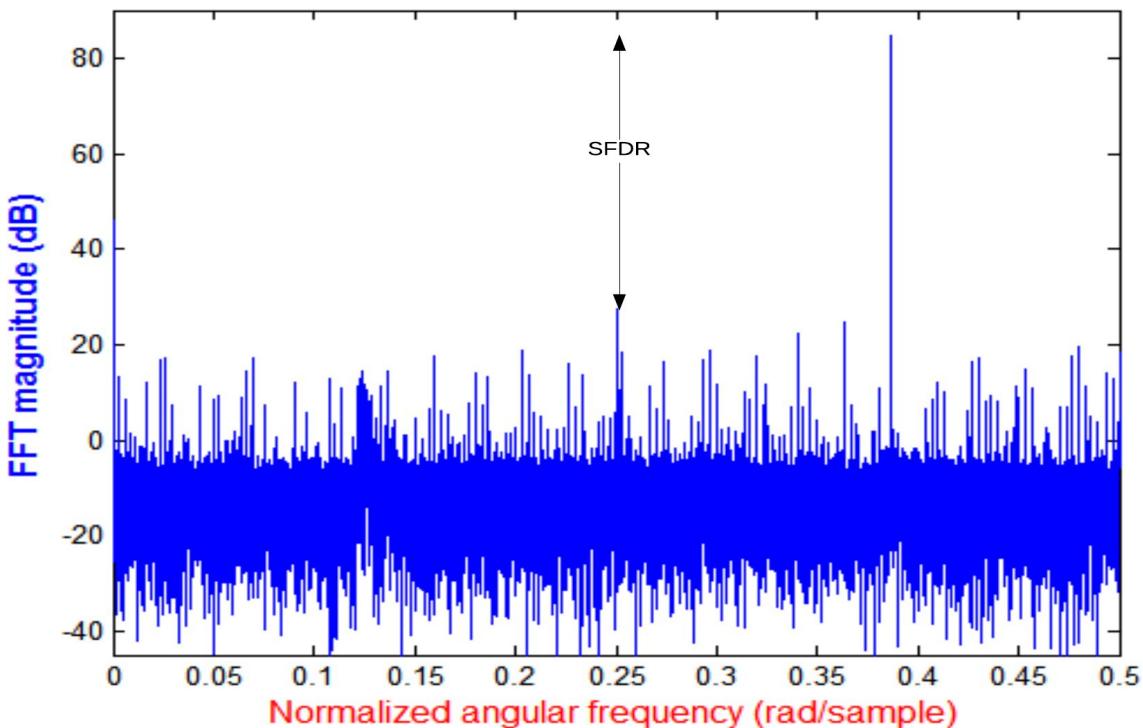


Figure 2.5.2: Illustration of SFDR measurement for a typical sinusoidal input, where SFDR could be measured by calculating the magnitude difference (in dB) between the fundamental frequency component and the highest spurious tone's frequency component.

2.5.5 Total Harmonic Distortion (THD)

The THD is a measure of the non-linear distortion introduced by the ADC under consideration. It is expressed as follows:

$$THD = \frac{\sum_{k=2}^N P_k}{P_1}. \quad (2.19)$$

Therefore, the THD corresponds to the ratio of the sum of the dominant harmonic powers P_k to the fundamental tone power P_1 .

2.6 Conclusions

In this chapter, various re-known architectures of ADC were reviewed briefly. A new architecture known as the Time-Interleaved ADC was introduced to the readers, which is suitable for the applications involving RF sampling. Along with this, the limitations of the TI ADC were discussed, and a brief literature survey was performed in order to understand different types of calibration performed, in order to overcome the limitations caused by mismatches in the TI ADC. Furthermore, the theoretical concepts such as the signal model of a typical ADC output is presented for the reader to understand about the ADC concepts. Based on this signal model several figure of merits were defined which shall be helpful in determining the performance parameters of the TI ADC. In the upcoming chapter, different models of the TI ADC (time domain and frequency domain model) shall be studied before proposing the calibration method to correct the effects of non-linearities from the output of the TI ADC under consideration.

3 MODELLING

3.1 Introduction

In the previous chapter, we have discussed the principle of the TI ADC, where several individual sub-converter's output are multiplexed in parallel to achieve an output sequence at a higher sampling rate. Although, each sub-converter has imperfections due to the fabrication process, and this changes its behaviour from the other sub-converters in the array. This affects the transfer function of each sub-converter converter, causing them to be different from each other, thereby, introducing the spurious tones in the output frequency spectrum of the TI ADC. A representation of transfer functions of these mismatches is presented in Figure 3.1.1. They would be studied in detail in Section 3.3.

In this chapter, we study the frequency model of the TI ADC, where we present an analytical proof which shows that the TI ADC's output could be constructed by its sub-converters' output in the frequency domain, just by adding their Discrete Fourier Transforms(DFT).

Along with the above-mentioned frequency model, we study the mismatches in the sub-converters and its effects on the output of the TI ADC. This is modelled in the time domain in MATLAB for a complete understanding.

Distortion Cancellation in Time-Interleaved ADCs

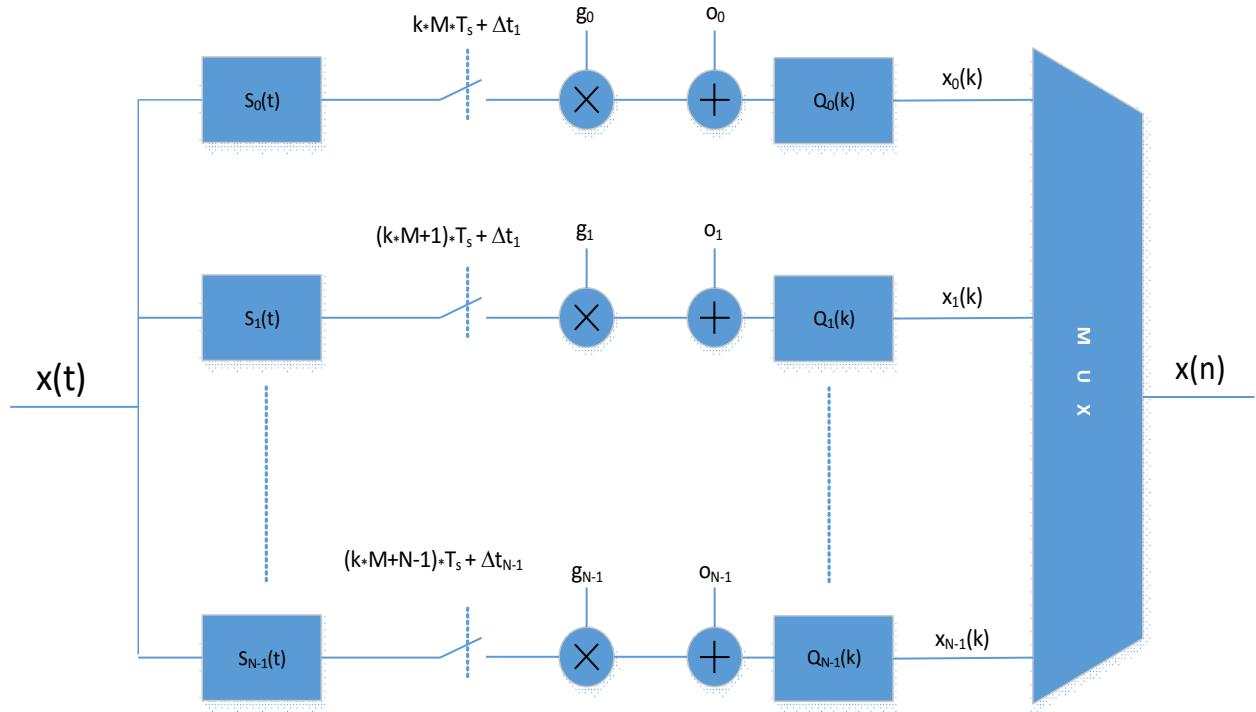


Figure 3.1.1: Elaborated model of TI ADC.

3.2 TI ADC frequency model

An accurate model of the TI ADC in terms of its sub-converters is illustrated in this section, which provides a good framework for analysis of the TI ADC's output in terms of its individual sub-converters' output in the frequency domain.

Here, a TI ADC consisting of four sub-converters working in parallel is considered.

Let us start with the definition of discrete Fourier transform [1] denoted as $X(k)$, for a continuous time domain signal $x(n)$, and is given by:

$$X(k) = \sum_{n=0}^{M-1} x(n) e^{\frac{-j2\pi kn}{M}}, \quad (3.1)$$

where M is the number of samples of the time domain signal, and k varies from 0 to $M-1$.

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Let $x(n)$ be the output code of the time-Interleaved ADC containing M samples. Its DFT $X(k)$ could be obtained from (3.1).

The output of each individual sub-converter in the TI ADC architecture contributes to every fourth sample in the total converter's output. Therefore, the output of each sub-converter could be defined as follows:

$$\text{Sub-converter 1} = x_0(q) = x(4l), \quad (3.2)$$

$$\text{Sub-converter 2} = x_1(q) = x(4l+1), \quad (3.3)$$

$$\text{Sub-converter 3} = x_2(q) = x(4l+2), \quad (3.4)$$

$$\text{Sub-converter 4} = x_3(q) = x(4l+3), \quad (3.5)$$

$$\text{where } l = \frac{n}{4}.$$

To express the total converter's output in terms of the discrete Fourier transform (DFT) of individual sub-converter's output, the limits of the DFTs corresponding to the individual sub-converters should be redefined as follows:

$$n \text{ varies from 0 to } M-1, \quad l \& q \text{ vary from 0 to } \frac{M}{4}-1.$$

Therefore, using (3.2), (3.3), (3.4), and (3.5), the DFT of the TI ADC's output could be expressed in terms of the DFTs of the sub-converters' output as follows:

$$X(k) = \left\{ \sum_{l=0}^{\frac{M}{4}-1} x(4l)e^{-j2\pi k(4l)} + \sum_{l=0}^{\frac{M}{4}-1} x(4l+1)e^{-j2\pi k(4l+1)} + \sum_{l=0}^{\frac{M}{4}-1} x(4l+2)e^{-j2\pi k(4l+2)} \right. \\ \left. + \sum_{l=0}^{\frac{M}{4}-1} x(4l+3)e^{-j2\pi k(4l+3)} \right\}, \quad (3.6)$$

where $X(k)$ represents the DFT of the TI ADC's output.

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Re arranging (3.6) in the exponential part, it could be written as follows:

$$X(k) = \left\{ \sum_{q=0}^{\frac{M}{4}-1} x_0(q) e^{-j2\Pi k \frac{(q)}{\frac{M}{4}}} + \sum_{q=0}^{\frac{M}{4}-1} x_1(q) e^{-j2\Pi k \frac{(q+\frac{1}{4})}{\frac{M}{4}}} + \sum_{q=0}^{\frac{M}{4}-1} x_2(q) e^{-j2\Pi k \frac{(q+\frac{1}{2})}{\frac{M}{4}}} \right. \\ \left. + \sum_{q=0}^{\frac{M}{4}-1} x_3(q) e^{-j2\Pi k \frac{(q+\frac{3}{4})}{\frac{M}{4}}} \right\}. \quad (3.7)$$

For simplicity, we choose to represent $\frac{M}{4} = p$.

Therefore, after variable change, (3.7) could be re-written as follows:

$$X(k) = \left\{ \sum_{q=0}^{p-1} x_0(q) e^{-j2\Pi k \frac{(q)}{p}} + \sum_{q=0}^{p-1} x_1(q) e^{-j2\Pi k \frac{(q)}{p}} e^{-j2\Pi k \frac{(\frac{1}{4})}{p}} \right. \\ \left. + \sum_{q=0}^{p-1} x_2(q) e^{-j2\Pi k \frac{(q)}{p}} e^{-j2\Pi k \frac{(\frac{1}{2})}{p}} \right. \\ \left. + \sum_{q=0}^{p-1} x_3(q) e^{-j2\Pi k \frac{(q)}{p}} e^{-j2\Pi k \frac{(\frac{3}{4})}{p}} \right\}, \quad (3.8)$$

$$X(k) = X_0(k) + X_1(k) e^{-j2\Pi k \frac{(\frac{1}{4})}{M}} + X_2(k) e^{-j2\Pi k \frac{(\frac{1}{2})}{M}} + X_3(k) e^{-j2\Pi k \frac{(\frac{3}{4})}{M}}, \quad (3.9)$$

where k varies from 0 to $M-1$.

In Figure 3.2.1, the spectrum of individual sub-converters is shown. By adding the DFTs of the individual sub-converters' output according to (3.9), we obtain the combined output which is the same as that of the TI ADC's output. Also, one could clearly observe from Figure 3.2.2 that, there is no difference between the combined spectrum of the four sub-converters (which is obtained by adding the sub-converters' output), and the original spectrum of the whole converter. Hence, the non-linearities (which shall be explained in detail in Section 3.4) in the form of harmonics present in the total TI ADC output spectrum, originates from the individual sub-converters and are in fact an average of the all the sub-converters' non-linearities. Therefore, this information will be used to develop a post-correction methodology that will calibrate the whole TI ADC's output to mitigate the effects of harmonics.

Distortion Cancellation in Time-Interleaved ADCs

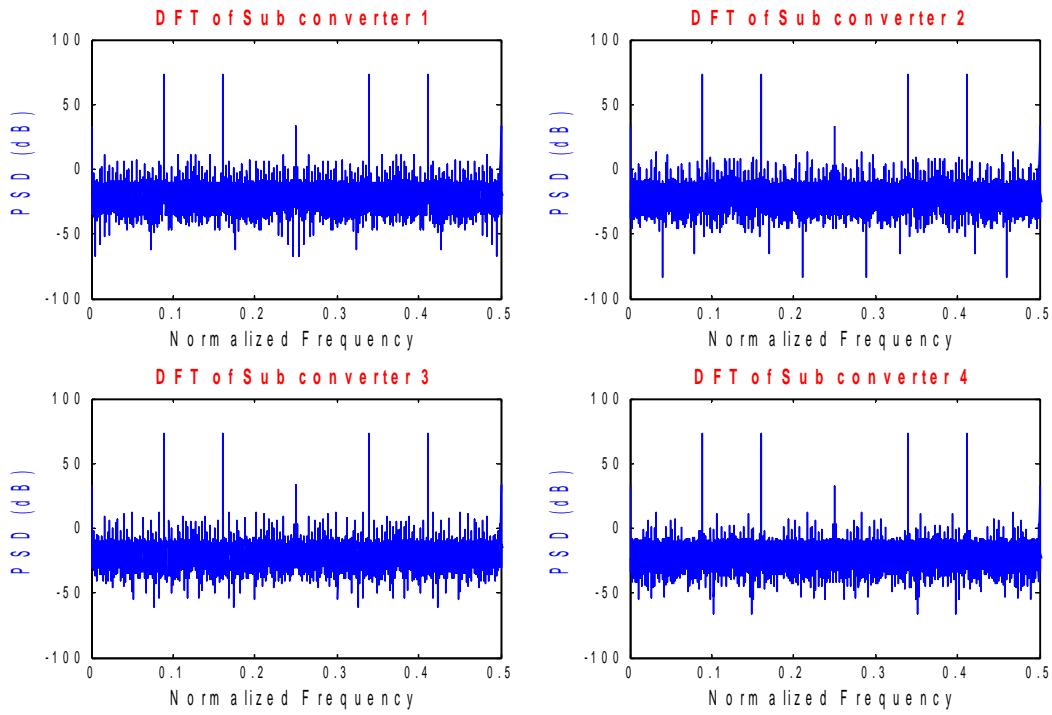


Figure 3.2.1: Spectrum of individual sub-converters obtained by segregating every fourth sample of the TI ADC's output and performing DFT.

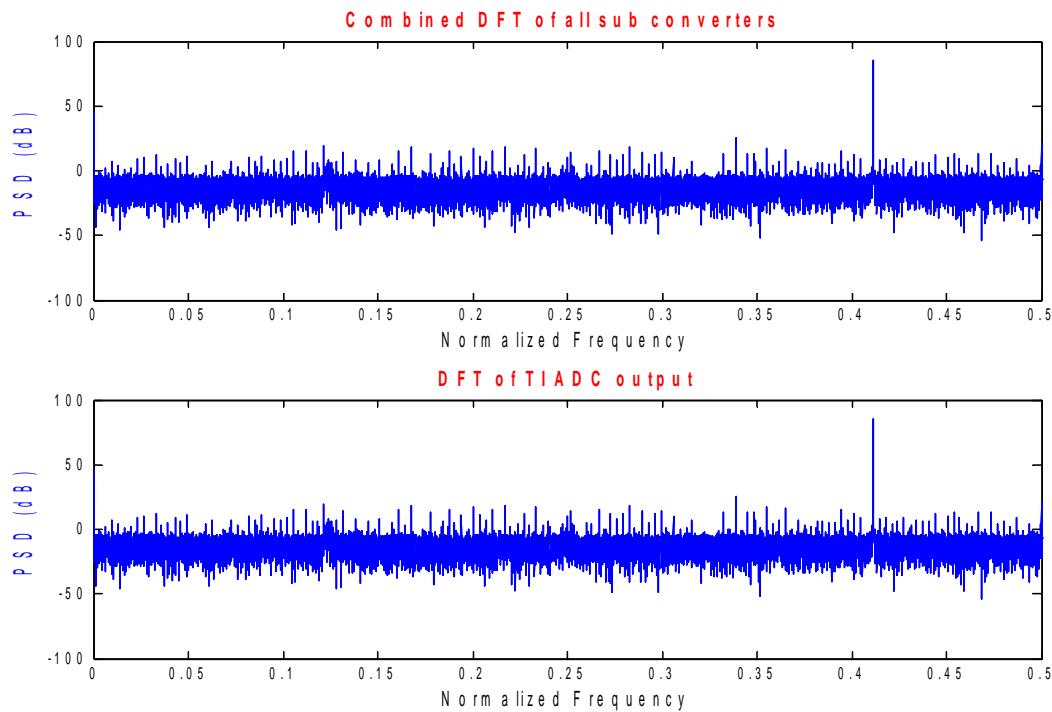


Figure 3.2.2: Comparison of the combined DFT and the original DFT of the TI ADC output.

3.3 TI ADC mismatches

The different mismatches present among each sub-converter in the TI ADC architecture like gain, offset and phase mismatches, and also its impact on the TI ADC's output shall be studied in detail in this section.

3.3.1 Modelling of mismatches

A four channel interleaving process is created in this section[15],[16],[17]. An input signal $x(t)$ consisting of two sinusoidal signals having an amplitude A_1 and A_2 , and frequency f_1 and f_2 , respectively is considered, and is as shown below:

$$x(t) = A_1 \sin(2\pi f_1 t) + A_2 \sin(2\pi f_2 t). \quad (3.10)$$

This signal is branched into four paths, namely $x_0(t)$, $x_1(t)$, $x_2(t)$ and $x_3(t)$. Also, $x_0(t)$ is taken as a reference. In $x_1(t)$, $x_2(t)$ and $x_3(t)$, gain, offset, and timing errors are introduced.

The expressions for the same is given below:

$$x_0(kT_s) = A_1 \sin(2\pi f_1 k T_s) + A_2 \sin(2\pi f_2 k T_s), \quad (3.11)$$

$$x_1(kT_s) = (1 \pm \alpha_1) [(A_1 \sin(2\pi f_1 k (T_s \pm \Delta t_1))) + (A_2 \sin(2\pi f_2 k (T_s \pm \Delta t_1)))] + o_1, \quad (3.12)$$

$$x_2(kT_s) = (1 \pm \alpha_2) [(A_1 \sin(2\pi f_1 k (T_s \pm \Delta t_2))) + (A_2 \sin(2\pi f_2 k (T_s \pm \Delta t_2)))] + o_2, \quad (3.13)$$

$$x_3(kT_s) = (1 \pm \alpha_3) [(A_1 \sin(2\pi f_1 k (T_s \pm \Delta t_3))) + (A_2 \sin(2\pi f_2 k (T_s \pm \Delta t_3)))] + o_3, \quad (3.14)$$

where T_s is the sampling period of each sub-converter.

In the equations (3.12), (3.13), and (3.14) the terms α_1 , α_2 and α_3 are the gain mismatches present in the last three branches of the sub-converters, respectively. Also, Δt_1 , Δt_2 , and Δt_3 corresponds to the skewing errors respectively. And o_1 , o_2 and o_3 are the offset mismatches, respectively.

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These four signals are then multiplexed to form an up-sampled version of the output, whose new sampling period is given by:

$$T_{\text{samp}} = \frac{T_s}{4}. \quad (3.15)$$

Therefore, the new sampling rate is given by

$$F_{\text{samp}} = \frac{1}{T_{\text{samp}}}, \quad (3.16)$$

$$F_{\text{samp}} = \frac{4}{T_s}, \quad (3.17)$$

$$F_{\text{samp}} = 4F_s, \quad (3.18)$$

where F_{samp} is the new sampling frequency after multiplexing, and F_s is the sampling frequency of each sub-converter core.

The multiplexed or interleaved output could be written as follows:

$$x_{\text{mux}}(k T_{\text{samp}}) = \begin{cases} x_0\left(\frac{hT_s}{4}\right) & h=0,4,\dots,(4k) \\ x_1\left(\frac{hT_s}{4}\right) & h=1,5,\dots,(4k+1) \\ x_2\left(\frac{hT_s}{4}\right) & h=2,6,\dots,(4k+2) \\ x_3\left(\frac{hT_s}{4}\right) & h=3,7,\dots,(4k+3) \end{cases}. \quad (3.19)$$

The process of interleaving the sub-converters as shown in (3.19) was modelled in time domain using MATLAB. In the upcoming section two tone tests were simulated using this model.

3.3.2 Mismatch model simulation

Two-tone simulations were performed for the mismatch model developed in Subsection 3.3.1, for both oversampling and subsampling cases. The amplitude of the two sinusoidal input tones are denoted by A_1 and A_2 , whose values are set to one. The gain and skew errors are set to 0.05% along with an offset error of 0.1 LSB (Least Significant Bit). All the frequency values are normalized with respect to its sampling frequency F_{samp} and are measured in *radians per sample*.

The normalized values could be obtained by the following relation:

$$F_{\text{norm}} = 2\pi \frac{F_i}{F_{\text{samp}}}, \quad (3.20)$$

where F_i is the input frequency, and F_{samp} is the sampling frequency.

Depending on the location of the input tones, the model is evaluated for the following two cases:

1. Two-tone input in the first Nyquist zone:

Two sinusoidal tones at frequencies $f_1=0.105\pi$ and $f_2=0.11\pi$, present in the first Nyquist zone (i.e. the input frequencies are less than $0.5F_{\text{samp}}$) are used as input. This creates six spurs at 0.13π , 0.14π , 0.35π , 0.36π , 0.38π , 0.39π which are caused by the gain and skew mismatches. Along with these, there are spurs at DC, 0.25π and 0.5π which are caused by the offset mismatches.

2. Two-tone input in the second Nyquist zone:

Two sinusoidal tones at frequencies $f_1=0.62\pi$ and $f_2=0.65\pi$, present in the second Nyquist zone (i.e. the input frequencies are greater than $0.5F_{\text{samp}}$) are used as input. These are aliased back to the first Nyquist Zone at $f_1=0.35\pi$ and $f_2=0.38\pi$. Also, the spurs are located at 0.10π , 0.11π , 0.13π , 0.15π , 0.36π , 0.40π which are caused by the gain and skew mismatches. Along with these, there are spurs at DC, 0.25π and 0.5π which are caused by the offset mismatches.

Illustration of the first case where the two tone input is present in the first Nyquist zone is shown in Figure 3.3.1 and the second case where the two tone input is present in the second Nyquist zone is shown in Figure 3.3.2.

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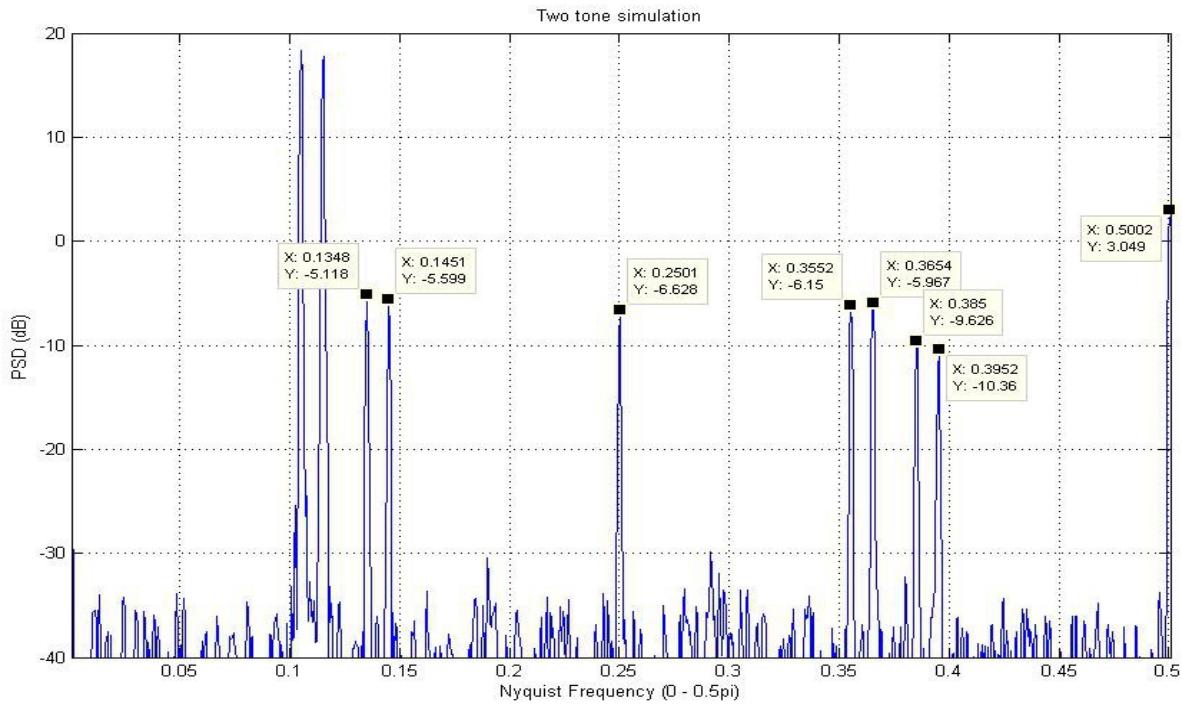


Figure 3.3.1: Four channel interleaving case, when the frequencies of two-tone input signals f_1 and f_2 are present in the first Nyquist Zone.

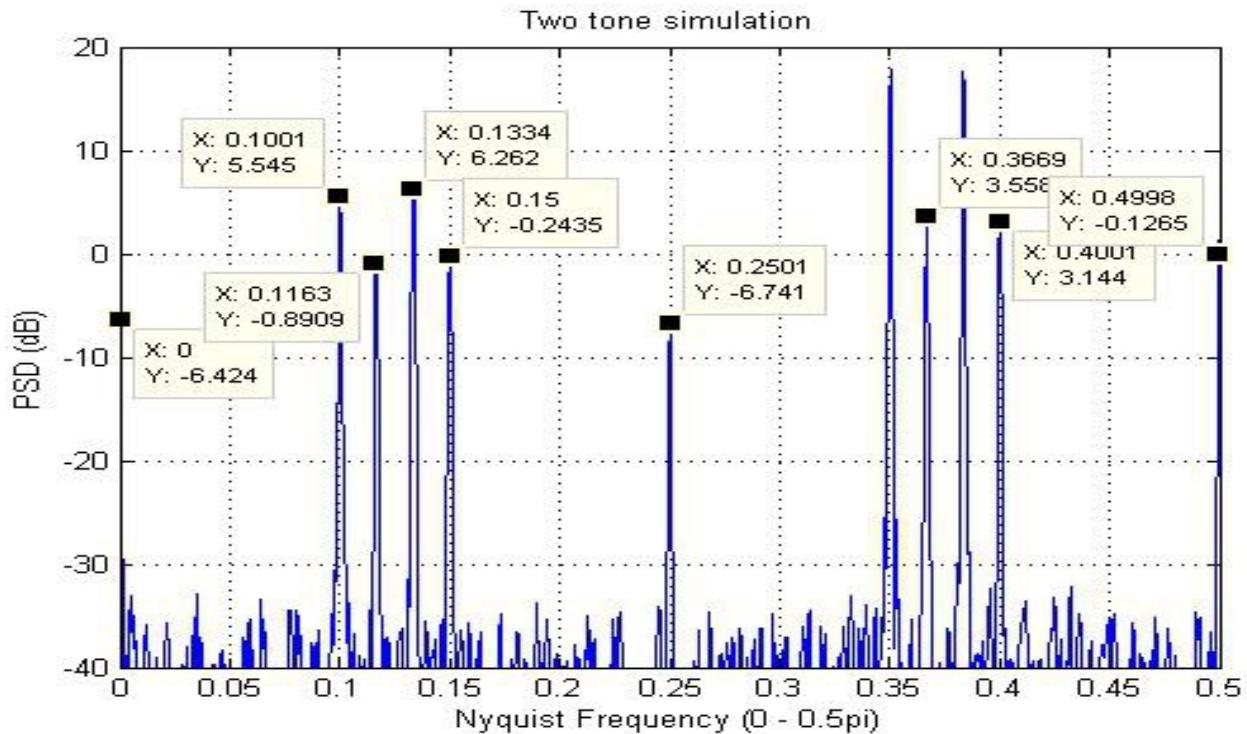


Figure 3.3.2: Four channel interleaving case, when the frequencies of two-tone input signals f_1 and f_2 are present in the second Nyquist Zone.

3.3.3 Mismatches frequency calculation

After the two-tone simulation of the time domain model of the TI ADC, we deal with the frequency calculation of the spurious tones caused by mismatches present in the TI ADC [17].

Here, a TI ADC which consists of N sub-converter cores is considered. The sampling frequency of the TI ADC and its sub-converters are F_{samp} and F_s respectively. Let $x(t)$ be the input signal whose frequency is F_i , which lies in the Nyquist zone n .

The Nyquist zone could be calculated by the following relation:

$$n = \left\lceil 2 \left(\frac{F_i}{F_{\text{samp}}} \right) \right\rceil . \quad (3.21)$$

The frequencies at which the spurious tones resulting from gain and skew mismatches F_{gs} , could be calculated from the equations as shown below:

$$F_{gs} = \sum_{j=1}^{n-1} |\Delta F_j| , \quad (3.22)$$

$$\text{where } \Delta F_j = \begin{cases} \frac{j}{N}(F_{\text{samp}}) - F_i & j > \frac{2}{N} \left(\frac{2F_i}{F_{\text{samp}}} + 1 \right) \\ \left(1 - \frac{j}{N} \right)(F_{\text{samp}}) - F_i & j < \frac{2}{N} \left(\frac{2F_i}{F_{\text{samp}}} + 1 \right) \end{cases} . \quad (3.23)$$

Similarly, along with the DC offset, the frequencies of spurious tones caused by the offset mismatch F_{of} , could be calculated as follows:

$$F_{of} = \sum_{j=1}^{N-1} \left| \left(\frac{j}{N} \right) F_{\text{samp}} \right| , \quad (3.24)$$

where N is the number of sub-converters.

3.4 Non-linearities

The mismatches of the individual sub-converter cores were modelled in the time domain in the previous section and the resulting spurious tones created in the process were studied. In this section, we shall consider the effects of non-linearities on the output of the TI ADC.

3.4.1 Introduction

The output of the TI ADC for a sinusoidal input signal is shown in Figure 3.2.2. It is clearly evident that the TI ADC under consideration contains a lot of repetitive tones which could be termed as harmonics, in the frequency spectrum. This motivated us to characterize the harmonics by studying a non-linearity model.

3.4.2 Modelling

The basic and simple form of modelling a non-linear system is by defining a memoryless power series [18], which is based on normal polynomials, and it could be defined as shown below:

$$Y = \sum_{j=0}^L A_j x^j. \quad (3.25)$$

In (3.25), substituting for $x = \cos(2\pi ft + \Phi_o)$, we get

$$Y = \sum_{j=0}^L A_j (\cos(2\pi ft + \Phi_o))^j. \quad (3.26)$$

Also, (3.26) could be re written as follows:

$$Y = [(A_0) + (A_1(\cos^1(2\pi ft + \Phi_o))) + \dots + (A_L(\cos^L(2\pi ft + \Phi_o)))] , \quad (3.27)$$

where A_0 is DC offset, f is the frequency of the fundamental tone (input frequency), and Φ_o is the phase offset of the fundamental tone.

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In (3.27), for an input sine wave of frequency f , harmonics up to the order of L is considered. In the current calculation, we ignore all the DC offsets and limit the characterization to the second and the third harmonic (first order harmonics) for simplicity. But, the higher order harmonic tones also follows the same concept.

Therefore, (3.27) could be re-written as follows:

$$Y = [(A_1(\cos^1(2\pi ft + \Phi_o)))+(A_2(\cos^2(2\pi ft + \Phi_o)))+(A_3(\cos^3(2\pi ft + \Phi_o)))] . \quad (3.28)$$

Representing the fundamental tone as $\cos(\Theta)$, where $\Theta = 2\pi ft + \Phi_0$, then according to trigonometric identities, we can represent the second harmonic as $\cos(2\Theta)$ which could be defined as follows:

$$\cos(2\Theta) = 2\cos^2(\Theta) - 1 , \quad (3.29)$$

$$\cos^2(\Theta) = \frac{\cos(2\Theta) + 1}{2} , \quad (3.30)$$

$$\cos^2(\Theta) \approx \frac{\cos(2\Theta)}{2} . \quad (3.31)$$

Similarly, we can define the third harmonic as $\cos(3\Theta)$ which is given by:

$$\cos(3\Theta) = 4\cos^3(\Theta) - 3\cos(\Theta) , \quad (3.32)$$

$$\cos^3(\Theta) = \frac{\cos(3\Theta) + 3\cos(\Theta)}{4} . \quad (3.33)$$

Substituting (3.33) and (3.32) in (3.28) we get,

$$Y \approx \left[(A'_1(\cos(2\pi ft + \Phi_o)) + (\frac{1}{2} A_2(\cos(2\pi ft(2) + 2\Phi_o))) + (\frac{1}{4} A_3(\cos(2\pi ft(3) + 3\Phi_o))) \right] , \quad (3.34)$$

$$Y \approx \left[(A'_1(\cos(2\pi ft + \Phi_o))) + \left(\frac{1}{2} A_2(\cos(4\pi ft + 2\Phi_o)) \right) + \left(\frac{1}{4} A_3(\cos(6\pi ft + 3\Phi_o)) \right) \right]. \quad (3.35)$$

In (3.35), because of the contribution from third harmonic as seen in (3.33), the term A_1 could be re-defined as follows:

$$A'_1 = A_1 + \frac{3}{4}. \quad (3.36)$$

It could be observed that the second and the third harmonic are in phase with the fundamental tone. But, in reality, this condition is not true, due to the presence of phase error which is dynamic with respect to frequency, although static with time. This constitutes the dynamic non-linear distortion, which causes the harmonics' phase to fall out of the fundamental tone's phase (i.e. the harmonics' phase will not be exact multiples of fundamental tone's phase)

Including the dynamic phase error, (3.35) could be re-written as follows:

$$Y \approx \left[(A'_1(\cos(2\pi ft + \Phi_o))) + \left(\frac{1}{2} A_2(\cos(4\pi ft + 2\Phi_o + \Phi_{d2})) \right) + \left(\frac{1}{4} A_3(\cos(6\pi ft + 3\Phi_o + \Phi_{d3})) \right) \right], \quad (3.37)$$

where Φ_{d2} and Φ_{d3} are the dynamic phase errors caused in the second and the third harmonic respectively. Also, (3.37) constitutes the base for the harmonic calibration by making use of the output of the TI ADC and its powers.

3.4.3 Characterization of dynamic phase error

Before characterizing the dynamic phase error, the spectral responses of the TI ADC needs to be calculated. Irrespective of the type of sampling performed, the details of which are mentioned in Section 2.2, the output of the TI ADC is folded back to the first Nyquist zone. Considering the Time-Interleaved ADC as a Nyquist Sampling ADC, the output frequency of the TI ADC could be calculated as follows:

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$$F_o = \begin{cases} \left| \left(\frac{n}{2} \right) F_{\text{samp}} - F_i \right| & n=2,4,6.. \text{even} \\ \left| \left(\frac{n-1}{2} \right) F_{\text{samp}} - F_i \right| & n=1,3,5.. \text{odd} \end{cases}, \quad (3.38)$$

where F_{samp} is the sampling frequency, F_o is the output frequency, F_i is the input frequency, and n is the Nyquist zone.

Nyquist zone n could be calculated by dividing the input frequency by half the sampling rate and rounding up to the nearest integer and is as shown below:

$$n = \left\lceil 2 \frac{F_i}{F_{\text{samp}}} \right\rceil. \quad (3.39)$$

An example demonstrating the use of the equations mentioned in (3.38) and (3.39) is given below.

Considering that the ADC is sampled at 600 MSps and the input signal has a frequency of 550 MHz (present in the second Nyquist zone), the signal shall be folded back to the first Nyquist zone (which could be referred to as aliased signal) and the new frequency of the signal could be calculated as follows:

$$F_o = \frac{2}{2}(600-550) = 50 \text{MHz}, \quad (3.40)$$

where F_o is the aliased signal.

The harmonics of the input signal at 550 MHz could be calculated as follows:

$$F_{HD2} = 2F_i = 1100 \text{MHz} \quad (n=4), \quad (3.41)$$

$$F_{HD3} = 3F_i = 1650 \text{MHz} \quad (n=6), \quad (3.42)$$

$$F_{HD4} = 4F_i = 2200 \text{MHz} \quad (n=8), \quad (3.43)$$

$$F_{HD5} = 5F_i = 2750 \text{MHz} \quad (n=10). \quad (3.44)$$

In (3.41) to (3.44), F_{HD2} , F_{HD3} , F_{HD4} , and F_{HD5} represents the second, third, fourth, and the fifth harmonic respectively.

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Similarly, these harmonics are aliased back to the first Nyquist zone, and their new frequencies are calculated as follows:

$$F_{HD2} = \left| \left(\frac{4}{2} \right) 600 - 1100 \right| = |1200 - 1100| = 100 \text{ MHz}, \quad (3.45)$$

$$F_{HD3} = \left| \left(\frac{6}{2} \right) 600 - 1650 \right| = |1800 - 1650| = 150 \text{ MHz}, \quad (3.46)$$

$$F_{HD4} = \left| \left(\frac{8}{2} \right) 600 - 2200 \right| = |2400 - 2200| = 200 \text{ MHz}, \quad (3.47)$$

$$F_{HD5} = \left| \left(\frac{10}{2} \right) 600 - 2750 \right| = |3000 - 2750| = 250 \text{ MHz}. \quad (3.48)$$

This is illustrated in Figure 3.4.1. Here, the fundamental tone is present in the second Nyquist zone and the harmonics (up till the fifth order is considered) generated are in the higher Nyquist zones. These harmonics are aliased back to the first Nyquist zone.

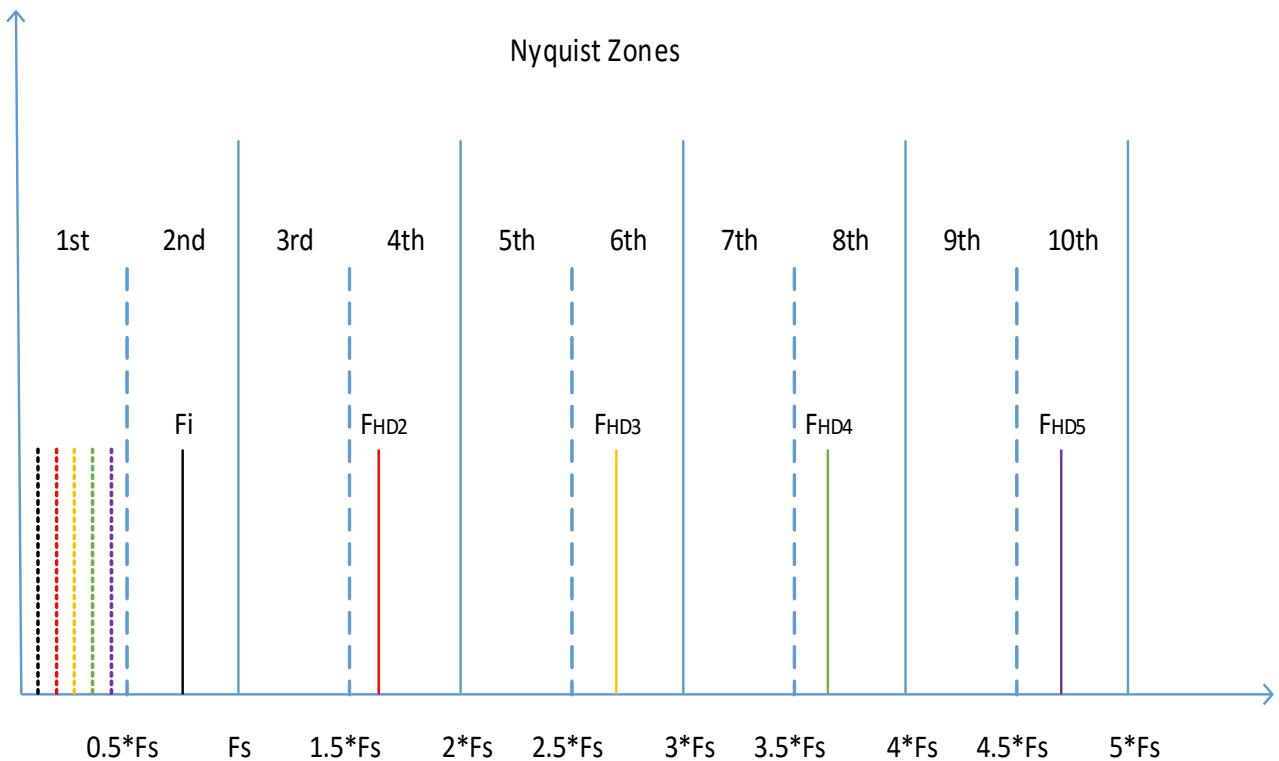


Figure 3.4.1: Aliasing of Fundamental tone and its harmonics (till the fifth order) located in the higher Nyquist zones back to the first Nyquist zone. The dotted lines in the first Nyquist zone represent the aliased signals.

3.4.4 Dynamic phase error estimation

Once the location of harmonics is known, then by performing Fourier transform, the angle of these harmonics could be calculated. The calculations are limited to the second and the third harmonic in the upcoming chapter. The theoretical values of these harmonics could be calculated with the use of (3.29) and (3.32), where $\cos(\Theta)$, $\cos(2\Theta)$, and $\cos(3\Theta)$ are the fundamental tone, second harmonic and the third harmonic respectively.

Once the angle of the harmonics is calculated (both theoretical and from the actual output of the ADC), the difference between the theoretical and the actual value is computed. The calculation of dynamic phase error is a crucial step in the design of the post-correction block since it contains linear time invariant filters. Therefore, the wrap around condition present in FIR filters should be taken into account as well as the sign flip due to the folding of harmonics from the higher Nyquist zones. The latter part could be classified into six different cases as seen in Figure 3.4.2.

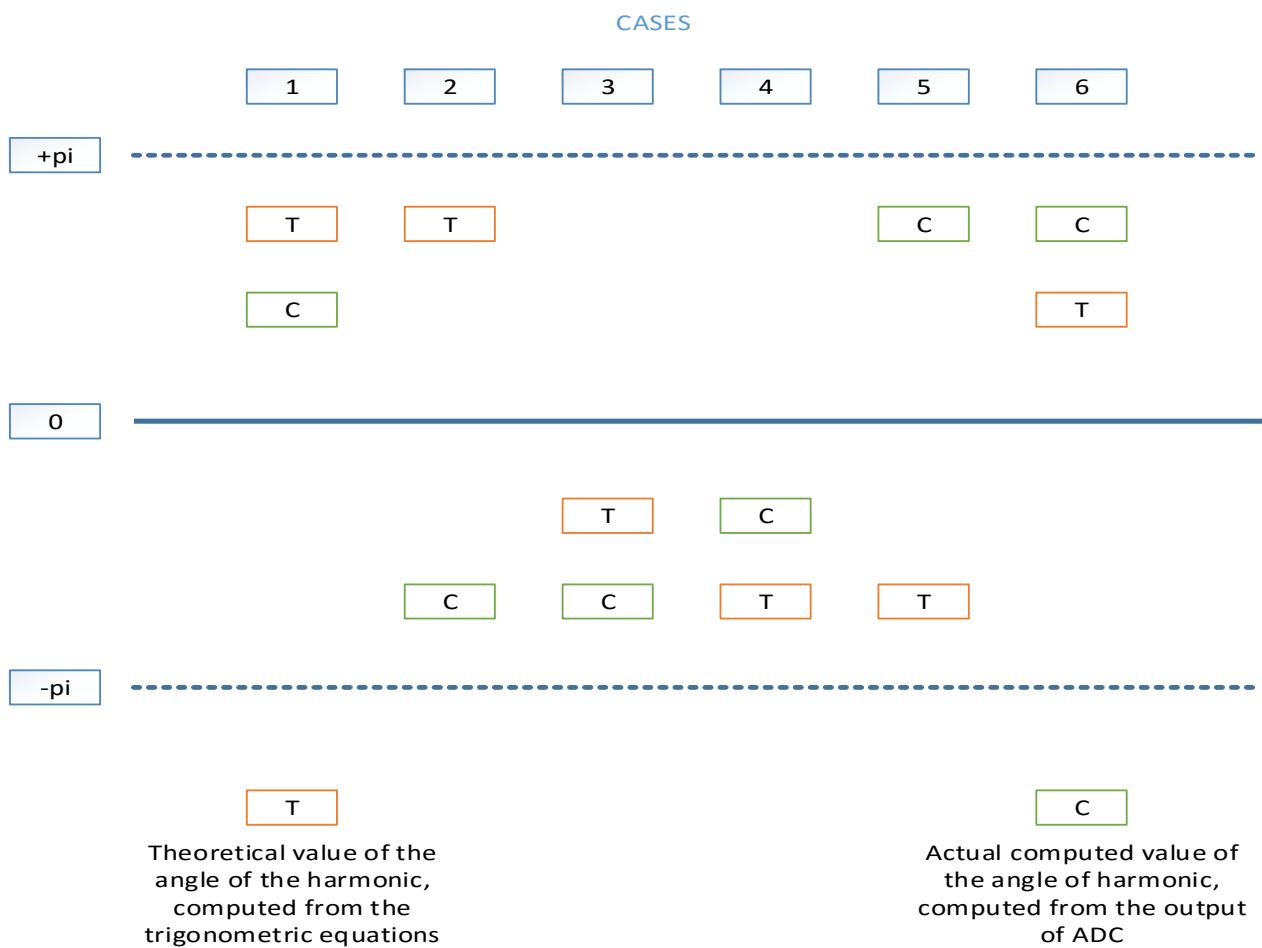


Figure 3.4.2: Wrap around condition of the dynamic phase error.

In Figure 3.4.2, the notation T stands for the theoretical value and C stands for the actual computed value. The resultant angle is obtained by taking the difference of T and C (if T is greater than C) or vice versa depending on which value is greater.

Depending on which Nyquist zone the harmonics are folded back from, the sign of the resultant angle is either inverted or left as it is, after computation. Considering if the harmonic is being folded back from any even Nyquist zone, i.e. $n \bmod 2 = 0$, then for the first three cases, where the theoretical value is greater than the actually computed angle of the corresponding harmonic, the resultant angle is not inverted. Please refer to Figure 3.4.2 for a clear understanding. While, for the last three cases, where the actually computed angle of the corresponding harmonic is greater than its theoretical value, the sign of the resultant angle obtained after subtracting the actually and theoretical value, is inverted.

Similarly, if the harmonic under consideration is folded back from an odd Nyquist zone, i.e. $n \bmod 2 \neq 0$, then for the first three cases mentioned in Figure 3.4.2, the resultant angle's sign is inverted, while for the last three cases the resultant angle's sign is not inverted.

3.5 Characterization of dynamic phase error of sub-converters

The internal architecture of the TI ADC under consideration is not known with respect to whether a single sample-hold (S/H) circuit is used for all the sub-converters or different S/H for different sub-converters. Therefore, the output of the TI ADC was segregated for every fourth sample, in order to obtain each individual sub-converter's output. The dynamic phase error (which could be termed as 'extra phase shift' for simplicity) was calculated for each sub-converter's output. The spread of extra phase shift for harmonics up to the order of seven for different sub-converters is given in Figure 3.5.1 and the spread of extra phase shift for the individual sub-converters to the harmonics up to the seventh order is plotted in Figure 3.5.2. It could be observed that the values of the extra phase shift of the individual sub-converters are different. This implies that different sample and hold circuits are used for each individual sub-converter in the TI ADC. It is only logical that we are supposed to implement a post-correction block at the end of each sub-converter to cancel out the effects of the harmonics. But in the next chapter, we show that it is enough to implement a single post-correction block, that compensates for the harmonics generated from each individual sub-converter in the TI ADC.

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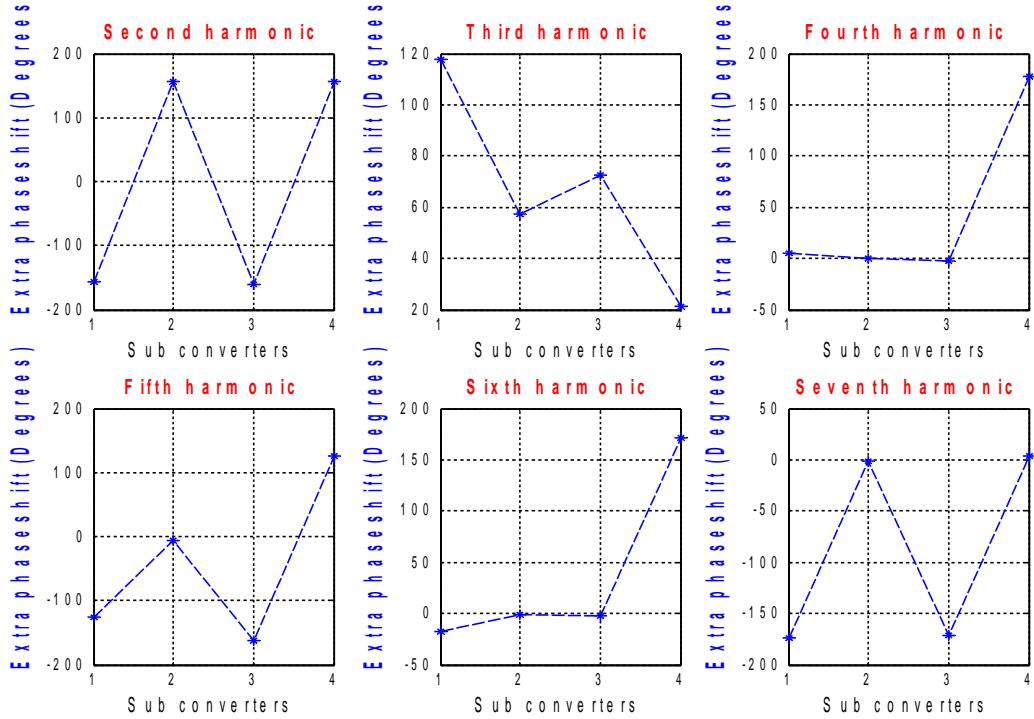


Figure 3.5.1: Spread of extra phase shift of harmonics for different sub-converters.

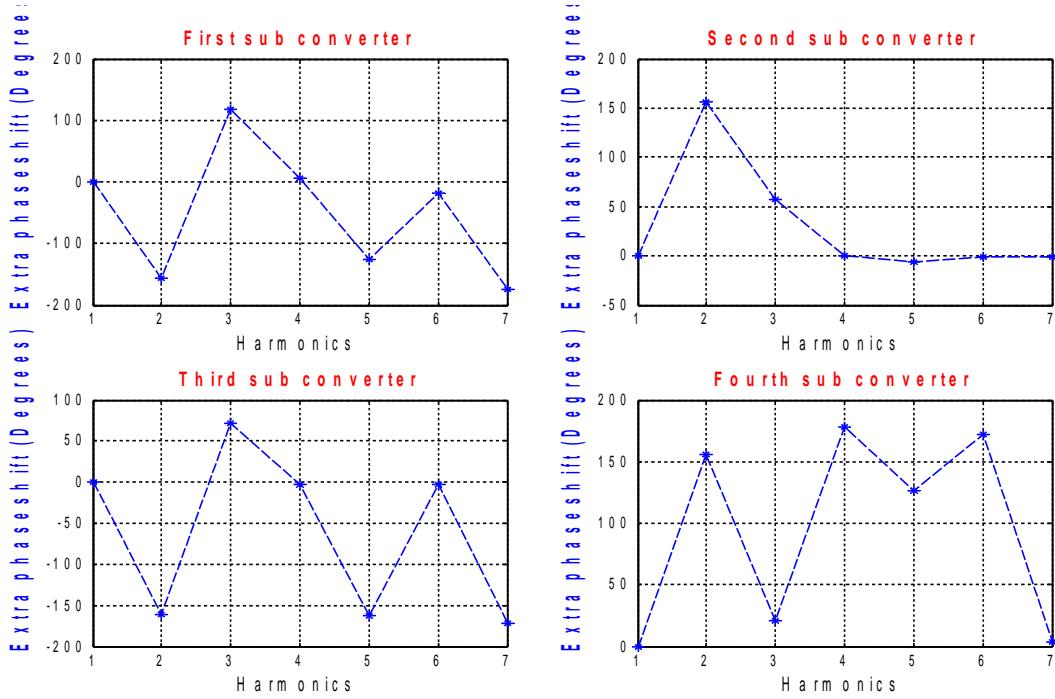


Figure 3.5.2: Spread of extra phase shift of different sub-converters for different harmonics.

3.6 Conclusions

In this chapter, we developed a time domain model of a four channel TI ADC, considering the gain, offset and skew mismatches in order to simulate its effects on the output of the TI ADC. Also, the frequency relations of these mismatches were drawn from the developed time domain model.

We also modelled the harmonics using a memoryless power system which gave a thorough understanding of the frequency relations of the harmonics which are folded back from the higher Nyquist zones. Also, this step was crucial, as it provided a framework for determining the non-linear phase distortion. Along with this, we developed an analytical model of a four channel TI ADC in the frequency domain where it was seen that the whole converter's output is the sum of its sub- converter's output in the frequency domain. This model is really crucial in developing the proposed post-correction block, which shall be explained in the upcoming chapter.

4 COMPENSATION TECHNIQUES

4.1 Introduction

The Time-Interleaved architecture is suitable for applications which require ADCs with a higher sampling rate and a good resolution. But, in the previous chapters, it was seen that the TI ADC suffers from mismatches between its sub-converters, along with the non-linearities generating from each individual sub-converter, which deteriorates the TI ADC's output. With the advancement in the digital circuits, it is of interest that these errors are corrected in the digital domain because of its versatility. Another advantage of this is that once this calibration block is designed, it does not require the knowledge of the input signal, and also the calibration is performed in real time.

In Figure 4.1.1, it could be observed that the TI ADC's output contains a large number of harmonics. This also applies to the individual sub-converters' output, whose average in the frequency domain constitutes the total output of the TI ADC, as demonstrated in Section 3.2. Also, the internal 'on chip' calibration present was not efficient in suppressing the harmonics. This motivated us to develop a compensation method in order to correct the output of the TI ADC for the errors caused by the non-linearities.

In this chapter, we present a post-correction block which is used to compensate for the harmonic tones from the output of the TI ADC. The dynamic phase distortion which was estimated in Chapter 3, is modelled using linear time invariant filters. The modelling is performed in MATLAB. The performance improvements are obtained in terms of IMD (intermodulation distortion) and THD (total harmonic distortion). This chapter is organised as follows. In Section 4.2, we explain the test bed set up in detail, which is used for collecting the output sequences for characterization and testing. In

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Section 4.3, we describe the post-correction block. The results obtained after calibration are presented in Section 4.4, and Section 4.5 concludes the chapter.

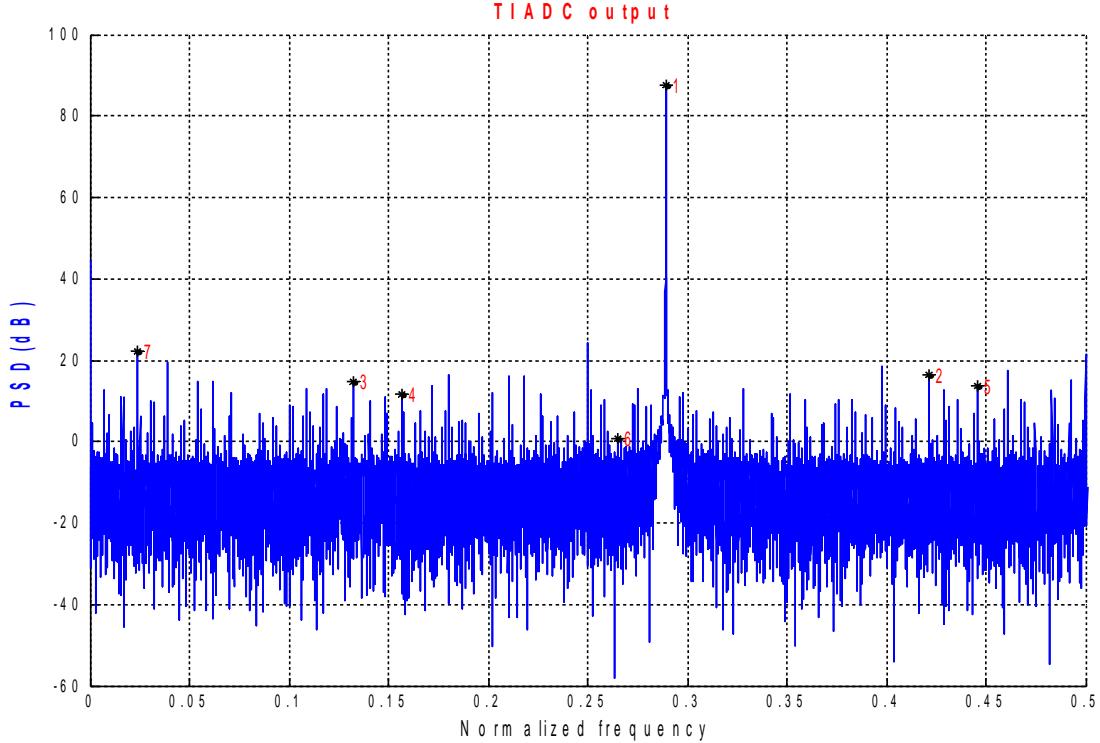


Figure 4.1.1: TI ADC's output for an input sinusoidal signal whose frequency = 0.289π .

4.2 Experimental setup

The device under test and the test bed Set up that was used in this thesis work shall be briefly explained in this section.

4.2.1 Device under test

The ADC under consideration is a commercial 12-bit, four channel Time-Interleaved ADC (TIADC12J400) by Texas Instruments [19], intended for direct Radio frequency sampling, which operates up to a four GSps conversion rate. According to the data-sheet, it has a spurious free dynamic range (SFDR) ranging from 59.8 dBFS to 70.7 dBFS for the frequencies within the bandwidth under consideration at -1 dBFS. A typical SFDR value is 63.4 dBFS at 600MHz. The signal to noise ratio (SNR) is typically 53.9 dBFS and the effective number of bits (ENOB) is 8.7 bits at 600 MHz. In the Time-Interleaved ADC, the sub- converter's present in each channel is of pipeline architecture.

4.2.2 Test bed set-up

The test bed used for the TI ADC measurements is shown in Figure 4.2.1. The evaluation module consists of two boards [20], and they are an FPGA data capture board, with a Xilinx Kintex-7 FPGA and the ADC evaluation board. Two different software packages are installed on a personal computer (PC), one to configure the evaluation board and the other one is used for data capture. More information about the test bed set up, in general, could be found in [21]. The RF input signal is generated with a Rohde & Schwartz SMA100A signal source followed by a K&L low pass filter to clean the RF input signal from the harmonics generated by the signal source (up to -80dBFS). The data used for characterization is measured at -1 dBFS. An additional signal source is used for the two-tone test. It is also connected to a spectrum analyser with the help of an Agilent directional coupler for monitoring. An external signal generator (Agilent MXG) followed by a low pass filter and a power divider is used to create the clocking signals for both LMCLK (clocking used for FPGA) and DEVCLK (ADC12J4000 sampling clock). Also, a 3 dB attenuator is connected to LMCLK input to get 3 dB lower power. The ADC output sequences of length 2^{16} samples (which is greater than $2^N\pi$ [22]) were taken at certain calculated frequencies at an interval of 20 MHz, in the bandwidth under consideration, with the help of data capture software.

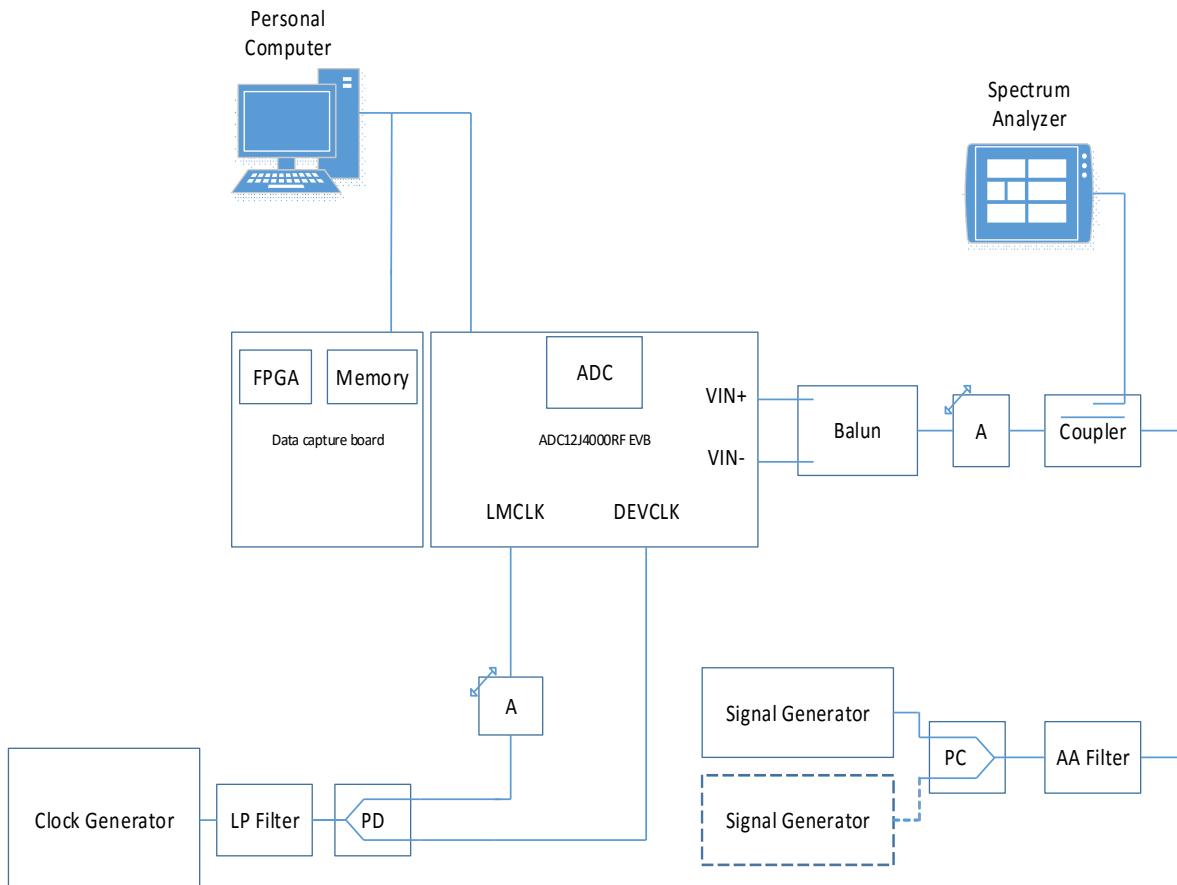


Figure 4.2.1: Test bed schematic used to characterize the TI ADC under consideration.

Distortion Cancellation in Time-Interleaved ADCs

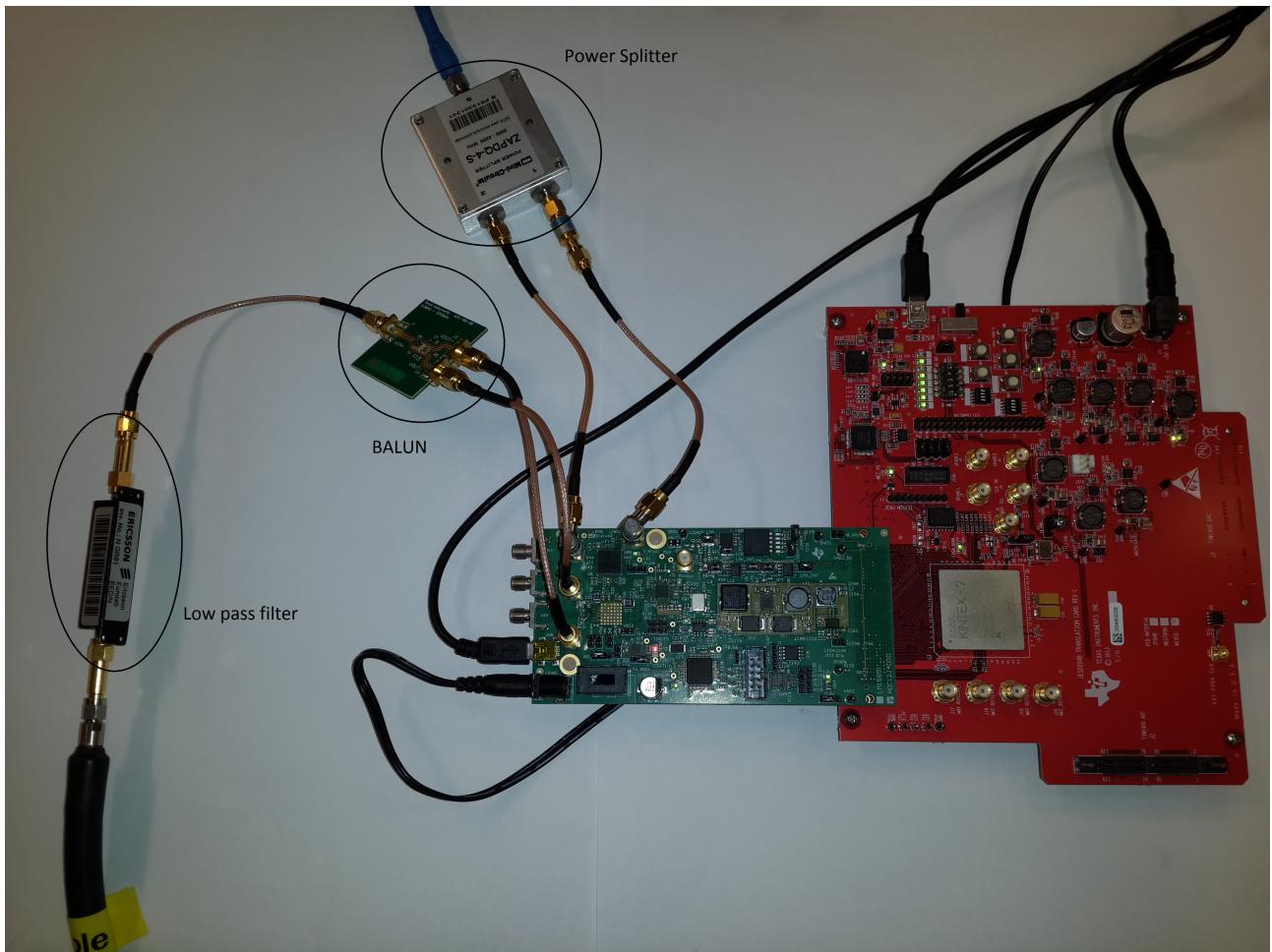


Figure 4.2.2: Actual photo of the evaluation module used to characterize the TI ADC under consideration.

In Figure 4.2.2, the red color board is the FPGA data capture board and the green color board is the TI ADC evaluation board. The actual TI ADC under consideration is behind the evaluation board and is as shown in Figure 4.2.3.

Distortion Cancellation in Time-Interleaved ADCs

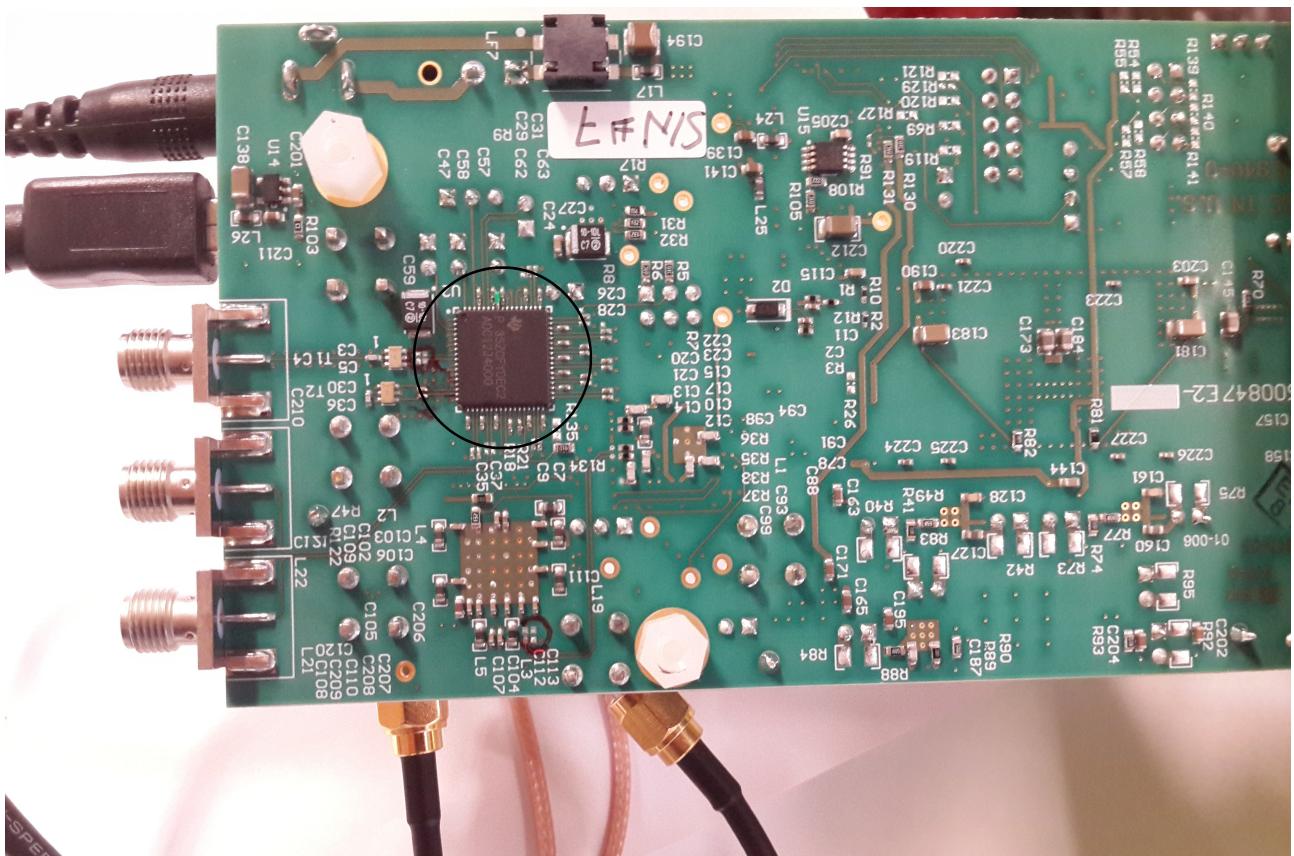


Figure 4.2.3: Actual photo of the TIADC12J4000 (the one marked in black circle).

4.3 Post-correction of harmonics

WARNING: Due to the confidentiality policy of ERICSSON AB, certain parts of this section are truncated in order not to disclose critical details about the company's on-going developments on this topic.

The post-correction block [23], used to cancel out the harmonics up to the order of L is presented in Figure 4.3.1. As mentioned above, due to confidentiality policy, we represent the post-correction block as a black box. The output code of the TI ADC $x(n)$, is given as an input to the post-correction block. We have implemented the calibration technique for the second and the third harmonic, but this method holds true for any order harmonic without the loss of generality.

The post-correction block contains linear time invariant (LTI) filters, which are designed using certain frequency points f_k , where k varies from one to K in the bandwidth under consideration. The normalised output code $x(n)$ and its powers $x^{L-1}(n)$ (for L^{th} harmonic) are weighted by the frequency response of the corresponding LTI filter, which is then used to generate the post-correction term. This is added to the output of the TI ADC to obtain the calibration. The parameters required for the filter design are dependent on ADC input $x(t)$.

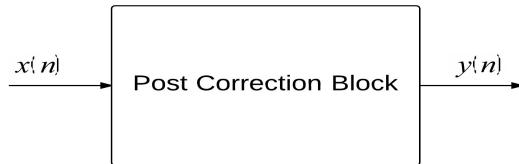


Figure 4.3.1: TI ADC post-correction block. Here $x(n)$ is the output code of the TI ADC which is input to the post-correction block. $y(n)$ represents the corrected output, post calibration.

The bandwidth under consideration is divided into K equally spaced frequency points. The frequency selection at these points will be dealt in Subsection 4.3.1. The magnitude and the phase responses of the filter G_L , designed for L^{th} harmonic could be defined as follows:

$$\angle G_L(w_k) = \Phi_{dL,k}, \quad (4.1)$$

where $\angle G_L(w_k)$ is the phase response of the LTI filter, and $\Phi_{dL,k}$ is the non-linear phase term or the extra phase shift of L^{th} harmonic at frequency w_k .

Similarly,

$$|G_L(w_k)| = r_{L,k}, \quad (4.2)$$

where $|G_L(w_k)|$ is the magnitude response of the filter at frequency w_k , and $r_{L,k}$ is the ratio of the magnitude of the L^{th} harmonic over the magnitude of the input fundamental tone, which could be obtained by performing FFT on the TI ADC output code $x(n)$.

Also, $r_{L,k}$ is defined as:

$$r_{L,k} = \frac{|X(f_L)|}{|X(f_k)|}, \quad (4.3)$$

where $X(f_L)$ and $X(f_k)$ are the frequency bins of the L^{th} harmonic and the fundamental tone, respectively.

In (4.1) and (4.2), w_k is the normalized frequency which can be defined as follows:

$$w_k = \frac{2\pi f_k}{f_{samp}}, \quad (4.4)$$

where f_{samp} is the sampling frequency of the TI ADC, and k varies from one to K .

The designed filter for L^{th} harmonic has a corresponding magnitude and phase response whose values are obtained from characterization, as mentioned in (4.1) and (4.2). Also, the response for negative frequencies is implicitly mirrored.

4.3.1 Frequency selection of sine wave for characterization

As mentioned previously, the signal bandwidth under consideration is divided into K frequency points at which the characterization is performed to obtain the parameters required to design the LTI filter. The frequency selection is a critical step [22], [24], in order to make sure that, with the frequency under consideration, it is possible to obtain maximum number of distinct input signal phases that are sampled by the TI ADC in M points which are equal to the total number samples (record length). It also ensures that there is, at least, one sample for each output code of the TI ADC.

The frequency selection is performed in three stages, coarse, medium and fine. The coarse and medium stages' criteria are taken care of after determining K number of

frequency points in the bandwidth under consideration, by making sure that the higher order harmonics do not coincide with the lower order harmonics after being folded back to the first Nyquist zone. The frequency selection in fine stage is performed by considering the following condition:

$$f_{sel} = \frac{J}{M} f_{samp}, \quad (4.5)$$

where f_{sel} is the selected frequency, f_{samp} is the sampling frequency, and J is an integer which is mutually prime to M .

This condition of choosing mutually prime frequencies with respect to the sampling frequency makes sure that the samples in each recorded output sequence are uniformly distributed in phase, from 0 to 2π .

4.3.2 Spread of the extra phase shift and the magnitude ratio

The post calibration block is designed for the bandwidth where the frequencies are ranging from 690 MHz to 1.11 GHz. Therefore, in the given bandwidth, the frequency points are considered at every 20 MHz and the frequency selection is performed as mentioned in Subsection 4.3.1. Here, the extra phase shift and the magnitude ratio of the output of the whole converter (TI ADC) is plotted for the second harmonic, for different sets of output data and the same is shown in Figure 4.3.2.

One could easily observe that the extra phase shift and the magnitude ratio for different sets of data are converging. This facilitates us to implement the post-correction block in an easier way i.e. a single post-correction block for the second harmonic suppression could be designed at the output of the TI ADC, without having the knowledge of individual sub-converter's output. This is better explained in Section 3.2 where the final output of the TI ADC is represented in terms of its sub-converters' output. Therefore, the extra phase shift and the magnitude ratio of the total output will be the resultant sum of its individual sub-converters' output.

Also, we do not have access to the individual sub-converters' output. Although, while characterizing, segregation of individual sub-converters' output could be performed easily by separating every fourth sample from the total output in MATLAB. But, it is still difficult to obtain similar converging values of the extra phase shift and the magnitude ratio for each sub-converter since the sampling instant of while capturing the output at the data capture unit is not synchronized and therefore, the reference keeps varying for different sets of data.

The extra phase shift and magnitude ratio of the output of the whole converter (TI ADC) are plotted for the third harmonic in Figure 4.3.3. The average of these values shall be used to design the filter used in the post-correction block.

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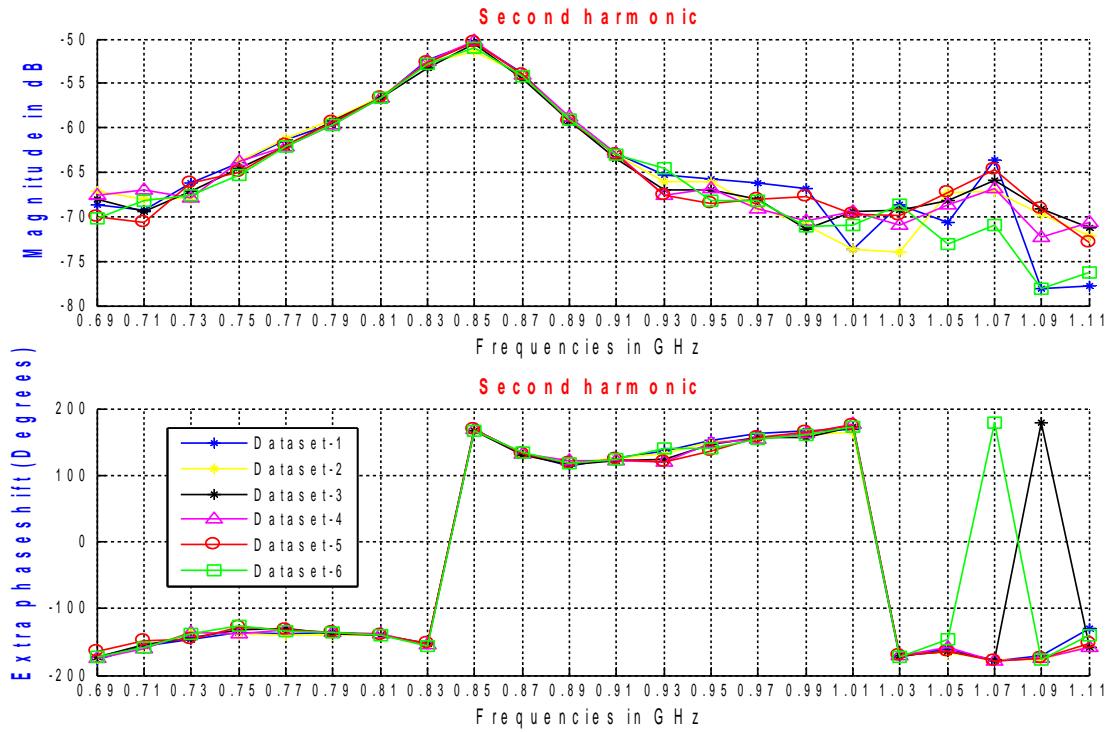


Figure 4.3.2: The spread of the extra phase shift and the magnitude ratio over the bandwidth under consideration for the second harmonic.

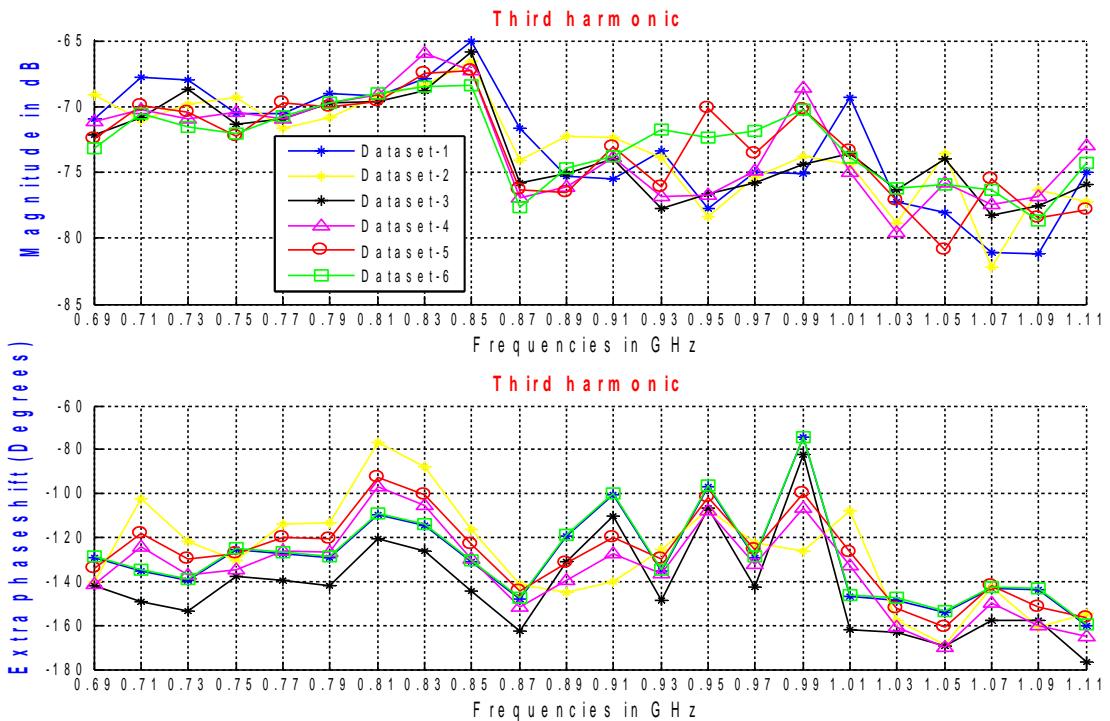


Figure 4.3.3: The spread of the extra phase shift and the magnitude ratio over the bandwidth under consideration for the third harmonic.

4.3.3 Weighted least squares approach

The LTI filters are designed using weighted least squares method [23], [25], [26], whose frequency response is based on the extra phase shift and the magnitude ratios which are obtained after characterising the second and the third harmonic. The frequency responses of the LTI filters designed for the second and the third harmonic are shown in Figure 4.3.4 and Figure 4.3.5 respectively. The phase response is critical in this case, and it could be observed that the average error in phase response is less than 0.1π . For the second harmonic, the extra phase shift and the magnitude ratio are converging for the different sets of output data obtained from the TI ADC under consideration. In Figure 4.3.2, one could observe that there is a toggle between -180 degrees and 180 degrees in the phase response at 1.07 GHz and 1.09 GHz for the dataset 3 and dataset 6. This is taken care of by the wrap around condition of FIR filter where -180 and 180 degrees are equal. Therefore, we considered the dataset one to design the second harmonic filter. But in the case of the third harmonic, although there is a similarity in the pattern, there is a slight variation in the extra phase shift and the magnitude ratios obtained after characterizing the different sets of output data. Therefore, we consider the mean of the extra phase shift and the magnitude ratio of different datasets to design the third harmonic filter. Also, the magnitude ratios and the extra phase shift tend to stabilize over time.

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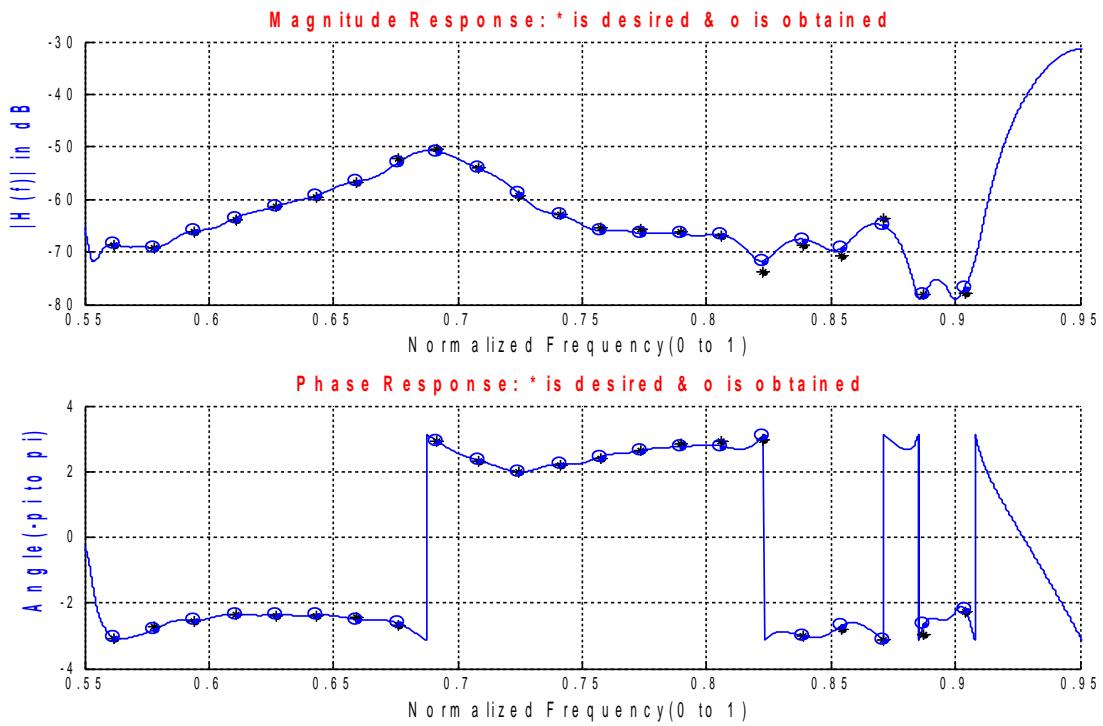


Figure 4.3.4: Second harmonic filter design for the bandwidth under consideration.

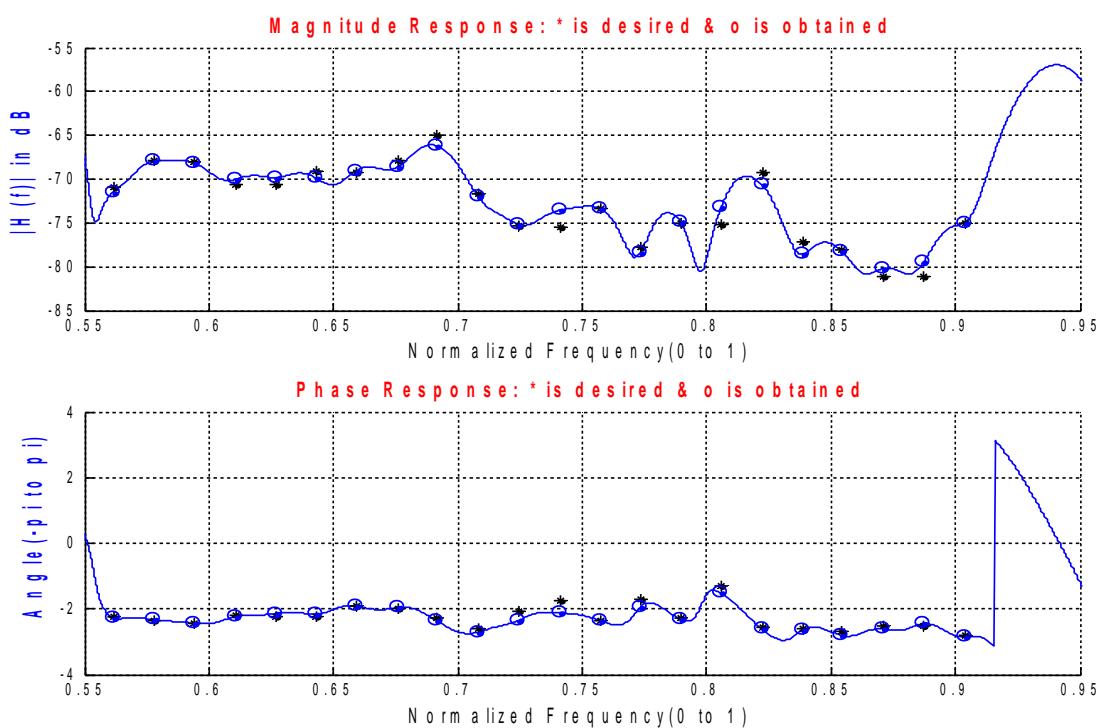


Figure 4.3.5: Third harmonic filter design for the bandwidth under consideration.

4.4 Experimental validation

The characterization of the extra phase shift and the magnitude ratio was performed over 420 MHz wide frequency band ranging from 690 MHz to 1110 GHz for the TI ADC under consideration. The TI ADC's output was collected at specific input frequencies spanning the bandwidth with a frequency step of 20 MHz. The data used for characterization was measured at -1 dBFS (Decibels relative to full-scale). The figure of merits (FOM) used to measure the performance improvements in the TI ADC under consideration, after using the post-correction methodology are IMD and THD. Since the second and the third harmonic are not the only spurious tones present in the output spectrum of the TI ADC, we are considering SFDR as a figure of merit only during the cases when either the second or the third harmonic is the highest spur in the output spectrum.

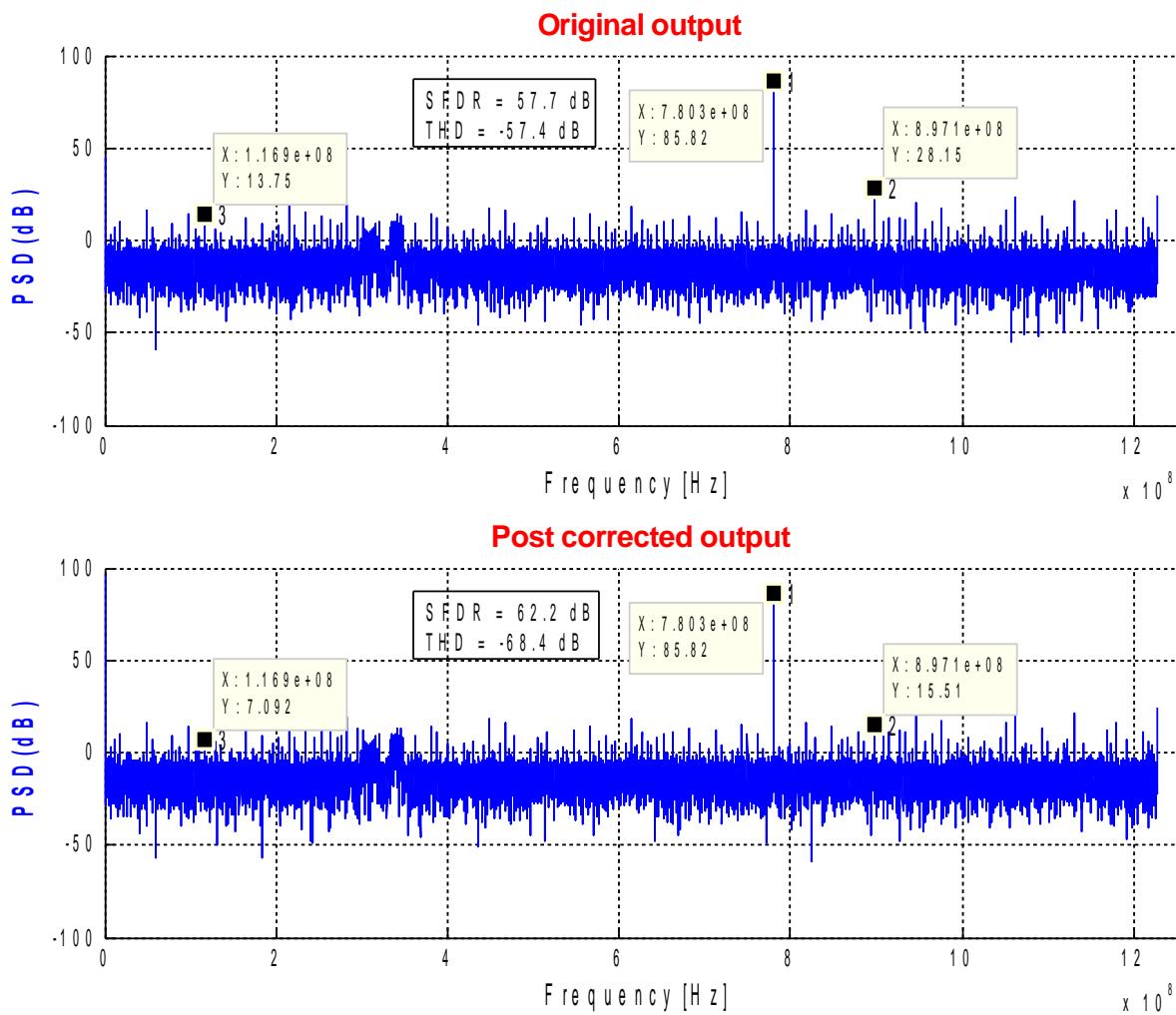


Figure 4.4.1: Improvements in the SFDR and the THD for the output sequence of the TI ADC measured at 780 MHz.

Distortion Cancellation in Time-Interleaved ADCs

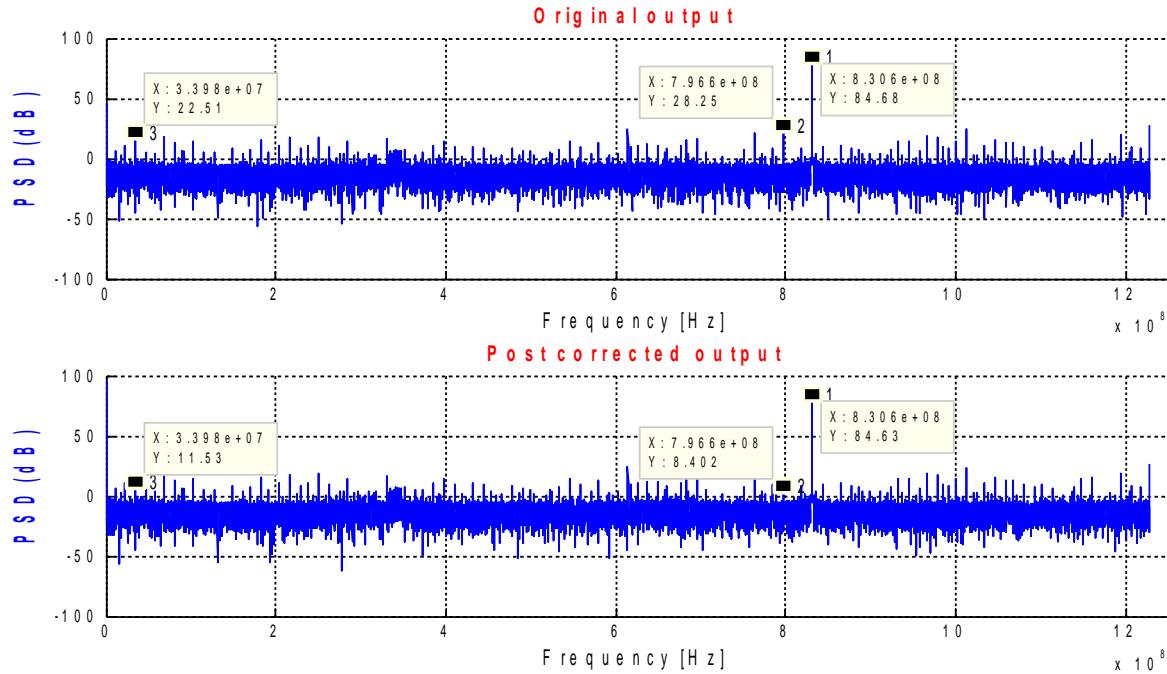


Figure 4.4.2: The original output sequence and the post corrected output of the TI ADC measured at 830 MHz. It could be clearly observed from the post corrected output that the second and third harmonics are suppressed by 19.8 dB and 11 dB respectively.

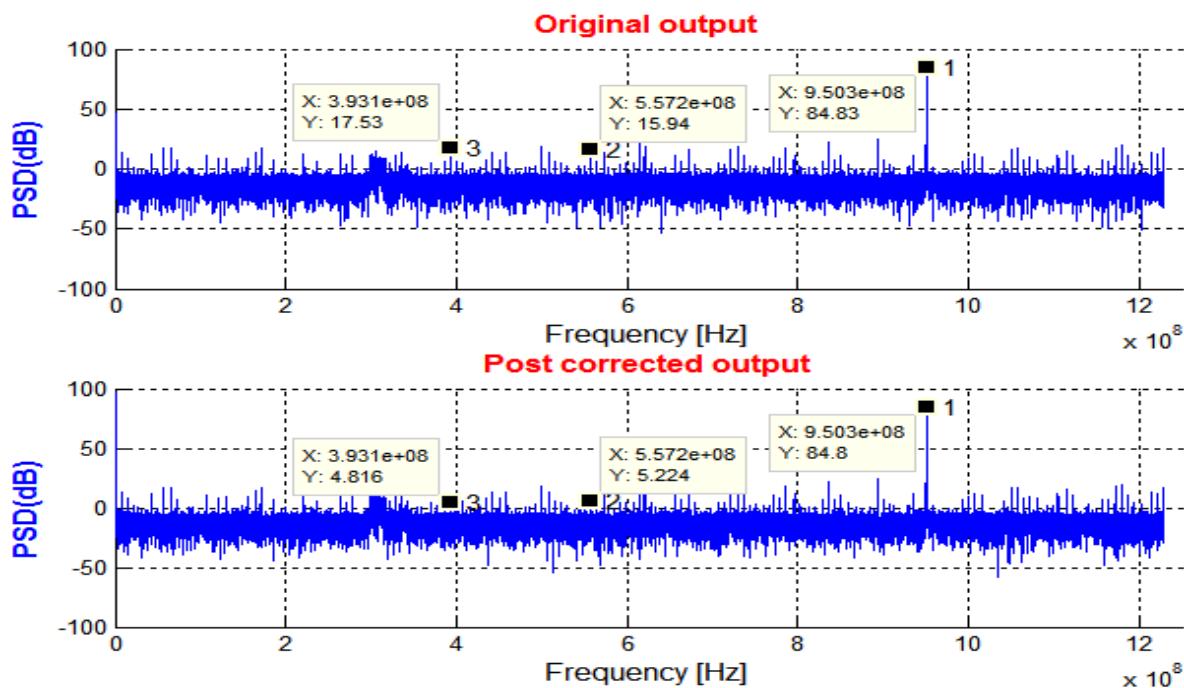


Figure 4.4.3: The original output sequence and the post corrected output of the TI ADC measured at 950 MHz. It could be clearly observed from the post corrected output that the second and third harmonics are suppressed by 10.7 dB and 12.7 dB respectively.

Distortion Cancellation in Time-Interleaved ADCs

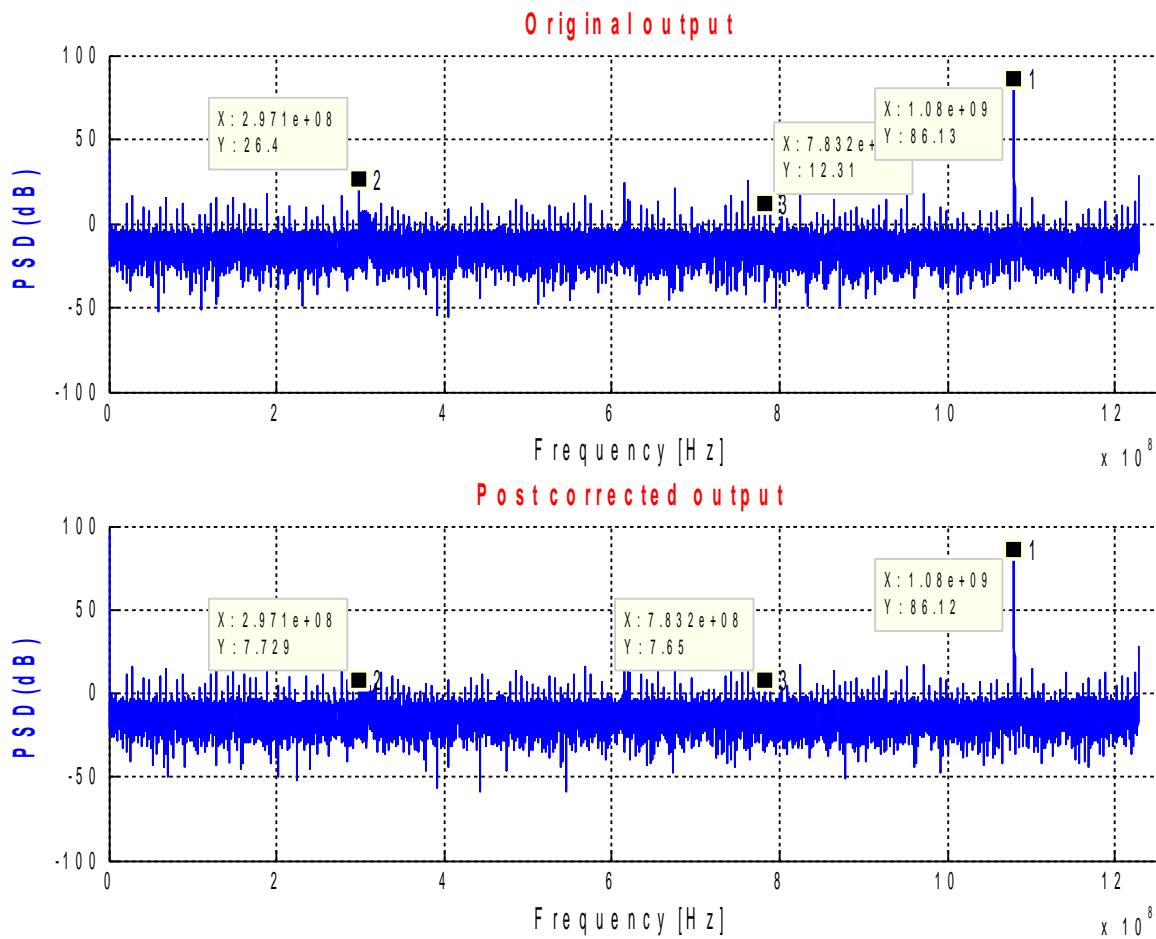


Figure 4.4.4: The original output sequence and the post corrected output of the TI ADC measured at 1080 MHz. It could be clearly observed from the post corrected output that the second and third harmonics are suppressed by 18.6 dB and 4.7 dB respectively.

4.4.1 THD and SFDR improvements

The post-correction block was evaluated for various single tone input signals, traversing the bandwidth under consideration. As an illustration, the improvements in SFDR and THD for a 780 MHz output sequence of the TI ADC is shown in Figure 4.4.1. An improvement of 4.5 dB in the SFDR and 11 dB in the THD is achieved. The THD is calculated with respect to the first five harmonics. More details about THD and SFDR calculation could be found in Section 2.5.

Similarly, the evaluation of the post-correction block for the TI ADC's output sequences at 830 MHz, 950 MHz and 1030 MHz are shown in Figure 4.4.2, Figure 4.4.3, and Figure 4.4.4 respectively.

The improvements in THD over the bandwidth in use is shown in Figure 4.4.5. Also, the magnitude of the second and third harmonic suppression is shown in Figure 4.4.6. The output sequences of the TI ADC used to test the post-correction block were different from the ones used for characterization. The frequencies in between the characterized frequencies were also considered for validation.

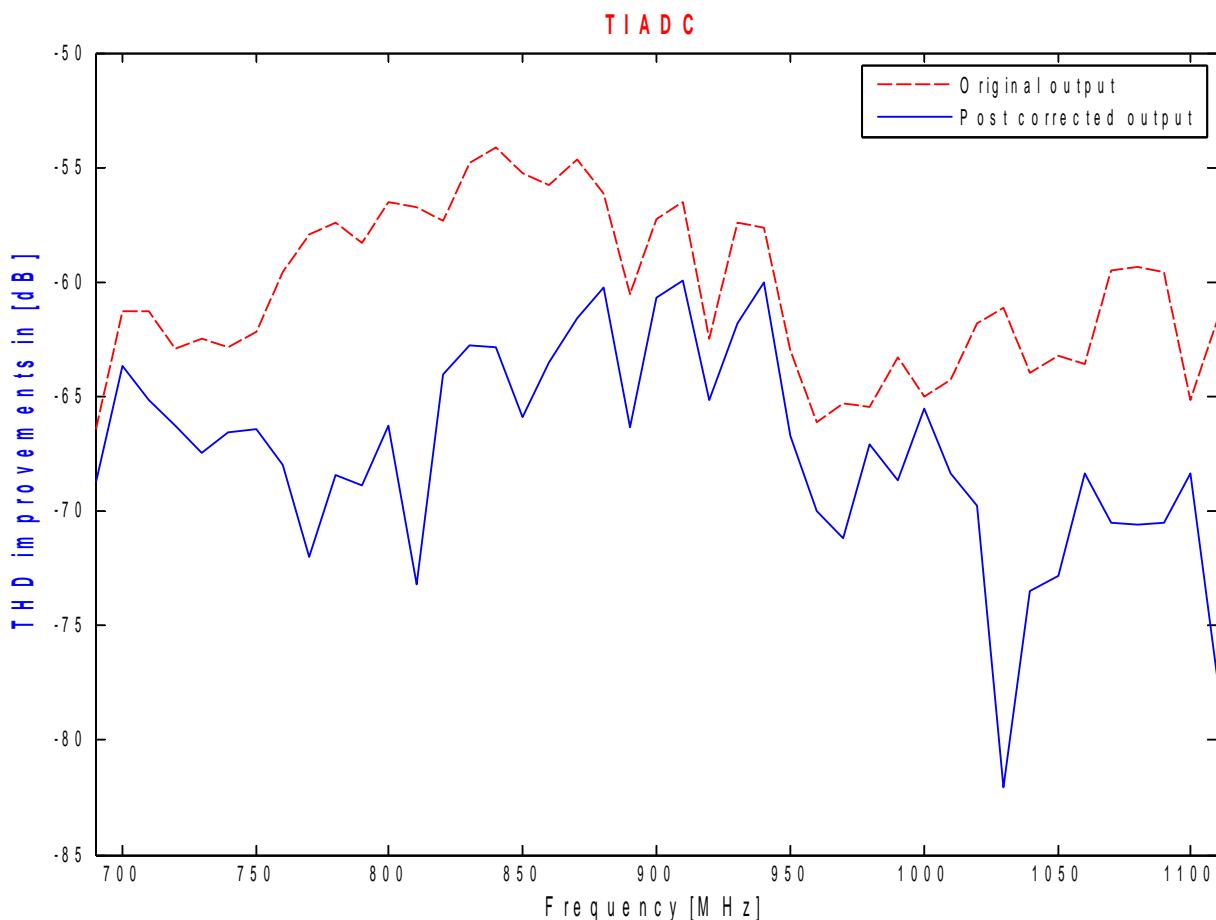


Figure 4.4.5: Improvements in the THD in the TI ADC's output observed over the bandwidth under consideration.

Distortion Cancellation in Time-Interleaved ADCs

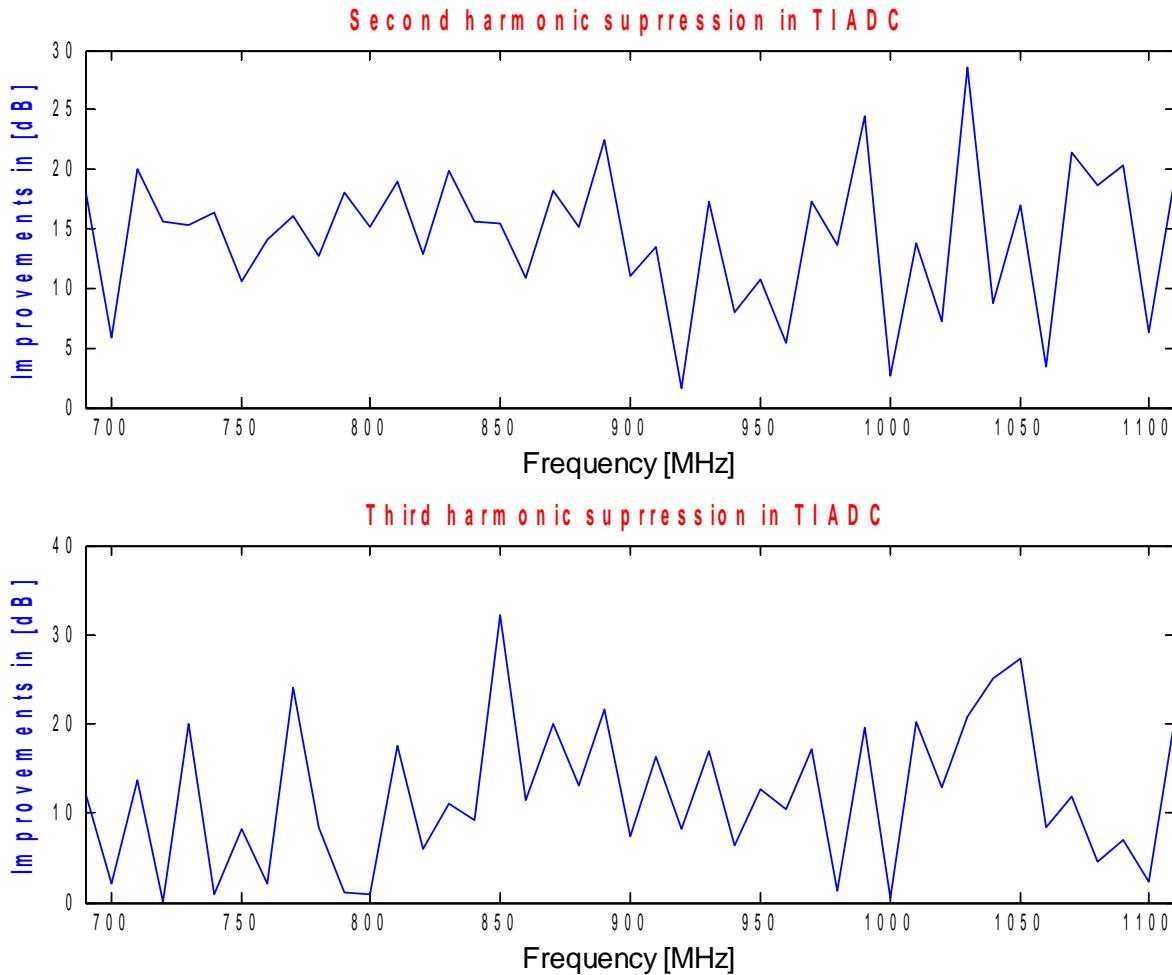


Figure 4.4.6: The magnitude of the second and third harmonic suppression over the bandwidth under consideration.

4.4.2 IMD improvements

Two-tone tests were performed for the TI ADC under consideration for various cases to observe the improvements in IMD (Intermodulation Distortion) [27]. To avoid the intermodulation between the signal generators we had to change the bandpass filter ranging from 880 MHz to 920 MHz due to the unavailability of isolators at the output of signal generators. The IMD improvements are presented in Table 4.1. In all the cases, the two- tone input at -5 dBFS were considered. Also, the third order IMD products (i.e. $2f_1 - f_2$ and $2f_2 - f_1$) are the most critical ones since they occur near the two-tone input.

Frequencies		f1 = 880 MHz f2 = 890 MHz		f1 = 890 MHz f2 = 900 MHz		f1 = 898 MHz f2 = 909 MHz		f1 = 909 MHz f2 = 915 MHz		f1 = 910 MHz f2 = 920 MHz	
IMD & Harmonics		BC	PC								
1	2.f1	-68.83	-76.61	-72.32	-76.94	-71.2	-75.61	-73.33	-88.03	-69.27	-79.9
2	2.f2	-68.95	-76.63	-69.05	-76.83	-69.93	-75.31	-71.18	-84.67	-74.69	-88.11
3	f1 + f2	-62.22	-71.42	-63.49	-69.87	-64.46	-70.35	-65.75	-78.45	-65.37	-74.76
4	f1 - f2	-64.05	-71.27	-65.03	-71.03	-66.09	-74.26	-66.83	-73.31	-65.71	-70.73
5	2.f1 + f2	-69.63	-76.71	-71.27	-84.06	-73.1	-88.12	-76.73	-82.35	-77.75	-86.85
6	2.f2 + f1	-69.6	-77.61	-71.23	-84.04	-72.53	-92.62	-75.41	-79.86	-78.77	-86.05
7	2.f1 - f2	-70.32	-79.65	-71.38	-83.85	-72.67	-95.62	-76.24	-79.95	-80.09	-86.61
8	2.f2 - f1	-70.43	-81.5	-70.77	-81.55	-73.96	-80.86	-76.83	-80.25	-78.27	-82.49
9	3.f1	-72.61	-75.81	-74.74	-78.47	-80.54	-98.33	-88.96	-98.24	-80.31	-83.47
10	3.f2	-71.71	-74.51	-74.02	-77.79	-79.44	-91.45	-86.26	-92.75	-85.64	-89.47

Table 4.1: TI ADC's IMD measurements in dBFS. **BC** denotes Before calibration and **PC** denotes Post calibration. Rows 3 and 4 denote the second order IMD and the rows 5 to 8 denote the third order IMD.

4.5 Conclusions

We have presented a technique to compensate for the harmonics caused by the non-linearities. The post-correction block presented here is input dependent i.e. the parameters required to design the LTI filter (for the extra phase shift and the magnitude ratio) is obtained by characterizing the output sequence recorded from the TI ADC. This method is interesting from an implementation point of view since it requires a relatively small amount of hardware. Also, it requires the storage of notably fewer parameters when compared to the LUT methods [28]. Another advantage of this method over LUT is that there is no need for additional interpolation to cover the cases of in-between frequencies (i.e. any frequency other than those used for characterization) since we assume that the extra phase shift and magnitude ratio vary smoothly between the frequencies used for characterization. This method is valid for the other ADC architectures too.

5 DISCUSSION

In this chapter, the results presented in the previous chapter shall be analysed and discussed. Along with this, we shall discuss the methods used and its reliability.

5.1 Results

The post corrected output, as compared to the original output for the case when an input sinusoidal signal at 780 MHz is used, is as shown in Figure 4.4.1. One could observe that there is an improvement of 12.64 dB and 6.65 dB for the second and the third harmonic respectively. Similarly, in Figure 4.4.2, one could observe the post-calibration result, where an improvement of 19.8 dB and 11 dB is obtained for the second and the third harmonic respectively when an input sinusoidal signal at 830 MHz is used. Similarly in Figure 4.4.3, a case when an input signal at 950 MHz is used, the improvement was found to be 10.7 dB and 12.7 dB for the second and third harmonic respectively. In Figure 4.4.4, an improvement of 18.6 dB and 4.7 dB is obtained for the second and the third harmonic respectively for the case when an input signal at 1.08 GHz is used. The spread of calibration for the second and third harmonic over the bandwidth under consideration is shown in Figure 4.4.6.

In most of the cases mentioned above, there is a remarkable improvement when we consider the suppression of the second and the third harmonic with the use of the developed post-correction block. Although, one could argue that in certain cases, say at 800 MHz and 1 GHz, there is a little improvement when it comes to the suppression of third harmonic. This could be attributed to two reasons.

- First one being, the magnitude of the harmonics at certain frequency points are really low even before the calibration was performed. Therefore, post calibration the suppression of these harmonics shows an improvement which appears to be

low or negligible when compared to the other frequency points in the bandwidth under consideration in spite of efficient suppression of the harmonics.

- While proposing the post-correction block an assumption was made. That is while characterizing the TI ADC under consideration for the phase error and the magnitude ratio as explained in Subsection 4.3.2, it was assumed that the frequencies in between any two selected frequency points will have an average error function which shall be an average of these two frequency points. But one could observe that in Subsection 4.3.2, the values of the third harmonic were not always converging for different sets of output sequences. This kind of contradicted to the assumption made in the first place. But after strenuous debugging, it was found that the power level of the input signals generated by the function generator kept varying for different input frequencies (which was not expected) when the TI ADC output sequences were collected for characterization. This had a considerable impact on dynamic phase error. Therefore, with estimates of dynamic phase error varying for different sets of data, the initial post-correction block designed for suppression of the third harmonic had to be redesigned, since it sometimes even resulted in negative calibration. This could be attributed as another reason as to why at certain frequencies there is low suppression of the harmonic under consideration.

Also, in Figure 4.4.5, one could observe considerable improvements in the THD although we considered up to the fifth harmonic while calculating the THD. This shows that the developed post-correction block is really efficient in suppressing the harmonics.

Another measure to check the validity of the proposed post-correction block is IMD. Several two-tone tests were performed. The details of which could be found in Table 4.1. In all the cases there were huge improvements in the suppression of IMD products. Also, the third order IMD products (i.e. $2f_1 - f_2$ and $2f_2 - f_1$) are the most critical ones since they occur near the two-tone input and are difficult to filter out. The developed post-correction block is successful in suppressing these tones. This validates the developed post-correction block.

5.2 Methods

This work started off at a theoretical level, where two different analytical models of a four channel TI ADC were developed to get a thorough understanding of the working of the TI ADC. After this, we considered the non-linearity modelling which was crucial since the aim was to develop a post-correction block for the suppression of harmonics. Later, the internal structure of the correction block was designed and with the LTI filter design being a crucial part, this took a considerable amount of time due to unavailability of filter design methods which was capable of designing an optimized, real-valued FIR filter of a lower order.

5.3 Reliability

The developed post-correction block is successfully validated for different sets of output sequences collected from the test bed setup. It was capable of suppressing the harmonics for all these data sets. This makes the developed post-correction block worth implementing on an ASIC to be used in real time. Although one could speculate about the cost of hardware. This design requires a 30-40 tap FIR filter and a MAC unit for each harmonic. Although, operating a 40 tap filter at few GHz would still be costly, implementation wise. But if the implementation is done for a down converted sampling frequency, say by a factor of five, then this design could be easily realizable in an ASIC.

The developed post-correction block is advantageous over the generic LUT methods since it would require comparatively fewer storage parameters and also, there is no need for any additional interpolation to cover the cases of in-between frequencies since we assume that the extra phase shift and magnitude ratio vary smoothly between the selected frequencies points used, which are used for characterization.

Another important aspect is that this post correction block is valid for other architectures of ADC, i.e. it is architecture independent. This simply means that the same methodology applies to the other ADC architectures such as pipeline ADCs and sigma-delta ADCs.

6 CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

Various subjects have been treated in this work of distortion cancellation in TI ADCs. In Chapter 2, we studied the industrial needs of ADCs that are used in the modern communication systems which are supposed to have higher sampling rates along with a good resolution, and also how the TI ADC is a good option for achieving the same. We also saw that this architecture has drawbacks because of the mismatches present between its sub-converters. Also, the TI ADC under consideration contained a lot of harmonics that motivated us to develop a digital compensation technique for the same, due to the several advantages it offered over its analog counterpart.

In Chapter 3, we developed a model which shows that the output of the TI ADC is a sum of its sub-converters' output in the frequency domain. The process of developing this model was very useful, since it gave a deep insight about the harmonics caused by the non-linearities, and it was known that the harmonics present at the output of the TI ADC were, in fact, the average of the sum of the harmonics originating in its individual sub-converters. This facilitated us in proposing a compensation method to mitigate the harmonics at the output of the TI ADC without having to worry about the individual sub-converters' output. Also, a time domain model of the TI ADC was created, to understand the effects caused by the mismatches. For that purpose, we demonstrated the results of a two-tone test for this model. These results were used to obtain the expressions to calculate the frequencies of spurs caused by these mismatches. Along with this, the harmonics caused by the non-linearities were modelled and the extra phase shift and the magnitude ratios were obtained for the second and the third harmonic.

In Chapter 4, we presented a post-correction block that has the ability to dynamically compensate the harmonics of any order. This method is based on linear filtering of the output sequence of the TI ADC and this filtered output is used to produce the correction signals which when added to the output of the TI ADC mitigates the corresponding harmonic. The major breakthrough here is the filter design since we design a low order real co-efficient filter that is capable of creating the inverse model of harmonics, including its non-linear phase distortion. The performance analysis showed that, once the filters are designed for the non-linearities upon characterization, this technique was efficient for any type of sinusoidal input signal within the limits of the bandwidth, for which the post-correction block is designed. Also, the test bed set up used for collecting the output sequence of the TI ADC was explained in detail.

6.2 Future work

Although the post-correction block was validated successfully, the TI ADC under consideration contained harmonics up to the order of 60 which clearly indicates that this is not a state of the art ADC for communication systems. Even though the proposed post-correction block is capable of correcting the harmonics of any order, the computational complexity increases drastically with higher order harmonics which makes it impractical to implement the post-correction block for the higher order harmonics in real-time. Therefore, improvements in performance, in terms of SFDR could not be observed for all the cases and was only considered when either the second or the third harmonic was the dominant spurious tone in the frequency spectrum. Therefore, this post-correction block needs to be cross-validated with a state of the art ADC where the dominant harmonics range from third to seventh order.

The work has to be extended for the compensation of spurious tones caused by skew and bandwidth mismatches which were not treated in this work due to the shortage of time.

The temperature and ageing effects were not considered while characterizing the non-linearities. It would be interesting to explore the effects of temperature on the extra phase shift and the magnitude ratios.

The current validation has been tested for RF sampling. However for the ASIC implementation, the post-correction block has to be modified for a down converted sampling rate. Moreover, it is a critical work since efficient implementation could save a lot of area and power requirements.

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