A Scalable Bandwidth Mismatch Calibration Technique for Time-Interleaved ADCs

Yunsoo Park, *Student Member, IEEE*, Jintae Kim, *Member, IEEE*, and Chulwoo Kim, *Senior Member, IEEE*

***Abstract*—This paper presents a foreground calibration method for both a sampler and a track-and-hold (T/H) buffer bandwidth mismatch in highly time-interleaved analog-to-digital converters (TI-ADCs). The T/H buffer bandwidth mismatch stems from the length difference of interconnect lines between the buffer and the channel ADC, while the sampler bandwidth mismatch arises from the mismatch in a switch and a sampling capacitor. To address both mismatches along with other mismatches residing in TI-ADCs, this papers utilizes least-squares (LS) minimization technique in order to extract mismatch parameters while injecting a sinewave at two distinct frequencies. Programmable capacitor arrays (PCAs) are used to tune the bandwidth of sampler, and correcting buffer bandwidth mismatch is performed in digital-domain. The method presented here is scalable to arbitrary number of interleaved paths, and can easily be combined with existing calibration methods for gain, offset, and timing-skew mismatches. Numerical experiment via Monte-Carlo simulations demonstrates significant performance improvement in the spurious-free dynamic range (SFDR) from 38 dB to 75 dB for a 32-channel time-interleaved ADC model that includes all major mismatches.**

***Index Terms*—Analog-to-digital conversion, bandwidth mismatch, channel mismatch, time-interleaved analog-to-digital converters (TI-ADCs) calibration.**

I. Introduction

TIME-INTERLEAVED analog-to-digital converters (TI-ADCs) are widely used for designing extremely high-speed ADCs with sampling frequency beyond several GHz [1]. The performance of TI-ADC is primarily limited by mismatches in offset, gain, timing, and sampling bandwidth of parallel ADCs. Correcting these errors in TI-ADCs through calibration, therefore, has become commonplace to achieve desired linearity performance of the TI-ADCs. While there have been many research papers that propose various calibration algorithms and methods for gain, offset, and timing-skew mismatches in TI-ADCs [2], [3], correcting bandwidth mismatch in TI-ADCs has also been a popular topic of many research papers [4]–[8]. Just as the timing-skew mismatch, the sampling bandwidth mismatch degrades high-frequency linearity of ADC, leading to frequency-dependent SFDR degradation. Fig. 1 displays the survey of SFDR in TI-ADCs with sampling rate over 1-GHz that were recently published at ISSCC and VLSI [9]. The survey indicates that even when the timing-skew calibrations are utilized, the residual sampling bandwidth mismatch seems to limit the achievable SFDR below 50 dB for signal frequency over 3-GHz.

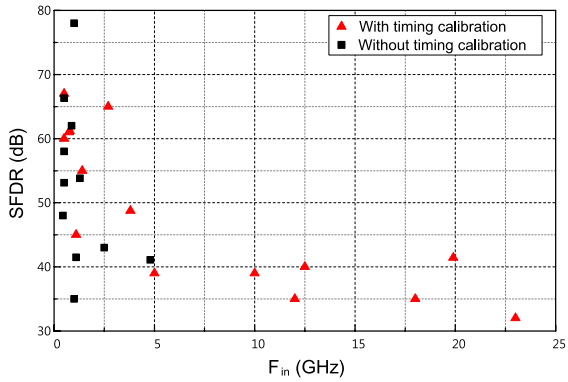

Fig. 1. Reported SFDR with input frequency of TI-ADC in ISSCC and VLSI from 2003 to 2015. Timing-skew calibrated TI-ADC is displayed with triangle shape.

Correcting sampling bandwidth mismatch poses a unique design challenge. Specifically, since both the timing-skew mismatch and sampling bandwidth mismatch impact the high-frequency linearity, it is not straightforward to distinguish these errors and make appropriate corrections. One notable difference, though, is that the phase error from the timing skew is linear with input frequency, and can be corrected by programmable delay line. In case of bandwidth mismatch, however, due to the non-linear relation between input frequency and phase, the phase error is not perfectly corrected by the programmable delay line [4]. To address these challenges, various calibration techniques for bandwidth mismatch have been proposed. In [5] and [6], the mismatch is detected by injected test signal and oversampling, respectively. Adaptive receive equalizer is used to correct all mismatches in [7]. In [8], a compensation algorithm is implemented with a number of fixed filters and few variable multipliers to reduce complexity and power. The limitation in [5] and [6] is that the technique has been demonstrated for only two channel TI-ADC. Also, note that the techniques used in [5]–[8] utilize digital-domain correction; while in theory digital-domain correction has greater flexibility, implementing very fine programmable phase response in digital filter requires enormous power and area even in advanced CMOS technology. For example, the timing-skew

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Y. Park and C. Kim are with the School of Electrical Engineering, Korea University, Seoul 136-701, South Korea (e-mail: ckim@korea.ac.kr).

J. Kim is with the Department of Electronics Engineering, Konkuk University, Seoul 143-701, South Korea (e-mail: jintkim@konkuk.ac.kr).

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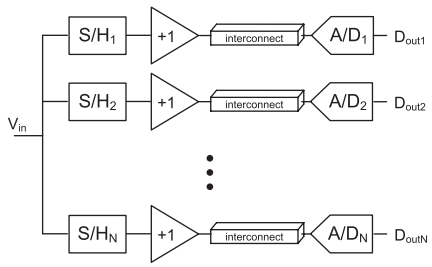

Fig. 2. Block diagram of time-interleaved analog-to-digital converter.

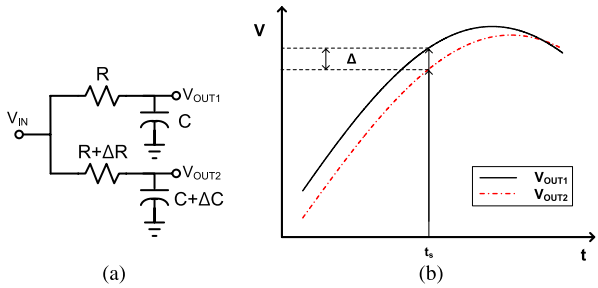

Fig. 3. (a) A two-channel T/H model with reference and mismatched channel. (b) Bandwidth mismatch error (Δ) in time domain.

calibration method in [3] reports that the digital circuit blocks for timing-skew calibration consumes significant amount of power while occupying even larger area than the ADC core, implying that the digital correction for timing-skew or phase mismatch may be power and area inefficient. On the contrary, [4] presented analog-domain correction technique. In this work, timing-skew and bandwidth mismatch are calibrated with reference ADC and analog differentiator. The challenge here is that the reference ADC limits the sampling speed of TI-ADC and the chopper is required to remove comparator offset.

In this paper, we present a mixed-signal two-tone calibration method to correct sampling bandwidth mismatch. The correction hardware is implemented in analog domain, but the calibration algorithm runs fully in digital domain. The proposed method is a foreground calibration that requires two-tone testing at two different frequencies, but it does not need any dedicated hardware for measuring mismatch between channels. The method is scalable to arbitrary number of TI-ADC channels and is compatible with a calibration method for other mismatches such as offset, gain and timing. In this paper, when demonstrating the bandwidth calibration method, we show that the calibration parameters for major mismatches—gain, offset, timing, and bandwidth—can be sequentially obtained to eventually address all major mismatch errors. The paper also covers static buffer bandwidth mismatch error from non-uniform routing between the buffer and the ADC in parallel channels. While the sampling bandwidth mismatch is improved with programmable capacitor arrays (PCAs) in analog domain, we show that the buffer bandwidth mismatch can be more easily corrected in digital domain.

Section II describes two types of bandwidth mismatch we consider. Section III presents proposed calibration method for N-channel TI-ADC. An analog correction method for sampler bandwidth mismatch is shown in Section IV. Section V provides various simulation results to verify the proposed algorithm with a TI-ADC model.

II. TI-ADC Bandwidth Mismatch Model

Fig. 2 illustrates a typical TI-ADC with N channels where each channel consists of a sample and hold (S/H), a unity-gain buffer and a channel ADC. In this arrangement, two bandwidth mismatch mechanisms can be identified. First, the S/H in each channel is nominally identical but suffers from random mismatches in on-resistance as well as sampling capacitance. We refer to this mismatch as *sampler mismatch*. Second, the interconnect lines between the buffer and sub-ADC tend to have non-uniform lengths, leading to systematic bandwidth mismatch at the buffer output. This mismatch is referred to as *buffer bandwidth mismatch*. Section II examines both of the mismatch mechanisms and analyzes key differences between them.

A. Sampler Bandwidth Mismatch

The S/H in Fig. 2 can be modeled as a switch with an on-resistance $R_{\rm on}$ and a sampling capacitor C_S during the sampling phase. The variance of sampler bandwidth $f_{\rm BW} = 1/(2\pi \cdot R_{\rm on}C_S)$ can be expressed using the area proportionality constant for threshold voltage ($A_{\rm VT}$) and beta (A_β) as

$$\left(\frac{\sigma_{f_{\rm BW}}}{f_{\rm BW}}\right)^2 = \left(\frac{\sigma_{R_{\rm on}}}{R_{\rm on}}\right)^2 + \left(\frac{\sigma_{C_S}}{C_S}\right)^2 = \frac{A_\beta^2}{W \cdot L} + \frac{A_{\rm VT}^2}{W \cdot L} \cdot \frac{1}{(V_{\rm gs} - V_{\rm th})^2} + \frac{\sigma_{C_S}^2}{C_S^2} \quad (1)$$

where W, L, β, $V_{\rm gs}$, and $V_{\rm th}$ are the width, length, beta, gate source voltage and threshold voltage of a switch, respectively [10]. Since the switch is typically implemented using MOS transistor, on-resistance in triode region ($R_{\rm on} = 1/\beta \cdot (V_{\rm gs} - V_{\rm th})$) is used for (1). While C_S is constrained primarily by the thermal noise consideration, (1) indicates that both the smaller channel length for higher bandwidth applications and the smaller overdrive voltage in advanced technology degrade the bandwidth mismatch of the sampler.

For further analysis, we regard a S/H in sampling mode as a single-pole network having a transfer function

$$H(jw) = \frac{A_0}{1 + j\frac{w}{w_b}} \quad (2)$$

where A_0 and w_b are DC-gain and bandwidth of the sampler [11]. The gain A and phase θ for specific input frequency $w_{\rm in}$ are then given by

$$A(w_{\rm in}, w_b) = \frac{A_0}{\sqrt{1 + (w_{\rm in}/w_b)^2}} \quad (3)$$

$$\theta(w_{\rm in}, w_b) = -\tan^{-1}\left(\frac{w_{\rm in}}{w_b}\right). \quad (4)$$

Fig. 3 illustrates the bandwidth mismatch error in time domain. For simplicity, we use a two-channel S/H model with capacitor mismatch ΔC and switch on-resistance mismatch ΔR as shown in Fig. 3(a). We also assume the same sampling time for the two channel for illustration purpose (in reality, the sampling clocks for these two samplers are separated by the inverse of total sampling frequency). With existence of

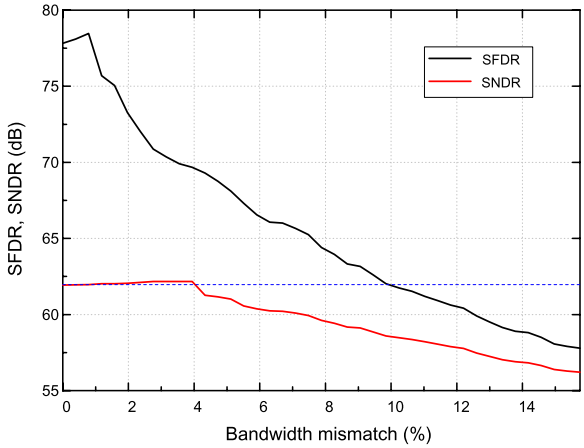

Fig. 4. SFDR and SNDR for sampler bandwidth mismatch in 2-channel TI-ADC. The bandwidth of the reference channel is eight times the Nyquist frequency. X-axis is percentage of bandwidth mismatch for Nyquist frequency. The dotted line presents SNDR for 10-bit accuaracy.

the bandwidth mismatch, the sampled output of channel with narrower bandwidth, which is V_{OUT2} in Fig. 3(b), exhibits smaller amplitude and phase lag when compared with the reference channel output V_{OUT1}. Mathematically, assuming $V_{\mathrm{in}} = A \cdot \cos(w_{\mathrm{in}} t)$, the combined error Δ from the phase and gain mismatches is expressed as

$$\begin{aligned}\Delta &= V_{\mathrm{OUT1}} - V_{\mathrm{OUT2}} \\ &\approx A_{\mathrm{ch1}} \cdot \Delta\theta \cdot \sin(w_{\mathrm{in}} + \theta_{\mathrm{ch1}}) - \Delta A \cdot \cos(w_{\mathrm{in}} + \theta_{\mathrm{ch1}}) \end{aligned} \quad (5)$$

where

$$\begin{aligned} V_{\mathrm{OUT1}} &= A_{\mathrm{ch1}} \cos(w_{\mathrm{in}} t + \theta_{\mathrm{ch1}}) \\ V_{\mathrm{OUT2}} &= A_{\mathrm{ch2}} \cos(w_{\mathrm{in}} t + \theta_{\mathrm{ch2}}) \\ &= (A_{\mathrm{ch1}} + \Delta A) \cos(w_{\mathrm{in}} t + \theta_{\mathrm{ch1}} + \Delta\theta) \\ \Delta A &= \frac{\partial A(w_{\mathrm{in}}, w_b)}{\partial w_b} \cdot \Delta w_b = \frac{1}{\sqrt{1+(w_{\mathrm{in}}/w_b)^2}^3} \cdot \frac{w_{\mathrm{in}}^2}{w_b^3} \cdot \Delta w_b \\ \Delta\theta &= \frac{\partial \theta(w_{\mathrm{in}}, w_b)}{\partial w_b} \cdot \Delta w_b = \frac{-1}{1+(w_{\mathrm{in}}/w_b)^2} \cdot \frac{w_{\mathrm{in}}}{w_b^2} \cdot \Delta w_b. \end{aligned}$$

The A_{ch} and θ_{ch} are gain and phase of each channel at input frequency, respectively.

For high-linearity TI-ADC design, the sampler bandwidth w_b is typically chosen to be at least 8 to 10 times higher than the maximum input frequency to allow enough settling time in tracking mode. In such a case, it has been previously shown that the first term related to phase difference $\Delta\theta$ in (5) becomes dominant error source [12].

To check the required bandwidth mismatch quantitatively, Fig. 4 shows a simulated SNDR and SFDR of a two-channel 10-bit TI-ADC while sweeping bandwidth mismatch for Nyquist input frequency. The simulation shows that the bandwidth mismatch has to be less than 4% to avoid excessive linearity degradation. Otherwise, a calibration method is required to compensate the raw mismatch of the samplers.

B. Buffer Bandwidth Mismatch

When TI-ADC is used with high number of interleaved channels (> 16), it is common to have different channel-to-channel pitch for S/H and A/D converter, which inevitably leads to non-uniform on-chip interconnect length between the buffer and channel ADC. For example, the die photograph in [13] shows that there is an approximately 760 μm difference between the longest and shortest interconnect between the buffer and channel ADC. Since the interconnect line in deeply scaled nanometer process has a characteristic of R-C dominant line [14], the discrepancy between the interconnect line length leads to buffer bandwidth mismatch.

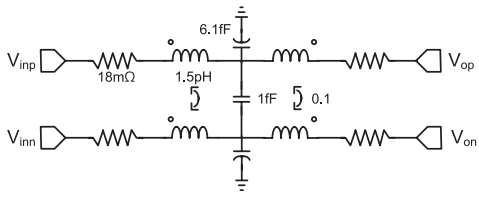

Fig. 5. 20μm RLGC model of interconnect line in 65-nm CMOS process.

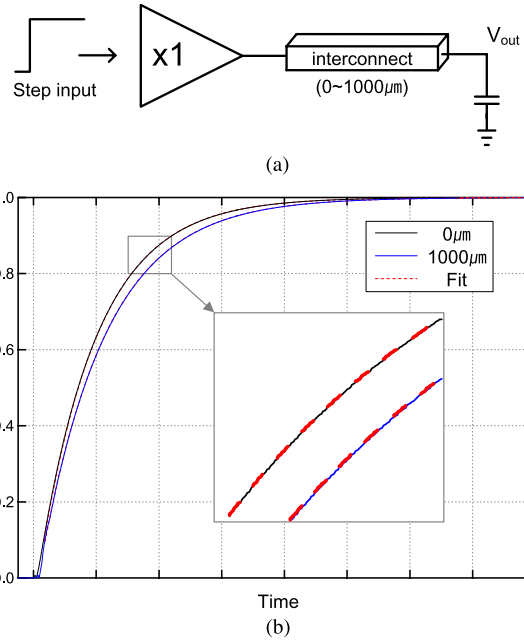

Fig. 6. (a) Simulation setup for interconnect. (b) Simulated waveform and fitting result with exponential function.

To numerically simulate the buffer bandwidth mismatch, we use an EM-extracted 20 μm RLGC line segment in 65 nm CMOS process as a unit element of the interconnect, and cascade them to implement actual interconnect line. Fig. 5 illustrates the schematic diagram of the unit element and interconnect line model. By using this model, a step response of open-loop unity-gain buffer in transistor level was simulated with an ADC load and on-chip interconnect while varying the line length from 0 to 1000 μm as depicted in Fig. 6(a). The resulting simulated waveform is numerically fitted to the first-order linear model with time constant τ for 0 μm and 1000 μm interconnect length in Fig. 6(b). The simulation results with other length are also fitted well and summarized in Table I. The data shows that the SPICE-simulated step response of a buffer with interconnect line can be reasonably well modeled as a first-order linear model with exponential settling behavior. Note that the time constant of the channel increases by about $4 \sim 5ps$

TABLE I
STEP RESPONSE FITTING RESULTS WITH INTERCONNECT MODEL

Length (mm)	0	0.2	0.4	0.6	0.8	1
$\tau\ (ps)$	185.3	189.9	194.5	199.2	203.8	208.5

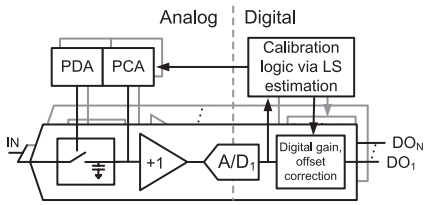

Fig. 7. System of proposed calibration algorithm for TI-ADC.

with every 200 μm increment. Therefore, for the same settling period, the ADC in each channel sees a slightly different input due to the difference in incomplete settling.

However, it is worth noting that there are two fundamental differences between the buffer bandwidth mismatch and the sampler bandwidth mismatch: First, the buffer bandwidth mismatch is static and deterministic since it stems from non-uniform interconnect length. Second, the buffer transfers a "held" voltage to the ADC input whereas S/H tracks fast-changing sinewave. Therefore, with appropriate reset before the S/H activation, the buffer bandwidth mismatch does not cause a frequency-dependent error. Rather, it leads to a frequency-independent DC gain error.

The buffer bandwidth mismatch has to be corrected for high-resolution TI-ADCs. Based on our buffer and interconnect model, a simulated step response achieves 0.216% gain error in a channel with 1-mm-long interconnect. On the other hand, the buffer settles with 0.1% gain error at the same time without the interconnect line. Since the ADC outputs are combined in TI-ADC, the difference in settling error leads to substantial linearity degradation. One may argue that if settling errors in all channels are small enough for the target linearity, the buffer bandwidth mismatch would not degrade the linearity of combined ADC output. However, reducing time constant of the buffer demands significant power overhead since the buffer is a power-hungry block in TI-ADC. Therefore, calibration to correct buffer bandwidth error is necessary to achieve both low-power and high linearity performance of TI-ADCs.

III. CALIBRATION ALGORITHM

A. System-level Overview

The calibration we present belongs to a foreground method, thereby requiring a known input sequence for the calibration. The system-level architecture is depicted in Fig. 7. Mismatch corrections are performed in both analog and digital domain. In analog domain, Programmable Delay Array (PDA) is used to adjust the clock path delay in each sampler, and the Programmable Capacitor Array (PCA) is added at the output of the sampler so that the output bandwidth can be changed in a programmable way. In digital domain, gain and offset between channels are corrected. The parameter extraction for calibration runs fully in digital using ADC output without using any extra circuits dedicated to calibration.

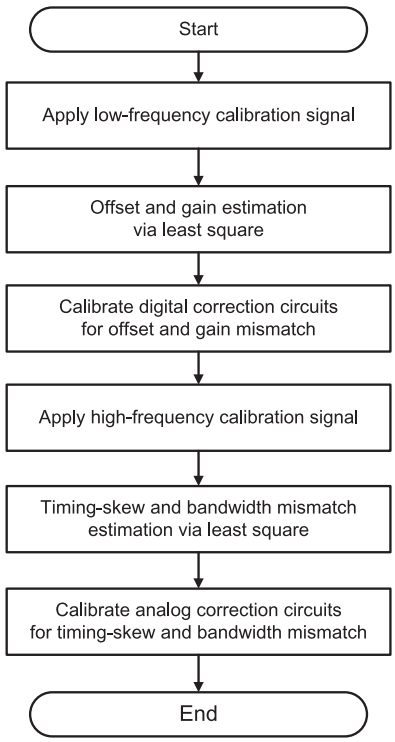

Fig. 8. Flow diagram of calibration for offset,gain,timing-skew and bandwidth mismatches.

The calibration flow diagram is illustrated in Fig. 8. In the proposed algorithm, a sinusoidal signal with known frequency is applied to TI-ADC to extract calibration parameters. The output of TI-ADC in each channel is fitted to ideal ADC output of the respective channel, and the optimal gain, offset, timing, and bandwidth mismatch between channels are estimated using the errors obtained from the fitting. Afterwards, obtained parameters are used to adjust the correction circuits in analog and digital domains [15]. Specifically, offset and gain mismatch are corrected with adders and multipliers in digital domain. The timing-skew mismatch is tuned by adjusting PDAs in the sampler clock path such a way that the sample time between each channel is as close to ideal as possible [16]. The bandwidth mismatch is calibrated by adjusting the extra capacitance arising from PCAs at the sampler output. We will further provide details of PCA implementation in Section IV.

B. Mathematical Model

To show the detailed mathematical formulation of the calibration algorithm, let us assume that output of each channel with sinusoidal input $y(wt)$ is expressed as the following:

$$g_i(w) \cdot y(wt + \theta_i(w)) + o_i = d_i \cdot r + e_q \tag{6}$$

where $g_i(w)$, $\theta_i(w)$, o_i, and d_i are gain, phase, offset, and digital output of ith channel at the input frequency, respectively. Also, e_q and r are the quantization error and scaling factor between ADC input and output (ideally, the scaling factor r is analog full scale/digital full scale). With a known input and digital output(d_i) record length of k, the g_i, θ_i, and o_i

of ith channel can be estimated optimally by a least-square minimization, i.e.,

$$\text{minimize} \sum_{n=1}^{k} \{a \cdot \cos(w_c t_s \cdot n) + b \cdot \sin(w_c t_s \cdot n) + o_i - d_i(n) \cdot r\}^2 \quad (7)$$

where

$$g_i|_{w=w_c} = \sqrt{a^2 + b^2}$$
$$\theta_i|_{w=w_c} = \tan^{-1}\left(\frac{b}{a}\right).$$

The w_c and t_s denotes frequency of calibration signal and sampling period of each sub-ADC.

Once formulated, the least-squares problem can easily be solved via efficient matrix operation. In this work, the algorithm is implemented using CVX optimization toolbox in MATLAB [17]. The formulation shown here is scalable in a straightforward manner, and therefore a TI-ADC with arbitrary number of channels can be calibrated by this algorithm. When using the algorithm, a few different input sequences can be used for different calibration purposes. For example, DC gain and offset mismatch can be found by applying a low-frequency sine input since they are mostly DC gain errors. Because the buffer bandwidth mismatch is also considered as DC gain mismatch, calibration and correction method for buffer bandwidth are identical to that of DC gain mismatch.

For the timing-skew calibration, it is typical to inject high-frequency signal to increase phase error due to phase mismatch, as demonstrated in [16]. In this work, we employ a two-tone calibration signal containing low-frequency for buffer bandwidth mismatch and high-frequency for timing-skew and sampling bandwidth mismatch. Note that the calibration algorithm shown here simultaneously can extract the calibration parameters for offset and gain mismatch of TI-ADC, but no gain and offset mismatches are assumed for simplicity.

C. Sampler Bandwidth Mismatch Calibration

The timing-skew and S/H mismatch of ith channel are measured from the phase ($\theta_i(w_c)$) and gain ($g_i(w_c)$) obtained by solving the problem formulated in (7) for a high-frequency (w_c) calibration signal. For the high-frequency calibration signal, we use near-Nyquist frequency of TI-ADC to fully exercise the bandwidth mismatch of S/H. The challenge here is that both of the mismatches produce phase error at high-frequency, so it is not straightforward to distinguish the error sources solely from the phase response. To address this challenge, we propose a two-step approach that sequentially estimates S/H bandwidth mismatch and timing-skew mismatch. First, to estimate S/H bandwidth mismatch, the gain variation in (3) is utilized. Specifically, the estimated bandwidth of a channel (w_b) is

$$w_b = \frac{w_c}{\sqrt{(\frac{1}{g_i(w_c)})^2 - 1}} \quad (8)$$

1: Inject high-frequency (f_{cal}) calibration signal
2: Solve the least-square problem in (7)
3: $\Delta\theta \leftarrow$ measured phase
4: $\Delta A \leftarrow$ measured gain
5: Bandwidth estimation (f_b) with f_{cal} and ΔA in (3)
6: Calculate phase from bandwidth ($\Delta\theta_{f_{BW}}$) in (4)
7: Extract timing-skew information $(\Delta\theta - \Delta\theta_{f_{BW}})/2\pi f_{cal}$
8: Calibrate circuits for timing-skew and bandwidth mismatch

Fig. 9. Pseudo code for the calibration algorithm.

where w_c is frequency of calibration signal. Then, timing skew is also obtained with measured phase and calculated phase from S/H bandwidth in (4). The phase from timing skew (θ_s) is

$$\theta_s = \theta_i - \theta_{f_{\mathrm{BW}}} = \theta_i(w_c) + \tan^{-1}\left(\frac{w_c}{w_b}\right). \quad (9)$$

Although the bandwidth of entire S/H is calibrated to match the S/H with the narrowest bandwidth, the linearity performance improvement is far more significant than the small bandwidth reduction. The sampling time difference between the channels is also set as close to the ideal sampling period of the whole TI ADC as possible by adjusting PDA. Fig. 9 shows the pseudo code for how to separate timing-skew and bandwidth mismatch error.

IV. Mismatch Correction

The buffer and sampler bandwidth mismatches are corrected in different manners. Given that the buffer bandwidth mismatch results in DC gain error, the error can be corrected by multiplying the inverse of the DC gain of respective channel. Such a correction can be more easily implemented in digital domain by using digital multiplier. In case of sampling bandwidth mismatch, correction in analog domain is preferred because of the complexity of implementing sub-sample phase delay in digital filter. For example, one approach reported in [4] realized sampling bandwidth tuning circuit with body biasing. In this approach, however, digital-to-analog converters (DACs) are needed for generating body bias voltage, adding significant design complexity given that each sampler will require individual DACs to accurately adjust the phase response of each sampler. As an alternative approach, this paper proposes a programmable capacitor arrays (PCAs) to adjust the sampling bandwidth mismatch.

A. Programmable Capacitor Array

The unit element of PCA for adjusting S/H bandwidth of each channel is shown in Fig. 10(a) and the PCA is connected to sampling node depicted in Fig. 10(b). We physically adjust the amount of sampling capacitance by selectively connecting the bottom-plate of the capacitor to either ground or the input node. This arrangement avoids floating during off-state capacitor, which prevents unwanted on-chip signal coupling through the floating node. The modified bandwidth by the PCAs can be expressed as following:

$$f_{\mathrm{BW}} = f_{\mathrm{BW0}} \cdot \frac{C_s}{C_s + C_{\mathrm{PCA}}} \quad (10)$$

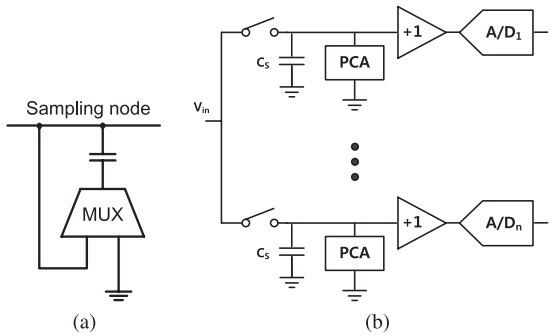

Fig. 10. (a) Unit block diagram of programmable capacitor array. (b) Connection with other circuit components. The unity-gain buffer drives a sub-ADC.

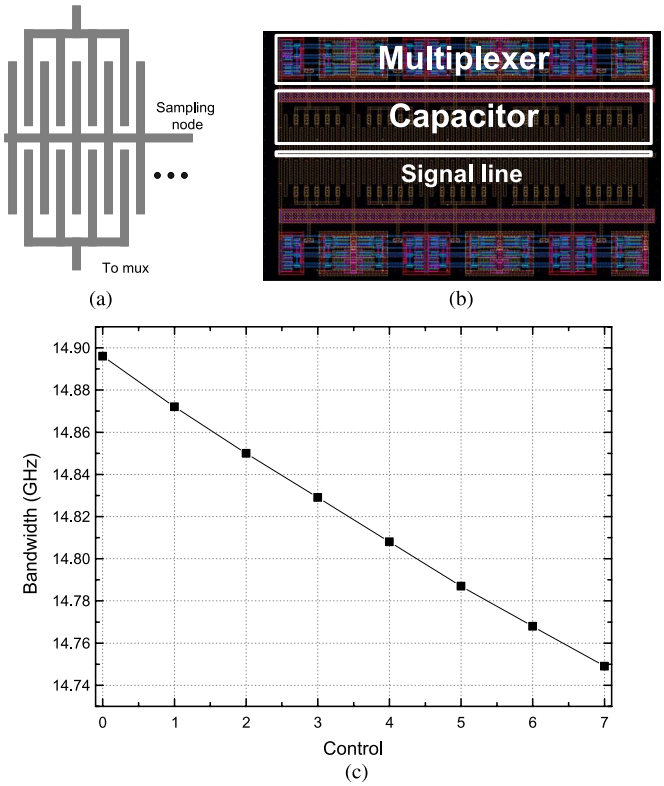

Fig. 11. (a) Capacitors used in the PCA. (b) Programmable capacitor arrays layout. (c) Simulated 3-dB bandwidth of PCA and S/H with control signal.

where f_{BW0}, f_{BW}, and C_{PCA} are original bandwidth, modified bandwidth and the extra capacitance from PCAs. Since we can only reduce the bandwidth of the S/H by adding more capacitance, the actual correction aligns the bandwidth of all channels to the lowest bandwidth of parallel channels. Although such a calibration reduces overall bandwidth of the ADC by a little bit, the correction improves linearity of the combined TI-ADC output dramatically. We have designed a 3-bit PCA using the error from bandwidth mismatch in (5) and 200 fF sampling capacitor are used where the required resolution of the PCAs is 1.6 fF. In order to achieve high resolution under 1 fF, capacitance between two metal is used as shown in Fig. 11(a) [18]. Fig. 11(b) shows layout of the PCA. Simulated PCA resolution when connected to actual S/H and buffer are shown in Fig. 11(c). The simulation shows that fine 3-dB bandwidth adjustment with resolution of roughly 20 MHz is realizable.

TABLE II
MISMATCH SETTING FOR SIMULATION

Model parameters	Value
Sampling rate	12.8 GS/s
Number of channels	32
ADC resolution	10 bit
Input range	0.4 Vpp
PDA resolution	15 fs
PCA resolution	1.6 fF
Mismatch parameters	Mean (Std.)
Sampling bandwidth	51.2 GHz (10%)
Buffer bandwidth	2 GHz (1%)
Offset	0 V (10LSB)
Gain	1 (1%)
Timing skew	[0, 3ps] (Uniform dist.)

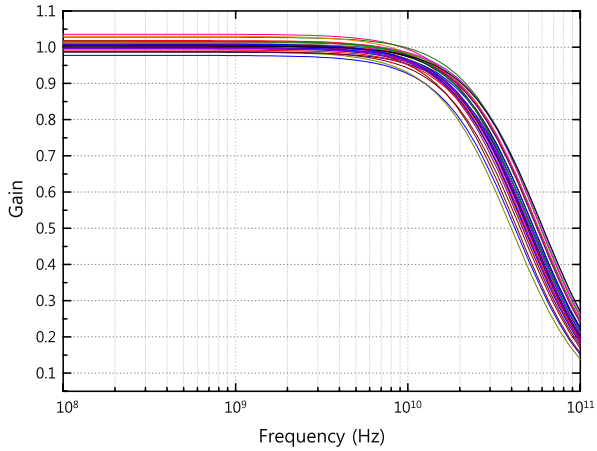

Fig. 12. Overlay 32 frequency response of S/H that shows slight bandwidth and gain mismatch.

V. SIMULATION RESULTS

To verify the algorithm, TI-ADC model described in Table II was implemented and simulated by the behavioral time-domain simulation package CppSim [19]. Table II shows mismatch parameters included in the model. The transfer function of simulated channels is plotted in Fig. 12. In CppSim model, we included digitally controlled delay with 15-fs resolution for timing-skew mismatch correction, and PCA with 1-fF resolution for S/H bandwidth mismatch correction. The digital-domain calibration for gain and offset mismatch correction is implemented in MATLAB. Two-tone calibration signal with 34-MHz and 6.2-GHz sine wave are injected in all the simulations in below, and we find calibration parameters for all mismatches we mentioned- gain, offset, timing, buffer bandwidth, and sampling bandwidth-, and make appropriate corrections.

In order to verify the performance of calibration algorithm, a 6.22-GHz sine input is applied, and exemplary FFT spectrums for calibrated and uncalibrated output are shown in Fig. 13. Although timing-skew and bandwidth mismatch are estimated simultaneously, FFT results are separated in Fig. 13(c) and (d) to prove effectiveness of bandwidth calibration. It is evident that SFDR and SNDR of TI-ADC output with calibration

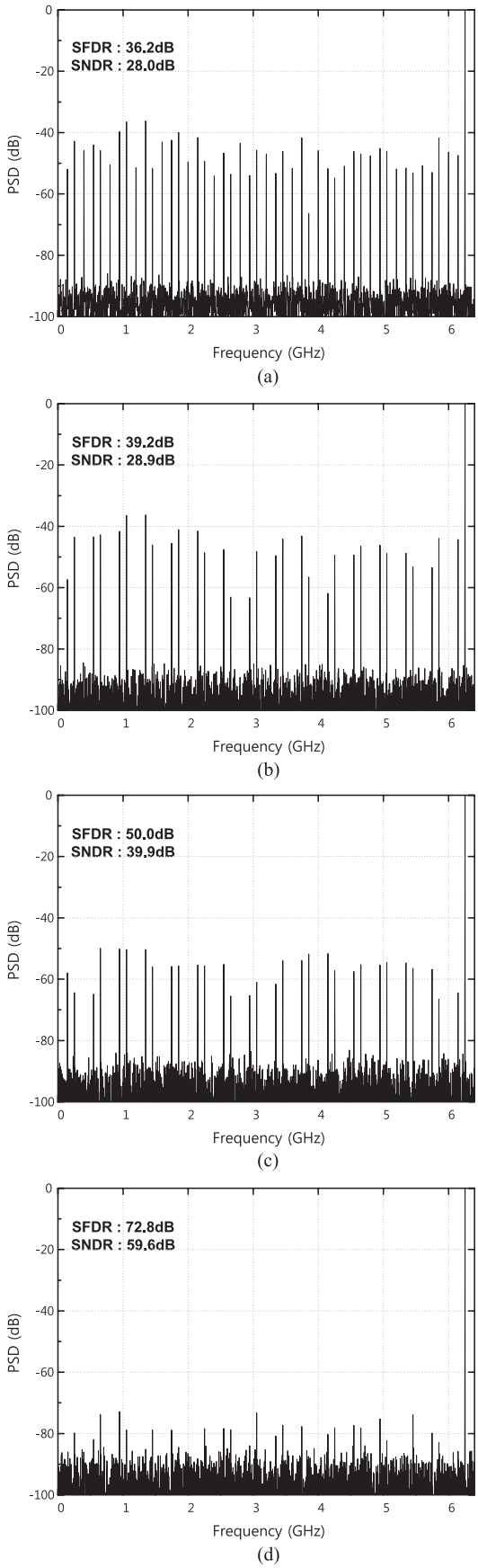

Fig. 13. Fast-Fourier Transform result of uncalibrated and calabrated TI-ADC. (a) Uncalibrated result. (b) Offset and gain calibrated result. (c) Timing-skew calibrated. (d) Bandwidth calibrated spectrum.

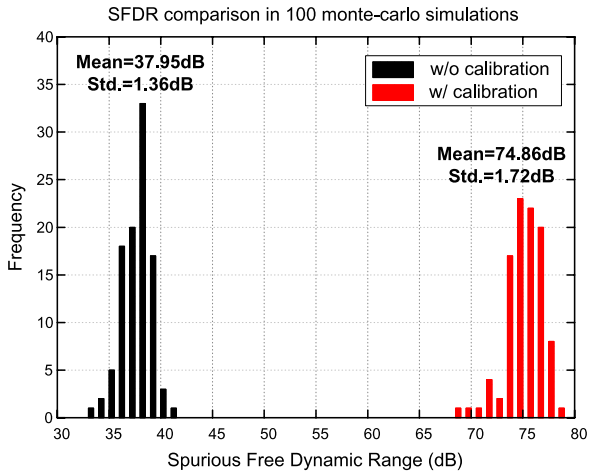

Fig. 14. 100 Monte-Carlo simulations for proposed calibration with simulation condition in Table II.

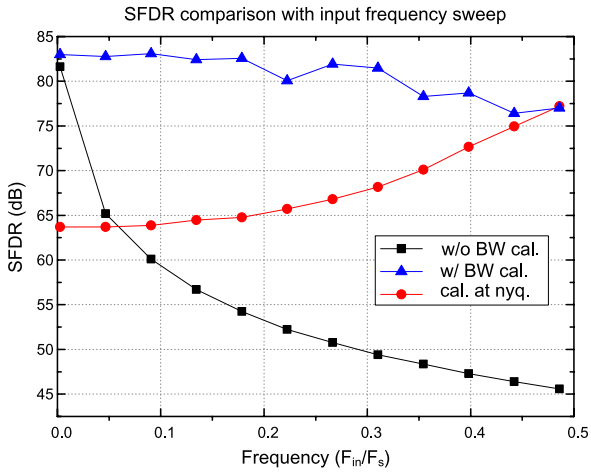

Fig. 15. Spurious-Free Dynamic Range versus the input frequency for before/after calibration and gain and timing-skew calibration at Nyquist frequency. Only sampling bandwdith mismatch is included in the simulation.

improves significantly by about 36.6 dB and 31.6 dB, respectively. To verify the robustness of our approach, we performed 100 Monte-Carlo simulations and applied the proposed calibration method. The SFDR histogram of raw and corrected TI-ADC output is shown in Fig. 14. The calibrated TI-ADC shows on average 74.86-dB SFDR with 1.72 dB standard deviation while the uncalibrated TI-ADC exhibits 37.95 dB with 1.36-dB standard deviation.

Also, to specifically prove validity of the performance improvement for wide range input frequency, SFDR of ADC output is plotted with frequency sweep in Fig. 15. In the graph, we show SFDR performance of three cases: 1) uncalibrated (black square), 2) with calibration for gain, offset, and timing skew (red circle), 3) with calibration for gain, offset, timing skew, and bandwidth (blue triangle). It is noteworthy that the calibrated performance of case 2) and 3) are roughly the same at near Nyquist frequency. This makes sense because at the frequency of injected calibration signal, the phase mismatch can be completely corrected only by timing-skew calibration; therefore, adding additional bandwidth calibration does not further improve the linearity performance. However, timing mismatch

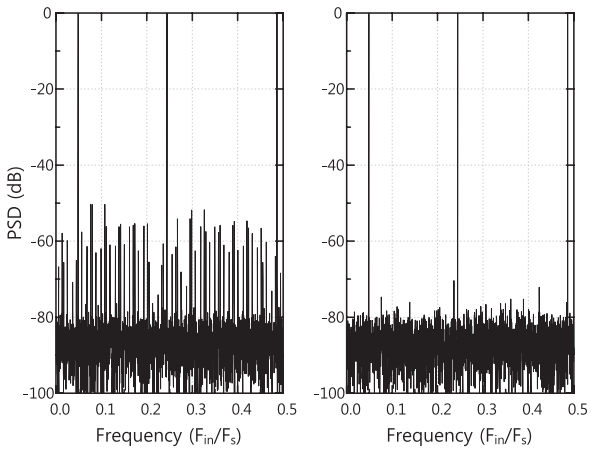

Fig. 16. ADC output power spectrum with multi tone input. (a) Result with bandwidth mismatch. (b) Calibrated result.

TABLE III
COMPARISON WITH OTHER BANDWIDTH MISMATCH CALIBRATION METHODS

	This work	[4]	[5]	[6]
Timing skew extraction	Digital	Both	-	-
Timing skew correction	Analog	Analog	-	-
S/H bandwidth extraction	Digital	Both	Digital	Digital
S/H bandwidth correction	Analog	Analog	Digital	Digital
Background calibration?	No	Yes	Yes	Yes
Dedicated hardware for mismatch estimation	No	Yes	No	No
Scalability	Yes	Limited	No	No

cannot correct the sampler bandwidth mismatch when the signal frequency differs from the calibration signal frequency, which is shown as SFDR degradation of case 2) when the signal frequency moves farther away from the calibration frequency. On the other hand, case 3) shows relatively flat SFDR performance over the entire frequency range, demonstrating that high SFDR performance is achievable over broad input frequency range with the adoption of sampler bandwidth mismatch calibration. ADC output spectrum with multi-tone signal in Fig. 16 also shows the validity for wide-band input. Table III compares our method with previously published bandwidth calibration methods. While our method is not a background technique, it can be more practically utilized given that our method does not need any extra hardware for mismatch estimation. Also, the straightforward scalability to any number of interleaved channels makes our method favorable to highly-interleaved ADC designs.

A. Discussions

Several issues of the proposed calibration algorithm are discussed in this subsection. The foreground calibration method uses two-tone signal as a calibration signal. In order to generate the signal, high-quality DAC is required, which might increase the system cost. Also, the initial training time is needed for foreground calibration. In consequence, this algorithm is suitable for high-end products such as measurement instruments where generating the two-tone signal does not add excessive cost to the overall system. Note that the proposed method does not operate in real time, so the calibration can be implemented in software on embedded processor of the high-end applications without additional hardware.

In some TI-SAR ADCs, an analog input is directly sampled at the capacitor digital-to-analog converter (DAC) of SAR ADC rather than front-end T/H sampler [20]–[22]. In this case, extra capacitor added to adjust bandwidth calibration would change the gain of each channel. This can be addressed by per-channel gain correction in digital domain. As the gain correction in digital domain has no effects on sampling bandwidth, both errors can be simultaneously corrected.

Complexity of the calibration algorithm and implementation is also an important issue. Two aspects of calibration should be considered separately; 1) estimating the calibration parameter and 2) correcting the bandwidth mismatch error. In a typical situation, high-performance TI-ADC is used as a part of high-performance acquisition system such as high-end instrument and radar system. Therefore, it is reasonable to assume that a microprocessor-based embedded processor is available, and we can write a software to estimate the calibration parameter on this processor. Under this scenario, there is no need for a dedicated hardware to extract calibration parameters. This is allowable because the presented calibration method is foreground, hence the calibration parameters do not need to be updated real-time.

To give an estimate of the required algorithm complexity, the calibration code that finds calibration parameters is written in MATLAB, which solves the least square problem using about 1000 output samples per channel. Running the calibration code takes 0.05 s for a single channel ADC in a PC which runs on Intel E3-1245 v3 processor with 32 G memory.

Regarding the correction of the mismatch error, the correction circuit needs to be implemented on-chip, but consumes no extra current during the normal operation. Although PCA adds load capacitor to input driver of TI-ADC, the extra load reduces bandwidth rather than increasing power consumption. Area of a unit correction circuit in Fig. 11(b) is 24 μm^2 in a 65-nm CMOS technology. If 200 fF sampling capacitor with 10% bandwidth mismatch is used, about 40 fF additional capacitance is needed to cover 1σ. Then, the correction circuits occupy $24\ \mu\text{m} \times 40\ \mu\text{m}$ in each channel where area of 200 fF capacitor is 250 μm^2. Note that the area can be further reduced by stacking more metal layers for higher capacitance density in the PCAs.

VI. CONCLUSION

A foreground calibration using two-tone calibration signal for sampler and buffer bandwidth mismatch is presented in this paper. The method in this paper extracts the bandwidth mismatch information using two-tone injection by solving least-squares minimization problem. The mismatch correction for the sampler and buffer bandwidth mismatch occurs in analog and digital domains, respectively. The sampler bandwidth correction requires fine bandwidth adjustment in analog domain, so the programmable capacitor array has been proposed to achieve sub-1fF resolution. The behavioral simulation using CppSim

verifies the validity of presented calibration method, indicating that the timing-skew calibration alone is not sufficient and the bandwidth calibration should be adopted to improve SFDR of the TI-ADC successfully over wide-frequency range.

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Yunsoo Park (S'14) received the B.S. degree in electrical engineering from Korea University, Seoul, South Korea, in 2014, where he is currently pursuing an integrated M.S. and Ph.D. degree in the area of integrated circuits and systems.

His research interests include time-interleaved ADC calibration and high-speed ADC designs.

Jintae Kim (S'02–M'08) received the B.S. degree in electrical engineering from Seoul National University, Seoul, South Korea, in 1997, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Los Angeles, CA, USA, in 2004 and 2008, respectively.

He held various industry positions at Barcelona Design, CA, SiTime Corporation, CA, and Agilent Technologies, CA, as a key technical contributor for their high-speed A/D converters and timing IC products. Since 2012, he has been an Assistant Professor at Konkuk University, Seoul, where he is focusing on low-power mixed-signal IC designs for communication and sensor applications.

Dr. Kim was a recipient of the IEEE Solid-State Circuits Predoctoral Fellowship in 2007.

Chulwoo Kim (S'98–M'02–SM'06) received the B.S. and M.S. degrees in electronics engineering from the Korea University, Seoul, South Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, in 2001.

In 1999, he was a summer intern in design technology at Intel Corporation, Santa Clara, CA. In May 2001, he joined IBM Microelectronics Division, Austin, TX, where he was involved in cell processor design. Since September 2002, he has been with the School of Electrical Engineering, Korea University, where he is currently a Professor. He was a Visiting Professor at the University of California at Los Angeles in 2008 and at the University of California at Santa Cruz in 2012. He is co-author of two books, CMOS Digital Integrated Circuits: Analysis and Design (New York: McGraw Hill, 2014) and High-Bandwidth Memory Interface (New York: Springer, 2013). His current research interests are in the areas of wireline transceiver, memory, power management and data converters.

Dr. Kim received the Samsung HumanTech Thesis Contest Bronze Award (1996), the ISLPED Low-Power Design Contest Award (2001, 2014), the DAC Student Design Contest Award (2002), SRC Inventor Recognition Awards (2002), the Young Scientist Award from the Ministry of Science and Technology of Korea (2003), the Seoktop Award for excellence in teaching (2006, 2011), the ASP-DAC Best Design Award (2008) and Special Feature Award (2014), and the Korea Semiconductor Design Contest: Ministry of Trade, Industry\Energy Award (2013). He served on the Technical Program Committee of the IEEE International Solid-State Circuits Conference and as a Guest Editor for the *IEEE Journal of Solid-State Circuits*. He is currently on the Editorial Board of IEEE TRANSACTIONS ON VERY LARGE-SCALE (VLSI) SYSTEMS and has been elected as Distinguished Lecturer of the IEEE Solid-State Circuits Society for 2015–2016.