Background Offset and Gain Calibration for Time-Interleaved ADC Using Digital Sinusoidal Calibration Signal

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This paper presents background offset and gain calibration for time-interleaved analog-to-digital converter (TIADC). The calibration technique depends on detecting the offset and the amplitude of a calibration signal. The detection is based on a simple algorithm performed in the digital part. A digital sinusoidal wave is needed to implement the calibration technique. The calibration technique behaviors are theoretically analysed and verified by simulations. A 12-bit, 4-channel, 800 MS/s TIADC is used as an example.

I. Introduction

Modern communication systems applications emphasize the need for faster, higher resolution, analog-to-digital converters (ADCs) than those commercially available. These applications do not only require faster ADC but also need large dynamic range and low distortion. Speed and resolution requirements became hard to achieve with a single ADC, so an array of M ADC is used. The time-interleaved ADC (TIADC) aims to get high speed converter using low speed ADC [1]. TIADC consists of M parallel ADCs channels. The channels operate with the same sampling frequency f_{clk} with M uniformly spaced phases as shown in Fig 1. The whole system sampling frequency f_s equals $M f_{clk}$. Mismatches between the different channels, result in a significant performance degradation of the TIADC. The signal-to-noise and distortion ratio (SNDR), i.e the effective number of bits ENOB, as well as the spurious-free dynamic range (SFDR) are the most affected performance aspects. Four different types of mismatches can appear in the TIADC; offset mismatch, gain mismatch, time skew mismatch and bandwidth mismatch [2]. In this paper, we focus on the offset and gain mismatches in the TIADC and we assume that the other types of mismatches are corrected. The paper is organised as follows: Section II discusses the effects of offset and gain mismatch, the proposed technique is developed in section III; whereas simulation results are presented in section IV. Section V concludes the paper.

II. Offset and Gain Mismatches

In order to illustrate the effects of offset and gain mismatch, a case study of a 12-bit, 4-channel, 800 MS/s TIADC is presented.

The offset mismatch, as shown in Fig 1, can be modelled as different DC offset voltages Voff_i - where i is an integer from 1 to M - added to each channel. The DC offsets have white Gaussian distribution with zero mean and standard deviation σ_{offset}. For a DC input signal, each channel will generate a different code because of these offset voltages. The offset mismatch produces spurious tones at $\frac{kf_s}{M}$, where k in an integer from 1 to M. We can see in Fig 2(a), the effect of the offset mismatch on the TIADC. These tones highly degrades the SFDR of the TIADC down to 61 dB.

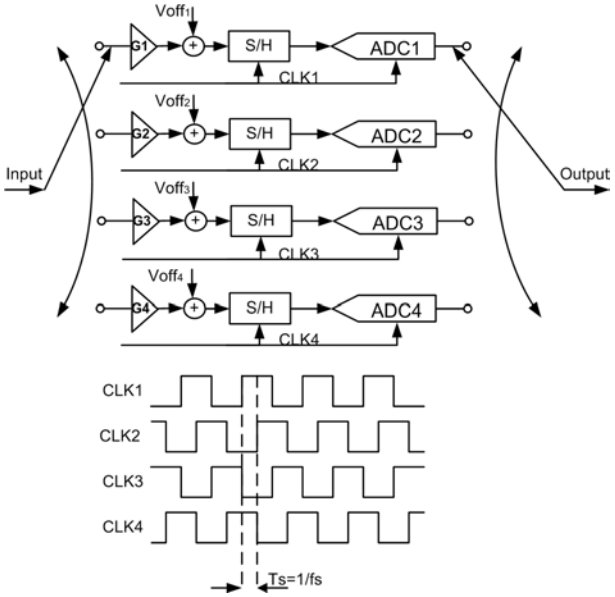


Fig. 1. Four channels time interleaved ADC

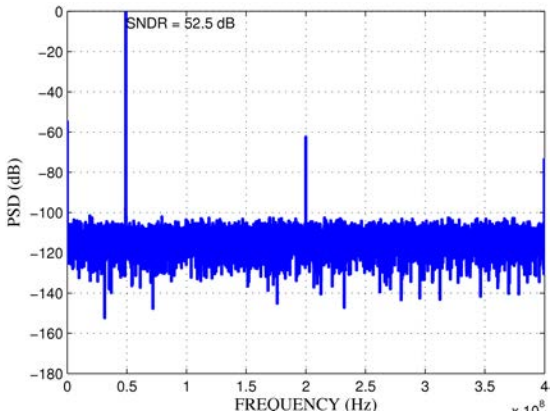
The gain mismatch is modelled as different gains G_i for each channel of the TIADC. These G_i are modelled as white Gaussian distribution with a mean equal to one and with a standard deviation σ_{gain}. The gain mismatch appears in the time domain as an amplitude modulation (AM) [2]. New spurious tones appear in the spectrum at $\frac{kf_s}{M} \pm f_{in}$ where f_{in} is the input signal frequency. These spurious tones degrade the SNDR of the TIADC down to 45.5 dB. As shown in Fig 2(b), the corresponding ENOB becomes 7.3 bit. The ENOB degradation caused by the offset and gain mismatch is independent of the input signal frequency.

Calibration techniques are necessary in order to maintain the

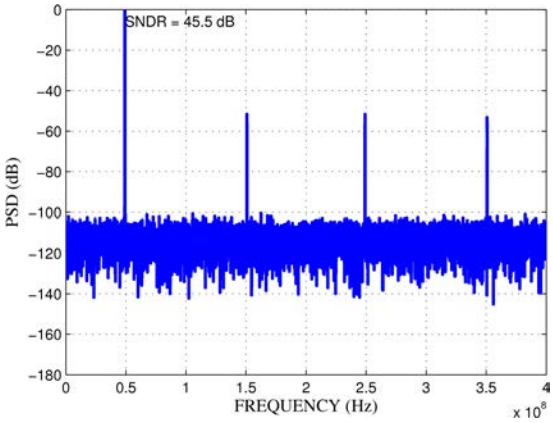
TIADC performances. There are two modes of calibration: the foreground mode and the background mode. The foreground mode is characterized by its simplicity because the calibration is performed when the ADC is offline. However it does not account for the temperature and supply variations. On the other hand, the background mode is more complex as the calibration is performed when the ADC is online. However it ensures better correction than the foreground mode. In previous publications, offset mismatch is corrected using random sampling method to increase the SFDR of the TIADC [3]–[5]. In this technique, extra ADCs are used to spread the power of the spurious tones in the bandwidth to improve the SFDR. The improvement of the SFDR depends on the number of extra ADCs but the SNDR is not improved. In [6], 2-channel TIADC was used. A random chopper-based is used to overcome the offset mismatch. the input signal is converted to white signal which allows the detection of the DC offset. On the other hand, the gain mismatch is corrected by correlation-based algorithms between the input signal and gain spurious tone. The drawback of this technique is the conversion rate that depends on the input signal. Also, The complexity of the notch filter used increases with number of ADCs used in the system. Our proposed offset and gain calibration technique is based on a simple algorithm, performed in background mode. The algorithm is presented in the following section.

III. Proposed Offset and Gain Calibration Techniques

Our proposed calibration technique is presented in Fig 3. An additional reference ADC (ADC_{ref}) is used as suggested in [7], [8]. ADC_{ref} operates with clock frequency CLK_{ref} equal to $\frac{f_s}{M+1}$, where M is the number of channels used in the TIADC. Therefore, the CLK_{ref} cycles are in phase with the other clocks as shown in Fig 4. Thus, the ADC_{ref} can replace the ADC under test ADC_{iUT} to convert the input signal. A sine wave calibration signal with frequency equal to f_{cal} is generated digitally and injected to the ADC_{iUT}. The generation of the calibration signal is performed using a Look-up table (LUT) and a digital-to-analog converter DAC as shown in Fig 5 and Fig 6. Digital algorithm is applied on the calibration signal at the output of the ADC_{iUT} to detect and correct the offset and gain mismatches errors.



(a) Effect of the offset mismatch on the output signal spectrum. ($\sigma_{\text{offset}} = 1mV$)



(b) Effect of the gain mismatch on the output signal spectrum. ($\sigma_{\text{gain}} = 0.005$)

Fig. 2. 12-bit, 4-channel, 800 MS/s time-interleaved ADC suffering from offset and gain mismatches

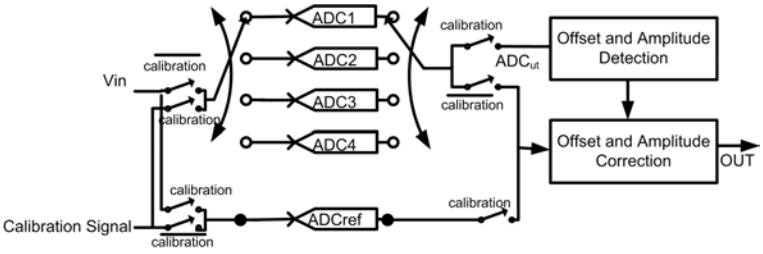


Fig. 3. Proposed background calibration technique using 4-channel time-interleaved ADC

A. Offset Calibration Technique

As mentioned earlier, the offset mismatch introduces different DC offset Voff_{i} in each channel. Voff_{i} is added to the digital output of the calibration signal for each ADC_{iUT}. From the equations below (Eq 1-Eq 3) , X_{lut} is the digital sinusoidal signal stored in the LUT. This digital signal is converted to analog by the DAC and injected to the ADC_{iUT}. The DC offset can be detected by averaging the ADC_{iUT} output during a known multiple of the calibration signal period. An accumulator is used for averaging the digital output of the calibration signal as shown in Fig 5.

$$\text{X}_{\text{lut}} = \sin(2\pi f_{cal}(t + (i-1)T_s)) \quad (1)$$

$$\text{ADC}_{\text{iUT}} = \text{Voff}_{\text{i}} + \text{G}_{\text{i}}\sin((2\pi f_{cal}(t + (i-1)T_s)) \quad (2)$$

$$\text{avg}(\text{ADC}_{\text{iUT}}) = \text{Voff}_{\text{i}} \quad (3)$$

The correction is done simply by subtracting the calculated offset Voff_{i} from ADC_{i} output. The offset of ADC_{ref} must be also calibrated.

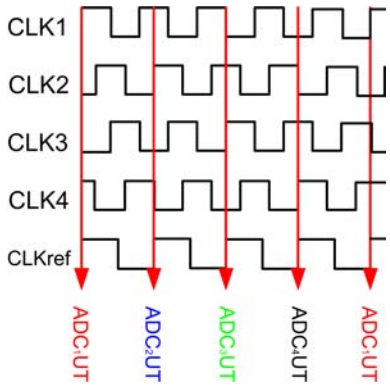


Fig. 4. Calibration sequence for the 4 ADCs in the system

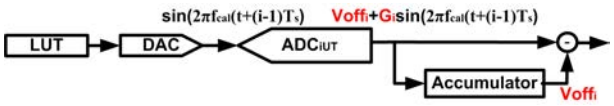


Fig. 5. The offset calibration technique for one ADC under test

B. Gain Calibration Technique

As shown in Fig 5, the output of the calibration signal from each ADC_{iUT} is multiplied by a gain G_i. This gain can be detected by calculating the amplitude of the ADC_{iUT} output. The used algorithm is illustrated in the following equations (Eq 4-Eq 9). The algorithm uses the sine and cosine digital signals stored in the LUT (X_{lut} & Y_{lut}). Fast Fourier Transform (FFT) is applied to the known calibration signal frequency f_{cal}.

$$ADC_{iUT}(t) = G_i \sin(2\pi f_{cal}(t + (i-1)Ts)) \quad (4)$$

$$X_{lut}(t) = \sin(2\pi f_{cal}(t + (i-1)Ts)) \quad (5)$$

$$Y_{lut}(t) = \cos(2\pi f_{cal}(t + (i-1)Ts)) \quad (6)$$

$$X = [\text{avg}(ADC_{iUT} \times X_{lut})]^2 \quad (7)$$

$$Y = [\text{avg}(ADC_{iUT} \times Y_{lut})]^2 \quad (8)$$

$$G_i = 2\sqrt{X+Y} \quad (9)$$

After detecting the gain G_i, ADC_i output is multiplied by $\frac{1}{G_i}$ to correct the gain mismatch as shown in Fig 6. The gain calibration technique can be performed in the presence of phase shift between the ADC output and the LUT. Also, there are no dependency between the gain and the offset techniques so they can be implemented in parallel.

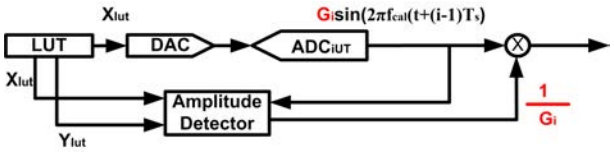


Fig. 6. The gain calibration technique for one ADC under test

IV. System Level Simulation Result

Simulink is used to model 12-bit, 4 ideal channels, 800 MS/s TIADC, shown in Fig 3. The sampling frequency of each ADC is 200 MHz and the clock frequency of the ADC_{ref} CLK_{ref} is 160 MHz. 4096 samples are used in the calibration algorithm to detect the offset $Voff_i$ and the gain G_i mismatches. The digitally generated calibration signal frequency f_{cal} is 60 MHz. The DAC is modelled to add some non-linearity (third harmonic distortion HD3) and thermal noise to the calibration signal, for which -50 dB and $1mV_{rms}$ are used respectively. Fig 7(a) shows the simulation results before applying the proposed technique. The input frequency f_{in} is selected to be 50 MHz. The power spectral density shows the spurious tones caused by the offset mismatch at 0, 200 MHz and 400 MHz. The spurious tones at 150 MHz, 250 MHz and 350 MHz are caused by the gain mismatch. The ENOB equals 7.1 bit and SFDR equals 62.6 dB. Fig 7(b) shows the simulation results after applying the offset calibration technique. The spurious tones caused by the offset mismatch are suppressed and the SFDR increases to 100dB. The gain calibration technique is further applied and ENOB increases to 11.6 bit as shown in Fig 7(c). The proposed technique has improved the TIADC performances using the calibration signal which is highly distorted by the DAC.

In Fig 8, a multiple-frequency input signal is injected instead of using single frequency input signal. In actual applications, the TIADC is used in multi-channel receiver to convert multiple-frequency input signal. In this test, equally spaced frequencies from 50 MHz to 390 MHz,i.e 132 different frequencies, are injected to the TIADC. Without calibration, these frequencies produce a lot of undesired spurious tones because of the offset and gain mismatches as shown in Fig 8(a). After applying the proposed calibration technique, the input frequencies are left alone, as shown in Fig 8(b), whereas the undesired spurious tones are totally suppressed.

V. Conclusion

An offset and gain background calibration technique has been proposed. The background mode is performed using a reference ADC that operates using a slower frequency. The calibration technique is based on applying digital algorithm on a digital sinusoidal calibration signal, injected to the ADC under test. The offset calibration depends on averaging the output of each ADC under test. The gain calibration depends on applying FFT to the output of the ADC under test. The calibration technique is tolerant to high distortion which simplifies the DAC implementation. The system simulation proves the efficiency of the proposed technique: a significant improvement has been demonstrated in both the ENOB and the SFDR performances of the TIADC.

VI. Acknowledgement

This project is funded by French Research Program NANO-2012 in cooperation with STMicroelectronics R&D Team, Grenoble.

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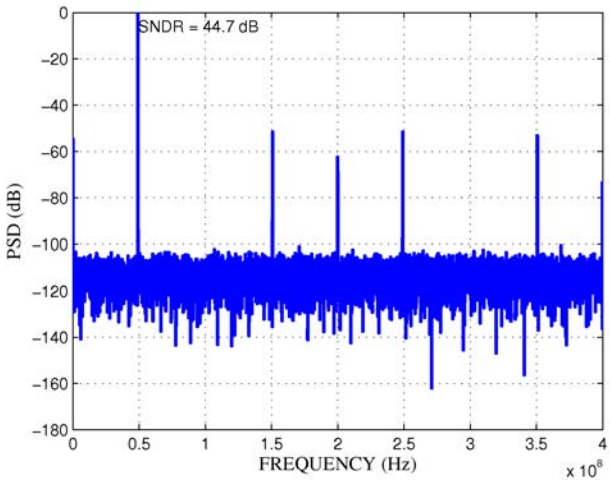
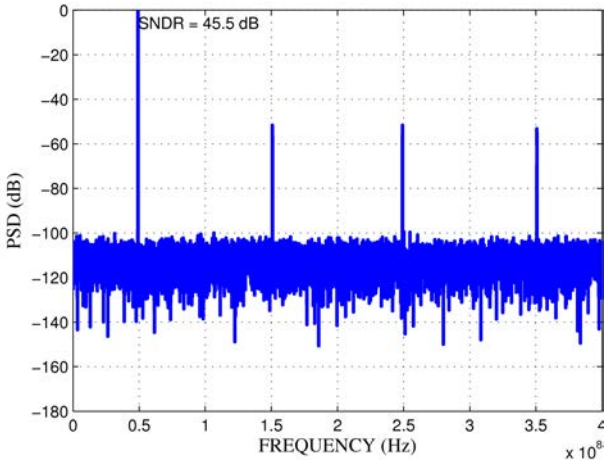
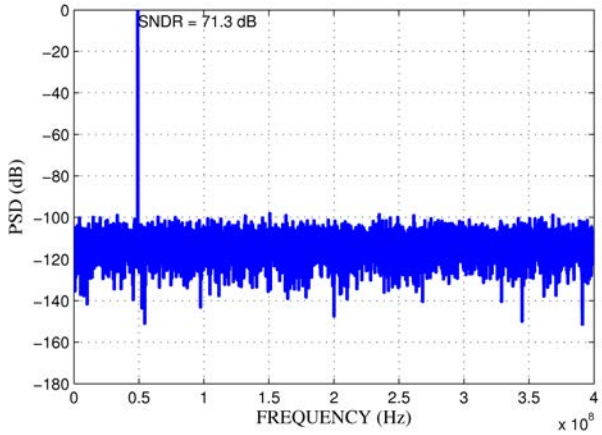


(a) Power spectral density of the output of the time-interleaved ADC before offset and gain calibration

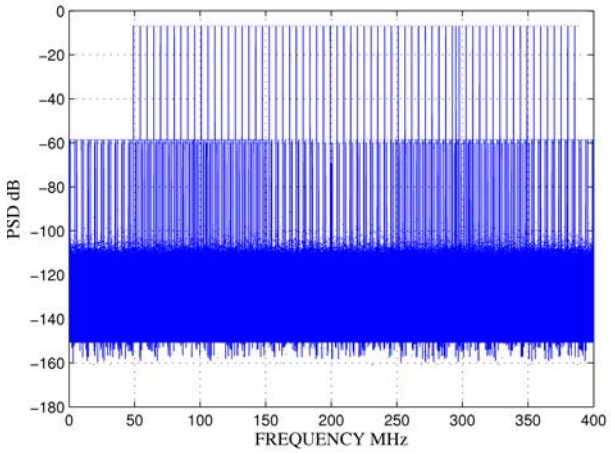


(b) Power spectral density of the output of the time-interleaved ADC after offset calibration

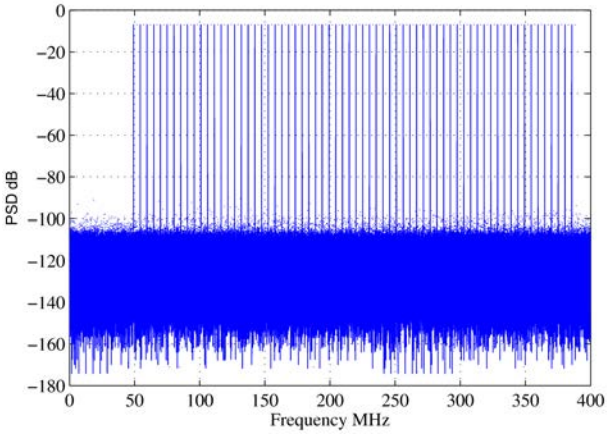


(c) Power spectral density of the output of the time-interleaved ADC after gain calibration

Fig. 7. 4-channel, 12-bit, 800 MS/s time-interleaved ADC calibration results



(a) The power spectral density of the output of the time-interleaved ADC before calibration.



(b) The Power spectral density of the output of the time-interleaved ADC after calibration.

Fig. 8. Multiple-frequency input signal injected to the time-interleaved ADC

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