AD9361 Register Map

GENERAL DESCRIPTION

The AD9361 Register Map contains a description of all of the user-programmable bits in the AD9361. When applicable, the map lists units, (such as dBFS) that the bits correspond to, the range of acceptable values, and the resolution of the value (such as 1dB/LSB).

In many cases, multiple bits or bytes work together to serve a particular function (e.g. those used to configure Automatic Gain Control and those used to configure the digital interface). This document describes each bit but more detailed functional setup and operation documentation may also be available.

Abbreviations

BBP = Baseband Processor

ENSM = Enable State Machine

REVISION HISTORY

7/2011—2.0 Release

7/2011—2.1 Updated 0x006 delay register description

8/2011—2.2 Corrected Immediate Update bit description in 0x07C[D6], corrected clock rate in 0x3F4[D3:D2] table

11/2011—2.3 Added text for AuxADC and Temp Sensor, clarified 0x230 & 0x270 [D0], added Tx and Rx BBF resampler and phase control bits, corrected Fast Lock register listing for table entry 0xD, added details for fast lock programming data format

1/2012—2.4 Clarified Tx Monitor Threshold in 0x06A, fixed 0x158 default, Correct Rx FIR gain settings, correct LNA gain setting table in 0x1B0, Correct Rx RF DC offset correction words in 0x074-0x181

2/2012—2.5 Fixed AuxADC clk rate equation, corrected symbol attenuation description, clarified TIA CC settings, removed unused TPM DC cal bit and configuration registers, minor formatting, clarified Tx 2nd filter CC and AmpBias settings, corrected operation of LVDS invert bits, corrected gain range of Rx quad cal words

8/2012—2.6 Updated TPM in 0x001, added register 0x200 to reduce confusion, changed 0x0F5[D4:D3] to say "rx", added reference to cal user guide for BBF tune dividers, corrected reference to 0x0D7[0], corrected Tx secondary filter resistance in 0x0D1, 0x106 applies to full and split modes, 0x114 applies to all gain control modes, 0x11A does not apply to MGC, 0128 description added, 0x109 works in all gain control modes, 0x130 clarified that it is not used to set current gain index, removed LNA and mixer gain examples to reduce confusion, corrected Gain Update Counter description, added comment for AuxADC divider = 0, Put 0x00B back into reg map to reduce confusion, corrected Rx Quad Cal exponent equations, added DCXO temperature compensation note.

3/2013 – 2.7 Updated 0x12D description.

4/2013—2.8 Corrected LMT threshold description; several minor corrections to peak overload text in 0x103; removed HB3 injection point for BIST; corrected resolution of power words in 0x161 & 0x163; fixed symbol gain resolution and descriptions; clarified BB DC tracking descriptions; removed cal time equation in 0x0A9 as this is already in the cal doc.

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GENERAL SETUP AND DIGITAL DATA PORT CONFIGURATION

CHIP LEVEL SETUP REGISTERS 000 THROUGH 007

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
000	*SPI Configuration*	Soft Reset	3-Wire SPI	LSB First	Open		LSB First	3-Wire SPI	Soft reset	00h	R/W
001	*Multi-Chip Sync and Tx Mon Control*	Open	Tx2 Monitor Enable	Tx1 Monitor Enable	Open	MCS RF Enable	MCS BBPLL enable	MCS Digital CLK Enable	MCS BB Enable	00h	R/W
002	*Tx Enable & Filter Control*	Tx channel Enable<1:0>		THB3 Enable & Interp<1:0>		THB2 Enable	THB1 Enable	Tx FIR Enable & Interpolation<1:0>		5Fh	R/W
003	*Rx Enable & Filter Control*	Rx channel Enable<1:0>		DEC3 Enable & Decimation<1:0>		RHB2 Enable	RHB1 Enable	Rx FIR Enable & Decimation<1:0>		5Fh	R/W
004	*Input Select*	0	TX Output	RX Input <5:0>						00h	R/W
005	*RFPLL Dividers*	TX VCO Divider<3:0>				RX VCO Divider<3:0>				00h	R/W
006	*Rx Clock & Data Delay*	DATA_CLK Delay<3:0>				Rx Data Delay <3:0>				00h	R/W
007	*Tx Clock & Data Delay*	FB_CLK Delay<3:0>				Tx Data Delay <3:0>				00h	R/W

There are many thousands of permutations of filter and divider settings, most of which are not valid operating modes.

SPI Register 0x000--SPI Configuration

This register is symmetrical (e.g., bit D7 is the same as bit D0). The AD9361 powers up with a default SPI operation of MSB first. If the BBP uses LSB first, the symmetrical register allows the BBP to write any or all of the three bits in register 0x000 without having to reverse the bit order in the SPI command. The symmetrical bits are ORed together so setting one bit sets both bits.

[D7] &[D0] Soft Reset When this bit is set, the device register values are asynchronously reset to their default states. All registers reset with the exception of 0x000, 0x009, and 0x00A, which retain their current values. The BBP must clear this bit before it can change any register value other than 0x000, 0x009, and 0x00A.

[D6] & [D1] 3-Wire SPI When clear SPI_DI pin is an input pin. When set, SPI_DI is bidirectional and SPI_DO is in a high impedance state.

[D5] & [D2] LSB First When clear, the SPI uses an MSB first format. When this bit is set, the SPI uses an LSB first format.

SPI Register 0x001—Multi-Chip Sync and Tx Monitor Control

[D6] Tx2 Monitor Enable This bit enables the Tx2 Mon pin but it also will shut down the normal receive path and the path will not power up even when the ENSM moves to the Rx state. To use transmit power monitoring, see register 0x057. If the "Always Enable Rx Data Port" bit (0x014[D7]) is also set, the signal at the Tx Mon 2 pin is sent as "I" and "Q" data to the Data Port.

[D5] Tx1 Monitor Enable Same as bit D6 but for the Tx Mon 1 pin.

[D3] MCS RF Enable Only used for multi-chip synchronization. Setting this bit keeps the RF LO dividers enabled in Alert mode so that the phase relationship between multiple devices remains constant. If the bit is clear, the dividers power down in Alert mode. If this bit is clear, the respective LO dividers also turn off in FDD Independent Mode when the Rx or Tx paths are disabled. Setting this bit prevents the LO dividers from turning off. This is important if the phase relationships must remain constant through enable & disable cycles.

[D2] MCS BBPLL Enable To synchronize the BBPLLs of multiple devices, write this bit high and then provide a sync pulse to SYNC_IN.

[D1] MCS Digital Clocks Enable To synchronize the digital clocks of multiple AD9361 devices, first synchronize the BBPLLs, then write this bit high and then provide a sync pulse to the SYNC_IN pins.

[D0] MCS BB Enable Setting this bit enables the capability of baseband multi-chip digital synchronization. See also bits D1 and D2.

SPI Register 0x002—Tx Enable & Filter Control

[D7:D6] Tx Channel Enable <1:0> These bits determine which of the two transmitters are enabled, with bit D6 corresponding to transmitter 1 and bit D7 corresponding to transmitter 2. Setting a bit enables a transmitter signal path. Clearing both bits disables both transmitters.

[D5:D4] THB3 Enable & Interpolation These bits set interpolation of the digital filter that feeds the DAC, per Table 1.

D5:D4	Interpolation Factor
00	Interpolate by 1, No Filtering
01	Interpolate by 2 (Half-Band Filter)
10	Interpolate by 3 & Filter
11	Invalid

Table 1. THB3 Interpolation Factor

[D3] THB2 Enable Setting this bit enables the interpolate-by-2 THB2 half band filter. Clearing this bit bypasses the filter.

[D2] THB1 Enable Setting this bit enables the interpolate-by-2 THB1 half band filter. Clearing this bit bypasses the filter.

[D1:D0] Tx FIR Enable and Interpolation These two bits control the programmable Tx FIR filter per Table ***2***.

D1:D0	Interpolation Factor
00	Interpolate by 1 and Bypass Filter
01	Interpolate by 1 and Enable Filter
10	Interpolate by 2 and Enable Filter
11	Interpolate by 4 and Enable Filter

Table 2. Tx FIR Interpolation and Filter Settings

SPI Register 0x003—Rx Enable and Filter Control

[D7:D6] Rx Channel Enable <1:0> These bits determine which of the two receivers are enabled, with bit D6 corresponding to receiver 1 and bit D7 corresponding to receiver 2. Setting a bit enables a receiver signal path. Clearing both bits disables both receivers.

[D5:D4] RHB3 Enable & Decimation These bits set the operation and decimation of the first filtering stage after the ADC per Table 3.

D5:D4	Decimation Factor
00	Decimate by 1, No Filtering
01	Decimate by 2 (Half-Band Filter)
10	Decimate by 3 & Filter
11	Invalid

Table 3. RHB3 Decimation Factor

[D3] RHB2 Enable Setting this bit enables the decimate-by-2 RHB2 half band filter. Clearing this bit bypasses the filter.

[D2] RHB1 Enable Setting this bit enables the decimate-by-2 RHB1 half band filter. Clearing this bit bypasses the filter.

[D1:D0] Rx FIR Enable and Decimation These two bits control the programmable Rx FIR filter per Table ***4***.

D1:D0	Decimation Factor and Filter Function
00	Decimate by 1 and Bypass Filter
01	Decimate by 1 and Enable Filter
10	Decimate by 2 and Enable Filter
11	Decimate by 4 and Enable Filter

Table 4. Rx FIR Decimation and Filter Settings

SPI Register 0x004—Input Select

[D7] Unused. Must be zero.

[D6] Tx Output Each transmitter signal path has two RF output ports, allowing different external components to connect to different outputs. Clearing this bit selects Tx1A for channel 1 and Tx2A for channel 2 while setting the bit selects Tx1B and Tx2B.

[D5:D0] Rx Input <5:0> Each receiver signal path has three internal LNAs from which to choose. In addition, the receivers can operate in balanced or unbalanced mode. The AD9361 configures both receiver signal paths the same way, with each of the six bits activating a particular input as shown in Figure 1.

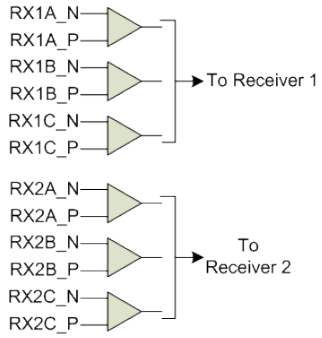

Figure 1. Receiver LNA Input Options

LNA inputs may not be mixed (RX1A_N cannot be combined with RX1C_P). Valid cases shown in Table 5. No other options are valid.

D5:D0	Enabled Rx Inputs
000001	RX1A_N and RX2A_N enabled; unbalanced
000010	RX1A_P and RX2A_P enabled; unbalanced
000100	RX1B_N and RX2B_N enabled; unbalanced
001000	RX1B_P and RX2B_P enabled; unbalanced
010000	RX1C_N and RX2C_N enabled; unbalanced
100000	RX1C_P and RX2C_P enabled; unbalanced
000011	(RX1A_N & RX1A_P) and (RX2A_N & RX2A_P) enabled; balanced
001100	(RX1B_N & RX1B_P) and (RX2B_N & RX2B_P) enabled; balanced
110000	(RX1C_N & RX1C_P) and (RX2C_N & RX2C_P) enabled; balanced

Table 5. Enabled Rx Inputs

SPI Register 0x005—RFPLL Dividers

[D7:D4] Tx VCO Divider <2:0> Only applies when using the internal Tx RF PLL/VCO. The VCO operating range is 6 GHz to 12 GHz. A divider after the VCO allows for a wide range of possible Tx Local Oscillator frequencies. The register value maps per Equation 1.

$$Divider\ Value = 2^{(Tx\ VCO\ Divier\ Register+1)}$$

Equation 1

The BBP must program this register correctly before the Tx LO frequency will be correct. Table 6 shows register vs. desired Tx LO.

For this Tx LO Frequency Range (MHz)	Divide by	Set TX VCO divider<2:0> to
3000~6000	2	0
1500~3000	4	1
750~1500	8	2
375~750	16	3
187.5~375	32	4
93.75~187.5	64	5
46.875~93.75	128	6
Up to 4GHz	Use External VCO. Tx LO = Ext VCO ÷2	7

Table 6. Tx VCO Divider

[D3:D0] Rx VCO Divider Same as bits D7:D4 but programs the Rx VCO Divider.

SPI Register 0x006—Rx Clock and Data Delay

These bits affect the DATA_CLK and the Rx Data delays. If the two nibbles are equal, then the data bits will approximately align with the DATA_CLK edge. The typical delay is approximately 0.3ns/LSB. Rx Frame Sync is delayed the same amount as the Data Port bits. Min delay setting is 0x0 and maximum delay is 0xF. Set this register so that the data from the AD9361 meets BBIC setup/hold specifications.

SPI Register 0x007—Tx Clock and Data Delay

Same as 0x006 but affects FB_CLK and the Tx Data bits. Tx Frame Sync is delayed the same amount as the Data Port bits. Set this register so that the data from the BBP meets the AD9361 setup/hold specifications.

CLOCK CONTROL REGISTERS 009 THROUGH 00A

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
009	*Clock Enable*	Open		Set to 0	XO Bypass	Set to 0	Digital Power Up	Set to 1	BBPLL Enable	10h	R/W
00A	*BBPLL*	CLKOUT Select<2:0>			CLKOUT Enable	DAC Clk div2	BBPLL Divider <2:0>			03h	RW

SPI Register 0x009—Clock Enable

[D4] XO Bypass This bit controls a MUX that selects between two different paths while also powering down the unselected path. Setting this bit high selects the XTALN path (and shuts down the DCXO and its buffers). Clearing the bit selects the XTALP path (and shuts down the XTALN buffers). Set the bit when using an external reference and clear it when using the DCXO. For the DCXO, an external crystal connects between the XTALP and XTALN pins, which feeds a trimming circuit. The output of the trimming circuit only uses the buffers in the XTALP path so the XTALN buffers can be powered down (by selecting XO bypass = 0).

[D2] Digital Power Up When clear, the AD9361 shuts down the digital logic clocks. The BBP may still write to the directly addressable SPI registers. When set, all digital clocks are operational. The AD9361 powers up with this bit clear and it is set during initialization.

[D0] BBPLL Enable Clearing this bit disables the BBPLL while setting it enables the BBPLL. The AD9361 powers up with this bit clear and it is set during initialization.

SPI Register 0x00A—BBPLL

[D7:D5] CLKOUT Select<2:0> These bits set the CLKOUT frequency per Table 7. Bit D4 must be set to enable this function.

CLKOUT Select<2:0>	CLKOUT Frequency
000	XTALN (or DCXO) (buffered)
001	ADC_CLK / 2
010	ADC_CLK / 3
011	ADC_CLK / 4
100	ADC_CLK / 8
101	ADC_CLK / 16
110	ADC_CLK / 32
111	ADC_CLK / 64

Table 7. CLKOUT Frequency

[D4] CLKOUT Enable Setting this bit enables a clock to be output on the CLKOUT ball. When clear, the AD9361 drives out logic zero.

[D3] DAC Clk Div2 When clear, the DAC clock rate equals the ADC clock rate. When set, the DAC clock equals ½ of the ADC rate.

[D2:D0] BBPLL Divider <2:0> The ADC clock rate equals the BBPLL divided by the factor in this register, shown in Equation 2.

$$ADC\ Clock\ Rate = \frac{BBPLL\ Clock\ Rate}{2^{BBPLL\ Divider<2:0>(decimal)}}$$

Equation 2

BBPLL Divider<2:0> is valid from 0 through 6 but a value of zero is only used as a special test mode.

TEMPERATURE SENSOR REGISTERS 00C THROUGH 00F

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
00B	*Offset*	Temp Sense Offset <7:0>								00h	R/W
00C	*Start Temp Reading*	Open							Start Temp Reading	0-h	R/W
00D	*Temp Sense2*	Measurement Time Interval<6:0>							Temp Sense Periodic Enable	03h	R/W
00E	*Temperature*	Temperature<7:0>								--h	R
00F	*Temp Sensor Config*	Open					Temp Sensor Decimation<2:0>			04h	R/W

AD9361 RSSI and DCXO functions can be temperature compensated if desired. RSSI temperature compensation can correct for the small temperature dependence of the algorithm if very high RSSI accuracy is required. Registers 0x00C through 0x00F are used with these functions. See registers 0x145 through 0x149 for more information. The temp sensor is internal to the AD9361 and as such the resulting temperature word is highly dependent on the operating mode (and thus power consumption) of the AD9361. To determine system temperature, it is highly recommended that one or more external temperature sensor(s) be used.

SPI Register 0x00B—Temp Sense Offset

See the Temperature register 0x00E.

SPI Register 0x00C—Temp Sense1

[D0] Start Temp Reading Set this bit to manually start a temperature reading. While the reading is in process, bit D1 is clear. When the reading is complete and a valid temperature value is in register 0x00E, bit D1 is set. Bit D0 is not self-clearing. To calculate the temperature again, this bit must be cleared and then set again. See also bit D0 of 0x00D.

SPI Register0x 00D—Temp Sense2

[D7:D1] Measurement Time Interval<6:0> Only applies if bit D0 is set, in which case the AD9361 takes temperature readings periodically at the rate per Equation 3. If bit D0 is clear, a measurement starts when the "Start Temp Reading" bit (0x00C[D0]) is set.

$$Calculation\ Time\ (s) = \frac{Measurement\ Time\ Interval < 6:0 > * \ 2^{29}}{BBPLL\ Clock\ Frequency\ (Hz)}$$

Equation 3

[D0] Temp Sense Periodic Enable See bits D7:D1.

SPI Register 0x00E—Temperature

Register 0x00E equals the measured temperature word of the device added to the temperature offset in 0x00B. 1 LSB/degree C. When reading the temperature, the AuxADC should be disabled by setting 0x01D[D0] to ensure a valid temperature reading.

SPI Register 0x00F—Temp Sensor Config

[D2:D0] Temp Sensor Decimation Decimation of the AuxADC used to derive the temperature per Equation 4. The AD9361 uses the sigma delta AuxADC to perform the temperature measurement. The AuxADC clock rate is always the BBPLL rate divided by 64 when using the temperature sensor.

$$Temp\ Sensor\ Decimation = 256 * \ 2^{Temp\ Sensor\ Decimation<2:0>}$$

Equation 4

PARALLEL PORT CONFIGURATION REGISTERS 010 THROUGH 012

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
010	*Parallel Port Configuration 1*	PP Tx Swap IQ	PP Rx Swap IQ	Tx Channel swap	Rx Channel swap	Rx Frame Pulse Mode	2R2T Timing	Invert data bus	Invert DATA CLK	C0h	R/W
011	*Parallel Port Configuration 2*	FDD Alt Word Order	Invert Rx1	Invert Rx2	Invert Tx1	Invert Tx2	Invert Rx Frame	Delay Rx Data<1:0>		00h	R/W
012	*Parallel Port Configuration 3*	FDD Rx Rate = 2*Tx Rate	Swap Ports	Single Data Rate	LVDS Mode	Half Duplex Mode	Single Port Mode	Full Port	Full Duplex Swap Bits	04h	R/W

There are many permutations of digital interface settings, many of which are not valid.

SPI Register 0x010—Parallel Port Configuration 1

[D7] PP Tx Swap IQ Clearing this bit swaps the positions of I and Q (performs a spectral inversion).

[D6] PP Rx Swap IQ Same as bit D7 but for the Rx path.

[D5] Tx Channel Swap Setting this bit swaps the positions of Tx1 and Tx2 samples.

[D4] Rx Channel Swap Same as bit D5 but for the Rx path.

[D3] Rx Frame Pulse Mode The AD9361 outputs an "Rx Frame Sync" signal to indicate the beginning of an Rx frame. When this bit is clear (level mode), the Rx Frame signal goes high coincident with the first valid receive sample on the data port. It stays high as long as the receivers are enabled. When this bit is set (pulse mode), the Rx Frame signal toggles with a duty cycle of 50%.

[D2] 2T2R Timing When set, the data port uses a 2T2R timing arrangement, regardless of how many receivers and/or transmitters are enabled. When the bit is clear, the timing will reflect the number of enabled receivers and transmitters.

[D1] Invert Data Bus Inverts the data port(s) from <11:0> to <0:11>.

[D0] Invert DATA CLK Setting this bit inverts DATA_CLK.

SPI Register 0x011—Parallel Port Configuration 2

[D7] FDD Alt Word Order Valid only in Full Duplex, Dual Port, Full Port Mode (0x012[D3:D2] clear, 0x012[D1] set). When this bit is set, each port splits into two 6-bit halves. Rx1 uses 6 bits of a port and Rx2 uses the other 6 bits of the port (i.e. the receivers are not interleaved). Tx1 and Tx2 are organized similarly. When this bit clear, the port configuration is set by the remaining bits.

[D6] Invert Rx1 Must be zero. Setting this bit digitally multiplies Rx1 by -1 which negatively affects DC offset operation.

[D5] Invert Rx2 Must be zero. Setting this bit digitally multiplies Rx2 by -1 which negatively affects DC offset operation.

[D4] Invert Tx1 Setting this bit digitally multiplies the Tx1 signal by -1.

[D3] Invert Tx2 Setting this bit digitally multiplies the Tx2 signal by -1.

[D2] Invert Rx Frame Setting this bit inverts Rx Frame. Rx Frame still has a 50% duty cycle if it is in pulse mode (0x010[D3] set).

[D1:D0] Delay Rx Data<1:0> These bits set the delay of the Rx data relative to the Rx Frame signal. The delay is measured in ½ DATA_CLK cycles for DDR and full DATA_CLK cycles for SDR.

SPI Register 0x012—Parallel Port Configuration 3

[D7] FDD Rx Rate = 2*Tx Rate When clear the Rx Sample rate is equal to the Tx sample rate. When set, the Rx rate is double the Tx rate. This bit can only be set when bit D3 of register 0x012 is clear (Full Duplex Mode).

[D6] Swap Ports Setting this bit swaps port 0 and port 1.

[D5] Single Data Rate When clear, both edges of DATA_CLK are used (one edge for "I" and one edge for "Q"). When set, only one edge of is used.

[D4] LVDS Mode When clear, the data port is single-ended CMOS. Setting this bit causes the AD9361 to use LVDS and requires Full Duplex Mode (0x012[D3] clear), DDR mode (0x012[D5] clear), and Dual Port Mode (0x012[D2] clear).

[D3] Half-Duplex Mode This bit controls only the data port. This bit clear allows simultaneous bi-directional data. This bit set allows data to flow in only one direction at a time. See also the FDD Mode bit (0x013[D0]. Normally, this bit equals the NOT of 0x013[D0].

[D2] Single Port Mode When clear, ports P0 and P1 are both used. When set, only one data port is used.

[D1] Full Port Used only in Full Duplex Mode ([D3] clear) and Dual Port Mode (D2 clear). Setting this bit forces the receivers to be on one port and the transmitters to be on the on the other port. Clearing the bit mixes receivers and transmitters on each port.

[D0] Full Duplex Swap Bits This bit toggles between which bits are used for receive data and which are used for transmit data with one exception. If the FDD Alt Word Order bit (0x011[D7]) is set, then the effect is to swap the most significant 6 bits with the least significant 6 bits. It is not always valid to set this bit.

ENABLE STATE MACHINE (ENSM) REGISTERS 013 THROUGH 017

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
013	*ENSM Mode*	Open							FDD Mode	01h	R/W
014	*ENSM Config 1*	Enable Rx Data Port for Cal	Force Rx On	Force Tx On	Enable ENSM Pin Control	Level Mode	Force Alert State	Auto Gain Lock	To Alert	13h	R/W
015	*ENSM Config 2*	FDD External Control Enable	Power Down Rx Synth	Power Down Tx Synth	TXNRX SPI Control	Synth Enable Pin Control Mode	Dual Synth Mode	Rx Synth Ready Mask	Tx Synth Ready Mask	08h	R/W
016	*Calibration Control*	Rx BB Tune	Tx BB Tune	Rx Quad Cal	Tx Quad Cal	Rx Gain Step Cal	Open	DC Cal RF Start	DC cal BB Start	00h	R/W
017	*State*	Calibration Sequence State<3:0>				ENSM State<3:0>				--	R

SPI Register 0x013—ENSM Mode

Bit D0 controls the ENSM. Normally, clear for TDD applications and set for FDD applications (which is the NOT of 0x012[D3]). One exception to this rule is if a particular data port setting (such as "Alt Word Order" in 0x011[D7]) is only valid in FDD mode but the AD9361 is to be used in a TDD application. In such a case, both the "half-duplex mode" bit and the "FDD Mode" bits would be set.

SPI Register 0x014—ENSM Config 1

[D7] Enable Rx Data Port for Cal Setting this bit enables is useful for two reasons. (1) In TDD mode, during the Tx state, setting this bit will enable the Rx data port. If Tx Monitor(s) are also enabled (see registers 0x001 and 0x057), the Tx monitor I/Q data will be present on the Rx I/O port. (2) As a test mode in the Alert State to verify the Tx tone level during a Tx Quadrature Calibration.

[D6] Force Rx On Setting this bit puts the AD9361 into the Receive state when operating in TDD mode. It is ignored in FDD mode (see 0x013D0]). Clearing this bit moves the AD9361 back to the Alert state. The receiver digital blocks flush their data for 384 ADC clock cycles and the AD9361 ignores SPI commands that affect the ENSM during this time.

[D5] Force Tx On Setting this bit puts the AD9361 into the Transmit state when operating in TDD mode. In FDD mode, setting this bit turns on the receivers and transmitters. Clearing this bit moves the AD9361 back to the Alert state. The transmitter digital blocks flush their data for 384 ADC clock cycles and the AD9361 ignores SPI commands that affect the ENSM during this time.

[D4] Enable ENSM Pin Control When set, the Enable State Machine responds to the Enable and TXNRX signals and changes states accordingly. When clear, SPI writes to bits in register 0x014 change the state. The FB_CLK samples the Enable and TXNRX signals.

[D3] Level Mode When clear, the Enable pulses move the AD9361 among its states. The pulse width must be a minimum of one DATA_CLK cycle. If the Level Mode bit is set, then the level of the ENABLE pin determines the AD9361 state. If ENABLE is low, then the AD9361 is in the Alert state. If ENABLE is high, then TXNRX determines the state in TDD mode (high for transmit, low for receive). TXNRX is ignored in FDD mode. TXNRX must be set while ENABLE is low.

[D2] Force Alert State This self-clearing bit forces the AD9361 into the Alert state from the Wait state. If the "To Alert" bit (D0) is set, then setting the Force Alert State bit forces the ENSM into the Alert state from the Rx or the Tx states. If bit D0 is clear, then setting the Force Alert State will cause the ENSM to go to the Wait state from the Rx or Tx states. This allows the BBP to synchronize to the ENSM if for any reason, the BBP loses track of the state.

[D1] Auto Gain Lock Only applies if the "Gain Unlock Control" (0x0FB[D6]) bit is set and only when the AGC is used in Fast Attack Mode. Setting this bit allows the gain to stay Locked even if certain overload conditions occur. See registers 0x0FB, 0x110, and 0x021.

[D0] To Alert If this bit is clear, the ENSM will always return from the Receive, Transmit, or FDD states to the Wait state. If this bit is set, the AD9361 returns to the Alert state. In TDD mode, the AD9361 ENSM must pass through the Wait or Alert states on its way to the Receive state from the Transmit state and vice versa.

SPI Register 0x015—ENSM Config 2

[D7] FDD External Control Enable This bit applies only when ENSM FDD bit (0x013[D0]) is set. Setting this bit allows independent control of the receivers and transmitters using the ENABLE and TXNRX signals. If the "Level Mode" bit is set (0x014[D3]), then Table 8 describes the operation and the ENABLE and TXNRX signals are level detected by the AD9361. If the "Level Mode" bit is clear, then pulses on these signals toggle the receivers and transmitters on and off.

ENABLE	TXNRX	Signal Paths Enabled
Low	Low	None
High	Low	Receivers Only
Low	High	Transmitters Only
High	High	Receivers and Transmitters

Table 8.FDD External Control Mapping

Disabling receivers or transmitters does not cause the AD9361 to exit the FDD state so the digital blocks do not flush its digital blocks automatically. Disabling receivers and/or transmitters causes the internal RxON and/or TxON signals to go low, respectively.

[D6] Power Down Rx Synth Test bit. Setting this bit manually powers down the Rx RF synthesizer.

[D5] Power Down Tx Synth Test bit. Setting this bit manually powers down the Tx RF synthesizer.

[D4] TXNRX SPI Control Only used in single synthesizer mode (D2 clear) and Synth Enable Pin Control Mode (D3) clear. See bit D3.

[D3] Synth Enable Pin Control Mode Ignored in dual synth mode ([D2] set). When set, the logic level of the TXNRX pin controls which RF synthesizer is enabled. When this bit is clear, the logic level of bit D4 controls which synthesizer is enabled. TXNRX (or bit D4) high turns on the Tx synthesizer and TXNRX (or bit D4) low turns on the Rx synthesizer.

[D2] Dual Synth Mode If this bit is clear, then only one RF synthesizer is on at any given time. When this bit is set, both synthesizers are on. For FDD mode, this bit must be set. The AD9361 does not set this bit automatically. For example, to use the Power Monitor feature (which uses receiver circuitry when the AD9361 is in the transmit state), this bit must be set.

[D1] Rx Synth Ready Mask Normally clear. When clear, the ENSM moves to the Rx state after the Rx RFVCO successfully calibrates (Rx RF Tuner Ready goes high). When set, the ENSM ignores the Receive RF Tuner Ready Signal.

[D0] Tx Synth Ready Mask Same as bit D1 but for the Transmit RF PLL.

SPI Register 0x016—Calibration Control

[D7] Rx BB Tune Setting this bit starts the receiver analog baseband filter calibration and self-clears when the calibration completes.

[D6] Tx BB Tune Same as bit D7 but for the transmit filter.

[D5] Rx Quad Cal Setting this bit starts the receiver quadrature calibration and self-clears when the calibration completes. The calibration will not run unless the "Free Run" bit (0x169[D3]) is clear.

[D4] Tx Quad Cal Setting this bit starts the transmit quadrature calibration and self-clears when the calibration completes.

[D3] Rx Gain Step Cal Setting this bit starts an LNA and Mixer gain step calibration and self-clears when the calibration completes. An external RF signal must be present at the Rx inputs. See registers 0x140-0x144.

[D1] RF DC Cal Setting this bit performs an RF DC Offset calibration of the Rx signal paths and the bit self-clears when the cal completes. Run a BB DC Cal (see bit D0) first. If D1 and D0 are set at the same time, the BB DC Cal runs first.

[D0] BB DC Cal Setting this bit performs a baseband DC Offset cal of the Rx signal paths and self-clears when the cal completes. Run this cal before running the RF DC cal (bit D1).

SPI Register 0x017—State—Read-Only Test Mode Bits

[D7:D4] Calibration Sequence State<3:0> Table 9 shows the states of the calibration state machine.

Calibration State	0x017[7:4]
Calibrations Done	1
Baseband DC Offset Calibration	2
RF DC Offset Calibration	3
Tx1 Quadrature Calibration	4
Tx2 Quadrature Calibration	5
Rx1 Quadrature Calibration	6
Rx2 Quadrature Calibration	7
Receiver Gain Step Calibration	9
Baseband Calibration Flush	A
RF Calibration Flush	B
Transmitter Quadrature Calibration Flush	C
Receiver Quadrature Calibration Flush	D
Transmitter Power Detector Calibration Flush	E
Receiver Gain Step Calibration Flush	F

Table 9.Calibration State

[D3:D0] ENSM State<3:0> Table 10 shows the states of the Enable State Machine (ENSM).

ENSM State	0x017[3:0]	Note
SLEEP or WAIT	0	AD9361 clocks/BBPLL disabled
ALERT	5	Synthesizers Enabled.
TX	6	Transmitter signal chain enabled
TX FLUSH	7	Transmitter digital block flush time
RX	8	Receiver signal chain enabled
RX FLUSH	9	Receiver digital block flush time
FDD	A	Transmit and receive signal chains enabled
FDD FLUSH	B	Flush all digital signal path blocks

Table 10. ENSM State

AUXDAC REGISTERS 018 THROUGH 01B

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
018	*AuxDAC 1 Word*	AuxDAC 1 Word<9:2>								00h	R/W
019	*AuxDAC 2 Word*	AuxDAC 2 Word<9:2>								00h	R/W
01A	*AuxDAC 1 Config*	Open		Comp Ctrl 1	AuxDAC1 Step Factor	AuxDAC 1 Vref<1:0>		AuxDAC 1 Word <1:0>		00h	R/W
01B	*AuxDAC 2 Config*	Open		Comp Ctrl 2	AuxDAC2 Step Factor	AuxDAC 2 Vref<1:0>		AuxDAC 2 Word <1:0>		00h	R/W

Registers 0x023, 0x026, and 0x030 through 0x033 determine when and how the AuxDACs are enabled.

SPI Registers 0x018, 0x019, 0x01A[D1:D0] and 0x01B[D1:D0] —AuxDAC 1(2) Word

The AuxDAC output voltage is defined by Equation 5 below.

$$AuxDAC\ Vout(V) = 0.97 * Vref + (0.000738 + 9 * 10^{-6} * (Vref * 1.6 - 2)) * AuxDAC\ Word < 9:0 > * Step\ Factor - 0.3572 * Step\ Factor + 0.05$$

Equation 5

Where:

Vref is set by 0x01A[D3:D2] (AuxDAC 1) and 0x01B[D3:D2] (AuxDAC 2)

Step Factor is set by register 0x01A[D4] (AuxDAC 1) and 0x01B[D4] (AuxDAC 2)

Registers 0x018through 0x01B are the AuxDAC Words

Maximum AuxDAC output voltage is limited to 3V for VDDA_GPO = 3.3V

SPI Register 0x01A—AuxDAC 1 Config

[D5] Comp Ctrl1 Normally clear. Setting this bit adds 400fF of capacitance to the AuxDAC to increase stability.

[D4] AuxDAC 1 Step Factor If this bit is clear, the Step Factor in the above equation = 2. If the bit is set, the Step Factor = 1.

[D3 :D2] AuxDAC 1 Vref<1:0> These bits encode the Vref factor in the above equation. Table 11 shows the encoding.

Vref<1:0>	Vref (V)
00	1.0
01	1.5
10	2.0
11	2.5

Table 11.AuxADC Vref

SPI Register 0x01B—AuxDAC 2 Config

Same as Register 0x01A but applies to AuxDAC 2.

AUXILIARY ADC REGISTERS 01C THROUGH 01F

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
01C	*AuxADC Clock Divider*	Open		AuxADC Clock Divider<5:0>						10h	R/W
01D	*Aux ADC Config*	Open				Aux ADC Decimation<2:0>			AuxADC Power Down	01h	R/W
01E	*AuxADC Word MSB*	AuxADC Word MSB<11:4>								--	R
01F	*AuxADC LSB*	Open				AuxADC Word LSB<3:0>				--	R

SPI Register 01C—AuxADC Clock Divider

[D5:D0] AuxADC Clock Divider<5:0> The AuxADC clock results from dividing down the BBPLL, described by Equation 6. A divider value of 0 is invalid.

$$AuxADC\ Clock\ Frequency = \frac{BBPLL\ Frequency}{AuxADC\ Clock\ Divider < 5:0 >}$$

Equation 6

SPI Register0x 01D—AuxADC Config

[D3:D1] AuxADC Decimation<2:0> These bits set the AuxADC decimation per Equation 7.

$$AuxADC\ Decimation = 256 * 2^{AuxADC\ Decimation<2:0>}$$

Equation 7

[D0] AuxADC Power Down Setting this bit powers down the AuxADC.

SPI Registers 0x01E & 0x01F—AuxADC Word

These registers hold the 12-bit AuxADC word. When reading the AuxADC word, the temperature sensor should be prevented from updating by clearing bit D0 in registers 0x00C and 0x00D.

GPO, AUXDAC, AGC DELAY, AND SYNTH DELAY CONTROL REGISTERS 020 THROUGH 033

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
020	*Auto GPO*	GPO Enable Auto Rx<3:0>				GPO Enable Auto Tx<3:0>				33h	R/W
021	*AGC Gain Lock Delay*	Gain Lock Delay<7:0>								0Ah	R/W
022	*AGC Attack Delay*	Open	Invert Bypassed LNA Polarity	AGC Attack Delay<5:0>						0Ah	R/W
023	*AuxDAC Enable Control*	AuxDac Manual Bar<1:0>		AuxDAC Auto Tx Bar<1:0>		AuxDAC Auto Rx Bar<1:0>		AuxDAC Init Bar<1:0>		3fh	R/W
024	*RX Load Synth Delay*	Rx Load Synthesizer Delay<7:0>								02h	R/W
025	*TX Load Synth Delay*	Tx Load Synthesizer Delay<7:0>								02h	R/W
026	*External LNA control*	AuxDAC Manual Select	External LNA2 control	External LNA1 control	GPO manual select	Open<3:0>				00h	R/W
027	*GPO Force and Init*	GPO Manual Control<3:0>				GPO Init State<3:0>				03h	R/W
028	*GPO0 Rx delay*	GPO0 Rx Delay<7:0>								00h	R/W
029	*GPO1 Rx delay*	GPO1 Rx Delay<7:0>								00h	R/W
02A	*GPO2 Rx delay*	GPO2 Rx Delay<7:0>								00h	R/W
02B	*GPO3 Rx delay*	GPO3 Rx Delay<7:0>								00h	R/W
02C	*GPO0 Tx Delay*	GPO0 Tx Delay<7:0>								00h	R/W
02D	*GPO1 Tx Delay*	GPO0 Tx Delay<7:0>								00h	R/W
02E	*GPO2 Tx Delay*	GPO0 Tx Delay<7:0>								00h	R/W
02F	*GPO3 Tx Delay*	GPO0 Tx Delay<7:0>								00h	R/W
030	*AuxDAC1 Rx Delay*	AuxDAC 1 Rx Delay <7:0>								00h	R/W
031	*AuxDAC2 Tx Delay*	AuxDAC 1 Tx Delay <7:0>								00h	R/W
032	*AuxDAC2 Rx Delay*	AuxDAC 2 Rx Delay <7:0>								00h	R/W
033	*AuxDAC2 Tx Delay*	AuxDAC 2 Tx Delay <7:0>								00h	R/W

When the AD9361 powers up into the sleep state, the default register values define the GPO logic levels. Thus, the GPOs will auto-toggle and GPO0 and GPO1 will be high while GPO2 and GPO3 will be low.

SPI Register 0x020—Auto GPO

[D7:D4] GPO Enable Auto Rx<3:0> This nibble controls which GPO pins change state when the ENSM enters the Rx state. Bit D7 controls GPO3, etc. Register 0x27 sets the initial (Alert state) logic level of the GPOs. Useful for TDD applications where the AD9361 transitions among the Alert, Receive, and Transmit states. Ignored if 0x026[D4] is set.

[D3:D0] GPO Enable Auto Tx<3:0> Same as D7:D4 but applies when the ENSM enters the Tx state. Ignored if 0x026[D4] is set.

SPI Register 0x021—AGC Gain Lock Delay

Only applies if 0x014[D1] and 0xFB[D6] are set, allowing the gain to stay Locked even if certain overload conditions occur. See registers 0x0FB and 0x110. Normally clear if the overload thresholds are set correctly.

SPI Register 0x022—AGC Attack Delay

[D6] Invert Bypassed LNA Polarity The phase response of the LNA when bypassed versus when it is not bypassed differs by approximately 180 degrees. Setting this bit will automatically rotate the phase of the Rx signal by 180 degrees when the LNA is bypassed.

[D5:D0] AGC Attack Delay Only applies for the fast AGC. The AGC Attack Delay prevents the AGC from starting its algorithm until the receive path has settled. The delay counter starts when the AD9361 enters the Receive state. Units: microseconds. Resolution: 1us/LSB. Range: 0 through 31 microseconds. For the value in microseconds to be accurate, register 0x03A must be set correctly.

SPI Register 0x023—AuxDAC Enable Control

[D7:D6] AuxDAC Manual Bar<1:0> *Clearing* bit D7 manually enables AuxDAC2. *Clearing* bit D6 manually enables AuxDAC1. Ignored if 0x026[D7] is clear.

[D5:D4] AuxDAC Auto Tx Bar<1:0> *Clearing* bit D5 causes AuxDAC 2 to change state (On to Off or vice versa) when the ENSM enters the Tx state. Bit D4 controls AuxDAC 1 in the same manner. Ignored if 0x026[D7] is set.

[D3:D2] AuxDAC Auto Rx Bar<1:0> *Clearing* bit D3 causes AuxDAC 2 to change state (On to Off or vice versa) when the ENSM enters the Rx state. Bit D2 controls AuxDAC 1 in the same manner. Ignored if 0x026[D7] is set.

[D1:D0] AuxDAC Initial Bar<1:0> *Clearing* bit D1 sets the state of AuxDAC2 to "On" when the AD9361 is in the Alert state. Bit D0 controls AuxDAC 1 in the same manner. Ignored if 0x026[D7] is set.

SPI Register 0x024—Rx Load Synthesizer Delay<7:0>

This register sets the delay from Rx synthesizer power up to synthesizer calibration. The resolution is 1us/LSB and register 0x03A must be correct for the delay to be accurate. The delay applies when the AD9361 transitions from the Wait state to the Alert state. In dual synthesizer mode (0x015[D2] high), both synthesizers power up when the AD9361 transitions from Wait to Alert so the Rx delay (and Tx delay in 0x025) is used. In single synthesizer mode and when using the ENSM in TDD mode, the VCO calibration waits for the Rx load synthesizer delay after entering the Rx state and it similarly waits for the Tx delay after entering the Tx state.

SPI Register 0x025—Tx Load Synthesizer Delay<7:0>

Same as for register 0x024 but affects the Tx synthesizer.

SPI Registers 0x026—External LNA Control

[D7] AuxDAC Manual Select When clear, the AuxDAC states slaves to the ENSM and, depending on the settings in register 0x023, may change state as the ENSM changes state. When set, SPI writes to 0x023[D7:D6] manually control the state of the AuxDACs.

[D6] External LNA 2 Control When set, the "Ext LNA Ctrl" bit in the Rx2 gain table sets the GPO1 state. See 0x12C for details.

[D5] External LNA 1 Control Same as bit D6 but applies to the receiver 1 gain table and GPO 0.

[D4] GPO Manual Select When clear, the GPOs slave to the ENSM, and, depending on the settings in register 0x020, may change state as the ENSM changes state. When set, 0x027[D7:D4] sets the value of the GPOs.

SPI Register 0x027—GPO Force and Init

[D7:D4] GPO Manual Control When clear, the GPOs are logic low. When set, the GPOs are logic high. Bit D7 controls GPO3, D6 controls GPO 2, etc. Only applies when 0x026[D4] is set.

[D3:D0] GPO Init State When clear, the GPOs are logic low in the Sleep, Wait, and Alert States and when set, the GPOs are logic high in the Alert state. Bit D3 controls GPO 3, D2 controls GPO 2, etc. Only applicable when the GPO states are slaved to the ENSM. Register 0x020 controls the GPO state changes as the ENSM changes state. Only applicable if 0x026[D4] is clear.

SPI Registers 0x028 through0x 02B—GPOn Rx Delay<7:0>

Only applicable if 0x026[D4] is clear. When the GPOs are slaved to the ENSM, these registers set the delay from an ENSM state change of Alert to Receive to the time that the GPOs change logic level. 1us/LSB with a range from 0 to 255 us. The delay from an ENSM state change of Receive to Alert is always fixed, allowing the Rx digital filters to flush before changing the state(s) of the GPO(s). Register 0x03A must be set correctly for the delay resolution to be 1LSB/us.

SPI Registers 0x02C through 0x02F—GPOn Tx Delay<7:0>

Same as registers 0x028 through 0x02B but for the transition from the Alert state to the Transmit State.

SPI Registers 0x030 through 0x033—AuxDAC Rx/Tx Delay<7:0>

These delays affect the state of the AuxDACs similar to how registers 0x028-0x02B affect the GPOs. Only applicable if 0x026[D7] is clear.

CONTROL OUTPUT REGISTERS 035 THROUGH 036

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
035	*Control Output Pointer*	Control Output Pointer<7:0>								00	R/W
036	*Control Output Enable*	En ctrl7	En ctrl6	En ctrl5	En ctrl4	En ctrl3	En ctrl2	En ctrl1	En ctrl0	FF	R/W

The AD9361 can port a variety of signals to the eight Control Output pins. A pointer to a table shown below controls which signals are ported. The pointer selects a row and each cell in that row corresponds to a particular Control Output pin. See Table 12 below.

	Control Output Bit Position							
Reg 0x035	**[7]**	**[6]**	**[5]**	**[4]**	**[3]**	**[2]**	**[1]**	**[0]**
00	Cal Done	TX CP Cal Done	RX CP Cal Done	Rx BB Filter Tuning Done	Tx BB Filter Tuning Done	Gain Step Cal Busy	Rx Synth VCO Cal Busy	Tx Synth VCO Cal Busy
01	Tx RF PLL Lock	Rx RF PLL Lock	BB PLL Lock	0	0	0	0	0
02	BB DC Cal Busy	RF DC Cal Busy	CH1 Rx Quad Cal Busy	CH1 Tx Quad Cal Busy	CH2 Rx Quad Cal Busy	CH2 Tx Quad Cal Busy	Gain Step Cal Busy	Tx Mon Cal Busy
03	CH1 Low Power	CH 1 Lg LMT Ovrg	CH 1 Lg ADC Ovrg	CH1 Sm ADC Ovrg	CH 2 Low Power	CH 2 Lg LMT Ovrg	CH 2 Lg ADC Ovrg	CH 2 Sm ADC Ovrg
04	CH 2 Rx Gain[6]	CH 2 Rx Gain[5]	CH 2 Rx Gain[4]	CH 2 Rx Gain[3]	CH 2 Rx Gain[2]	CH 2 Lg LMT Ovrg	CH 2 Lg ADC Ovrg	CH 2 Gain Lock
05	CH2 Gain Change	CH1 Gain Change	CH 2 Low Power	CH 2 Lg LMT Ovrg	CH 2 Lg ADC Ovrg	CH 2 Gain Lock	CH 2 Energy Lost	CH2 Stronger Signal
06	CH1Low Power	CH 1 Lg LMT Ovrg	CH 1 Lg ADC Ovrg	CH 1 Rx Gain[6]	CH 1 Rx Gain[5]	CH 1 Rx Gain[4]	CH 1 Rx Gain[3]	CH 1 Rx Gain[2]
07	CH1 Low Power	CH 1 Lg LMT Ovrg	CH 1 Lg ADC Ovrg	CH1 Sm ADC Ovrg	CH1 AGC State[2]	CH1 AGC State[1]	CH1 AGC State[0]	CH1 Gain Lock
08	CH 1 Stronger Signal	CH 1 Gain Lock	CH 1 Energy Lost	CH 1 Gain Change	CH 2 Stronger Signal	CH 2 Gain Lock	CH 2 Energy Lost	CH 2 Gain Change
09	RxOn	CH 1 RSSI Preamble Ready	CH 1 RSSI Symbol Ready	TxOn	CH 2 RSSI Preamble Ready	CH 2 RSSI Symbol Ready		
0A	CH 1 Tx Int3 Overflow	CH 1 Tx HB3 Overflow	CH 1 Tx HB2 Overflow	CH 1 Tx QEC Overflow	CH 1 Tx HB1 Overflow	CH 1 Tx FIR Overflow	CH 1 Rx FIR Overflow	
0B	Cal Seq State[3]	Cal Seq State [2]	Cal Seq State [1]	Cal Seq State [0]	ENSM[3]	ENSM[2]	ENSM[1]	ENSM[0]
0C	CH 1 Energy Lost	CH 1 Reset Peak Detect	CH 2 Energy Lost	CH 2 Reset Peak Detect	Gain Freeze	CH 1 Digital Sat	CH 2 Digital Sat	
0D	CH1 Tx Quad	CH1 Tx Quad	CH1 Tx Quad	RF DC Cal	CH2 Tx Quad	CH2 Tx Quad	CH2 Tx Quad	

	Control Output Bit Position							
Reg 0x035	**[7]**	**[6]**	**[5]**	**[4]**	**[3]**	**[2]**	**[1]**	**[0]**
	Cal Status[1]	Cal Status[0]	Cal Done	Busy	Cal Status[1]	Cal Status[0]	Cal Done	
0E	CH1 Rx Quad Cal Status[1]	CH1 Rx Quad Cal Status[0]	CH1 Rx Quad Cal Done	BB DC Cal Busy	CH2 Rx Quad Cal Status[1]	CH2 Rx Quad Cal Status[0]	CH2 Rx Quad Cal Done	
0F	CH1 AGC State[2]	CH1 AGC State[1]	CH1 AGC State[0]	CH1 Reset Peak Detect	CH2 Reset Peak Detect	CH 1 RF DC Cal State[1]	CH 1 RF DC Cal State[0]	
10	CH2 AGC State[2]	CH2 AGC State[1]	CH2 AGC State[0]	CH 2 Enable RSSI	CH 1Enable RSSI	CH 2 RF DC Cal State[1]	CH 2 RF DC Cal State[0]	
11	AuxADC Output[11]	AuxADC Output[10]	AuxADC Output[9]	AuxADC Output[8]	AuxADC Output[7]	AuxADC Output[6]	AuxADC Output[5]	AuxADC Output[4]
12	CH 1 Filter Power Ready	CH 1 Gain Lock	CH 1 Energy Lost	CH 1 Stronger Signal	CH 1 ADC Power Ready	CH 1 AGC State [2]	CH 1 AGC State [1]	CH 1 AGC State [0]
13	CH 2 Filter Power Ready	CH 2 Gain Lock	CH 2 Energy Lost	CH 2 Stronger Signal	CH 2 ADC Power Ready	CH 2 AGC State [2]	CH 2 AGC State [1]	CH 2 AGC State [0]
14	CH 2 Tx Int3 Overflow	CH 2 Tx HB3 Overflow	CH 2 Tx HB2 Overflow	CH 2 Tx QEC Overflow	CH 2 Tx HB1 Overflow	CH 2 Tx FIR Overflow	CH 2 Rx FIR Overflow	0
15	CH1 SOI Present	CH1 Update DCRF	CH1 Measure DCRF	CH1 DC Track Count Reached	0	0	0	0
16	CH1 Gain Lock	CH1 Rx Gain[6]	CH1 Rx Gain[5]	CH1 Rx Gain[4]	CH1 Rx Gain[3]	CH1 Rx Gain[2]	CH1 Rx Gain[1]	CH1 Rx Gain[0]
17	CH2 Gain Lock	CH2 Rx Gain[6]	CH2 Rx Gain[5]	CH2 Rx Gain[4]	CH2 Rx Gain[3]	CH2 Rx Gain[2]	CH2 Rx Gain[1]	CH2 Rx Gain[0]
18	CH2 SOI Present	CH2 Update DCRF	CH2 Measure DCRF	CH2 DC Track Count Reached	CH2Enable Dec Pwr	CH2 Enable ADC Pwr	CH1 Enable Dec Pwr	CH1 Enable ADC Pwr
19	RX Syn Cp Cal[3]	RX Syn Cp Cal[2]	RX Syn Cp Cal[1]	RX Syn Cp Cal[0]	TX Syn Cp Cal[3]	TX Syn Cp Cal[2]	TX Syn Cp Cal[1]	TX Syn Cp Cal[0]
1A	RX Syn VCO Tuning[8]	RX Synth VCO ALC[6]	RX Synth VCO ALC[5]	RX Synth VCO ALC[4]	RX Synth VCO ALC[3]	RX Synth VCO ALC[2]	RX Synth VCO ALC[1]	RX Synth VCO ALC[0]
1B	TX Syn VCO Tuning[8]	TX Synth VCO ALC[6]	TX Synth VCO ALC[5]	TX Synth VCO ALC[4]	TX Synth VCO ALC[3]	TX Synth VCO ALC[2]	TX Synth VCO ALC[1]	TX Synth VCO ALC[0]
1C	RX Syn VCO Tuning[7]	RX Syn VCO Tuning[6]	RX Syn VCO Tuning[5]	RX Syn VCO Tuning[4]	RX Syn VCO Tuning[3]	RX Syn VCO Tuning[2]	RX Syn VCO Tuning[1]	RX Syn VCO Tuning[0]
1D	TX Syn VCO Tuning[7]	TX Syn VCO Tuning[6]	TX Syn VCO Tuning[5]	TX Syn VCO Tuning[4]	TX Syn VCO Tuning[3]	TX Syn VCO Tuning[2]	TX Syn VCO Tuning[1]	TX Syn VCO Tuning[0]
1E	CH1Low Thresh Exceeded	CH1High Thresh Exceeded	CH1Gain Upd Count Exp	CH1AGC State [1]	CH1AGC State [0]	CH 1 Gain Change	Temp Sense Valid	AuxADC Valid
1F	CH2Low Thresh Exceeded	CH2High Thresh Exceeded	CH2Gain Upd Count Exp	CH2AGC State[1]	CH2AGC State[0]	CH 2 Gain Change		

Table 12. Control Output Map

SPI Register 0x036—Control Output Enable

This register controls which Control Output pins are enabled. Setting a particular bit enables the corresponding Control Output signal. Any bit cleared will cause the Control Output pin associated with that bit to drive out a logic zero. See Table 13 for mapping.

Control Output Bit Position	CTRL_OUT pin Name	AD9361 pin Designation
7	CTRL_OUT7	G4
6	CTRL_OUT6	F4
5	CTRL_OUT5	F5
4	CTRL_OUT4	F6

Control Output Bit Position	CTRL_OUT pin Name	AD9361 pin Designation
3	CTRL_OUT3	E6
2	CTRL_OUT2	E5
1	CTRL_OUT1	E4
0	CTRL_OUT0	D4

Table 13. Control Output Bit/Ball Mapping

PRODUCT ID REGISTER 037

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
037	*Product ID*	Open				9361	Rev[2:0]			--h	R

SPI Register 0x037—Product ID

Bits D3 set indicates that this is an AD9361. Bits D2 through D0 represent the revision of the device.

REFERENCE CLOCK CONFIGURATION REGISTER 038

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
038	*DCXO Output Buffer Config*	Open	Output Buffer Enable	Open	Output Buffer Drive<4:0>					80h	R/W

REFERENCE CLOCK DELAY UNIT COUNTER REGISTER 03A

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
03A	*Reference Clock Cycles*	open	Reference Clock Cycles per us<6:0>							00h	R/W

SPI Register 0x03A—Reference Clock Cycles

Many delay settings assume a resolution of 1LSB/microsecond. For the assumption to be correct, this register must be programmed with the number of reference clock cycles per microsecond minus 1. The "reference clock" is an external reference or the DCXO.

DIGITAL IO CONTROL REGISTERS 03B THROUGH 03E

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
03B	*Digital I/O Control*	CLK Out Drive	DATACLK drive	DATACLK slew <1:0>		0	Data Port Drive	Data Port Slew<1:0>		00h	R/W
03C	*LVDS Bias control*	CLK Out Slew<1:0>		Rx On Chip Term	Bypass Bias R	LVDS Tx LO VCM	LVDS Bias <2:0>			03h	R/W
03D	*LVDS Invert control1*	LVDS pn Invert<7:0>								00h	R/W
03E	*LVDS Invert control2*	LVDS pn Invert<15:8>								00h	R/W

SPI Register 0x03B—Digital I/O Control

[D7] CLKOUT Drive CLK_OUT drive strength. Setting this bit increases the drive strength by approximately 20%.

[D6] DATACLK Drive DATA_CLK drive strength. Setting this bit increases the drive strength by approximately 20%.

[D5:D4] DATACLK Slew<1:0> Slew control for DATA_CLK. 1'b00 = fastest rise/fall times. 1'b11 = slowest rise/fall times.

[D3] Not used. Must be zero.

[D2] Data Port Drive Data port output driver strength. Setting this bit increases the drive strength by approximately 20%

[D1:D0] Data Port Slew<1:0> Slew control for the Data Ports. 1'b00 = fastest rise/fall times. 1'b11 = slowest rise/fall times.

SPI Register 0x03C—LVDS Bias Control

[D7:D6] CLK Out Slew<1:0> Slew control for CLK_OUT. 1'b00 = fastest rise/fall times. 1'b11 = slowest rise/fall times.

[D5] Rx On Chip Term Use LVDS Rx100 on-chip termination. Do not set this bit if using CMOS I/O.

[D4] Bypass Bias R Bypass bias resistor in LVDS RX comparator.

[D3] LVDS Tx LO VCM Lowers output common mode voltage by 60mV.

[D2:D0] LVDS Bias<2:0> LVDS driver amplitude control. $|V_{OD}|$ = 75mV to 450mV; 75mV/LSB.

SPI Registers 0x03D & 0x03E—LVDS Invert Control

The phase of any LVDS pair can be inverted from their default configuration by setting bits in these two registers. The bits map per Table 14. Note that the default configuration (SPI bit set to zero) for the data bits is inverted so if LVDS is used, 0x03D = 0xFF and 0x03E = 0x0F results in no data inversion. The clock and frame signals are not inverted when the SPI bits are set to zero.

Register & Bits	Signals Affected	Chip Default Bit Value	Configuration for Chip Default	Recommended Configuration
SPI Reg 0x03D				
[D7]	P0[3:2]	0	Inverted	1
[D6]	P0[1:0]	0	Inverted	1
[D5]	P1[11:10]	0	Inverted	1
[D4]	P1[9:8]	0	Inverted	1
[D3]	P1[7:6]	0	Inverted	1
[D2]	P1[5:4]	0	Inverted	1
[D1]	P1[3:2]	0	Inverted	1
[D0]	P1[2:0]	0	Inverted	1
SPI Reg 0x03E				
[D7]	FBCLK	0	Not Inverted	0
[D6]	Tx Frame	0	Not Inverted	0
[D5]	DATACLK	0	Not Inverted	0
[D4]	Rx Frame	0	Not Inverted	0
[D3]	P0[11:10]	0	Inverted	1
[D2]	P0[9:8]	0	Inverted	1
[D1]	P0[7:6]	0	Inverted	1
[D0]	P0[5:4]	0	Inverted	1

Table 14. LVDS Signal Inversion Mapping

BBPLL CONTROL REGISTERS 03F THROUGH 04F

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
03F	*SDM Control 1*	SDM SIF Data<3:0>				BBPLL SDM CLK Enable Bar	Init BB FO CAL	BBPLL SDM Bypass	BBPLL Reset Bar	01h	R/W
040	*SDM Control 2*	Dither<1:0>		SIF Clk	SIF Addr<4:0>					00h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
041	*Fractional BB Freq Word 1*	Fractional BB Frequency Word<23:16>								00h	R/W
042	*Fractional BB Freq Word 2*	Fractional BB Frequency Word<15:8>								00h	R/W
043	*Fractional BB Freq Word 3*	Fractional BB Frequency Word<7:0>								00h	R/W
044	*Integer BB Freq Word*	Integer BB Frequency Word<7:0>								10h	R/W
045	*Clock Control*	PLL FB Inv	FB Clk Inv	Ref Clk Inv	PFD Reset Delay		PFD Clk Edge	Ref Frequency Scaler		00h	R/W
046	*CP Current*	CP Test Mode<1:0>		Charge Pump Current<5:0>						09h	R/W
047	*CP Bleed Current*	MCS refclk Scale En	Bleed Enable	Charge Pump Bleed Current<5:0>						00h	R/W
048	*Loop Filter 1*	C1 Word<2:0>			R1 Word<4:0>					C5h	R/W
049	*Loop Filter 2*	R2 Word<0>	C2 Word<4:0>					C1 Word<4:3>		B8h	R/W
04A	*Loop Filter 3*	Bypass C3	Bypass R2	C3 Word<3:0>				R2 Word<2:1>		2Eh	R/W
04B	*VCO Control*	Freq Cal Enable	Freq Cal Count Length<1:0>		Freq Cal Reset	Force VCO band enable	Forced VCO band word<2:0>			C0h	R/W
04C	*VCO Program 1*	SIF Addr<1:0>		SIF Data<5:0>						00h	R/W
04D	*VCO Program 2*	Open	Doubler Delay<1:0>		POR Override	SIF Reset	SIF Clk	SIF Addr<3:2>		00h	R/W
04E	*SDM Control*	MCS Pulse Delay<1:0>		VCO Cal Tol	Cal Clock div 4	SDM Reset	Lock Detect Reset	SDM Divider Reset	SDM SIF Reset	00h	R/W
04F	*BBPLL External Clock*	BBPLL Ext Clock Enable	Force Freq Cal State	Bypass Bias Filter	Force OTA CCAP	OTA1 CCAP<4:0>				00h	R/W

SPI Register 0x03F—SDM Control 1

[D2] Init BB FO Cal Setting this bit manually starts a BBPLL VCO cal. Bit D7 of register 0x04B must be set to enable the calibration. Set this bit after writing the BBPLL words. This is the only way to start a BBPLL calibration. When the calibration starts the AD9361 holds the BBPLL digital lock detect circuit in the reset state. When the calibration completes, the BBPLL Lock bit goes high. Clear Init BB FO Cal bit after setting it (it is not self-clearing). The set and clear instructions can be consecutive without waiting for the calibration to complete.

[D0] BBPLL Reset Bar When clear, the BBPLL is not running and all digital logic including the SDM, ref path dividers, and analog circuits power down. Setting this bit enables the BBPLL Set this bit after writing the BBPLL words.

SPI Registers 0x041 through 0x044—Fractional and Integer BB Freq. Words

See Equation 8 and Equation 9 below:

$$BBPLL\ Integer\ Word = Floor\left(\frac{BBPLL\ Frequency\ (MHz)}{Reference\ Clock\ Frequency}\right)$$

Equation 8

$$BBPLL\ Frac\ Word = Floor\left(\left(\frac{BBPLL\ Frequency\ (MHz)}{Reference\ Clock\ Frequency} - floor\left(\frac{BBPLL\ Frequency(MHz)}{Reference\ Clock\ Frequency}\right)\right) * 2088960\right)$$

Equation 9

For example, if the desired BBPLL Frequency is 716.8 MHz and the Reference Clock Frequency is 40 MHz, then the BBPLL Integer Word = 17(decimal) = 11(hex). The Fractional Word = 1921843(decimal) = 1D5333(hex). Thus, 0x043 = x33, 0x042 = x53, and 0x041 = x1D.

Equation 10rearranges the terms and shows the BBPLL output frequency in terms of the register words.

$$F_{OUT} = F_{REF} \cdot \left[N_{INTEGER} + \frac{N_{FRACTIONAL}}{2088960}\right]$$

Equation 10

Where

$N_{INTEGER}$ is the BBPLL Integer Word (decimal)

$N_{FRACTIONAL}$ is the BBPLL Fractional Word (decimal)

Note that the desired BBPLL frequency is approximate. The finite modulus of the fractional-N PLL results in a non-exact BBPLL frequency if the relationship between the reference clock and the BBPLL frequency is not a simple ratio. More importantly, the inherent accuracy tolerance of the reference clock also affects the BBPLL frequency.

SPI Register 0x045—Clock Control

[D1:D0] Ref Frequency Scaler<1:0> The reference clock frequency is scaled before it enters the BBPLL. 00: x1; 01: x½; 10: x¼; 11: x2.

SPI Register 0x046—CP Current

[D5:D0] Charge Pump Current<5:0> Charge pump bleed current setting. Resolution: 25 uA. Offset: 25 uA. Range: 25 uA to 1575 uA.

SPI Register 0x047—CP Bleed Current

[D7] MCS Refclk Scale En Only applies if using multi-chip synchronization. Set this bit high to use the BBPLL refclk scaler output as the clock domain that detects transitions on the SYNC_IN pin.

SPI Registers 0x048 through 0x04A—Loop Filter

Registers 048 through 04A refer to the loop filter schematic in Figure 2:

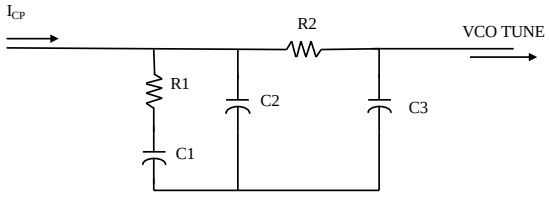

Figure 2. BBPLL Internal Loop Filter

The following equations describe the component values:

$$R1\ Word(decimal) = floor\left(\frac{20k}{R1} - 4\right)$$

Equation 11

$$C1\ Word(decimal) = floor\left(\frac{C1 - 40pF}{16.25pF}\right)$$

Equation 12

$$C2\ Word(decimal) = floor\left(\frac{ln(C2) - ln(1.17pF)}{ln(1.17)}\right)$$

Equation 13

$$R2\ Word(decimal) = floor\frac{(20k - 5*R2)}{4*R2}$$

Equation 14

SPI Register 0x04B—VCO Control

[D7] Freq Cal Enable Set this bit to enable VCO frequency calibration. See also the Init BB FO Cal bit (0x03F[D2]).

[D6:D5] Freq Cal Count Length 00 = 128; 01 = 256; 10 = 512; 11 = 1024. Longest cal time recommended.

[D4] Freq Cal Reset Set this bit to reset the VCO calibration state machine.

SPI Register 04E—SDM Control 3

[D4] Cal Clock div 4 Set this bit to slow down the BBPLL calibration clock by a factor of 4 (increases cal time proportionally).

POWER DOWN OVERRIDE REGISTERS 050 THROUGH 058

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
050	*Rx Synth Power Down Override*	Open			Rx LO Power Down	Rx Synth VCO ALC Power Down	Rx Synth PTAT Power Down	Rx Synth VCO Power Down	Rx Synth VCO LDO Power Down	00h	R/W
051	*TX Synth Power Down Override*	Open			Tx LO Power Down	Tx Synth VCO ALC Power Down	Tx Synth PTAT Power Down	Tx Synth VCO Power Down	Tx Synth VCO LDO Power Down	00h	R/W
052	*Rx Analog Power Down Override 1*	Rx Offset DAC CGin Power Down<1:0>		Rx LMT Overload Power Down<1:0>		Rx Mixer Gm Power Down<1:0>		Rx CGB Power Down<1:0>		03h	R/W
053	*Rx Analog Power Down Override 2*	Rx BBF Power Down<1:0>		Rx TIA Power Down<1:0>		Rx Mixer Power Down<1:0>		Rx Offset DAC CGOut Power Down<1:0>		00h	R/W
054	*Rx1 ADC Power Down Override*	Rx1 ADC Power Down<7:0>								00h	R/W
055	*Rx2 ADC Power Down Override*	Rx2 ADC Power Down<7:0>								00h	R/W
056	*Tx Analog Power Down Override 1*	Tx Secondary Filter Power Down<1:0>		Tx BBF Power Down<1:0>		Tx DAC Power Down<1:0>		Tx DAC Bias Power Down<1:0>		00h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
057	*Analog Power Down Override*	Open		Rx Ext VCO Buffer Power Down	Tx Ext VCO Buffer Power Down	Tx Monitor Power Down<1:0>		Tx Upconverter Power Down<1:0>		3Ch	R/W
058	*Misc Power Down Override*		Rx LNA Power Down	Open		Rx Calibration Power Down<1:0>		DCXO Power Down	Master Bias Power Down	30h	R/W

SPI Register 0x050—Rx Synth Power Down Override

[D4] Rx LO Power Down Setting this bit powers down the Rx LO dividers if MCS RF is disabled (0x001[D3]=0). If MCS RF is enabled, the AD9361 state machine (see register 0x015) enables and disables the Rx LO dividers. This state machine also enables and disables the Rx synthesizer. Thus, if D4 is set and MCS RF is enabled, the Rx LO dividers power up and down when the Rx synthesizer powers up and down. This bit applies to both external VCO and internal VCO operation (the Rx LO dividers are always powered down for external VCO operation).

[D3] Rx ALC Power Down Setting this bit powers down the Rx synthesizer VCO automatic level control.

[D2] Rx Synth PTAT Power Down Test bit. The PTAT is a temperature-compensated current used for the Rx synthesizer. This bit is ORed with the NOT of 0x242[D4:D3]. To turn off PTAT, set 0x050[D2] and clear 0x242[D4:D3]. The synth can still operate but it will not be temperature-compensated.

[D1] Rx Synth VCO Power Down Setting this bit powers down the Rx synthesizer VCO.

[D0] Rx Synth VCO LDO Power Down Setting this bit powers down the Rx synthesizer VCO LDO.

SPI Register 0x051—Tx Synth Power Down Override

Same as 0x050 but controls the transmitter LO circuits.

SPI Register 0x052—Rx Analog Power Down Override 1

[D7:D6] Rx Offset DAC CGin Power Down<1:0> Test bits, normally cleared. The CGin DAC is used for calculating Baseband DC offset at the input of the Common Gate Buffer (CGB) that feeds the TIA. The BB DC offset cal algorithm automatically uses the correct DC offset DAC (this one or the CGout DAC) depending on whether the CGB is on or off.

[D5:D4] Rx LMT Overload Power Down<1:0> Test bits. Setting these bits powers down the LMT overload detectors used by the gain control circuit. Bit D4 applies to Rx1 and bit D5 applies to Rx2.

[D3:D2] Rx Mixer Gm Power Down<1:0> Test bits. Setting these bits powers down the Rx mixer Gm. Bit D2 = Rx1 and bit D3 = Rx2.

[D1:D0] Rx CGB Power Down<1:0> These bits power down the Common Gate Buffer that feeds the TIA. Powering up the CGB reduces the flicker noise corner for certain applications. Normally, the CGB is powered down. Bit D0 affects Rx1 and bit D1 affects Rx2.

SPI Register 0x053—Rx Analog Power Down Override 2—Test Registers Only—Do not change these bits

[D7:D6] Rx BBF Power Down<1:0> Setting these bits powers down the Rx low pass baseband filters. Bit D6=Rx1 and bit D7=Rx2.

[D5:D4] Rx TIA Power Down<1:0> Setting this bit powers down the receive TIA. Bit D4 applies to Rx1 and bit D5 applies to Rx2.

[D3:D2] Rx Mixer Power Down<1:0> Setting this bit powers down the receive mixers. Bit D2 applies to Rx1 and bit D3 applies to Rx2.

[D1:D0] Rx OffsetDAC CGOut Power Down<1:0> See register 0x052[D7:D6]. This register affects the offset DAC at the output of the CGB.

SPI Registers 0x054 & 0x055—Rx1 and Rx2 ADC Power Down—Test mode only—do not change these bits

These registers control the receive ADCs. The only valid settings are 0x00 (ADC on) and 0xFF (ADC off).

SPI Register 0x056—Tx Analog Power Down Override 1—Test mode only—do not change these bits

[D7:D6] Tx Secondary Filter Power Down<1:0.> Setting these bits powers down the Tx secondary filter. Bit D6=Tx1 and bit D7=Tx2.

[D5:D4] Tx BBF Power Down<1:0> Setting these bits powers down the Tx baseband low pass filters. Bit D4=Tx1 and bit D5=Tx2.

[D3:D2] Tx DAC Power Down<1:0> Setting these bits powers down the Tx DACs. Bit D2 applies to Tx1 and bit D3 applies to Tx2.

[D1:D0] Tx DAC Bias Power Down<1:0> Setting these bits powers down the Tx DAC bias supplies. Bit D0=Tx1 and bit D1=Tx2.

SPI Register 0x057—Analog Power Down Override

[D5] Rx Ext VCO Buffer Power Down Clear this bit to use an external VCO instead of the internal VCO.

[D4] Tx Ext VCO Buffer Power Down Same as bit D5 but applies to the Tx VCO.

[D3:D2] Tx Monitor Power Down<1:0> Setting these bits powers down the Tx monitor circuit. Bit D2=Tx Mon1 and bit D3=Tx Mon 2. These bits are set by default. Clear the bits to use the Tx Monitor function.

[D1:D0] Tx Upconverter Power Down<1:0> Setting these bits powers down the Tx upconverters. Bit D0=Tx1 and bit D1=Tx2.

SPI Register 0x058—Misc Power Down Override

[D6] Rx LNA Power Down Test bit. Setting this bit powers down the Rx LNAs.

[D3:D2] Rx Calibration Power Down Test bits. Setting these bits powers down the Rx calibration blocks. Bit D3=Rx1 and bit D4=Rx2.

[D1] DCXO Power Down Set this bit when using an external reference clock to save power.

[D0] Master Bias Power Down Test bit. Setting this bit powers down all analog bias. Only leakage current will flow.

OVERFLOW REGISTERS 05E THROUGH 05F

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
05E	*CH 1 Overflow*	BBPLL Lock	CH 1 INT3	CH1 HB3	CH1 HB2	CH1 QEC	CH1 HB1	CH1 TFIR	CH1 RFIR	-	R
05F	*CH 2 Overflow*	Open	CH2 INT3	CH2 HB3	CH2 HB2	CH2 QEC	CH2 HB1	CH2 TFIR	CH2 RFIR	-	R

Note that none of the overload bits self-clears. During initialization, some of these overload bits may register overloads. To read the current status of the overload bits, perform two consecutive SPI Reads.

SPI Register 0x05E—CH 1 Overflow

[D7] BBPLL Lock If this bit is set, the BBPLL is locked.

[D6] INT3 If this bit is set, a digital overflow occurred in the Tx 1 interpolate by 3 filter.

[D5] HB3 If this bit is set, a digital overflow occurred in the Tx 1half-band 3 filter.

[D4]HB2 If this bit is set, a digital overflow occurred in the Tx 1 half-band 2 filter.

[D3]QEC If this bit is set, a digital overflow occurred in the Tx1 quadrature error correction filter.

[D2]HB1 If this bit is set, a digital overflow occurred in the Tx 1 half-band 1 filter.

[D1]TFIR If this bit is set, a digital overflow occurred in the Tx 1 FIR filter.

[D0]RFIR If this bit is set, a digital overflow occurred in the Rx 1 FIR filter.

SPI Register 0x05F—CH 2 Overflow

Same as register 05E but applies to Channel 2.

TRANSMITTER CONFIGURATION

TX PROGRAMMABLE FIR FILTER REGISTERS 060 THROUGH 065

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
060	*TX Filter Coefficient Address*	TX Filter Coefficient Address<7:0>								--	R/W
061	*TX Filter Coefficient Write Data 1*	TX Filter coefficient Write Data <7:0>								--	R/W
062	*TX Filter Coefficient Write Data 2*	TX Filter coefficient Write Data <15:8>								--	R/W
063	*TX Filter Coefficient Read Data 1*	TX Filter coefficient Read Data<7:0>								--	R
064	*TX Filter Coefficient Read Data 2*	TX Filter coefficient Read Data<15:8>								--	R
065	*TX Filter Configuration*	Number of Taps<2:0>			Select Tx CH<1:0>		Write Tx	Start Tx Clock	Filter Gain	00h	R/W

SPI Register 0x060—Tx Filter Coefficient Address

The digital filter coefficients are indirectly addressable. This register represents the indirect address of the coefficient.

SPI Registers 0x061 and 0x062—Tx Filter Coefficient Data 1& 2

When writing coefficients of a digital filter, write the coefficient value to these registers. Write these registers (along with register 0x060) before setting bit D2 of 0x065. Coefficients are 16-bit words in 2's complement format. The least significant bit is bit 0.

SPI Registers 0x063 and 0x064—Tx Filter Coefficient Read Data 1 & 2

When reading the filter coefficients, writ e the address in 0x060, write register 0x065 to start the programming clock and then read register 0x063 and 0x064. Coefficients are 16-bit words in 2's complement format. The least significant bit is bit 0.

SPI Register 0x065—Tx Filter Configuration

[D7:D5] Number of Taps<2:0> The number of taps (described by Equation 15) must be correct.

$$\#\,Taps = 16 * (Number\ of\ Taps + 1)$$

Equation 15

[D4:D3]Select Tx CH<1:0> When writing coefficients, bit D3 causes a write to Tx1, bit D4 causes a write to Tx2 and both bits set writes to both Tx filters. When reading coefficients, setting both bits is invalid.

[D2] Write Tx Set this self-clearing bit to write a coefficient. Each write operation must set this bit. After the table has been programmed, write to register 0x065 with the Write Tx bit cleared but the Start Tx Clock bit high. Then, write to 0x065 again, clearing the clock start bit. This ensures that the write bit resets internally before the clock stops. The filter table requires 4 Tx sample periods after "Write Tx" goes high for the value to write into the table. A small wait period may be necessary between consecutive writes.

[D1] Start Tx Clock Set this bit to start the programming clock. Only run the clock when writing or reading coefficients.

[D0] Filter Gain Setting this bit attenuates the digital samples by 6dB.

TX MONITOR REGISTERS 067 THROUGH 071

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
067	*Tx Mon Low Gain*	Open		Tx Mon Track	Tx Mon Low Gain<4:0>					13h	R/W
068	*Tx Mon High Gain*	Open			Tx Mon High Gain<4:0>					18h	R/W
069	*Tx Mon Delay*	Tx Mon delay counter<7:0>								00h	R/W
06A	*Tx Level Threshold*	Tx Level Threshold<5:0>						Tx Mon Delay Counter<9:8>		00h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
06B	*TX RSSI1*	Tx RSSI 1<8:1>								--	R
06C	*TX RSSI2*	Tx RSSI 2<8:1>								--	R
06D	*TX RSSI LSB*	Open						Tx RSSI 2<0>	TX RSSI 1<0>	--	R
06E	*TPM Mode Enable*	Set to 0	One Shot Mode	Set to 0	Open	Tx Mon Duration<3:0>				08h	R/W
06F	*Temp Gain Coefficient*	Temp Gain Coefficient<7:0> for Tx Mon								00h	R/W
070	*Tx Mon 1 Config*	Tx Mon 1 LO CM<5:0>						Tx Mon 1 Gain<1:0>		c1h	R/W
071	*Tx Mon 2 Config*	Tx Mon 2 LO CM<5:0>						Tx Mon 2 Gain<1:0>		c1h	R/W

The AD9361 can determine TxRSSI by measuring the signals on the Tx Mon 1 and Tx Mon 2 pins by using some of the Rx circuitry.

SPI Register 0x067--Tx Mon LowGain

[D5] Tx Mon Track Setting this bit enables the DC Offset tracking algorithm for the Tx monitor inputs.

[D4:D0] Tx Mon Low Gain. In conjunction with register 0x078, this register and 0x068[D4:D0] set the receive Low Pass Filter gain index to the value in these registers. Both Tx Monitor inputs use the same threshold, high gain, and low gain values. When the receiver uses the low gain setting, the AD9361 also sets TIA gain low. Conversely, when the receiver uses the high gain setting, the AD9361 automatically sets the TIA gain high. The TxRSSI function automatically compensates for these gain changes.

SPI Register 0x068—Tx Mon High Gain

See Tx Mon Low Gain in 0x067[D4:D0].

SPI Register 0x069—Tx Mon Delay

Ignored if D6 and D5 of 0x001 are clear. After the ENSM enters the Tx state, the TxRSSI block checks the Tx Level Threshold in 0x06A[D7:D2]. If this threshold = 0, then the Tx Mon Delay Counter starts. If the Tx Level Threshold in -0x06A[D7:D2] is non zero, then the AD9362 compares the 6 MSBs of the I and Q samples with the threshold in 0x06A[D7:D2]. If that threshold is exceeded, the Tx Mon Delay counter starts. Once the counter expires, the AD9362 performs TxRSSI measurements. The 10-bit wide counter also uses 0x06A[D1:D0]. Units = ADC clocks. 64 *ADC clocks/LSB.

SPI Register 0x06A—Tx Level Threshold

[D7:D2] Tx Level Threshold<5:0> See register 0x69.

[D1:D0] Tx Mon Delay Counter<9:8> The two most significant bits of the counter in 0x069.

SPI Registers 0x06B through 0x06D—Tx RSSI 1&2

Tx RSSI words. Resolution = 0.25dB/LSB. Units: -dBFS.

SPI Register 0x06E—TPM Mode Enable

[D6] One Shot Mode If this bit is set, the AD9361 performs one TxRSSI measurement when the ENSM enters the Tx state. If the bit is clear, the AD9361 continuously measures TxRSSI until the ENSM exits the Tx state.

[D3:D0] Tx Mon Duration<3:0> This register specifies the duration of the Tx RSSI measurement per Table 15.

Tx Mon Duration<3:0>	Rx Sample Cycles
0	16
1	32
2	64

3	128
4	256
5	512
6	1024
7	2048
8	4096
9	8192

Table 15.Tx Monitor Measurement Duration

SPI Register 0x06F—Temp Gain Coefficient<7:0> for Tx Mon

This value would be measured during system characterization and represents the Tx monitor path dependence on temperature. A ratio of gain difference per ° C would be determined and then coded in 2's complement notation to this register. Resolution = 0.0078dB/°C/LSB.

SPI Register 0x070 & 0x071—Tx Mon 1(2) Config

[D7:D2] Tx Mon LOCM<5:0> These bits set the common mode of the Tx monitor LO per Equation 16.

$$LO\ CM = \frac{Vdd*(Tx\ Mon\ LO\ CM<5:0> + 1)}{64}$$

Equation 16

[D1:D0] Tx Mon Gain<1:0> These bits control the Tx monitor front-end gain, per Table 16.

Tx Mon Gain<1:0>	Tx Monitor Gain
00	Open
01	0dB
10	6dB
11	9.5dB

Table 16. Tx Monitor Gain

TX POWER CONTROL & ATTENUATION REGISTERS 073 THROUGH 081

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
073	*Tx1 Atten 0*	Tx1 Attenuation<7:0>								00h	R/W
074	*Tx1 Atten 1*	Open							Tx 1 Atten <8>	00h	R/W
075	*Tx2 Atten 0*	Tx2 Attenuation<7:0>								00h	R/W
076	*Tx2 Atten 1*	Open							Tx 2 Atten <8>	00h	R/W
077	*Tx Atten Offset*	Open	Mask Clr Atten Update	Tx Atten Offset<5:0>						40h	R/W
078	*Tx Atten Threshold*	Tx Atten Thresh<7:0>								3ch	R/W
079	*Tx1 Dig Attenuation*	Open	Sel Tx1 & Ttx2	TPC Mode Tx1	Tx1 Digital Attenuation<4:0>					00h	R/W
07A	*Tx1 LO/HP Atten*	Tx1 LO Atten<1:0>		Tx1 HP Atten<5:0>						00h	R/W
07B	*Tx1 LP Atten*	Tx1 LP Atten<7:0>								00h	R/W
07C	*Tx2 Dig Attenuation*	Open	Immediately Update TPC Atten	TPC Mode Tx2	TX2 Digital Attenuation<4:0>					00h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
07D	*Tx2 LO/HP Atten*	Tx2 LO Atten<1:0>		Tx2 HP Atten<5:0>						00h	R/W
07E	*Tx2 LP Atten*	Tx2 LP Attenuation<7:0>								00h	R/W
07F	*TX1 Symbol Attenuation*	Open	Tx 1 Symbol Attenuation<6:0>							00h	R/W
080	*TX2 Symbol Attenuation*	Open	Tx 2 Symbol Attenuation<6:0>							00h	R/W
081	*TX Symbol Atten Config*	Open				Use Tx1 Pin & Symbol Atten	Open	Use CTRL IN for symbol Atten	Enable Symbol Atten	00h	R/W

SPI Registers 0x073 & 0x074—Tx1 Atten<8:0>

This 9-bit word sets the Tx path attenuation. A value of zero = zero attenuation. Resolution = 0.25dB/LSB. Valid range = 0 to 359 (d).

SPI Registers 0x075 & 0x076—Tx2 Atten<8:0>

Same as registers 0x073 & 0x074 but applies to Tx2 signal path.

SPI Register 0x077—Tx Atten Offset<5:0>

[D6] Mask Clr Atten Update When clear, the Immediate Update Bit in 0x07C[D6] self-clears. In this case, each time the Tx Atten word is updated, the immediate update bit needs to be set to make the change take effect. If Mask Clr Atten Update is set, then the Immediate Update Bit does not self-clear. If it is set, if the TxAtten word changes, the transmit power will update immediately.

[D5:D0] Tx Atten Offset<5:0> This non-signed value adds to the attenuation words in 0x073 through 0x076, resulting in new attenuation words. Resolution = 0.25dB/LSB.

SPI Register 0x078—Tx Atten Threshold

Only used with the Tx Monitor function. If the Tx Atten setting is above this threshold, the high gain index value is used in the Tx monitor path. If the Tx Atten value is equal to or less than this threshold, then the low gain index value is used. Registers 0x067 and 0x068 hold the low and high gain indices. The threshold is common to both Tx monitor inputs but the code that compares the threshold to the attenuation is separate for Tx Mon1 and Tx Mon2. For example, Tx Mon1 may be using the high gain value but Tx Mon 2 may be using the low gain setting. The resolution = 0.25dB/LSB.

SPI Register 0x079—Tx1 Dig Attenuation

[D6] Sel Tx1 & Tx2 Use the Tx1 attenuation value for both Tx1 and Tx2.

SPI Register 0x07C —Tx 2 Dig Attenuation

[D6] Immediately Update TPC Atten See 0x077[D6].

SPI Register 0x07F through 0x081 Symbol Attenuation

Not recommended for use. To change Tx attenuation, use registers 0x073 through 0x076.

TX QUADRATURE CALIBRATION PHASE, GAIN, AND OFFSET CORRECTION REGISTERS 08E THROUGH 09F

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
08E	*Tx1 Out 1 Phase Corr*	Tx1 Output 1 Phase Correction<7:0>								--h	R/W
08F	*Tx1 Out 1 Gain Corr*	Tx1 Output 1 Gain Correction<7:0>								--h	R/W
090	*Tx2 Out 1 Phase Corr*	Tx2 Output 1 Phase Correction<7:0>								--h	R/W
091	*Tx2 Out 1 Gain Corr*	Tx2 Output 1 Gain Correction<7:0>								--h	R/W
092	*Tx1 Out 1 Offset I*	Tx1 Output 1 Offset I<7:0>								--h	R/W
093	*Tx1 Out 1 Offset Q*	Ttx1 Output 1 Offset Q<7:0>								--h	R/W
094	*Tx2 Out 1 Offset I*	Tx2 Output 1 Offset I<7:0>								--h	R/W
095	*Tx2 Out 1 Offset Q*	Tx2 Output 1 Offset Q<7:0>								--h	R/W
096	*Tx1 Out 2 Phase Corr*	Tx1 Output 2 Phase Correction<7:0>								--h	R/W
097	*Tx1 Out 2 Gain Corr*	Tx1 Output 2 Gain Correction<7:0>								--h	R/W
098	*Tx2 Out 2 Phase Corr*	Tx2 Output 2 Phase Correction<7:0>								--h	R/W
099	*Tx2 Out 2 Gain Corr*	Tx2 Output 2 Gain Correction<7:0>								--h	R/W
09A	*Tx1 Out 2 Offset I*	Tx1 Output 2 Offset I<7:0>								--h	R/W
09B	*Tx1 Out 2 Offset Q*	Ttx1 Output 2 Offset Q<7:0>								--h	R/W
09C	*Tx2 Out 2 Offset I*	Tx2 Output 2 Offset I<7:0>								--h	R/W
09D	*Tx2 Out 2 Offset Q*	Tx2 Output 2 Offset Q<7:0>								--h	R/W
09e	*Open*	Open								--	
09F	*Force Bits*	Force Out 2 Tx2 Offset	Force Out 2 Tx1 Offset	Force Out 2 Tx2 Phase & Gain	Force Out 2 Tx1 Phase & Gain	Force Out 1 Tx2 Offset	Force Out 1 Tx1 Offset	Force Out 1 Tx2 Phase & Gain	Force Out 1 Tx1 Phase & Gain	00h	R/W

SPI Register 0x08E—Tx1 Out 1 Phase Corr

If 0x09F[D0] is clear, after a Tx Quad Cal has completed, this register holds the phase correction word for Output 1 of Tx1. See register 0x004[D6] for Output 1 vs. Output 2 settings. Coding is 2's complement with an approximate range of ±tan(7°). If 0x09F[D0] is set, the value written to this register is used as the phase correction word.

SPI Register 0x08F—Tx1 Out 1 Gain Corr—Test Register—Do not change these bits

If 0x09F[D0] is clear, after a Tx Quad Cal has completed, this register holds the gain correction word for Output 1 of Tx1. See register 0x004[D6] for Output 1 vs. Output 2 settings. Coding is 2's complement with an approximate range of ±0.5dB. If 0x09F[D0] is set, the value written to this register is used as the gain correction word.

SPI Register 0x090—Tx2 Out 1 Phase Corr-- Test Register—Do not change these bits

Same as 0x08E but applies to Tx2 and the force bit is 0x09F[D1].

SPI Register 0x091—Tx2 Out 1 Gain Corr-- Test Register—Do not change these bits

Same as register 0x08F but applies to Tx2 and the force bit is 0x09F[D1].

SPI Register 0x092—Tx 1 Out 1 Offset I-- Test Register—Do not change these bits

If 0x09F[D2] is clear, after a Tx Quad Cal has completed, this register holds the DC offset correction word for I signal path of Output 1 of Tx1. See register 0x004[D6] for Output 1 vs. Output 2 settings. 2's complement coded. If 0x09F[D2] is set, the value written to this register is used as the DC offset correction word.

SPI Register 0x093—Tx1 Out 1 Offset Q-- Test Register—Do not change these bits

Same as 0x092 but applies to the Q signal path.

SPI Register 0x094—Tx2 Out 1 Offset I-- Test Register—Do not change these bits

Same as register 0x092 but applies to Tx2 and the force bit is 0x09F[D3].

SPI Register 0x095—Tx2 Out 1 Offset Q-- Test Register—Do not change these bits

Same as register 0x092 but applies to the Q signal path of Tx2 and the force bit is 0x09F[D3].

SPI Register 0x096—Tx1 Out 2 Phase Corr-- Test Register—Do not change these bits

Same as register 0x08E but applies to Output 2 and the force bit is 0x09F[D4].

SPI Register 0x097—Tx1 Out 2 Gain Corr-- Test Register—Do not change these bits

Same as register 0x08F but applies to Output 2 and the force bit is 0x09F[D4].

SPI Register 0x098—Tx2 Out 2 Phase Corr-- Test Register—Do not change these bits

Same as register 0x08E but applies to Output 2 of Tx2 and the force bit is 0x09F[D5].

SPI Register 0x099—Tx2 Out 2 Gain Corr-- Test Register—Do not change these bits

Same as register 0x08F but applies to Output 2 of Tx2 and the force bit is 0x09F[D5].

SPI Register 0x9A—Tx1 Out 2 Offset I

Same as register 0x092 but applies to Output 2 and the force bit is 0x09F[D6].

SPI Register 0x09B—Tx1 Out 2 Offset Q-- Test Register—Do not change these bits

Same as register 0x092 but applies to the Q signal path of Output 2 and the force bit is 0x09F[D6].

SPI Register 0x09C—Tx2 Out 2 Offset I-- Test Register—Do not change these bits

Same as register 0x092 but applies to Output 2 of Tx2 and the force bit is 0x09F[D7].

SPI Register 0x09D—Tx2 Out 2 Offset Q-- Test Register—Do not change these bits

Same as register 0x092 but applies to the Q signal path of Output 2 of Tx2 and the force bit is 0x09F[D7].

SPI Register 0x09F—Force Bits-- Test Register—Do not change these bits

These bits force the values in registers 0x08E through 0x09D to be the Tx Quadrature Calibration correction words.

TX QUADRATURE CALIBRATION CONFIGURATION REGISTERS 0A0 THROUGH 0AE

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0A0	*Quad Cal NCO Freq & Phase Offset*	open	Rx NCO Frequency<1:0>		Rx NCO Phase Offset<4:0>					0Ch	R/W
0A1	*Quad Cal Control*	Free Run Enable	Settle Main Enable	DC Offset Enable	Gain Enable	Phase Enable	Quad Cal Soft Reset	M<1:0>		78h	R/W
0A2	*Kexp 1*	Kexp Tx<1:0>		Kexp Tx_comp <1:0>		Kexp DC I <1:0>		Kexp DC Q <1:0>		1Fh	R/W
0A3	*Kexp 2*	Tx NCO frequency<1:0>		Invert I data	Invert Q data	Kexp Phase <1:0>		Kexp Amp <1:0>		00h	R/W
0A4	*Settle count*	Settle Count<7:0>								10h	R/W
0A5	*Mag. Ftest Thresh*	Mag Ftest Thresh<7:0>								06h	R/W
0A6	*Mag. Ftest Thresh 2*	Mag Ftest Thresh2<7:0>								06h	R/W
0A7	*Quad cal status Tx1*	Tx1 Convergence Count<5:0>						Tx1 LO Conv	Tx1 SSB Conv	--	R
0A8	*Quad cal status Tx2*	Tx2 Convergence Count<5:0>						Tx2 LO Conv	Tx2 SSB Conv	--	R
0A9	*Quad cal Count*	Quad Cal Count<7:0>								20h	R/W
0AA	*Tx Quad Full/LMT Gain*	Open	RX Full table/LMT table gain<6:0>							0Ah	R/W
0AB	*Squarer Config*	Open		Gm Stage Time Con Override	Gm Stage MV HP Pole	Gm Stage Lower CM	Vbias Control<1:0>		Bypass Bias R	00h	R/W
0AC	*TX Quad Cal Atten*	TX quad Cal Atten Word<7:0>								00h	R/W
0AD	*Thresh Accum*	Open				Threshold Accumulator<3:0>				00h	R/W
0AE	*Tx Quad LPF Gain*	Open			RX LPF gain<4:0>					18h	R/W

SPI Register 0x0A0—Quad Cal NCO Freq & Phase Offset

[D6:D5] Rx NCO Frequency<1:0> This value sets the test frequency, per Equation 17, for the Rx path that processes the Tx test tone. The Rx NCO frequency should equal the Tx NCO frequency (0x0A3[D7:D6]). If ClkRF and ClkTF are equal, then the Rx NCO bits and the Tx NCO bits should be equal. For the default value of zero, M (0x0A1[D1:D0]) can't be zero. Both values zero makes the loop unstable because the decimate and dump function will only get a portion of a cycle, leading to incorrect error values.

$$Rx\ NCO\ Test\ Frequency = \frac{ClkRF * (Rx\ NCO\ Frequency < 1:0 > + 1)}{32}$$

Equation 17

[D4:D0] Rx NCO Phase Offset<4:0> This register compensates for the delay of the test signal through the signal path. It is affected by the digital receive filter settings in 0x003.

SPI Register 0x0A1—Quad Cal Control

[D7] Free Run Enable When this bit is clear, the Tx Quad Cal runs until the algorithm reduces the errors below the thresholds in registers 0x0A5 and 0x0A6 or, if those thresholds are not met, the cal runs for the time set by the "Quad Cal Count" (0x0A9) value. This "timeout" mode forces the algorithm to finish. If the bit is set, the algorithm will not finish until (or if) it meets the thresholds.

[D6] Settle Main Enable Test bit, normally set. When set, after the Rx NCO phase updates, the algorithm will run after the "Settle Counter" (0x0A4) decrements to zero. Clearing this bit allows the calibration to begin immediately after the Rx NCOs updates.

[D5] DC Offset Enable Normally set. When set, a Tx Quad Cal performs a DC offset correction. Clearing the bit disables this correction.

[D4] Gain Enable Normally set. When set, a Tx Quad Cal performs a gain offset correction. Clearing this bit disables this correction.

[D3] Phase Enable Normally set. When set, a Tx Quad Cal performs a phase offset correction. Clearing this bit disables this correction.

[D2] Quad Cal Soft Reset Normally cleared. Setting this bit resets the Tx Quad Cal state machine.

[D1:D0] M<1:0> These bits control the decimation used by the accumulate and dump block and the corresponding scaling of the Tx Quad Cal algorithm. Decimation = 16 * 2^M<1:0>. If 0x0A0[D6:D5] = 0, M cannot be zero.

SPI Register 0x0A2—Kexp1

0x78[D7:D6] Kexp Tx<1:0> These bits control the Tx test waveform power during quadrature calibration.

Kexp Tx	Bit Shift	dB Gain
0	>>1	-6dB
1	>>2	-12dB
2	>>3	-18dB
3	>>4	-24dB

Table 17. Kexp Tx vs. Linear Gain for Tx Quad Cal

0x78[D5:D4] Kexp Tx Comp<1:0> These bits perform an inverse scaling on the received magnitudes so that the Tx scaling does not directly affect the convergence of the algorithms. This function also can adjust the overall convergence of all the loops.

Kexp Tx Comp	Bit Shift	dB Gain
0	<<1	+6dBFS
1	<<2	+12dBFS
2	<<3	+18dBFS
3	<<4	+24dBFS

Table 18. Kexp Tx Comp vs. dB Gain

[D3:D2] Kexp DC I<1:0> These bits control Tx Quadrature Calibration loop gain and thus the rate of convergence for the I path per the table below. Higher values take more time to converge.

Kexp	Bit Shift	Linear Gain
0	>>0	¼
1	>>1	1/8
2	>>2	1/16
3	>>3	1/32

Table 19. Kexp DC vs. dB Gain

[D1:D0] Kexp DC Q<1:0> Same as [D3:D2] but applies to the quadrature signal path.

SPI Register 0x0A3--Kexp 2

[D7:D6] Tx NCO Frequency<1:0> This register sets the frequency of the test waveform per Equation 18.

$$Tx\ Quadrature\ Calibration\ Test\ Frequency = \frac{ClkTF * (Tx\ NCO\ Frequency < 1:0 > + 1)}{32}$$

Equation 18

Where:

ClkTF is the clock rate at the output of the transmit FIR filter

[D5] Invert I Data Setting this bit inverts the I data in the test waveform.

[D4] Invert Q Data Setting this bit inverts the Q data in the test waveform

[D3:D2] Kexp Phase<1:0> This factor controls the loop gain of the Tx Quadrature Calibration algorithm per table 19 and thus the rate of convergence. Higher values take more time to converge.

[D1:D0] Kexp Amp<1:0> Same as [D3:D2] but applies to the exponent amplitude.

SPI Register 0x0A4—Settle Count

This counter stalls the digital measurement and convergence algorithm while the analog loop settles. It must be high enough such that the DC offset from the squarer servo loop is removed and the amplitude/phase of the test tones is frequency stable.

SPI Registers 0x0A5 and 0x0A6--Mag Ftest Thresh and Mag Ftest Thresh2

These are the thresholds for the LO leakage and the Quadrature Correction. When the magnitudes of ftest 2ftest tone are both below their respective thresholds then the Calibration is complete. Ftest (0x0A5) corresponds to carrier feedthrough and Ftest2 (0x0A6) corresponds to undesired SSB rejection. Both tests run simultaneously.

SPI Registers 0x0A7 and 0x0A8 Quad Cal Status Tx1 and Tx2—Test Register

[D7:D2] Convergence Count<5:0> These bits indicate the duration of the Tx Quadrature Calibration. Higher values = longer duration.

[D1] LO Conv If this bit equals one, the carrier feedthrough algorithm reduced feedthrough below the threshold in 0x0A5. If the bit is clear after running the calibration, the loop did not converge.

[D0] SSB Conv If this bit equals one, the undesired SSB algorithm reduced the SSB below the threshold in 0x0A6. If the bit is clear after running the calibration, the loop did not converge.

SPI Register 0x0A9--Quad Cal Count

If the "Free Run Enable" bit in 0x0A1[D7] is clear, this register sets the maximum time that the Tx Quad Cal algorithm can run. See the Calibration User Guide for more details. If the Free Run Enable bit is set, Quad Cal Count is ignored.

SPI Register 0x0AA—Tx Quad Full/LMT Gain

The AD9361 uses some of the Rx signal path when performing a Tx Quad Cal and this register sets the Rx gain for the calibration. If the receivers are using the Full Table mode for gain control, then this register specifies the gain index. If the receivers are using the Split Table mode for gain control, then this register specifies the gain index of the LMT Table and register 0x0AE specifies the gain index of the Low Pass Filter (LPF) Table. See bit D3 of 0x0FB for an explanation of the Gain Table modes.

SPI Register 0x0AB—Squarer Config

[D5]Gm Stage Time Con Override Test bit, normally clear. There is a delay block on power down/enable, which allows charge up of the gm stage input bias. Setting this bit bypasses the delay block so that there is no pre-charge available.

[D4]Gm Stage MV HP Pole. Test bit, normally clear. Setting this bit moves the high pass portion of the squarer output bandpass filter out by a factor of 3.

[D3]Gm Stage Lower CM Test bit, normally clear. If this bit is clear, the Gm output CM Voltage = 660mV else CM voltage = 615mV.

[D2:D1]Vbias Control<1:0> The DC bias for the squarer top pair is based on a "battery" above the lower pair bias. If a headroom issue arises, the bias voltage can be modified per Table 20.

Vbias Control<1:0>	Bias Voltage (mV)
00	400 (default)
01	350
10	300
11	Invalid

Table 20. Squarer Vbias Control

[D0]Bypass Bias R This bit bypasses the upper and lower pair bias filter resistors and should be "0" under normal conditions.

SPI Register0x 0AC—Tx Quad Cal Atten

This register specifies the value of Tx Attenuation during Tx Quad Cal, overrides 0x073 through 0x076 and has a resolution of 0.5dB/LSB.

SPI Register 0x0AD—Thresh Accum

This is the number of times + 1 that the Ftest and 2*Ftest tones must be below their respective thresholds for the calibration routine to complete.

SPI Register0x 0AE—Tx Quad LPF Gain

Only applies if the Receive Split Gain Table is used. See register 0x0AA.

TX DAC REGISTERS 0B0 THROUGH 0B3

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0B0	*TxDAC Vds I*	Open		TxDAC Vds I<5:0>						00h	R/W
0B1	*TxDAC Vds Q*	Open		TxDAC Vds Q<5:0>						00h	R/W
0B2	*TxDAC gn I*	Open		txDAC_gn_I<5:0>						00h	R/W
0B3	*TxDAC gn Q*	Open		txDAC_gn_Q<5:0>						00h	R/W

SPI Register 0x0B0 and 0x0B1—TxDAC Vds I(Q)

These registers control the Vds bias trim for the I and Q current source arrays per Table 21. The FET voltage can vary from 2.883 to 483.6mV with a 3.1mV/LSB resolution. The nominal value of 387.5mV occurs at the default register setting of 0x00.

TxDAC Vds I(Q)<5:0>	*Current Source Vds (mV)*
111111	*384.4*
111110	*381.1*
…	…
100001	*291.4*
100000	*288.3*
011111	*483.6*
011110	*480.1*
…	…
000001	*390.6*
000000	387.5

Table 21.TxDAC Bias

SPI Register 0x0B2 and 0x0B3—TxDAC gn I(Q)

These registers control the full-scale current of the I and Q TxDACs per Table 22. The full scale output current of the each DAC can be varied from 0.744mV to 1.248mV with an 8uA resolution. The nominal value of 1mA occurs when this register = 0x00.

gain_i/gain_q<5:0> Value	Full Scale Current (mA)
111111	0.992
111110	0.984
…	…
100001	0.752
100000	0.744
011111	1.248
011110	1.240
…	…
000001	1.008
000000	1.000

Table 22.TxDAC Full Scale Current

TX BASEBAND FILTER REGISTERS 0C0 THROUGH 0CC

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0C0	*TxBBF OpAmp A*	Open	OpAmpA Output Bias<1:0>		OpAmpA RZ<1:0>		OpAmp A CC<2:0>			6Fh	R/W
0C1	*TxBBF OpAmp B*	Open	OpAmpB Output Bias<1:0>		OpAmpB RZ<1:0>		OpAmp B CC<2:0>			EFh	R/W
0C2	*Tx BBF R1*	Override enable	Open		R1<4:0>					1Fh	R/W
0C3	*Tx BBF R2*	Open			R2<4:0>					1Fh	R/W
0C4	*Tx BBF R3*	Open			R3<4:0>					1Fh	R/W
0C5	*Tx BBF R4*	Open			R4<4:0>					1Fh	R/W
0C6	*Tx BBF RP*	Open			Rp<4:0>					1Fh	R/W
0C7	*Tx BBF C1*	Open		C1<5:0>						2Ah	R/W
0C8	*Tx BBF C2*	Open		C2<5:0>						2Ah	R/W
0C9	*Tx BBF Cp*	Open		Cp<5:0>						2Ah	R/W
0CA	*Tx Tune Control*	Open	Tune Control<1:0>		Open		PD Tune	Tuner Resample	Tuner Resample Phase	20h	R/W
0CB	*Tx BBF R2b*	Bypass Bias R	Open	R2b Ovr	R2b<4:0>					00h	R/W
0CC	*Tx BBF Tune*	Open				BBF1 Comp I	BBF1 Comp Q	BBF2 Comp I	BBF2 Comp Q	--	R

SPI Register 0x0C0—Tx BBF OpAmp A—Test Register

[D6:D5] OpAmpA Output Bias<1:0> Output stage bias current control word for the 1st OpAmp stage, mapped per Table 23.

OpAmp Output Bias<1:0>	Bias Current (uA)
00	200
01	300
10	400
11	500

Table 23.TxBBF OpAmpA Bias Current

[D4:D3]OpAmpA RZ<1:0> Zero control word in 1st OpAmp stage, mapped per Table 24.

OpAmpA Rz<1:0>	Resistance (Ohms)
0	1500
1	750
2	750
3	500

Table 24. TxBBF OpAmpA Zero Control

[D2:D0]OpAmpA CC<2:0> Compensation cap word in 1st OpAmp stage per Equation 19. Bits <2:0>="D2", "D1", and "D0" respectively.

$$Cc = 360 * D2 + 120 * D1 + 60 * D0 + 60\ fF$$
Equation 19

SPI Register 0x0C1—Tx BBF OpAmp B—Test Register

Same as register 0x0C0 but applies to the 2nd OpAmp.

SPI Registers 0x0C2 --Tx BBF R1-- Test Register

[D7] Override Enable Setting this bit forces the baseband filter to use the values written into registers 0x0C2 through 0c0CB.

[D4:D0] R1<4:0> R1 control word where $\mathrm{R1(k\Omega)} = \frac{129\mathrm{k\Omega}}{\mathrm{R1<4:0>+1}}$ Equation 20

SPI Registers 0x0C3 through 0x0C5—Tx BBF R2 through Tx BBF R4-- Test Registers

R2 through R4 control words. See 0x0C2[D4:D0] for resistance vs. register value encoding.

SPI Register 0x0C6—Tx BBF RP--Test Register

The real pole control word where $RP(kOhms) = \frac{24k\Omega}{RP<4:0>+1}$ Equation 21

SPI Register 0x0C7 and 0x0C8—Tx BBF C1 and C2—Test Registers

C1 and C2 control words where $Cx(fF) = 855 + 95 * Cx<5:0>$ *Equation 22*

SPI Register 0x0C9—Tx BBF CP-- Test Registers

Real Pole control word where $CP(fF) = 1125 + 125 * Cx<5:0>$ *Equation 23*

SPI Register 0x0CA—Tx Tune Control

[D6:D5] Tune Control<1:0> Sets the filter CM voltage reference. Two settings are valid: the default 0x01=700mV and 0x10 = 710mV.

[D2] PD Tune *Clear* this bit to force tuner (calibration circuit) on. If this bit is *set* the digital calibration state machine controls the power on/off state of the tuner. In this case, the state machine will enable the tuner for a calibration and then disable it afterwards. This mode is

not recommended. Instead, the Tx BBF calibration circuit should be manually powered up for calibration and then powered down after calibration. Specifically, to tune BBF, clear the PD Tune bit and allow analog path to settle. Tune BBF then set PD Tune bit.

[D1] Tuner Resample Test bit. Set to bypass resampler. Clear to resample to div 8. Bits D1 and D0 are for use only to correct unlikely synchronization issues between analog and digital.

[D0] Tuner Resampler Phase Test bit. Set to use div 8 bar to resample, clear to use div 8 to resample.

SPI Register 0x0CB—Tx BBF R2b-- Test Registers

[D7] Bypass Bias R Bypasses the bias filter resistor in the tuning circuit.

[D5] R2b Ovr This is a force bit but it only allows the R2b value to be forced. Use only if performing a manual calibration.

[D4:D0] R2b<4:0> R2b control word. See 0x0C2[D4:D0] for resistance vs. register value encoding.

SPI Register 0x0CC—Tx BBF Tune-- Test Registers

[D3] BBF1 Comp I The tuning algorithm starts with component values that yield a baseband bandwidth (BBW) that is too large and this bit goes high. When this bit goes low, the filter tuning algorithm has found component values that result in an appropriate bandwidth. There are four comp bits, one for each of the four filters. This bit corresponds to the "I" signal path in Tx1.

[D2] BBF1 Comp Q Same as [D3] but applies to the "Q" signal path.

[D1] BBF2 Comp I Same as [D3] but applies to Tx2.

[D0] BBF2 Comp Q Same as [D3] but applies to Tx2 "Q" signal path.

TX SECONDARY FILTER REGISTERS 0D0 THROUGH 0D3

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0D0	*Config0*	Bias<1:0>		Rgm<1:0>		Cc<1:0>		AmpBias<1:0>		55h	R/W
0D1	*Resistor*	Open				Resistor<3:0>				0Fh	R/W
0D2	*Capacitor*	Open		Capacitor<5:0>						1Fh	R/W
0D3	*LO CM*	Open	LO Common Mode<1:0>			Open				60h	R/W

This register provides filtering for Tx noise that is far out from the SOI. Typically set the filter corner to 5x the baseband (real) BW.

SPI Register 0x0D0—Config 0

[D7:D6] Bias<1:0> Secondary filter bias current set according to Table 25. Higher bias current results in higher SNR. In general, set these bits the same as bits D5:D4.

Bias<1:0>	Rgm<1:0>	Bias Current	Resistor Value (Ohms)
00	00	600uA	1040
01	01	1.2mA	520
10	10	2.4mA	260
11	11	4.8mA	130

Table 25. Secondary filter bias current

[D5:D4] Rgm<1:0> Rgm resistor. See table above.

[D3:D2] Cc<1:0> Compensation network for the amplifiers. Set per Table 26.

RF Bandwidth (RF BW)	Cc<1:0>	AmpBias<1:0>
≤9MHz	10	01
9 MHz < RF BW ≤ 24 MHz	01	10
> 24 MHz	01	11

Table 26. Secondary Filter Cc and Amp Bias

[D1:D0] AmpBias<1:0> These bits set amplifier bias current. Set per Table 26. Higher current equals lower noise and wider BW.

SPI Register 0x0D1—Resistor<3:0>

Secondary Filter resistor, which, along with "Capacitor", sets the 3dB, corner (see 0x0D2). Valid settings mapped per Table 27.

Resistor<3:0>	Post-Filter Stage Resistance (Ohms)
0001	800
0011	400
0100	200
1100	100

Table 27.Post Secondary Filter Stage Resistance

SPI Register 0x0D2—Capacitor<5:0>

Secondary Filter capacitor, which, along with "Resistor", sets the 3dB corner (see 0x0D1). Set "Capacitor" such that "Resistor" stays as low as possible. Resolution: 1pF/LSB. Total capacitance is 12pF + Capacitor<5:0> *1pF.

SPI Register 0x0D3—LO CM

[D6:D5] LO Common Mode<1:0> The LO common mode control is used to optimize linearity and is mapped per Table 28.

LOCM<1:0>	LO common mode (V)
00	0.8
01	0.88
10	0.95
11	1.02 (best performance)

Table 28.LO common mode voltage

TX BBF TUNER CONFIGURATION REGISTERS 0D6 THROUGH 0D7

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0D6	*TX BBF Tune Divider*	TX BBF Tune Divider<7:0>								12h	R/W
0D7	*TX BBF Tune Mode*	Open	Tune Comp Mask<1:0>		EvalTime	Tuner Mode<2:0>			TX BBF Tune Divider<8>	1Eh	R/W

SPI Register 0x0D6 (and 0x0D7[D0])

The Tx BBF uses an oscillator during calibration. The AD9361 derives the oscillator by dividing down the BBPLL per Equation 24. See the Calibration User Guide for more information about the tune clock used for the calibration algorithm.

$$Tx\ BBF\ Tune\ Divider = Ceil\left(\frac{BBPLL\ Frequency * ln(2)}{BBW * 3.2 * \pi}\right)$$

Equation 24

SPI Register 0x0D7—Tx BBF Tune Mode

[D6:D5] Tune Comp Mask<1:0> Test bits, normally 2'b00. These bits select which, if any, tune comparator output should be masked when evaluating tuning. 2'b00 uses both channels. 2'b01 masks Tx2. 2'b10 masks Tx1. 2'b11 is unused. It is not necessary to set these bits according to the receiver(s) that are enabled. All filters turn on during tuning so there is no need to mask the outputs.

[D4] EvalTime This bit sets the delay in tune clock cycles (set by the divider described above) before the tune comparator outputs are sampled. 0 = 16 cycles and 1 = 32 cycles.

[D3:D1] Tuner Mode<2:0> These bits determine how the filter tuning algorithm uses the comparator outputs when checking to see if the tuning algorithm should finish. Table 29 shows this relationship.

Tuner Mode<2:0>	Action

Tuner Mode<2:0>	Action
0	Evaluate only 0x0CC[D3]
1	Evaluate only 0x0CC[D2]
2	Evaluate only 0x0CC[D1]
3	Evaluate only 0c0CC[D0]
4	Evaluate 0x0CC[D3:D0] and stop tuning if any 1 of them is low
5	Evaluate 0x0CC[D3:D0] and stop tuning if any 2 of them are low
6	Evaluate 0x0CC[D3:D0] and stop tuning if any 3 of them are low
7	Evaluate 0x0CC[D3:D0] and stop tuning if all 4 of them are low

Table 29. Baseband Filter Tuner Mode

RECEIVER CONFIGURATION

RX PROGRAMMABLE FIR FILTER REGISTERS 0F0 THROUGH 0F6

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0F0	*Rx Filter CoeffAddr*	Rx Filter Addr<7:0>								--	R/W
0F1	*Rx Filter CoeffData 1*	Rx Filter Coefficient Write Data<7:0>								--	R/W
0F2	*Rx Filter CoeffData 2*	Rx Filter Coefficient Write Data<15:8>								--	R/W
0F3	*Rx Filter CoeffRead Data 1*	Rx Filter Coefficient Read Back Data<7:0>								--	R
0F4	*Rx Filter Coeff Read Data 2*	Rx Filter Coefficient Read Back Data<15:8>								--	R
0F5	*Rx Filter Config*	Number of Taps			Select Rx Ch<1:0>		Write Rx	Start Rx Clock	open	00h	R/W
0F6	*Rx Filter Gain*	Open						Filter gain<1:0>		00h	R/W

SPI Register 0x0F0—Rx Filter Coeff Addr

The digital filter coefficients are indirectly addressable. Register 0x0F0 holds the address of the indirect coefficient address.

SPI Registers 0x0F1 and 0x0F2—Rx Filter Coeff Data 1& 2

Write the coefficient values to these registers. Write these registers (along with register 0x0F0) before setting bit D2 of 0x0F5. Coefficients are in 2's complement form and are 16-bits wide.

SPI Registers 0x0F3 and 0x0F4—Rx Filter Coeff Read Data 1 & 2

When reading the filter coefficients, writ e the address in 0x0F0, write register 0x0F5 to start the programming clock and then read registers 0x0F3 and 0x0F4. Coefficients are in 2's complement form and 16-bits wide.

SPI Register 0x0F5—Rx Filter Configuration

[D7:D5] Number of Taps<2:0> The number of taps of the Rx filter must be programmed when writing coefficients, mapped as shown below. The number of taps can be read by first writing to 0x0F5 to turn on the clocks and select the correct receiver. Then, read 0x0F5.

Number of Taps	Number of Taps<2:0>
16	000
32	001

Number of Taps	Number of Taps<2:0>
48	010
64	011
80	100
96	101
112	110
128	111

Table 30. Rx Filter Taps

[D4:D3]Select Rx CH<1:0> When writing coefficients, bit D3 causes a write to Rx1, bit D4 causes a write to Rx2 and both bits set writes to both Rx filters. When reading, setting both bits is an invalid case.

[D2] Write Rx Set this bit to write a coefficient and clear it to read a coefficient. After the values have been programmed, write to register 0x0F5 with the Write Rx bit cleared but the Start Rx Clock bit high. Then, write to 0x0F5 again with the clock start bit cleared. This ensures that the write bit resets before the clock stops. The table requires 4 Rx sample periods after "Write Rx" goes high for the value to write into the table. A small wait period may be necessary between consecutive writes.

[D1] Start Rx Clock Set this bit to start the programming clock.

SPI Register 0xF6—Rx Filter Gain

These bits affect how much digital gain adds to the digital samples after the RFIR filter per the table below. This is different from and in addition to the Gain Control digital gain in register 0x0FB[D2].

Rx Filter Gain<1:0>	Gain
3	-12dB
2	-6dB
1	0dB (default)
0	+6dB

Table 31.Rx Filter Gain

GAIN CONTROL GENERAL SETUP REGISTERS 0FA THROUGH 10E

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0FA	*AGC Config1*	Dec Pwr for Low Pwr	Dec Pwr for Lock Level	Dec Pwr for Gain Lock Exit	Slow Attack Hybrid Mode	Rx 2 Gain Control Setup<1:0>		Rx 1 Gain Control Setup<1:0>		E0h	R/W
0FB	*AGC config2*	Soft Reset	Gain Unlock Control	Open		Use Full Gain Table	Enable Digital Gain	Manual Gain Control Rx 2	Manual Gain Control Rx 1	08h	R/W
0FC	*AGC Config3*	Manual (CTRL_IN) Incr Gain Step Size<2:0>			Inc/Dec LMT Gain	Use AGC for LMT/LPF Gain	ADC Overrange Sample Size<2:0>			03h	R/W
0FD	*Max LMT/Full Gain*	Open	Maximum Full Table/LMT Table Index<6:0>							4Ch	R/W
0FE	*Peak Wait Time*	Manual (CTRL_IN) Decr Gain Step Size<2:0>			Peak Overload Wait Time<4:0>					44	R/W
0FF		Open								--	R/W
100	*Digital Gain*	Dig Gain Step Size<2:0>			Maximum Digital Gain<4:0>					6Fh	R/W
101	*AGC Lock Level*	Enable Dig Sat Ovrg	AGC Lock Level (Fast)/ AGC Inner High Threshold (Slow) <6:0>							0Ah	R/W
102	*ADC noise Correction Factor*	ADC Noise Correction Factor<9:2>								--h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
103	*Gain Step Config1*	LMT Detector Settling Time<2:0>			Dec Step Size for: Large LMT Overload/ Full Table Case #3 <2:0>			ADC Noise Correction Factor<1:0>		08h	R/W
104	*ADC Small Overload Threshold*	ADC Small Overload Threshold<7:0>								2Fh	R/W
105	*ADC Large Overload Threshold*	ADC Large Overload Threshold<7:0>								3Ah	R/W
106	*Gain Step Config 2*	Open	Fast Attack Only. Decrement Step Size for: Small LPF Gain Change / Full Table Case #2 <2:0>				Decrement Step Size for: Large LPF Gain Change / Full Table Case #1<3:0>			25h	R/W
107	*Small LMT Overload Threshold*	Force PD Reset Rx2	For PD Reset Rx1	Small LMT Overload Threshold<5:0>						3Fh	R/W
108	*Large LMT Overload Threshold*	Open		Large LMT Overload Threshold<5:0>						1Fh	R/W
109	*Rx1 Manual LMT/Full Gain*	Power Meas in State 5<3>	Rx1 Manual Full table/LMT table Gain Index<6:0>							4Ch	R/W
10A	*Rx1 Manual LPF gain*	Power Meas in State 5<2:0>			Rx1 Manual LPF Gain <4:0>					58h	R/W
10B	*Rx1 Manual Digital/Forced Gain*	Open		Force Rx1 Digital Gain	Rx1 Manual/Forced Digital Gain<4:0>					00h	R/W
10C	*Rx2 ManualLMT/Full Gain*	Open	Rx2 Manual Full table/ LMT table Gain Index<6:0>							4Ch	R/W
10D	*Rx2 Manual LPF Gain*	Open			Rx2 Manual LPF Gain<4:0>					18h	R/W
10E	*Rx2 Manual Digital/Forced Gain*	Open		Force Rx2 Digital Gain	Rx2 Manual/Forced Digital Gain<4:0>					00h	R/W

SPI Register 0x0FA—AGC Config 1

[D7] Dec Pwr for Low Pwr When comparing average signal power to the Low Power Threshold (0x114), setting this bit causes the averaging block to use the signal at the output of either the Half-Band 1 filter or the RFIR filter, depending on the setting of 0x15C[D6]. This is the recommended setting. If this bit is clear, the signal at the output of the ADC or of Half-Band Filter 3 is used.

[D6] Dec Pwr for Lock Level When comparing averaged signal power to the Lock Level Threshold (0x101), setting this bit causes the averaging block to use the signal at the output of either the Half-Band 1 filter or the RFIR filter, depending on the setting of 0x15C[D6]. This is the recommended setting. If this bit is clear, the signal at the output of the ADC or of Half-Band Filter 3 is used.

[D5] Dec Pwr for Gain Lock Exit When comparing averaged signal power to the Energy Lost Threshold (0x112) or the Stronger Signal Threshold (0x113), setting this bit causes the averaging block to use the signal at the output of either the Half-Band 1 filter or the RFIR filter, depending on the setting of 0x15C[D6]. This is the recommended setting. If this bit is clear, the signal at the output of the ADC or of Half-Band Filter 3 is used.

[D4] Slow Attack Hybrid AGC Mode Set this bit if using the Slow Attack Hybrid AGC mode (see D3:D0.) Clear it for any other mode.

[D3:D2] Rx2 Gain Control Setup<1:0> Gain Control operation maps to these setup bits per Table 32.

Gain Control Setup<1:0>	Gain Control Mode
0	Manual Gain

Gain Control Setup<1:0>	Gain Control Mode
1	Fast Attack Automatic Gain Control (AGC)
2	Slow Attack AGC
3	Slow Attack Hybrid AGC—also set 0x0FA[D4]

Table 32.Gain Control Setup

[D1:D0] Rx1 Gain Control Setup<1:0> Same as [D3:D2] but applies to Rx1.

SPI Register 0x0FB—AGC Config 2

[D7] Soft Reset Setting this bit resets the AGC state machines to their reset states and clears all over range detectors, counters and power accumulators. Any registers set via SPI writes are not changed. The bit must be set and then cleared.

[D6] Gain Unlock Control Only applies to the Fast AGC and allows the gain to stay locked even under certain overload conditions. If using the Gain Lock Delay mode (0x014[D1] set), set this bit.

[D3] Use Full Gain Table Set this bit to use a gain table architecture of one contiguous table that uses one index (pointer). Clear the bit to split the table into two parts with two pointers, one that only adjusts LNA, Mixer, and Transimpedance Amplifier (LMT) Gain and the other that adjusts Low Pass Filter (LPF) Gain. The default table is a Full Table. A Split Table must be programmed (see 0x130-0x137).

[D2] Enable Digital Gain This bit only has an effect in the split table mode. In the full table mode, digital gain can be explicitly added to the gain table and as the gain index move to areas with digital gain, this gain is automatically used. In the split table mode, digital gain is controlled independently from the LMT gain table. Bit D2 must be set for digital gain to be used in any gain control mode in split table mode.

[D1] Manual Gain Control Rx2 Only applies in Manual Gain Mode. If this bit is clear, SPI writes change the gain index. When this bit is set, Control Input pins control the gain indices. The signals on the Control Input pins are edge detected and transitioning high causes the gain to change. When this bit transitions high, the gain always resets to its maximum analog value.

[D0] Manual Gain Control Rx1 Same as bit D1 but applies to Rx1.

SPI Register 0x0FC—AGC Config 3

[D7:D5] Manual (CTRL_IN) Incr Gain Step Size<2:0> Only applies in manual gain mode (0x0FA[D3:D0] clear) and if the CTRL_IN pins control the gain (0x0FB[D1:D0] set). If CTRL_IN0 transitions high, the gain index of Rx1 increases by the value in this register + 1. Rx2 is similarly affected by CTRL_IN2.

[D4] Inc/Dec LMT Gain Only applies in manual gain mode (0x0FA[D3:D0] clear), if the Control Input signals control the gain (0x0FB[D1:D0] set), if the Split Gain Table is used (0x0FB[D3] clear) and if bit [D3] is clear. If this bit is high, the gain will change only in the LNA, Mixer, Transimpedance Amplifier (LMT). If this bit is clear, only Low Pass Filter (LPF) gain will change.

[D3] Use AGC for LMT/LPF Gain Only applies in manual gain mode (0x0FA[D3:D0] clear) and if the Control Input signals control the gain (0x0FB[D1:D0] set) and if the Split Gain Table is used (0x0FB[D3] clear). If this bit is clear, then bit D4 determines where the gain is changed (LMT or LPF). If this bit is set, bit D4 is ignored and the AGC uses its peak detectors to determine where the gain will change.

[D2:D0] ADC Over range Sample Size<2:0> The ADC is an oversampling Sigma-Delta Converter with a 4-bit output. Over Range is determined by taking a sum of the squares of a number of samples and comparing that value to two different Over Range limits in registers 0x104 and 0x105. The number of samples used is equal to this register value + 1.

SPI Register 0x0FD—Max LMT/Full Gain

When the "Use Full Gain Table" bit (0x0FB[D3]) is set, this register represents the maximum full gain table index and the maximum value is 90(d). In Split Table Mode (0x0FB[D3] clear), this register represents the maximum gain table index for the LMT table and the maximum value is 40(d).

SPI Register 0x0FE—Peak Wait Time

[D7:D5] Manual (CTRL_IN) Decr Gain Step Size<2:0> Only applies in manual gain mode (0x0FA[D3:D0] clear) and if the Control Input signals control the gain (0x0FB[D1:D0] set). If CTRL_IN1 transitions high, the gain index of Rx1 decreases by the value in this register + 1. Rx2 is similarly affected by CTRL_IN3.

[D4:D0] Peak Overload Wait Time<4:0> After a gain change occurs, the LMT and ADC Peak Detectors are cleared and they ignore overloads while the analog signal path plus ADCs settle. This register sets this settling time in ClkRF sample periods. ClkRF is the input clock to the RFIR. This register affects all gain control modes.

SPI Register 0x100—Digital Gain

[D7:D5] Digital Gain Step Size<2:0> Only applies in AGC modes, if digital gain is enabled (0x0FB[D2] set), and when using the Split Gain Table (0x0FB[D3] clear). If digital saturation occurs, the digital gain index reduces by the number in this register +1.

[D4:D0] Maximum Digital Gain<4:0> Only applies if digital gain is enabled (0x0FB[D2] set). This register sets the upper limit on how much digital gain may be used. This value applies to AGC and MGC modes. The maximum possible value is 31dB. 1dB/LSB.

SPI Register 0x101—AGC Lock Level (Fast)/AGC Inner Threshold High (Slow)

[D7] Enable Dig Sat Ovrg When clear, digital sat does not cause a gain decrease in any state. When set, using the full table, and if the digital gain > 0, a digital sat event can cause a gain decrease in any state. Only applies to the Fast AGC, full gain table.

[D6:D0] AGC Lock Level (Fast)/AGC Inner High Threshold (Slow)<6:0> Only applies in AGC modes. For the Fast Attack AGC, this register specifies the AGC Lock level in –dBFS at 1dBFS/LSB. For the Slow Attack AGC, this register specifies the lower of two thresholds that will result in a gain decrease if the average signal power exceeds this threshold (see Figure 4).

SPI Register 0x0102 (and 0x0103[D1:D0]—ADC Noise Correction Factor—Do not change these bits

This word reduces the noise of the ADC output fed to the power measuring blocks. The actual value used is this register divided by 8.

SPI Register 0x103—Gain Step Config 1

[D7:D5] LMT Detector Settling Time<2:0> This register sets the bias current (and thus attack time) for the peak detector per Table 33. It is strongly recommended to leave the setting at its default value of zero.

LMT Detector Settling Time<2:0>	Nominal Bias Current (uA)	95% Settling Time (ns)
0	6.000	7
1	3.000	10
2	1.500	18
3	0.750	35
4	0.365	70
5	0.188	140
6	0.094	230
7	0.047	400

Table 33.LMT Detector Settling Time

[D4:D2] Step Size for: Large LMT Overload/ Full Table Case #3<2:0> Only applies in AGC modes. The equations and table below show how the bits in this register and those in register 0x106[D6:D0] affect the AGC for various conditions.

When the Fast Attack AGC (see 0x0FB[D3:D0]) and Full Gain Table (0x0FB[D3] set) are used, equations below describe the operation.

Use Full Table Case #1 (0x106[D3:D0]) if : Large ADC Overload AND (Large LMT Overload OR Digital Saturation) *Equation 25*
Use Full Table Case #2 (0x106[D6:D4]) if : Large ADC Overload OR Large LMT Overload OR Digital Saturation *Equation 26*
Use Full Table Case #3 (0x103[D4:D2] if : Small ADC Overload *Equation 27*

For other AGC modes, Table 34 describes which step sizes are used. The Large LMT Step is set by 0x103[D4:D2], the Large LPF Gain Change is set by 0x106[D3:D0], and the Small LPF Gain Change is set by 0x106[D6:D4].

AGC Mode	Gain Table Mode	Overload Type	# of Overload Occurrences	Step Size Used
Fast	Split	Large LMT	1	Large LMT
Fast	Split	Small LMT	1	None. Prevents LMT Gain Increase if Low Power Detected
Fast	Split	Large ADC	1	Large LPF if adjusting LPF gain and Large LMT if adjusting LMT gain
Fast	Split	Small ADC	1	Small LPF if adjusting LPF gain and Large LMT if adjusting LMT gain
Slow	Full	Large LMT	≥ Large LMT Overload Threshold Counter (0x121[D7:D4])	Large LMT
Slow	Full	Small LMT	≥ Small LMT Overload Threshold Counter (0x121[D3:D0])	None. Prevents gain increases
Slow	Full	Large ADC	≥ Large ADC Overload Threshold Counter (0x122[D7:D4])	Large LPF
Slow	Full	Small ADC	≥ Small ADC Overload Threshold Counter (0x122[D3:D0])	None. Prevents gain increases
Slow	Split	Large LMT	≥ Large LMT Overload Threshold Counter (0x121[D7:D4])	Large LMT
Slow	Split	Small LMT	≥ Small LMT Overload Threshold Counter (0x121[D3:D0])	None. Prevents LMT Gain Increase
Slow	Split	Large ADC	≥ Large ADC Overload Threshold Counter (0x122[D7:D4])	Large LPF if adjusting LPF gain and Large LMT if adjusting LMT gain
Slow	Split	Small ADC	≥ Small ADC Overload Threshold Counter (0x122[D3:D0])	None. Prevents LMT Gain Increase

Table 34. LMT Overload and Full Table Step #3 vs. Overload Condition

SPI Register 0x104—ADC Small Overload Threshold

See register 0x0FC[D2:D0] for a description of ADC overloads. This register is one of two that the AGC compares against the sum of squares. This register should be the smaller of the two values, indicating that a small overload has occurred.

SPI Register 0x105—ADC Large Overload Threshold

Same as register 0x104 but this register should be the larger of the two values and indicates a larger overload condition.

SPI Register 0x106—Gain Step Config 2

[D6:D4] Fast Attack Only. Decrement Step Size for: Small LPF Gain Change/ Full Table Case #2<2:0> Only applies in the Fast AGC mode (see 0x0FA[D3:D0]). See table Table 34.

[D3:D0] Decrement Step Size for: Large LPF Gain Change/Full Table Case #1 Only applies in AGC modes. See table Table 34.

SPI Register 0x107—Small LMT Overload Threshold

[D7] Force PD Reset Rx2 Setting this bit forces the RX2 ADC and LMT peak detectors to ignore peak overloads.

[D6] Force PD Reset Rx1 Same as D7 but applies to Rx1.

[D5:D0] Small LMT Overload Threshold<5:0>These bits, mapped per Equation 28, set the Small LMT overload threshold. The threshold detector uses the signal at the input to the LPF. This value should be the smaller of two thresholds, with this threshold indicating the less severe overload condition. The valid range of the register is from 0x07 to 0x31. 0x108 holds the larger threshold.

$$LMT\ Overload\ Threshold\ (mVpeak) = 16mV * (LMT\ Overload\ Threshold < 5:0 > +1)$$

Equation 28

SPI Register 0x108—Large LMT Overload Threshold

Same as 0x107 (and uses the same equation) but should be the larger of the two LMT overload thresholds.

SPI Register 0x109—Rx1 Manual LMT/Full Gain

[D7] Power Meas in State 5<3> These bits control the power measurement duration in exactly the same way as the "Dec Power Measurement Duration" function in 0x15C[D3:D0] but apply only to State 5 (Gain Lock) for the Fast Attack AGC.

[D6:D0] Rx1 Manual Full table/LMT table Gain Index<6:0> For MGC and when using the Full Gain Table (0x0FB[D3]), write this register to set the Full Gain Table index. When using the Split Gain Table, this register sets the value of the LMT Gain Table Index. The LPF Gain Table Index (in Split Table Mode) for Rx1 is set by register 0x10A. For AGC, this register holds the current full or LMT index.

SPI Register 0x10A—Rx1 Manual LPF Gain

[D7:D5] Power Meas in State 5<2:0> See 0x109[D7].

[D4:D0] Rx1 Manual LPF Gain <4:0> Only applies when in Manual Gain Mode (0x0FA[D1:D0]. When using the Split Gain Table (0x0FB[D3]), write this register to set the LPF Gain Table index value. The LMT Gain Table Index for Rx1 is set by register 0x109.

SPI Register 0x10B—Rx1 Manual Digital Gain

[D5] Force Rx1 Digital Gain Setting this bit forces the digital gain to the fixed value in bits D4:D0. Ignored if digital gain is disabled.

[D4:D0] Rx1 Manual/Forced Digital Gain Ignored if digital gain is disabled. In Manual Gain Mode (0x0FA[D1:D0] clear), write this register to set the Digital Gain Index value. In AGC mode and if bit D5 is set, the digital gain index is always forced to this value.

SPI Registers 0x10C through 0x10E—Manual Gain Registers

Same as registers 0x109 through 0x10B but these apply to Rx2.

FAST ATTACK AGC SETUP REGISTERS 110 THROUGH 11B

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
110	*Config 1*	Enable Gain Inc after Gain Lock	Goto Opt Gain if Energy Lost or EN_AGC High	Goto Set Gain if EN_AGC High	Goto Set Gain if Exit Rx State	Don't Unlock Gain if Energy Lost	Goto Optimized Gain if Exit Rx State	Don't Unlock Gain If Lg ADC or LMT Ovrg	Enable Incr Gain	02h	R/W
111	*Config 2 & Settling Delay*	Use Last Lock Level for Set Gain	Enable LMT Gain Inc for Lock Level	Goto Max Gain or Opt Gain if EN_AGC High	Settling Delay<4:0>					CAh	R/W
112	*Energy Lost Threshold*	Post Lock Level Step Size for: LPF Table/ Full Table <1:0>		Energy lost threshold<5:0>						4Ah	R/W
113	*Stronger Signal Threshold*	Post Lock Level Step for LMT Table <1:0>		Stronger Signal Threshold<5:0>						4Ah	R/W
114	*Low Power Threshold*	Don't unlock gain if ADC Ovrg	Low Power Threshold<6:0>							80h	R/W
115	*Strong Signal*	Don't unlock gain if	Open							64h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
	Freeze	Stronger Signal									
116	*Final Over Range and Opt Gain*	Final Over Range Count<2:0>			Open	Optimize Gain Offset<3:0>				65h	R/W
117	*Energy Detect Count*	Increment Gain Step (LPF/LMT)<2:0>			Energy Detect count<4:0>					08h	R/W
118	*AGCLL Upper Limit*	Open		AGCLL Max Increase<5:0>						3Fh	R/W
119	*Gain Lock Exit Count*	Open		Gain Lock Exit Count<5:0>						08h	R/W
11A	*Initial LMT Gain Limit*	Open	Initial LMT Gain Limit<6:0>							1Ch	R/W
11B	*Increment Time*	Increment Time<7:0>								0Ah	R/W

SPI Register 0x110—Config 1

[D7] Enable Gain Inc after Gain Lock Only applies to the Fast AGC and if the "Enable Gain Incr" bit (0x110[D0]) is set. Set this bit to have the AGC check if the signal power has dropped below the Low Power Threshold (0x114) after the AGC adjusts the gain for the AGC Lock Level. If this occurs for a duration set by "Incr Time" (0x11B), then the AGC increases the gain by the "Increment Gain Step" (0x117[D7:D5]). If this bit is clear the gain cannot increase after Lock Level adjustment.

[D6] Goto Optimize Gain if Energy Lost/EN_AGC High After the AGC has locked the gain, various conditions cause the AGC to unlock the gain and return to its reset state. When the gain unlocks, the AGC can change the gain to one of three index values or it can keep the gain at the same value. Table 35 defines the three index values.

Gain Index	Set by	Definition
Max Gain	Maximum Full Table/LMT Table Index (0x0FD)	Maximum Analog Gain allowed by 0x0FD
Optimize Gain	AGC Gain Lock Index at end of last burst Plus Optimize Gain Offset (0x116[D3:D0])	An optimized value that reduces the amount of steps the AGC should typically take to Lock the gain for each burst.
Set Gain	AGC Gain Lock Index at the start of the last burst Or AGC Gain Lock Index at the end of the last burst	Similar to Optimize Gain but has different conditions for Unlocking the gain. Usually not needed as Optimize Gain will handle most situations
No Gain Change	N/A	No change to the Gain Index

Table 35.Gain Index Definitions

Several bit settings affect what happens to the Gain Index when various conditions occur. Table 36 defines how to configure the bits to force the Gain Index to a certain value given certain conditions.

Condition that Unlocks the Gain	Gain Index Type	Set Bits	Clear Bits
Exit Rx State	Max Gain	None Required	0x110[D4], 0x110[D2]
Exit Rx State	Optimize Gain	0x110[D2]	0x110[D4]
Exit Rx State	Set Gain	0x110[D4]	0x110[D2]
Stronger Signal Threshold Exceeded	No Gain Change	None Required	0x110[D3] only if 0x0FB[D6] set
Energy Lost Threshold Exceeded	Max Gain	None Required	0x110[D6]. 0x110[D3] only if 0x0FB[D6] set

Condition that Unlocks the Gain	Gain Index Type	Set Bits	Clear Bits
Energy Lost Threshold Exceeded	Optimize Gain	0x110[D6]	0x110[D3] only if 0x0FB[D6] set
Large ADC or LMT Overload	No Gain Change	None Required	None Required
EN_AGC pulled High	Max Gain	0x0FB[D6], 0x111[D5]	0x110[D6:D5]
EN_AGC pulled High	Optimize Gain	0x0FB[D6], 0x110[D6], 0x111[D5]	0x110[D5]
EN_AGC pulled High	Set Gain	0x0FB[D6], 0x110[D5]	0x111[D5]
EN_AGC Pulled High	No Gain Change	0x0FB[D6]	0x110[D5], 0x111[D5]

Table 36.Gain Index Type after Unlock vs. Input Conditions and Bit Settings

[D5] Goto Set Gain if EN_AGC is High This bit applies to the final state of the Fast AGC after it locks the gain. See tables 40 and 41.

[D4] Goto Set Gain if Exit Rx State This bit applies to the final state of the Fast AGC after it locks the gain. See tables 40 and 41.

[D3] Don't Unlock Gain if Energy Lost Only applies if "Gain Unlock Control" (0x0FB[D6]) is set. Setting this bit prevents the gain from unlocking even if the average signal power decreases more than the "Energy Lost Threshold" in 0x112. Only applies to the Fast AGC.

[D2] Goto Optimized Gain if Exit Rx State Setting this bit causes the Fast AGC to move the gain index to the value Locked at the end of the last burst plus the value in 0x116[D3:D0] when the AD9361 exited Rx mode. See tables 40 and 41.

[D1] Don't Unlock Gain if Large ADC or LMT Ovrg Setting this bit prevents the gain from unlocking even if large ADC or LMT overloads occur. This bit should be set along with the "Don't unlock gain if ADC ovrg" bit (0x114[D7]). Only applies to the Fast AGC.

[D0] Enable Incr Gain Setting this bit allows the Fast AGC to increase the gain while it adjusts the gain towards its final state (Gain Lock). Clearing this bit prevents the gain from increasing under any condition except when the Fast AGC unlocks.

SPI Register 0x111—Config 2 and Settling Delay

[D7] Use Last Lock Level for Set Gain This bit applies to the final state of the Fast AGC after it locks the gain. See tables 40 and 41.

[D6] Enable LMT Gain Incr for Lock Level Only applies to the Fast AGC and a Split Gain Table (0x0FB[D3]). If the gain needs to increase for the AGC Lock Level adjustment (0x101), setting this bit allows LMT gain to be increased. The maximum LMT gain used is set by the LMT Gain Step (0x103[D4:D2]). The difference (if any) is made up by LPF gain. If this bit is clear, only LPF gain increases.

[D5] Goto Max Gain or Opt Gain if EN_AGC High Applies to the final state of the Fast AGC after it locks the gain. See tables 40 & 41.

[D4:D0] Settling Delay<4:0> Applies to the Fast and Slow AGC. Before measuring power, the AD9361 waits for the Rx signal path to settle. This register sets this "Settling Delay" and it equals this register * 2. ClkRF (at the input of the RFIR filter) clocks the counter.

SPI Register 0x112—Energy Lost Threshold

[D7:D6] Post Lock Level Step Size for: LPF Table/ Full Table <1:0> After the AGC makes the Lock Level adjustment (0x101), it checks if the ADC Large Overload, LMT Overload, or Digital Sat has occurred. If so, the AGC decreases the gain and checks again. For a Full Gain Table (0x0FB[D3] set), the gain reduces by the step size in this register. For the Split Table, (1) if an ADC Large Overload occurs and the LMT Gain Index < LMT Index Limit, the gain reduces by the value in this register. (2), if a Large LMT Overload occurs or if a Large ADC Overload occurs and the LMT Gain Index > LMT Index Limit, the gain reduces by the value in 0x113ID7:D6]. If the number of overloads exceeds the "Final Over Range Count" (0x116[D7:D5]), then the AGC algorithm restarts.

[D5:D0] Energy Lost Threshold<5:0> Applies to the Fast AGC after gain lock. See Table 35 and Table 36. After gain lock, the AGC measures the signal power and uses it as a comparison value. If a later power result is lower than the original value by an amount equal to or greater than this Energy Lost Threshold, a counter starts running at the ClkRF rate. If the counter exceeds *twice* the "Gain Lock Exit Count" (0x119), the gain may unlock depending on the AGC configuration bits given in tables Table 35 and Table 36. 1dB/LSB.

SPI Register 0x113—Stronger Signal Threshold

[D7:D6] Post Lock Level Step for LMT Table <1:0> LMT step used for peak overloads after AGC lock level adjust. See 0x112[D7:D5].

[D5:D0] Stronger Signal Threshold<5:0> Applies to the Fast AGC after gain lock. See Table 35 and Table 36. After Gain Lock, the AGC measures the signal power and uses it as a comparison value. If a later power result is higher than the original value by an amount equal to or greater than this Stronger Signal Threshold, a counter starts running at the ClkRF rate. If the counter exceeds *twice* the "Gain Lock Exit Count" value (0x119), the gain may unlock depending on the AGC configuration bits given in tables 40 and 41. 1dB/LSB.

SPI Register 0x114—Low Power Threshold

[D7] Don't unlock gain if ADC Ovrg Valid for the Fast AGC if the "Don't Unlock Gain If Large ADC or LMT Overload" bit (0x110[D1]) is set. 0x114[D7] prevents gain unlock for ADC overloads without any additional setup bits (besides 0x110[D1]).

[D6:D0] Low Power Threshold<6:0> Valid for the Fast AGC if the "Enable Incr Gain" bit (0x110[D0]) is set. The "Enable Gain Incr after Gain Lock" bit (0x110[D7] also affects when this threshold is used. See these bits for details. Also can be used in MGC mode. Units: -dBFS; 0.5dB/LSB.

SPI Register 0x115—Don't Unlock Gain if Stronger Signal

Valid for the Fast AGC if "Gain Unlock Control" (0x0FB[D6]) is set. Setting 0x115[D7] prevents gain unlock f the signal power increases more than the "Stronger Signal Threshold" in 0x113.

SPI Register 0x116—Final Over Range and Opt Gain

[D7:D5] Final Over Range Count <2:0> Fast AGC. See the "Post Lock Level Step Size for: LPF Table/Full Table<1:0> in 0x112[D7:D6].

[D3:D0] Optimize Gain Offset<3:0> Fast AGC. See tables Table 35 and Table 36 to see how this value is used.

SPI Register 0x117—Energy Detect Count

[D7:D5] Slow Decay Gain Step Size<2:0> Fast AGC only and if the "Enable Incr Gain" bit (0x110[D0] is set. See this bit and bit D7 of register 0x110 for a description of how this step is used. The gain increases by the value in this register +1.

[D4:D0] Energy Detect Count<4:0> Fast AGC only, state 1 (peak overload detect). The AGC will move to state 2 only if no overloads occur for the time specified in this register. ClkRF (RFIR input clock) clocks the counter. 1clkRF cycle/LSB.

SPI Register 0x118—AGCLL Max Increase

Fast AGC Only. This register sets the maximum gain index increase that the AGC can use for the lock level adjustment (see 0x101).

SPI Register 0x119—Gain Lock Exit Count

See the "Energy Lost Threshold" (0x112[D4:D0] and the "Stronger Signal Threshold" (0x113[D4:D0] for details.

SPI Register 0x11A—LMT Index Limit

Applies to AGC gain control modes. Applies when using the "Split Gain Table" (0x0FB[D3] clear). The LMT table splits at this value.

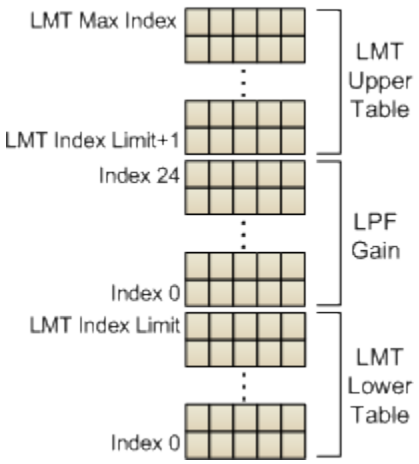

Figure 3.Split Gain Table in AGC Fast Attack Mode

SPI Register 0x11B—Increment Time<7:0>

Fast AGC, applies if "Enable Gain Increase" (0x110[D0]) is set. If the signal power drops below "Low Power Threshold" (0x114) for greater than or equal to "Increment Time", the gain index increases by the "Slow Decay Gain Step" (0x117[D7:D5]). 1LSB/1ClkRF cycle.

SLOW ATTACK & HYBRID AGC REGISTERS 120 THROUGH 12A

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
120	*AGC Inner Low Threshold*	Prevent Gain Inc	AGC Inner Low Threshold<6:0>							--h	R/W
121	*LMT Overload Counters*	Large LMT Overload Exceeded Counter<3:0>				Small LMT Overload Exceeded Counter<3:0>				--h	R/W
122	*ADC Overload Counters*	Large ADC Overload Exceeded Counter<3:0>				Small ADC Overload Exceeded Counter<3:0>				--h	R/W
123	*Gain Step1*	Immed. Gain Change if Lg LMT Overload	AGC Inner High Threshold Exceeded Step Size<2:0>			Immed. Gain Change if Lg ADC Overload	AGC Inner Low Threshold Exceeded Step Size<2:0>			--h	R/W
124	*Gain Update Counter1*	Gain update counter<7:0>								--h	R/W
125	*Gain Update Counter2*	Gain update counter<15:8>								--h	R/W
126		Open								--h	R/W
127		Open								--h	R/W
128	*Digital Sat Counter*	Open		Double Gain Counter	Enable Sync for Gain Counter	Dig Saturation Exceeded Counter<3:0>				--h	R/W
129	*Outer Power Thresholds*	AGC Outer High Threshold<3:0>				AGC Outer Low Threshold<3:0>				--h	R/W
12A	*Gain Step 2*	AGC Outer High Threshold Exceeded Step Size<3:0>				AGC Outer Low Threshold Exceeded Step Size<3:0>				--h	R/W

The AGC Slow Attack/Hybrid registers do not have defaults. To use these AGC modes, the BBP must program registers 0x120-0x123, 0x129, and 0x12A at a minimum. 0x124 through 0x125 are required for the Gain Update Counter and 0x128 is required for digital gain.

SPI Register 0x120—AGC Inner Lower Threshold

[D7] Prevent Gain Increase Setting this bit prevents a gain increase if a Small LMT or Small ADC Overload occurs. See bits D6:D0.

[D6:D0] AGC Inner Low Threshold<6:0> This register, along with registers 0x101 and 0x129, set the slow attack thresholds per Figure 4. No gain changes occur if the signal power remains between the Inner Thresholds. If the signal power is higher than the Upper Threshold or lower than the Lower Threshold, the gain changes appropriately. See bit D7 for preventing gain increases. Gain changes occur when the "Gain Update Counter" expires (0x0FA[D4] clear) or when CTRL_IN2 transitions high (0x0FA[D4] set).

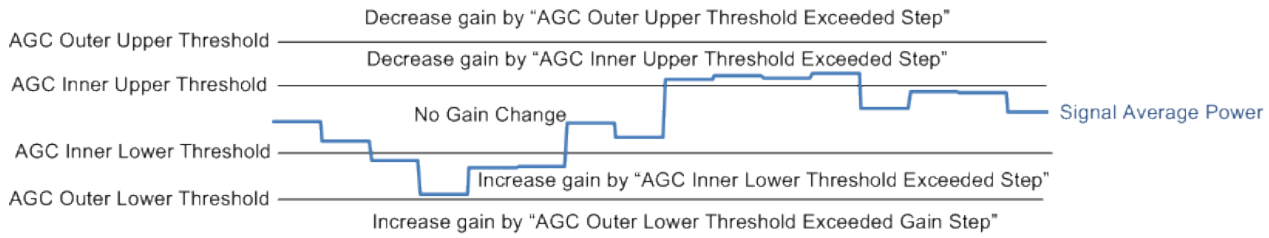

Figure 4.AGC Slow Attack Thresholds and Gain Steps

The AGC Inner Lower Threshold is specified in –dBFS with a resolution of 1dB/LSB.

SPI Register 0x121—LMT End Overload Counters

[D7:D4] Large LMT Overload Exceeded Counter<3:0> This counter specifies the number of Large LMT Overloads that must occur before the gain decreases by the "LMT Gain Step" specified in 0x103[D4:D2]. Gain changes occur when the "Gain Update Counter" expires (0x0FA[D4] clear) or when CTRL_IN2 transitions high (0x0FA[D4] set).

[D3:D0] Small LMT Overload Exceeded Counter<3:0> Applies if the "Prevent Gain Increase" bit (0x120[D7]) is set. This counter specifies the number of small LMT overloads that much occur in order to prevent a gain increase (see 0x120[D7]).

SPI Register 0x122—ADC Overload Counters

[D7:D4] Large ADC Overload Exceeded Counter<3:0> If a Large ADC Overload occurs the number of times specified in this counter, the gain will decrease by the "Large ADC Overload" gain step in register 0x106[D3:D0].

[D3:D0] Small ADC Overload Exceeded Counter<3:0> Applies if the "Prevent Gain Increase" bit (0x120[D7]) is set. This counter specifies the number of small ADC overloads that much occur in order to prevent a gain increase (see 0x120[D7]).

SPI Register 0x123—Gain Step 1

[D7] Immed Gain Change if Large LMT Overload Same operation as that shown in 0x121[D7:D4] but the gain change will happen immediately (ignoring the Gain Update Counter and the CTRL_IN2 pin).

[D6:D4] AGC Inner High Threshold Exceeded Step<2:0> See 0x120[D6:D0].

[D3] Immed Gain Change if Large ADC Overload Same operation as that described in 0x122[D7:D4] but the gain change will happen immediately (ignoring the Gain Update Counter and the CTRL_IN2 pin).

[D2:D0] AGC Inner Low Threshold Exceeded Step<2:0> See 0x120[D6:D0].

SPI Registers 0x124 and 0x125—Gain Update Counter

Applies if 0x0FA[D4] is clear and at least one receiver is in Slow AGC Mode (0xFA[D3:D2] and/or 0xFA[D1:D0] = 2'b11). A gain change only occurs when this counter expires (unless 0x123[D7] and/or 0x123[D3] are set. Gain changes will occur on slot boundaries if the Gain Update Counter is set appropriately. The counter clocks at the ClkRF rate and starts counting 3 ClkRF cycles after the AD9361 enters the Rx state. The counter is clocked at the ClkRF rate (the input rate of the RFIR). The depth of the counter is equal to double the value in these registers. Or, if bit D5 of 0x128 is set, it is equal to 4x the value in these registers. If "Enable Sync for Gain Counter" (0x128[D4]) is set and CTRL_IN2 transitions high while the counter is running, the counter resets, allowing the BBP to synchronize the counter.

SPI Register 0x128—Digital Sat Counter

[D5] Double Gain Counter See 0x124 and 0x125.

[D4] Enable Sync for Gain Counter See 0x124 and 0x125.

[D3:D0] Digital Saturation Exceeded Counter Same as 0x121[D3:D0] but applies to digital saturation.

SPI Register 0x129—Outer Power Thresholds

[D7:D4] AGC Outer High Threshold<3:0> See 0x120[D6:D0]. First determine the "AGC Inner High Threshold " (0x101). Then load the difference between the Outer and Inner High Thresholds into the "AGC Outer High Threshold" register. 1dB/LSB.

[D3:D0] AGC Outer Low Threshold<3:0> See 0x120[D6]D0]. First determine the "AGC Inner Low Threshold " (0x101). Then load this difference between the Outer and Inner Low Thresholds into this "AGC Outer Low Threshold" register. 1dB/LSB.

SPI Register 0x12A—Gain Step 2

[D7:D4] AGC Outer High Threshold Exceeded Step<3:0> See 0x120[D6:D0].

[D3:D0] AGC Outer Low Threshold Exceeded Step<3:0> See 0x120[D6:D0].

EXTERNAL LNA GAIN WORD REGISTERS 12C THROUGH 12D

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
12C	*Ext LNA High Gain*	Open		Ext LNA High Gain<5:0>						--h	R/W
12D	*Ext LNA Low Gain*	Open		Ext LNA Low Gain<5:0>						00h	R/W

SPI Registers 0x12C and 0x012D—Ext LNA High Gain and Ext LNA Low Gain

These registers should have non-zero values only if (1) an external LNA is used and (2) the "Ext LNA ctrl" bits (see 0x131[D7]) in the Gain Table have been programmed. For a fixed-gain LNA, set 0x12C to the gain of the LNA and leave register 0x12D at its default of 0x00. For an external LNA with a bypass mode, program register 0x12C with the "high gain" (non-bypass) value and program register 0x12D with the "low gain" (bypass) value. The part considers both values to represent positive gain in the front end prior to the AD9361. Both registers range from 0 to 31.5dB in 0.5dB steps/LSB. See register 0x026 to route the external LNA gain table bits to the GPO pins.

AGC GAIN TABLE REGISTERS 130 THROUGH 137

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
130	*Gain Table Address*	Open	Gain Table Address<6:0>							--h	R/W
131	*Gain Table Write Data1*	Ext LNA Ctrl	LNA Gain <1:0>		Mixer Gm Gain <4:0>					--h	R/W
132	*Gain Table Write Data2*	Open		TIA Gain	LPF Gain <4:0>					--h	R/W
133	*Gain Table Write Data 3*	Open		RF DC Cal	Digital Gain <4:0>					--h	R/W
134	*Gain Table Read Data 1*	Ext LNA Ctrl	LNA Gain <1:0>		Mixer Gm Gain <4:0>					--h	R
135	*Gain Table Read Data 2*	Open		TIA Gain	LPF Gain <4:0>					--h	R
136	*Gain Table Read Data 3*	Open		RF DC Cal	Digital Gain <4:0>					--h	R
137	*Gain Table Config*	Open			Receiver Select<1:0>		Write Gain	Start Gain Table Clock	Open	08h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
							Table				

Registers 0x130 through 0x137 allow the user to program custom gain tables into the AD9361 and/or to read back the gain table entries. These registers do not set the current gain index. Registers 0x109 through 0x10E are used for that purpose.

SPI Register 0x130—Gain Table Address

This is the Gain Table Index (pointer) and it varies from 0 to 90(d) when in Full Table Mode and from 0 to 40(d) in Split Table Mode.

SPI Register 0x131—Gain Table Write Data 1

[D7] Ext LNA Ctrl The external LNA control bit. Set this bit at a particular index if an external LNA is used and if that LNA is adding gain to the receive path. See 0x012C for further details on how this bit is used.

[D6:D5] LNA Gain<1:0> Internal LNA gain Index. There are 4 possible values ranging from 0 through 3. 3 represents max gain, 0 is minimum gain. The steps are monotonic but not evenly spaced and the gain changes with LO frequency, temperature and process. See the gain control user guide for more information.

[D4:D0] Mixer Gm Gain<4:0> The Mixer Gain Index. There are 16 possible values ranging from 0 through F. F represents max gain, 0 is minimum gain. The steps are monotonic but not evenly spaced and the gain changes with LO frequency, temperature and process. See the gain control user guide for more information.

SPI Register 0x132—Gain Table Write Data 2

[D5] TIA Gain The transimpedance amplifier gain. If this bit is 0, TIA gain equals -6dB and if the bit is set, the gain equals 0dB.

[D4:D0] LPF Gain Low Pass Filter (LPF) Index. Gain(dB) = Index. Range: 0-24dB. 1 LSB/1dB. Full Gain Table (0x0FB[D3] set) only.

SPI Register 0x133—Gain Table Write Data 3

[D5] RF DC Cal If an RF DC calibration runs, setting this bit causes the calibration to occur at the gain index specified in 0x130. The intent is for the RF DC Offset to calibrate at all unique LMT indices. Ignored in Split Gain Table Mode (see 0x0FB[D3]).

[D4:D0] Digital Gain<4:0> Only applicable if digital gain is enabled in (0x0FB[D6] high). Digital gain maps as 1 dB gain/LSB.

SPI Registers 0x134 through 0x136—Gain Table Read 1, 2, 3

Same as registers 0x131 through 0x133 but apply when reading the gain table. Clear the "Start Gain Table Clock" bit when reading.

SPI Register 0x137—Gain Table Config

[D4:D3] Receiver Select Bit D3 set accesses Rx1, bit D4 set accesses Rx2. When reading the table, setting both bits is an invalid case.

[D2] Write Gain Table Set this self-clearing bit to write the values in 0x130-0x133 to the gain table. After writing all table entries, write 0x137 with the "Write Gain Table" bit cleared but the Start Gain Table Clock bit high. Then, write 0x137 again with the clock start bit cleared. This ensures that the write bit clears after the last write operation.

[D1] Start Gain Table Clock Set only when writing to the gain table. The gain table requires 4 Rx sample periods after "Write Gain Table" goes high for the value to write into the table. A small wait period may be necessary between consecutive writes.

MIXER SUB-TABLE REGISTERS 138 THROUGH 13F

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
138	Gm Sub Table Address	Gm Sub Table Address<7:0>								--h	R/W
139	Gm Sub Table Gain	Open	Gm Sub Table Gain Word Write<6:0>							--h	R/W

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
	Word Write										
13A	Gm Sub Table Bias Word Write	Open			Gm Sub Table Bias Word Write<4:0>					--h	R/W
13B	Gm Sub Table Control Word Write	Open			Gm Sub Table Control Word Write<5:0>					--h	R/W
13C	Gm Sub Table Gain Word Read	Open	Gm Sub Table Gain Word Read<6:0>							--h	R
13D	Gm Sub Table Bias Word Read	Open			Gm Sub Table Bias Word Read<4:0>					--h	R
13E	Gm Sub Table Control Word Read	Open			Gm Sub Table Control Word Read<5:0>					--h	R
13F	Gm Sub Table Config	Open					Write Gm Sub Table	Start Gm Sub Table Clock	Open	00h	R/W

SPI Register 0x138—Gm Sub Table Word Address

This is the Gm Table Index (pointer), which can vary between 0 through 24(d).

SPI Register 0x139—Gm Sub Table Gain Word Write

The Bias word in 0x13A and the Control word in 0x13B at a particular sub table address in 0x138 determine the mixer Gm gain. Program the mixer Gm gain in dB * 4 into this register so that the RSSI algorithm compensates for this gain correctly.

SPI Register 0x13A—Gm Sub Table Bias Word Write

Controls the bias word for the Mixer Gm Sub Table.

SPI Register 0x13B—GM Sub Table Control Word Write

See table above.

SPI Registers 0x13C through 0x13E—GM Sub Table Word Reads

Registers 0x139 through 0x13B define the words in these read-back registers.

SPI Register 0x13F—Gm Sub Table Config

[D2] Write Gm Sub Table Set this bit only when writing to the table.

[D1] Start Gm Sub Table Clock Used when writing to the Gm Sub Table. Allow at least 4 Rx Sample Periods between consecutive writes.

CALIBRATION GAIN TABLE REGISTERS 140 THROUGH 144

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
140	*Word Address*	Calibration Table Addr<7:0>								--h	R/W
141	*Gain Diff Word/Error Write*	Open			Calib Table Gain Diff/Error Word<5:0>					--h	W
142	*Gain Error Read*	Open				Calib Table Gain Error<4:0>				--h	R

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
143	*Config*	Open	Calib Table Select<1:0>		Read Select	Write Mixer Error Table	Write LNA Error Table	Write LNA Gain Diff	Start Calib Table Clock	00h	R/W
144	*LNA Gain Diff Read Back*	Open		LNA Calib Table Gain Difference Word<5:0>						--h	R

The AD9361 can perform a calibration of the Rx gain steps with a resolution of 0.25dB so that the RSSI values are accurate. An external signal is required so the calibration is generally performed as part of factory test. The calibration creates "error words" which represent the deviation of the actual steps in gain from the nominal values used in the gain table. After running the calibration, the error words may be read out of the AD9361 and stored, and then written back into the AD9361 when the system is in the field.

SPI Register 0x140—Word Address

Program the index of the gain stage in this register.

SPI Register 0x141—Gain Diff Word/Error Write

This register has two different functions, depending on which bits are set in 0x143. If bit "Write LNA Gain Diff" (0x143[D1]) is set (along with the Clock bit in D0), then register 0x141 is a gain difference value that is used by the calibration algorithm. These values are the gain differences between maximum gain and the gain at the index (set in 0x140) being programmed. Resolution: 0.5dB.

If the "Write Mixer Error Table" bit (D3) or the "Write LNA Error Table" bit (D2) in 0x143 is set, then the error words can be programmed into this register for the index specified in 0x140. Error word resolution: 0.25dB.

SPI Register 0x142—Gain Error Read

This is the gain error determined by the calibration at the index in register 0x140. These value can be determined as part of a system factory calibration using an external signal, stored, and then programmed into the AD9361 in the field by writing these values into 0x141.

SPI Register 0x143—Config

[D6:D5] Calib Table Select<1:0> Bit D5 set accesses Rx1 and bit D6 accesses Rx2. When reading only one bit may be set.

[D4] Read Select When reading the errors, clear this bit to read mixer errors and set the bit to read LNA errors.

[D3] Write Mixer Error Table Set this bit to write the Mixer Gm Error words in 0x141. D2 & D1 must be clear. After writing all of the values, write to register 0x143 with the Write Mixer Error Table bit cleared but the Start Calib Table Clock bit still high. Then, write to 0x143 again with the clock start bit cleared. This ensures that the write signal resets before the clock stops.

[D2] Write LNA Error Table Set this bit to write the LNA Error words in 0x141. D3 and D1 must be clear. After writing all of the values, write to register 0x143 with the Write LNA Error Table bit cleared but the Start Calib Table Clock bit still high. Then, write to 0x143 again with the clock start bit cleared. This ensures that the write signal resets before the clock stops.

[D1] Write LNA Gain Diff Set this self-clearing bit to write gain difference words into 0x141. D3 & D2 must be clear. After the values have been programmed, write to register 0x143 with the Write LNA Gain Diff bit cleared but the Start Calib Table Clock bit still high. Then, write to 0x143 again with the clock start bit cleared. This ensures that the write signal resets before the clock stops.

[D0] Start Calib Table Clock Set this bit to access the Calibration Gain Table registers.

SPI Register 0x144—LNA Gain Diff Read Back

The LNA gain difference words written into register 0x141 can be read back from register 0x144. To read back these words, write the address of the table into register 0x140 and read the difference word from 0x144.

GENERAL CALIBRATION REGISTERS 145 THROUGH 149

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
145	*Max Mixer*	Open			Max Mixer Calibration Gain Index<4:0>					0Bh	R/W

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
	Calibration Gain Index										
146	*Temp Gain Coefficient*	Temp Gain Coefficient<7:0>								00h	R/W
147	*Settle Time*	Enable Dig Gain Corr	Force Temp Sensor for Cal	Settle Time<5:0>						10h	R/W
148	*Measure Duration*	Open				Gain Cal Meas Duration<3:0>				04h	R/W
149	*Cal Temp sensor word*	Cal Temp Sense word<7:0>								00h	R/W

SPI Register 0x145—Max Mixer Calibration Gain Index

This register is only used if the AD9361 performs a gain step calibration (see 0x016[D3]), in which case this register must be set to the mixer maximum gain index programmed in register 0x140. The default mixer table uses 0xF entries so this register would be set to 0xF.

SPI Register 0x146—Temp Gain Coefficient

This value is used with RSSI temperature compensation if that function is required in the application. This value would be measured during system characterization and represents the dependence of the LNA and Gm gain stages on temperature. A ratio of gain difference per ° C would first be determined and then coded in 2's complement notation to this register. The resolution is 0.0078dB with an approximate maximum of ±1dB/°C. Used with the "Cal Temp Sensor Word" in 0x149.

SPI Register 0x147—Settle Time

[D7] Enable Dig Gain Corr Set this bit to enable gain step error correction, after a gain step calibration has run. See 0x140.

[D6] Force Temp Sensor for Cal When the AD9361 compensates a parameter for temperature drift (e.g. RSSI or DCXO frequency), it does so by first calculating a temperature delta from a nominal value. Typically, a factory or bench-level test has already been performed which has characterized various parameters vs. temperature. During that test, the "nominal" temperature word is read from 0x00E and recorded along with a matrix of data. After programming the nominal temperature word into 0x149, setting this bit forces the AD9361 to use the value in 0x149 as the nominal value. During operation, the delta temperature would be the difference between 0x149 and 0x00E. This bit must be clear when running the Gain Step Calibration described in registers 0x140 through 0x143 but it must be set when (if) running a temperature vs. DCXO frequency sweep described in registers 0x298[D7]. Set it to enable any temperature compensation.

[D5:D0] Settle Time<5:0> This value specifies the time duration in clkRF cycles before the power measurement for the gain calibration algorithm at a specific gain starts. This delay allows the analog circuitry to settle. The default value of 0x10 is sufficient for most scenarios.

SPI Register 0x148—Measure Duration

This register specifies the duration of the power measurement used for gain calibration. The duration is per Equation 29.

$$Power\ Measurement\ Duration\ (ClkRF\ Cycles) = 2^{Gain\ Cal\ Meas\ Duration<3:0>}$$

Equation 29

SPI Register 0x149—Cal Temp Sensor Word

When Gain Step Calibration occurs, the AD9361 stores the temperature at which it occurred in this register. See 0x146.

RSSI MEASUREMENT CONFIGURATION REGISTERS 150 THROUGH 15D

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
150	*Measure Duration 0&1*	Measurement duration 1 <3:0>				Measurement duration 0 <3:0>				08h	R/W
151	*Measure*	Measurement duration 3 <3:0>				Measurement duration 2 <3:0>				--h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
	Duration 2&3										
152	*Weight 0*	Weighted Multiplier 0 <7:0>								00h	R/W
153	*Weight 1*	Weighted multiplier 1 <7:0>								00h	R/W
154	*Weight 2*	Weighted Multiplier 2 <7:0>								00h	R/W
155	*Weight 3*	Weighted Multiplier 3 <7:0>								00h	R/W
156	*RSSI delay*	RSSI Delay<7:0>								00h	R/W
157	*RSSI wait time*	RSSI Wait<7:0>								00h	R/W
158	*RSSI Config*	RFIR for RSSI measurement<1:0>		Start RSSI Meas (Mode 4)	RSSI Mode Select<2:0>			Enable ADC Power Meas.	Default RSSI Meas Mode	01h	R/W
159	*ADC Measure Duration 0&1*	ADC Power Measurement Duration 1<3:0>				ADC Power Measurement Duration 0 <3:0>				22h	R/W
15A	*Weight 0*	Weighted ADC Power Multiplier 0 <7:0>								00h	R/W
15B	*Weight 1*	Weighted ADC Power Multiplier 1 <7:0>								00h	R/W
15C	*Dec Power Measure Duration 0*	Use HB3 Out for ADC Pwr Meas	Use HB1 Out for Dec pwr Meas	Enable Dec Pwr Meas	Default Mode ADC Power	Dec Power Measurement Duration <3:0>				15h	R/W
15D	*LNA Gain*	Max LNA Gain<6:0>							dB Gain Read-back Channel	B1h	R/W

SPI Registers 150 and 151—Measure Duration 0,1,2,3

If the "Default RSSI Meas Mode" bit (0x158[D0]) is set, then Equation 30 sets the RSSI measurement duration.

$$RSSI\ Total\ Measurement\ Duration = 2^{Measurement\ Duration\ 0<3:0>}$$

Equation 30

All bits other than 0x150[D3:D0] are ignored. If the "Default RSSI Meas Mode" bit is clear, then Equation 31 describes the duration.

$$RSSI\ Total\ Measurement\ Duration = \sum_{i=0}^{3} 2^{Measurement\ Duration\ i<3:0>}$$

Equation 31

RSSI Total Measurement Duration is measured at the rate at the RFIR RSSI output sample rate (see register x158[D7:D6]).

The maximum value for any of these four nibbles is 0xE (not 0xF).

SPI Registers 152 through 155—Weight 0,1,2,3

Only applies if x158[D0] is clear. The RSSI Total Duration is a sum of 4 (possibly unequal) values so each of the 4 addends must be weighted. Calculate the weights per Equation 32 and program them into 0x152 - 0x155. The total of all weights must equal 0xFF.

$$Weight\ n = 255 * \left(\frac{2^{Measurement\ Duration\ n}}{RSSI\ Measurement\ Duration} \right)$$

Equation 32

SPI Registers 156 and 157—RSSI Delay and RSSI Wait

When an event occurs that starts the RSSI algorithm (see 0x158[D4:D2]), the AD9361 first waits for the "RSSI Delay" counter to expire, calculates RSSI, and then stuffs these values in x1A7 rough x1AE. After the first calculation, the algorithm waits for the "RSSI Wait" counter to expire. Another calculation occurs, after which the RSSI Symbol registers update but the RSSI Preamble registers do not. This process repeats until the AD9361 exits the Rx state or another event set by 0x158[D4:D2] restarts the algorithm. Figure 5 below shows an FDD example. RSSI Delay is clocked at the Rx Sample Rate divided by 8. RSSI Wait is clocked at the Rx Sample Rate divided by 4.

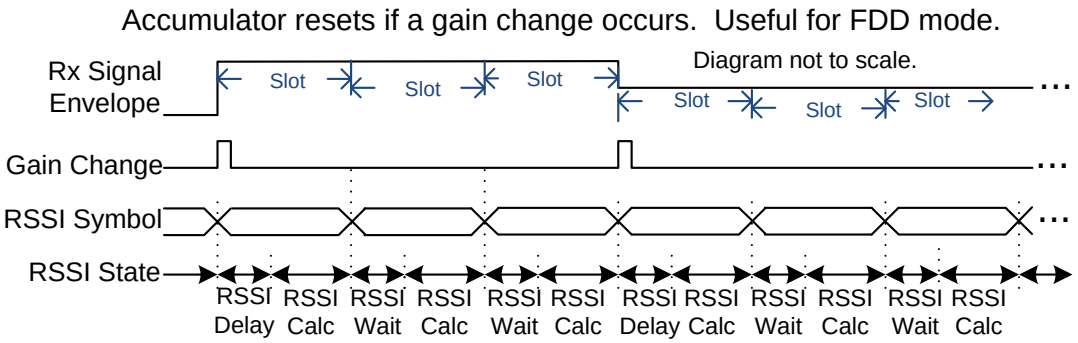

Figure 5. Example RSSI operation for FDD, using a Gain Change Event to trigger a reset of the RSSI Accumulator

SPI Register 158—RSSI Config

[D7:D6] RFIR for RSSI Measurement<1:0> Applies if the RFIR filter used for data is bypassed (see 0x003[D1:D0]). In this case, the RSSI calculation can still use the RFIR. Table 37 shows the encoding. If 0x003[D1:D0] ≠ 2'b00, then the AD9361 ignores 0x158[D7:D6].

0x158[D7:D6]	RSSI RFIR Decimation Factor & Filter Function
00	Decimate by 1 and Bypass Filter
01	Decimate by 1 and Enable Filter
10	Decimate by 2 and Enable Filter
11	Decimate by 4 and Enable Filter

Table 37. RSSI RFIR Decimation Factor and Filter Function

[D5] Enable RSSI Measurement Only applies if bits D4:D2 = 3'b100. Setting this bit restarts the RSSI algorithm.

[D4:D2] RSSI Mode Select<2:0> The RSSI algorithm (re)starts and clears its accumulator when the event(s) in Table 38 occur. If the EN_AGC pin is used, the RSSI Delay in 0x156 must be set to 0.

D4:D2	The RSSI Algorithm will (re)start when:
000	AGC in Fast Attack Mode Locks the Gain
001	EN_AGC pin is pulled High
010	AD9361 Enters Rx Mode
011	Gain Change Occurs
100	SPI Write to Register 0x158[D5]
101	Gain Change Occurs OR EN_AGC pin pulled High

Table 38. RSSI Mode

[D1] Enable ADC Power Measurement Setting this bit uses the ADC output or the HB3 output to measure power. See 0x15C[D7]. The noise correction factor in 0x0102 and 0x0103[D1:D0] must be set correctly.

[D0] Default RSSI Meas Mode See 0x150 & 0x151.

SPI Register 159—ADC Measurement Duration 0&1

If ADC Power Measurement is enabled (0x158[D1] set), these nibbles set the ADC power measurement duration. If the "Default Mode ADC Power" bit (0x15C[D4] is set, the Total Power Measurement Duration is set by Equation 33.

$$ADC\ Total\ Power\ Measurement\ Duration = 2^{ADC\ Power\ Measurement\ Duration\ 0}$$

Equation 33

If 0x15C[D4] is clear, the duration is set by Equation 34.

$$ADC\ Total\ Power\ Measurement\ Duration = 2^{ADC\ Power\ Measurement\ Duration\ 0} + 2^{ADC\ Power\ Measurement\ Duration\ 1}$$

Equation 34

Duration is in ADC clock cycles if "Use HB3 Output for ADC Pwr Meas" bit (0x15C[D7]) is clear or HB3 output cycles if that bit is set.

SPI Registers 15A and 15B—Weight 0,1

Only applies if 0x158[D1] is set and 0x15C[D4] is clear. Since the ADC power measurement is a sum of 2 (possibly unequal) values, each of the 2 addends must be weighted. Calculate the weights per Equation 35 and program them into 0x15A and 0x15B.

$$Weight\ n = 255 * \left(\frac{2^{\ ADC\ Power\ Measurement\ Duration\ n}}{ADC\ Total\ Power\ Measurement\ Duration}\right)$$

Equation 35

SPI Register 15C—Dec Power Measurement Duration

[D7] Use HB3 Out for ADC Pwr Meas Selects the HB3 output for power measurements if "Enable ADC Power Meas" (0x158[D1] is set.

[D6] Use HB1 Out for Dec Only applies if "Enable Dec Pwr Meas" (0x15C[D5]) is set. Setting this bit causes the AD9361 to use the output of the HB1 filter for the decimated power measurements. If this bit is clear, the output of the RFIR is used.

[D5] Enable Dec Pwr Meas Setting this bit enables the decimated power measurement block. See also bit D6.

[D4] Default Mode ADC Pwr Only applies if "Enable ADC Power Meas" bit (0x158[D1]) is set. See registers 0x15A & 0x15B.

[D3:D0] Dec Power Measurement Duration<3:0> The power measurement duration used by the gain control algorithm (not RSSI). The duration is per Equation 36 below.

$$Dec\ Power\ Meas\ Duration\ (Rx\ Sample\ Periods) = 16 * 2^{Dec\ Power\ Measurement\ Duration<3:0>}$$

Equation 36

SPI Register 15D—Max LNA Gain

[D7:D1] Max LNA Gain<6:0>The RSSI calculation uses this value. This register equals the maximum LNA gain in dB multiplied by 4, rounded and converted to hex. Resolution: 0.25dB.

[D0] dB Gain Readback Channel Once Gm and the internal LNA calibrations complete, the actual gain of the AD9361 can be determined by reading registers x1AD and x1AE.

POWER WORD REGISTERS 160 THROUGH 163

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
160	*CH1 ADC Power*	CH1 ADC power <7:0>								--h	R
161	*CH1 Rx filter Power*	CH1 Rx filter power <7:0>								--h	R
162	*CH2 ADC Power*	CH2 ADC power <7:0>								--h	R
163	*CH2 Rx filter Power*	CH2 Rx filter power <7:0>								--h	R

SPI Registers 0x160 and 0x162—CH1(2) ADC Power

Not used.

SPI Registers 0x161 and 0x163—CH1(2) Rx Filter Power

This read-only register holds the Rx1(2) power measured at the output of the RFIR filter or the HB1 filter in –dBFS with steps of 0.25dB/LSB. HB1 is used if the "Use HB1 out for Dec Pwr" bit (0x15C[D6]) is set.

RX QUADRATURE CALIBRATION REGISTERS 168 THROUGH 16F

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
168	*Rx Quad Cal Level*	Open				Rx Quad Cal Level <3 :0>				00	RW
169	*Calibration Config 1*	Enable Phase Corr	Enable Gain Corr	Use Settle Count for DC Cal Wait	Fixed DC Cal Wait Time	Free Run Mode	Enable Corr Word Decimation	Enable Tracking Mode CH 2	Enable Tracking Mode CH1	C0h	R/W
16A	*Calibration config2*	Soft Reset	Must be 2'b11		K exp Phase<4:0>					08h	R/W
16B	*Calibration config3*	Prevent Pos Loop Gain	Open		K exp Amplitude<4:0>					08h	
16C	*Calib count*	Calibration count<7:0>								FFh	R/W
16D	*Settle count*	Settle count<7:0>								00h	R/W
16E	*Rx Quad gain1*	Open	Rx Full table/LMT table gain<6:0>							0Bh	R/W
16F	*Rx Quad gain2*	Correction Word Decimation M<2:0>			Rx LPF gain<4:0>					18h	R/W

SPI Register 0x168—Rx Quad Cal Level

The initialization Rx Quadrature Cal algorithm uses a test tone which is provided by the Tx LO. This register sets the amplitude of the tone injected into the Mixer input, per Equation 37 below.

$$Tx\ Tone\ Level\ (mVpeak) = 8mVpeak * (Rx\ Quad\ Cal\ Level < 3:0 > +1)$$

Equation 37

SPI Register 0x169—Calibration Config 1

[D7] Enable Phase Corr Test bit, normally set. Set this bit to enable the phase correction feedback loop and algorithm.

[D6] Enable Gain Corr Test bit, normally set. Set this bit to enable the gain correction feedback loop and algorithm.

[D5] Use Settle Count for DC Cal Wait Not normally used. Only applies if "Fixed DC Cal Wait Time" (bit D4) is set. See Table 39.

[D4] Fixed DC Cal Wait Time Test bit, normally cleared. When an Rx Quad Cal starts, the Rx Quad Cal state machine first initiates an RF DC cal at the Rx gain index specified by registers 0x16E and 0x16F. Table 39 indicates when the Rx Quad Cal itself starts depending on the status of "Use Settle Count for DC Cal Wait" (bit D5) and "Fixed DC Cal Wait Time" (bit D4).

Fixed DC Cal Wait Time	Use Settle Count for DC Cal Wait	Action
0	X	Wait for DC Cal to finish before starting Rx Quad Cal
1	0	Start Rx Quad Cal immediately
1	1	Start Rx Quad Cal after Settle Count timer expires

Table 39. Start Time of Rx Quad Cal

[D3] Free run mode When clear, the calibration count value determines the duration of quadrature calibration. When set, the counters are disabled and the Quadrature calibration/tracking runs for as long as this bit is set. Set this bit for tracking mode.

[D2] Enable corr word decimation Setting this bit causes the algorithm to decimate the correction word before applying it to the data. See "Calib Count" (0x16C).

[D1] Enable tracking mode Ch2 Set to enable Rx Quadrature Tracking for Rx2.

[D0] Enable tracking mode Ch1 Set to enable Rx Quadrature Tracking for Rx1.

SPI Register 0x16A—Calibration Config 2

[D7] Soft Reset Resets all existing calculated phase and amplitude correction information to the defaults (zero). Not self-clearing.

[D4:D0] Kexp Phase<4:0> This is the scaling factor for the feedback path going to the phase accumulator per Equation 38. The equation below applies to power in the digital domain of 0dBFS. For every decrease of power of 6dB, the algorithm increases the exponent by 1. A an example, if the Kexp Phase<4:0> = 20 and the received power = 0dBFS, the exponent = -10. For a measured power level of -12dBFS, the exponent = -8. As the equation shows, it is possible to have positive exponents which can make the loop unstable for very low input power levels. It is recommended to set the "Prevent Pos Loop Gain" bit in 0x16B[D7] to make sure the exponent remains negative.

$$Scaling\ Factor = 2^{10 - Kexp\ Phase<4:0>}$$

Equation 38

SPI Register 0x16B—Calibration Config 3

[D7] Prevent Pos Loop Gain If set, the Rx quadrature calibration algorithm can only use negative loop gain.

[D4:D0] K exp amplitude<4:0> This is a scaling factor for the feedback path going to the gain accumulator per Equation 39. See additional information regarding the exponent in 0x16A[D4:D0].

$$Scaling\ Factor = 2^{10 - Kexp\ Amplitude<4:0>}$$

Equation 39

SPI Register 0x16C—Calib Count

This counter multiplied by 2048 sets the number of samples accumulated by the algorithm, clocked by ClkRF.

SPI Register 0x16D—Settle Count

This register value compensates for the delay encountered by the test tone through the analog and ADC paths.

SPI Register 0x16E—Rx Quad Cal Gain1

This is the receiver gain used when the AD9361 runs an Rx Quadrature Calibration using a test tone. The LNA gain is not relevant since the tone injects into the mixer input. For a full gain table (0x0FB[D3] clear), this register is the Gain Table Index and 0x16F[D4:D0] is not used. For a split gain table, 0x16E specifies the LMT Index and 0x16F[D4:D0] specifies the LPF index.

SPI Register 0x16F—Rx Quad Cal Gain 2

[D7:D5] Correction Word Decimation M<2:0> These bits control the decimation used by the accumulate and dump block of the Rx Quad Cal algorithm and are only applicable if 0x169[D2] = 1.

[D4:D0] LPF Gain See 0x16E.

RX PHASE AND GAIN CORRECTION REGISTERS 170 THROUGH 182

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
170	*Rx1 Input A Phase Corr*	Rx1 Input A Phase Correction<7:0>								--h	R/W
171	*Rx1 Input A Gain Corr*	Rx1 Input A Gain Correction<7:0>								--h	R/W
172	*Rx2 Input A Phase Corr*	Rx2 Input A Phase Correction<7:0>								--h	R/W
173	*Rx2 Input A Gain Corr*	Rx2 Input A Gain Correction<7:0>								--h	R/W
174	*Rx1 Input A "Q" Offset*	Rx1 Input A "Q" DC Offset<7:0>								--h	R/W
175	*Rx1 Input A Offsets*	Rx1 Input A "I" DC Offset<5:0>						Rx1 Input A "Q" DC Offset<9:8>		--h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
176	*Input A Offsets 1*	Rx2 Input A "Q" DC Offset<3:0>				Rx1 Input A "I" DC Offset<9:6>				--h	R/W
177	*Rx2 Input A Offsets*	Rx2 Input A "I" DC Offset<1:0>		Rx2 Input A "Q" DC Offset<9:4>						--h	R/W
178	*Rx2 Input A "I" Offset*	Rx2 Input A "I" DC Offset<9:2>								--h	R/W
179	*Rx1 Input B&C Phase Corr*	Rx1 Input B&C Phase Correction<7:0>								--h	R/W
17A	*Rx1 Input B&C Gain Corr*	Rx1 Input B&C Gain Correction<7:0>								--h	R/W
17B	*Rx2 Input B&C Phase Corr*	Rx2 Input B&C Phase Correction<7:0>								--h	R/W
17C	*Rx2 Input B&C Gain Corr*	Rx2 Input B&C Gain Correction<7:0>								--h	R/W
17D	*Rx1 Input B&C "Q" Offset*	Rx1 Input B&C "Q" DC Offset<7:0>								--h	R/W
17E	*Rx1 Input B&C Offsets*	Rx1 Input B&C "I" DC Offset<5:0>						Rx1 Input B&C "Q" DC Offset<9:8>		--h	R/W
17F	*Input B&C Offsets 1*	Rx2 Input B&C "Q" DC Offset<3:0>				Rx1 Input B&C "I" DC Offset<9:6>				--h	R/W
180	*Rx2 Input B&C Offsets*	Rx2 Input B&C "I" DC Offset<1:0>		Rx2 Input B&C "Q" DC Offset<9:4>						--h	R/W
181	*Rx2 Input B&C "I" Offset*	Rx2 Input B&C "I" DC Offset<9:2>									R/W
182	*Force Bits*	Rx2 Input B&C Force offset	Rx1 Input B&C Force offset	Rx2 Input B&C Force Ph/Gain	Rx1 Input B&C Force Ph/Gain	Rx2 Input A Force offset	Rx1 Input A Force offset	Rx2 Input A Force Ph/Gain	Rx1 Input A Force Ph/Gain	00h	R/W

SPI Register 0x170—Rx1 Input A Phase Corr

If 0x182[D0] is clear, after an Rx quad cal completes, this register holds the phase correction word for the signal path using input A of Rx1. Input selection is described in 0x004[D5:D0]. 2's compliment with a range of ±tan(7°). If 0x182[D0] is set, the value written to this register is the forced phase correction word.

SPI Register 0x171—Rx1 Input A Gain Corr

If 0x182[D0] is clear, after an Rx quad cal completes, this register holds the gain correction word for the signal path using input A of Rx1. Input selection is described in 0x004[D5:D0]. 2's compliment with a range of ±1dB. If 0x182[D0] is set, the value written to this register is the forced phase correction word.

SPI Register 0x172—Rx2 Input A Phase corr

Same as 0x170 but applies to Rx2. The force bit is0x182[D1].

SPI Register 0x173—Rx2 Input A Gain Corr

Same as 0x171 but applies to Rx2. The force bit is 0x182[D1].

SPI Register 0x174—Rx1 Input A "Q" Offset

If 0x182[D2] is clear, after an Rx Quad Cal completes, this register holds the least significant 8 bits of the value of the DC offset correction word in the Q signal path of Input A of Rx1. Input selection is described in 0x004[D5:D0]. 2's complement coded. If 0x182[D2] is set, the value written to this register is the forced DC offset correction word. The top two bits are in 0x175[D1:D0].

SPI Register 0x175—Rx1 Input A Offsets

[D7:D2] Rx1 Input A "I" Offset<5:0>Same as 0x174 but refers to the least significant 6 bits of the "I" path. The force bit is 0x182[D2].

[D1:D0] Rx1 Input A "Q" Offset<9:8> The two most significant bits of the Rx1 Input A "Q" Offset Correction word (see 0x174).

SPI Register 0x176—Input A Offsets

[D7:D4] Rx2 Input A "Q" Offset<3:0> Same as 0x174 but refers to the least significant 4 bits of Rx2. The force bit is 0x182[D3].

[D3:D0] Rx1 Input A "I" Offset<9:6> Same as 0x174 but refers to the most significant 4 bits of the "I" path. The force bit is 0x182[D2].

SPI Register 0x177-Rx2 Input A Offsets

[D7:D6] Rx2 Input A "I" Offset<1:0> Same as 0x174 but applies to the 2 least significant bits of the Rx2 "I" path. Force bit=0x182[D3].

[D5:D0] Rx2 Input A "Q" Offset<9:4> Same as 0x174 but applies to the most significant 6 bits of the Rx2 "Q" path. Force bit=0x182[D2].

SPI Register 0x178—Rx2 Input A "I" Offset

Same as register 0x174 but applies to the most significant 8 bits of the Rx2 "I" signal path.

SPI Register 0x179—Rx1 Input B&C Phase Corr

Same as register 0x170 but applies to the "B" and "C" LNA inputs. The force bit is 0x182[D4].

SPI Register 0x17A—Rx1 Input B&C Gain Corr

Same as register 0x171 but applies to the "B" and "C" LNA inputs. The force bit is 0x182[D4].

SPI Register 0x17B—Rx2 Input B&C Phase Corr

Same as register 0x172 but applies to the "B" and "C" LNA inputs. The force bit is 0x182[D5].

SPI Register 0x17C—Rx2 Input B&C Gain Corr

Same as register 0x173 but applies to the "B" and "C" LNA inputs. The force bit is 0x182[D5].

SPI Register 0x17D—Rx1 Input B&C "Q" Offset

Same as register 0x174 but applies to the "B" and "C" LNA inputs. The force bit is 0x182[D6].

SPI Register 0x17E—Rx1 Input B&C Offsets

Same as register 0x175 but applies to the "B" and "C" LNA inputs. The force bit is 0x182[D6].

SPI Register 0x17F—Input B&C Offsets 1

Same as register 0x176 but applies to the "B" and "C" LNA inputs. The force bit is 0x182[D6] for Rx1 and 0x182[D7] for Rx2.

SPI Register 0x180—Rx2 Input B&C Offsets

Same as register 0x177 but applies to the "B" and "C" LNA inputs. The force bit is 0x182[D7].

SPI Register 0x181—Rx2 Inputs B&C "I" Offset

Same as register 0x178 but applies to the "B" and "C" LNA inputs. The force bit is 0x182[D7].

SPI Register 0x182—Force Bits

These bits force the AD9361 to use the values in 0x170 through 0x181 as the Rx Quadrature Calibration correction words.

RX DC OFFSET CONTROL REGISTERS 185 THROUGH 194

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
185	*Wait Count*	Wait Count<7:0>								10h	R/W
186	*RF DC Offset Count*	RF DC Offset Count<7:0>								B4h	R/W
187	*RF DC Offset Config1*	Open		DAC FS<1:0>		RF DC Calibration Count<3:0>				1Ch	R/W
188	*RF DC Offset Attenuation*	RF DC Offset Table Update Count<2:0>			RF DC Offset Attenuation<4:0>					05h	R/W
189	*Invert Bits*	Invert Rx2 RF DC CGin Word	Invert Rx1 RF DC CGin Word	Invert Rx2 RF DC CGout Word	Invert Rx1 RF DC CGout Word	Open				30h	R/W
18A		Open								FFh	R/W
18B	*DC Offset Config2*	Use Wait Counter for RF DC Init Cal	Enable Fast Settle Mode	Enable BB DC Offset Tracking	Reset Acc on Gain Change	Enable RF Offset Tracking	DC Offset Update<2:0>			8Dh	R/W
18C	*RF Cal Gain Index*	Open	RF Minimum Calibration Gain Index<6:0>							00h	R/W
18D	*SOI Threshold*	Open	RF SOI Threshold<6:0>							64h	R/W
18E		Open								00h	R/W
18F		Open								--h	R/W
190	*BB DC Offset Shift*	Increase Count Duration	BB Tracking Decimate<1:0>		BB DC M Shift<4:0>					0Dh	R/W
191	*BB DC Offset Fast Settle Shift*	Read Back CH Sel	Update Tracking Word	Force Rx Null	BB DC Tracking Fast Settle M Shift<4:0>					06h	R/W
192	*BB Fast Settle Dur*	BB DC Tracking Fast Settle Duration<7:0>								03h	R/W
193	*BB DC Offset Count*	BB DC Offset Count<7:0>								3Fh	R/W
194	*BB DC Offset Attenuation*	Open				BB DC Offset Atten<3:0>				01h	R/W

"BB DC Offset" correction reduces analog LPF stage DC offset. "RF DC Offset" correction reduces LNA, Mixer, or TIA stage DC offset. These algorithms run during initialization and can "track" during normal operation. For the full gain table, RF DC offset runs at indices in the table that have the DC Cal bit set. For the split table, the cal runs at all LMT indices. The initial RF DC cal creates an internal table of calibrated gain indices vs. I and Q correction words. RF DC tracking runs during operation and updates the correction word table per to (0x18B[2:0]). The initial BB DC offset calibration also creates a table that maps each LPF index to I and Q correction words. BB DC tracking creates yet another correction word pair but only at the current gain index. These correction words are added to the RF DC

correction words and the initial BB DC correction words. While RF DC offset and tracking and the BB initial calibration accumulate-and-dump samples, BB DC tracking instead computes a running average that is divided down to create the correction words.

SPI Register 0x185 Wait Count

As the initial DC offset calibration algorithm steps through the gain indices, it must wait for the Rx path to settle before running the calibration at each gain index. BB DC cals and the RF DC tracking algorithm always wait for this counter to expire before running the calibration. There are 2 options for the RF DC initial calibration. If 0x18B[D7] is high, then the AD9361 uses the "Wait Count" value for this calibration as well. ADI recommends this setting as it ensures that the calibration always completes. If D7 of 0x18B is low (only applicable in for the Fast AGC), then the algorithm waits for the AGC to set "Gain Lock" high before calibrating at a particular index. A large input signal may prevent the algorithm from completing. ClkRF clocks the counter.

SPI Register 0x186—RF DC Offset Count

This register affects both RF DC Offset initialization and tracking. This register sets the number of integrated samples and the loop gain. The number of samples equals 256 * RF DC Offset Count<7:0> in ClkRF cycles. Increasing this value increases loop gain.

SPI Registers 0x187—DC Offset Config 1

[D5:D4] DAC FS<1:0> Sets the range of current injected by the correction DAC per Table 40. Increasing this value increases loop gain.

DAC FS<1:0>	DC Offset Correction Step Size
00	Default range of offset correction DAC
01	2x range & step-size of offset correction DAC
10	4x range & step-size of offset correction DAC
11	8x range &step-size of offset correction DAC

Table 40.DC Offset Correction Step Size

[D3:D0] RF DC Calibration Count<3:0> Applies only to the initial RF DC Offset calibration. This register specifies the number of times the integrated samples are accumulated at each calibrated gain index.

SPI Register 0x188—RF DC Offset Attenuation

[D7:D5] RF DC Offset Table Update Count<2:0> This register determines the number of table entries to update every time a correction word is updated in the RF correction table. This occurs for the initial RF cal and during tracking. If zero, the AD9361 updates the correction word at the current index. If the value is a non-zero value "n", the correction word at the current gain index "m" updates along with gain indices "m+1", "m+2", etc up to "m+n".

[D4:D0] RF DC Offset Attenuation<4:0> These bits control the loop gain attenuator for the initialization and tracking RF DC offset calibrations. The integrated data shifts by this value. The value is 2's complement, ranging from -16 to +15.

SPI Register 0x189—Invert Bits

[D7] Invert Rx2 RF DC CGin Word Test bit. Inverts the Rx2 CGin DC Offset correction word.

[D6] Invert Rx1 F DC CGout Word Test bit. Inverts the Rx1 CGin DC Offset correction word.

[D5] Invert Rx2 RF DC CGin Word Test bit. Inverts the Rx2 CGout DC Offset correction word.

[D4] Invert Rx1 F DC CGout Word Test bit. Inverts the Rx1 CGout DC Offset correction word.

SPI Register 0x18B – DC Offset Config2

[D7] Use Wait Counter See register 0x185.

[D6] Enable Fast Settle Mode Applies to BB DC Offset Tracking (D5 set) which speeds up convergence. The algorithm uses the "BB DC Tracking Fast Settle Shift M" attenuation value in 0x191 for "BB Tracking Fast Settle Count" time (0x192), followed by the "BB DC Shift M" attenuation value in 0x190. The value in 0x190 is used until the gain changes, at which time the fast settle mode repeats this sequence. If the "fast settle" attenuation value is lower than other attenuation value, then the BB DC tracking algorithm will converge more quickly. The algorithm *applies* correction words at a rate set by the decimation factor (0x190[D6:D5]) just as it does in normal

tracking mode. Note that fast convergence can lead to the algorithm affecting data that resides near DC so care must be taken when enabling this feature.

[D5] Enable BB DC Offset Tracking Setting this bit enables BB DC Offset tracking. The correction words apply at a rate set by the decimation setting (0x190[D6:D5]).

[D4] Reset Acc on Gain Change Only applies if using BB DC Offset tracking (bit D5 set). When this bit is set, the DC offset accumulator clears when a gain change occurs.

[D3] Enable RF Offset Tracking Setting this bit enables RF DC Offset tracking.

[D2:D0] DC Offset Update<2:0> This bits specify when correction words apply during RF tracking, per Table 41. See 0x18D for the "SOI Threshold".

D2	D1	D0
Gain Change	Rx Signal lower than SOI Threshold	Exit Rx Mode
Apply a new tracking word when a gain change occurs.	Apply a new tracking word when the received signal is less than the SOI Threshold.	Apply a new tracking word after the device exits the receive state.

Table 41.DC Offset Update Conditions

SPI Register0x18C—RF Cal Gain Index

This register sets the starting gain index for RF DC Offset calibration. This 7-bit word represents the LNA gain (2 bits), the Mixer Gm gain (4 bits) and the TIA gain (1 bit).

SPI Register 0x18D—RF SOI Threshold

This register sets the Signal of Interest Threshold in –dBFS with 1dB/LSB resolution. See 0x118B[D2:D0] (specifically bit D1).

SPI Register 0x190—BB DC Offset Shift

[D7] Increase Count Duration Applies in the initial BB DC calibration. This bit, along with "BB DC offset Count" (x193), determines the integration time for the initial BB DC Offset cal per Table 42.

Increase Count Duration	Integration Cycles
0	BB DC Offset Count * 256
1	BB DC Offset Count * 1024

Table 42. BB DC Offset Integration Cycles

[D6:D5] BB Tracking Decimation<1:0> Only applies in BB DC Offset Tracking Mode (bit D5 of 0x18B set). These bits set the correction word update rate per Table 43.

0x190[D6:D5]	Decimation	Update Rate
00	No decimation	ClkRF
01	By 2	ClkRF/2
10	By 4	ClkRF/4

Table 43.Decimation in BB DC Offset Tracking Mode

[D4:D0] BB DC Shift M<4:0> Applicable in BB DC Tracking Mode (bit D5 of 0x18B set). These bits determine the loop gain attenuation. The integrated data shifts by "BB DC M Shift" + 1. M ranges from 1 to 32. See 0x18B[D6].

SPI Register 0x191—BB DC Tracking Offset Fast Settle Shift

[D7] Read Back CH Sel Set to read back Rx1 correction words at 0x1A2 through 0x1A5. Clear to read Rx2 words. Also see D6.

[D6] Update Tracking Words Toggle this bit to copy the current BBDC tracking words to registers 0x1A2-0x1A5. Correction word updates occur quickly so these words are not copied to the SPI registers unless this bit transitions high to save power and also to prevent the words from changing during the SPI read itself. The bit is not self-clearing and must be cleared and set to copy the words again.

[D5] Force Rx Null Test bit. Setting this bit grounds the input to the Low Pass Filter.

[D4:D0] BB DC Tracking Fast Settle Shift M<4:0> Applies in BB DC Fast Settle Tracking mode (see 0x18B[D5:D6] set). Range 1-32.

SPI Register 0x192—BB Tracking Fast Settle Count

Only applies in BB DC Fast Settle Tracking mode (0x18B[D6:D5] set). These bits set the "Fast Settle M Shift" duration. See 0x18B[D6]. The total time is this register value * 8 and is measured in ClkRF cycles.

SPI Register 0x193—BB DC Offset Count

This register sets the "BB DC Offset Count" value shown in the tables and descriptions for bit D7 of 0x190 and bit D6 of 0x18B. Only applies to the non-tracking (initial) BB DC calibration.

SPI Register 0x194—BB DC Offset Attenuation

[D3:D0] BB DC Offset Atten<3:0> These bits set the BB DC Offset loop gain attenuation during the initial calibration. Range: +7 to -8.

RX BB DC OFFSET REGISTERS 19A THROUGH 1A5

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
19A	*RX1 BB DC word I MSB*	Open	RX1 BB DC Offset Correction word I<14:8>							--h	R
19B	*RX1 BB DC word I LSB*	RX1 BB DC Offset Correction word I<7:0>								--h	R
19C	*RX1 BB DC word Q MSB*	Open	RX1 BB DC Offset Correction word Q<14:8>							--h	R
19D	*RX1 BB DC word Q LSB*	RX1 BB DC Offset Correction word Q<7:0>								--h	R
19E	*RX2 BB DC word I MSB*	Open	RX2 BB DC Offset Correction word I<14:8>							--h	R
19F	*RX2 BB DC word I LSB*	RX2 BB DC Offset Correction word I<7:0>								--h	R
1A0	*RX2 BB DC word Q MSB*	Open	RX2 BB DC Offset Correction word Q<14:8>							--h	R
1A1	*RX2 BB DC word Q LSB*	RX2 BB DC Offset Correction word Q<7:0>								--h	R
1A2	*BB Track corr word I MSB*	Open	RX1/RX2 BB DC Offset Tracking correction word I<14:8>							--h	R
1A3	*BB Track corr word I LSB*	RX1/RX2 BB DC Offset Tracking correction word I<7:0>								--h	R
1A4	*BB Track corr word Q MSB*	Open	RX1/RX2 BB DC Offset Tracking correction word Q<14:8>							--h	R
1A5	*BB Track corr word Q LSB*	RX1/RX2 BB DC Offset Tracking correction word Q<7:0>								--h	R

All of the above read-only registers are test words used for internal debug purposes.

SPI Registers 0x19A-0x19D—Rx1 BB DC I/Q Words—Test Registers

These are the Rx 1 BB DC Offset I/Q correction words. During calibration, correction words are calculated for different LPF gains. The words read back in these registers are the correction word corresponding to the current LPF gain index.

SPI Registers 0x19E-0x1A1—Rx2 BB DC I/Q Words—Test Registers

Same as registers 0x19A through 0x19D but apply to Rx2.

SPI Registers 0x1A2-0x1A5—Rx1/2 BB Tracking Corr I/Q Words—Test Registers

These are the BB DC Offset Tracking I/Q correction words. When the "Read Back Ch Sel" bit reg0x191[7] is set, the words correspond to Rx1, else they correspond to Rx2. When BB DC Offset tracking is enabled (reg0x18B[5]), the words update every ClkRF cycle.

RSSI READBACK REGISTERS 1A7 THROUGH 1AE

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
1A7	*Rx1 RSSI Symbol*	Rx1 RSSI Symbol<8:1>								--h	R
1A8	*Rx1 RSSI preamble*	Rx1 RSSI preamble<8:1>								--h	R
1A9	*Rx2 RSSI symbol*	Rx2 RSSI symbol<8:1>								--h	R
1AA	*Rx2 RSSI preamble*	Rx2 RSSI preamble<8:1>								--h	R
1AB	*Symbol LSB*	Open						Rx2 RSSI symbol <0>	Rx1 RSSI symbol <0>	--h	R
1AC	*Preamble LSB*	Open						Rx2 RSSI preamble <0>	Rx1 RSSI preamble <0>	--h	R
1AD	*Rx Path Gain*	Rx Path Gain<8:1>								--h	R
1AE	*Rx Path Gain*	Open							Rx Path Gain<0>	--h	R

SPI Register 0x1A7 and 0x1AB[D0]—Rx1 RSSI Symbol

This register updates after every measurement interval. Range: 0 to -128. Resolution: 0.25dB/LSB for 9 bits, 0.5dB/LSB for 8 bits. RSSI compensates for Rx gain.

SPI Register 0x1A8 and 0x1AC[D0]—Rx1 RSSI Preamble

This register updates once after the event set in register 0x158[D4:D2] occurs with the exception that it does not update after gain changes (0x158[D4:D2] = 3'b011). Range: 0 to -128. Resolution: 0.25dB/LSB for 9 bits, 0.5dB for 8 bits. RSSI compensates for Rx gain.

SPI Register 0x1A9 and 0x1AB[D1]—Rx2 RSSI Symbol

Same as registers 0x1A& and 0x1AB[D0] but applies to Rx2.

SPI Registers 0x1AA and 0x1AC[D1]—Rx2 RSSI Preamble

Same as registers 0x1A8 and 0x1AC[D0] but applies to Rx2.

SPI Register 0x1AD and 0x1AE[D0]—Rx Path Gain

Gain in dB with resolution of 0.25dB and the channel selected by reg 15d[0].

RX LNA REGISTERS 1B0 THROUGH 1B3

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
1B0	*Rx Diff LNA Force*	Force Rx2 LNA Gain	Rx2 LNA Bypass	Rx2 LNA Gain<1:0>		Force Rx1 LNA Gain	Rx1 LNA Bypass	Rx1 LNA Gain<1:0>		00h	R/W
1B1	*Rx LNA Bias Coarse*	Open				Rx LNA Bias Coarse<3:0>				07h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
1B2	*Rx LNA Bias Fine 0*	Rx LNA p-Cascode Bias<2:0>			Rx LNA Bias<4:0>					C0h	R/W
1B3	*Rx LNA Bias Fine 1*	Open						Rx LNA p-Cascode Bias Fine<4:3>		03h	R/W

SPI Register 0x1B0—Rx Diff LNA Force—Test Register Only

[D7] Force Rx2 LNA Gain Test bit, normally clear. If set, D5:D4 force the Rx2 LNA gain independent of the gain table. See table in [D5:D4].

[D6] Rx2 LNA Bypass Normally cleared. Set this bit to bypass the Rx2 LNA. See the table below.

[D5:D4] Rx2 LNA Gain<1:0> Rx2 LNA gain, mapped per the table below.

Force Rx LNA Gain	Rx2 LNA Bypass	Rx2 LNA Gain<1:0>	LNA Gain @ 1GHz (dB)*
0	X	X	Set by Gain Table Index
1	0	00	20
1	0	01	17
1	0	10	15
1	0	11	6
1	1	11	6

Table 44.LNA Gain

*LNA absolute gain and gain steps are frequency-dependent and is for reference only.

[D3:D0] Same as the upper nibble but applies to Rx1.

SPI Register 0x1B1—Rx LNA Bias Coarse

Controls the fine LNA bias current per Table 45.

Rx LNA Coarse<3:0>	Current/Side (uA)
0000	0
0001	51*Iref
0011	102*Iref
0111	153*Iref
1111	204*Iref

Table 45.LNA Coarse Bias Current

Where Iref is set by the Rx LNA Bias Fine words in registers 0x1B2 and 0x1B3.

SPI Register 0x1B2 Rx LNA Bias Fine

[D7:D5] Rx LNA p-cascode<2:0> Table 46 maps the LNA p-cascode bias current to the 3 least significant bits in register 0x1B2 and the 2 most significant two bits in 0x1B3.

Rx LNA p-cascode Bias<4:0>	Bias Current (uA/side)
00000	500
00001	600
00011	700
00111	800
01111	900
11111	1000

Table 46.Rx LNA p-cascode Bias

[D4:D0] Rx LNA Bias<4:0> Fine bias for the Rx LNA, set per Table 47.

Rx LNA Bias<4:0>	Iref (uA)
00000	25
00001	30
00011	35
00111	40
01111	45
11111	50

Table 47.Rx LNA Bias

SPI Register 0x1B3—Rx LNA Bias Fine

The upper 2 bits of the LNA p-cascode bias mapped per Table 46 above.

RX MIX GM REGISTERS 1C0 THROUGH 1C4

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
1C0	*Rx Mix Gm Config*	Rx Mix Gm CM Out<2:0>			Open			Rx Mix Gm pload <1:0>		43h	R/W
1C1	*Rx1 Mix Gm Force*	Open	Force Rx1 Mix Gm	Rx1 Mix Gm Gain<5:0>						00h	R/W
1C2	*Rx1 Mix Gm Bias (Force)*	Open			Rx1 Mix Gm Bias<4:0>					00h	R/W
1C3	*Rx2 Mix Gm Force*	Open	Force Rx2 Mix Gm	Rx2 Mix Gm Gain<5:0>						00h	R/W
1C4	*Rx2 Mix Gm Bias (Force)*	Open			Rx2 Mix Gm Bias<4:0>					00h	R/W

SPI Register 0x1C0—Rx Mix Gm Config—Test Register

[D7:D5] Rx Mix Gm CM Out<2:0> These bits set the mixer GM output common mode voltage, mapped per Table 48.

Rx Mix Gm CM Out<2:0>	RX Mixer GM Output Common Mode Voltage, VDDA=1.3V (V)
0	0.89
1	0.85
2	0.81
3	0.77
4	0.72
5	0.69
6	0.65
7	0.6

Table 48.Rx Mixer GM Common Mode Output Voltage

[D1:D0] Rx Mix Gm pload<1:0> These bits set the number of pFET current sources turned on at the Gm load to this register value + 1.

SPI Register 0x1C1—Rx1 Mix Gm Force—Test Register Only-Do not change these bits

[D6] Force Rx1 Mix Gm Test bit, normally clear. If set, D5:D0 force the Rx1 Mixer gain independent of the gain table. See Table 49

[D5:D0] Rx1 Mix Gm Gain<5:0> Only applicable if D6 is set. This register, along with 0x1C2 sets the Mixer Gm gain per Table 49.

Mixer Gain Reduction	Gm Units	Bias Units	Mix Gm<5:0> (hex) (0x1C1 and 0x1C3)	Mix Gm Bias<4:0> (hex) (0x1C2 and 0x1C3)

Mixer Gain Reduction	Gm Units	Bias Units	Mix Gm<5:0> (hex) (0x1C1 and 0x1C3)	Mix Gm Bias<4:0> (hex) (0x1C2 and 0x1C3)
0	64	32	0	0
1	51	26	D	6
2	40	20	18	C
3	32	16	20	10
4	25	13	27	13
5	20	10	2C	16
6	16	8	30	18
7	14	8	32	18
8	13	8	33	18
9	11	8	35	18
10	10	8	36	18
11	9	8	37	18
12	8	8	38	18
13.2	7	8	39	18
14.5	6	8	3A	18
16.1	5	8	3B	18
18.0	4	8	3C	18
20.5	3	8	3D	18
24.0	2	8	3E	18
30.1	1	8	3F	18

Table 49. Mixer Gm Gain

SPI Register 0x1C2—Rx1 Mix Gm Bias (Force)

Only applicable if D6 is set. This register, along with 0x1C1[D5:D0] forces the gain of the Mixer Gm stage per Table 49.

SPI Registers 0x1C3 and 0x1C4

Same as registers 0x1C1 and 0x1C2 but applies to Rx2.

RX OFFSET DAC CGIN REGISTERS 1C8 THROUGH 1D2

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
1C8	*Input A MSBs*	Input A RX1 Q<9:8>		Input A RX1 I<9:8>		Input A RX2 I<9:8>		Input A RX2 Q<9:8>		--h	R/W
1C9	*Input A RX1 I*	Input A RX1 I<7:0>								--h	R/W
1CA	*Input A RX1 Q*	Input A RX1 Q<7:0>								--h	R/W
1CB	*Input A RX2 I*	Input A RX2 I<7:0>								--h	R/W
1CC	*Input A RX2 Q*	Input A RX2 Q<7:0>								--h	R/W
1CD	*Inputs B&C RX1 I*	Inputs B&C RX1 I<7:0>								--h	R/W
1CE	*Band1 RX1 Q*	Inputs B&C RX1 Q<7:0>								--h	R/W
1CF	*Inputs B&C RX2 I*	Inputs B&C RX2 I<7:0>								--h	R/W
1D0	*Inputs B&C RX2 Q*	Inputs B&C RX2 Q<7:0>								--h	R/W
1D1	*Inputs B&C MSBs*	Inputs B&C RX1 Q<9:8>		Inputs B&C RX1 I<9:8>		Inputs B&C RX2 I<9:8>		Inputs B&C RX2 Q<9:8>		--h	R/W

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
1D2	*Force OS DAC*	Open					Force CGin DAC	Open		00h	R/W

These test registers represent the offset DAC at the common gate (CG) inputs for various signal blocks. A value of 0 corresponds to a negative full scale DAC output, a value of 511 results in an output of zero, and a value of 1023 results in a positive full scale DAC output. Inputs "A" and "B&C" correspond to LNA inputs as described in 0x004[D5:D0].

SPI Register 0x1D2—Force OS DAC

Setting bit D2 overrides digital control of the CG input offset DAC, enabling control of the DAC outputs using registers 0x1C8-0x1D1.

RX MIXER REGISTERS 1D5 THROUGH 1D7

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
1D5	*Rx Mix LO CM*	Open		Rx Mix LO CM<5:0>						28h	R/W
1D6	*Rx CGB Seg Enable*	Open		Rx CGB Seg Enable<5:0>						4Fh	R/W
1D7	*Rx Mix Input/Bias*	Open		Rx CGB Input CM Sel<1:0>		Rx CGB Bias<3:0>				13h	R/W

SPI Register 0x1D5—Rx Mix LO CM

This register sets the value of the Rx mixer LO port common mode voltage, per Equation 40.

$$V_{CM} = \frac{VDD1P3_{RX_{RF}} * (Rx\ Mix\ LO\ CM < 5:0 > + 1)}{64}$$

Equation 40

SPI Register 0x1D6—Rx CGB Seg Enable

Enables up to six pFET and nFET current source segments in the RX common gate buffer. The word is thermometer encoded so the number of segments enabled equals the number of "1"s in this register.

SPI Register 0x1D7—Rx Mix Input/Bias

[D5:D4] Rx CGB Input CM Sel<1:0> These bits control the common mode voltage for the common gate buffer input per Table 50.

Rx CGB CM Sel<1:0>	V_{CM} (V)
00	0.3
01	0.4
10, 11	0.5

Table 50. Rx Common Gate Buffer Common Mode Voltage

[D3:D0] Rx CGB Bias<3:0> These bits control the Rx CG buffer bias current per current source segment. Thermometer encoded per Table 51.

Rx CGB Bias<3:0>	Current/Segment/Side (uA)
0000	83
0001	100
0011	125
0111	166
1111	250

Table 51.Rx CGB Bias

RX TIA REGISTERS 1DB THROUGH 1DF

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
1DB	*Rx TIA Config*	TIA Sel CC<2:0>			Open	TIA2 Override C	TIA2 Override R	TIA1 Override C	TIA1 Override R	60h	R/W
1DC	*TIA1 C LSB*	TIA1 RF<1:0>			TIA1 C LSB<5:0>					03h	R/W
1DD	*TIA1 C MSB*	Open	TIA1 C MSB<6:0>							0Bh	R/W
1DE	*TIA2 C LSB*	TIA2 RF<1:0>			TIA2 C LSB<5:0>					03h	R/W
1DF	*TIA2 C MSB*	Open	TIA2 C MSB<6:0>							0Bh	R/W

The initialization script normally sets the feedback capacitor value "C". This value used with a 3.5kΩ resistor sets the single-pole corner frequency at 0dB gain. In normal operation, the Gain Control circuit controls both R and C values, allowing the gain to change but keeping the corner constant. Override bits force R and C (i.e. ignore the digital controls coming from the Gain Control blocks).

SPI Register 0x1DB—Rx TIA Config

[D7:D5] TIA Sel CC<2:0> These bits must be set per Table 52.

Baseband (Real) Bandwidth (BBBW)	TIA Sel CC<2:0>
BBBW ≤3MHz	7
3MHz< BBBW < 10MHz	3
BBBW ≥ 10MHz	1

Table 52. TIA Sel CC

[D3] TIA 2 Override C Test bit. Override digital control of the RX2 TIA feedback capacitors with TIA2 C LSB and TIA2 C MSB.

[D2] TIA 2 Override R Test bit. Override digital control of the RX2 TIA feedback resistor with TIA2 RF CNT.

[D1] TIA 1 Override C Test bit. Same as bit D3 but applies to Rx1.

[D0] TIA 1 Override R Test bit. Same as bit D2 but applies to Rx1.

SPI Register 0x1DC—TIA C LSB

[D7:D6] TIA 1 RF CNT<1:0> Sets the value of the feedback resistor in the Rx1 TIA per Table 53 "TIA 1 Override R" is set (0x1DB[D0]).

TIA RF<1:0>	R_{TIA}	Gain (dB)
01	3.50kΩ	0
11	1.75kΩ	-6

Table 53. TIA Forced Feedback Resistor Value

[D5:D0] TIA C LSB<5:0> Sets lower 6 bits of the value of the feedback capacitor. See Table 54 where the upper 7 bits are set.

SPI Register 0x1DD—TIA 1 C MSB

Sets the upper 7 bits of the feedback capacitor per Table 54. For nominal process corner,

$$Feedback\ Capacitance\ (CTIA) = 400fF + 320fF * TIA\ C\ MSB + 40fF * TIA\ C\ LSB$$

Equation 41

CTIA	TIA C MSB<6:0>	TIA C LSB<5:0>
>2.92pF	$\frac{C_{TIA} - 400\,fF}{320\,fF}$	0
<2.92pF	0	$\frac{C_{TIA} - 400\,fF}{40\,fF}$

Table 54. TIA Feedback Capacitor

SPI Registers 0x1DE and 0x1DF

Same as registers 0x1DC and 0x1DD but apply to Rx2. The override bit for the Rx2 feedback resistor is D2.

RX BBF REGISTERS 1E0 THROUGH 1F5

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
1E0	*Rx1 BBF R1A*	Force Rx1 Resistors	Open	Rx1 BBF R1A<5:0>						03h	R/W
1E1	*Rx2 BBF R1A*	Force Rx2 Resistors	Open	Rx2 BBF R1A<5:0>						03h	R/W
1E2	*Rx1 Tune Control*	Open					Rx1 Tune Resample Phase	Rx1 Tune Resample	Rx1 PD Tune	00h	R/W
1E3	*Rx2 Tune Control*	Open					Rx2 Tune Resample Phase	Rx2 Tune Resample	Rx2 PD Tune	00h	R/W
1E4	*Rx1 BBF R5*	Rx1 BBF R5<7:0>								01h	R/W
1E5	*Rx2 BBF R5*	Rx2 BBF R5<7:0>								01h	R/W
1E6	*Rx BBF R2346*	Tune Override	Open				Rx BBF R2346<2:0>			01h	R/W
1E7	*Rx BBF C1 MSB*	Open		Rx BBF C1 MSB<5:0>						00h	R/W
1E8	*Rx BBF C1 LSB*	Open	Rx BBF C1 LSB<6:0>							60h	R/W
1E9	*Rx BBF C2 MSB*	Open		Rx BBF C2 MSB<5:0>						00h	R/W
1EA	*Rx BBF C2 LSB*	Open	Rx BBF C2 LSB<6:0>							60h	R/W
1EB	*Rx BBF C3 MSB*	Open		Rx BBF C3 MSB<5:0>						00h	R/W
1EC	*Rx BBF C3 LSB*	Open	Rx BBF C3 LSB<6:0>							60h	R/W
1ED	*Rx BBF CC1 Ctr*	Open	Rx BBF CC1 Ctr<6:0>							07h	R/W
1EE	*Rx BBF Pow Rz Byte0*	Must be zero	Rx1 BBF Pow Ctr<1:0>		Rx BBF Rz1 Ctr<1:0>		Open			60h	R/W
1EF	*Rx BBF CC2 Ctr*	Open	Rx BBF CC2 Ctr<6:0>							07h	R/W
1F0	*Rx BBF Pow Rz Byte1*	Rx BBF Pow3 Ctr<1:0>		Rx BBF RZ3 Ctr<1:0>		Rx BBF Pow2 Ctr<1:0>		Rx BBF Rz2 Ctr<1:0>		CCh	R/W
1F1	*Rx BBF CC3 Ctr*	Open	Rx BBF CC3 Ctr<6:0>							07h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
1F2	*Rx BBF R5 Tune*	Rx BBF R5 Tune<7:0>								00h	R/W
1F3	*Rx BBF Tune*	RxBBF Bypass Bias R	Rx BBF Tune Ctr<1:0>		Rx BBF R5 Tune	Rx1 BBF Tune Comp I	Rx1 BBF Tune Comp Q	Rx2 BBF Tune Comp I	Rx2 BBF Tune Comp Q	20h	R/W
1F4	*Rx1 BBF Man Gain*	Open		Rx1 BBF Force Gain	Rx1 BBF BQ Gain<1:0>		Rx1 BBF Pole Gain<2:0>			00h	R/W
1F5	*Rx2 BBF Man Gain*	Open		Rx2 BBF Force Gain	Rx2 BBF BQ Gain<1:0>		Rx2 BBF Pole Gain<2:0>			00h	R/W

0x1E0-0x1F5 are test registers, not normally accessed. Calibrating the Rx BBF requires writing to registers 0x1F8-0x1FC and then initiating an Rx BBF Calibration (bit D7 in 0x016).

SPI Register 0x1E0--Rx1 BBF R1A

[D7] Force Rx1 Resistors Test bit, should be normally cleared. Setting this bit forces the use of the resistor register values.

[D5:D0] Rx1 BBF R1A<5:0> This register in combination with R4 (0x1E6) sets the Bi-Quad signal gain (R4/R1A = Av). See Table 55.

Rx1 BBF R1A<5:0>	R1A Value (Ohms)	Rx BBF R2346<2:0>	R4 Value (Ohms)	Bi Quad Gain (dB)
001000	16k	001	16k	0
001100	8k	001	16k	6
000010	4k	001	16k	12
000011	2k	001	16k	18
110000	32k	010	32k	0
001000	16k	010	32k	6
001100	8k	010	32k	12
000010	4k	010	32k	18
100000	64k	100	64k	0
110000	32k	100	64k	6
001000	16k	100	64k	12
001100	8k	100	64k	18

Table 55. R1A and R4 vs. BiQuad Gain

SPI Register 0x1E1—Rx2 BBF R1A

Same as register 0x1E0 but applies to Rx2.

SPI Register 0x1E2—Rx1 Tune Control

[D2] Rx1 Tuner Resampler Phase Test bit. Set to use div 8 bar for resampler, clear to use div 8 to resample. Bits D2 and D1 are for use only to correct unlikely synchronization issues between analog and digital.

[D1] Rx1 Tuner Resample Test bit. Set to bypass resampler, clear to resample to div 8.

[D0] Rx1 PD Tune *Clear* this bit to force tuner (calibration circuit) on. If this bit is *set* the digital calibration state machine controls the power on/off state of the tuner. In this case, the state machine will enable the tuner for a calibration and then disable it afterwards. This mode is *not* recommended. Instead, the Rx BBF calibration circuit should be manually powered up for calibration and then powered down after calibration. Specifically, to tune BBF, clear the PD Tune bit and allow analog path to settle. Tune BBF then set PD Tune bit.

SPI Register 0x1E3—Rx2 Tune Control

Same as 0x1E2 but applies to Rx2

SPI Register 0x1E4—Rx1 BBF R5—Test Register Only-- Do not change these bits

This register along with R6 (0x1E6) controls the pole signal gain (R6/F5 = Av) per Table 56. *If this register is non-zero, 0x1F2 must be zero.*

Rx BBF R5<7:0>	R5 (Ohms)	Rx BBF R2346<2:0>	R6 Value (Ohms)	Gain (dB)
10011000	18286	001	18.3k	0
01001100	16297	001	18.3k	1
00100110	14525	001	18.3k	2
10110010	12945	001	18.3k	3
01010110	11538	001	18.3k	4
11011010	10283	001	18.3k	5
00111110	9165	001	18.3k	6
00000001	4593	001	18.3k	12
00000010	36571	010	32.6k	0
10100000	32594	010	32.6k	1
01010000	29050	010	32.6k	2
00101000	25891	010	32.6k	3
00010100	23075	010	32.6k	4
00001010	20566	010	32.6k	5
10011000	18329	010	32.6k	6
00111110	9186	010	32.6k	12
10000000	73143	100	73.2k	0
01000000	65189	100	73.2k	1
00100000	58099	100	73.2k	2
00010000	51781	100	73.2k	3
00001000	46150	100	73.2k	4
00000100	41131	100	73.2k	5
00000010	36658	100	73.2k	6
10011000	18373	100	73.2k	12

Table 56.Rx BBF Pole Gain

SPI Register 0x1E5—Rx2 BBF R5—Test Register Only-- Do not change these bits

Same as register 0x1E4 but applies to Rx2.

SPI Register 0x1E6—Rx BBF R2346—Test Register Only-- Do not change these bits

[D7] Tune Override Setting this bit overrides the calibration values, forcing the filter to use the R2346 value and all capacitor words.

[D2:D0] Rx BBF R2346 These bits control the value of resistors R2, R3, R4, and R6 per Table 57.

Rx BBF R2346<2:0>	R2 (Ohms)	R3 (Ohms)	R4(Ohms)	R6(Ohms)
001	5.3K	9.3K	16K	18.3K
010	10.6K	18.6K	32K	36.6K
100	21.2K	37.3K	64K	73.2K

Table 57. Rx BBF R2, R3, R4, R6

SPI Register 0x1E7 and 0x1E9—Rx BBF C1 & 2 MSB—Test Register Only-- Do not change these bits

These bits affect the C1 & C2 BBF capacitors. Binary weighted from 0 to 20.16pF in 320fF steps with an offset of 280fF. Typically, both registers, along with 0x1EB, should have the same control word.

SPI Registers 0x1E8 and 0x1EA—Rx BBF C1& 2 LSB--Test Register Only-- Do not change these bits

These bits affect the C1 & C2 BBF capacitors. Binary weighted from 0 to 2.54pF using 20fF steps with an offset of 280fF. Typically, all three registers, along with 0x1EC, should have the same control word.

SPI Register 0x1EB—Rx BBF C3 MSB--Test Register Only-- Do not change these bits

These bits affect the C3 BBF capacitor. Binary weighted from 0 to 10.08pF in 160fF steps with an offset of 140fF. Typically equal to 0x1E7 and 0x1E9.

SPI Register 0x1EC—Rx BBF C3 LSB--Test Register Only-- Do not change these bits

These bits affect the C3 BBF capacitor. Binary weighted from 0 to 1.27pF in 10fF steps with an offset of 140fF. Typically equal to 0x1E8 and 0x1EA.

SPI Register 0x1ED—Rx BBF CC1 Ctr--Test Register Only-- Do not change these bits

These bits control the Miller compensation capacitor for OpAmp 1. Binary weighted from 60fF to 6pF with 60fF/LSB.

SPI Register 0x1EE—Rx BBF Pow RZ --Test Register Only-- Do not change these bits

[D6:D5] Rx BBF Pow Ctr<1:0> Power control for OpAmp1, mapped per Table 58. Set to 2'b11.

Rx BBF Ctr<1:0>	Bias Current(uA/Leg)
00	200
10	300
10	400
11	500 (recommended)

Table 58.Rx BBF bias current

[D4:D3] Rx BBF Rz1 Ctr<1:0> Controls the OpAmp 1 zero compensation resistor. Set to 2'b00. Mapped per Table 59.

Rx BBF Rz1 Ctr<1:0>	Zero Compensation Resistor (Ohms)
00	1500
01, 10	750
11	500

Table 59. Rx BBF Zero Compensation Resistor

SPI Register 0x1EF—Rx BBF CC2 Ctr—Test Register Only-- Do not change these bits

Same as 0x1ED but applies to OpAmp2.

SPI Register 0x1F0—Rx BBF Pow Rz Byte1—Test Register Only-- Do not change these bits

[D7:D6] Rx BBF Pow 3 Ctr <1:0>OpAmp 3 power control. Mapped per Table 58.

[D5:D4] Rx BBF Rz Ctr<1:0> OpAmp 3 zero compensation resistor, mapped per Table 59.

[D3:D2] Rx BBF Pow 2 Ctr<1:0> OpAmp 2 power control, mapped per Table 58.

D1:D0] Rx BBF Rz Ctr<1:0> OpAmp 2 zero compensation resistor, mapped per Table 59.

SPI Register 0x1F1—Rx BBF CC3 Ctr—Test Register Only-- Do not change these bits

Same as 0x1ED but applies to OpAmp 3.

SPI Register 0x1F2—Rx BBF R5 Tune—Test Register Only-- Do not change these bits

This register along with the value of R6 (0x1E6) sets the pole signal gain during calibration. *If this is non-zero, 0x1E$ and 0x1E5 must be all zeros.* The gain steps are 0, 3, and 6dB. 6dB is not available for the highest frequency band. Table 60 below shows valid combinations.

Rx BBF R5 Tune<7:0>	R5 (Ohms)	R6 (Ohms)	Gain (dB)
10011000	18286	18.3k (high band)	0
10110010	12945	18.3k (high band)	3
00000010	36571	32.6k (Mid Band)	0
00101000	25891	32.6k (Mid Band)	3
10011000	18329	32.6k (Mid Band)	6
10000000	73143	73.2k (Low Band)	0
00010000	51781	73.2k (Low Band)	3
00000010	36658	73.2k (Low Band)	6

Table 60. R5 Tune

SPI Register 0x1F3—Rx BBF Tune—Test Register Only-- Do not change these bits

[D7] Rx BBF Bypass Bias R Setting this bit bypasses the OpAmp bias resistors. Always keep this bit cleared.

[D6:D5] Rx BBF Tune Ctr<1:0> These bits control the common mode voltage. Vcm = 660mV for 2'b01 and Vcm = 670mV for 2'b10. Other settings not valid. Always set to 660mV.

[D4] RxBBF R5 Tune Setting this bit forces the value in 0x1F2 to be used for tuning.

[D3:D0] Rx1/2 BBF Tune Comp I/Q These read-only bits are the tuning comparator outputs. See 0x1F9 (Tune Mode) for details.

SPI Registers 0x1F4 and 0x1F5—Rx1/2 BBF Man Gain—Test Register Only-- Do not change these bits

[D5] Rx BBF Force Gain Forces the values in the lower bits to be used for the BiQuad and Pole gain.

[D4:D3] Rx BBF BQ Gain <1:0> Only applicable if D5 is set. These bits force the BiQuad Gain per Table 61.

Rx BBF BQ Gain <1:0>	Rx BBF Bi Quad Gain
0	0 dB
1	6dB
2	12dB
3	18dB

Table 61.Rx BBF BiQuad Gain

[D2:D0] Rx BBF Pole Gain<1:0> Only applicable if D5 is set. These bits force the Pole Gain per Table 62.

Rx BBF Pole Gain<1:0>	Rx BBF Real Pole Gain
0	0 dB
1	1dB
2	2dB
3	3dB
4	4dB
5	5dB
6	6dB
7	12dB

Table 62.Rx BBP Pole Gain

RX BBF TUNER CONFIGURATION REGISTERS 1F8 THROUGH 1FC

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
1F8	*RX BBF Tune Divide*	RX BBF Tune Divide<7:0>								14h	R/W
1F9	*RX BBF Tune Config*	Open	Tune Comp Mask <1:0>		Rx Tune Evaltime	Rx Tune Mode<2:0>			RX BBF Tune Divide<8>	1Eh	R/W
1FA	*Pole gain*	Open						Pole Gain Tune<1:0>		01h	R/W
1FB	*Rx BBBW MHz*	Open			Rx Tune BBBW MHz<4::0>					05h	R/W
1FC	*Rx BBBW kHz*	Open	Rx Tune BBBW kHz<6:0>							00h	R/W

The BBP must write to some of these registers with the correct setup values before the Rx BBF calibration routine runs.

0x1F8 & 0x1F9[D0]—Rx BBF Tune Divide

The tuning algorithm must be driven with a "tune clock" that is dependent on the BBPLL frequency as well as the baseband (real) bandwidth (BBBW) multiplied by a constant. This register sets a divider that outputs the tune clock, set per Equation 42. See the Calibration User Guide for more information about the tune clock used for the calibration algorithm.

$$Rx\ BBF\ Tune\ Divide < 8:0 > = ceil\left(\frac{BBPLL\ Frequency * \ ln(2)}{BBBW * 1.4 * 2 * \pi}\right)$$

Equation 42

The range of the divider is 1 to 511 where the 9 bits map directly to the divider value. A register value of zero is not valid.

0x1F9—Rx BBF Tune Config

[D6:D5] Tune Comp Mask<1:0> Test bits, normally cleared. These bits select which, if any, tune comparator output should be masked when evaluating tuning. 2'b00 uses both channels. 2'b01 masks Rx2. 2'b10 masks Rx1. 2'b11 is unused. It is not necessary to set these bits according to the receiver(s) that are enabled. All filters turn on during tuning so there is no need to mask the outputs.

[D4] Rx Tune Evaltime This bit sets the delay in tune clock cycles (set by the divider described above) before the tune comparator outputs should be sampled. 0 = 16 cycles and 1 = 32 cycles.

[D3:D1] Rx Tune Mode<2:0> These bits, mapped per Table 63, determine when the BBF algorithm stops.

Rx Tune Mode<2:0>	Action
000	Evaluate using Rx2 BBF Tune Comp Q only
001	Evaluate using Rx2 BBF Tune Comp I only
010	Evaluate using Rx1 BBF Tune Comp Q only
011	Evaluate using Rx1 BBF Tune Comp I only
100	Evaluate all comparator signals. Stop tuning after any 1 of them is low.
101	Evaluate all comparator signals. Stop tuning after any 2 of them are low.
110	Evaluate all comparator signals. Stop tuning after any 3 of them are low.
111	Evaluate all comparator signals. Stop when all are low.

Table 63. Rx BBF Tune Mode

0x1FA—Pole Gain

These bits force the pole stage gain during tuning per Table 64.

Pole Gain<1:0>	Gain (dB)
00	0dB
01	3dB (default)
10	6dB
11	Invalid

Table 64.Rx BBF Pole Gain

0x1FB—Rx BBBW MHz

Program this register with floor (Rx Baseband (real) BW) to set the Rz and Cc of the filter. E.g. if the channel (RF) BW = 10MHz, Rx BBBW MHz = floor(10/2) = 5MHz. Range: 0 to 31MHz. Resolution: 1MHz/LSB. The tune clock (0x1F8) sets the filter corner.

0x1FC—Rx BBBW kHz

The BBP must program this register per Equation 43.

$$Rx\ Tune\ BBBW\ kHz < 6:0 >= Round\left(\frac{\left(BBBW - floor\ (BBBW)\right) * 1000}{7.8125}\right)$$

Equation 43

RX ADC REGISTERS 201 THROUGH 226

Register Address	*Name*	D7 D6 D5 D4 D3 D2 D1 D0	Default	R/W
200	*Not Used*	Not Used	00h	R/W
201	*FB DAC Clk Delay1*	FB DAC Clk Delay1<7:0>	00h	R/W
202	*FB DAC Clk Delay2*	FB DAC Clk Delay2<7:0>	00h	R/W
203	*Flash Sample Clk Delay 3p*	Flash Sample Clk Delay 3p<7:0>	24h	R/W
204	*Flash Sample Clk Delay 3p*	Flash Sample Clk Delay 3n<7:0>	24h	R/W
205	*Test MUX 2i*	Test MUX 2i<7:0>	00h	R/W
206	*Test MUX 2q*	Test MUX 2q<7:0>	00h	R/W
207	*Integrator 1 Resistance*	Integrator 1 Resistance<7:0>	28h	R/W
208	*Integrator 1 Capacitance*	Integrator 1 Capacitance<7:0>	14h	R/W
209	*Integrator 23 Resistance*	Integrator 23 Resistance<7:0>	20h	R/W
20A	*Integrator 2 Resistance*	Integrator 2 Resistance<7:0>	28h	R/W
20B	*Integrator 2 Capacitance*	Integrator 2 Capacitance<7:0>	14h	R/W
20C	*Integrator 3 Resistance*	Integrator 3 Resistance<7:0>	28h	R/W
20D	*Integrator 3 Capacitance*	Integrator 3 Capacitance<7:0>	14h	R/W
20E	*Integrator Amp Cc*	Integrator Amplifier Compensation Capacitor<7:0>	00h	R/W
20F	*Int 1 FB DAC NMOS Current Source*	Integrator 1 FB DAC Current Source<7:0>	29h	R/W
210	*Int 1 FB DAC NMOS Casoade Bias Current*	Integrator 1 FB DAC Cascade Bias Current<7:0>	29h	R/W
211	*Int 1 FB DAC PMOS Current Source*	Integrator 1 FB DAC Current Source<7:0>	29h	R/W
212	*Int 2 FB DAC NMOS Current Source*	Integrator 2 FB DAC Current Source<7:0>	27h	R/W
213	*Int 2 FB DAC NMOS Cascode Bias Current*	Integrator 2 FB DAC Cascade Bias Current<7:0>	27h	R/W
214	*Int 2 FB DAC PMOS Current Source*	Integrator 2 FB DAC Current Source<7:0>	27h	R/W
215	*Int 3 FB DAC NMOS Current Source*	Integrator 3 FB DAC Current Source<7:0>	27h	R/W
216	*Int 3 FB DAC NMOS Cascode Bias Current*	Integrator 3 FB DAC Cascade Bias Current<7:0>	27h	R/W
217	*Int 3 FB DAC PMOS Current Source*	Integrator 3 FB DAC Current Source<7:0>	27h	R/W
218	*FB DAC Bias Current*	FB DAC Bias Current<7:0>	2Eh	R/W
219	*Int 1 1st Stage Current*	Integrator 1 1st Stage Current<7:0>	90h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
21A	*Int 1 1st Stage Cascode Current*	Integrator 1 1st Stage Cascode Current<7:0>								15h	R/W
21B	*Int 1 2nd Stage Current*	Integrator 1 2nd Stage Current<7:0>								10h	R/W
21C	*Integrator 2 1st Stage Current*	Integrator 2 1st Stage Current<7:0>								90h	R/W
21D	*Int 2 1st Stage Cascode Current*	Integrator 2 1st Stage Cascode Current<7:0>								15h	R/W
21E	*Int 2 2nd Stage Current*	Integrator 2 2nd Stage Current<7:0>								10h	R/W
21F	*Int 3 1st Stage Current*	Integrator 3 1st Stage Current<7:0>								90h	R/W
220	*Int 3 1st Stage Cascode Current*	Integrator 3 1st Stage Cascode Current<7:0>								15h	R/W
221	*Int 3 2nd Stage Current*	Integrator 3 2nd Stage Current<7:0>								20h	R/W
222	*Flash Bias Current*	Flash Bias Current<7:0>								20h	R/W
223	*Flash Ladder Bias*	Flash Ladder Bias<7:0>								40h	R/W
224	*Flash Ladder Cascode Current*	Flash Ladder Cascode Current<7:0>								40h	R/W
225	*Flash Ladder Bias2*	Flash Ladder Bias<7:0>								2Ch	R/W
226	*Reset*	Reset<7:0>								00h	R/W

The receive ADCs are 3rd order continuous time delta sigma modulators. The above register settings are dependent on several variables so equations should be used during initialization to determine the register values as described in the Calibration User Guide.

ANALOG REGISTERS

RX SYNTHESIZER REGISTERS 230 THROUGH 251

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
230	*PFD Config*	Open		Div Test En	Open	PFD Width <1:0>		PFD Clk Edge	Bypass Ld Synth	54h	R/W
231	*Integer Byte 0*	Synthesizer Integer Word<7:0>								00h	R/W
232	*Integer Byte 1*	SDM Bypass	SDM Power Down	Open			Synthesizer Integer Word<10:8>			00h	R/W
233	*Fractional Byte 0*	Synthesizer Fractional Word<7:0>								00h	R/W
234	*Fractional Byte 1*	Synthesizer Fractional Word <15:8>								00h	R/W
235	*Fractional Byte 2*	Open	Synthesizer Fractional Word <22:16>							00h	R/W
236	*Force ALC*	Force ALC Enable	Force ALC Word<6:0>							00h	R/W
237	*Force VCO Tune 0*	Force VCO Tune<7:0>								00h	R/W
238	*Force VCO Tune 1*	Bypass Load Delay	VCO Cal Offset<3:0>				Open	Force VCO Tune Enable	Force VCO Tune<8>	00h	R/W
239	*ALC/Varactor*	Init ALC Value<3:0>				VCO Varactor<3:0>				82h	R/W
23A	*VCO Output*	Open	PORb VCO Logic	Open		VCO Output Level<3:0>				0Ah	R/W
23B	*CP Current*	Set to 1	Vtune Out	Charge Pump Current<5:0>						00h	R/W
23C	*CP Offset*	Synth Re-Cal	Open	Charge Pump Offset<5:0>						00h	R/W
23D	*CP Config*	Half Vco	Dither	Open	Cp	F Cpcal	Cp Cal	Cp Test <1:0>		80h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
		Cal Clk	Mode		Offset Off		Enable				
23E	*Loop Filter 1*	Loop Filter C2<3:0>				Loop Filter C1<3:0>				00h	R/W
23F	*Loop Filter 2*	Loop Filter R1<3:0>				Loop Filter C3<3:0>				00h	R/W
240	*Loop Filter 3*	Loop Filter Bypass R3	Loop Filter Bypass R1	Loop Filter Bypass C2	Loop Filter Bypass C1	Loop Filter R3<3:0>				00h	R/W
241	*Dither/CP Cal*	Number SDM Dither Bits<3:0>				Forced CP Cal Word<3:0>				00h	R/W
242	*VCO Bias 1*	Open	Must be zeros		VCO Bias Tcf<1:0>		VCO Bias Ref<2:0>			04h	R/W
243	*VCO Bias 2*	VCO Bypass Bias DAC R	Open		VCO Comp Bypass Bias R	Bypass Prescale R	Last ALC Enable	Prescale Bias <1:0>		0Dh	R/W
244	*Cal Status*	CP Cal Valid	Comp Out	CP Cal Done	VCO Cal Busy	CP Cal Word<3:0>				--H	R
245	*VCO Cal Ref*	Open				VCO Cal Ref Monitor	VCO Cal Ref Tcf<2:0>			00h	R/W
246	*VCO Pd Overrides*	Open				Power Down Varactor Ref	Pwr Down Varact Ref Tcf	Power Down Cal Tcf	Power Down VCO Bufffer	00h	R/W
247	*CP Over Range/VCO Lock*	CP Ovrg High	CP Ovrg Low	Open				Lock	Open	--H	R
248	*VCO LDO*	VCO LDO Bypass	VCO LDO Inrush<1:0>		VCO LDO Sel<2:0>			VCO LDO Vdrop Sel<1:0>		07h	R/W
249	*VCO Cal*	VCO Cal En	VCO Cal ALC Wait <2:0>			VCO Cal Count <1:0>		FB clock adv <1:0>		02h	R/W
24A	*Lock Detect Config*	Open				Lock Detect Count<1:0>		Lock Detect Mode<1:0>		02h	R/W
24B	*CP Level Detect*	Open	CP Level Detect Power Down	CP Level Threshold Low<2:0>		CP Level Threshold High<2:0>				17h	R/W
24C	*DSM Setup 0*	Open				DSM Prog<3:0>				00h	R/W
24D	*DSM Setup 1*	Open	SIF clock	SIF Reset Bar	SIF Addr<4:0>					00h	R/W
24E	*Correction Word0*	Update Freq Word	Open	Read Effective Tuning Word	Frequency Correction Word<11:7>					00h	R/W
24F	*Correction Word1*	Update Freq Word	Frequency Correction Word<6:0>							00h	R/W
250	*VCO Varactor Control 0*	Open	VCO Varactor Reference Tcf<2:0>			VCO Varactor Offset<3:0>				63h	R/W
251	*VCO Varactor*	Open				VCO Varactor Reference<3:0>				08h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
	Control 1										

SPI Register 0x230— PFD Config

[D0] Bypass Ld Ssynth Set this bit to prevent a VCO cal when the integer frequency word changes or if the ENSM is in TDD mode and moves from the Tx state to the Alert state. (This bit in 0x270 prevents a VCO cal when the ENSM moves from the Rx state to the Alert state).

SPI Registers 0x231— Frequency Integer Byte0

This byte is the lower 8 bits of the Rx synthesizer integer word. The local oscillator (LO) frequency equals the RF VCO divided down by a power-of-two divider. Rearranged, it appears as shown as Equation 44 below.

$$F_{RFVCO} = LO * 2^{(Rx\ VCO\ Divider + 1)}$$

Equation 44

Where

F_{RVCOL} units are the same as those used for the LO

The "Rx VCO Divider" is programmed in register 0x005[D3:D0].

The RF VCO can run at frequencies between 6GHz and 12GHz so the divider reduces the carrier to the desired frequency.

$$F_{RFVCO} = F_{REF} * \left(N_{Integer} + \frac{N_{Fractional}}{8{,}388{,}593}\right)$$

Equation 45

Where

F_{REF} = Reference Clock Frequency (external or DCXO). This rate is ***after*** the reference divider in 0x2AB[D0] and 0x2AC[D7].

$N_{Integer}$ = 11-bit Integer word programmed in registers 0x231 and 0x232

$N_{Fractional}$ = 23-bit Fractional word programmed in registers 0x233 through 0x235

Equation 46 and Equation 47 derive the integer and fractional words. All frequencies must use the same units (e.g. MHz).

$$N_{Integer} = Floor\left(\frac{F_{RFPLL}}{F_{REF}}\right)$$

Equation 46

$$N_{Fractional} = Round\left(8{,}388{,}593 * \left(\frac{F_{RFPLL}}{F_{REF}} - N_{Integer}\right)\right)$$

Equation 47

Where

F_{REF} = Reference Clock Frequency (external or DCXO). This rate is ***after*** the reference divider in 0x2AB[D0] and 0x2AC[D7].

$N_{Integer}$ = 11-bit Integer word programmed in registers 0x231 and 0x232

$N_{Fractional}$ = 23-bit Fractional word programmed in registers 0x233 through 0x235

Table 65 shows a typical process for determining the integer and fractional word, along with an example.

External Reference Frequency (F_{REF}) = 30.72MHz; 0x2AB[D0] and 0x2AC[D7] = 0 (reference is buffered only)		
Step #	**Description**	**Example**
1	Given desired LO frequency	902.2MHz
2	Determine "Rx VCO Divider"	902.2MHz * 2^3 = 7217.6MHz

External Reference Frequency (F_{REF}) = 30.72MHz; 0x2AB[D0] and 0x2AC[D7] = 0 (reference is buffered only)		
Step #	**Description**	**Example**
		7217.6 MHz is between 6GHz and 12GHZ so the divider register= 2 (0x005[D3:D0] = 3'b010)
3	Determine Integer Word	$N_{Integer} = Floor\left(\frac{7217.6MHz}{30.72MHz}\right) = 234(d) = 0x0EA$ 0x231[D7:D0] = 0xEA 0x232[D2:D0] = 3'b000
4	Determine Fractional Word	$N_{Frac} = Round\left(8{,}388{,}593 * \left(\frac{7217.6MHz}{30.72MHz} - 234\right)\right)$ =7,951,687(d) = 0x795547 0x233[D7:D0] = 0x47 0x234[D7:D0] = 0x55 0x235[D6:D0] = 0x79

Table 65. Programming Rx Synthesizer Frequency Words

SPI Register 0x232—Integer Byte 1

[D2:D0] Frequency Integer Word<10:8> The upper 3 bits of the synthesizer frequency word. See 0x231.

SPI Registers 0x233 through 0x235—Fractional bytes 0, 1, 2

These registers are the fractional synthesizer bytes that make up the fractional word. See registers 0x231.

SPI Register 0x238—Force VCO Tune 1

[D6:D3] VCO Cal Offset<3:0> These bits set the VCO Cal voltage. 15mV/LSB. Normally zeros. For reference, see Equation 48, Equation 49 and Table 66.

$$V_{Cal}(T) = V_{DD} - V_{GS}(T) - 15mV * VCO\ Cal\ Offset<3:0> + V_{Temp}(T) * (1 - 2 * Power\ Down\ Varactor\ Ref)$$

Equation 48

Where

$$V_{Temp}(T) = 94mV * \left(1 - 2499ppm * \left(1 + \frac{VCO\ Cal\ Ref\ Tcf<2:0>}{3}\right) * (T - 27°C) * (1 - Power\ Down\ Cal\ Tcf)\right)$$

Equation 49

$V_{GS}(T)$ = 334mv, 263mv, 178mv At -40, 27, 110°C respectively

VCO Cal Offset<3:0>is set by D6:D3 of 0x238 (normally set to zero)

Power Down Varactor Ref is set by D3 of 0x246

VCO Cal Ref Tcf<2:0> is set by D2:D0 of 0x245 (normally cleared) and equals -833ppm/LSB with a range of -2500ppm to -8333ppm.

Power Down Cal Tcf is set by D1 of 0x246 (normally cleared)

		VCO Cal Voltage (numbers in mV)		
Rxsynth Vco Cal Ref Tcf<2:0>	**Rxsyn Pd Var Ref**	**-40°C**	**27°C**	**110°C**
000	0	Vdd-228	Vdd-172	Vdd-103
111	0	Vdd-191	Vdd-172	Vdd-149
000	1	Vdd-447	Vdd-360	Vdd-252
111	1	Vdd-484	Vdd-360	Vdd-207

Table 66. Example of VCO Calibration Voltages and Configuration Words

SPI Register 0x239—ALC/Varactor

[D7:D4] Init ALC Value<3:0> These bits set the Initial ALC value (VCO bias DAC setting) when running a VCO calibration. The actual DAC word equals these 4 bits multiplied by 8 (shifted three positions to the left).

[D3:D0] VCO Varactor<3:0> These bits set the varactor size which sets the Kv. Higher register value equals higher Kv. The total varactor value (0x239[D3:D0] + 0x251[D3:D0]) must be 15(d) or less. See 0x251 for other restrictions on the setting of these bits.

SPI Register 0x23A—VCO Output

[D6] PORb VCO Logic clearing this bit resets the VCO calibration logic. Clear and then set this bit before the VCO calibrates.

[D3:D0] VCO Output Level<3:0> These bits set the VCO output voltage level which sets the VCO phase noise performance and power consumption. Range: 0.5V to 1.5V, step size = 67mV. Normally set to 0xA.

SPI Register 0x23B—CP Current

[D5:D0] Charge Pump Current<5:0>. These bits set the charge pump current. Range: 0.1mA to 6.4mA, resolution = 100uA/LSB.

SPI Register 0x23C—CP Offset

[D7] Synth Re-Cal Setting this self-clearing bit forces the charge pump to re-calibrate either the next time the synthesizer powers up or when "CP Cal Enable" (0x23D[D2]) is cleared and then set. Clear for normal operation.

SPI Register 0x23D—CP Config

[D7] Half VCO Cal Clk Affects VCO cal time but only halves the clock for the ALC portion of the calibration. VCO Cal count in 0x249 has the largest effect on cal time.

[D3] Force CP Cal Setting this bit overrides the calibration result. In normal operation, this bit goes high after the charge pump calibration completes. Clear for normal operation.

[D2] CP Cal Enable Set this bit to force a charge pump calibration the first time the synthesizer powers up. When the calibration completes, the "CP Cal Valid" and "CP Cal Done" ([D7] and [D5] of 0x244) go high. The charge pump calibration will not restart unless "CP Cal Valid" goes low. If the "CP Cal Enable" bit is clear, the charge pump will not calibrate.

SPI Register 0x23E—Loop Filter 1

[D7:D4] Loop Filter C2<3:0> These bits set the 2nd pole loop filter capacitor per Equation 50. 1.93pF/LSB at 27°C.

$$C2(pF) = 1.93pF * (Loop\ Filter\ C2 < 3:0 > + \overline{Loop\ Filter\ Bypass\ C2\ LSB})$$

Equation 50

Where

$\overline{Loop\ Filter\ Bypass\ C2\ LSB}$ is set by 0x240[D5]. Setting this bit shorts out an *additional* LSB of C2.

[D3:D0] Loop Filter C1<3:0> These bits set the capacitor for the loop filter zero per Equation 51. 114.4pF/LSB at 27°C.

$$C1(pF) = 114.4pF * (Loop\ Filter\ C1 < 3:0 > + \overline{Loop\ Filter\ Bypass\ C1\ LSB})$$

Equation 51

Where

$\overline{Loop\ Filter\ Bypass\ C1\ LSB}$ is set by 0x240[D4]. Setting this bit shorts out an *additional* LSB of C1.

SPI Register 0x23F—Loop Filter 2

[D7:D4] Loop Filter R1<3:0> These bits set the resistor value for the loop filter zero. There are 16 resistors in parallel. Range: 8.68kΩ to 543Ω (all R's in parallel with the bits set to zero). Setting the "Loop Filter Bypass R1" (0x240[D6]) bit shorts R1. See Equation 52.

$$R1 = \frac{8.68k\Omega}{\overline{Loop\ Filter\ R1 < 3:0 >} + 1} * \overline{Loop\ Filter\ Bypass\ R1}$$

Equation 52

Where $Loop\ Filter\ Bypass\ R1$ is set by 0x240[D6].

[D3:D0] Loop Filter C3<3:0> These bits set the 3rd pole loop filter capacitor. Range: 2.86pF to 47.4pF; resolution: 2.86pF at 27°C. See Equation 53.

$$C3 = 2.86pF * (1 + Loop\ Filter\ C3 < 3:0 >)$$

Equation 53

SPI Register 0x240—Loop Filter 3

[D7] Loop Filter Bypass R3 Setting this bit bypasses R3 of the loop filter. See bits [D3:D0].

[D6] Loop Filter Bypass R1 Setting this bit bypasses R1 of the loop filter. See 0x23F[D7:D4].

[D5] Loop Filter Bypass C2 See 0x23E[D7:D4]. Setting this bit shorts out an *additional* LSB of C2.

[D4] Loop Filter Bypass C1 See 0x23E[D3:D0]. Setting this bit shorts out an *additional* LSB of C1.

[D3:D0] Loop Filter R3<3:0> These bits set the 3rd pole loop filter resistor. There are 16 resistors in parallel. Range: 2.79kΩ to 174Ω (all resistors in parallel with all bits set to zero). Setting the "Loop Filter Bypass R3" (0x240[D7]) bit shorts R3. See Equation 54

$$R3 = \frac{2.79k\Omega}{\overline{Loop\ Filter\ R3 < 3:0 >} + 1} * \overline{Loop\ Filter\ Bypass\ R3}$$

Equation 54

Where $\overline{Loop\ Filter\ Bypass\ R3}$ is set by 0x240[D7].

SPI Register 0x241—Dither/CP Cal

[D3:D0] Forced CP Cal Word<3:0> Test bits only. Writing this nibble overwrites the CP calibration word.

SPI Register 0x242—VCO Bias 1

[D4:D3] VCO Bias Tcf<1:0> These bits control the VCO bias DAC temperature coefficient per Equation 55.

$$I_{DC}(T) = I_{DC}(27°C) * \left(1 + (990ppm + 700ppm * VCO\ BiasTdf < 1:0 >) * (T - 27°C)\right)$$

Equation 55

[D2:D0] VCO Bias Ref<2:0> These bits control the VCO bias reference DAC. Range: 50uA to 400uA; resolution: 50uA.

SPI Register 0x244—Cal Status—Read Only Test Register

[D7] CP Cal Valid This is a bit generated by the digital blocks and goes high after "CP Cal Done" (bit D5) goes high (indicating that a calibration completed). When a cal is successful, the results are pushed into the proper registers after the synthesizer has been powered down and is then powered back up. This bit clears (forcing a re-calibration when the synthesizer powers up) if:

"CP Cal Enable" (0x23D[D2] goes low
"Re-Cal" (0x23C[D6]) goes high
"Force CP Cal" (0x23D[D3]) goes low

[D5] CP Cal Done D5 is an analog status bit that indicates a successful charge pump calibration. In normal operation, monitor bit D7 as bits D5 and D7 have the same value. The only time they would be different is if a CP Cal completes (setting both bits), then the BBP powers down the synthesizer (D5 goes low) but the digital portion of the AD9361 does not change state (D7 stays high). Powering the synthesizer back up will use the old cal results since D7 is high.

[D4] VCO Cal Busy This bit set indicates that a VCO calibration is running.

[D3:D0] CP Cal Word<3:0> These bits are the charge pump calibration results. If the "Force CP Cal" (0x23D[D3]) bit is set, then these bits will be forced by the "Forced CP Cal Word" in 0x241[D3:D0]).

SPI Register 0x245—VCO Cal Ref

[D2:D0] VCO Cal Ref These bits set a portion of the VCO calibration voltage temperature coefficient. See equations for 0x238.

SPI Register 0x246—VCO Power Down Overrides—Test register only—Do not change these bits

[D3] Power Down Varactor Ref Setting this bit powers down the varactor reference voltage.

[D2] Power Down Varactor Ref Tcf Setting this bit powers down the varactor reference voltage temperature coefficient.

[D1] Power Down Cal Tcf Setting this bit powers down the VCO calibration reference voltage temperature coefficient.

[D0] Power Down VCO Buffer Setting this bit powers down the VCO buffer.

SPI Register 0x247—CP Over Range/VCO Lock—Read Only

[D7] CP Over Range High Applies if 0x24B[D6] is clear. If set, the CP output is above "CP Level Threshold High" (0x24B[D2:D0]).

[D6] CP Over Range Low Applies if 0x24B[D6] is clear. If set, the CP output is below "CP Level Threshold Low" (0x24B[D5:D3]).

[D1] Lock Applies if 0x24A[D1:D0] = 2'b01 or 2'b10. If set, the synth locked in the number of clock cycles set by "Lock Detect Count" (0x24A[D3:D2].

SPI Register 0x248—VCO LDO

[D7] VCO LDO Bypass Test bit. Setting this bit bypasses the VCO LDO. Normally cleared.

[D6:D5] VCO LDO Inrush<1:0> Limits the inrush current to the VCO LDO per Table 67 (assuming 1uF external cap).

VCO LDO Inrush<1:0>	Idd Inrush (mA)	Start-up Time (uS)
00	250	34
01	300	25
10	350	18
11	750	10

Table 67.VCO LDO Inrush current and startup time

[D4:D2] VCO LDO Sel<2:0> These bits select the LDO output voltage and noise. Table 68 shows the output voltage, noise, and Ibias vs setting when the band gap reference is selected (D6 of Reg. 2A8). When the bandgap reference is not selected, the output voltage determined by the following:

$$Vout = \frac{Vdd}{2} \cdot \left(1 + \frac{R1}{R2}\right)$$

Where Vdd is the voltage at the primary side of the LDO input and R1 and R2 are shown in Table 68.

VCO LDO Sel <2:0>	R1	R2	Vout [V]	Noise	Ibias
000	11.5*R	15.9*R	1.14	High	250µA
001	1.44*R	2*R	1.14	Med	2mA
010	1*R	1.64*R	1.14	Low	3mA
011	Not defined				
100	11.5*R	17.3*R	1.10	High	250µA
101	1.44*R	2.2*R	1.10	Med	2mA
110	1*R	1.5*R	1.10	Low	3mA
111	Not defined				

Table 68: VCO LDO output voltage and noise

[D1:D0] VCO LDO Vdrop Sel<1:0> Sets LDO dropout voltage. 00b=max dropout, 11b=min dropout voltage. Default=11

SPI Register 0x249—VCO Cal

[D7] VCO Cal En This bit enables the VCO Cal block. To reduce power consumption and spurious emissions, VCO Cal En should be low after the VCO calibration has completed.

[D6:D4] VCO ALC Wait <2:0> These bits are used to set how long to wait after the VCO ALC cal has been completed before starting the frequency cal. The minimum and maximum delay for 80MHz reference is 0.5 and 4µs in 0.5 µs steps. The minimum and maximum delay for 10MHz reference is 4 and 32µs in 4 µs steps.

$$VCO\ ALC\ Wait < 2:0 >= \frac{T_{delay} \cdot F_{ref}}{40} - 1$$

T_{delay} is desired wait time [sec]

F_{ref} is synthesizer reference clock [1/sec]

[D3:D2] VCO Cal Count<1:0> These bits set the VCO Frequency Cal Counter Length. 00=128, 01=256, 10=512,11=1024. See Table 69 for example VCO cal times.

Fref (MHz)	Load Synth Delay (0x024-0x025)	Hafl VCO Cal Clk (0x23D[D7])	VCO ALC Wait (0x249[D6:D4])	Init ALC Value (0x239[D7:D4])	VCO Cal Count (0x249[D3:D2])	Frequency Cal Clock Cycles	ALC Cal Clock Cycles	Avg Cal Time (us)	Use
19.2	2	0	000	0xC	00	128	12	87.7	TDD
30.72	2	0	000	0xC	00	128	12	55.6	TDD
40	2	0	000	0xC	00	128	12	43.2	TDD
61.44	2	0	000	0xC	01	256	12	47.5	TDD
80	2	0	000	0xC	01	256	12	37.0	TDD
19.2	2	0	000	0xC	11	1024	12	507.7	FDD
30.72	2	0	000	0xC	11	1024	12	318.1	FDD
40	2	0	000	0xC	11	1024	12	244.8	FDD
61.44	2	0	000	0xC	11	1024	12	160.0	FDD
80	2	0	000	0xC	11	1024	12	123.4	FDD

Table 69. Example Calibration Times for RF VCO Cal

Where Fref is reference clock input to the RFPLL after the scaling set by 0x2AB and 0x2AC (only 0x2AC for the Tx RFPLL)

SPI Register 0x24A—Lock Detect Config

[D3:D2] Lock Detect Count<1:0> These bits set the maximum time allowed for the RFPLL to lock. If it locks within the specified time, the "Lock" bit (0x247[D1]) goes high. The time is measured in reference clock cycles per Table 70.

Lock Detect Count<1:0>	Reference Clock Cycles
0 0	256
0 1	512
1 0	1024
1 1	2048

Table 70.Lock Detect Count

[D1:D0] Lock Detect Mode<1:0> These bits set the lock detect mode of operation per Table 71.

Lock Detect Mode<1:0>	RFPLL Lock Detect Mode
0 0	Disable Lock Detect
0 1	Run Lock Detect Once, when RFPLL is enabled
1 0	Run Lock Detect Continuously
1 1	Do not use

Table 71. RFPLL Lock Detect Mode

SPI Register 0x24B—CP Level Detect

[D6] CP Level Detect Power Down Setting this bit high disables the CP comparator. If clear, the AD9361 compares the CP voltage to the threshold in bits D5:D0. If the voltage exceeds one of these thresholds, the AD9361 sets the "CP Over Range" bits in 0x247.

[D5:D3] CP Level Threshold Low<2:0> These bits set the low threshold for the CP level detector. Range: 150mV-Vss to 500mV – Vss; resolution: -50mV/LSB. All zeros = 500mV – Vss.

[D2:D0] CP Level Threshold High<2:0> These bits set the low threshold for the CP level detector. Range: Vdd-150mV to Vdd-500mV; resolution: -50mV/LSB. All zeros = VDD – 150mV.

SPI Register 0x24C—DSM Setup 0—Test bits only—do not access these bits

The SDM Serial Interface (SIF) uses an internal register map used to program the SDM seed and modulus values. These are SIF data bits.

SPI Register 0x24D—DSM Setup 1

[D6] SIF Clk Do not change this bit. Used by the SIF to clock in/out seed and modulus values.

[D5] SIF Reset Bar Do not change this bit. Setting this bit runs the SIF logic (only used if reading or writing SDM seed/modulus values).

[D4:D0] SIF Addr<4:0> Do not change these bits. This is the address for the internal SDM register map.

SPI Register 0x24E—Correction Word 0

[D7] Update Freq Word When this self-clearing bit is set, the synthesizer word updates with the values in bits D4:D0 and 0x24F[D6:D0]. The bit is ORed with bit D7 in 0x24F.

[D5] Read Effective Tuning Word When this bit is set, the integer and fractional words in registers 0x231 through 0x235 reflect the addition of the correction words to the frequency (see bits D4:D0).

[D4:D0] Frequency Correction Word<11:7> The most significant 5 bits of a 12-bit frequency correction word. 2's complement using the same mapping as shown in the Equation 44 through Equation 47. Internal in the AD9361, this word adds to the fractional word in registers 0x233 through 0x235. If the fractional word overflows, the integer word in registers 0x231 and 0x232 also updates but the VCO calibration does not occur. Used for minor frequency corrections.

SPI Register 0x24F—Correction Word 1

[D7] Update Freq Word Wire Ored with D7 of 0x24E.

[D6:D0] Frequency Correction Word<6:0> the least significant bits of the correction word. See 0x24E[D4:D0].

SPI Register 0x250—VCO Varactor Control 0

[D6:D4] VCO Varactor Reference Tcf<2:0> This is a temperature compensating voltage used to keep the RFPLL locked over temperature while maintaining a low Kv. The varactor reference voltage attaches to the tune port of varactors (see 0x251[D3:D0]) that are not connected to the loop filter output. For reference, Equation 56 describes the varactor reference voltage. See also Table 73

$$V_{Var-ref}\ (T) = V_{DD} - V_{scale} - V_{Temp}(T)$$

Equation 56

Where

VCO Varactor Offset <3:0>	Vscale @27°C [mV]
0000	289
1000	315
1100	335
1110	382
1111	Not defined

Table 72. VCO Varactor Offset vs. Vscale for Equation 60

$$V_{Temp}(T) = 284mV * \left(1 - 2400ppm * \left(1 + \frac{VCO\ Varactor\ Reference\ Tcf < 2:0 >}{3}\right) * (T - 27°C) * (1 - Power\ Down\ Varactor\ Ref\ Tcf)\right)$$

Equation 57

$Power\ Down\ Varactor\ Ref\ Tcf$ is given by D2 of 0x246.

$VCO\ Varactor\ Offset < 3:0 >$ is given by 0x250[D3:D0]. Resolution: 15mV/LSB.

$VCO\ Varactor\ Reference\ Tcf < 2:0 >$ is given by 0x250[D6:D4]. Range: -2400ppm to -8000ppm; resolution = -800ppm/LSB.

			VCO Var Ref (numbers in mV)		
VCO Varactor Offset<3:0>	**VCO Varactor Reference Tcf<2:0>**	**Power Down Varactor Ref Tcf**	**-40°C**	**27°C**	**110°C**
0000	111	0	Vdd-797	Vdd-576	Vdd-297

Table 73.VCO Varactor Compensation

[D3:D0] VCO Varactor Offset<3:0> See bits D6:D4. Resolution: 15mV/LSB.

SPI Register 0x251—VCO Varactor Control 1

These bits set the number of varactors connected to the VCO varactor reference voltage. The varactor consists of 4 binary weighted sections. See Table 74 for example valid settings. It is never valid to set the same bit in both words (0x239[D3:D0] and 0x251[D3:D0] as that would connect the loop filter (controlled by 0x239) to the same varactor that the varactor reference voltage is connected to Further, 0x251[D3:D0] + 0x239[D3:D0] must always be less than 15(d).

VCO Varactor<3:0> (0x239[D3:D0])	VCO Varactor Reference<3:0> (0x251[D3:D0]	Varactor Tune Port Connections
0000	0000	<3:0> connected to Vdd
0001	0000	<3:1> connected to Vdd, <0> connected to loop filter output
0010	0001	<3:2> connected to Vdd <1> connected to loop filter output <0> connected to varactor reference volt

Table 74.VCO Varactor Connections

RX FAST LOCK REGISTERS 25A THROUGH 25F

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
25A	*Rx Fast Lock Setup*	Rx Fast Lock Profile<2:0>			Open	Rx Fast Lock Load Synth	Rx Fast Lock Profile Init	Rx Fast Lock Profile Pin Select	Rx Fast Lock Mode Enable	00h	R/W
25B	*Rx Fast Lock Setup Init Delay*	Rx Fast Lock Init Delay<7:0>								00h	R/W
25C	*Rx Fast Lock Program Addr*	Rx Fast Lock Program Address<7:0>								--H	R/W
25D	*Rx Fast Lock Program Data*	Rx Fast Lock Program Data<7:0>								--H	R/W
25E	*Rx Fast Lock Program Read*	Rx Fast Lock Program Read Data<7:0>								--H	R
25F	*Rx Fast Lock Program Control*	Open						Rx Fast Lock Program Write	Rx Fast Lock Program Clock Enable	00h	R/W

"Fast Lock" offers two benefits. First, VCO cal results for up to 8 different LO frequencies can be determined during initialization and stored in the AD9361. During operation, if the LO frequency changes, the VCO can recall the calibration results for the desired profile,

eliminating the need for a VCO calibration. The VCO must still lock but this duration is much shorter than the cal duration. Second, the lock time itself can be decreased by using a wide initial loop BW for fast convergence and then a narrow loop BW for best phase noise.

SPI Register 0x25A—Rx Fast Lock Setup

[D7:D5] Rx Fast Lock Profile<2:0> Ignored if bit D1 is set. These bits select the profile number (0-7) when creating or using a profile.

[D3] Rx Fast Lock Load Synth Setting this bit forces a VCO calibration. After calibration completes, the AD9361 saves the resulting calibration words and then this bit self-clears. Only valid when D0 and D2 are set. If the VCO Tune and VCO Alc words (see Program Address<3:0> entries 0xE and 0xF in Table 75) are written manually into the profile along with the other parameters, then it is not necessary to set this bit and run a VCO calibration. If these entries are not programmed as part of the profile, this bit must be set after writing all other parameters into the profile so the AD9361 can determine the VCO Tune and ALC values and add them to the profile.

[D2] Rx Fast Lock Profile Init Set this bit when creating a profile. This bit set allows the calibrated VCO values to be saved to a specific profile. To create more than one profile, this bit must be set low and then high again. Only valid when bit D0 is set. Clear this bit to use saved profiles (after all fast lock programming completes).

[D1] Rx Fast Lock Profile Pin Select With this bit set, the CTRL_IN0 through CTRL_IN2 pins select the Rx fast lock profile. With this bit clear, the "Rx Fast Lock Profile" value in bits D7:D5 select the fast lock profile. Only valid when D0 is set.

[D0] Rx Fast Lock Mode Enable Set this bit when creating profiles or in normal operation when using profiles.

SPI Register 0x25B—Rx Fast Lock Setup Init Delay

These bits set the time that the charge pump current, R1, R3, and C3 of the loop filter remain at their initial values before changing to final values during fast lock. 250ns/LSB, range of 0ns to 63.75us. All profiles share this delay setting. Allows for a faster lock time by initially increasing the loop BW (for the time equal to this register) and then reducing the loop BW for better phase noise performance.

SPI Register 0x25C—Rx Fast Lock Program Address

These bits set the profile calibration word addresses per Table 75. To write all setup words for a particular profile into the table, hold the upper nibble constant and write the lower nibble 13 or 15 times (x0 to xD or xF), changing the data written to register 0x25D for each write operation. See 0x25A[D3] for the difference between using 13 table entries vs. 15 entries.

Program Address<7:4>	Assignment	Program Address<3:0>	Assignment (written to 0x25D) (see 0x25D for details of this column)	Location of Setup Words
0	profile0	0	Synthesizer Integer Word<7:0>	0x231[D7:D0]
1	profile1	1	Synthesizer Integer Word<10:8>	0x232[D2:D0]
2	profile2	2	Synthesizer Fractional Word<7:0>	0x233[D7:D0]
3	profile3	3	Synthesizer Fractional Word <15:8>	0x234[D7:D0]
4	profile4	4	Synthesizer Fractional Word <22:16>	0x235[D6:D0]
5	profile5	5	VCO Bias Ref<2:0> shift left by 4 + VCO Varactor <3:0>	0x242[D2:D0] 0x239[D3:D0]
6	profile6	6	VCO Bias Tcf<1:0> shift left by 3 + Charge Pump Current (Init)<5:0>	0x242[D4:D3] See PLL User Guide
7	profile7	7	Charge Pump Current<5:0>	0x23B[D5:D0]
8	Not Used	8	Loop Filter R3<3:0> shift left by 4 + Loop Filter R3 (Init)<3:0>	0x240[D3:D0] See PLL User Guide
9	Not Used	9	Loop Filter C3<3:0> shift left by 4 + Loop Filter C3 (Init)<3:0>	0x23F[D3:D0] See PLL User Guide
A	Not Used	A	Loop Filter C1<3:0> shift left by 4 + Loop Filter C2<3:0> shift right by 4	0x23E[D3:D0] 0x23E[D7:D4]

Program Address<7:4>	Assignment	Program Address<3:0>	Assignment (written to 0x25D) (see 0x25D for details of this column)	Location of Setup Words
B	Not Used	B	Loop Filter R1<3:0> + Loop Filter R1 (Init)<3:0>	0x23F[D7:D4] See PLL User Guide
C	Not Used	C	VCO Varactor Reference Tcf<2:0> + Rx VCO Divider<3:0>	0x250[D6:D4] 0x005[D3:D0]
D	Not Used	D	VCO Cal Offset<3:0> shift left by 1 + VCO Varactor Reference<3:0>	0x238[D6:D3] 0x251[D3:D0]
E	Not Used	E	Force VCO Tune<7:0>	0x237[D7:D0]
F	Not Used	F	Force ALC word<6:0> shift left by 1 + Force VCO Tune<8>	0x236[D6:D0] 0x238[D0]

Table 75.Rx Fast Lock Profile Table

SPI Register 0x25D—Rx Fast Lock Program Data

When creating a profile, the words written into this register set the calibration setup parameters. See the table under register 0x25C. Also see the table above. When bits are extracted from the "Location of Setup Words" column shown in the table above, the bits may not be in the correct location when they are programmed into register 0x25D. For example, for Program Address <3:0> = 0x6, 0x242[D4:D3] are needed but those bits need to be shifted so that they are in the correct location and also added to an initial CP current value. CP current is a 6-bit value so 0x242[D4:D3] need to be shifted such that these bits are placed into bits D7:D6 in 0x25D. If 0x242[D4:D3] are extracted by ANDing register 0x242 with the value 8'b00011000, all bits except the desired bits are zeros and the location of the desired bits is unchanged. Shifting the bits by 3 moves them to locations D7:D6. D5:D0 would then be filled by the 6-bit initial CP current value.

SPI Register 0x25E—Rx Fast Lock Program Read Data

If desired, the words programmed into a specific profile can be read from this register.

SPI Register 0x25F—Rx Fast Lock Program Control

[D1] Rx Fast Lock Program Write Set this self-clearing bit any time a write operation to the Fast Lock Table is performed. Also set D0.

[D0] Rx Fast Lock Program Clock Enable Set to 1 to read data from or write data to a profile.

RX LO GENERATION REGISTER 261

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
261	*Rx LO Gen Power Mode*	Open		Power Mode<1:0>		Open				00h	R/W

SPI Register 0x261—Rx LO Gen Power Mode

These bits control the bias current of the 1st VCO divider, driven by the internal VCO output and thermometer coded per Table 76.

Power Mode<1:0>	Bias Current (mA)	Relative Speed and Phase Noise
00	5	Best (recommended)
01	N/A	Not Used
11	0 (Powered Down)	N/A

Table 76. Rx LO Generator Bias Current

TX SYNTHESIZER REGISTERS 270 THROUGH 291

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
270	*PFD Config*	Open		Div Test En	Open	PFD Width <1:0>		PFD Clk Edge	Bypass Ld Synth	54h	R/W
271	*Integer Byte 0*	Synthesizer Integer Word<7:0>								00h	R/W
272	*Integer Byte 1*	SDM Bypass	SDM Power Down	Open			Synthesizer Integer Word<10:8>			00h	R/W
273	*Fractional Byte 0*	Synthesizer Fractional Word<7:0>								00h	R/W
274	*Fractional Byte 1*	Synthesizer Fractional Word <15:8>								00h	R/W
275	*Fractional Byte 2*	Open	Synthesizer Fractional Word <22:16>							00h	R/W
276	*Force ALC*	Force ALC Enable	Force ALC Word<6:0>							00h	R/W
277	*Force VCO Tune 0*	Force VCO Tune<7:0>								00h	R/W
278	*Force VCO Tune 1*	Bypass Load Delay	VCO Cal Offset<3:0>				Open	Force VCO Tune Enable	Force VCO Tune<8>	00h	R/W
279	*ALC/Varactor*	Init ALC Value<3:0>				VCO Varactor<3:0>				82h	R/W
27A	*VCO Output*	Open	PORb VCO Logic	Open		VCO Output Level<3:0>				0Ah	R/W
27B	*CP Current*	Set to 1	Vtune Force	Charge Pump Current<5:0>						00h	R/W
27C	*CP Offset*	Synth Re-Cal	Open	Charge Pump Offset<5:0>						00h	R/W
27D	*CP Config*	Half Vco Cal Clk	Dither Mode	Open	Cp Offset Off	F Cpcal	Cp Cal Enable	Cp Test <1:0>		80h	R/W
27E	*Loop Filter 1*	Loop Filter C2<3:0>				Loop Filter C1<3:0>				00h	R/W
27F	*Loop Filter 2*	Loop Filter R1<3:0>				Loop Filter C3<3:0>				00h	R/W
280	*Loop Filter 3*	Loop Filter Bypass R3	Loop Filter Bypass R1	Loop Filter Bypass C2	Loop Filter Bypass C1	Loop Filter R3<3:0>				00h	R/W
281	*Dither/CP Cal*	Number SDM Dither Bits<3:0>				Forced CP Cal Word<3:0>				00h	R/W
282	*VCO Bias 1*	Open	Must be zeros		VCO Bias Tcf<1:0>		VCO Bias Ref<2:0>			04h	R/W
283	*VCO Bias 2*	VCO Bypass Bias DAC R	Open		VCO Comp Bypass Bias R	Bypass Prescale R	Last ALC Enable	Prescale Bias <1:0>		0Dh	R/W
284	*Cal Status*	CP Cal Valid	Comp Out	CP Cal Done	VCO Cal Busy	CP Cal Word<3:0>				--h	R
285	*VCO Cal Ref*	Open				VCO Cal Ref Monitor	VCO Cal Ref Tcf<2:0>			00h	R/W

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
286	VCO Pd Overrides	Open				Power Down Varactor Ref	Power Down Varact Ref Tcf	Power Down Cal Tcf	Power Down VCO Bufffer	00h	R/W
287	CP Over Range/VCO Lock	CP Ovrg High	CP Ovrg Low	Open				Lock	Open	--H	R
288	VCO LDO	VCO LDO Bypass	VCO LDO Inrush<1:0>		VCO LDO Vout Sel<2:0>			VCO LDO Vdrop Sel<1:0>		07h	R/W
289	VCO Cal	VCO Cal En	VCO Cal ALC Wait<2:0)			VCO Cal Count<1:0>		FB Clock Adv<1:0>		02h	R/W
28A	Lock Detect Config	Open				Lock Detect Count<1:0>		Lock Detect Mode<1:0>		02h	R/W
28B	CP Level Detect	Open	CP Level Detect Power Down	CP Level Detect Threshold Low<2:0>			CP Level Detect Threshold High<2:0>			40h	R/W
28C	DSM Setup 0	Open				DSM Prog<3:0>				00h	R/W
28D	DSM Setup 1	Open	SIF clock	SIF Reset Bar	SIF Addr<4:0>					80h	R/W
28E	Correction Word0	Update Freq Word	Open	Read Effective Tuning Word	Frequency Correction Word<11:7>					00h	R/W
28F	Correction Word1	Update Freq Word	Frequency Correction Word<6:0>							00h	R/W
290	VCO Varactor Control 0	Open	VCO Varactor Reference Tcf<2:0>			VCO Varactor Offset<3:0>				63h	R/W
291	VCO Varactor Control 1	Open				VCO Varactor Reference<3:0>				08h	R/W

These Tx registers are identical to the Rx registers in 0x230-0x251. See those registers for definitions. The description in register 0x231 refers to the reference divider if an external clock is used. For Tx frequency words in 0x271-0x275, reference divider is in 0x2AC[D3:D2].

DCXO REGISTERS 292 THROUGH 299

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
292	DCXO Coarse Tune	Open			DCXO Tune Coarse<5:0>					00h	R/W
293	DCXO Fine Tune2	DCXO Tune Fine<12:5>								00h	R/W
294	DCXO Fine Tune1	DCXO Tune Fine<4:0>				Open				00h	R/W
295	DCXO Config	Must be zero	DCXO Rtail<2:0>			DCXO Rd<1:0>		Open		14h	R/W
296	DCXO Tempco Write	DCXO Temperature Coefficient Write <7:0>								00h	R/W
297	DCXO Tempco Read	DCXO Temperature Coefficient Read <7:0>								--h	R
298	DCXO Tempco	DCXO	DCXO	DCXO Temperature Coefficient Address<5:0>						00h	R/W

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
	Addr	Tempco En	Tempco Clk								
299	Delta T Read	Delta T Read Back<7:0>									R

SPI Registers 0x292 through 0x294—DCXO Coarse Tune and DCXO Fine Tune

Only valid when the DCXO is used and bit D4 of 0x009 ("XO Bypass") is cleared. The DCXO is trimmed by adjusting capacitance in the AD9361. Equation 58 shows the dependence of the capacitance on the coarse and fine words.

$$Capacitance = 200fF * DCXO\ Tune\ Coarse < 5:0 > + 0.5fF * DCXO\ Tune\ Fine < 12:0 >$$

Equation 58

SPI Register 0x295—DCXO Config

[D6:D4] DCXO R Tail<2:0> Control word for R_{TAIL} of the DCXO maintaining amplifier, mapped per Table 77. Set to 0x001.

DCXO R Tail<1:0>	R Tail(Ohms)
000	316
001	158 (nominal)
010	236
011	78
100	236
101	78
110	158
111	0

Table 77. DCXO R Tail

[D3:D2] DCXO Rd<1:0> Control word for R_D o f DCXO maintaining amplifier, mapped per Table 78. Set to 0x01.

DCXO R_D<1:0>	R_D (Ohms)
00	711
01	1.4k
10	2.1k
11	2.8k

Table 78.DCXO RD

SPI Register 0x296—DCXO Tempco Write

When changing the DCXO temperature correction lookup table, write the data word in this register. This word will be written to the address in 0x298. See 0x298[D7] for details on DCXO temperature compensation.

SPI Register 0x297—DCXO Tempco Read

The temperature coefficient data at the address specified in 0x298 is read from this register. See 0x298[D7] for details on DCXO temperature compensation.

SPI Register 0x298—DCXO Tempco Addr

[D7] Tempco En Set this bit to enable DCXO temperature compensation after programming the lookup table. This feature allows the AD9361 to automatically correct the DCXO fine word to compensate for temperature drift. A one-time system-level sweep of DCXO frequency vs. temperature would have already been completed and a matrix of results stored during initialization into the lookup table accessed by registers 0x296 through 0x299. **Important Note:** Temperature compensation accuracy is limited and this limitation is multiplied up by the synthesizer. For this reason, temperature compensation is not recommended for LO frequencies > 1GHz. For lower LO frequencies, the required accuracy should be weighed against the accuracy of the algorithm.

[D6] Tempco Clk This bit is used only when writing to the temperature coefficient table. The data in address 0x296 is written to the internal address specified in 0x298 on the rising edge of this "clock". Not self-clearing. See also bit D7.

[D5:D0] DCXO Temperature Coefficient Address

Set the address of the temperature correction table entry in this register to read from or write to the lookup table. See also 0x298[D7].

SPI Register 0x299—Delta T Read

This register holds the delta temperature used for DCXO correction (if enabled by 0x298[D7]). See also 0x298[D7].

TX SYNTH FAST LOCK REGISTERS 29A THROUGH 29F

Register Address	*Name*	D7 D6 D5	D4	D3	D2	D1	D0	Default	R/W
29A	*Tx Fast Lock Setup*	Tx Fast Lock Profile<2:0>	Open	Tx Fast Lock Load Synth	Tx Fast Lock Profile Init	Tx Fast Lock Profile Pin Select	Tx Fast Lock Mode Enable	00h	R/W
29B	*Tx Fast Lock Setup Init Delay*	Tx Fast Lock Init Delay<7:0>						00h	R/W
29C	*Tx Fast Lock Program Addr*	Tx Fast Lock Program Address<7:0>						--h	R/W
29D	*Tx Fast Lock Program Data*	Tx Fast Lock Program Data<7:0>						--h	R/W
29E	*Tx Fast Lock Program Read*	Tx Fast Lock Program Read Data<7:0>						--h	R
29F	*Tx Fast Lock Program Ctrl*	Open				Tx Fast Lock Program Write	Tx Fast Lock Program Clock Enable	00h	R/W

These registers are identical to the Rx Fast Lock registers 25A-25F but apply to the Tx profiles. See 0x25A-0x25F. See Table 79 for the Fast Lock profile table (referencing Tx registers).

Program Address<7:4>	Assignment	Program Address<3:0>	Assignment (written to 0x29D) (see 0x29D for details of this column)	Location of Setup Words
0	profile0	0	Synthesizer Integer Word<7:0>	0x271[D7:D0]
1	profile1	1	Synthesizer Integer Word<10:8>	0x272[D2:D0]
2	profile2	2	Synthesizer Fractional Word<7:0>	0x273[D7:D0]
3	profile3	3	Synthesizer Fractional Word <15:8>	0x274[D7:D0]
4	profile4	4	Synthesizer Fractional Word <22:16>	0x275[D6:D0]
5	profile5	5	VCO Bias Ref<2:0> shift left by 4 + VCO Varactor <3:0>	0x282[D2:D0] 0x279[D3:D0]
6	profile6	6	VCO Bias Tcf<1:0> shift left by 3 + Charge Pump Current (Init)<5:0>	0x282[D4:D3] See PLL User Guide
7	profile7	7	Charge Pump Current<5:0>	0x27B[D5:D0]
8	Not Used	8	Loop Filter R3<3:0> shift left by 4 + Loop Filter R3 (Init)<3:0>	0x280[D3:D0] See PLL User Guide
9	Not Used	9	Loop Filter C3<3:0> shift left by 4 + Loop Filter C3 (Init)<3:0>	0x27F[D3:D0] See PLL User Guide
A	Not Used	A	Loop Filter C1<3:0> shift left by 4 + Loop Filter C2<3:0> shift right by 4	0x27E[D3:D0] 0x27E[D7:D4])

Program Address<7:4>	Assignment	Program Address<3:0>	Assignment (written to 0x29D) (see 0x29D for details of this column)	Location of Setup Words
B	Not Used	B	Loop Filter R1<3:0> + Loop Filter R1 (Init)<3:0>	0x27F[D7:D4] See PLL User Guide
C	Not Used	C	VCO Varactor Reference Tcf<2:0> + Rx VCO Divider<3:0>	0x290[D6:D4] 0x005[D7:D4]
D	Not Used	D	VCO Cal Offset<3:0> shift left by 1 + VCO Varactor Reference<3:0>	0x278[D6:D3] 0x291[D3:D0]
E	Not Used	E	Force VCO Tune<7:0>	0x277[D7:D0]
F	Not Used	F	Force ALC word<6:0> shift left by 1 + Force VCO Tune<8>	0x276[D6:D0] 0x278[D0]

Table 79.Tx Synthesizer Fast Lock Profile Table

TX LO GENERATION REGISTER 2A1

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
2A1	*Tx LO Gen Power Mode*	Power Mode<3:0>				Open				00h	R/W

SPI Register 0x2A1—Tx LO Gen Power Mode

These 4 bits control the bias current of the first divider, driven by the Tx VCO output. It is thermometer coded per Table 80.

Power Mode<3:0>	Bias Current (mA)	Relative Speed and Phase Noise
0000	16	Best (recommended)
0001	14	
0011	12	
0111	N/A	Not Used
1111	0 (Powered Down)	N/A

Table 80. Tx LO Bias Current

MASTER BIAS AND BANDGAP CONFIGURATION REGISTERS 2A6 AND 2A8

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
2A6	*Bandgap Config0*	Power Down Bandgap Ref	Master Bias Filter Bypass	Master Bias Ref Sel	Master Bias Trim<4:0>					04h	R/W
2A8	*Bandgap Config1*	VCO LDO Filter Bypass	VCO LDO Ref Sel	Bandgap Ref Reset	Bandgap Temp Trim<4:0>					00h	R/W

These registers set up the master bias and Bandgap reference in the AD9361. Configure these before enabling the clocks in 0x009.

SPI Register 0x2A6—Bandgap Config0

[D7] Power Down Bandgap Ref This signal, along with the PLL Enable bit in 0x009[D0] and the Master Bias Power Down bit in 0x058[D0], controls the states of the Master Bias and the Bandgap Reference per Table 81.

Power Down Bandgap Reference (0x2A6[D7])	Master Bias Power Down (0x058[D0])	PLL Enable (0x009[D0]	Master Bias Power State	Bandgap Power State
0	0	1	Up	Up
1	0	1	Down	Up

Power Down Bandgap Reference (0x2A6[D7])	Master Bias Power Down (0x058[D0])	PLL Enable (0x009[D0]	Master Bias Power State	Bandgap Power State
X	1	X	Down	Down
X	X	0	Down	Down

Table 81. Bandgap and Master Bias Power Down Bits

[D6] Master Bias Filter Bypass Test bit; set to zero. Setting this bit bypasses the master bias reference filters, allowing fast settling. Setting this bit is unnecessary because the AD9361 automatically generates a bypass pulse at VCO LDO power up. If this bit is used, set it high for at least 50us and then clear it.

[D5] Master Bias Ref Sel When clear, the master bias circuit uses a reference derived from the internal bandgap reference circuit. Setting this bit causes the master bias circuit to use a voltage supply derived reference.

[D4:D0] Master Bias Trim<4:0> These bits set the master bias reference level. Expected levels: if the "Master Bias Ref Sel" bit D5 is set, the trim should be 0x04 else it should be 0x0E. Expected levels may change.

SPI Register 0x2A8—Bandgap Config 1

[D7] VCO LDO Filter Bypass Test bit; set to zero. Setting this bit bypasses the VCO LDO reference filters, which allows fast settling. Setting this bit is unnecessary because the AD9361 automatically generates a bypass pulse upon master bias power up. If this bit is used, set it high for at least 50us and then clear it.

[D6] VCO LDO Ref Sel When clear, the VCO LDO reference derives from the internal bandgap circuit. If this bit is set to 1, the VCO LDO reference derives from the LDO input supply voltage (VDDA1P3_RX_VCO_LDO and VDDA1P3_TX_VCO_LDO).

[D5] Bandgap Ref Reset Test bit; set to zero. Setting this bit forces the bandgap reference into the correct operating condition. Setting this bit is unnecessary because the AD9361 generates a reset pulse internally upon bandgap circuit power up. If this is used, set it high for at least 100ns and then clear it.

[D4:D0] Bandgap Temp Trim<4:0> Expected value is 0x0E. Expected level may change.

REFERENCE DIVIDER REGISTERS 2AB AND 2AC

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
2AB	*Ref Divide Config 1*	Open					Set to 1	Rx Ref Reset Bar	Rx Ref Divider<1>	04h	R/W
2AC	*Ref Divide Config 2*	Rx Ref Divider<0>	Rx Ref Doubler FB Delay<1:0>		Tx Ref Reset Bar	Tx Ref Divider<1:0>		Tx Ref Doubler FB Delay<1:0>		00	R/W

SPI Register 0x2AB—Ref Divide Config 1

[D1] Rx Ref Reset Bar Clear this bit to reset the Rx synthesizer reference path divider flops.

[D0] Rx Ref Divider<1> The most significant bit of the Rx path divider control bits, mapped per Table 82. The LSB is in 0x2AC[D7].

Rx Ref Divider<1:0>	Divider Ratio
00	1
01	½
10	¼
11	2

Table 82. Rx Ref Divider Ratio

SPI Register 0x2AC—Ref Divider Config 2

[D7] Rx Ref Divider<0> See 0x2AB[D0].

[D6:D5] Rx Ref Doubler FB Delay<1:0>. Controls the feedback delay for the frequency doubler of the Rx synthesizer reference path. 0x00 results in a minimum delay while 0x11 results in maximum delay.

[D4] Tx Ref Reset Bar Clear this bit to reset the Tx synthesizer reference path divider flops.

[D3:D2] Tx Ref Divider<1:0> These bits control the Tx path divider, per the table described in bit D0 of 0x2AB.

[D1:D0] Tx Ref Doubler FB Delay<1:0> Same as bits D6:D5 but applies to the Tx path.

RX GAIN READ BACK REGISTERS 2B0 THROUGH 2B9

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
2B0	*Gain Rx1*	Open	Full Table Gain Index Rx1/LMT Gain Rx1<6:0>							--h	R
2B1	*LPF Gain Rx1*	Open			LPF gain Rx1<4:0>					--h	R
2B2	*Dig gain Rx1*	Open			Digital gain Rx1<4:0>					--h	R
2B3	*Fast Attack State*	Open	Fast Attack State Rx2<2:0>			Open	Fast Attack State Rx1<2:0>			--h	R
2B4	*Slow Loop State*	Open	Slow Loop State Rx2<2:0>			Open	Slow Loop State Rx1<2:0>			--h	R
2B5	*Gain Rx2*	Open	Full Table Gain IndexRx2/LMT Gain Rx1<6:0>							--h	R
2B6	*LPF Gain Rx2*	Open			LPF gain Rx2<4:0>					--h	R
2B7	*Dig Gain Rx2*	Open			Digital gain Rx2<4:0>					--h	R
2B8	*Ovrg Sigs Rx1*	Open	Gain Lock 1	Low Power 1	Large LMT OL	Small LMT OL	Large ADC OL	Small ADC OL	Dig Sat	--h	R
2B9	*Ovrg Sigs Rx2*	Open	Gain Lock 1	Low Power 2	Large LMT OL	Small LMT OL	Large ADC OL	Small ADC OL	Dig Sat	--h	R

SPI Register 0x2B0—Gain Rx1

This register holds the Rx1 gain index when the AD9361 is in a non-calibration state. It is valid for all gain control modes when the receivers are enabled. For full table mode (0x0FB[D3] set),this register returns the gain index of the full table. For Split Table Mode, this register returns the LMT gain index, 0x2B1 returns the LPF gain index, and 0x2B2 returns the Digital Gain index.

SPI Register 0x2B1—LPF Gain Rx1

See 0x2B0. Only valid in Split Gain Table Mode.

SPI Register 0x2B2—Dig Gain Rx1

See 0x2B0. Only valid in Split Gain Table Mode. Gain (dB) = index value. Gain is added between HB1 and RFIR filters.

SPI Register 0x2B3—Fast Attack State—Test Register

[D6:D4] Fast Attack State Rx2<2:0> The state of the Rx2 Fast AGC state machine mapped per Table 83. Valid for Rx or FDD modes.

Fast Attack State Rx2<2:0>	State Name	Description
0	Reset Peak Detectors	The state machine initializes to this state at start of RxON. The AD9361 holds all power and peak detectors in reset.
1	Peak Detect	In State 1, the AD9361 detects peak overloads and reduces gain until the overloads cease.
2	Power Measurement	The state machine waits for settling delay, measures power, and then adjusts gain to match the signal level to the AGC Lock Level.
3	Final Settling	If large peak overloads occur, the AD9361 decreases gain and moves to Final Over Range state, else it moves to state 5.
4	Final Over Range	The state machine resets the peak detectors and for the Peak Wait duration. On expiration of this counter, the state machine transitions to state 3.
5	Gain Lock	The state machine remains in this state until unlocked.

Table 83. Fast Attack AGC States

[D2:D0] Fast Attack State Rx1<2:0> Same as bit D6:D4 but applies to Rx1.

SPI Register 0x2B4—Slow Loop State

[D6:D4] Slow Loop State Rx2<1:0> This register indicates the state of the slow loop AGC for channel 1. This is valid only when channel 1 is in slow loop mode (see 0x0FA) and the receivers are enabled. The states are mapped per Table 84.

Slow Attack State Rx2<1:0>	State Name	Description
0	Reset	The state machine initializes to this state at start of RXON. The gain update counter and related functionality resets to 0.
1	Slow Measurement	Power measurement of the signal occur. A counter increments until it reaches the Gain Update Count, at which time the state machine moves to the Gain Change state.
2	Gain Change	Based on the results of the previous Slow Measurement state, the gain changes accordingly.
3	Clear Peak Detectors	The peak detector thresholds clear and the state machine stays in this state until the settling delay expires. This allows the Rx signal to settle before the AD9361 makes the next power measurement.

Table 84. Slow Attack AGC States

[D2:D1] Slow Loop State Rx1<1:0> Same as bits D6:D4 but applies to Rx1.

SPI Registers 0x2B5 through 0x2B7—Test Registers

These registers are the same as registers 0x2B0 through 0x2B2 but apply to Rx2.

SPI Register 0x2B8—Ovrg Sigs Rx1

[D6] Gain Lock 1 This bit high indicates that the Rx1 Fast Attack AGC has locked the gain.

[D5] Low Power 1 This bit high indicates that the Rx1 average signal power has dropped below the Low Power Threshold.

[D4] Large LMT OL 1 This bit high indicates that a large LMT overload occurred. The threshold for this overload is set in register 0x107.

[D3] Small LMT OL 1 This bit high indicates that a small LMT overload occurred in Rx1. The overload threshold is set in register 0x108.

[D2] Large ADC OL 1 This bit high indicates that a large ADC overload occurred in Rx1. The overload threshold is set in register 0x105.

[D1] Small ADC OL 1 This bit high indicates that a small ADC overload occurred in Rx1. The overload threshold is set in register 0x104.

[D0] Digital Sat 1 This bit high indicates that the signal saturated between HB1 RFIR in Rx1.

SPI Register 0x2B9—Ovrg Sigs Rx2-Test Register

Same as register 0x2B8 but applies to Rx2.

CONTROL REGISTER 3DF

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
3DF	*Control*	Open							Set to 1	00h	R/W

DIGITAL TEST REGISTERS 3F4 THROUGH 3F6

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
3F4	*BIST Config*	Tone Frequency<1:0>		Tone Level<1:0>		BIST Control Point <1:0>		Tone/ PRBS	BIST Enable	00h	R/W
3F5	*Observe Config*	Data Port SP, HD Loop Test OE	Rx Mask	Channel	Observation Point<2:0>				Data Port Loop Test Enable	00h	R/W
3F6	*BIST and*	Temp Sense Vbe		BIST	BIST	BIST	BIST	Data	Use Data	00h	R/W

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
	Data Port Test Config	Test<1:0>		Mask Channel 2 Q data	Mask Channel 2 I data	Mask Channel 1 Q data	Mask Channel 1 I data	Port Hi/Low	Port		

SPI Register 0x3F4—BIST Config—Test Register

[D7:D6] Tone Frequency<1:0> Sets the BIST frequency according to Equation 59.

$$BIST\ Tone\ Frequency = \frac{Clk * (Tone\ Frequency < 1:0 > +1)}{32}$$

Equation 59

Where the Tone frequency units are the same as for Clk and Clk is clock rate shown in Table 86.

[D5:D4] Tone Level<1:0> Sets the gain of the tone signal per Table 85. "FS" represents a full scale digital output.

Tone Level<1:0>	Amplitude
00	±FS
01	±FS/2
10	±FS/4
11	±FS/8

Table 85. BIST Tone Level

[D3:D2] BIST Control Point<1:0> These bits control where the BIST signal is injected per Table 86

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Control Point<1:0>	Injection Point	"Clk" used for BIST Tone Frequency	Comments
00	Input of Tx (output of Data Port)	Tx Sample Rate	Tx Only
01	Not Used		
10	Input of Data Port	Rx Sample Rate	Rx Only
11	Not Used	N/A	N/A

Table 86.BIST Control Point

[D1] Tone/PRBS When this bit is clear, the BIST outputs a PRBS signal. When set, the BIST outputs a tone. The PRBS is a 16-stage, 14-tap generator that uses the 16th order polynomial shown in Equation 60.

$$G(x) = x^{16} + x^{15} + x^{14} + x^{13} + x^{12} + x^{11} + x^{10} + x^9 + x^8 + x^7 + x^6 + x^5 + x^3 + x^2 + 1$$

Equation 60

The AD9361 implements this polynomial as a 16-bit shift register, 14 taps of which are XORed and then fed into the input of the bit 15 of the shift register. See Figure 6.

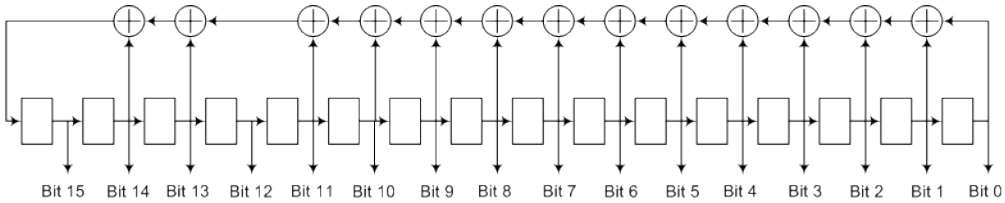

Figure 6.PRBS Shift Register and XOR implementation. "I" Word Shown.

The polynomial exponents 1 to 16 map to bit positions 15 to 0. Since x^1 and x^4 are not part of the polynomial, the outputs of shift registers 15 and 12 are not tapped. The PRBS is implemented using the code shown below.

```
// PRBS polynomial - 16 15 14 13 12 11 10 9 8 7 6 5 3 2
//-----------------------------------------------------------------------
always @ ( posedge I_bist_clk )
 if ( ~O_bist_enable )
  prbs_data <= 16'h0A54;              /*this is the seed value  */
 else
  prbs_data <= { (prbs_data[ 0] ^ prbs_data[ 1] ^ prbs_data[ 2] ^ prbs_data[ 3] ^
            prbs_data[ 4] ^ prbs_data[ 5] ^ prbs_data[ 6] ^ prbs_data[ 7] ^
            prbs_data[ 8] ^ prbs_data[ 9] ^ prbs_data[10] ^ prbs_data[11] ^
            prbs_data[13] ^ prbs_data[14] ), prbs_data[15:1] };

assign prbs_data_rev = { prbs_data[ 0], prbs_data[ 1], prbs_data[ 2], prbs_data[ 3],
                  prbs_data[ 4], prbs_data[ 5], prbs_data[ 6], prbs_data[ 7],
                  prbs_data[ 8], prbs_data[ 9], prbs_data[10], prbs_data[11],
                  prbs_data[12], prbs_data[13], prbs_data[14], prbs_data[15] };
```

Where
prbs_data is the "I" PRBS data
prbs_data_rev is the "Q" PRBS data and is a bit inversion of the "I" data (e.g. bit 0 of "I" is bit 15 of "Q").

[D0] BIST Enable Set this bit to enable the BIST generator.

SPI Register 0x3F5—Observe Config—Test Register

[D7] Data Port SP, HD Loop Test OE See D0. If performing a loop-back test and the AD9361 is in single-port, half-duplex mode, this bit must also be set. This causes the data driven into the TX data bits to loop back onto the Rx data port of the Port not being used.

[D6] Rx Mask Set this bit to mask the analog signals from propagating to the digital blocks.

[D5] Channel When this bit is clear, observe Channel 1. When the bit is set, observe Channel 2.

[D4:D1] Observation Point<3:0> These bits determine where the in the digital signal path the data is sent to the Data Port. See Table 87.

Observation Point<3:0>	Output Block
0000	Rx ADC Data (4 bits)
0001	Tx HB2 Output Data (15 bits)
0010	Tx HB3/Int3 Output Data (12 bits)
0011	Rx RFIR Output Data (16 bits)
0100	Tx Quad Cal DC_I, DC_Q Outputs (12 bits)
0101	Tx Quad Cal Amplitude, Phase Outputs (8 bits)
0110	Rx Quad Cal Amplitude, Phase Outputs (11 bits)

Table 87.BIST Observation Point

[D0] Data Port Loop Test Enable Test bit. When set, this bit causes the data driven into the TX data bits to loop back onto the Rx data port of the port not being used. Useful for testing setup/hold times of the data ports. If in single port, half-duplex mode, also set D7.

SPI Register 0x3F6—BIST and Data Port Test Config—Test Register

[D7:D6] Temp Sense Vbe Test<1:0> Test bits. Set to zero for normal operation. Test modes listed in Table 88.

Temp Sense Vbe Test<1:0>	Operation
00	Normal operation (select Temp Sensor if it is powered up, else select AuxADC)
01	Force temp sensor Vbe to power up and set the Vbe voltage to the low current Vbe state
10	Force Input to AuxADC to be the AuxADC input (not temp sensor)
11	Force temp sensor Vbe to power up and set the Vbe voltage to the high current Vbe state

Table 88.Temp Sense VBE Test

[D5:D2] BIST Mask Bits Setting one of these 4 bits zeros out the data in question. E.g, setting bit D5 zeros out Channel 2 "Q" Data.

[D1] Data Port Hi/Low If clear, the lower 12 bits of the observation data propagate to the Data Port, else the upper 12 bits propagate to the Data Port.

[D0] Use Data Port Set this bit to enable the Data Port to drive observation data out of the AD9361.

DAC TEST REGISTERS 3FC THROUGH 3FE

Register Address	*Name*	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
3FC	*DAC Test 0*	DAC test Word <7:0>								FFh	R/W
3FD	*DAC Test 1*	DAC test Word <15:8>								FFh	R/W
3FE	*DAC Test 2*	DAC Test Enable	DAC test Word <22:16>							3Fh	R/W

Test registers used for DC characterization of the DAC on ATE. When 0x3FE[D7] is set, the DAC word for all enabled TX channels is driven by the word <22:0> in registers 0x3FC through 0x3FE.