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RESEARCH ARTICLE

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Time-interleaved SAR ADC design with background calibration

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Summary

In this article, a low power time-interleaved SAR (TI-SAR) ADC is presented. Background calibration is used to improve the linearity of the ADC. Offset, gain, and capacitor mismatches between interleaved channels are calibrated by postprocessing the ADC output. Besides, a novel trimming-based calibration algorithm is used to calibrate the timing mismatches between channels. The proposed calibration algorithm is more power-efficient compared with most of its counterparts. The ADC consists of 18 parallel channels, a reference channel with two dummy channels, and a channel for timing calibration. The timing calibration channel is clocked only when the reference channel samples. The dummy channels are utilized to equalize the input load over time as they sample one after another to fill the gap where the reference channel does not sample. There is no need for any other dummy channels for timing calibration channel since it has low kickback noise over input driver. Each parallel channel operates at 111 ms/s while the reference channel runs at 105 ms/s. The aggregate sampling speed of the converter is 2 GS/s, and 52-dB SNDR is accomplished near Nyquist frequencies.

KEYWORDS

differentiator, time-interleaving background calibration, trimming

1 | INTRODUCTION

High-speed analog-to-digital converters with moderate resolutions are used in many applications such wireless communication, optical communication, serial-link receivers, direct-sampling TV receivers, and digital oscilloscopes. On the other hand, power-efficient wideband analog-to-digital converters (ADCs) are needed for many battery-powered portable devices. Increasing speed or resolution of ADCs results in power penalty. Power consumption increases nearly linearly with increasing resolution or sample rate up to process boundaries. However, when approaching process boundaries, power consumption increases beyond linear.[1,2] Time-interleaved ADCs are commonly used to overcome this problem since they have effective power/speed trade-off when the speed approaches the process boundaries.[2,3] Besides, since comparator speed decreases by interleaving subADCs, metastability rate also decreases by time-interleaved architecture.[3]

Despite the benefits mentioned before, mismatches among the subADC channels can degrade linearity.[4-12] Mismatch errors can be categorized into two classes: static and dynamic errors. Gain mismatch, offset mismatch, and capacitor mismatch of subADCs are static error sources. Static errors are frequency independent and dealt easier compared

Abbreviations: ADC, analog to digital converter; SAR, successive approximation register; TI, time-interleaved; FATI, Flash assisted time-interleaved.

with dynamic errors. Dynamic errors are input frequency-dependent errors, which include timing skew mismatch and bandwidth mismatch errors. Dynamic mismatch errors gain dominance as input signal frequency increases and may become most dominant error source when digitizing high-frequency inputs. Both static and dynamic mismatch errors can be corrected by utilizing calibration circuits.

There are many studies about time-interleaved ADCs and their calibration. The mismatches between subchannels in TI-ADC circuits can be detected either using reference channels[13-16] or by applying stochastic analysis to the ADC output.[17-19] In Le Dortz et al,[18] a 1.62-GS/s time-interleaved successive approximation register (SAR) ADC is realized. Digital-to-analog converter (DAC) capacitors in Le Dortz et al[18] are finger metal-oxide-metal (MOM) structures, which allow to realize smaller unit capacitances with good matching. Such MOM capacitors are used in that study. A digital background calibration mechanism is proposed to calibrate offset, gain, and skew mismatches. However, digital filters can be power hungry and can reduce the overall power efficiency. Besides, the calibration engine requires the input signal to be wide-sense stationary and band-limited to the Nyquist frequency. In Liu et al,[16] two reference channels are used for calibration, which relax input signal requirements. One of these channels is used to calibrate offset, gain, and capacitor mismatches while the other channel is used for timing skew calibration only. However, to equalize input load over time, four dummy channels are used that cause redundant power dissipation and extra input load. In this study, one reference channel with two dummy channels are used to calibrate offset, gain, and capacitor mismatches as in Stepanovic and Nikolic, [16] while for timing calibration, a new method is proposed that allows reducing extra load and realizing a approximately 20% lower power dissipation in comparison with Stepanovic and Nikolic.[16] The proposed ADC consists of 18 parallel channels, one reference channel, and two dummy channels. An additional channel used for timing skew calibration. The digital background calibration system is designed and simulated in MATLAB and Verilog environment. Sampling speed of the converter is 2 GS/s and 52-dB SNDR is accomplished around Nyquist frequencies.

In Section 2, the architecture of the TI-ADC is given. In Section 3, the SAR subADCs are modeled. The applied calibration algorithm is detailed in Section 4. Finally, the simulation results are presented, and paper is concluded in Sections 3.2 and 3.3.

2 | ADC ARCHITECTURE

The overall structure of the ADC is given in Figure 1. As seen from the figure, the ADC consists of 18 parallel working channels, a reference channel with two dummies, and a channel for timing calibration. The dummy channels of the reference are used to have constant load at the input as in Stepanovic and Nikolic.[16] In Figure 2, the clocking scheme is shown for all channels including the reference and dummy channels. Two dummy channels are clocked accordingly to fill the gap after the reference channel, and they are reset before each activation to avoid memory effects.

Track and hold circuits (T/H) shown in Figure 1 are functional blocks instead of separate front-end circuits. Figure 3 shows the SAR subADC circuits, which corresponds to "T/H" and "ADC" blocks in Figure 1. However, in Figure 3, a single ended structure is shown for simplicity, where the real subADCs are differential. The input switches in this circuit

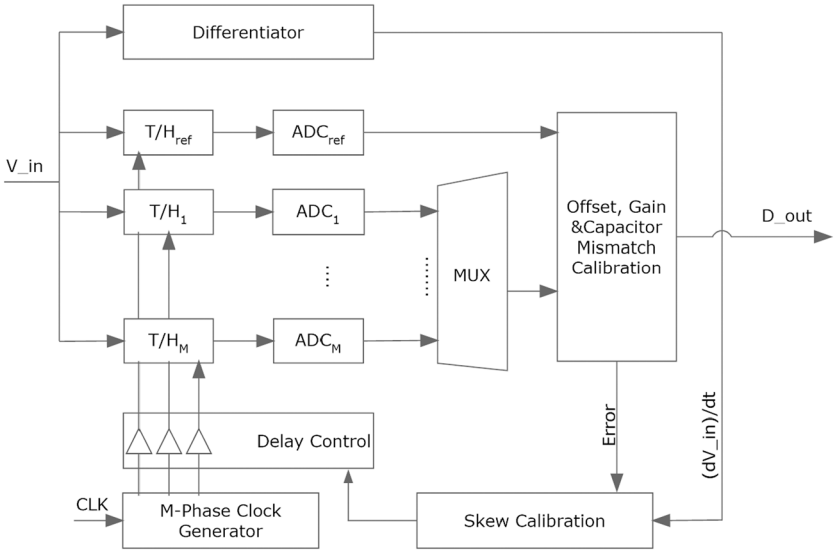

FIGURE 1 Overall analog-to-digital converter (ADC) architecture

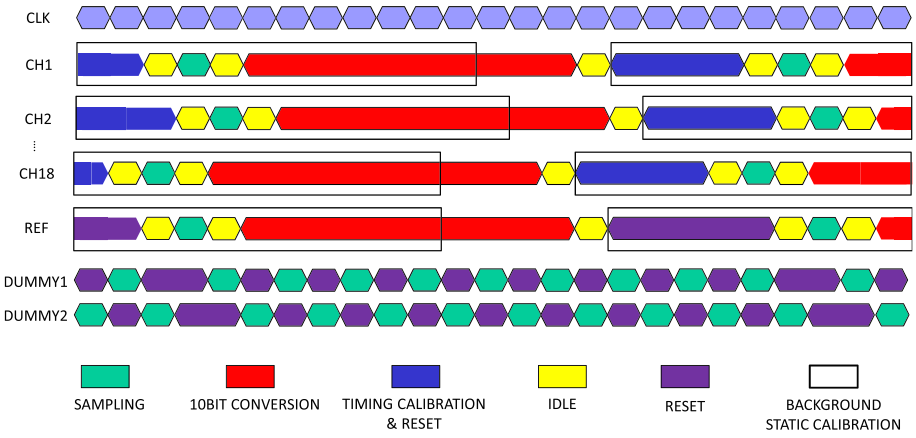

FIGURE 2 Relative timing of subchannels and modes of operation [Colour figure can be viewed at wileyonlinelibrary.com]

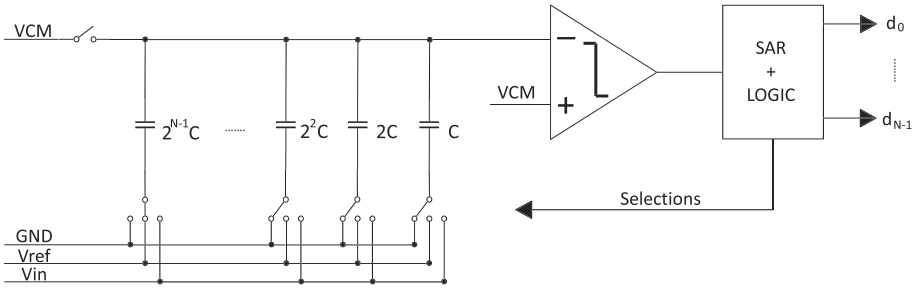

FIGURE 3 The SAR subADC circuit

are bootstrapped sampling switches. The comparator is a classical strong arm latch comparator and the SAR logic consists of a classical shift register and flip flops to retain the bits. To control the sampling clock delays, the low jitter multiphase clock distribution circuit proposed in Stepanovic and Nikolic[16] is used.

The minimum number of subADCs is determined by the sampling cycle in addition to the conversion and reset cycles. Therefore, considering 10-cycle conversion, one cycle sampling and one cycle of reset yields a minimum of 12 cycles per conversion; a minimum number of 12 subADCs are needed. Note that to calibrate skew mismatches, sampling clock delays must be trimmed also (will be explained later). However, clock delays can be trimmed any time outside the sampling phase. On the other hand, at least 10 cycles (5 ns) are required for static background calibration for the worst-case scenario (corner: slow-slow, $V_{DD} = 0.81V, temp = 125^oC$). To alleviate timing constraints, 14 cycles are allocated for static mismatch calibration. Since the reference channel must be calibrated between each conversion, minimum 13 subADCs are needed (14 cycles interval between consecutive calibration routines) for a healthy calibration mechanism. In our design, we decided to use 18 parallel subADCs to alleviate timing constraints for both conversion and calibration phases. In conversion phase, 3 idle cycles are added, and "reset & timing calibration" step is extended to 4 cycles. In static background calibration, 4 idle cycles are added for the interleaved channels, and 5 idle cycles are added for the reference channel. This overhead is decided to relieve timing constraints and to make the design flexible for further improvements in terms of speed or resolution. We should note that this number of subADCs can be reduced (to a minimum of 12 subADCs) at the expense of tighter timing constraints as well as reduced flexibility in the design.

The clocking scheme of the ADC is illustrated in Figure 2. In the figure, each hexagon corresponds to a phase. The clock schemes of the first, second, and last (18^{th}) channels are given in addition to the schemes of the reference and dummy channels. The phases are coloured different from each other to understand the operation clearly. As seen from the figure, the reference channel convolves over the interleaved channels and two dummy channels are used to fill the gap when the reference channel does not sample.

3 | MODELING TI-SAR ADC

In this section, first, the ideal input-output (I/O) relation of an ideal SAR ADC is modeled. Then, static and dynamic error sources of the SAR ADC are modeled. Finally, the effect of the mismatch errors between multiple SAR subADC channels in TI-ADC structure are examined.

3.1 | Modeling ideal SAR ADC

In Figure 3, a simple SAR ADC circuit is shown. Assuming an input voltage Vin within $[0, V_{ref}]$ range and comparator differential input $V_x = V_p - V_n$, testing each bit from MSB to LSB yields V_x value of

$$\Delta V_x = V_{ref} \frac{C_i}{C_{tot}}. \tag{1}$$

Summing these differences gives I/O relation of the ADC as

$$V_{in} = V_Q + V_{ref} \sum_{i=0}^{N-1} \left(d_i \frac{C_i}{C_{tot}} \right), \ where \ \frac{C_i}{C_{tot}} = 2^{i-N}. \tag{2}$$

V_{in} is analog input voltage, V_Q is quantization noise, d_i is the conversion result related to i^{th} bit, C_i is capacitance in the array related to i^{th} bit, C_{tot} is total capacitance in the array, and N is number of bits.

3.2 | Modeling static errors

Static error sources in SAR ADCs are radix errors due to DAC capacitor mismatches, offset error due to antisymmetric comparator, and gain error due to the deviation in the reference voltages.[2,20] Besides, charge injection may contribute to both gain and offset errors. All these errors can be modeled by the equation below

$$V_{in} = V_Q + V_{OS} + (1 + \Delta G)\ V_{ref} \sum_{i=0}^{N-1} \left(d_i \frac{C_i}{C_{tot}} \right), \tag{3}$$

where V_{OS} is offset and ΔG is gain errors. This equation can be simplified by lumping all the terms other than comparator decisions d_i into w_i, which can be interpreted as a modified bit weight for the i^{th} output bit. With such a simplification and ignoring quantization noise V_Q, equation 3 simplifies to the following:

$$V_{in} = V_{OS} + \sum_{i=0}^{N-1} (d_i w_i), \tag{4}$$

where

$$w_i = (1 + \Delta G)\ V_{ref}\ \frac{C_i}{C_{tot}}. \tag{5}$$

Equation 4 can be rewritten in matrix form as

$$V_{in} = V_{OS} + DW, \tag{6}$$

where

$$D = \begin{pmatrix} d_0 \\ d_1 \\ . \\ . \\ d_{N-2} \\ d_{N-1} \end{pmatrix}^T, W = \begin{pmatrix} w_0 \\ w_1 \\ . \\ . \\ w_{N-2} \\ w_{N-1}. \end{pmatrix} \tag{7}$$

Note that Equation 4 can be generalized to the differential SAR ADCs by simply extracting "V_{ref}" from the right side of the equation. Even without changing the equation, the differential SAR ADC can be modeled since the offset parameter V_{OS} can include the constant term '$-V_{ref}$'.

Equation 6 is used in digital background calibration. Knowing offset voltage V_{OS} and weight coefficient vector W, the correct value of the input voltage V_{in} can be calculated using this equation. Note that the gain and offset errors do not degrade linearity in a single core ADC. However, in time-interleaving architectures mismatch of these errors among channels degrade linearity by a significant amount.

3.3 | Modeling dynamic errors

Dynamic errors are input frequency dependent errors. Sampling aperture and finite bandwidth are dynamic error sources.

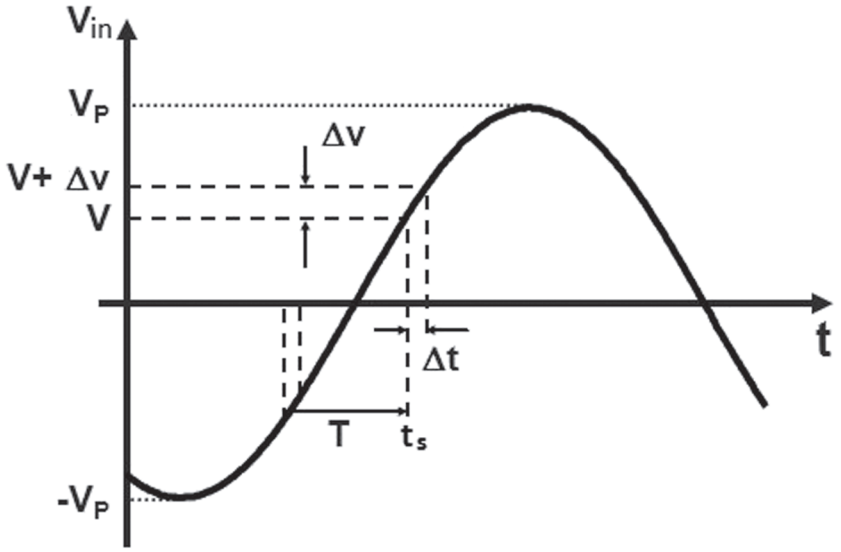

FIGURE 4 Sampling aperture

Sampling aperture is caused by shifting of the sampling clock signal in time domain. Let us denote the clock edge shift in time as Δt and expected sampling time as t_s. Then, the actual sampling time with sampling aperture becomes $t_s + \Delta t$ as shown in Figure 2. The error caused by the static timing error can be calculated using Taylor approximation as

$$\varepsilon_t = V_{in}(t_s + \Delta t) - V_{in}(t_s) \cong \Delta t \frac{d}{dt} V_{in}(t_s). \tag{8}$$

The sampling aperture can be expressed as a function of derivation of the input signal and the error caused by aperture.

$$\Delta t \cong \frac{\varepsilon_t}{\frac{d}{dt} V_{in}(t_s)}. \tag{9}$$

Static timing error (skew) does not degrade linearity in a single core ADC. However, sampling aperture mismatch between channels of a TI-ADC degrades linearity especially when high-frequency input signal exists.

3.4 | Channel mismatch errors in TI-ADC

Equations 6 and 8 were derived to model static and dynamic errors in a single core ADC. Combining them gives

$$V_{in} = V_{OS_j} + DW_j + \Delta t_j \frac{d}{dt} V_{in}. \tag{10}$$

In equation 11, "j" indicates the j^{th} parallel channel in TI-ADC structure.

3.5 | Other error sources in TI-ADC

In this section, error sources that are not included in the model derived in Equation 11 and their effects are discussed.

3.5.1 | Noise

Since the designed ADC operates at high frequencies, thermal noise has dominance over other low frequency noise types. In general, the total sampling capacitance in ADC circuits is determined by thermal noise. The thermal noise in our circuit would be dominated by the comparator noise, and the sampling switch thermal noise would be a minor contributor. As a result, we assumed that the switch thermal noise would be a minor noise source, which can be assumed to have a level similar to the quantization noise. Using this level, we calculated a lower limit for the sampling capacitor depending on the desired number of bits "N" and positive and negative reference voltages "$V_{ref}+$" and "$V_{ref}-$" as

$$C_S \geq \frac{3kT}{((V_{ref}+) - (V_{ref}-))^2} 2^{2N+1}, \tag{11}$$

where "k" is Boltzman constant and "T" is absolute temperature. For 10-bit resolution and $1.8 - V$ differential full-scale swing, the sampling capacitance must be higher than $32fF$. In our case, the sampling capacitor is determined considering

not only the front-end thermal noise but also the comparator noise, capacitor mismatches, and parasitics. Thus, the sampling capacitance is determined $80fF$. Kick-back noise is another important noise contributor in ADC circuits. To lower kick-back noise, input buffer is generally preferred option,[21,22] but it comes with power penalty. In our circuit, input capacitance is small, which eliminates the necessity of using buffer. Instead, input load is equalized over time using dummy channels.

3.5.2 | Clock jitter

Clock jitter is an important error source in high-bandwidth ADCs. Equation 8 can be used to see the effect of jitter also and determine the limit of the jitter for a given input frequency. The difference between the jitter and skew is that the skew is constant timing aperture while jitter is random like noise. To lower the jitter, the sampling clock path is shortened, and noisy elements on the clock path are eliminated as possible as in Stepanovic and Nikolic.[16]

3.5.3 | Bandwidth mismatch

Bandwidth mismatch is another error source especially for high-bandwidth TI-ADCs. Input resistance of the driver forms a pole with the sampling capacitance of the ADC. If this parasitic pole is near Nyquist frequency, the bandwidth mismatch between channels degrade linearity. In our case, 50Ω input driver resistance, 230Ω switch resistance and $200fF$ total input capacitance cause a pole in $2.8GHz$, which is distant enough from Nyquist frequency. Thus, bandwidth mismatch correction is not necessary in our case.

Other error sources include nonlinear charge injection, finite slew rate, and other nonlinear mismatches between channels. To lower the nonlinear charge injection bottom-plate sampling method is used to have constant charge leakage over the DAC capacitors and top plates of the DAC capacitors are connected to the input via bootstrapped switches to linearize the leakage as possible. Finite slew rate has lower effect in our case since the capacitors are small. Note that any static linear error can be modeled by the Equation 11 and corrected by the calibration algorithm.

4 | CALIBRATION

Calibration mechanism works to find the exact values of W_j and V_{OSj} parameters of each channel to correct the ADC results by postprocessing. On the other hand, it corrects timing mismatch errors by trimming sampling clock delays of each channel.

4.1 | Calibration of static errors

Ignoring the timing error in Equation 11, it can be simplified as below:

$$V_{in} = V_{OS_j} + DW_j. \tag{12}$$

This equation is sufficient for modeling offset, gain, and capacitor mismatches among channels. Calibration algorithm is expected to find the values of the W_j and V_{OSj} parameters of each channel. Note that all the linear nonidealities (including constant and linear portion of charge injection) can be lumped into Equation 13 and calibrated as explained below. Of course, the mentioned linearity here refers to Equation 13, where the variables are raw output bits (D). Timing skew is a nonlinear type of nonideality that our calibration addresses. However, except for errors due to timing skew, additional nonlinear errors cannot be addressed by the current algorithm.

As stated before, a reference channel is used to calibrate mismatches between channels. Offset error of each channel V_{OSj} is calculated according to the reference channel, and its effects on output are eliminated by postprocessing. Capacitor and gain mismatches are also calibrated by adjusting W_j parameters. The calibration mechanism can be explained in several steps:

1. The input signal is sampled onto both the reference channel and the channel under calibration.
2. The digital outputs D_0 and D_j are obtained after conversion, where D_0 and D_j are the raw output words of the reference channel and j^{th} parallel channel, respectively.
3. The digital words are calibrated using current offset and weight coefficients for the channels and calibrated outputs are obtained as

$$D_{out_0} = D_0 W_0, \tag{13}$$

$$D_{out_j} = V_{OS_j} + D_j W_j, \tag{14}$$

where D_{out0} and $D_{out\,j}$ are calibrated outputs. Then $D_{out\,j}$ is conducted to the output.

4. Comparing the reference and the current channel outputs, the error is calculated.

$$\varepsilon = D_{out_0} - D_{out_j}. \tag{15}$$

Note that ideally, the outputs are same, and error is 0 since both the reference and current channel samples the same input signal. Calibration mechanism is expected to decrease the error term to a certain interval.

5. The offset parameter and weight coefficients of the subchannels are updated according to the LMS algorithm.

$$V_{OS_j}{}^{k+1} = V_{OS_j}{}^{k} - \varepsilon \mu_{OS}, \tag{16}$$

$$W_0{}^{k+1} = W_0{}^{k} + \varepsilon(\mu_W \odot D_0), \tag{17}$$

$$W_j{}^{k+1} = W_j{}^{k} - \varepsilon(\mu_W \odot D_j), \tag{18}$$

where k is the number of iteration, $V_{OS_j}{}^{k}$ is the offset parameter of the j^{th} subchannel at the k^{th} iteration, $W_j{}^{k}$ is the k^{th} iteration of the bit weight vector for the j^{th} subchannel, and $W_0{}^{k}$ is the k^{th} iteration of the bit weight vector for the reference channel. μ_{OS} is convergence coefficient for offset, μ_W is the vector of convergence coefficients for DAC capacitors'; weights and $\odot$ is the symbol for element-wise product (or Hadamard product).

6. Repeat all steps for the next channel to be calibrated (ie, increase j or if it is 18 reset it to 1).

Note that in Equation 18 and 19, the weight vectors of the reference channel and the current channel under calibration are updated in opposite directions. Thus, all-zero solution is avoided.

After calibration interleaving channels'; offsets are equalized to the offset of the reference channel. Thus, the whole ADC works as a single core ADC, which has same offset with the reference channel. Note that offset error does not degrade linearity for a single core ADC. Capacitor and gain mismatches are also calibrated by adjusting W_j parameters. The gain and capacitor mismatches of the reference channel are also calibrated by adjusting W_0 parameter. Thus, the gain and capacitor weight coefficients converge some average values.

4.2 | Calibration of timing mismatches

Timing mismatches are trimmed by the calibration algorithm using delay elements on the sampling clock paths. All sampling apertures of the interleaving channels are aligned according to the reference channel.

Knowing the sampling aperture-related error at the output and the derivation of the input signal, channel delay can be calculated as

$$\Delta t_j \cong \frac{\varepsilon_t}{\frac{d}{dt}V_{in}(t_s)}, \tag{19}$$

where ε_t is sampling aperture-related error at the output and Δt_j is adjustable sampling clock delay of the j^{th} channel.

To find the sampling aperture error ε_t, the outputs of the reference channel and the current channel under calibration are subtracted as in Equation 16, which is used to find the static error.

$$\varepsilon_t = D_{out_0} - D_{out_j} = \varepsilon. \tag{20}$$

The difference between the reference and the current interleaving channels' outputs is used both in static and dynamic calibration algorithm since the static and dynamic errors cannot be separated. Using LMS algorithm, channel delay can be trimmed as

$$\Delta t_j{}^{k+1} = \Delta t_j{}^{k} + \frac{\varepsilon}{\frac{dV_{in}(t_s)}{dt}}\mu_t. \tag{21}$$

However, an accurate value of the derivation of the input signal cannot be attained easily, and multiplications and divisions in digital domain consume much power and time if Equation 22 is used in calibration routine. To overcome this issue, an accurate value of the channel skew t_j can be approximated by constant steps μ_t, which can be forward or backward according to the sign of the error and derivation.[16]

$$\Delta t_j{}^{k+1} = \Delta t_j{}^{k} + sign(\varepsilon)\ sign\left(\frac{dV_{in}(t_s)}{dt}\right)\ \mu_t. \tag{22}$$

To trim channel skew Δt_j, a capacitor array is used. Inserting or disconnecting a unit capacitor on clock path causes μ_t delay change. Note that the calibration parameters ε and ε_t are same and obtained by subtracting the calibrated outputs of the reference and the current channel under calibration. Once the error term ε is obtained (4^{th} step of the static calibration in Section 4.1), it can be used to trim the timing skew anytime outside the sampling phase. In our work, the skew is trimmed after 10-bit conversion inside the reset phase after updating the static calibration parameters as seen in Figure 1. The trimming range Δt_{max} and trimming resolution μ_t are determined according to the expected maximum timing mismatches and required maximum delay resolution. After calibration, Δt_j can be lowered than μ_t. In this case, timing error is desired to be lower than 9-bit level around Nyquist frequencies. To calculate μ_t, let us have sinusoidal input signal at Nyquist frequency

$$V_{in}(t) = \sin\,(2\pi 10^9 t). \tag{23}$$

Then, after calibration channel, delay mismatches will be lowered than μ_t, and in this case, the timing error will be

$$\varepsilon_t \leq V_{in}(t_s + \mu_t) - V_{in}(t_s) \cong \mu_t \,\frac{d}{dt} V_{in}(t_s). \tag{24}$$

To guarantee that timing error is lower than 9-bit level, μ_t must be chosen small enough.

$$\varepsilon \leq \frac{1}{2^9}. \tag{25}$$

$$\mu_t\,(2\pi 10^9 t)\;\cos\,(2\pi 10^9 t) \leq \frac{1}{2^9}. \tag{26}$$

$$\mu_t \leq 311 fs. \tag{27}$$

Since expected maximum channel delay deviation is around 15 ps and maximum step is 311 fs, the minimum number of delay levels is $\frac{15ps}{311fs} = 50$.

Timing calibration is necessary if high-frequency input signal is applied. If low-frequency input signal is applied, the timing related portion of the error term ε will be small enough to be ignored. Besides, applying timing calibration at low frequencies may cause divergence of calibration since other error sources may be confused with timing error and reacted this way. To overcome this issue, timing calibration must be switched on only when high-frequency input signal is applied. Figure 5 shows the switching properties of the timing calibration over amplitude and frequency of the sine wave input signal.

Note that the activation of the timing calibration is actually related to the value of the input signal's derivative. The amplitude of this derivative is easy to figure out for the special case of a sinusoidal input, which is indicated by the curve in Figure. As a more general rule, if the derivative of the input signal exceeds a threshold, the calibration would be activated. Since the error contribution due to timing skew is proportional with the derivative of the input signal and the timing calibration is activated when the derivative is high, it means that the timing calibration is activated only when it is needed.

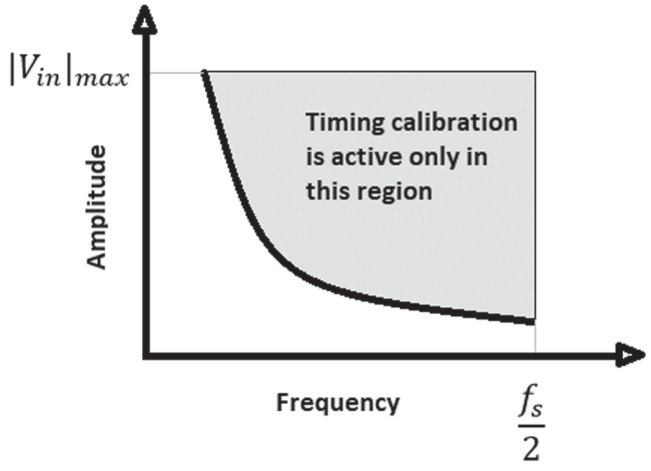

FIGURE 5 Activation of timing mismatch calibration depending on the input amplitude and frequency

4.3 | A novel switching circuit for timing calibration

In this section, a novel circuit structure is proposed to control timing calibration. Timing calibration must be activated only when a high-frequency input signal (with sufficiently high amplitude) is applied as shown in Figure 5. In other words, when input signal changes faster than some predetermined level, timing calibration must be activated.

Figure 6 shows input differentiator circuit, which gives 3 possible outcomes (00,01,10) with 2 bits UP and DOWN. CLK signal is inverted sampling clock of the reference channel. In this circuit, capacitor currents are sensed by current conveyors and transferred to the inputs of the tilted comparators. If the comparators flip to the different sides, one of the output ports (UP or DOWN ports) flips to "HIGH"; otherwise, both outputs remain.

The schematic implementation of the tilted current comparators is given in Figure 7. To change the prime state ("LOW") of the output nodes ('UP' and 'DOWN' ports), current difference between C1 and C2 capacitors must be high enough. Thus, only high amplitude and high-frequency input signals can change the prime state as shown in Figure 5. If the prime state changes, calibration engine senses this change, and clock delay is adjusted. If "UP" signal rises, an extra delay capacitor is added to the clock path, and if "DOWN" signal rises, the last added delay capacitor is removed from the clock path.

The tilted current comparator used in switching circuit is given in Figure 7. One of the two tail MOSFETs (M1 or M2) is wider than other to implement the tilting. This causes deliberately added offset between comparator inputs. Thus, only sufficiently high differential input signals can change the prime state of the comparator; otherwise, the comparator output remains the same at each cycle.

The main reason to use this type of comparator is to have minimum front end distortion. In comparison with strong ARM latch comparator,[23] this circuit has lower kick-back noise back to the driver circuit. Because, the kick-back signal is coupled to the input through gate-drain capacitance C_{gd} instead of gate-source capacitance C_{gs}. We should note that

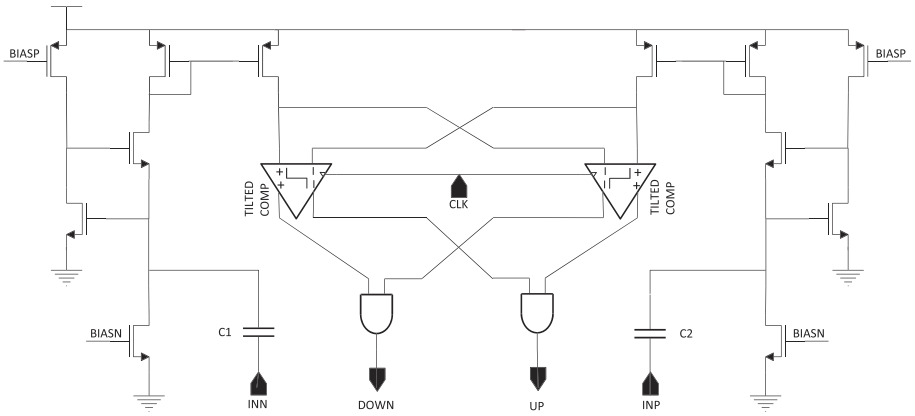

FIGURE 6 Current conveyor based differentiator

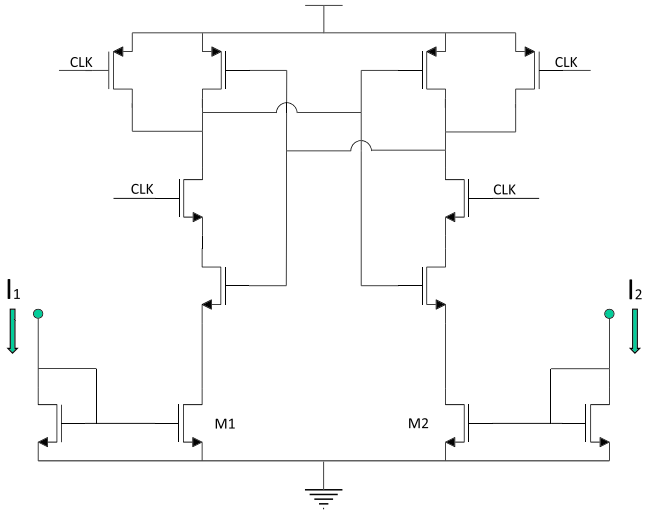

FIGURE 7 Tilted current comparator [Colour figure can be viewed at wileyonlinelibrary.com]

front-end distortion is one of the main bottlenecks in the design since a front-end buffer is not used, and kick-back noise forms an important part of the overall front-end distortion.

The differentiator structure proposed in this study consumes much less power than digital differentiators. In Le Dortz et al,[18] the proposed digital differentiator-based skew calibration consumes 35 mW, which corresponds to 38% of the overall power consumption. Other than that, in Stepanovic and Nikolic,[16] the power consumption due to the timing calibration is estimated to reach 20% to 25% of the overall the power consumption of the analog part since an extra channel loads input driver with dummies and all conversion cycle required for the calibration. However, in our proposal, only two comparators need to be clocked at each calibration cycle. Besides, the capacitors used at the input are smaller than the sampling capacitors of the calibration channel in Stepanovic and Nikolic.[16] In Xu,[24] a high pass filter with a comparator at the output is proposed to obtain the direction of the input signal and thus to switch calibration mechanism accordingly. However, a simple RC circuit has a tradeoff between output signal swing and phase distortion if the band of interest approaches the high-pass corner frequency. It is not possible to obtain exact 90^o phase shift and high amplitude at the filter output. The high frequency pole can be shifted away using opamp-based differentiator. However, opamp-based differentiators could also suffer from tradeoff between phase distortion and output swing if the opamp gain is not sufficiently high. Besides, since the supply voltage is small, the voltage-based differentiator could saturate easily and cause extra delay. In our work, thanks to the feedback mechanism on the current-sensing node of the current conveyor, the high-pass corner frequency is set high enough so that the phase distortion remains tolerable throughout the ADC Nyquist band and maintain a differentiator response. Therefore, to achieve a small phase distortion while maintaining an acceptable output signal, a current conveyor-based architecture was preferred.

The differentiating function is realized by the input capacitors C_1 and C_2. The local feedback at the input at the node where the differentiating capacitors connect lowers the impedance of that node. Therefore, as long as the driver has low enough impedance, the differentiator response is dominated by the capacitor (C_1 and C_2). This capacitor has better linearity than an alternative with active components. After the differentiator, all the node impedances are dominated by diode connected transistors. As a result, all the nodes within the conveyor are either low impedance nodes. This fact ensures reduced swing of node voltages. As a result, the use of an analog differentiator is not expected to cause any significant second-, third-, or higher-order harmonics.

There are some trade-offs when designing the tilted comparator and the differentiator. The deliberately added offset and capacitor sizes must be determined considering the selectivity and stability of the circuit. The deliberately added offset of the comparator may vary due to the mismatches or dynamic conditions. It is important to ensure that the comparator offset remains sufficiently greater than 0 despite variations. If the deliberately added offset approaches to zero, there is a significant chance that errors due to static mismatch between the reference and the subchannels can be perceived as timing error, which degrades the performance of the ADC. Additionally, if the sign of the offset changes, the timing calibration will change the clock path delays incorrectly resulting in a higher timing mismatch error especially for high-frequency inputs. As a rule of thumb $V_{OStcomp} > \frac{1}{3}V_{OSdesired}$ where $V_{OStcomp}$ is the comparator offset including variations and $V_{OSdesired}$ is the desired comparator offset. Any mismatch between the input capacitors of the differentiator can be considered as additional sources of dynamic mismatch. However, the capacitor mismatches are insignificant

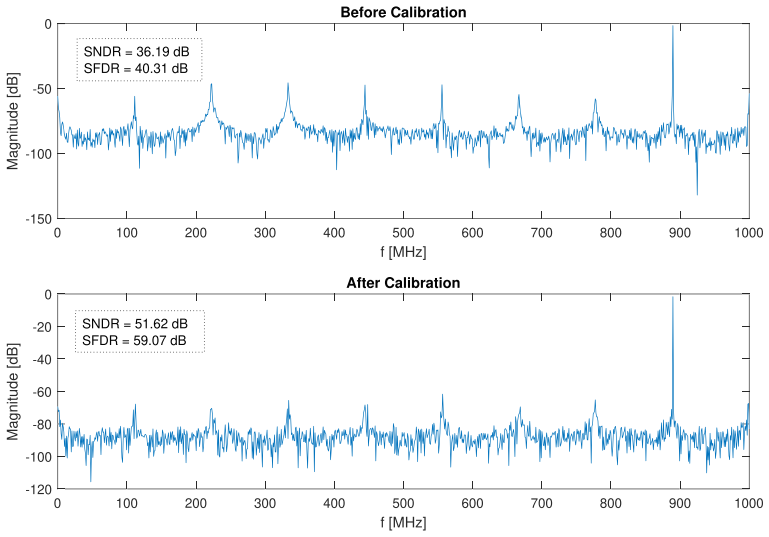

FIGURE 8 Output spectrum before and after calibration for single tone input, where $f_{in} = 889MHz, f_s = 2GHz, N = 2048$ [Colour figure can be viewed at wileyonlinelibrary.com]

with respect to the comparator offset and do not impact the timing calibration. Increasing both the high-pass capacitors and the comparator offset improves the stability without changing selectivity. However, higher high-pass capacitors at the input decrease the input bandwidth of the ADC and increase the power. These effects must be considered when determining the comparator offset and high-pass capacitors. In this study, the input high-pass capacitors are around one third of the sampling capacitance.

5 | SIMULATION RESULTS

The proposed TI-ADC is designed in 40-nm CMOS technology. The frequency spectrums of the output w/ and w/o calibration for both single tone and double tone input signals are given in Figures 8 and 9. (SNDR vs f_{in}) and (SFDR vs f_{in}) plots are given for different cases in Fig. 10. Besides, the convergence of the algorithm is seen in Figure 11. The x-axis of the figure is calibration cycle (1 calibration cycle = 19 x 18 x 500ps), and the y-axis is RMS error of the interleaved channels. The simulations are carried out at nominal process, voltage (0.9 V) and temperature (27^{o}C), and the differential input range is 1.8 V. The front-end thermal noise (kT/C) is 227μV_{RMS}, and the comparator noise from transient noise simulations is 556μV_{RMS}. The clock jitter is assumed 250 fs. The device mismatches are also included. The calibration circuit is implemented in both MATLAB and Verilog environments to see the effects. According to the simulation results, the calibrated ADC reaches 52-dB SNDR around Nyquist frequencies, which corresponds to 8.4-bit ENOB while the effect of the calibration is 2.4 bits.

Table 1 shows the comparison of TI-ADC designed in this study and few other works. "TI-SAR" stands for time-interleaved SAR ADC, and "FATI-SAR" stands for flash assisted TI-SAR ADC. The main novelty of our study is

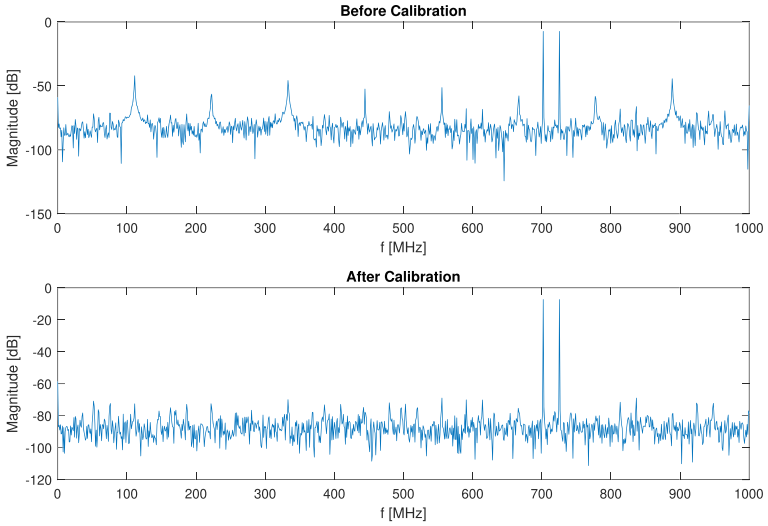

FIGURE 9 Output spectrum before and after calibration for double tone input ($f_c = 714MHz$ and $\Delta f = 23.4MHz$, $f_s = 2GHz, N = 2048$) [Colour figure can be viewed at wileyonlinelibrary.com]

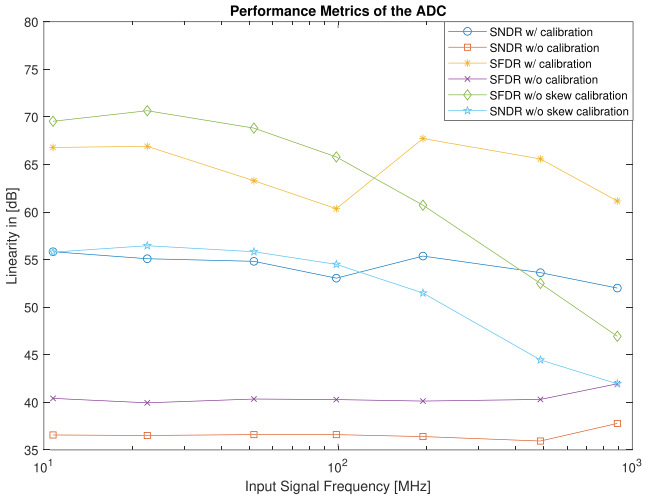

FIGURE 10 [SNDR and SFDR] versus [w/ calibration, w/o skew calibration and w/o any calibration] [Colour figure can be viewed at wileyonlinelibrary.com]

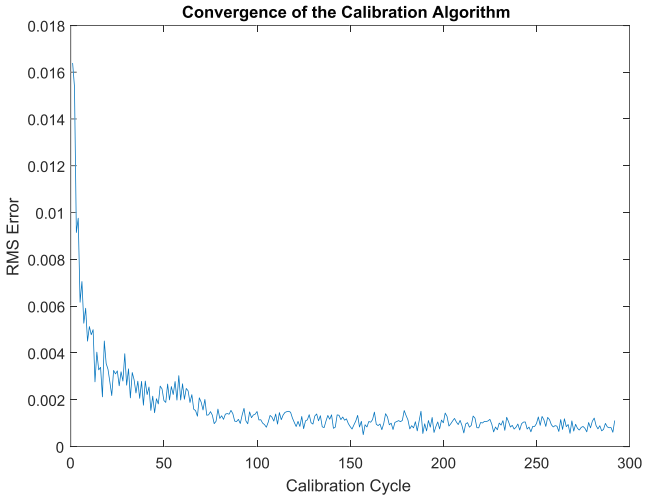

FIGURE 11 Convergence of the error between the reference and the calibrated channels [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 1 Comparison with the state of the art

Specs	[25]	[26]	[16]	[18]	[27]	[This]
Process[nm]	45	65	65	40	40	40
Speed [GS/s]	1.6	1	2.8	1.62	0.8	2
ENOB [bit]	9	8.2	*5, 8	7.7	7.7	*6, 8.4
Power [mW]	17.3	18.9	*34, 44.6	93	4.9	*6, 10.5
Type	FATI-SAR	FATI-SAR	TI-SAR	TI-SAR	TI-SAR	TI-SAR
Supply [V]	1.1	1	1.2	1.1	1.1	0.9
FOMw [fJ/conv.-step]	21	62.3	*480, 78	283	29.8	*72.8, 24.2

* without calibration.

potentially increased power efficiency. The power consumption of the ADC without calibration is 6 mW, which corresponds to 72.8fJ/conv.-step. After calibration, the total power increases to 10.5 mW, and figure of merit (FoM) becomes 24.2 fJ/conv.-step.

6 | CONCLUSION

In this study, a low-power time-interleaved SAR ADC is presented. Offset, gain, and capacitor mismatches between interleaved channels are calibrated by postprocessing the ADC output. Besides, a novel trimming-based calibration algorithm is used to calibrate the timing mismatches between channels. The calibration circuit proposes to use simple timing mismatch calibration circuits to result in power savings. Sampling speed of the ADC is 2 GS/s, and 52-dB SNDR is accomplished around Nyquist frequencies using a 40 nm CMOS technology. As a result of this implementation, the circuit is consumes 10-mW total including calibration.

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